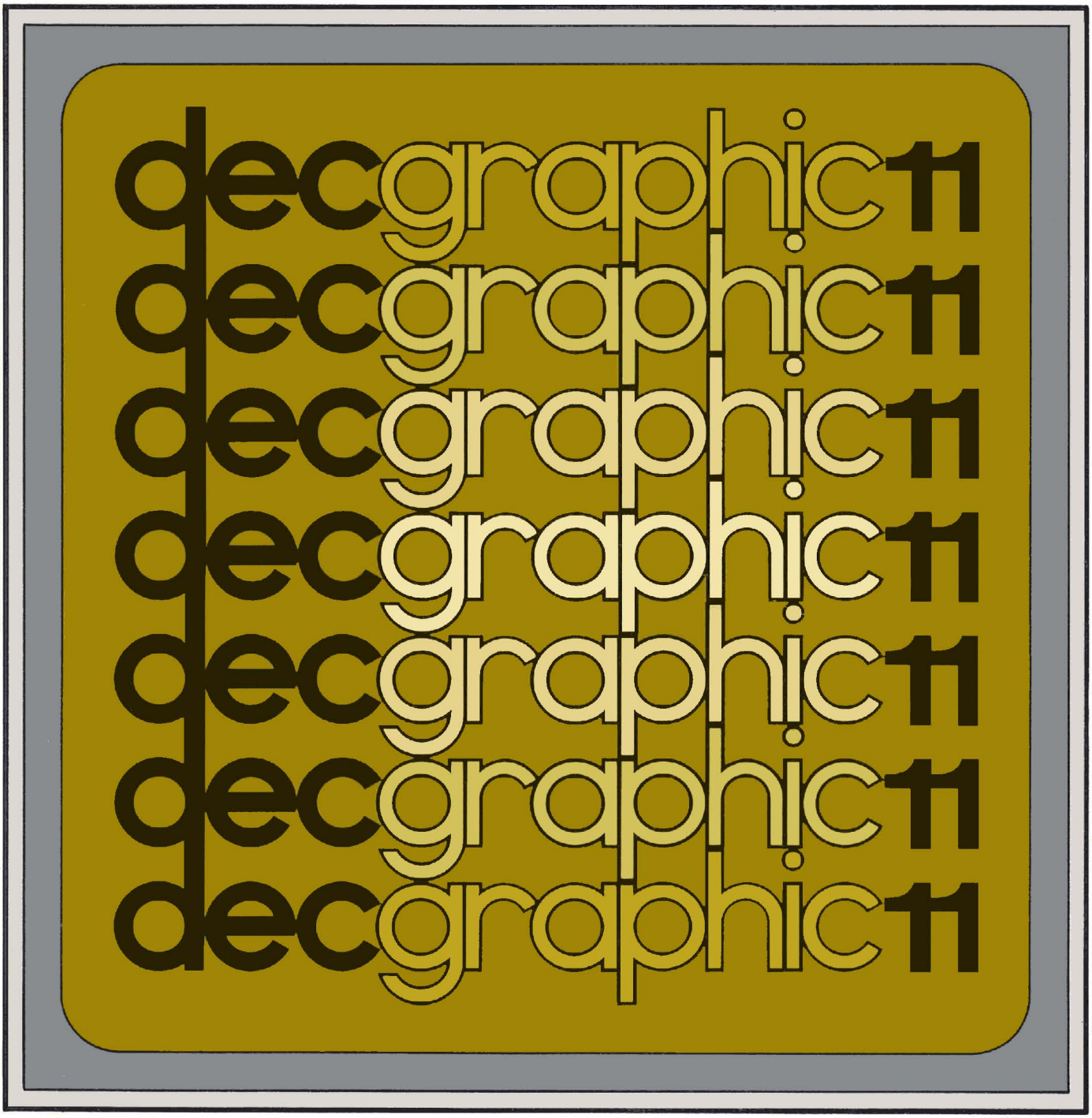
# VT11
## graphic display processor




digital

DEC-11-HVTGA-A-D

# VT11
## graphic display processor

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## ILLUSTRATIONS (Cont)



## TABLES

# CHAPTER 1
# INTRODUCTION

## 1.1 PURPOSE AND SCOPE

This manual describes the purpose and use of the VT11 Graphic Display Processor. The following information is also included: theory of operation, diagnostic programming, and maintenance information and procedures. The reader must have access to the applicable engineering drawings and documents listed in Chapter 4.

## 1.2 GENERAL DESCRIPTION

The VT11 Graphic Display Processor is a high performance display processing unit (DPU) that can operate as a peripheral to any PDP-11 series computer. It "sits" on the Unibus like any other peripheral (Figure 1-1) and can be addressed by the PDP-11 central processing unit (CPU). The VT11 Graphic Display Processor is a direct memory accessing (DMA) device, and can, if granted control of the Unibus by the PDP-11, fetch it's display program independently of the central processor. The VT11 display processor can operate with any PDP-11 compatible memory. The VT11 issues NPR requests for the Unibus. When these requests are granted, it fetches a program word from memory, decodes and executes the word, and issues another NPR so that it can fetch the next program word. All calculations necessary to execute the program are done in the display processor.

The VT11 also issues interrupts to the central processor, when it encounters an illegal character code or unresponsive memory. If enabled by a program, it will issue an interrupt when instructed to stop or when a light pen hit is sensed.

The VT11 is a stable device that requires only minimum adjustments because it employs a combination of digital and analog techniques as opposed to analog circuits alone. The vector function operates efficiently, providing a good compromise of speed and accuracy and assuring a precise vector calculation. The presentation and accumulation of vectors means that every point of a vector is available in digital form.

All beam position calculations are done digitally. After plotting each vector, the end-point position is automatically updated to the digitally calculated values preventing accumulated errors or drift. Four different vector types – solid, long dash, short dash, and dot dash – are possible through standard hardware.

The VT11 character generator has both upper and lower case capability with a large repertoire of displayable characters. The display is the automatically refreshing type rather than the storage type so that a bright, continuous

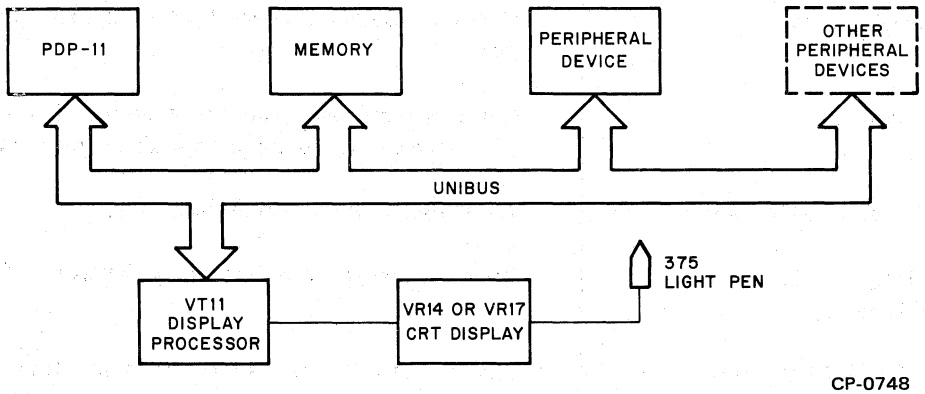



Figure 1-1 VT11 Graphic Display Processor in System Configuration

image, with excellent contrast ratio, is provided during motion or while changes are being made in the elements of the picture. A hardware blink feature is applicable to any characters or graphics drawn on the screen. A separate line clock input to the display processor permits the VT11 to be synchronized to line frequency.

The VT11 includes logic for descender characters such as "p" and "g", positioning them correctly with respect to the text line. In addition to the 96 ASCII printing characters, 31 special characters are included which are addressed through the shift-in/shift-out control codes. These special characters include some Greek letters, architectural symbols, and math symbols. Characters can be drawn in italics simply by selecting the feature through the status instruction bit. Eight intensity levels permit the brightness and contrast to be varied so that the scope can be viewed in a normally lighted room.

The instruction set consists of five control instructions and six data formats. The control instructions set the mode of data interpretation, set the parameters of the displayed image, and allow branching of the instruction flow. Data can be interpreted in any of six different formats, allowing multiple tasks to be accomplished efficiently from both a core usage and time standpoint. The graph/plot feature of the VT11 automatically plots the x or y axis according to preset distances as values for the opposite axis are recorded.

The VT11 will drive either the VR17 or VR14 CRT. The VR17 is identical to the VR14 except that it has a larger display screen. A 375 Light Pen, which plugs into the VR14/VR17 front panel, allows operator-processor interaction.

Power for the VT11 is obtained from external sources. Power to drive the analog circuitry is obtained from the VR14/VR17. This is in the form of ±22 V, which is regulated down to ±15 V in the VT11. The +5 V needed to drive the VT11 TTL logic is obtained from the PDP-11 power supply. The PDP-11 power supply also provides +15 V used by the display processor clock.

## 1.3 PHYSICAL DESCRIPTION

Table 1-1 lists the items that comprise the VT11 Graphic Display Processor.

The VT11 Graphic Display Processor is shown in Figure 1-2. The items listed in Table 1-1 are called out, as well as Unibus connection slots.

## 1.4 VT11 SPECIFICATIONS

Power Input

8 A at +5 V
100 mA at +15 V
500 mA at +22 V
500 mA at -22 V

**Table 1-1**
**Components of VT11 Graphic Display Processor**

| Item | Function |
|---|---|
| VT11 Backplane, DEC part no. 7009450 | Interconnects VT11 logic modules. |
| M7013 hex-height module | Contains timing, character control, and instruction decode logic. |
| M7014 YA hex-height module | Contains address decode, Unibus control, and vector control logic. |
| A320 hex-height module | Contains vector and character generators, beam position registers, ±15 V regulator, and digital-to-analog converters. |
| Scope Cable, DEC part no. 7009449 | Interconnects A320 module and CRT. |
| Power Harness, DEC part no. 7009099 (or 7009563 *) | Connects power and power supply signals to VT11. |
| Electromagnetic Shield, DEC part no. 17-00021-00 | Shields DACs on A320 module from electromagnetic interference. |

* required in some configurations

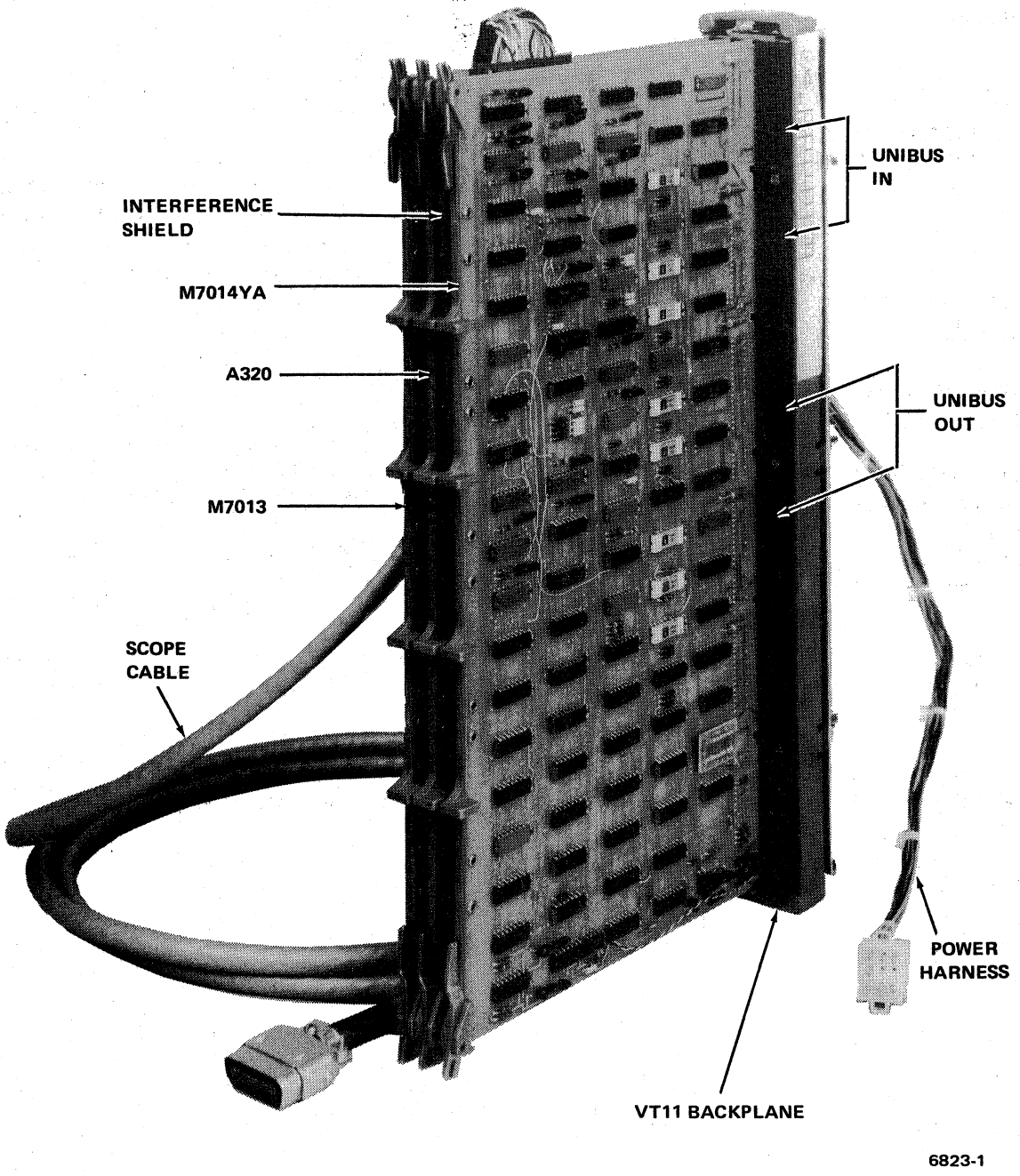



Figure 1-2 VT11 Graphic Display Processor

Instruction Word Length
16 bits

Raster Definition
10 bits

Viewable Area
x = 1024 ($1777_8$) raster units
y = 768 ($1377_8$) or 1024 ($1777_8$) raster units

Paper Size
12 bits

Hardware Blink
Programmable

Hardware Intensity Levels
8

Line Frequency Synchronization
Hardware programmable

Character Font
6 X 8 dot matrix

Characters/Line
73 (85 possible)

Number of Lines
31 on VR14 (29 possible), 42 on VR17 (39 possible)

Character Set
96 ASCII – upper and lower case plus 31 specials (Greek letters, math symbols, etc.) (Refer to Appendix A)

Control Characters
Carriage return
Line feed
Backspace

Italics
Hardware programmable

Line Type
Solid
Long dash
Short dash
Dot-dash

Data Formats
Character (2 char/word)
Short Vector (1 word)
Long Vector (2 words)
Point (2 words)
Relative Point (1 word)
Graphplot x/y (1 word/pt)

DPU Instructions
Set Graphic Modes
Jump
No operation (NOP)
Load Status Register A
Load Status Register B

# CHAPTER 2
# THEORY OF OPERATION

## 2.1 INTRODUCTION

This chapter provides the user with the operational theory needed to understand and maintain the VT11 Graphic Display Processor. The description in the following paragraphs is intended to present the reader with information necessary to understand normal system operation. Understanding this information is a prerequisite in analyzing trouble symptoms and determining necessary corrective action.

A complete set of engineering drawings and circuit schematics is provided with the VT11. The general logic symbols used on these drawings are described in the *DEC Logic Handbook*, 1971. Specific symbols and conventions are also included in the *PDP-11 Conventions Manual*, DEC-11-HR6B-D, and in certain PDP-11 system manuals. Instruction flow diagrams for both control instructions and data words are also included in the engineering drawing set. The purpose of the flow diagrams is to illustrate the sequential operations that take place when instructions and data words are executed. The individual steps in the diagrams itemize events or conditions that are necessary to complete the entire instruction. They also provide keys as to where the applicable logic is located in the drawing set. Only the main operations and decisions are shown however, in order that the diagrams not be over-detailed and therefore cumbersome. More detailed flow diagrams are also included in this manual, where necessary, to explain complex procedures. The following paragraphs describe the signal nomenclature conventions used on the drawing set.

Signal names in the VT11 print set are in the following basic form:

SOURCE SIGNAL NAME POLARITY

SOURCE indicates the drawing number of the print set where the signal originates. The drawing number of a print is located in the lower righthand corner of the print title block (VC1, SABR, DCR, etc.).

SIGNAL NAME is the name proper of the signal. The names used on the print set are also used in this manual for correlation between the two.

POLARITY is either H or L to indicate the voltage level of the signal: H means +3 V; L means ground.

For example, the signal:

VC2 VEC GEN OP DONE H

originates on sheet 8 of the M7014YA module drawing and is read, "when VEC GEN OP DONE is true, this signal is at +3 V."

Unibus signal lines do not carry a SOURCE indicator. Except for the grant lines, these signal names represent a bidirectional wire-ORed bus; as a result, multiple sources for a particular bus signal exist. Each Unibus signal name is prefixed with the word BUS.

In text, references to a specific engineering drawing are in abbreviated form. For example "drawing M7014YA-LEI" refers to drawing D-CS-M7014YA-0-1, sheet 9, Light Pen Edge and Intensity Logic.

## 2.2 VT11 DISPLAY PROCESSOR

### 2.2.1 Introduction

The VT11 Display Processor circuitry is contained on three hex-height modules: A320, M7013, and M7014YA. The M7013 contains timing, instruction decode, and character control logic while the A320 possesses the vector generator logic, analog circuitry, and interfaces with the display monitor. The M7014YA module contains the Unibus interface and control, vector control, and address decode logic. The functions of the three modules are so integrated that separate descriptions are precluded; in an operational sense they can be considered one module.

Capable of executing its own display program, the display processor, once started, can function independently. It requires only the granting of non-processor requests (NPR) by the PDP-11. The display program is updated by the PDP-11, as dictated by the overall objective of the program, in order to effect a timely display. However, this function is not necessary, in itself, for display processor operation.

The graphic oriented set of five versatile instructions provides the basis for a very proficient display program. This program, containing the data and commands necessary to produce a CRT display, is stored in the memory. It is transferred, as the result of NPRs, one word at a time via the Unibus to the display processor.

Once brought into the display processor, the data words and instructions are decoded and stored. The signals necessary to execute the instructions are developed, vector and character calculations are made, and outputs to the CRT display are generated. This, in brief terms, is the primary role of the VT11 Display Processor. Drawing D-BD-GT40-0-4 is a block diagram of the display processor.

### 2.2.2 Initialization

The first signal input to the VT11 Display Processor is BUS INIT L. It is asserted, when power is applied to the system, by pressing the START switch on the PDP-11 console, or by issuing a programmed RESET instruction. This signal sets all logic to the appropriate initial states, e.g., clears the Display Program Counter (DPC) and any flags that are set.

### 2.2.3 Starting the Display Processor

Starting the display only requires the addressing of the display processor's DPC followed by the transfer of data into the DPC. Briefly, the start sequence begins when the PDP-11 places the address of the DPC (772000) on the Unibus address lines and data on the Unibus data lines; the data is then loaded into the DPC. Decoding the DPC address in the M7014YA address selection logic automatically starts the display. The VT11 is subsequently granted an NPR, becomes bus master, and the data that was loaded into the DPC is placed on the Unibus address lines to the memory. This results in the retrieval and transfer to the VT11 of the first instruction in the display program; display operation has begun. A more detailed description of this operation, and the particular signals generated, is contained in the following paragraph.

Table 2-1
**VT11 Hardware Registers**

| Register | Unibus Address* | CPU Operation | Contents | Bit |
|---|---|---|---|---|
| Program Counter | 772000 | Read/Write | Address of next word in display file | (15:0) |
| Status Register | 772002 | Read Only | Stop Flag | (15) |
| | | | Mode | (14:11) |
| | | | Intensity | (10:8) |
| | | | Light Pen Flag | (7) |
| | | | Shift Out | (6) |
| | | | Edge Indicator | (5) |
| | | | Italics | (4) |
| | | | Blink | (3) |
| | | | Spare (Not Used) | (2) |
| | | | Line | (1:0) |
| X Position & Graphplot Increment | 772004 | Read Only | X Position | (9:0) |
| | | | Graphplot Increment | (15:10) |
| Y Position & Character | 772006 | Read Only | Y Position | (9:0) |
| | | | Character Register | (15:10) |

*The two high order bits are forced to a 1 to assert an MSD = 7.

### 2.2.4 Address Selection

Decoding of Unibus addresses is the function of the M7014YA address selection logic (drawing M7014YA-ASL). The only recognizable addresses are those of the four hardware registers in the VT11 (Table 2-1); all other bus addresses are invalid as far as the VT11 is concerned. The initiation by the CPU of any display processor operation is dependent on the decoding of a valid address from the Unibus.

The CPU can read the contents of all four hardware registers, but only the DPC can be written into. Bus control bit C1 determines whether the operation is a read (Bus C1 a logic high) or write (Bus C1 a logic low). As indicated in Table 2-1, address bits 1 and 2 are used to identify the particular registers; the other bits are the same for all four registers.

Read and write functions begin when the CPU places the display processor register address on the bus address lines and transmits BUS MSYN L. As originated in the PDP-11, the VT11 address equals 17200X. However, the two high-order address bits are forced to a 1 on the Unibus, asserting an address of 77200X. Of the 17 address bits that are decoded (bit 0 is not considered), eleven, BUS A (12:11, 09:01) L, are input to the display processor through three 8838 Bus Transceivers and six, BUS A (17:13, 10) L, bypass the transceivers. (The bit 10 input to the transceivers is not used.)

As shown on drawing M7014YA-ASL, the bus transceivers are also employed when the VT11 becomes bus master and places the first twelve bits of the DPC [PCC PC (12:01) H] on the bus address lines. The routing of the Unibus address and data bits is shown in Figure 2-1.

The lower order address bits [ASL (12, 9:3) H] are input to 8242 Exclusive-NOR comparator gates in the decoding circuit. These gates require the correct address jumper configuration at their second inputs. Table 2-2 lists the jumpers and shows their relationship to the addressing scheme. The common output of the Exclusive-NOR gates must be a logic high in order for the Unibus address to be recognized. Therefore, none of the gates can be enabled. If a jumper is in place, a 0 input (a logic low at this point) disables the gate. Likewise, 1 bits disable those gates where the jumper has been removed. Note that address bits 10 and 11 are not decoded with address jumpers. BUS A 10 L is decoded directly from the Unibus; ASL BA 11 L enters the decoder circuit at a later point.

**Table 2-2**
**Address Jumper Configuration**

| Unibus Address | Address Bits | State | Address Jumper | Jumper Condition |
|---|---|---|---|---|
| | BUS A 17 L | 1 | | |
| 7 | 16 | 1 | | |
| | 15 | 1 | | |
| | 14 | 1 | | |
| 7 | 13 | 1 | | |
| | 12 | 1 | W11 | OUT |
| | 11 | 0 | | |
| 2 | 10 | 1 | | |
| | 9 | 0 | W13 | IN |
| | 8 | 0 | W16 | IN |
| 0 | 7 | 0 | W19 | IN |
| | 6 | 0 | W17 | IN |
| | 5 | 0 | W18 | IN |
| 0 | 4 | 0 | W14 | IN |
| | 3 | 0 | W12 | IN |
| | 2 | X | | |
| X | 1 | X | | |
| | 0 | X | | |

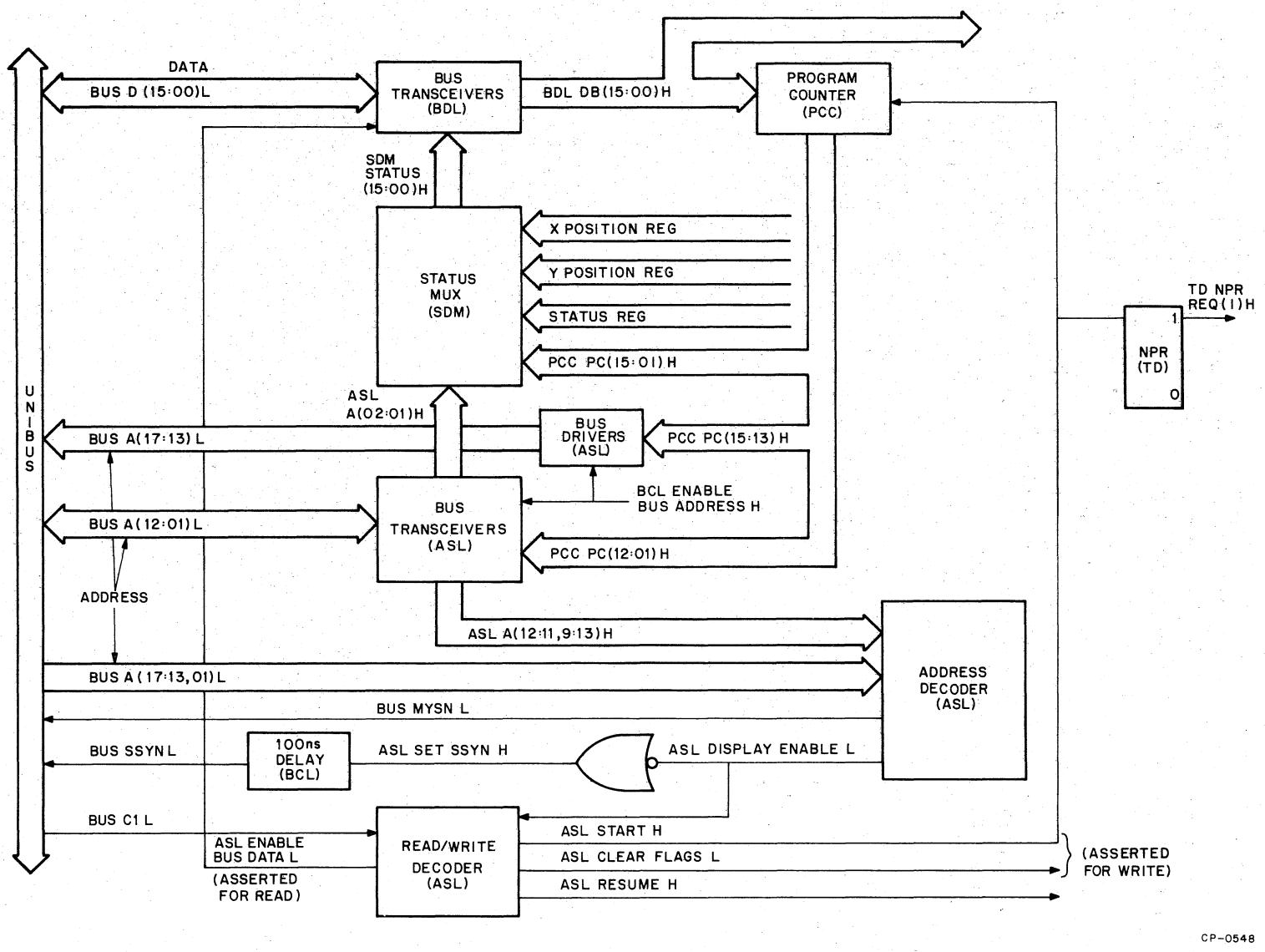



Figure 2-1 Unibus Address and Data, Block Diagram

The remaining address bits [BUS A (17:13, 10) L], along with BUS MSYN L, are sent directly from the Unibus to a type 314, 7-input AND gate in the decoder. The output of this gate is ANDed with the high common output of the Exclusive-NOR gates to assert ASL DISPLAY ENABLE L. BUS MSYN L is sent by the PDP-11 (about 150 ns after the address is placed on the Unibus) to initiate a read or write operation in the VT11 Display Processor.

ASL DISPLAY ENABLE L performs two functions: first, it causes ASL SET SSYN L, and consequently BUS SSYN L, to be asserted; second, it is ANDed with BUS C1 L to generate internally used signals necessary to execute a read or write request from the PDP-11. BUS SSYN L notifies the PDP-11 that the request (BUS MSYN L) and address have been accepted and that data has been received from the Unibus data lines (write to DPC) or placed on the Unibus lines (read). In generating BUS SSYN L, ASL SET SSYN L is input to a circuit (drawing M7014YA-BCL) consisting of a 74123 Monostable Multivibrator and a 7474 D-type flip-flop that function together as a 100-ns delay. The delay allows time for read data to be transferred through the transceiver gates and become settled on the Unibus before it is strobed by the PDP-11. Similarly, during a write operation the delay is needed before the display processor acknowledges receipt of data from the Unibus. BUS SSYN L, during both read and write operations, causes the PDP-11 to drop BUS MSYN L from the Unibus; this terminates the transfer operation. However, other events take place in the display processor while this delay is timing out.

ASL START H, one of the signals generated when the condition of BUS C1 L (a low) specifies a write operation, causes the data on the Unibus data lines to be gated into the DPC and sets the NPR flip-flop in the M7013 module in preparation for an NPR request to the PDP-11. Note that ASL START H can only be asserted when address bits 1 and 2 [BUS A (02:01) L] both equal 0, which specifies the DPC, and data bit 0 = 0 (BDL DB 00 L), because only even data inputs to the DPC are valid (this data, in turn, becomes an address directed to the memory). When BUS C1 L is a logic high, indicating a read is to take place, ASL DISPLAY ENABLE L generates ASL ENABLE BUS DATA L. This latter signal gates the data (DPC, Status Register, X Position Register, or Y Position Register) from the Status Multiplexer onto the Unibus data lines by way of the bus transceivers (Paragraph 2.2.4.1). Figure 2-2 shows the timing for these operations and signals.

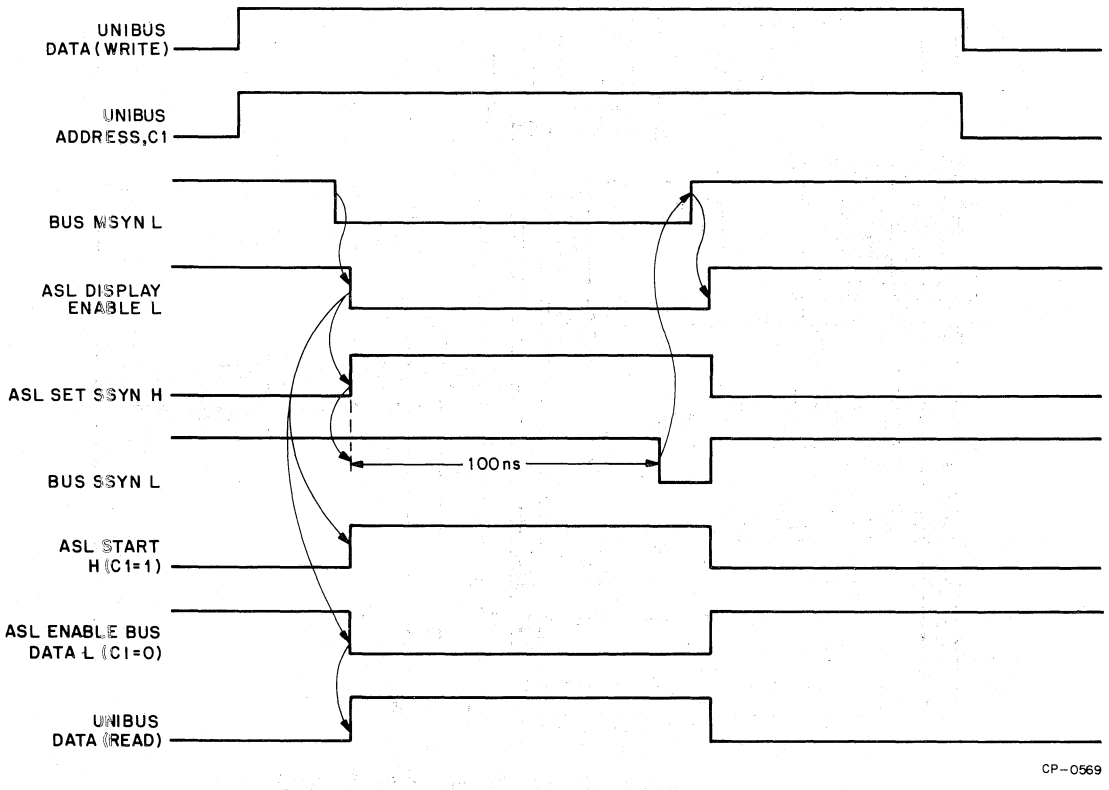



Figure 2-2 Unibus Transfer Timing

**2.2.4.1 Reading Status** – Although capable of writing into only one register (DPC) in the VT11, the PDP-11 can read the contents of four registers (DPC, X Position Register, Y Position Register, and Graphplot Increment Register) and the state or status of 21 other flip-flops and signals. Called reading status, the CPU uses this operation to determine the condition of VT11 registers and signals.

As stated previously, read and write operations are decided by the state of control bit C1. When reading status, the PDP-11 places the address (Table 2-1) and BUS C1 L on the Unibus followed by BUS MSYN L. The address is decoded and, if valid in the VT11, is ANDed with BUS MSYN L to assert ASL DISPLAY ENABLE L. The latter signal is then ANDed with BUS C1 L, a logic high, to assert a second signal, ASL ENABLE BUS DATA L. The two low-order address bits [ASL A (02:01) H] are used to select which of the four, 16-bit inputs to the Status Multiplexer (M7013-SDM) are to generate SDM STATUS (15:00) H. These 16 bits are then gated to the Unibus via the bus transceivers (M7014YA-BDL) by ASL ENABLE BUS DATA L. The Status Multiplexer is composed of eight Type 74153, dual, 4-to-1 multiplexer chips. They are shown as the top two rows of chips in drawing M7013-SDM; Figure 2-3 is a simplified diagram of the reading status logic including the multiplexer.

**2.2.5 NPR Data Requests**

Operation of the VT11 Display Processor is a function of the display program stored in the memory. Retrieval of instructions in this program is effected when the PDP-11 responds to NPRs that originate in the display processor and allows the display processor to become bus master. At this time, the display processor transmits, via the Unibus, a request for data (BUS MSYN L) and memory address of the data. The arrival of the data from memory initiates a timing sequence that terminates in the assertion of the next NPR and the process is repeated.

The initial NPR is generated when the signal ASL START H sets the NPR flip-flop (drawing M7013-TD). ASL START H also loads the DPC with the memory address of the first instruction in the display program (drawing M7014YA-PCC). (This sequence is described in Paragraph 2.2.4.) With the NPR flip-flop set, BCL NPR (1) H is ANDed with the outputs from two 7474 flip-flops (S+BSY and $\overline{S}$·BSY) to assert BUS NPR L (drawing M7014YA-BCL and Figure 2-4). This signal on the Unibus indicates that the display processor desires control of the bus, i.e., to become bus master. The PDP-11 acknowledges the NPR by placing a grant signal, BUS NPG IN H, on the Unibus to denote that control will be relinquished to the requestor (the display processor in this case) at the conclusion of the present bus cycle.

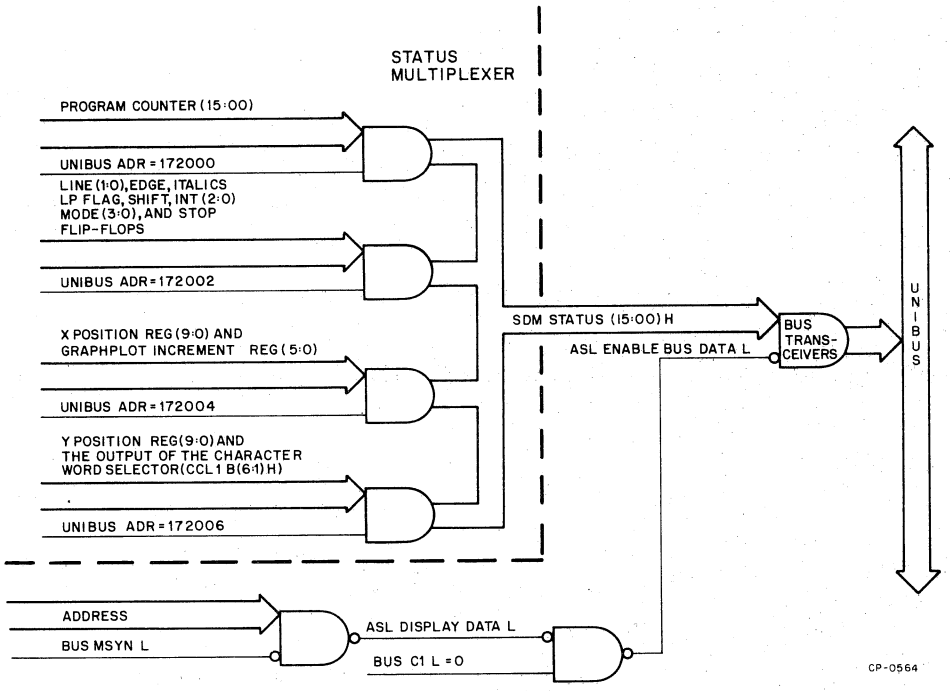



Figure 2-3 Reading Status, Block Diagram

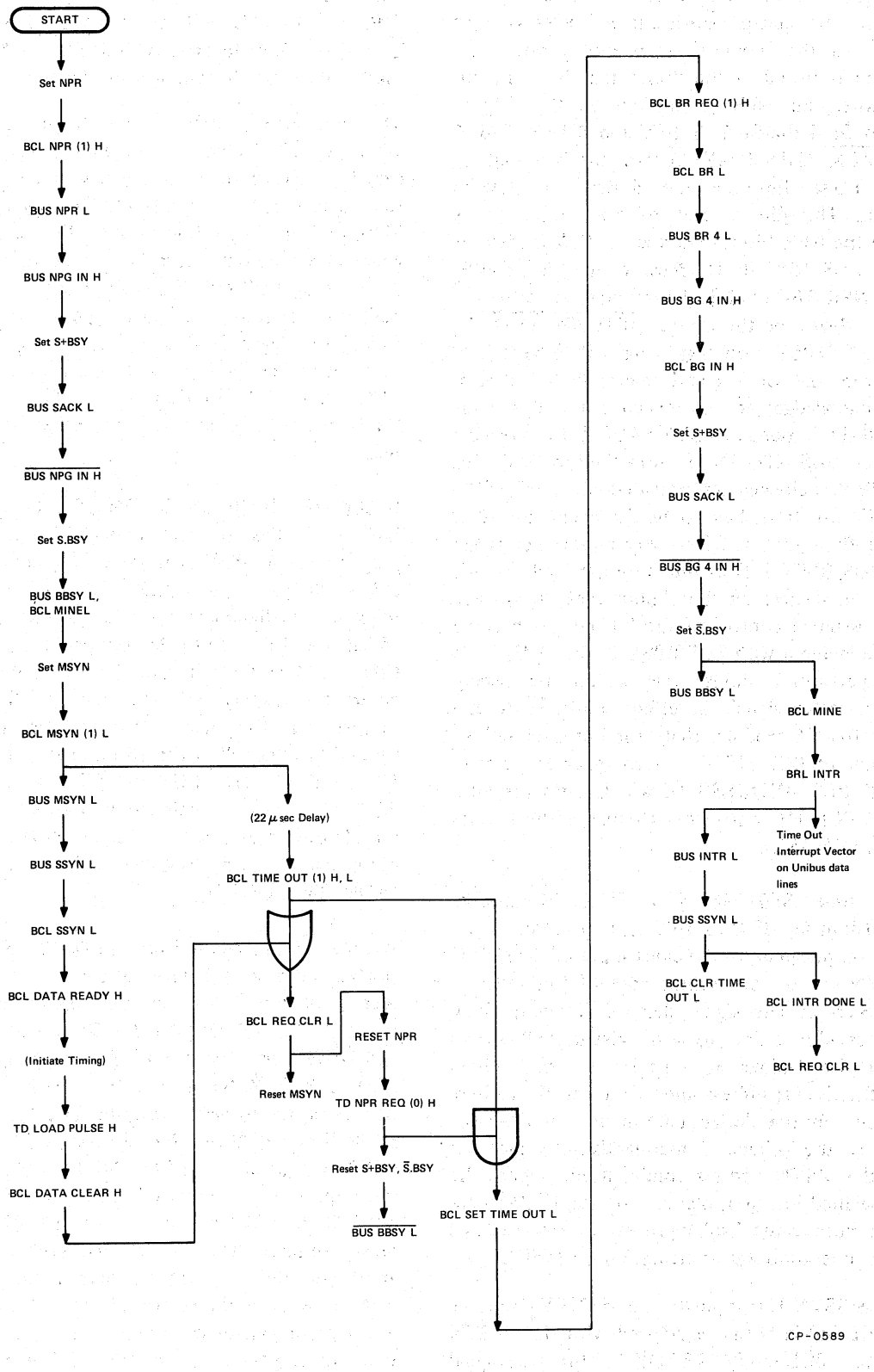



Figure 2-4 NPR/Time Out Interrupt, Flow Diagram

The VT11 Display Processor now obtains control of the Unibus and can issue control signals and addresses to other (slave) devices on the Unibus. The memory, where the display program is stored, is the device that is communicated with when an NPR is granted to the display processor. Two 7474 flip-flops, S+BSY and $\overline{S}$·BSY (SACK OR BUSY, SACK AND BUSY) control the handshaking that ensues. These flip-flops are shown on drawing M7014YA-BCL. The direct reset to both flip-flops is dropped when the NPR flip-flop is reset. S+BSY is then set on receipt of BUS NPG IN H. Because there is an NPR pending [BCL NPR REQ (1) H], the bus grant is not passed on to the next device on the Unibus (BUS NPG OUT H). The 1 output of S+BSY, now high, causes BUS NPR L to be dropped from the Unibus and asserts BUS SACK L (Selection Acknowledge) to acknowledge the bus grant signal. The PDP-11 responds to BUS SACK L by dropping the grant signal, BUS NPG IN H, from the bus. With this input low, $\overline{S}$·BSY is clocked set, provided both BUS SSYN and BUS BBSY are false. Several results occur now that both 7474 flip-flops are set. Of primary importance is the assertion of BUS BBSY L (Bus Busy) on the Unibus. This signal notifies all devices on the Unibus that the display processor has assumed control of the bus (it has become bus master). Coincident with BUS BBSY L, BCL MINE L is generated to perform a similar role within the display processor. This latter signal, in effect, indicates to the M7013 and M7014YA modules that "the bus is mine." An immediate result of BCL MINE L is to generate a signal, BCL ENABLE BUS ADDRESS H, which gates the DPC [PCC PC (15:00) H] onto the Unibus address lines (drawing M7014YA-ASL).

At the same time, SET MSYN, a 74123 Monostable Multivibrator (drawing M7014YA-BCL), is triggered generating a 100-ns output pulse to the clock input of the MSYN flip-flop. MSYN sets on the trailing edge of this pulse to assert BUS MSYN L. This signal, delayed 100 ns to allow time for the bus address lines to settle, instructs all devices connected to the Unibus to respond to the address presently on the Unibus address lines. However, the address is recognized in only one device, core memory in this case, and ignored by the others. Consequently, the memory responds to the MSYN address combination, fetches the data at the specified location, places it on the Unibus data lines, and then notifies the display processor (after a 100-ns delay) of this operation by asserting BUS SSYN L.

The signal BUS SSYN L is input to the M7014YA module and asserts BCL SSYN H that is ANDed with BCL MSYN (1) H to generate BCL DATA READY L. This latter signal is used to start the timing in the M7013. One of these timing signals (Paragraph 2.2.6), TD LOAD PULSE H, asserts BCL DATA CLEAR H. This signal asserts BCL REQ CLR L, which resets the MSYN and NPR flip-flops. Consequently, TD NPR REQ (0) H resets the S+BSY and $\overline{S}$·BSY flip-flops to drop BUS BBSY and BCL MINE L; the display processor is no longer bus master.

The sequence described above is the normal chain of events when an NPR is issued. However, it is possible that the signals to the slave can go unanswered, e.g., if the address sent to memory is nonexistent. The time out circuit on the M7014YA module (drawing M7014YA-BCL) is designed to generate a time out interrupt if this situation should occur. At the time BUS MSYN L was placed on the Unibus, BCL MSYN (1) H allowed a 22 $\mu$s, type 74123 delay (Time Out Delay) to trigger. If BUS SSYN L is not returned within 22 $\mu$s after MSYN is asserted, the delay times out and the BCL Time Out flip-flop is set. The NPR and MSYN flip-flops are then reset, as is normally the case, freeing the bus.

In addition, the BCL SET TIME OUT L signal is asserted to initiate the bus request sequence via the priority jumper plug on the M7014YA module; this concludes with BUS BR 4 L being output to the PDP-11 (Figure 2-5). The bus request is evaluated in the CPU priority arbitration logic, and if found to have the highest priority, causes a bus grant (BUS BG 4 IN H) to be issued to the Unibus. The bus grant enters the display processor through the same priority jumper plug to generate BCL BG IN H which sets the S+BSY flip-flop. With this flip-flop set, and a BR in effect [BCL BR (1) H], BUS BG OUT H to the Unibus is inhibited; a delay in this circuit allows time for S+BSY to set. (If there was a priority jumper plug for a priority level other than 4 present, BUS BG 4 IN H would be direct wired to BUS BG 4 OUT H.)

Another output to the Unibus, BUS SACK L, is asserted by the display processor when BCL BG IN H sets S+BSY. On receipt of this bus grant acknowledgment, the PDP-11 drops BUS BG 4 IN H and $\overline{S}$·BSY set. With both S+BSY and $\overline{S}$·BSY set, the display processor again becomes bus master; BUS BBSY L and BCL MINE L are asserted. Because a bus request is pending, BCL MINE L asserts BRL INTR H and BUS INTR L (drawing M7014YA-BRL). BRL INTR H is gated with BCL TIME OUT (1) H to generate an interrupt vector address of 330 on the Unibus data lines [BUS D (08:00) L]. Jumpers W7, W8, W9, W10, and W15 must also be of the correct configuration (Table 2-3) before any vector address can be output to the Unibus. The PDP-11 reads in the vector address, which results in entry into a particular software routine, and transmits BUS SSYN L to the display processor. BCL SSYN H is then ANDed with BRL INTR H (drawing M7014YA-BCL) to generate BCL INTR DONE H and BCL CLR TIME OUT H; this concludes the time out interrupt operation.

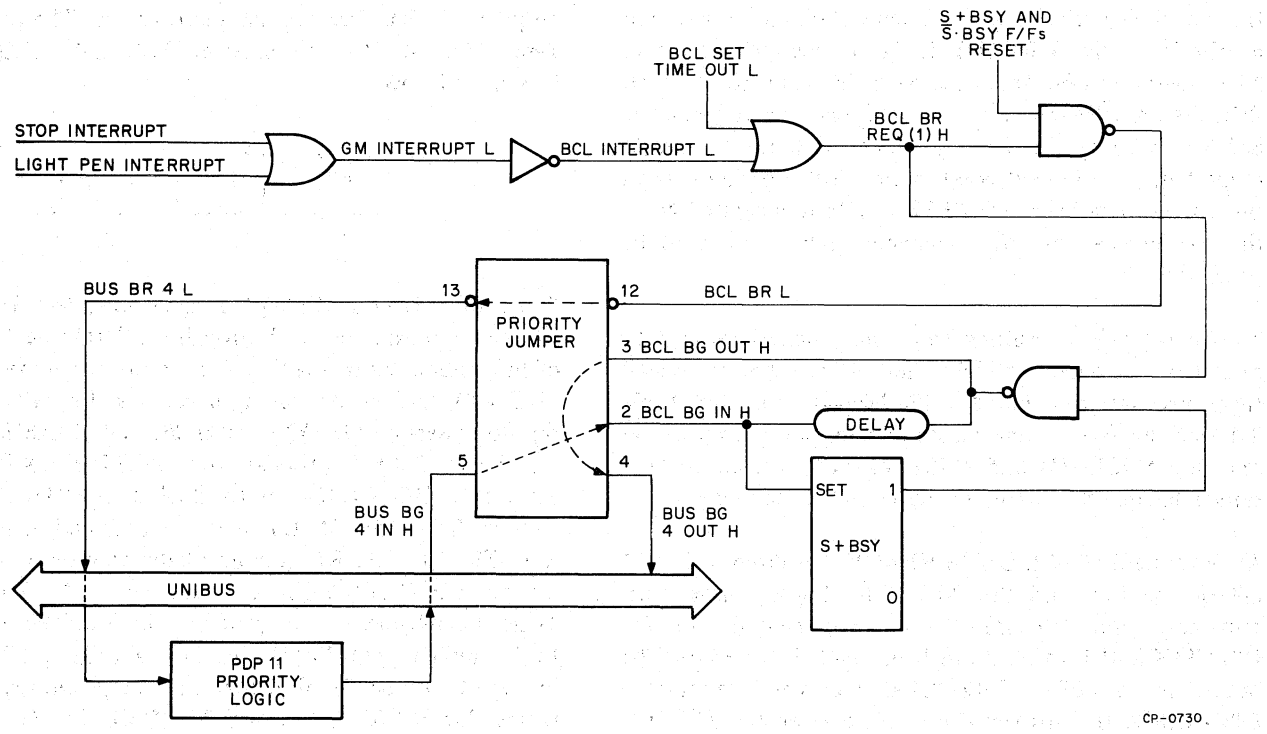



Figure 2-5 Bus Request and Bus Grant, M7014YA Module

**Table 2-3**
**Interrupt Vector Addresses**

| Jumpers | Bus DXX L | Stop INT Vector | Light Pen INT Vector | Char INT and Time Out INT Vector |
|---|---|---|---|---|
| W8-OUT | 08 | 0 | 0 | 0 |
| W7-IN | 07 | 1 | 1 | 1 |
| W10-IN | 06 | 1 | 1 | 1 |
| W15-OUT | 05 | 0 | 0 | 0 |
| W9-IN | 04 | 1 | 1 | 1 |
| – | 03 | 0 | 0 | 1 |
| – | 02 | 0 | 1 | 0 |
| – | 01 | 0 | 0 | 0 |
| – | 00 | 0 | 0 | 0 |
| Interrupt Vector Address | | $320_8$ | $324_8$ | $330_8$ |

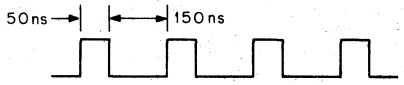
### 2.2.6 Timing

Internal timing for the VT11 Display Processor is initiated by the BCL DATA READY L signal generated during an NPR operation (Paragraph 2.2.5) or by TD RESTART H. BCL DATA READY L is generated when memory asserts SSYN, notifying the Display Processor that the data it requested, i.e., the next word of the display program, is on the Unibus data lines. TD RESTART H is generated when the second character of a character data word is to be processed.

The timing pulses resulting from these signals are used to gate data, increment the DPC, and effect other controlled functions that are required in the Display Processor. Table 2-4 lists the four timing pulses. Timing logic is shown on drawings M7013-TD and M7014YA-PCC. Figure 2-6 is a timing diagram for the timing pulses and related signals.

At the time that BCL DATA READY is asserted, the 7474 D-type flip-flop and the 7473 J-K flip-flop have been previously reset. TD TIME ON L is not asserted, and PCC DIS CLOCK H is gated through the 7400 NAND gate. The output at pin 3 of the 7400 NAND gate is an inverted PCC DIS CLOCK H. This signal will cease when the 7473 J-K flip-flop is set.

PCC DIS CLOCK H originates in a 20-MHz, crystal controlled, clock pulse generator in the M7014YA module (drawing M7014YA-PCC). Input through a jumper (W24) to the first of two 74S74 D-type flip-flops that operate as frequency dividers, the 20-MHz signal generates PCC ANALOG CLOCK H (10-MHz). The second flip-flop outputs a 5-MHz free running pulse stream. The two clock signals are ANDed to produce PCC DIS CLOCK H, illustrated below.




When BCL DATA READY L goes low, two PCC DIS CLOCK H pulses are gated through the 7402 gate. The first of these pulses clears the 74193 4-bit binary counter (TIME CNT UP), and on its trailing edge, sets the 7474 D-type flip-flop asserting TD SYNC UP H. PCC DIS CLOCK H now sets the 7473 J-K flip-flop asserting TD TIME ON H, which gates PCC DIS CLOCK H to clock the TIME CNT UP counter. TD TIME ON L is now low and inhibits the 7402 gate. The R0, R1, R2 outputs of the counter, along with the gated PCC DIS CLOCK H, activate a 74155 1-line to 4-line demultiplexer, to produce the four time states: LOAD MODE, LOAD PULSE, TP1, and TP2. TP2 resets the 7474 D-type flip-flop that was set previously, terminating TD SYNC UP H and TD TIME ON H, thereby inhibiting further up counting of the binary counter. The timing decoder will now remain in a quiescent state until the next DATA READY or RESTART signal. When TD RESTART H triggers the generation of timing pulses, it presets the binary number two into the TIME CNT UP counter. Therefore LOAD MODE and LOAD PULSE are not generated.

**Table 2-4**
**VT11 Display Processor Timing Pulses**

| Signal | Use |
|---|---|
| TD LOAD MODE A | Strobe data from Unibus data lines. |
| TD LOAD PULSE H | Gate data into the Data Mode, Control Mode and other registers; resets MSYN. |
| TD TP1 H | Increment the DPC. |
| TD TP2 H | Generates another NPR (if not inhibited) or initiates a character, point, graph, or vector. |

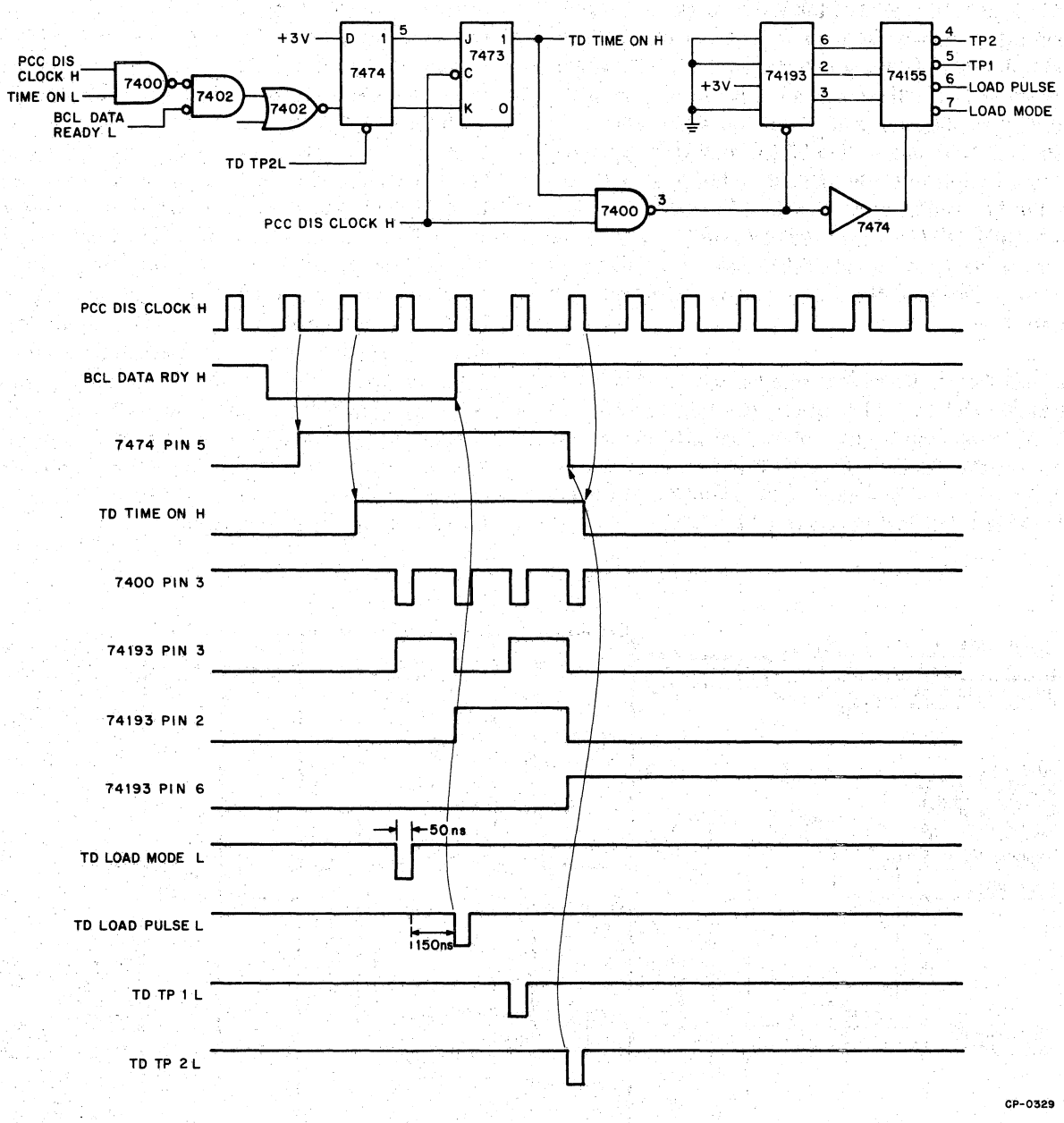



Figure 2-6 Display Processor Timing Diagram – M7013 Module

### 2.2.7 Display Processor Mode Control

The mode control logic in the M7013 module (drawing M7013-MD and Figure 2-7) is used to identify the information currently on the Unibus data lines and generate the appropriate signals required to execute the specified operation. A series of timing pulses is generated (Paragraph 2.2.6) when an instruction or data in the display program is read from core memory and placed on the Unibus data lines. One of these pulses, TD LOAD MODE H, gates the data on the Unibus into the mode decoding logic. Depending on the bit configuration (Table 2-5) of the five high order bits [BDL DB (15:14) H and SDM DB (14:11) L] the bus data is decoded as an instruction or as data; an instruction is further defined as a control instruction or a data instruction.

Unibus data bit 15 determines whether data on the bus is an instruction (bit 15 = 1) or strictly data (bit 15 = 0), e.g., the X, Y coordinates that follow an instruction, are presently on the bus data lines. If an instruction is on the Unibus, bit 14 is used to denote if it is a control instruction (bit 14 = 1) or a data instruction (bit 14 = 0).

The Control Mode and Data Mode Registers hold the codes for the current operation. These codes cause signals to be asserted that will establish the operational parameters or display data on the CRT. When a control instruction (Jump, No-op, Load Status A, Load Status B) is on the Unibus, the bus bits [SDM DB (13:11) L] are clocked into the Control Mode Register; the Data Mode Register remains unchanged. However, if a data instruction, i.e., one of the Graphic Mode instructions, is decoded, the bus bits [BDL (14:11) H] are clocked into the Data Mode Register. The Control Mode Register is also clocked but all three D inputs are inhibited because bit 14 = 0. This results in the code for Set Graphic Mode (000) being stored in this register. Note that if a Jump is in effect neither of the two registers are clocked; their previous contents remain unchanged. This allows a graphic mode operation to be resumed after a Jump (which is executed for the purpose of reading data from another memory area) without requiring that the Graphic Mode instruction be respecified; the Data Mode Register still contains the code for the graphic instruction. This can result in a significant decrease in the number of instructions required in a program.

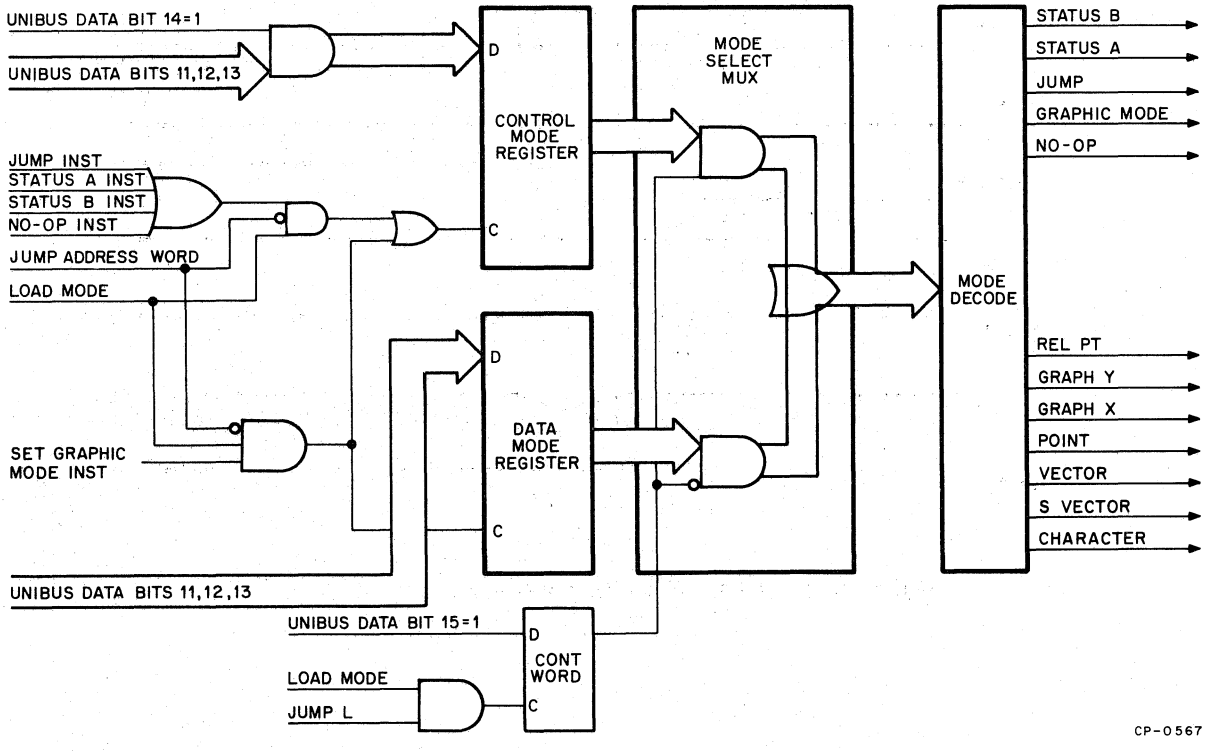



Figure 2-7 Mode Control

**Table 2-5**
**Unibus Instruction and Data Codes**

| Instruction/Data | Unibus Data Bit | | | | |
|---|---|---|---|---|---|
| | 15 | 14 | 13 | 12 | 11 |
| All Data Words | 0 | X | X | X | X |
| Set Graphic Mode | 1 | 0 | – | – | – |
| (Set Character Mode) | | | 0 | 0 | 0 |
| (Set Short Vector Mode) | | | 0 | 0 | 1 |
| (Set Long Vector Mode) | | | 0 | 1 | 0 |
| (Set Point Mode) | | | 0 | 1 | 1 |
| (Set Graph X Mode) | | | 1 | 0 | 0 |
| (Set Graph Y Mode) | | | 1 | 0 | 1 |
| (Set Relative Point Mode) | | | 1 | 1 | 0 |
| (Spare)** | | | 1 | 1 | 1 |
| * | 1 | 1 | 0 | 0 | 0 |
| SPARE** | 1 | 1 | 0 | 0 | 1 |
| SPARE** | 1 | 1 | 0 | 1 | 0 |
| SPARE** | 1 | 1 | 0 | 1 | 1 |
| JUMP | 1 | 1 | 1 | 0 | 0 |
| NO-OP | 1 | 1 | 1 | 0 | 1 |
| LOAD STATUS REG A | 1 | 1 | 1 | 1 | 0 |
| LOAD STATUS REG B | 1 | 1 | 1 | 1 | 1 |

*Serves no function except to assert MD GRAPHIC MODE H and set NPR; Data Mode Register is not loaded.

**The display processor hangs when a spare code is decoded.

Two other decoder functions take place when Unibus data bit 15 (=1) is ANDed with the same TD LOAD MODE H pulse that clocked the two mode registers. Unless the second word of a Jump instruction is about to be read (MD JMP WORD 1 L is asserted at this time) the signal MD CLR WORD L is generated when any instruction is on the Unibus data lines (bit 15 = 1). MD CLR WORD L clears the Word flip-flop (drawing M7013-PVCS); coincident with this the Cont Word (control word) flip-flop is clocked set. (The flip-flop is already set if the previous word was a control instruction.) MD CONT WORD (1) H is asserted and the contents of the Control Mode Register are gated into the multiplexer. As a result, one of the control signals (STATUS A, STATUS B, JUMP, GRAPHIC MODE, or NO-OP) is output from the mode decoder. The Cont Word flip-flop is clocked reset when one of the data words (bit 15 = 0) that follow a Graphic Mode instruction is on the Unibus. The set output from the flip-flop is now low ($\overline{\text{MD CONT WORD (1) H}}$) and the contents of the Data Mode Register are gated into the Mode Select Multiplexer; one of the graphic mode signals (POINT, VECTOR, GRAPH X, etc.) is then asserted. The Cont Word flip-flop cannot be clocked if the second word of a Jump instruction (MD JUMP WORD 1 L) is being read. This word, an address on the bus data lines, could cause the Cont Word flip-flop to change states and, therefore, the C input is inhibited.

The Mode Select Multiplexer outputs four signals [MD MODE (3:0) H] that are decoded in the 74154 4-Line to 16-Line Demultiplexer (mode decode) to generate a single output signal. Table 2-6 lists all the decoder outputs along with their requisite input signals.

The mode decoder outputs serve many functions in carrying out the explicit steps required by a particular instruction. For example, MD STATUS A H is used to clock Unibus data bits into the Status A Register flip-flops (drawing M7013-SABR) to establish certain operating parameters. The state of one of these flip-flops, LP INT HIT ENA, determines if future light pen hits are to be accepted or not.

In conclusion, several points should be reviewed. Unibus data bit 15 = 1 denotes an instruction on the Unibus. Bits 11, 12, and 13 are gated into the Mode Control Register and one of five control instruction signals is concurrently

Table 2-6
Mode Decoder Outputs

| 74175 Control Mode Register Outputs | | | 74175 Data Mode Register Outputs | | | Mode Select MUX Output* (MD MODE X H) | | | | 74154 Mode Decode Asserted Output | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| R1(1) (DB13) | R2(1) (DB12) | R3(1) (DB11) | R1(1) (DB13) | R2(1) (DB12) | R3(1) (DB11) | 3 | 2 | 1 | 0 | | |
| L | L | L | | | | H | L | L | L | MD GRAPHIC MODE L | Control Instructions |
| L | L | H | | | | H | L | L | H | (No connection)** | |
| L | H | L | | | | H | L | H | L | (No connection)** | |
| L | H | H | | | | H | L | H | H | (No connection)** | |
| H | L | L | | | | H | H | L | L | MD JUMP L | |
| H | L | H | | | | H | H | L | H | MD DNOP L | |
| H | H | L | | | | H | H | H | L | MD STATUS A L | |
| H | H | H | | | | H | H | H | H | MD STATUS B L | |
| | | | L | L | L | L | L | L | L | MD CHARACTER L | Data Instructions |
| | | | L | L | H | L | L | L | H | MD S VECTOR L | |
| | | | L | H | L | L | L | H | L | MD VECTOR L | |
| | | | L | H | H | L | L | H | H | MD POINT L | |
| | | | H | L | L | L | H | L | L | MD GRAPH X L | |
| | | | H | L | H | L | H | L | H | MD GRAPH Y L | |
| | | | H | H | L | L | H | H | L | MD REL PT L | |
| | | | H | H | H | L | H | H | H | (No connection)** | |

*Mode Select MUX accepts inputs from the Data Mode Register when bit 15 = 0.
Mode Select MUX accepts inputs from the Control Mode Register when bit 15 = 1.
**The display processor will hang if these outputs are asserted.

output from the mode decode. The information on the Unibus is data (as opposed to an instruction) when bit 15 = 0; the two mode registers remain unchanged. At the same time, the previously loaded Data Mode Register is read and one of the graphic mode signals is asserted from the mode decode. Unibus bit 14 = 1 when a control instruction (not Set Graphic Mode) is on the Unibus; the Data Mode Register is not changed at this time. When bit 14 = 0, the mode control contains the code for Set Graphic Mode and the Data Control Register is loaded with the particular op code for the graphic mode.

### 2.2.8 Control Instructions

The five instruction repertoire of the VT11 Display Processor is capable of effecting all display, control, and interrupt functions required for VT11 operation. These instructions, read from the display file in the memory as the result of NPRs and then decoded, generate those signals necessary to carry out the specified operations.

Purposes for the display instructions are distinctive – although there is some overlap in this respect (three of the instructions are used to establish operating parameters). In determining the type of display, the Set Graphic Mode instruction is the most important of this small, though powerful, instruction set. This instruction initiates the graphic or display mode of operation, in a general sense, and at the same time clearly defines one of the seven types of displays (op codes). Several display qualifications are also specified. The Jump instruction allows the display program flow to be changed to a non-contiguous memory area; the second word of this instruction is retrieved from memory and inserted into the DPC to become the address of the next memory location to be read. No-op also performs in the classic manner. Aside from incrementing the DPC, no-op does not affect the VT11 display or change the display parameters; it is used primarily as a "filler" between the other instructions or data. The operating parameters are specified by the Load Status Register A, Load Status Register B, and Set Graphic Mode instructions. The first two are devoted solely to such functions as determining whether the character font is to be normal or italics and whether to generate an interrupt to the PDP-11 when the display stops. Figure 2-8 is a breakdown of each of the instruction words.

**2.2.8.1 Load Status Register A** – This instruction, decoded (Paragraph 2.2.7) when Unibus data bits (15:11) = $11110_2$, sets or clears five flip-flops shown on M7013-SABR. Figure 2-9 picks up the instruction flow where the signal MD STATUS A H is asserted by the mode decoder.

Depending on the parameters to be established, one or more of the five flip-flops controlled by Load Status Register A can be set/cleared by TD LOAD PULSE H when the instruction is decoded. Three of the flip-flops (SABR Stop Interrupt Enable, SABR Italics, and SABR Light Pen Hit Enable) can be set or cleared as determined by the instruction's bit configuration (Figure 2-8). The other two (SABR Stop and SABR Sync) can only be set when this instruction is decoded; they are automatically cleared at some later point.

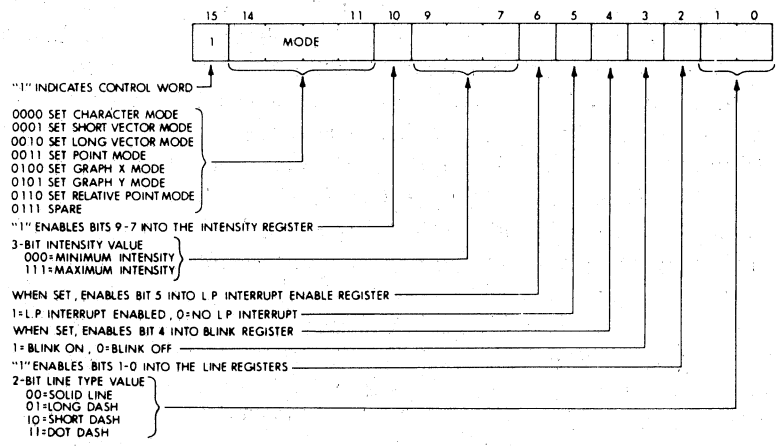
The SABR Stop Int Ena flip-flop performs its function of initiating a stop interrupt only in the presence of a set SABR Stop flip-flop. (Normal NPR assertion occurs if Stop is not set.) However, the SABR Stop flip-flop can produce a usable output regardless of the state of Stop Int Ena. In either configuration further NPRs are temporarily inhibited, thus halting the display program. This is to allow time for the PDP-11 to update the display file in core memory. Assertion of stop interrupt on the Unibus (both flip-flops must be set) is the more positive means of informing the CPU of the stop condition. There is no stop interrupt generated when only SABR Stop is set; the DPU depends on the CPU reading status to ascertain the stop condition. In both cases the CPU, under program control, may alter the display file and then flag the display processor by placing the DPC address and BUS MSYN L on the Unibus. Under program control, the CPU may also set Unibus data bit 0 to a 1 as it addresses the DPC. This serves two functions: first, it inhibits the assertion of ASL START H and, therefore, the DPC is not loaded (changed); second, ASL RESUME H is generated and an NPR is asserted (drawing M7013-TD). Display program execution now resumes at the point it was stopped. In the meantime, the display processor responds to MSYN by asserting BUS SSYN L. The PDP-11 now drops BUS MYSN L which, in turn, inhibits ASL RESUME H and SABR Stop is cleared. SABR Stop Int Ena is reset explicitly by a Load Status Register A instruction.

**NOTE**

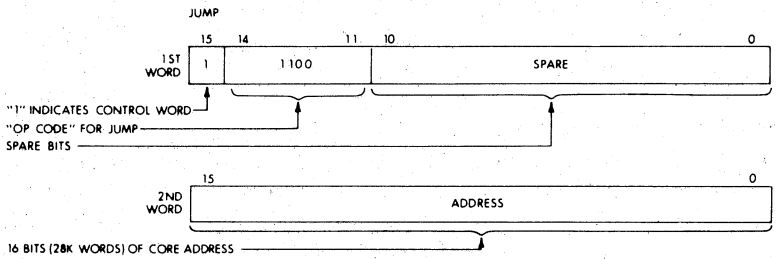
**Do not stop the display (bit 10 = 1) and synchronize the display (bit 2 = 1) with the same Load Status Register A instruction. If Stop Interrupts are disabled, doing so causes the display to stop and then restart in sync immediately, i.e., sync overrides stop. If Stop Interrupts are enabled, DPU response is undetermined.**

The Italics flip-flop can be set or cleared with a Load Status Register A instruction to control the font of the displayed characters. Briefly, when the Italics flip-flop is set, the CRT X and Y drive signals are mixed and thus produce the italics effect.

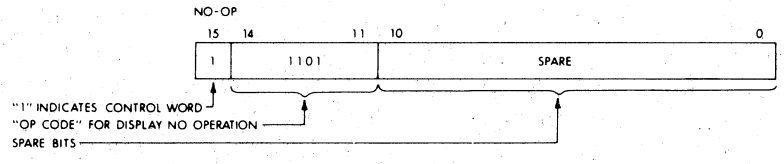
## SET GRAPHIC MODE



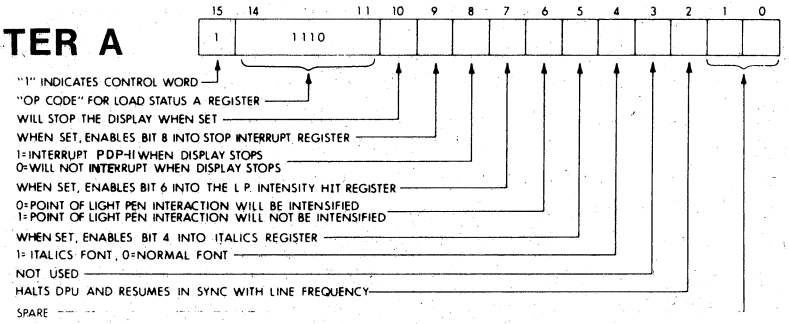

## JUMP




## NO-OP




## LOAD STATUS REGISTER A




## LOAD STATUS REGISTER B

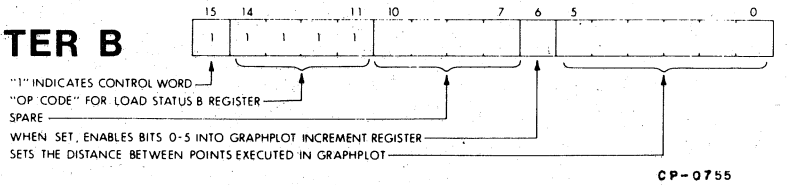



Figure 2-8 Instruction Word Functions

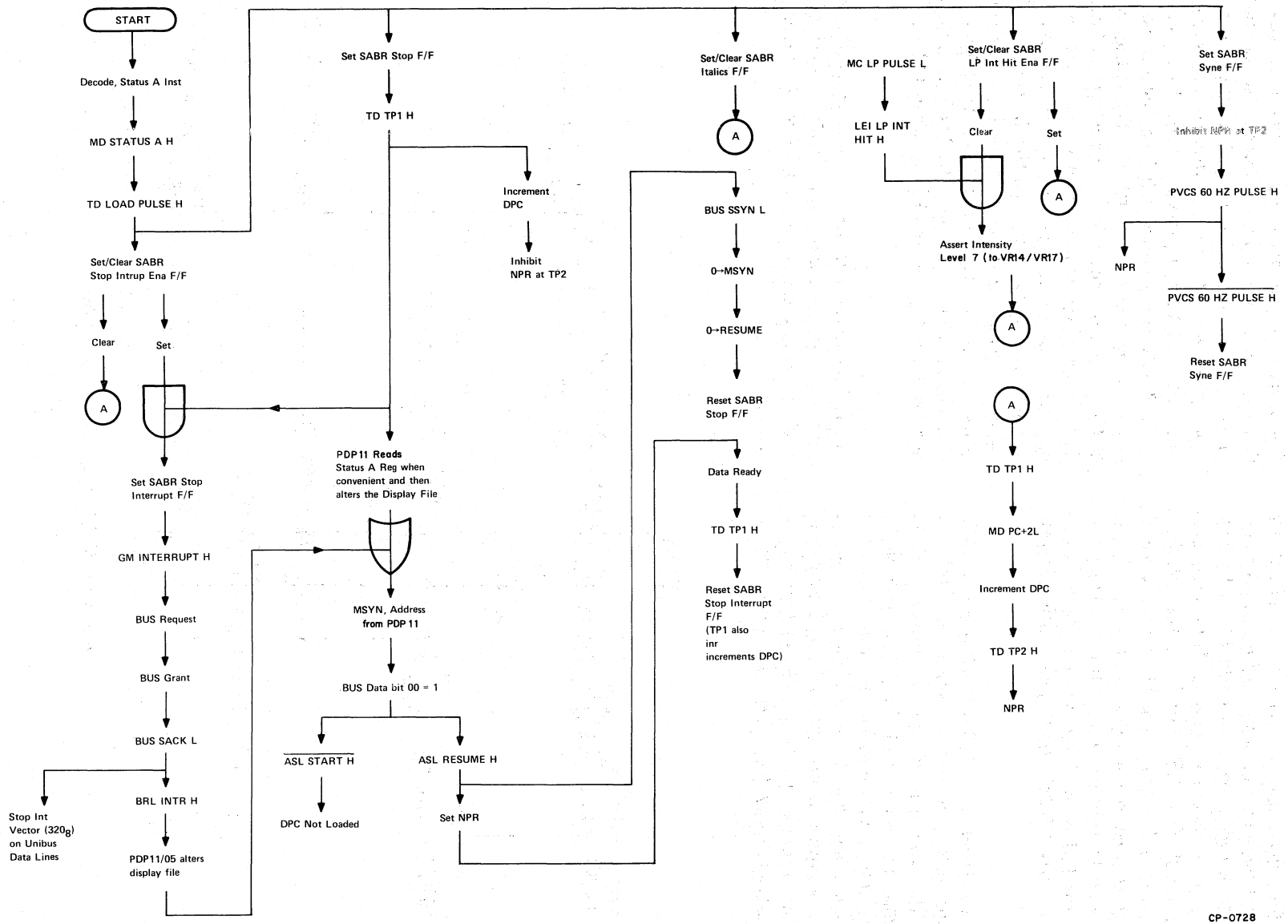



Figure 2-9 Status A Instruction Flow Diagram

The third flip-flop that can either be set or cleared is SABR LP Int Hit Ena. Each light pen hit (MC LP PULSE L) triggers a 74123 single-shot to assert the 2 μs signal LEI LP INT HIT H. If this pulse finds the SABR LP Int Hit Ena flip-flop in a reset condition (drawing M7013-GM and Figure 2-10), signals GM INT (3:0) L are asserted. This forces intensity level 7 to be generated in the VR14/VR17 (unless already asserted by the display program) for 2 μs at the point where the light pen is aimed; image brightness increases to the highest level possible for the particular setting of the VR14/VR17 front panel BRIGHTNESS control.

One of the factors controlling the brightness of a given CRT display is the repetition rate at which the display is intensified. This rate depends on the display program execution time, i.e., the size of the display program; a relatively large display of many characters and/or vectors is intensified less often than a smaller display program. Consequently, a smaller display, intensified at a faster rate, appears brighter because there is insufficient time for the CRT fluorescence to decay. Figure 2-11 shows this relationship between image brightness and display execution time. This variance in brightness can be eliminated for all displays that take less than 16.67 ms to intensify by establishing a single program repetition rate. With the SABR Sync flip-flop set by the Load Status Register A instruction, the next NPR is inhibited (drawing M7013-TD) until PVCS 60 Hz PULSE H is asserted. This 70-ns pulse is the output of a 74123 Monostable Multivibrator that is triggered by a 60-Hz signal from the PDP-11 power supply. Therefore, those display program routines that contain a Load Status Register A instruction with Sync specified can have a repetition rate no faster than 60 Hz; the brightness level is uniform when all display programs with an execution time of less than 16.67 ms are so structured. The brightness level is halved for longer programs. The SABR Sync flip-flop is reset on the trailing edge of PVCS 60 Hz PULSE H.

As the Load Status Register A instruction is processed, the DPC is incremented, and another NPR is issued. This will result in the next display program word being fetched and processed.

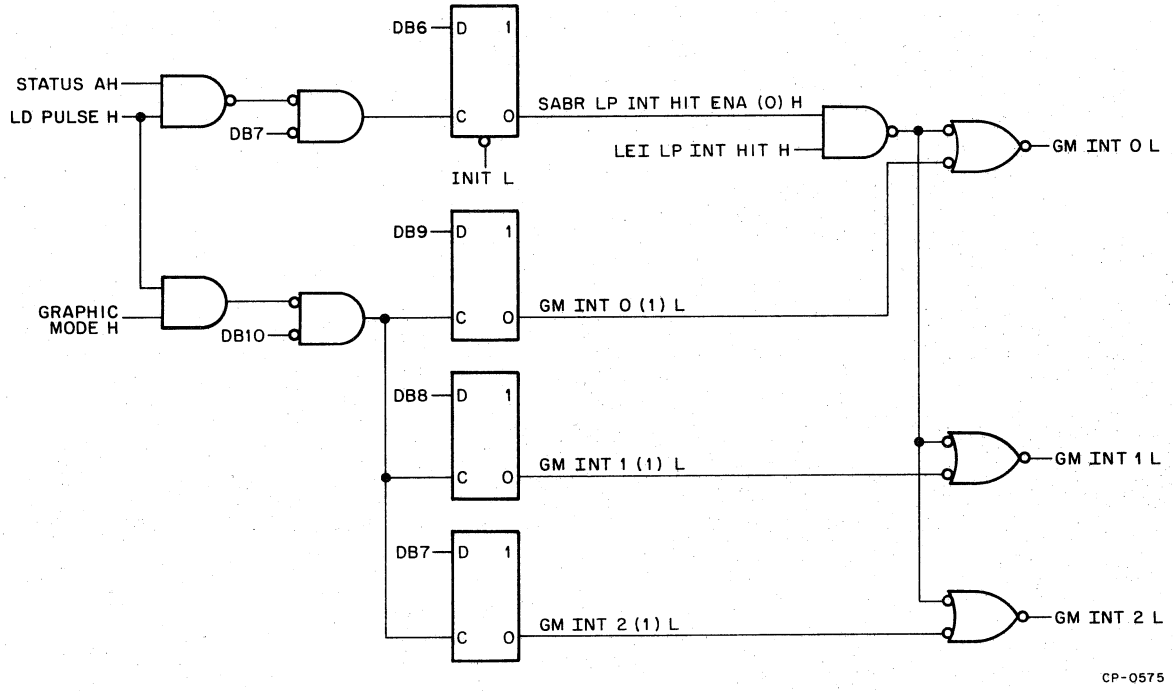



Figure 2-10 M7013 Intensity Level Control

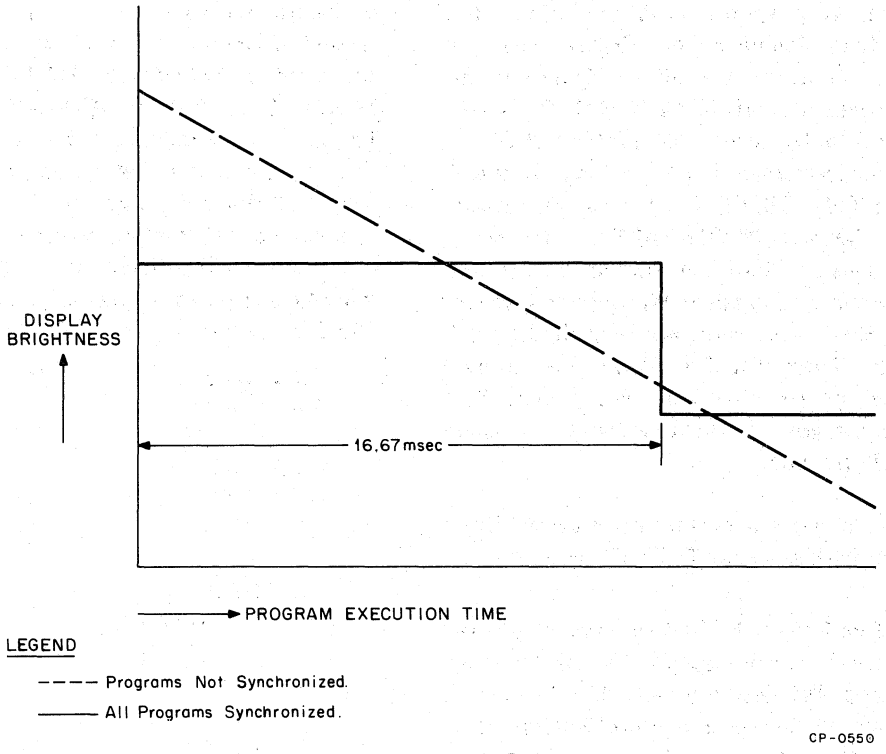



Figure 2-11 Relationship of CRT Brightness to Program Length

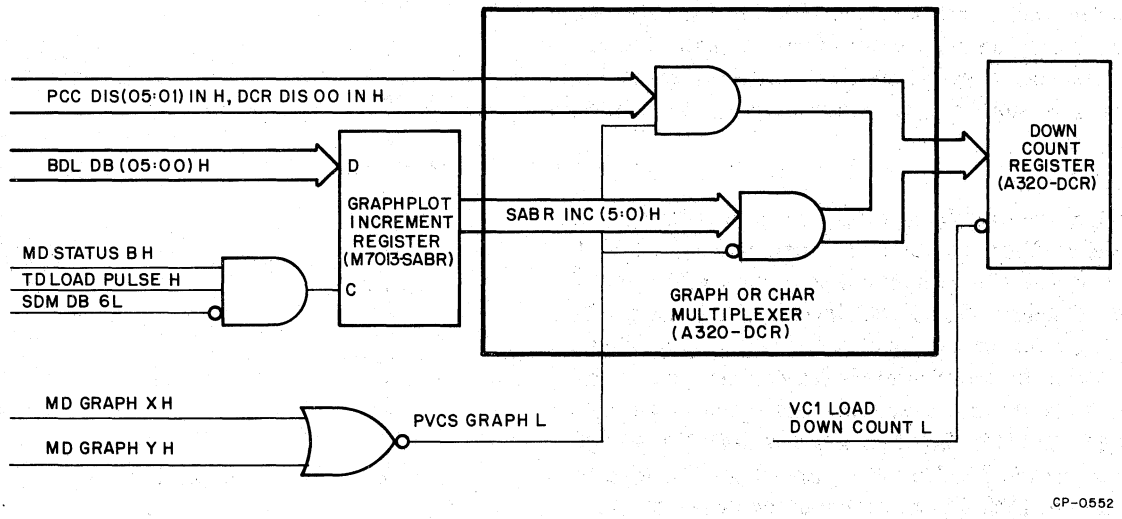



Figure 2-12 Graphplot Logic

**2.2.8.2 Load Status Register B** – Decoding this instruction results in a relatively simple operation. Unibus data bits (15:11) = $11111_2$ denote a Load Status Register B instruction. As the result of this bit configuration, the mode decode logic generates MD STATUS B H. This signal, on the assertion of timing signal TD LOAD PULSE H, provided bit 6 of the instruction is a 1, gates bits 0 through 5 of the instruction (BDL DB 05:00 L) into the Graphplot Increment Register (drawing M7013-SABR). This register, type 74174 (five D-type flip-flops), outputs SABR INC (5:0) H to the Graph or Character Multiplexer (drawing A320-DCR) when the display processor is in the Graph X or Graph Y mode. These five bits define the distance between intensified points in a graphplot. Figure 2-12 illustrates the relationship of the Graphplot Increment Register to the A320 module.

Timing proceeds in the normal manner and another NPR is issued (drawing M7013-TD) when TD TP 2H is asserted.

**2.2.8.3 Jump Instruction** – Of the five instructions used by the VT11 Display Processor, Jump is the only one that consists of two words. The first word uses bits 11 through 15 (= $11100_2$) to specify the op code; the eleven low-order bits are spares. However, all 16 bits of the second word are used. This part of the instruction contains an address that identifies the next core memory location to be read. Replacing the current address in the DPC, this new address interrupts the normal retrieval of sequential (contiguous) memory locations and causes a new memory area to be accessed. The Jump instruction is thus used to connect sections of a program, e.g., instructions and data, that are located in separate areas of memory and to cause certain routines in a program (or the entire program itself) to be repeated.

As a result of the handshaking that takes place between the VT11 Display Processor and the memory, BCL DATA READY L initiates the generation of a timing pulse stream. The first of these, TD LOAD MODE H (Figure 2-13), clocks bits 11 through 13 of the first word of the Jump instruction into the Control Mode Register and asserts MD JUMP H. As is the case when any instruction is decoded (bit 15 = 1), TD LOAD MODE also asserts MD CLR WORD L, which resets the Word flip-flop (drawing M7013-PVCS). At TP1 time the DPC is incremented by two when MD PC + 2 L is generated; the DPC now contains the core memory address of the second word of the Jump instruction. This is placed on the Unibus address lines and on the leading edge of TD TP2 H an NPR is issued. The specified memory location is then read and the contents placed on the Unibus data lines; this data is the address of the next memory location to be accessed. The Word flip-flop is set at the trailing edge of TD TP2 H 50 ns after the NPR is issued. Signal PVCS WORD (1) H, indicating the second word of an instruction/data word is on the Unibus, or that the second character of a character data word is being processed, is ANDed with MD JUMP H to assert MD JUMP WORD (1) L (drawing M7013-MD). This latter signal will inhibit the forthcoming TD LOAD MODE H signal from clocking the Control Mode and Data Mode Registers and the Cont Word flip-flop; their contents and output will remain unchanged when the second word of the instruction is accepted by the display processor. MD JUMP WORD 1 L will also inhibit the assertion of MD CLR WORD L and the Word flip-flop is not cleared (if BDL DB15 = 1).

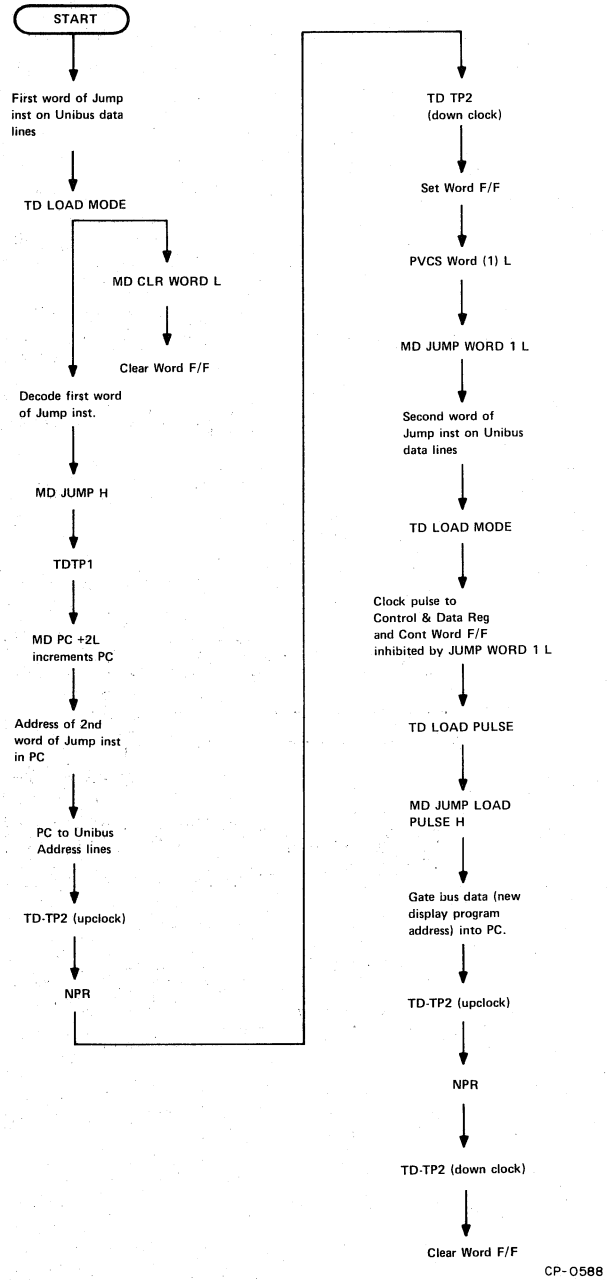



Figure 2-13 Jump Instruction Flow Diagram

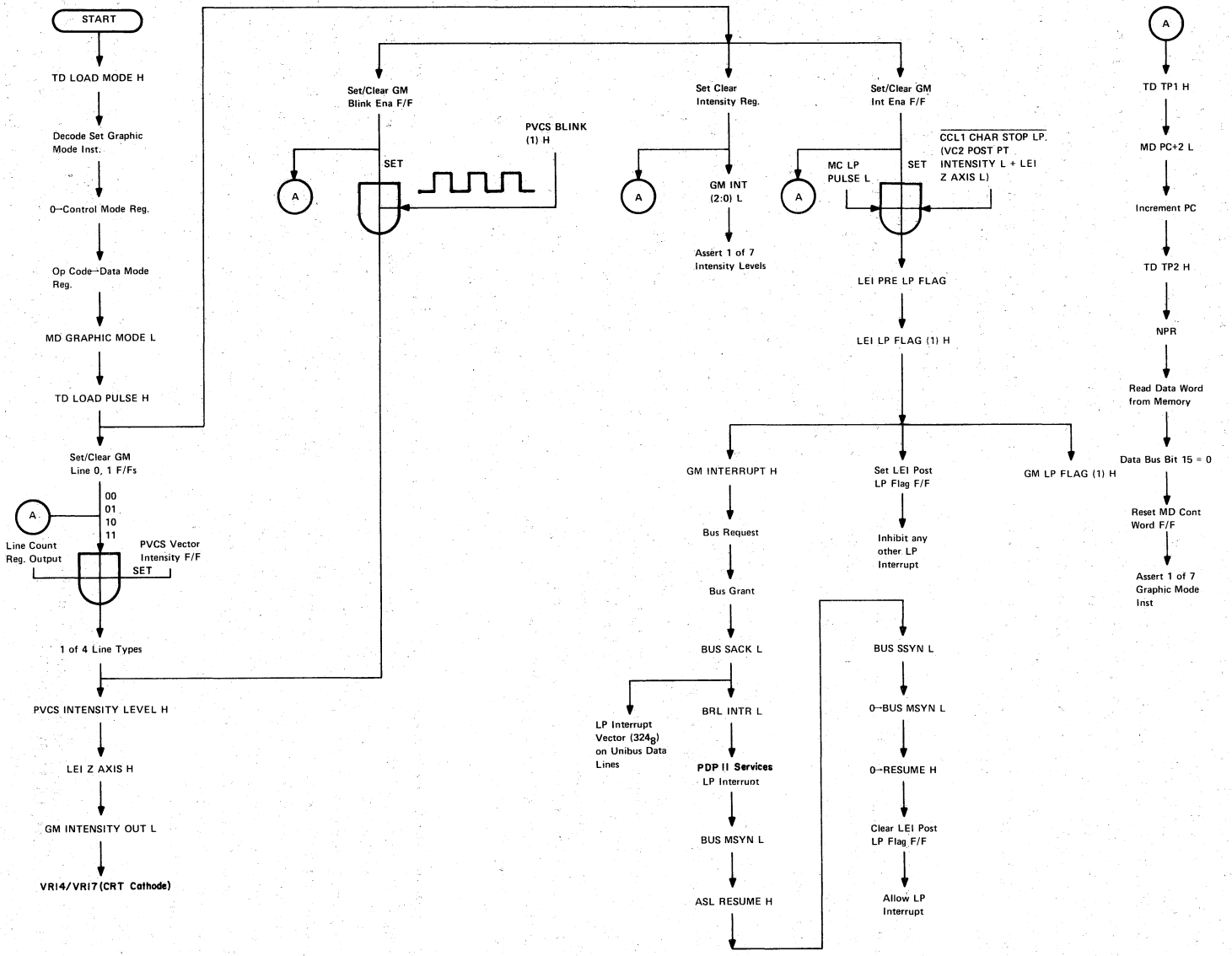



Figure 2-14 Set Graphic Mode Instruction Flow Diagram

When the second word of the Jump instruction is read, the ensuing four-signal series of timing pulses is generated by the timing logic. With the advent of TD LOAD PULSE L, MD JUMP LOAD PULSE H is asserted. This signal gates the data on the Unibus [BDL DB (15:01)] into the DPC (drawing M7014YA-PCC) replacing the current address. The DPC is not incremented by the subsequent TD TP1 H because MD JUMP WORD 1 L continues to be true. At the leading edge of TD TP2 H another NPR is issued and the display program now "jumps" to the new memory address. The operation concludes with the clearing of the Word flip-flop at the trailing edge of TD TP2 H.

**2.2.8.4 No-Op Instruction** – No-op is the simplest of the display processor instructions in that there is no resultant display function or change of parameters. No-op is used as a core filler in the display program or to replace another unwanted instruction.

In response to an NPR, the instruction is input to the VT11 Display Processor via the Unibus data lines. The accompanying BUS SSYN L signal asserts BCL DATA RDY L which triggers the stream of timing pulses. MD DNOP L is generated by the decoding logic when the op code (bus bits 11 through 15 = $11101_2$) is decoded at TD LOAD MODE time. The display program counter is then incremented by MD PC + 2 L when TD TP1 H is asserted. To complete the operation, an NPR is generated by TD TP2 L and the next memory location is read.

**2.2.8.5 Set Graphic Mode Instruction** – This instruction could be termed the data instruction in that it contains the code (bits 14:11 = $0XXX_2$) that identifies one of the graphic or data mode instructions (Table 2-5 and Paragraph 2.2.7). This data mode op code denotes the type of CRT display that will be generated, i.e., vector, point, character, etc. The eleven low-order bits (bits 0 through 10) of the Set Graphic Mode instruction are used to specify certain display parameters: intensity level, light pen interrupt enable, blink, and line type.

When an NPR results in a Set Graphic Mode instruction being read from memory, bit 15 = 1 and bit 14 = 0 are decoded at Load Mode time and the Control Mode Register is loaded to 000 (drawing M7013-MD and Figure 2-14). The MD Cont Word flip-flop is set at this time (if not already set) and the contents ($000_2$) of the Control Mode Register are output from the Mode Select Multiplexer to the 74154 Mode Decode, which asserts the signal MD GRAPHIC MODE L.

The signal TD LOAD MODE L also clocks the data mode bits (Unibus bits 13:11) into the Data Mode Register. However, the graphic data mode signal (MD CHARACTER, MD POINT, MD VECTOR, etc.) is not asserted because the Control Mode Register is selected at this time.

The assertion of TD LOAD PULSE H causes one or more of the four control flip-flops and three Intensity Register flip-flops to be set or cleared as determined by bus data bits 0 through 10. At TD TP1 time the DPC is incremented by two (MD PC + 2 L) and then with TD TP2 H the next NPR is generated. A data word (or a Jump and then a data word) is read from memory as the result of this NPR. The type of data word that should be read now was determined by the op code specified in the Set Graphic Mode instruction previously read and presently stored in the Data Mode Register. However, all data words have bit 15 = 0 and at Load Mode time the clock inputs to the Control Mode and Data Mode Registers are inhibited (the two registers remain unchanged) and the Cont Word flip-flop is cleared. The (1) H output from this flip-flop, now low, gates the contents of the Data Mode Register into the Mode Select Multiplexer and then to the Mode Decode Register. Therefore, at Load Mode time of the data word the signal MD GRAPHIC MODE L is dropped and one of the seven graphic data mode signals is asserted.

The flip-flops controlled by the Set Graphic Mode instruction are GM Line 0, GM Line 1, GM Blink Ena, GM Int Ena, and the three in the Intensity Register. All are shown on drawing M7013-GM.

The two line flip-flops are used to generate one of four vector line types (Table 2-7) that are shown in Figure 3-13. The outputs from these flip-flops gate one of four data inputs into the 74153 Line Decoder, shown on drawing M7013-PVCS, when the PVCS Vector Intensity flip-flop is set. Both line flip-flops must be in the reset state if a solid line is to be displayed; this configuration selects the +3VB input. The other three line types require one or more inputs from the 74193 Line Count Register, shown on the same drawing.

The Line Count Register, a 4-bit binary counter, is preset to $15_{10}$, i.e., all outputs are asserted, at the beginning of the vector (PVCS LD LINE CT REG L). VC2 DOWN COUNT CLK L is divided by a single stage frequency divider and this divided clock is used to clock the Line Count Register. Timing for this operation is shown in Figure 2-15. VC2 DOWN COUNT CLK L is used because its instantaneous frequency is the same as the frequency of the vector being drawn.

**Table 2-7**
**Line Decoder Signals**

| GM Line Flip-Flop | | Selected Input(s) | Type of Line Generated |
|---|---|---|---|
| 1 (1) H | 0 (1) H | | |
| L | L | +3VB | Solid |
| L | H | PVCS LC 4 H | Long Dash |
| H | L | PVCS LC 3 H | Short Dash |
| H | H | (PVCS LC (2:1) H• PVCS LC 3 L) + PVCS LC 4 L | Dot Dash |

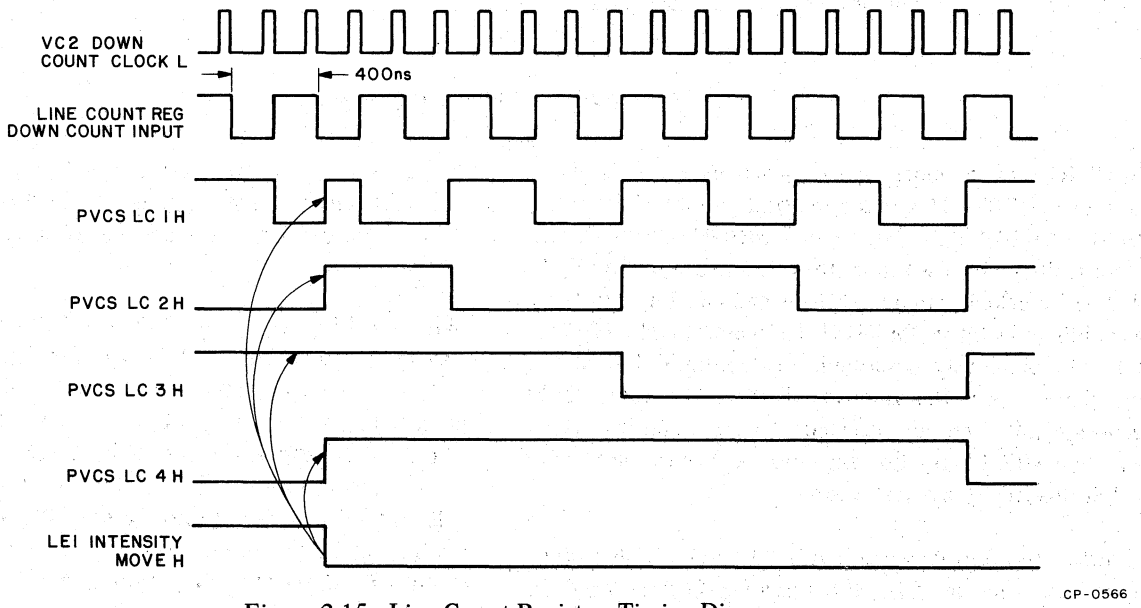



Figure 2-15 Line Count Register, Timing Diagram

The line counter output becomes PVCS INTENSITY LEVEL H, which is sent to the M7014YA module where it enables LEI Z AXIS H. LEI Z AXIS H is then returned to the M7013 module where it becomes GM INTENSITY OUT L. This latter signal is routed through the A320 module to the VR14/VR17, where it causes the CRT cathode to go from ≅+62 V to 0 V and thus go into conduction. Any of the four line types can also be made to blink because the blink function, if selected, overrides the output of the line decoder.

The blink operation, where the display is repeatedly blanked and unblanked, is a means for gaining the operator's attention. The two bits (3 and 4) in the Set Graphic Mode instruction that control the blink operation are used to set or reset the GM Blink Ena flip-flop. The (1) H and (0) H outputs of this circuit are input to two NAND gates in the PVCS INTENSITY LEVEL H circuit where the (1) H output gates PVCS BLINK (1) H and the output of the line decoder to assert the intensity level. Therefore, when Blink Ena is set, the intensity level to the VR14/VR17 is controlled by the output of the PVCS Blink flip-flop. This flip-flop, clocked by the high-order output of a 7493 frequency divider (Divide By Four Register), is set for 266 ms and then reset for 266 ms. Consequently, all, or a selected portion of the CRT display, repeatedly flashes on and off (about twice each second) as long as the GM Blink Ena flip-flop is set. Figure 2-16 is a timing diagram for this circuit.

The 7493 Frequency Divider (drawing M7013-PVCS) is clocked by a repeatedly asserted (60 Hz) output from a 7413 Schmitt trigger. (The input to the 7413 is derived from the power supply.) Outputs from the frequency divider are divisions of the input: 30, 15, 7.5, and 3.75 Hz. Only one output, the R3 (1), is used; it clocks the Blink flip-flop.

The parallel output of the three flip-flop Intensity Register (Figure 2-10 and drawing M7013-GM) is used in the

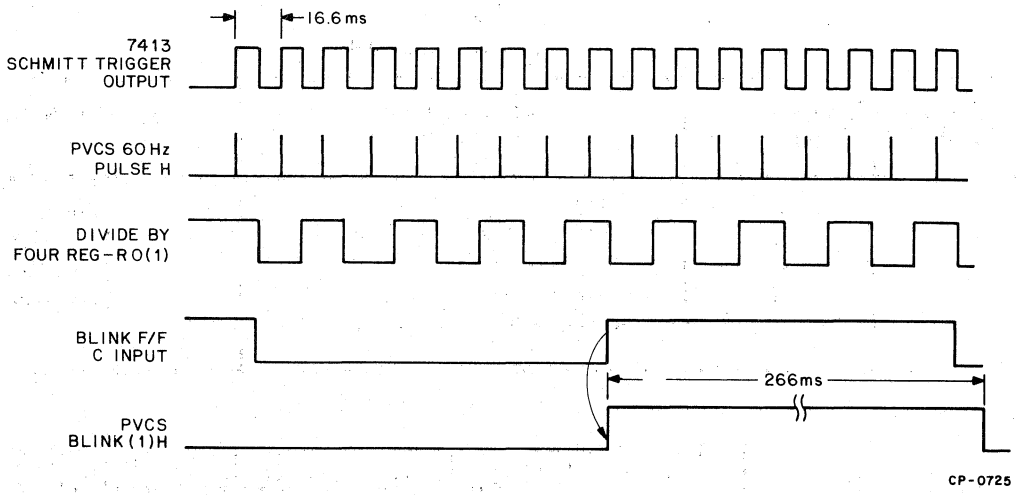



Figure 2-16 Blink Timing Diagram

VR14/VR17 to generate one of seven intensity levels to grid 1 in the CRT. This is the method employed, together with the VR14/VR17 front panel BRIGHTNESS switch, for controlling the CRT brightness level. Unibus bits 7, 8, and 9 are clocked into the register at Load Pulse time by the enabling bus bit (SDM DB 10 L) to assert GM INT (2:0) (0) H. As previously described, any configuration of the three signals from the Intensity Register is momentarily overridden (all three are asserted) if a light pen hit occurs after the SABR LP Int Ena flip-flop has been cleared by a Load Status Register A instruction.

One other flip-flop is controlled by the Set Graphic Mode instruction. When the GM LP Int Ena flip-flop is set by this instruction, a subsequent light pen (LP) hit (MC LP PULSE L) causes an LP interrupt (flag) to the PDP-11. Only one LP flag is allowed on any one point, vector, or character and LP interrupts for other areas of the display are inhibited until the interrupt operation in progress is completed.

The LEI Pre LP Flag flip-flop in the light pen logic is primed by two conditions: GM LP Int Ena flip-flop set and CCL1 CHAR STOP LP H must be false indicating the LP hit is not on the first or last column of a character. When intensification occurs at the position (point, vector, or character) where the LP is aimed, the signal MC LP PULSE L is asserted and the LEI Pre LP Flag flip-flop is clocked.

LEI PRE LP FLAG H primes the LP Flag flip-flop which is then set, if the LP hit is on a vector, on the trailing edge of VC1 VEC CLK H, or after the end of the operation (VC2 OP DONE L) if the hit was on a point, relative point, or character. In the case of a point or relative point operation, VC2 OP DONE L is caused by the 100 ns VC2 POINT DONE L that was initiated by VC2 POST PT INTENSITY L. The purpose of this sequence of signals is to incorporate a 3.2 $\mu$s delay in the LP circuit to compensate for an inherent delay in the light pen pulse from the 375 Light Pen. (Timing relative to this operation is shown in Figure 2-27.)

With the LEI LP Flag flip-flop set, LEI LP FLAG (1) L is asserted, and sets a 7474 D-type flip-flop, which inhibits further clocking of the LEI Pre LP Flag flip-flop by LP pulses. LEI LP FLAG (1) L also sets the LEI Post LP Flag flip-flop. At the same time LEI LP FLAG (0) H (low) asserts GM INTERRUPT H. This causes the VT11 to issue a BR and an interrupt, to notify the CPU of the LP hit. LEI POST LP FLAG (1) H is used to load the DACs (VC1 LOAD DAC H) with the coordinates of the LP hit. If the LP hit was on a vector, LEI POST LP FLAG (1) H halts VC1 VEC CLK H, and the vector generation ceases at the point of the LP hit. In response to the interrupt, the PDP-11 may issue a resume (ASL RESUME H) or a start (VC1 RESET L). If ASL RESUME H is asserted, the vector continues from the point where it stopped. The start operation (Paragraph 2.2.1) causes the DPC to be loaded with a new display program address.

The BR and interrupt sequence, started by GM INTERRUPT H, is similar to a stop interrupt (shown in the Status A instruction flow diagram, Figure 2-9). The most notable exception is that a light pen interrupt vector ($324_8$), instead of a stop interrupt vector, is placed on the Unibus data lines. The PDP-11 reads in the vector address, transmits BUS SSYN L to the display processor, and enters into a particular software routine. In the display processor, the consequent BCL SSYN H signal is ANDed with BRL INTR H (drawing M7014YA-BCL) to generate BCL INTR DONE H and BCL REQ CLR L. This latter signal generates ASL CLR FLAGS L which resets the LEI LP Flag flip-flop. The circuit is again receptive to LP hits until such time as the LP Int Ena flip-flop is reset.

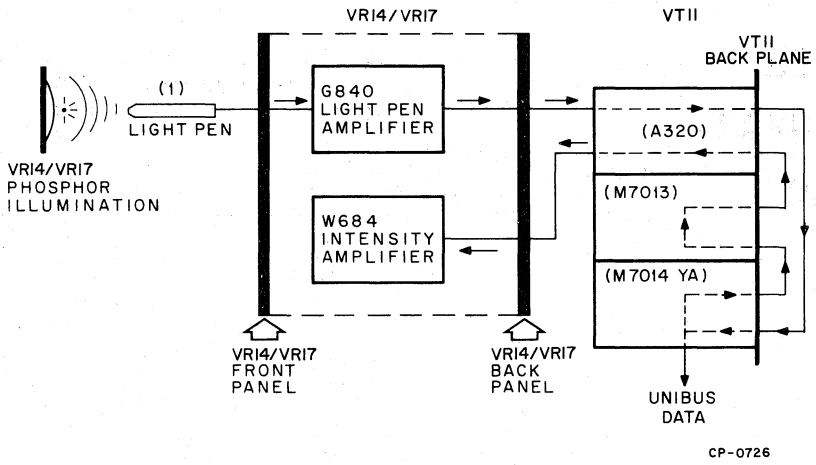



Figure 2-17 Light Pen Signal Path

Figure 2-17 sums up the routing of the LP pulse from the LP through the VR14/VR17 to the VT11 where an LP interrupt, if enabled, is asserted on the Unibus. The LP hit is also shown returning to the VR14/VR17 as an increased intensity level if SABR LP Int Ena is not set.

### 2.2.9 Data Words

Each of the seven display modes that can be initiated by the Set Graphic Mode instruction requires a distinctive data word. These data words convey information such as vector length, vector and point screen position (coordinates), and the direction a vector or relative point is to move.

Data words are 16 bits long and are identified by bit 15 = 0. Two word types, long vector and point, are always read in pairs; the first word contains X information and the second (following) word contains Y information. In the other modes all data relative to a single coordinate or expression of magnitude is contained in one 16-bit word.

Figure 2-18 shows the format and bit functions for each type of data word. The different data words, when received from the Unibus data lines, are delivered to specific destinations. Figure 2-19 shows data word routing from the bus to the initial storage register. In brief, short and long vector and relative point words go to the $\Delta X$ and $\Delta Y$ Registers in the A320 module, point and Graphplot X/Y words are input to the X and Y Position Registers, also in the A320 module, and character words are gated into the Character Register. The specific gating signals required to transfer a data word into these registers are a function of the data mode in effect at the time the data word is placed on the Unibus.

**2.2.9.1 Data Word Functions** – Use of the data words is determined by the particular graphic mode instruction being executed, i.e., that mode presently stored in the Data Mode Register.

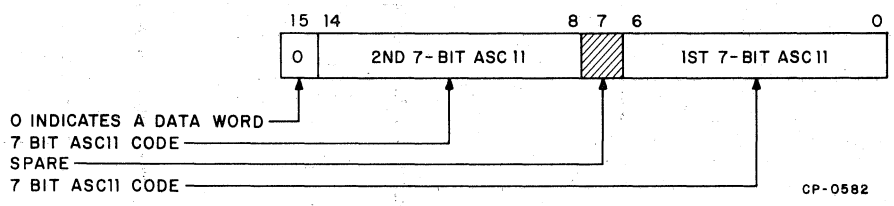
Character data words contain the codes for two 7-bit characters that are decoded and display two 6 X 8 dot format characters. The characters are selected from the 127 (96 ASCII and 31 special characters) available in the VT11 print repertoire. A simplified program example of the type used to display a group of characters is listed in Table 2-8; Figure 2-20 shows the result of this sequence.

Long and short vector data words contain information that defines the magnitude or length of the vector (termed $\Delta X$ and $\Delta Y$) and the angle at which the vector is to be drawn (left-right, up-down). The long vector data requires two words; they are read back to back.

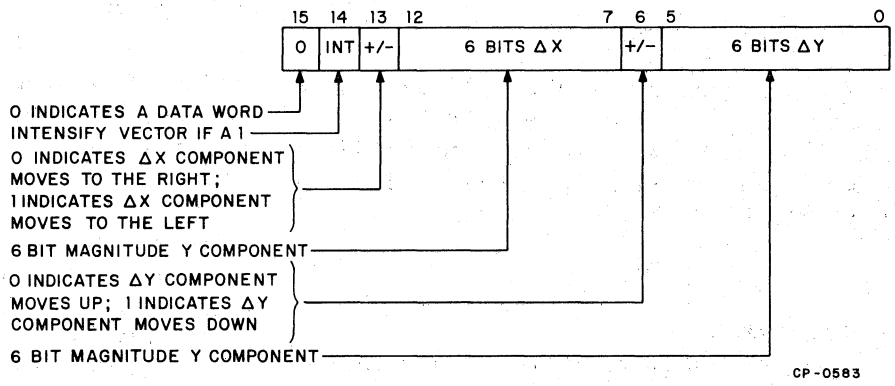
Table 2-8 and Figure 2-20 show a programming example and the resultant display, respectively, for a long vector. A second vector can be drawn in a similar manner; the starting point is the termination point of the first vector, which has been retained following completion of the first vector.

One application of the point data word has been described – to specify the starting point when characters or vectors are displayed. The data word can also be displayed as a single intensified point on the CRT. Subsequent data words in the same mode display other points in any relationship (distance, position) to each other (this is in contrast to a Graphplot display described below). Point data words are read in pairs. The first word contains a 10-bit X coordinate; the Y coordinate follows in the next word. The point may or may not be intensified as specified by bit 14 (first word); no magnitude or direction bits are included in either word.

## CHARACTER DATA FORMAT- Mode 0000




## SHORT VECTOR MODE- Mode 0001




## LONG VECTOR DATA FORMAT- 0010

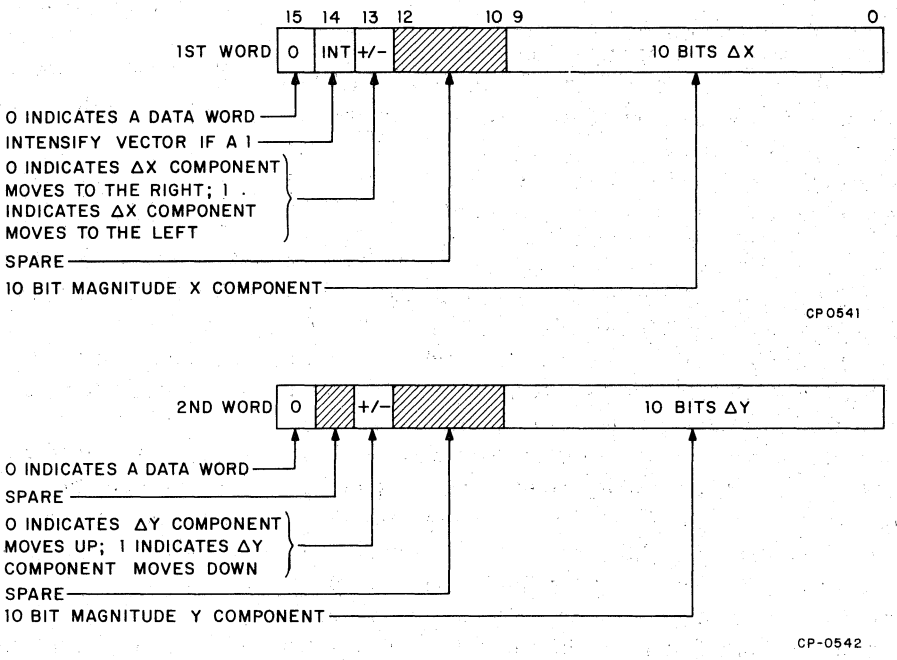
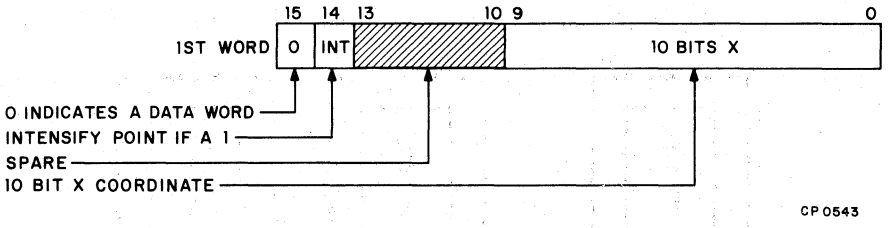
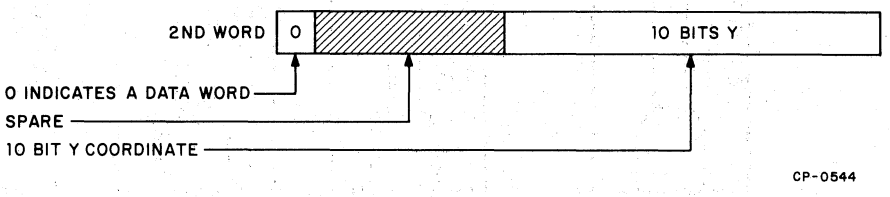



Figure 2-18 Data Word Formats (Sheet 1 of 2)

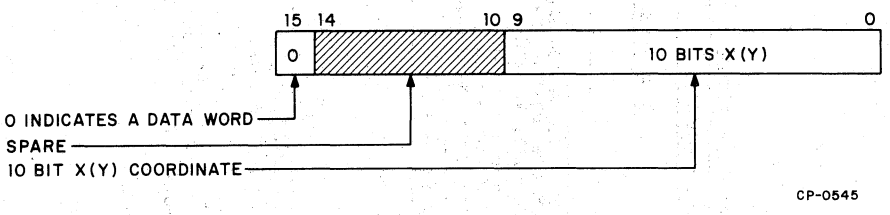
**POINT DATA MODE-**
**Mode 0011**




**GRAPHPLOT X-**
**Mode 0100**

**GRAPHPLOT Y-**
**Mode 0101**




**RELATIVE POINT MODE-**
**Mode 0110**

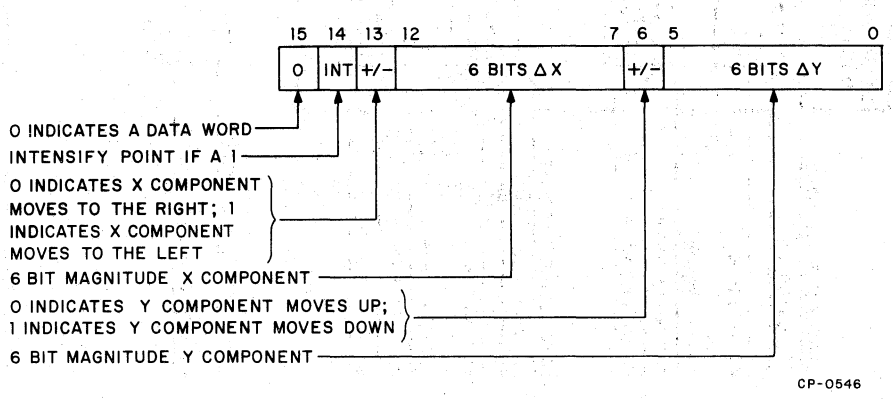



Figure 2-18 Data Word Formats (Sheet 2 of 2)

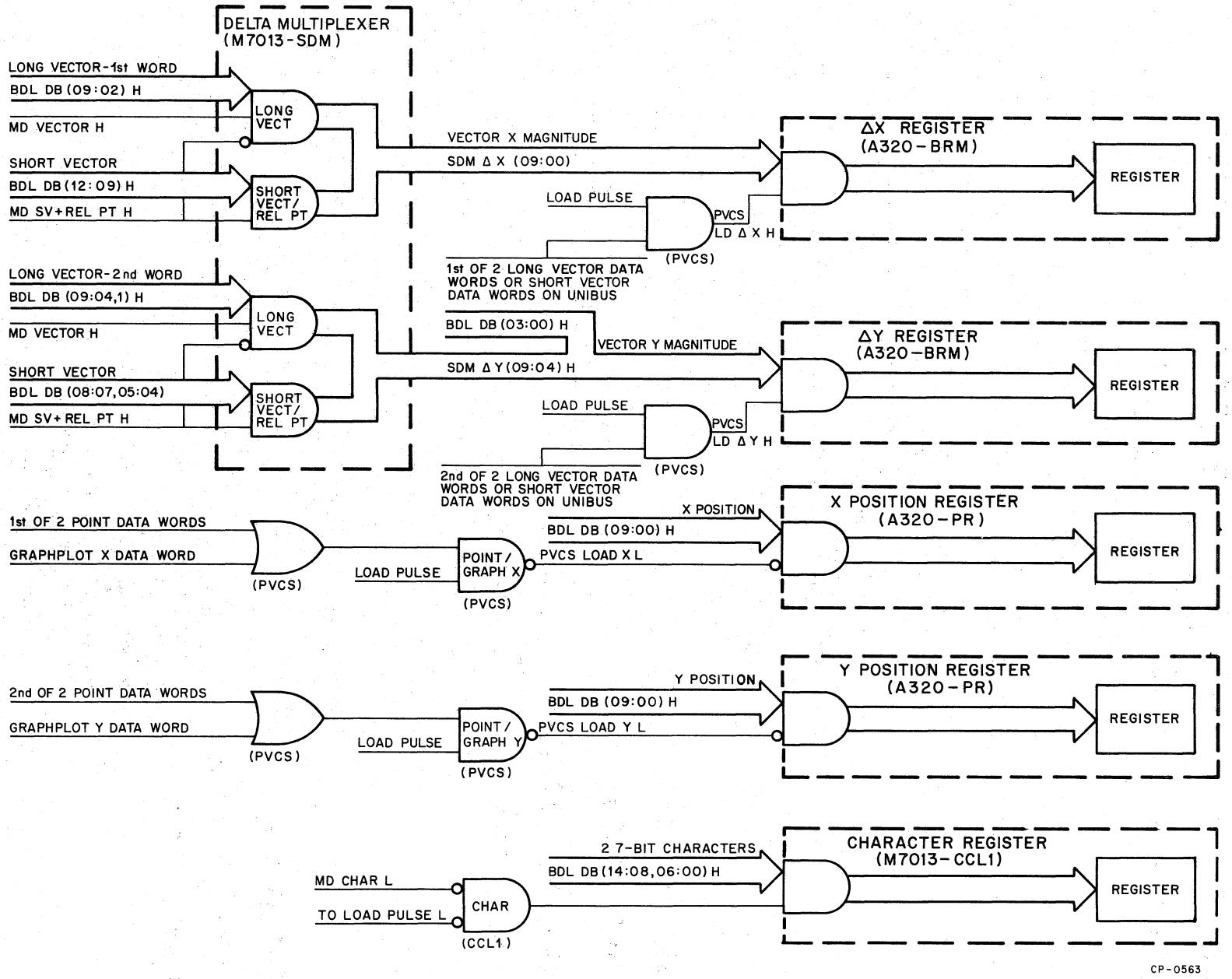



Figure 2-19 Data Word Storage

**Table 2-8**
**Control and Data Word Applications**

| Display Type | Typical Program Sequence | Purpose for the Control/Data Word |
|---|---|---|
| Character | Set Graphic Mode Instruction (Point Mode) | Establishes the mode for the data that follows. |
| | 2 Point Data Words | Not intensified; defines the screen location of the first character displayed. |
| | Set Graphic Mode Instruction (Character Mode) | Establishes the operational mode for the data that follows. |
| | Character Data Word | Contains the codes for the first two characters that are displayed. Screen positioning is automatically moved (to the right) after each character is displayed. |
| | Character Data Word | Contains the codes for the second two characters. |
| | etc. | This sequence is repeated until the message is completed at which time the mode is changed. A second line of characters can be displayed if carriage return (CR) or line feed (LF) is sensed. |
| Long Vector | Set Graphic Mode Instruction (Point Mode) | Sets the mode for the data that follows. |
| | 2 Point Data Words | May be intensified; defines the screen location for the start of the vector to be displayed. |
| | Set Graphic Mode Instruction (Long Vector Mode) | Establishes the operational mode for the data that follows. The VT11 uses the data in 2 word groups. |
| | Long Vector Data Word (1st word) | Contains the $\Delta X$ component, intensify, and X direction bits for the 1st vector. |
| | Long Vector Data Word (2nd word) | Contains the $\Delta Y$ component and the Y direction bit. The first vector is now displayed. |
| | Long Vector Data Words (1st and 2nd) | Display the second vector. |
| | etc. | Repeat the above sequence, until the mode is changed. |
| GRAPH Y | Load Status Register B Instruction | Contains the X constant that is stored in the Graphplot Increment Register. |
| | Set Graphic Mode Instruction (Point Mode) | Establishes the mode for the data that follows. |

**Table 2-8 (Cont)**
**Control and Data Word Applications**

| Display Type | Typical Program Sequence | Purpose for the Control/Data Word |
|---|---|---|
| | 2 Point Data Words | Intensified; locates and displays the first point and provides the starting (X) location for subsequent Graph Y data words. |
| | Set Graphic Mode Instruction (Graph Y Mode) | Establishes the mode for the Graph Y data words that follow. |
| | Graph Y Data Word | Contains the Y coordinate for the next point displayed. The X coordinate is derived from the previous X coordinate to which is added the constant in the Graphplot Increment Register. If the Point instruction is omitted, the first point is displayed at the left edge of the CRT. |
| | etc. | Repeat until mode is changed. |

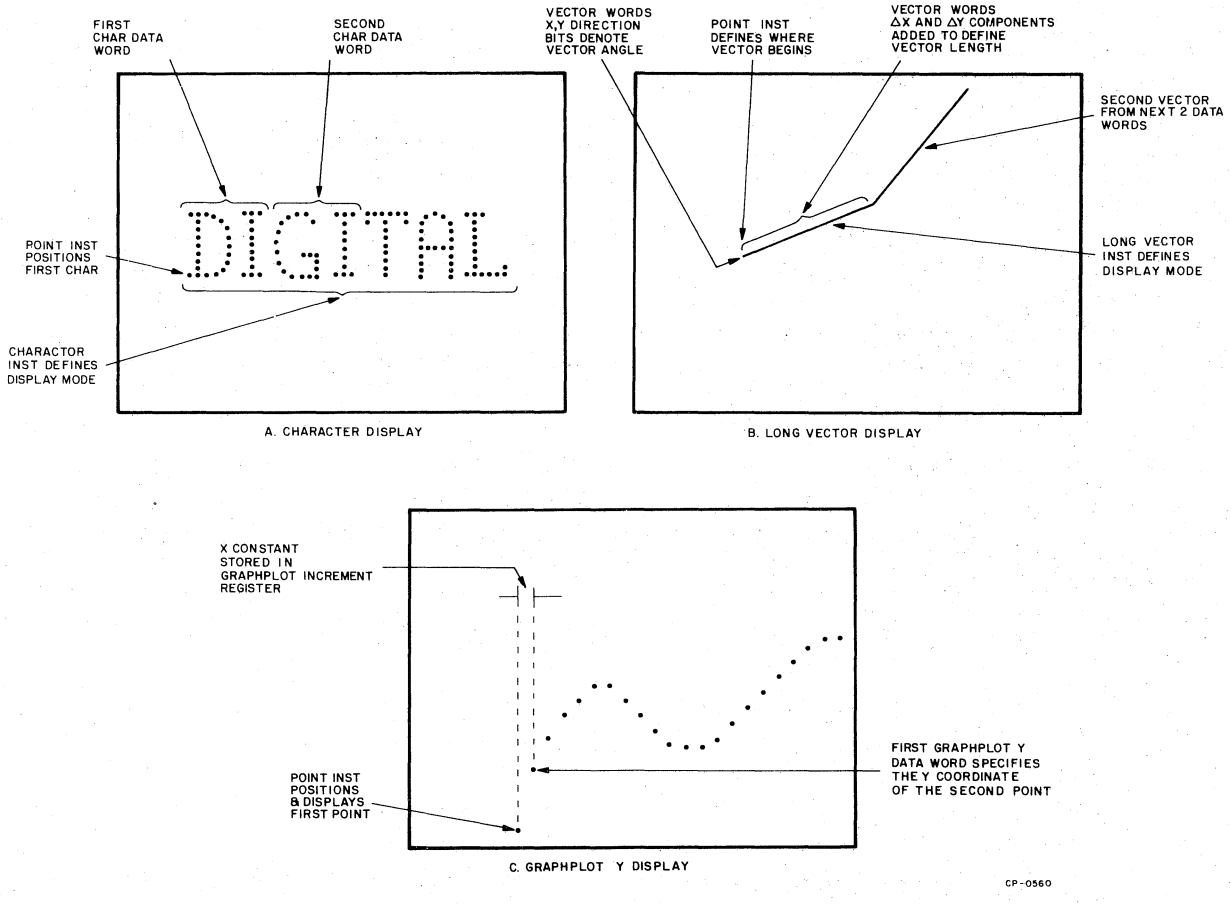



Figure 2-20 Display Examples

Graph (Graphplot) X and Graph Y words cause a series of points to be displayed that are equidistant in the opposite plane. For example, Graph Y data words (Figure 2-20) define variable positions in the Y dimension that are equidistant in the X dimension. The X coordinate is incremented after each point is displayed by a constant that was specified in a previous Load Status Register B instruction and is now stored in the Graphplot Increment Register (Paragraph 2.2.8.2 and Figure 2-12). In the Graph X display the constant is used for equal increases in the Y direction.

Relative point data words have the same format as short vector data words. They function in the same manner except that intensification is inhibited until the end of the "vector"; the consequent display appears as an intensified point.

### 2.2.10 Vector Generation

A vector is a line, drawn on the CRT screen, that presents a quantity having direction and magnitude. Both direction and magnitude are specified by two mathematical components, one for the X dimension and one for the Y dimension. It is the addition of these two vector components that produces the resultant vector on the CRT.

The long vector instruction is used to draw a line, the magnitude and direction of which are specified in two data words. The first word defines ΔX (X magnitude or length) and the second defines ΔY (Paragraph 2.2.9). The short vector instruction is similar to a long vector instruction except that the former requires only a single data word to convey both the ΔX and ΔY information. The following discussion assumes a long vector is being executed.

Figure 2-21a shows the bit position for the vector mode instruction. The first word specifies the magnitude of the X component (bits 0 through 9), bit 13 specifies the direction of this component, and bit 14 indicates if the vector is to be intensified. The second word is identical to the first except that it specifies the Y component and the intensification bit is omitted. Figure 2-21b shows the two components of a typical vector: an X magnitude of $1777_8$ in the positive direction and the same magnitude and direction for the Y dimension. The resultant vector is the sum of the two and is drawn relative to the initial beam position on the CRT. Figure 2-21c illustrates the resultant if the ΔY component is halved to $1000_8$; the angle of the vector from the horizontal decreases. Figure 2-21d shows the results if a negative value is specified in the Y axis (word 2, bit 13 = 1). In this case the vector is drawn in the negative Y direction relative to the starting point.

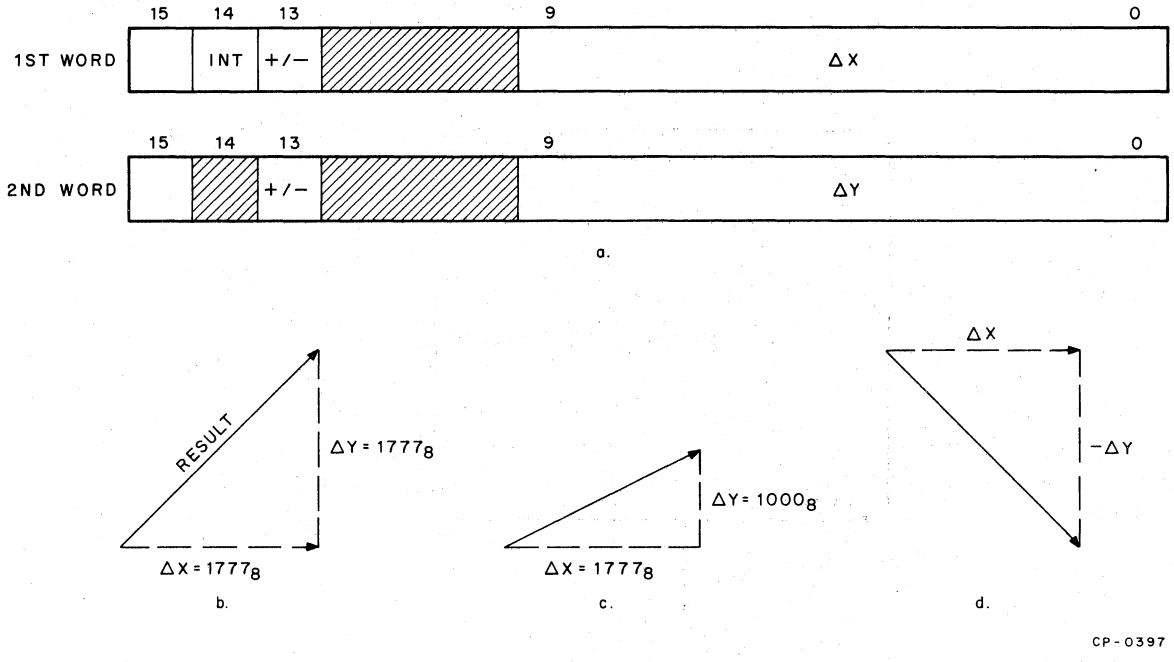



Figure 2-21 Vector Instructions and Examples

If the vector in Figure 2-21d is drawn on the CRT and the starting point is 0,0 the line is entirely cut off and cannot be seen. This is illustrated in Figure 2-22, which also depicts the situation where vector components of $\Delta X = 1777_8$ and $\Delta Y = 1777_8$, both being of the maximum magnitude, result in a partially cut-off display when the starting point is $1000_8, 1000_8$.

**2.2.10.1 General Description** – Figure 2-23 is a simplified block diagram of the vector generating logic in the A320 module. The X and Y analog signals to the X and Y CRT deflection drivers are the summed output of the respective DACs and ramp generators. The DACs generate the analog equivalent of the digital contents of the holding registers. At the start of a vector the holding registers contain coordinates of the starting point. These might be the coordinates for the end of the previous vector, if several vectors are to be joined, or an initial set of coordinates brought in by a Point instruction, if an unconnected vector is to be drawn. At the conclusion of the present vector, the holding registers are updated by the X and Y Position Registers to reflect the termination coordinates. The ramp generators, not the DACs, generate the X and Y outputs. The DACs simply hold the basic beam position. This is the initial beam position while the vector is being drawn and the final beam position after the vector is completed. The outputs from the ramp generators are two ramps, X and Y, whose slopes are proportional to the frequency of the COUNT X and COUNT Y clocks. Therefore, in determining the dimensions of the X and Y slopes, COUNT X and COUNT Y, in effect, control the angle of the displayed vector.

The COUNT X and COUNT Y pulses are the buffered outputs of the X and Y Binary Rate Multipliers (BRM). They are used external to the A320 module. The unbuffered ANALOG X and ANALOG Y BRM outputs are used in the A320 module to generate the vector ramps; otherwise, ANALOG X(Y) and COUNT X(Y) may be considered identical. The BRMs are controlled by the "normalized" magnitude components in the $\Delta X$ and $\Delta Y$ registers, and by the input clock signal (VC1 COUNT CLOCK L derived from PCC DIS CLOCK L). The COUNT X and COUNT Y clock frequencies may be equal to or lower than the frequency of VC1 COUNT CLOCK L (5 MHz). The contents of the $\Delta X$ and $\Delta Y$ Registers are also compared with each other and the larger of the two is loaded into the Down Count Register to control vector length. As the vector is being drawn the Down Count Register is clocked by either COUNT X or COUNT Y; the vector stops when the Down Count Register = 0.

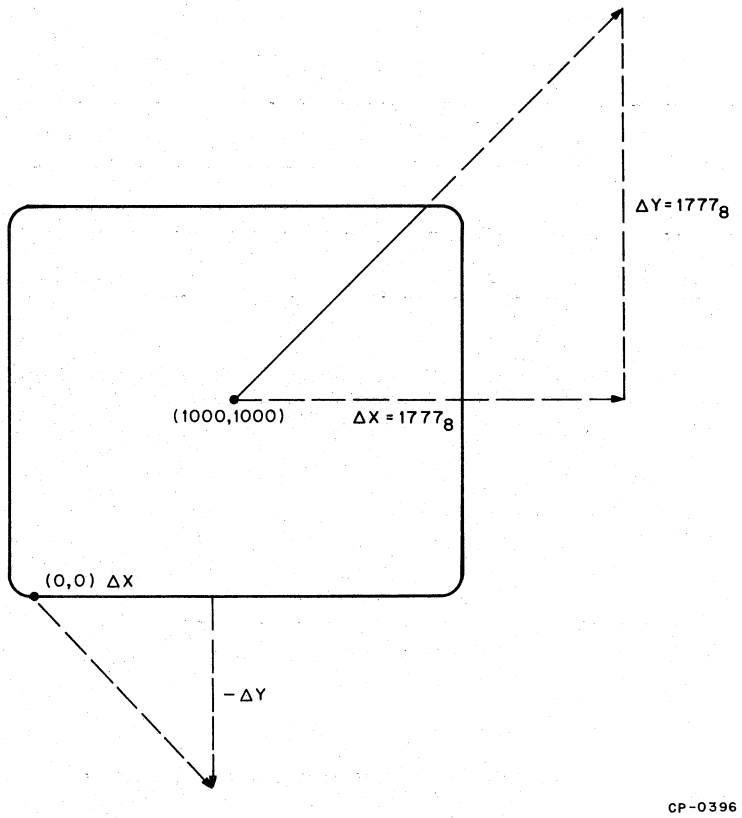



Figure 2-22 Cut-Off Vector Displays

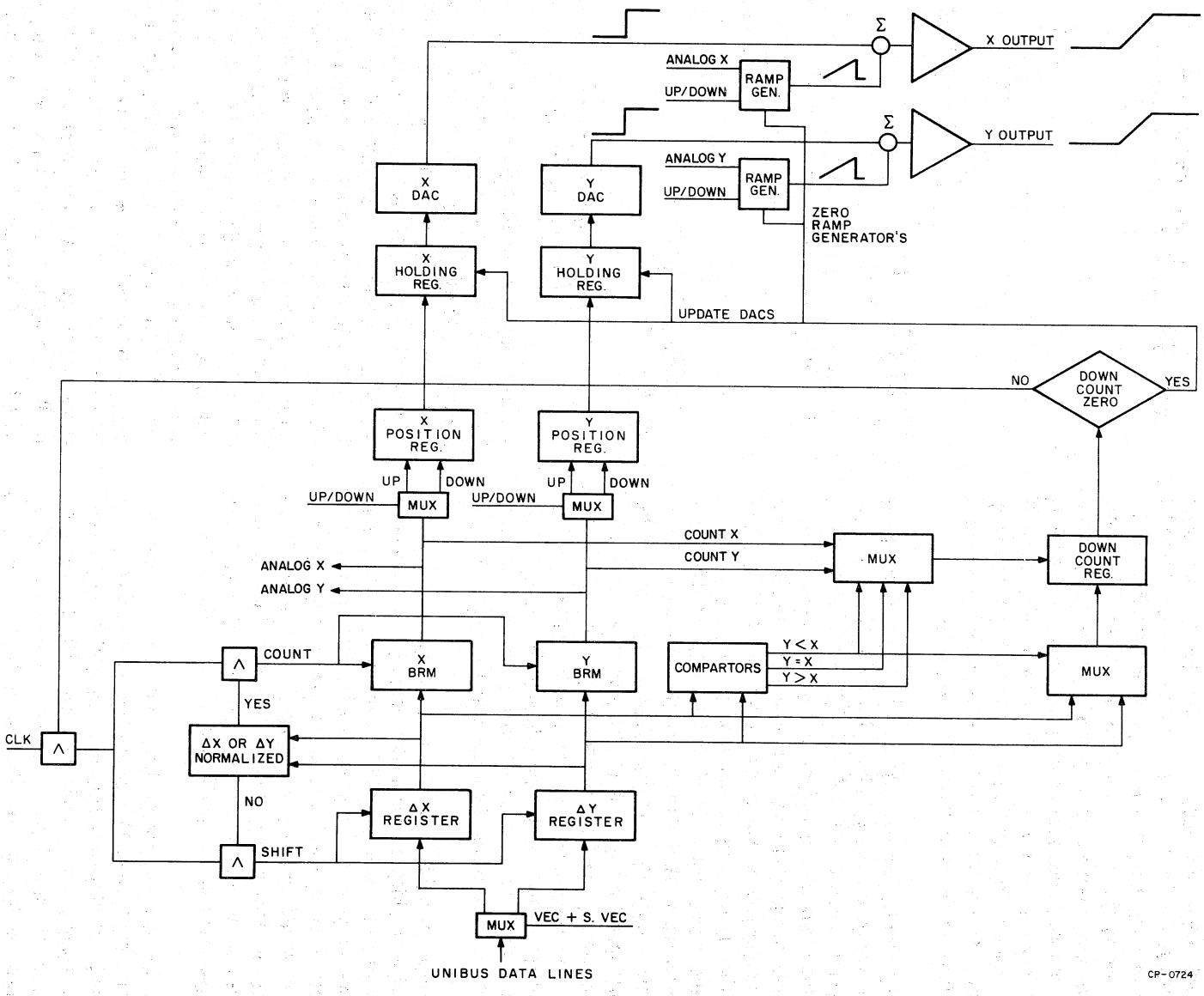



Figure 2-23 Vector Generator, Block Diagram

The X Position and Y Position Registers are continually being up-counted or down-counted while the vector is being drawn; therefore, they are dynamic registers in that they reflect the current beam position. (In the event of an LP interrupt while the vector is being drawn, the exact coordinates of the LP hit are available to the PDP-11.) These two registers, shown on drawing A320-PR, can be direct set as the result of a Point instruction. As in the programming example given in Table 2-8, this instruction could be used to pre-position the beam prior to intensifying a vector. At the end of the vector the value held in the X and Y Position Registers is gated into the X and Y Holding Registers. As a result, the DACs' outputs hold the unintensified beam at the point where the vector stopped.

**2.2.10.2 Normalization** – As noted previously, the angle of the vector on the CRT is a function of the relative frequency of the COUNT X and COUNT Y clock pulses. With the occurrence of each pulse, current is injected into a capacitor in the respective ramp generator and the output ramp rises proportionally as shown in Figure 2-24. It can be seen that it takes twice the time to attain a particular capacitor charge when the clock rate is halved. Therefore, the faster the clock rate the faster the capacitor is charged and the sooner the vector is drawn. Since one of the primary objectives is to draw the vector in the shortest possible time, it can be concluded that the fastest possible clock rate should be used. This is the purpose of the normalization process in the ΔX and ΔY Registers: to decrease the time it takes to draw a vector as much as possible and still retain the same X and Y magnitude ratio.

The longest possible vector has a magnitude of $1777_8$. It is clocked at a 5 MHz rate and takes about 200 μs to draw. A vector of half that length ($1000_8$) also takes about 200 μs to draw because it is clocked at a 2.5 MHz rate. If it is possible to clock the $1777_8$ length vector at the 2.5 MHz rate, it would take twice as long for the vector to be completed. This is not desirable (nor is it done) because time is critical; it shows, however, the relationship between the clock rate and the time it takes to display the vector.

When the two long vector data words are read from core memory, the ΔX and ΔY magnitude bits are loaded into the ΔX and ΔY Registers (drawing A320-BRM and Figure 2-19). Assume, for example, that ΔX = $+0170_8$ and ΔY = $0017_8$, a 8:1 ratio. The ΔX component, being the larger of the two, is loaded into the Down Count Register to establish the absolute vector length and then the contents of the two Δ registers are simultaneously shifted left until the high order bit of one of them equals 1; in this example, the ΔX component becomes $1700_8$ and the ΔY component becomes $0170_8$. Now normalized, they are the largest possible figures that retain the 8:1 relative size ratio. However, the higher figures allow higher COUNT X and COUNT Y clock rates from the BRMs and consequently the vector is drawn in the shortest possible time.

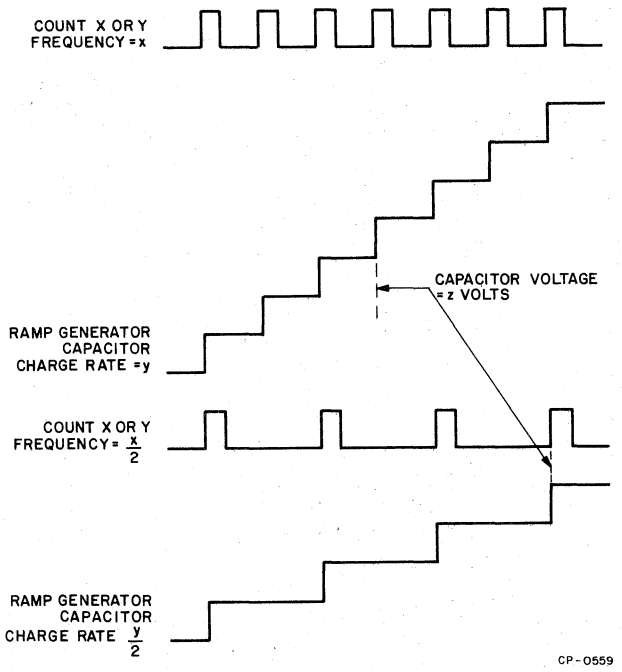



Figure 2-24 Relationship of Clock Frequency to Ramp Generator Output

**2.2.10.3 Binary Rate Multipliers** – The 7497 Binary Rate Multiplier chips, two for X and two for Y, are shown on drawing A320-BRM. This circuit performs a fixed-rate division of the 5 MHz input clock pulse, VC1 COUNT CLK L. The output of the BRMs is the input clock multiplied by the binary number in the ΔX and ΔY Registers after normalization. At this time the maximum vector magnitude component ($1777_8$) is unchanged because the MSD already equals 1. However, the smallest magnitude ($0001_8$) is $1000_8$ after normalization. Therefore, within the ΔX and ΔY pair for a single vector the larger (controlling) magnitude component is within the $1777–1000_8$ range after normalization. Consequently, all vectors assert a COUNT X (or COUNT Y, as determined by which is the larger Δ component) at a rate between 2.5 and 5.0 MHz; even very short vectors are drawn at a relatively fast rate, never at less than half the maximum 5 MHz rate. (The smaller Δ component of the vector word can, of course, be $<1000_8$ after normalization; it does not affect the drawing rate.)

**2.2.10.4 Vector Generator Synchronization** – The adjusted clock pulses, COUNT X and COUNT Y, from the BRMs are used to synchronize the internal operation of the vector generator. They simultaneously cause additional

current to be input to the ramp generator capacitors, increment (or decrement if the data word bit 13 = 1) the X and Y Position Registers (absolute vector length), and decrement the Down Count Register (COUNT X performs this last function if the register was loaded with ΔX data; COUNT Y if loaded with ΔY data). Therefore, the output analog ramp is increased, the Y and X Position Registers are updated to reflect the current beam position, and the remaining count in the Down Count Register becomes less – all in unison, as controlled by the COUNT X and COUNT Y pulses.

Figure 2-25 is a timing diagram for two consecutive vectors. The first has a ΔX = +1000 and a ΔY = +1777. The second has a ΔX = +1000 and a ΔY = -1777. (All figures represent normalized magnitude components.) The COUNT Y clock is the same frequency as the system clock and the COUNT X frequency is one-half the COUNT Y frequency. Thus the X ramp slope is one-half the Y ramp slope. When the Down Count Register equals 0 the first vector is concluded. The ramp generator output returns to zero and the DACs are updated from the X and Y Position Registers to hold the now unintensified beam at the point where the vector stopped. The signal VC2 VEC GEN OP DONE H is now asserted signifying the completion of the operation. This signal sets the NPR flip-flop and the data words for the second vector are read from core memory.

The second vector, which has a negative Y ramp, starts at the point where the first vector terminated. Since the magnitude of the two vectors are the same, the second will be the same length as the first. However, it will be drawn in the top to bottom direction. Again, at the conclusion of the vector, the ramp generator returns to zero and the DACs are updated to hold the unintensified beam at the new location. Note that during the first vector both position registers were incremented, but during the second vector the Y Position Register was decremented while the X Position Register was being incremented.

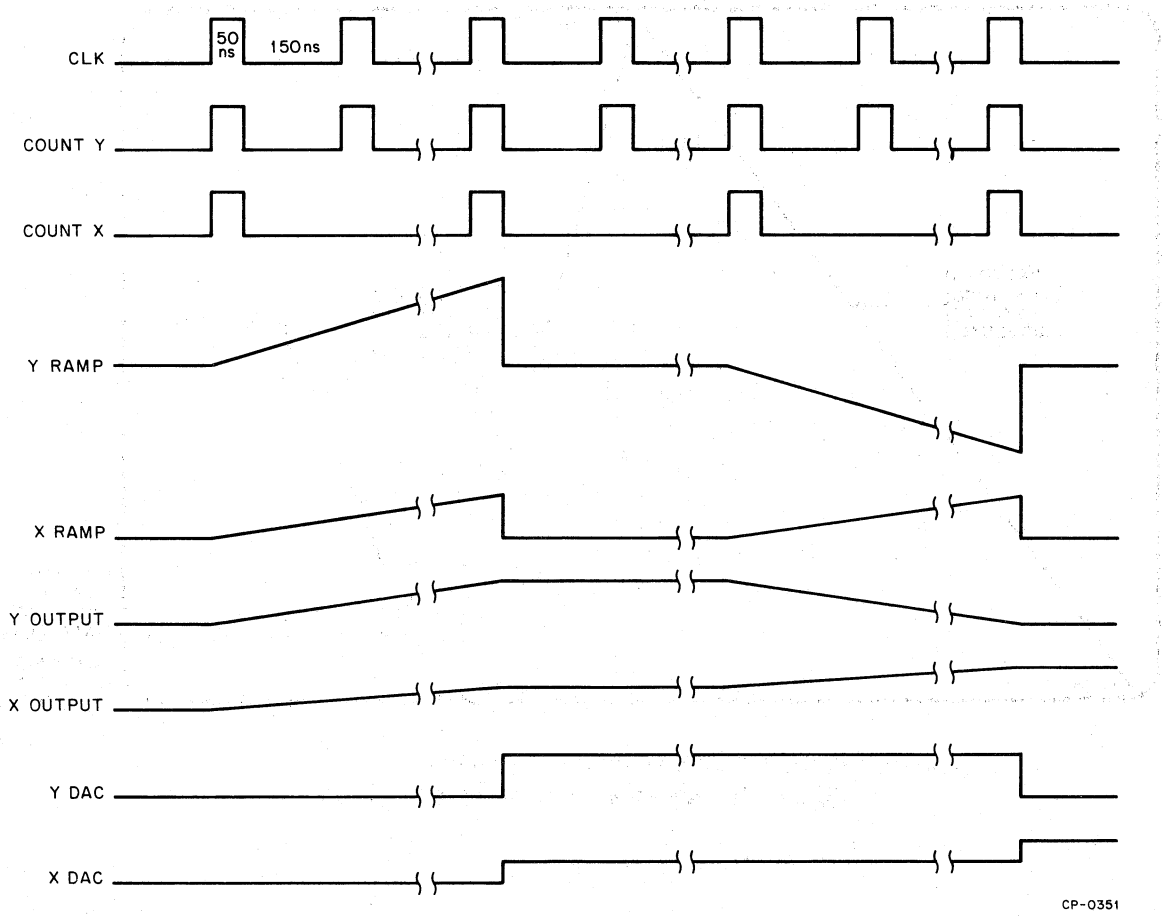



Figure 2-25 Vector Generator, Timing Diagram

Three consecutive vectors are shown in Figure 2-26. Vector 3 also shows the result of normalization; although shorter than the first two vectors, it is drawn at almost the same rate.

A unique condition exists if both ΔX and ΔY components indicate zero length vectors. If normalization were attempted the logic would be caught in an endless loop. Therefore, the Down Count Register, loaded before normalization, is checked for a zero length vector; if this is indicated, the vector instruction is aborted.

### 2.2.11 Point Intensification

After a Set Graphic Mode instruction has placed the VT11 Display Processor in the graphic mode and loaded the Data Mode Register with the Point code (Paragraph 2.2.8.5) the first of the two Point data words is read from memory (Paragraph 2.2.9). At this point the mode decode logic asserts MD POINT H indicating how the present and successive data words on the Unibus are to be treated.

The PVCS Word flip-flop, reset by MD CLR WORD L when the Set Graphic Mode instruction was read, and MD POINT L, assert PVCS POINT WORD 0 H. This signal performs two functions: first, it generates the PVCS LOAD X L signal at TD LOAD PULSE time, and then it sets the NPR flip-flop at TD TP2 time. PVCS LOAD X L loads the 74193 4-bit binary counters of the X Position Register (drawing A320-PR) with the X coordinates from the bus data lines [BDL DB (09:00) L].

The second Point data word is placed on the Unibus in response to the NPR. The PVCS Word flip-flop, which was set on the trailing edge of the first data word TP2 pulse, now asserts PVCS LOAD Y L at TD LOAD PULSE time and the Y coordinates are loaded into the Y Position Register. The X and Y Position Registers now contain the two 10-bit position coordinates that will shortly be converted, in the DACs, to an analog voltage for the VR14/VR17.

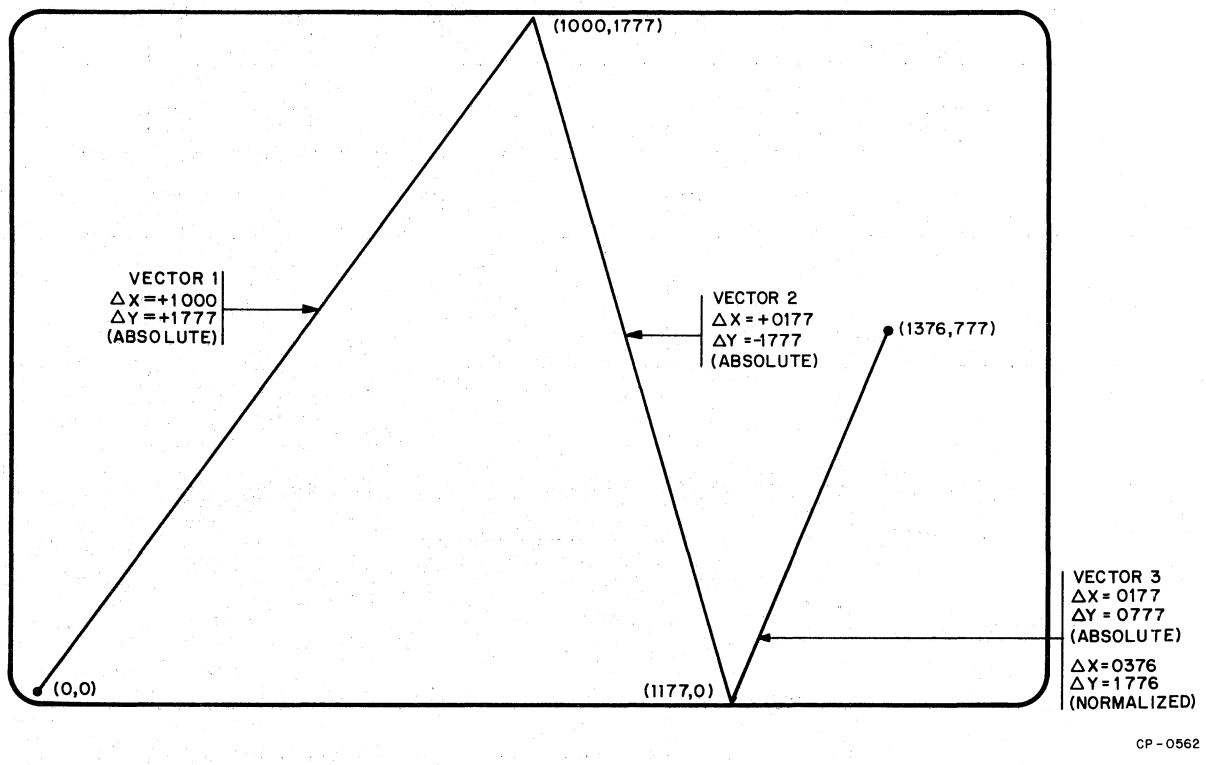



Figure 2-26 Absolute and Normalized Magnitude

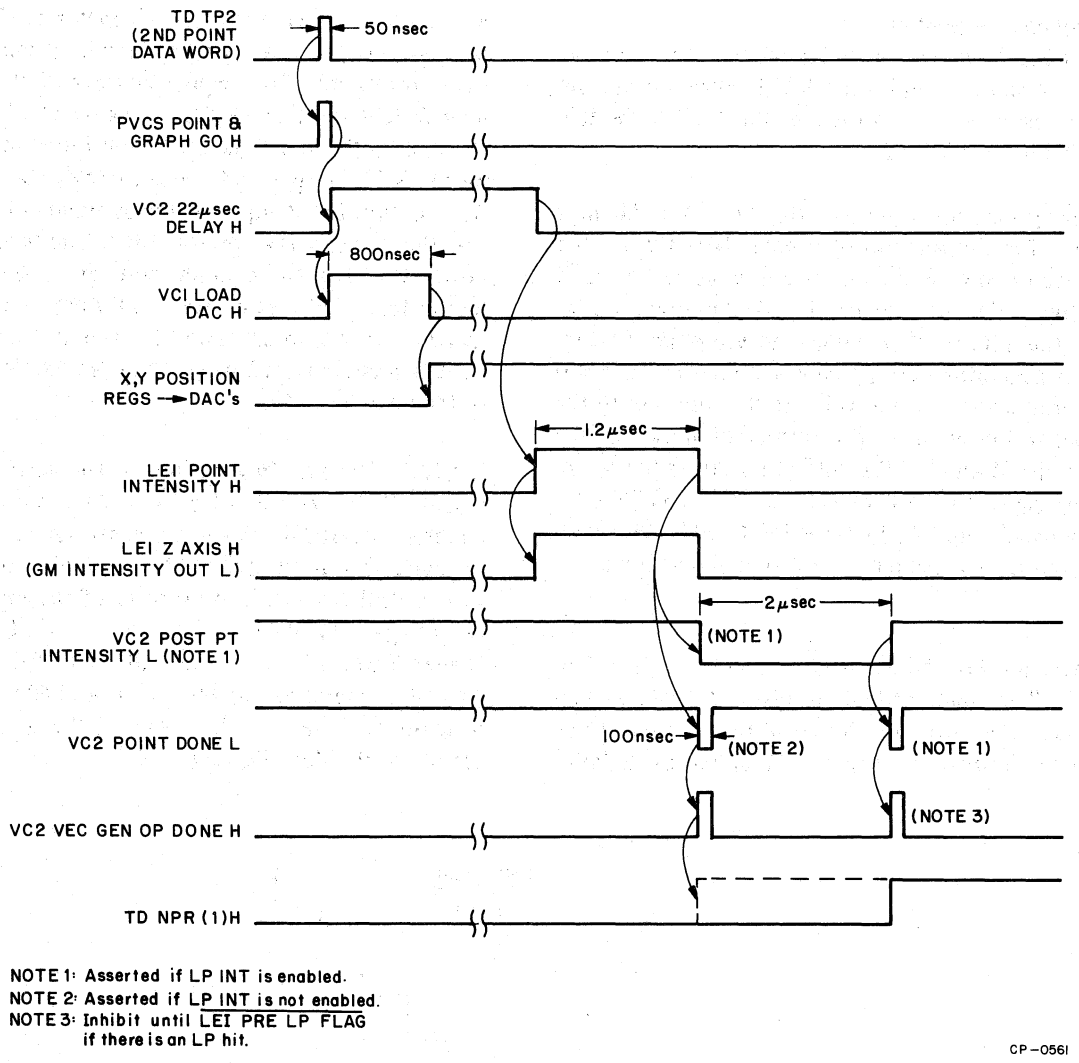



Figure 2-27 Point Instruction (Termination), Timing Diagram

At TP2 time of the second data word the NPR request is inhibited because PVCS POINT WORD 0 H went false when the PVCS Word flip-flop was set. On the trailing edge of TD TP2 H, PVCS POINT + GRAPH GO H goes low (Figure 2-27) to trigger a 74123 Single Shot (drawing M7014YA-VC2) which asserts VC2 22 μs DELAY H. At the trailing edge of the 800 ns VC1 LOAD DAC H signal asserted by this signal, the data in the X and Y Position Registers is gated into the respective DACs (drawing A320-DAC). The DACs' analog outputs are summed in the X and Y summers (drawing A320-CGS), which assert CGS X OUT and CGS Y OUT to the VR14/VR17 via the scope cable. These signals are then employed in generating the X and Y deflection voltages to the CRT yokes. About 21 μs after the DACs are loaded and the CRT yokes have had time to settle, the LEI POINT INTENSITY H and LEI Z AXIS H signals are brought up. The latter signal is transmitted to the VR14/VR17 as GM INTENSITY OUT L, where it causes the CRT cathode to go low and unblank the beam.

One of two signals is asserted at the trailing edge of the 1.2 μs LEI POINT INTENSITY H signal. If LP interrupts are not allowed (GM LP INTRUP ENA (0) H is high) VC2 POINT DONE L is generated immediately (drawing M7014YA-VC2). However, if LP interrupts are allowed VC POINT DONE L is delayed an additional 2 μs by a 74123 single-shot (VC2 POST PT INTENSITY L, Paragraph 2.2.8.5). In either case, VC2 POINT DONE L asserts VC2 VEC GEN OP DONE H which, in turn, sets the NPR flip-flop and the next word (point data word or control instruction) is read. If there was an LP hit on this point VC2 VEC GEN OP DONE H is inhibited until the LEI PRE LP FLAG flip-flop is reset by ASL CLR FLAGS L.

### 2.2.12 Character Generation

The 127 different characters and symbols (Appendix A) that can be displayed with the VT11 result from the decoding of character data words in the M7013 module (Paragraph 2.2.9 and Figure 2-19).

The character generation logic uses six 256 X 4 ROM chips as the source for character display data. Directed by the M7013 character control circuits, this data develops the X and Y analog deflection signals and the intensity pulses required by the VR14/VR17. Similar to vector generation, the character generator uses the same summers in the A320 module to produce the analog voltages that are sent to the X and Y deflection circuits. The output of these circuits then goes to the X and Y CRT yokes to position the beam. The enabling signal to the CRT cathode, GM INTENSITY OUT L, is derived from CCL1 CHAR INTENSITY H, which is asserted each time a character dot is to be intensified.

All characters are intensified in the manner illustrated in Figure 2-28. The unintensified or blanked beam is pre-positioned near the lower left corner of the character to be displayed (the bottom of column 1) either by a Point instruction, if this is the first character displayed, or after the previous character is completed if several characters are being displayed. The display starts with the beam being moved right and then vertically as a result of the X step and Y ramp to the summers. Dot intensification is determined by the ROM output and control circuits. At the top of the first column the X input to the X summer is stepped again and the Y ramp reverses direction. The beam now sweeps down the second column and the required dots are intensified. This sequence continues until the beam traverses all six columns and then, unintensified, is moved right a predetermined distance in preparation for the start of the next character.

**2.2.12.1 General Description** – The character generator (Figure 2-29) consists of a bit (Y) counter, a column (X) counter, the ROM, and input character register and word selector, an output shift and intensity circuit, and timing and control circuits. The majority of the logic is shown on drawings M7013-CCL1 and CCL2. Drawing D-FD-GT40-0-14 is a flow diagram for the character generator operation; drawing D-TD-GT40-0-16 is a timing diagram for this circuit. Figure 2-30 is an abbreviated version of the flow diagram.

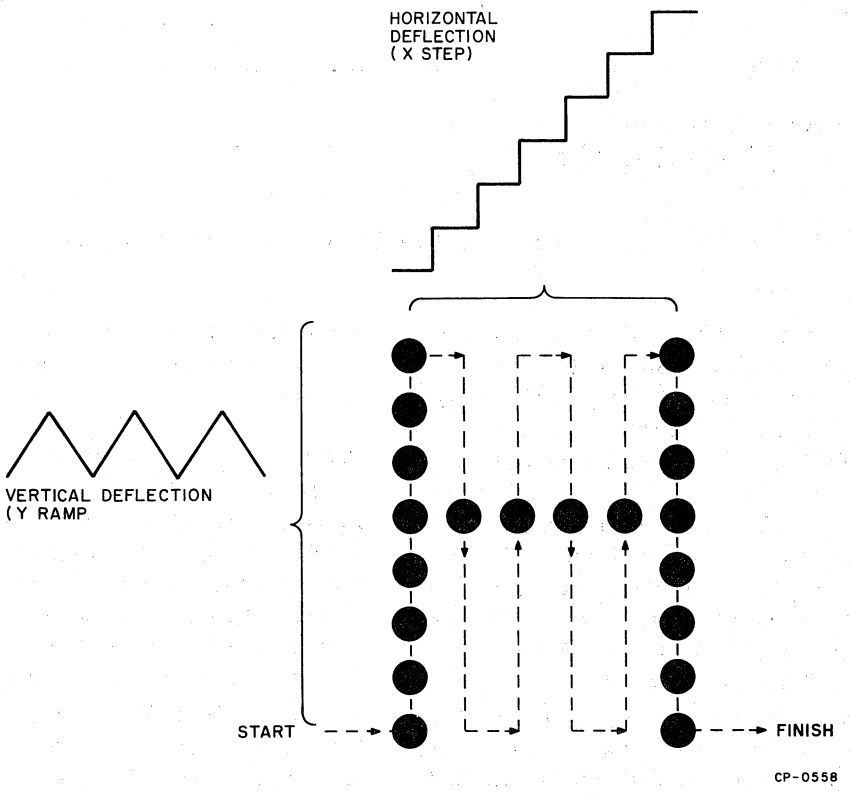



Figure 2-28 Path of Electron Beam as Influenced by X and Y Deflection Signals

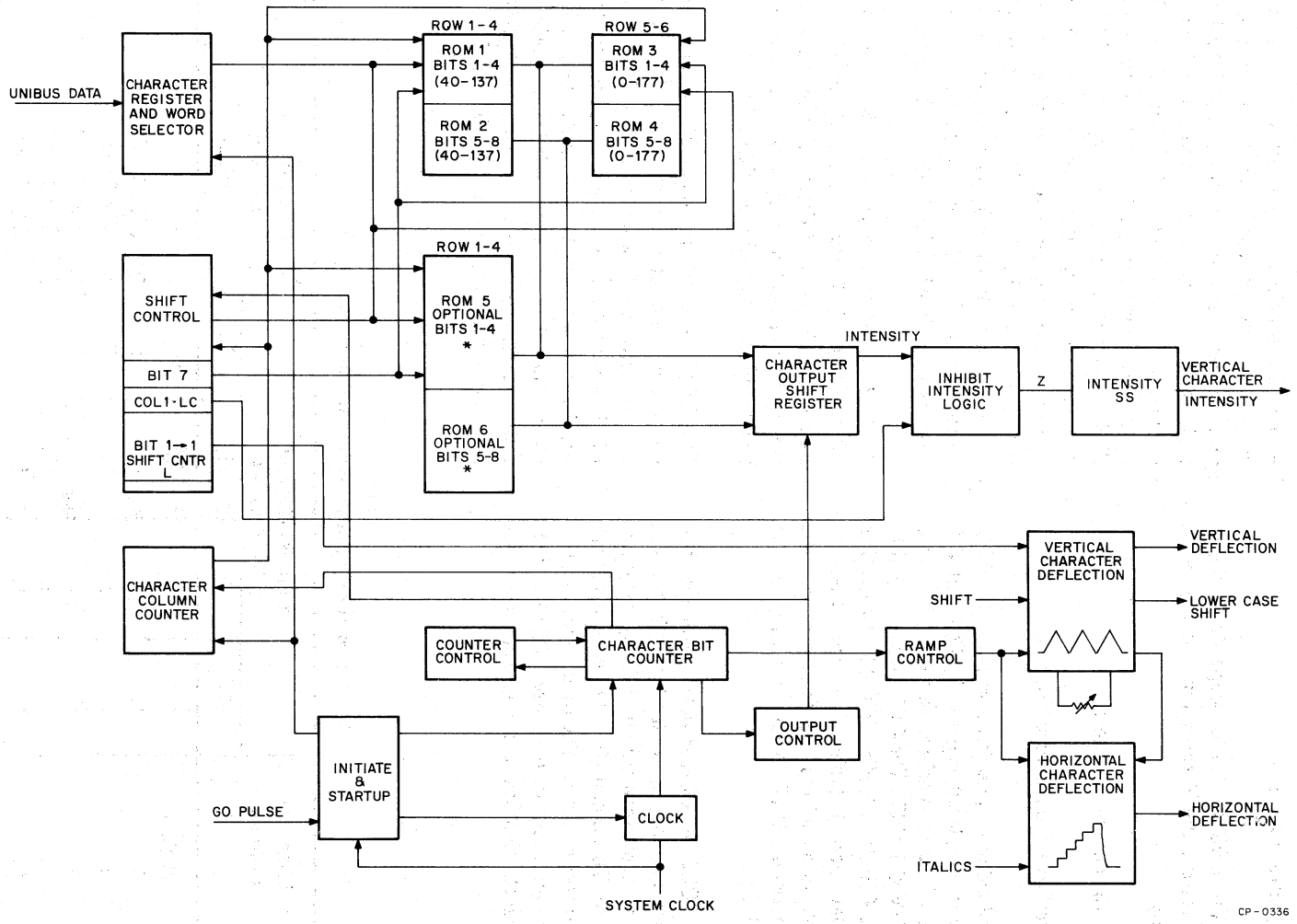



Figure 2-29 Character Generator, Block Diagram

**2.2.12.2 Character Bit Counter and Decoder** – The function of this circuit (drawing M7013-CCL2) is to determine the correct time to:

a. load the output shift registers with the column intensity information;

b. trigger the 0.98 to 1.4 μs scope delay single-shot to reverse the Y axis ramp and step the X axis ramp;

c. advance the column counter;

d. reset itself to a decimal count of zero.

The bit counter, following an initialization (BCL INIT H), or when a character is completed, is preset by CCL2 EOC L to a decimal count of 12 to synchronize the X, Y, and Z delays in the VR14/VR17 CRT. The CRT delay is equal to four times the CCL2 CHAR CLK H period (4 X 0.4 μs) plus the single-shot delay period (adjustable from 0.98 to 1.4 μs). This variable delay allows the delay period to be adjusted to the particular CRT. Nominal setting of the single-shot delay is 1.2 μs.

With the advent of CCL2 GO CLK H pulses after the Run flip-flop has been set, the counter counts from 12 to $15_{10}$, overflows naturally to zero, then counts to $10_{10}$ and resets on the eleventh pulse. This count (0 – 11) is repeated for each of the six character columns. The final count of $11_{10}$ is gated with a column count of 6 to assert CCL1 CHAR GEN DONE H, which signifies the completion of the character.

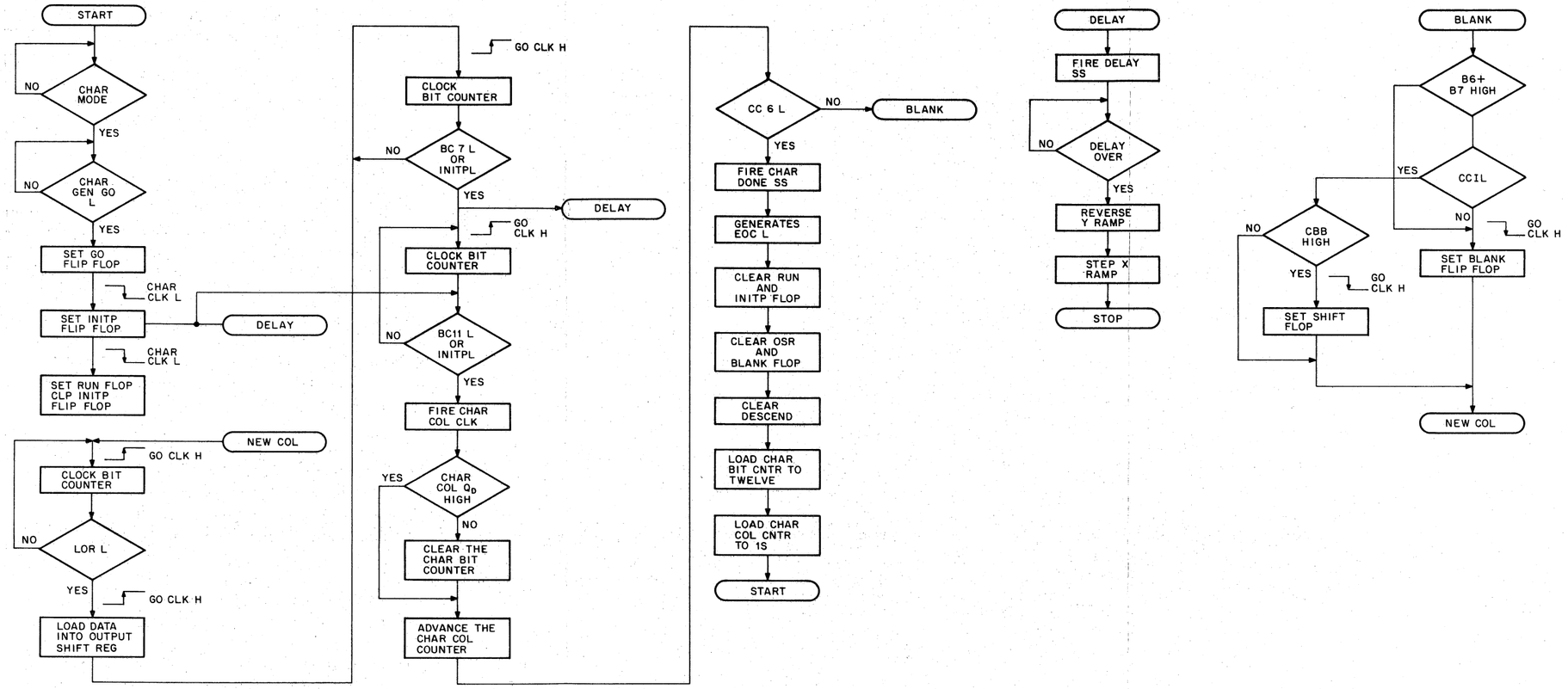
**2.2.12.3 Character Column Counter and Decoder** – Consisting of a 4-bit synchronous counter and a 4-to-10 line decoder, this circuit (drawing M7013-CCL1) is preset to a count of $15_{10}$ at the end of each character (and during power initiation) by a CCL2 EOC L pulse. Signals generated during the timed operation are shown in Table 2-9. The counter outputs are used to select which pair of ROMs are read to the Character Output Shift Register. The CCL1 COUNT 4 L signal is low when the Character Column Counter contains a count of 0 through 7. This condition allows the Character Bit Counter to be cleared by CCL2 CLK H when it reaches a count of $11_{10}$. (There is no count of $11_{10}$ during the time the first column is displayed; therefore, the Character Bit Counter cannot be cleared during this period.) The CCL1 CC1 L output from the decoder is used in the shift and unblank circuits described below. CCL1 CC6 L, the last output for each character, asserts CCL1 CHAR GEN DONE H (Paragraph 2.2.12.2).

**2.2.12.4 ROM Organization** – The intensity information for the 127 ASCII characters is stored in six 256 X 4 bit ROMs (drawing M7013-CRD). The outputs of these ROMs are of the open-collector type that allow all outputs to be connected in a wired-OR configuration.

Two ROMs are read simultaneously to obtain intensity data for a 8-bit character column. This is repeated for each column until the character is displayed. A total of four ROMs are accessed for any one character. To address the ROMs, the six-by-eight bit character matrix is divided into blocks that are related to individual ROMs. Figures 2-31 and 2-32 illustrate this division of the ROMs; Table 2-10 lists the contents of all six ROMs. ROM outputs can be

**Table 2-9**
**Character Column Counter and Decoder**

| Character Column | Counter Outputs CCL1 COUNT | | | | Asserted Decoder Output |
|---|---|---|---|---|---|
| | 4L | 3L | 2L | 1L | |
| (EOC) | H | H | H | H | |
| 1 | L | L | L | L | (CCL1 CC1 L) |
| 2 | L | L | L | H | (Pin 2-low) |
| 3 | L | L | H | L | (Pin 3-low) |
| 4 | L | L | H | H | (Pin 4-low) |
| 5 | L | H | L | L | (Pin 5-low) |
| 6 | L | H | L | H | (CCL1 CC6 L) |




CP-0337

Figure 2-30 Character Generator, Flow Diagram

verified by using Table 2-10 and Appendix A to determine which two ROMs a character column is associated with and then observing the ROM outputs on an oscilloscope. Synchronize the oscilloscope on the character column decoder output (Table 2-9) corresponding to the column that is being checked. Determine that each bit in that column is correct.

Each of the ROMs used has eight address lines and two chip enable lines. Manipulation of these ten lines produces the organization described above. ROMs 1 and 2 are used for columns 1–4, bits 1–8. Both receive identical address codes. The two chip enables are connected to ASCII bit 7 (CCL1 B7 H) and the CCL1 COUNT 3 L output of the column counter. This means that the chip is only enabled when both are low; this is true during columns 1–4 for these two ROMs. The remaining address lines, beginning with the MSD, are then controlled by ASCII bits 1–6 and the CCL1 COUNT (2:1) L outputs of the column counter. This provides a unique address for each column of intensity data.

ROMs 3 and 4 addressed in exactly the same manner as ROMs 1 and 2 except that an inverted ASCII bit 7 (CCL1 B7 L) controls one of the chip enable lines. This results in these two chips being enabled for columns 1–4 of ASCII codes 100–$177_8$. ROMs 5 and 6 have both chip enable lines connected to the inverted 2 output (CCL1 COUNT 3 H) of the column counter. These two chips are enabled for columns 5 and 6 because CCL1 COUNT 3 H goes low when the count exceeds 4. The address lines are connected, in addition to CCL1 COUNT 1 L, to all seven ASCII bits and therefore decode the full set of codes (000–$777_8$).

**2.2.12.5 Intensity Output and Control** – This circuit (drawing M7013-CCL1 and Figure 2-33) consists of two type 74194 4-bit Shift Registers connected to form a single 8-bit register, a 7473 J-K Mode Control flip-flop, a 74123 Intensity Pulse Single Shot, a 7474 D-type Edge Detector flip-flop, and associated AND and OR gates.

The two bidirectional shift registers form a parallel-to-serial converter for the ROM data. This data is input, one column at a time in parallel format, shifted at the bit clock rate, and output as serial data to the VR14/VR17. The operation begins, for each character, when the Character Bit Counter reaches a count of two and the load output register (CCL2 LOR L) signal forces both S0 and S1 mode lines high (the required configuration for loading the register). The rising edge of the same CCL2 GO CLK H signal that asserted CCL2 LOR L also loads the input from the ROMs into the shift register.

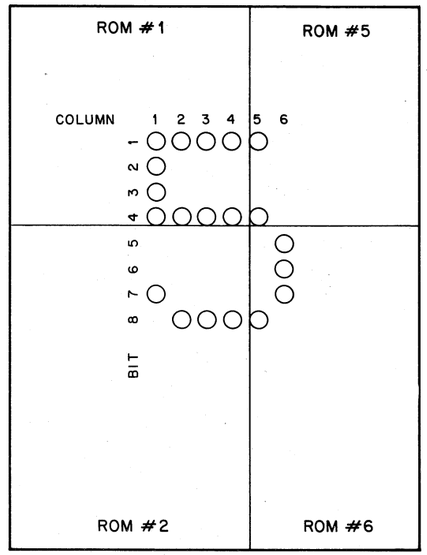



Figure 2-31 ROM/Character Relationship

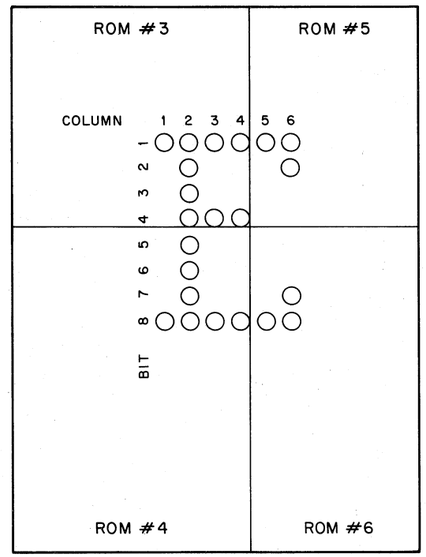



Figure 2-32 ROM/Character Relationship

**Table 2-10**
**Character ROM Contents**

| ROM | Character Columns | Column Bits | ASCII Codes (Octal) |
|---|---|---|---|
| 1 | 1–4 | 1–4 | 000–077 |
| 2 | 1–4 | 5–8 | 000–077 |
| 3 | 1–4 | 1–4 | 100–177 |
| 4 | 1–4 | 5–8 | 100–177 |
| 5 | 5–6 | 1–4 | 000–177 |
| 6 | 5–6 | 5–8 | 000–177 |

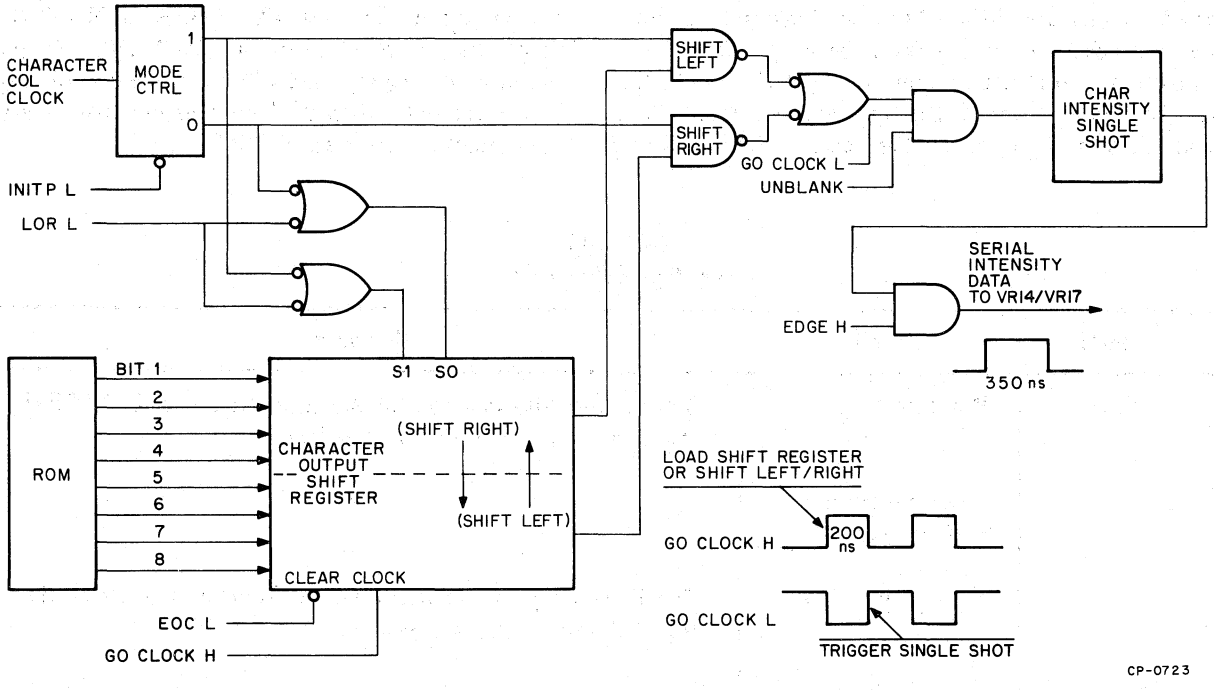



Figure 2-33 Generation of Intensity Data to the VR14/VR17

The Mode Control flip-flop, reset by CCL2 INIT P L at the beginning of each character, is ORed with CCL2 LOR L to control the S0 and S1 control lines. When CCL2 LOR L goes high and the mode control output causes the control lines to assume the shift right configuration, S0=H and S1=L. If the first bit (8) to be displayed is a 1, the trailing edge of CCL2 GO CLK L (the reciprocal of the CCL2 GO CLK H pulse that loaded the register) triggers the character intensity single shot. The resultant 350 ns CCL1 CHAR INTENSITY H pulse is sent to the VR14/VR17 (as GM INTENSITY OUT L) and the lower-left character dot is intensified. This would be the case, for example, if the character is an "H" as in Figure 2-28. Note that the Unblank flip-flop must be set and the unintensified beam positioned in the visible portion of the CRT (LEI EDGE H) before any serial data can be transmitted.

The shift register is shifted right on the leading edge of the next CCL2 GO CLK H pulse. Bit 7 is now on the output line from the register and is transmitted on the trailing edge of CCL2 GO CLK L. This shift-transmit sequence is repeated for each dot in the first column that is to be intensified (0 bits are shifted but the single-shot is not triggered when they are output from the shift register). At the completion of the first column CCL2 CHAR COL CLK L sets the Mode Control flip-flop and advances the Character Column Counter to the second column. The mode control lines are now in the shift-left configuration: S0=L and S1=H. The shift is changed from shift-right to shift-left operation because the first column of dots is displayed as the beam moves toward the top of the character and the next column is displayed as the beam moves downward. This alternating between shift-left and shift-right continues until the character is completed, at which time the Unblank flip-flop is reset and further CCL1 CHAR INTENSITY H pulses are inhibited.

The period of the single-shot is adjusted for a duty cycle of 75 percent (350 ns). This provides an intensity pulse that produces maximum character brightness. The use of a single-shot also prevents burning of the phosphor in the event of a failure, e.g., clock pulse failure, in the logic prior to that point.

**2.2.12.6 Operational Sequence** – Character generation begins with the assertion of the end of character (CCL2 EOC L) signal in the M7013 module (drawing M7013-CCL2). This signal, generated at the conclusion of each character display (CCL1 CHAR GEN DONE H) or when power is first brought up (BCL INIT H), performs certain housekeeping functions to ensure that the logic is in the correct state when the next character display is started. These functions are listed in Table 2-11.

**Table 2-11**
**EOC Signal Functions**

| Function | Circuit | Remarks |
|---|---|---|
| Clear | Run Flip-Flop | Inhibit erroneous displays following power up. BCL INIT P H also clears the Go flip-flop at this time. |
| | Character Output Shift Register | |
| | Ramp Y Flip-Flop | The first sweep of the beam will be from the bottom to the top of the first character column. |
| | Descend Flip-Flop | |
| | Unblank Flip-Flop | Inhibit display until 1st or 2nd character column. |
| Preset | Character Bit Counter | $= 12_{10}$ |
| | Character Column Counter | $= 15_{10}$ (Inhibits clearing the bit counter during the first column.) |

The character generation logic remains quiescent until the first character data word following a Set Graphic Mode instruction asserts MD CHARACTER L. At TD LOAD PULSE time the two 7-bit characters on the Unibus data lines are clocked into the Character Register (drawing M7013-CCL1). (Succeeding data words are treated identically.) PVCS WORD 1 H is low at this time and therefore the output [CCL1 B (7:1) H] of the Character Word Selector is determined by the contents of the first character on the bus data lines [BDL DB (06:00) H]. The Character Word Selecter output provides the memory address for the ROM. Consequently, the intensity information for the first character column (of the first of two characters) is read from the ROM and sent to the Character Output Shift Register at TD LOAD PULSE time of the data word. Accessing ROM is the first event in the display of any character. At the conclusion of the present character display, the Word flip-flop is toggled by VC2 VEC GEN OP DONE H (derived from VC1 DONE L) and the second 7-bit character in the Character Register [BDL DB (14:08) H] furnishes the memory addresses for the ROM. This switching from one 7-bit input to the other continues as successive character data words are read from core memory (Figure 2-34).

At TD TP 2 time of each character data word the signal PVCS CHAR GEN GO H is asserted. Unless a space character is decoded or a control character (codes 000 through 037) is not preceded by Shift Out (CSC SO L), CSC ENABLE PRINT H is asserted and ANDed with PVCS CHAR GEN GO to generate CSC PRINT CHAR L. The leading edge of this signal, which must be asserted before any character can be displayed, sets the Go flip-flop and a synchronization sequence is initiated. Timing for character display is derived from the 5 MHz system clock (PCC DIS CLOCK H) which triggers a J-K flip-flop to assert the 2.5 MHz (400 ns period) signals CCL2 CHAR CLK H and CCL2 CHAR CLK L. The Init P flip-flop is set on the leading edge of the first CCL2 CHAR CLK L pulse after the Go flip-flop is set. This marks the point where the command is synchronized to the character generator clock. CCL2 INIT P L and CCL2 INIT + INIT P L now clear the Go flip-flop and trigger the 0.98–1.4 $\mu$s scope delay (Paragraph 2.2.12.2) and the character clock single shots. The 400 ns CCL2 CHAR CLK L signal also steps the Character Column Counter to an all zero output. This causes the Character Column Decoder to assert CCL1 CC1 L (Table 2-9) to denote column one is being displayed.

The Run flip-flop is set and the Init P flip-flop is cleared by the next CCL2 CHAR CLK L signal. CCL2 GO CLK H is now asserted every 400 ns until the Run flip-flop is reset after the last column is displayed. CCL2 GO CLK H pulses, which follow the CCL2 CHAR CLK H pulses, are used to up count the character bit counter; this operation is now started. At a point determined by the setting of the scope delay single-shot, the Step single-shot is triggered to assert CCL2 STEP X H and the Ramp Y flip-flop is set. The CRT beam is moved (right) to the bottom of the first character column and CCL2 RAMP Y (1) H starts the vertical sweep.

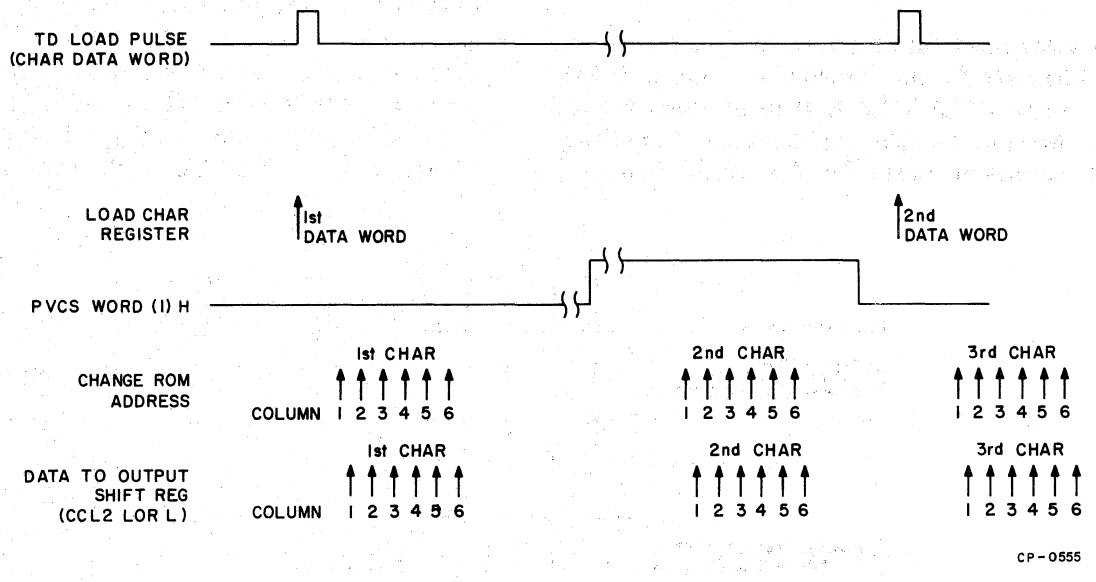



Figure 2-34 Word Selection and ROM Addressing, Timing Diagram

The scope delay single-shot is adjusted so that this repositioning of the beam coincides with the assertion of CCL2 LOR L; this occurs when the bit counter = $2_{10}$. Provided a lower-case character is not decoded (ASCII bits 6 and 7 = 1), the Unblank flip-flop is set on the leading edge of the next CCL2 GO CLK L pulse. On the trailing edge of the same signal the character intensity single-shot is triggered if the lower left dot is to be displayed. The beam is now sweeping up and the Character Output Shift Register is shifted right; the display of the first character column is underway.

The Character Bit Counter continues to up count and the CCL1 CHAR INTENSITY H pulses are asserted when a dot is to be displayed. Both of these functions occur at a rate determined by the CCL2 GO CLK pulses (Figure 2-35). When the bit counter reaches a count of 7, CCL2 DEFL DONE is asserted and the 0.98–1.4 μs scope delay single-shot is triggered again in preparation for the second column display. The signal CCL2 CBC11 L, generated when the bit counter reaches a count of 11, triggers a 100 ns single-shot to assert CCL2 CHAR COL CLK L and CCL2 CLK H. The Character Bit Counter, cleared by this latter signal, now restarts the 1–11 count sequence.

The signal CCL2 CHAR COL CLK L up clocks the Character Column Counter to cause the second column intensity data to be read from ROM; at the same time it toggles the Mode Control flip-flop in the character intensity circuit. This results in the Character Output Shift Register performing a shift-left for each dot position (intensified or not) in the second column.

The scope delay times out at approximately the same time that the Character Column Counter is up-clocked. This causes the signal CCL2 STEP X H to be asserted again, moving the beam to the right, and the Ramp Y flip-flop is reset; the downward sweep for the second column is started. The second column intensity pulse stream is generated in the same manner as when the first column was displayed except that it emanates from the opposite end of the Character Output Shift Register because the register is in a shift-left configuration.

At the end of the second column the Character Column Counter is clocked again and the third column display begins. The sequence continues until all six columns have been displayed at which time the seventh CCL1 CHAR COL CLK L pulse is ANDed with CCL1 CC6 L to assert CCL1 CHAR GEN DONE H (Figure 2-36). The first of two characters contained in the data word has been displayed. A timed sequence now starts. At the termination of this sequence the second character (if present) will be displayed.

After a 2.5 μs delay to allow time for the yokes to settle, CCL1 CHAR GEN DONE H causes the assertion of a 100 ns signal, TD RESTART H (drawing M7013-TD). This signal is only generated after the display of the first of two characters in a data word when PVCS WORD 0 H is high. The resultant TD SYNCH UP H synchronizes the system clock to the timing pulse generation logic and two, as opposed to the normal four (Paragraph 2.2.6), timing pulses are asserted. This is because TD RESTART L presets the 74193 4-Bit Binary Counter, Time Cnt Up, to a count of two. This causes the 74155, 1–4 line demultiplexer S1 input to be high and the S0 input to be low. Consequently, the next two PCC DIS CLOCK H pulses assert TD TP1 and TD TP2; TD LOAD MODE L and TD LOAD PULSE L are not generated. At TD TP2 L time the signal PVCS CHAR GEN GO H is asserted and display of the second character is initiated with CSC PRINT CHAR L.

When display of the second character is completed the same termination signals are repeated except that TD RESTART H (and subsequent signals) is inhibited. However, the NPR flip-flop is set by VC2 GEN OP DONE H because MD

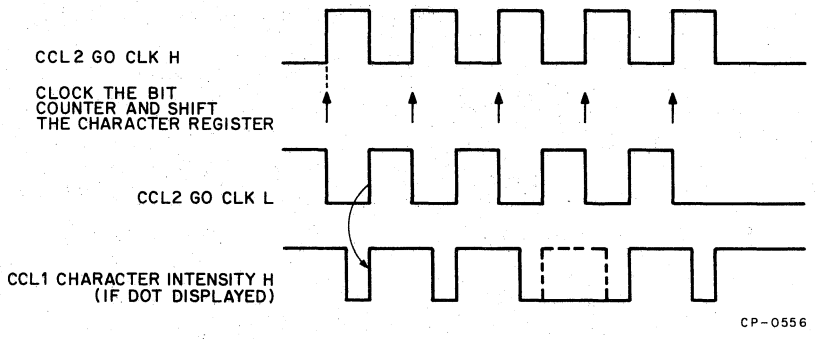



Figure 2-35 Character Bit Timing

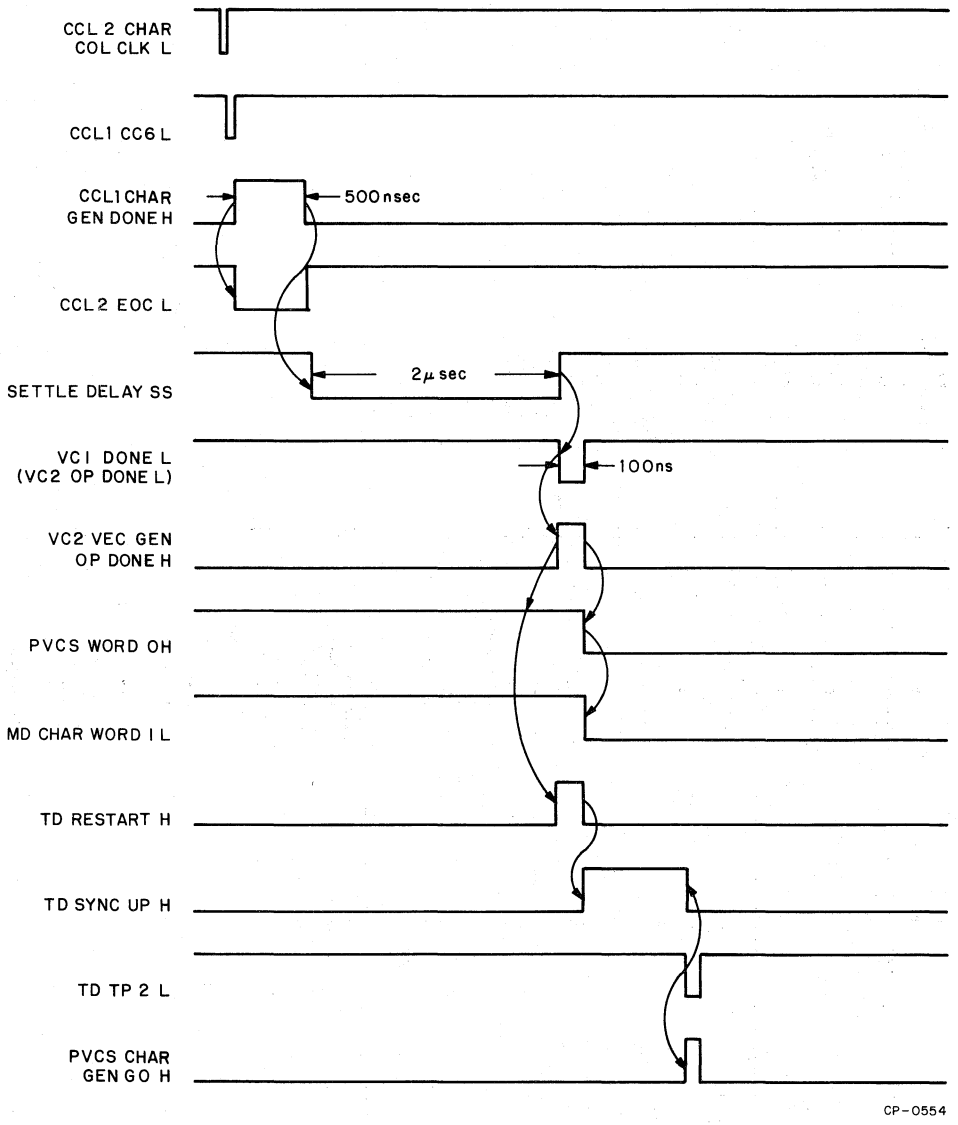



Figure 2-36 Character Timing Between Characters in a Single Data Word

CHAR WORD 1 L went low after the first character was displayed. The NPR will cause the next character data word to be read from core memory if additional characters are to be displayed.

**2.2.12.7 Character Spacing** – After each character is displayed the unintensified CRT beam is positioned near the bottom of column 1 of the next character (Paragraph 2.2.12). This intercharacter positioning sequence begins at TD TP2 time of each character when PVCS CHAR GEN GO L is asserted (Figure 2-37). This signal actuates the Time Shift Register (drawing M7014YA-VC1), which outputs a pair of timed pulses (VC1 TIME 1 H and VC1 TIME 2 H, Figure 2-38) and loads the Down Count Register (VC1 LOAD DOWN COUNT L) with a character space constant that represents the distance the beam is to be moved in X direction.

The constant (always a $14_8$ or $16_8$ unless LF or CR are specified) is derived from the character spacing logic (drawing M7014YA-PCC). Table 2-12 shows the outputs of this circuit as determined by the jumper configuration (W3, W4, W5, and W6) on the M7014YA module.

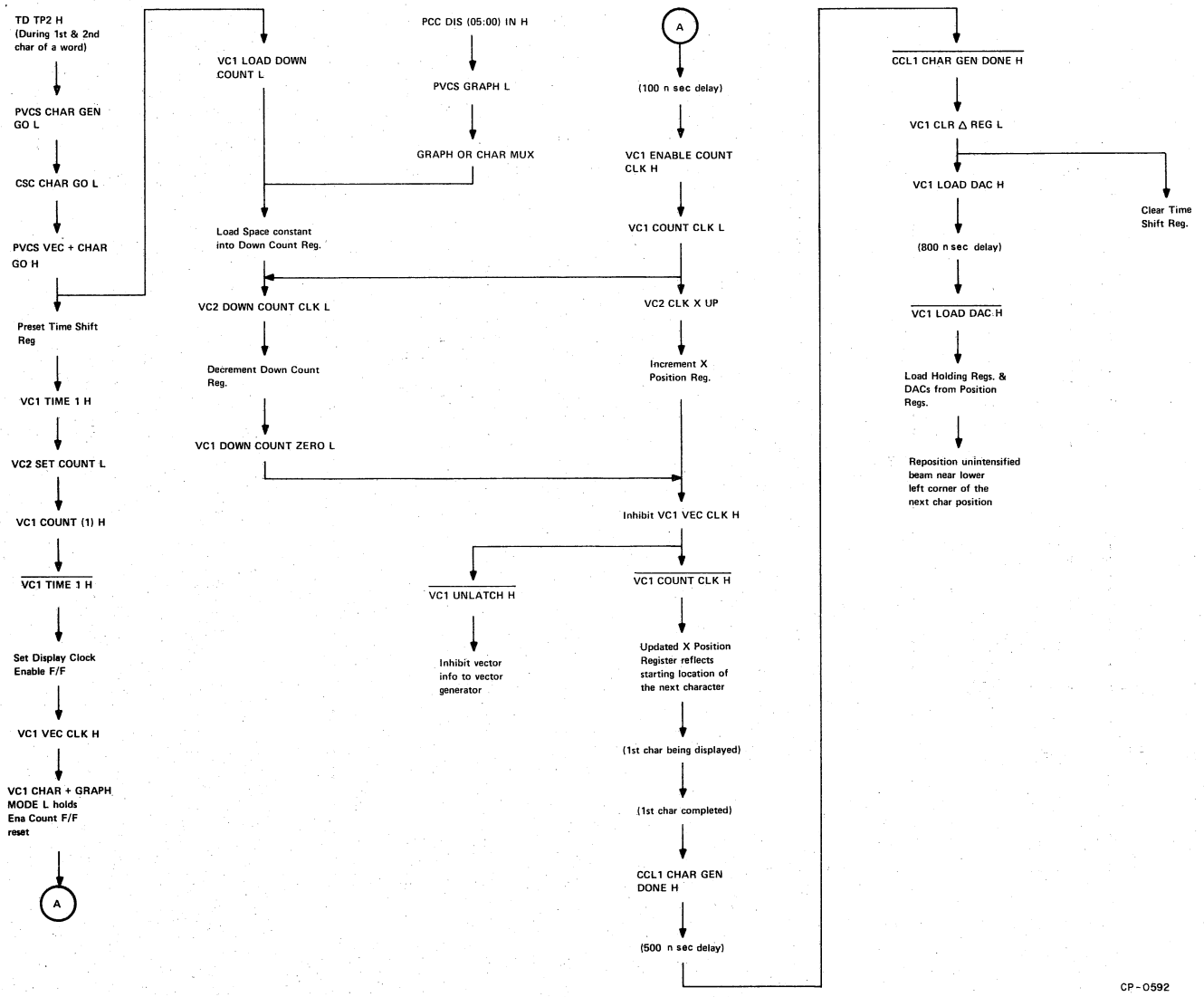



Figure 2-37 Intercharacter X Position Update, Flow Diagram

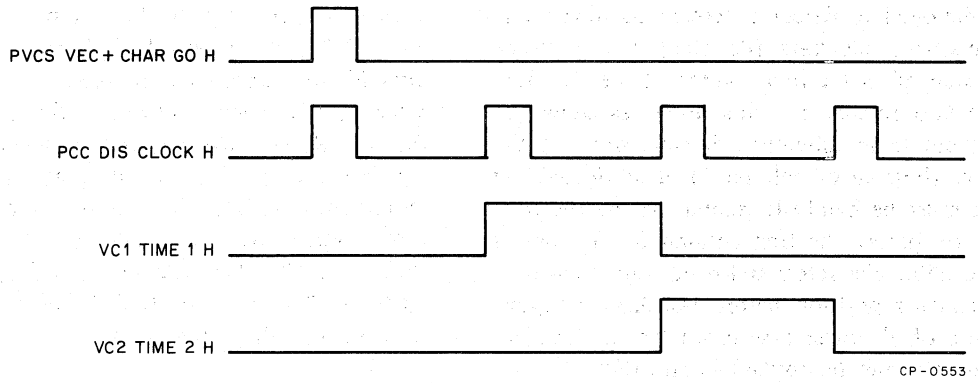



Figure 2-38 Time Shift Register, Timing Diagram (M7014YA-VC1)

**Table 2-12**
**Character Spacing Jumpers**

| Jumper In Place | Characters/Row | Rows | | Asserted Output* PCC DIS | | | |
|---|---|---|---|---|---|---|---|
| | | VR14 | VR17 | 4 IN H | 3 IN H | 2 IN H | 1 IN H |
| W3 | 85 | 29 | 39 | L | H | H | L |
| W4 | 73 | 29 | 39 | L | H | H | H |
| W5 | 73 | 31 | 42 | L | H | H | H |
| W6 | 85 | 31 | 42 | L | H | H | L |

*Unless CR or LF are asserted.

The space constant is loaded into the Down Count Register via the Graph or Character Multiplexer (drawing A320-DCR and Figure 2-12) because PVCS GRAPH L is high. After a delay, VC1 COUNT CLK L simultaneously increments the X Position Register contents and decrements the constant in the Down Count Register. This takes place at the 5 MHz system clock rate. When VC1 DOWN COUNT ZERO L is asserted (the count = 0) VC1 VEC CLK H goes low and incrementing of the X Position Register halts. This register now contains the X component of the starting location of the next character. No further action occurs in this operation until the conclusion of the character display when CCL2 EOC L is asserted. This signal ensures that the Y ramp is returned to the starting point and, unless LF is asserted, the Y Position Register remains unchanged. 500 ns later the trailing edge of CCL1 CHAR GEN DONE H asserts the 800 ns VC1 LOAD DAC H. (The 2 $\mu$s settle delay, whose function was previously mentioned, is also triggered at this time.) The holding registers and DACs are then loaded from the X and Y Position Registers on the trailing edge of VC1 LOAD DAC H. Since this occurs approximately 1.2 $\mu$s before VC2 BEC GEN OP DONE L is asserted, the CRT yokes have sufficient time to settle before TD RESTART H is asserted or an NPR is issued.

**2.2.12.8 Descending Characters** – The Descend flip-flop and the gating necessary to detect a descending lower case character, i.e., j, g, p, q, and y, constitute the digital portion of the descend control (drawing M7013-CCL2). ASCII bits 6 and 7 (CCL1 B6 H and CCL1 B7 H) are examined during character column 1 (CCL1 CC1 L) to determine if a lower case character is to be printed and then the ROM output is tested (CRD CB 8 H) for a descending character. If all conditions are met, the Descend flip-flop is set on the trailing edge of the first CCL2 GO CLK H pulse. The portion of the descend circuit on the analog module (drawing A320-CSG) consists of a resistor and a diode that form a voltage divider. The voltage at their juncture provides one of the inputs to the Y summer. When a descending character is detected [CCL2 Descend (0) H goes low] the output of the 7417 Buffer forces this point to ground and effectively shifts the vertical position of that character downward by the correct amount.

The method employed to detect a descending lower case character necessitates blanking (deleting) the intensity information contained in the first column of these characters. There are two reasons for this. First, as shown in Figure 2-39, there is an inherent "descend dot" at the lower-left corner (bottom of column 1) of all descending characters that must be blanked; second, during the time normally used to display the first column the Y yoke is shifted for descending characters and needs time to assume the modified starting position before the display begins. The first column of all lower case characters is therefore blanked in order that they be displayed uniformly.

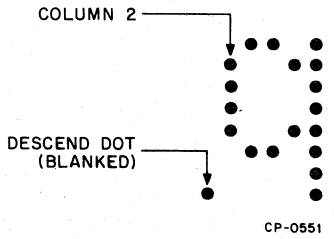



Figure 2-39 Descending Character (Ex: Lower Case Q)

**2.2.12.9 Y Axis Ramp Generator** – This circuit (drawing A320-CGS) consists of a positive and negative current source, an LM302 Buffer, and a 0 V clamp. The positive source is turned on and off by the CCL2 RAMP Y (1) H signal generated in the logic. The negative source provides one-half the current of the positive source and is adjustable to provide for tolerance variation in the circuits, most notably the 5 percent Zener diodes. Figures 2-40 and 2-41 are simplified schematics of the positive and negative sources, respectively. In the positive current source, Zener diode D31, R121 and C72 form a voltage divider and establish the operating potential on the base of Q34. D31 is a 5.6 V, ±5% Zener and essentially establishes the current through R122 since the emitter-base drop of Q34 nearly equals the forward voltage drop across D15. D15 provides temperature stabilization to offset changes occurring in Q34's $V_{BE}$ due to temperature variation. The current through R122 then becomes $V_Z/R_{R4}$ or approximately 2.06 mA. This current, ±6%, is then the collector current for Q34 (actually $I_c$ = alpha X $I_E$).

Source switching is accomplished by means of R119, R120, D14, and the SN7417 Open-Collector Buffer. When the output transistor of the buffer is turned on, the collector goes to 0.4 V and forces the junction of R119, R120, and D14 to approximately 6 V. D14 is now forward biased and places the emitter of Q34 at approximately 6.6 V. This turns Q34 off since the base emitter junction is now reverse biased with the base setting at approximately 8.8 V. When the output transistor of the SN7417 turns off, the junction of R119, R120, and D14 rises at an exponential rate toward +15 V. D14 will again become reverse biased allowing Q34 to turn on and deliver current to the capacitor. The rise time of the signal on the output of the buffer is less than 100 ns, even with the addition of the scope probe capacitance (less than 13 pF). The fall time is much less since the point is actively pulled down by the buffer, less than 20 ns. R123, D16, and D17 form a clamp that prevents the voltage on the capacitor from going more negative than 0 V. 0 V was chosen as the clamp point for two reasons. First, no offset would be introduced into the summing amplifier due to the character generator signal.

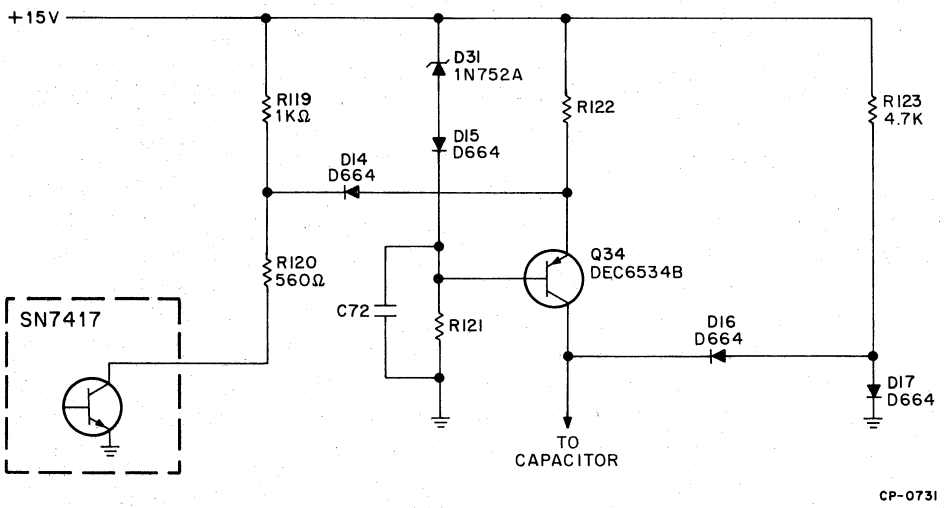



Figure 2-40 Positive Current Source

Second, the LM302 Buffer is capable of delivering more current when operating between 0 V and +15 V than when it operates in the negative region. This allows the use of smaller resistors in the voltage divider following the buffer and minimizes the resistance change due to the italics switch. This resistance change had to be minimized to reduce as much as possible the gain change when the character display alternates between italicized and normal type.

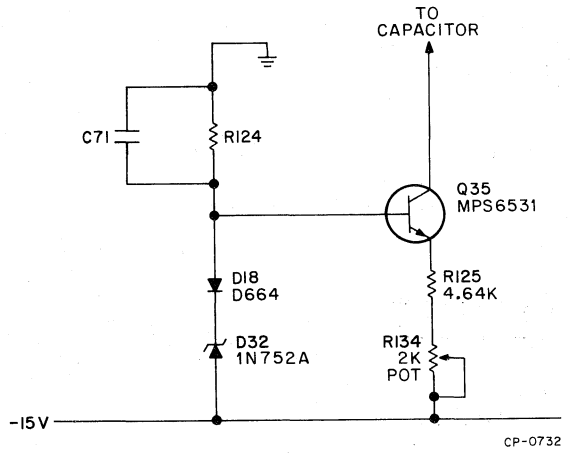



Figure 2-41 Negative Current Source

The negative current source, Figure 2-41, remains on at all times and supplies one-half the current of the positive source. When no character is being printed, the positive source is off and the negative source is on.

The ramp capacitor is discharged until the clamp activates and delivers the 1.04 mA of current to the capacitor. Half of this goes to the negative source, while the remaining half deposits a charge on the capacitor. The charge rate may be determined from the formula $\Delta e/\Delta t = I/C$ and is about 1.04 V/$\mu$s. The negative source is identical to the positive source except for polarities and values. R134 is necessary to allow for Zener tolerance and provides approximately +12 percent adjustment of the negative current from the nominal value.

An LM302, Figure 2-42, buffers the voltage appearing on the capacitors in the X axis and Y axis ramp generators. The 15K resistor, used in series with the input, protects the buffer should a short circuit condition exist on its output. The output signal is reduced in amplitude by a voltage divider and summed with other signals in the summing amplifier. The gain of the summing amplifier with respect to the character generator signal is approximately unity.

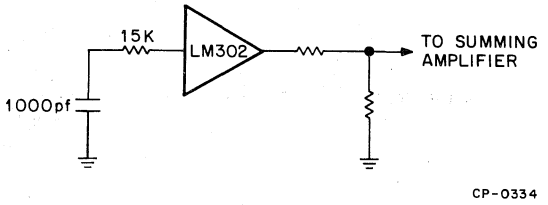



Figure 2-42 LM302 Diagram

**2.2.12.10 X Axis Ramp Generator** – The X axis ramp generator is identical to the positive source for the Y axis ramp generator. The input to it is a 200 ns positive pulse, CCL2 STEP X H, each time a new character column is to be displayed. This produces a stair-step voltage on the capacitor rather than a ramp as in the Y axis. At the completion of each character, the logic signal, CCL2 RUN (0) H, goes high turning on the transistor switch across the capacitor and discharging it to ground.

**2.2.12.11 Italics Switch** – The italics control consists of two transistors, four resistors, and three diodes (Figure 2-43). R45, D23, D24, and D25 form a voltage divider that biases the emitter of Q17 at 1.8 V and allows the transistor to operate from a TTL level output. A logic 1 on the base of Q17 turns it off since the emitter is at 1.8 V. With Q17 off, no base current is supplied to Q16 and it is also turned off. R44 serves to bypass some of the current supplied by Q17 so that a smaller stored charge is produced, thus enabling Q16 to turn off more quickly. With Q16 off, the Y axis deflection is summed with the X axis deflection and sent to the X summing amplifier. This action produces the italics effect. A low level on the italics input turns both Q16 and Q17 on and grounds the Y axis deflection at the junction of R42 and R43. Figure 2-43 also shows the waveforms that appear at various points in the circuit.

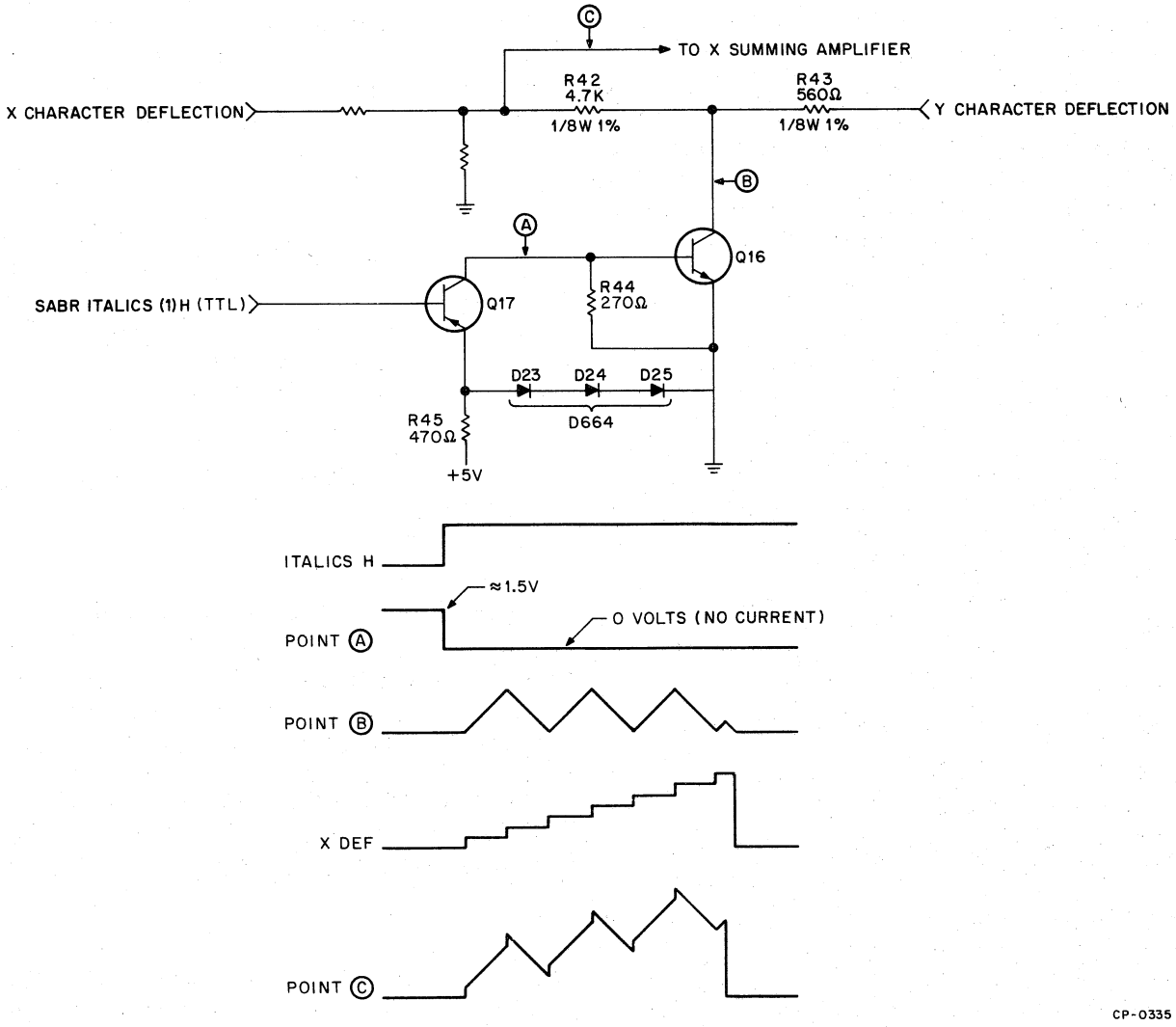



Figure 2-43 Italics Control Circuit

### 2.2.13 Analog Circuits

**2.2.13.1 General Description** – The digital quantities generated in the VT11 Display Processor must be converted to a corresponding analog value for the VR14/VR17 CRT Display to perform its required function. This operation is termed digital-to-analog (D/A) conversion. There are several factors consistent with all D/A conversion methods:

- The conversion must be performed as a bit parallel operation because at a given instant the analog equivalent of a binary number available at the same instant must be produced.
- Conversion always produces an analog voltage or analog current that is the equivalent of the digital input.
- The basic method of conversion is to produce for each 1-bit a voltage (or current) magnitude that is a function of the proportional weight of that bit and then add the several voltages (currents) to produce a summed analog output.

The VT11 A320 module analog circuit uses two LM318 Current Summers (Figure 2-44) to produce the required analog voltages to the VR14/VR17. The inputs to the summers are the X and Y DACs, vector generators, character generators, and the descend circuit. These circuits, with the exception of the descend and character analog circuits (Paragraphs 2.2.12.8 through 2.2.12.11) are described in the following paragraphs.

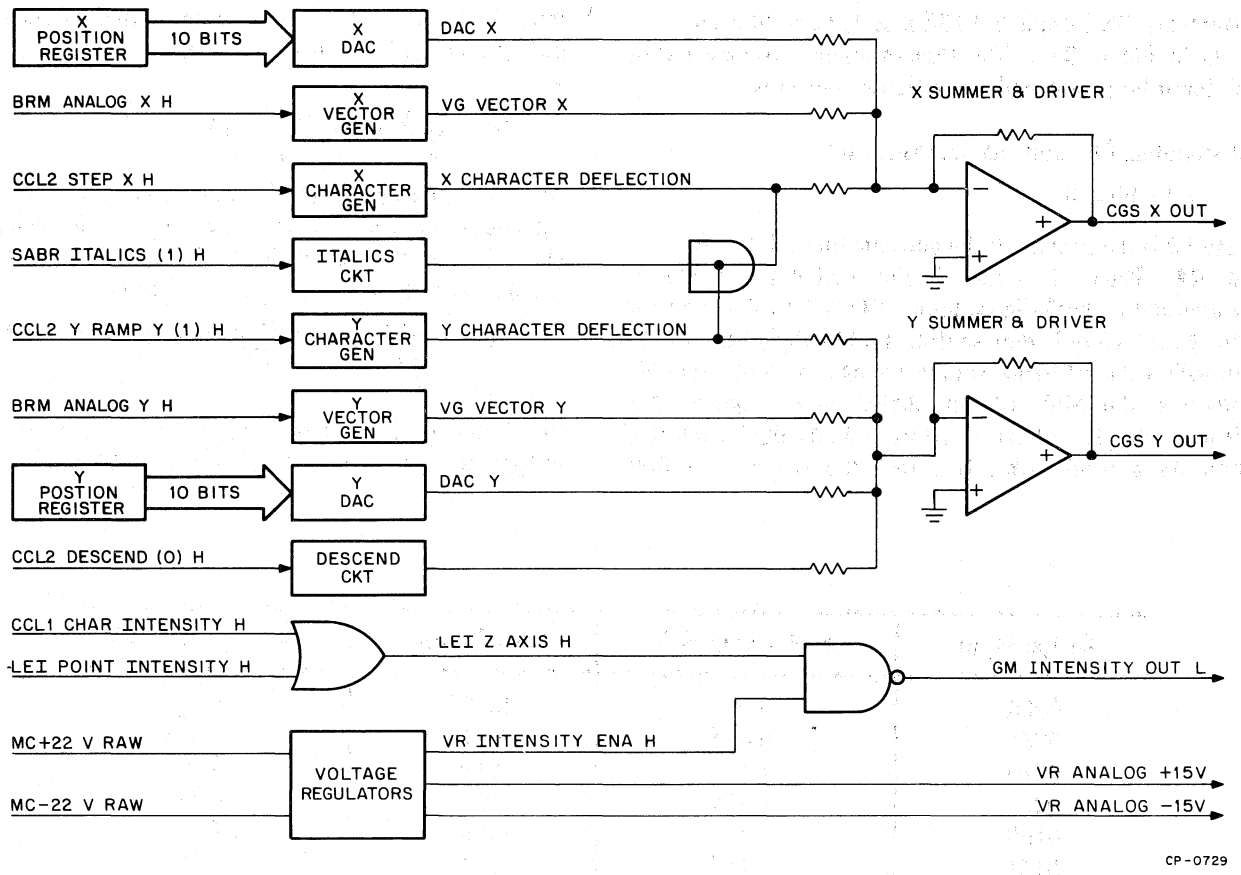



Figure 2-44 Analog Circuit, Block Diagram

**2.2.13.2 Voltage Regulators** – This circuit provides the regulated +15 and −15 V power for the analog circuits (Figure 2-44 and drawing A320-VR). Another output, VR INTENSITY ENA H, indicating a power-up condition, is ANDed with the intensity signal (LEI Z AXIS H) to assert GM INTENSITY OUT L. This signal turns on the CRT to intensify the beam.

Input power to the regulators is MC + 22 V RAW and MC −22 V RAW that originates in the VR14/VR17 and is delivered to the A320 module via the scope cable.

Operation of the +15 Vdc regulator is described below. The −15 Vdc regulator is functionally identical to the +15 Vdc regulator.

A Zener reference, formed by R52 and D28, is applied by R53 to the noninverting terminal of amplifier E2. The output of E2 is buffered by R57 from the current booster transistors Q18 and Q20. The output of Q20 is fed back, through current sense resistors R60 and R156, to the inverting terminal of E2. The feedback signal is attenuated by R61 and R62.

The output voltage will be: $V_z\ (1 + \frac{R61}{R62})$ or approximately +15 Vdc. Current limiting of the +15 Vdc regulator occurs whenever the voltage developed by R60 exceeds the base to emitter turn on voltage ($V_{BEon}$) of Q21. Once Q21 begins to conduct, it limits the base drive to Q18 the current booster transistor. Current limiting occurs when the output current exceeds 500 mA. A normally reversed biased diode (D7) is in parallel with the +15 Vdc regulator. In the event the +15 Vdc output is connected to a current limited negative voltage, D7 holds the regulator to the current limit and the output at a point just below ground (ground less the voltage drop across D7).

The outputs of the 15 V regulators are connected by jumpers to the remaining circuitry on the A320. This allows for external power supply connections, requirements are: +15 Vdc ±1%@500 mA, and −15 Vdc ±1%@500 mA.

**2.2.13.3 Digital-to-Analog Converters (DAC)** – The DACs used in the A320 module analog circuit employ current summing ladder networks similar in operation to the X and

Y summers (Paragraph 2.3.13.5). A typical 4-bit ladder is shown in Figure 2-45. The resistor values associated with each input bit produce binary-weighted currents.

The summing function characteristics are:

$$VO = IO \times R$$

where IO is the sum of all the currents through R1, R2, R3, and R4. Thus, if none of the switches are closed, representing a 0000 digital input, VO is 0 V. When all the switches are closed, representing a 1111 digital input, VO approaches the reference supply voltage. Assume that SW1 represents the MSB of the digital input register, the reference supply voltage is 10 V, and the digital input is 1000. As a result, SW1 is closed and the current flow through R1 is 10/2R. With no other switches closed, this is the total current through R. Therefore, the output voltage is:

$$VO = \frac{10\ V}{2R} \times R = \frac{10\ V}{2} = 5\ V$$

As a second example of the D/A conversion, assume that the digital input is 0101, causing switches SW2 and SW4 to close. Current through R2 is 10/4R and current through R4 is 10/16R. As a result, the output voltage is:

$$VO = \frac{10\ V}{4R} \times R + \frac{10\ V}{16R} \times R = 2.5\ V + 0.625\ V = 3.125\ V$$

The following DAC conversion table lists the 16 possible outputs that can be generated from a 4-bit input.

| Digital Input | Analog Output V | Digital Input | Analog Output V |
|---|---|---|---|
| 0000 | 0.0 | 1000 | 5.1 |
| 0001 | 0.625 | 1001 | 5.625 |
| 0010 | 1.25 | 1010 | 6.125 |
| 0011 | 1.875 | 1011 | 6.75 |
| 0100 | 2.5 | 1100 | 7.5 |
| 0101 | 3.125 | 1101 | 8.125 |
| 0110 | 3.75 | 1110 | 8.75 |
| 0111 | 4.375 | 1111 | 9.375 |

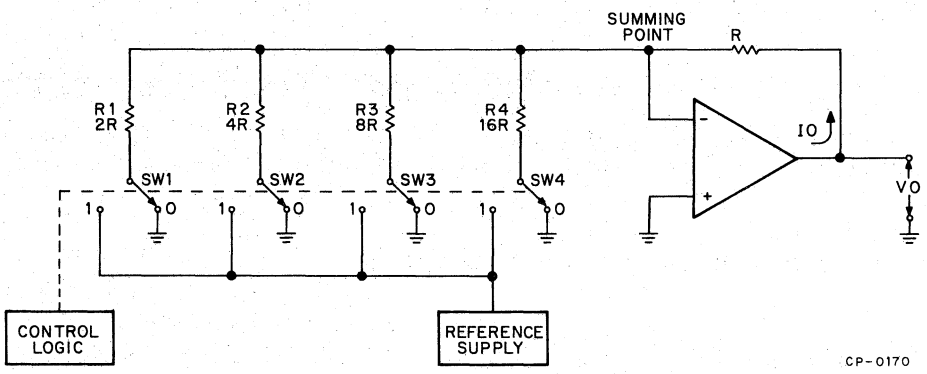



Figure 2-45 Typical Current Summing Ladder

To have good conversion accuracy, resistor values must be precise and the reference voltage supply must be well regulated.

The two DACs in the VT11 Display Processor generate a voltage (current) reflecting an absolute CRT position that is summed with the vector or character generator output. The type A6000 DACs used have a 12-bit input. However, in this application, they operate as 10-bit input circuits because the two least significant bits (pins 21 and 22) are connected to ground and therefore turned off. Operation is in the bipolar mode because offset pins 1 and 2 are connected together. The 10-bit inputs (from the X and Y Position Registers) exercise the DACs from + full output (+0.5 Vdc) to - full output (-0.5). These outputs are buffered by type LM310 Voltage Followers and then applied to the X and Y summing amplifiers.

Specifications for the A6000 are listed in Table 2-13.

**2.2.13.4 X and Y Vector Deflection Generators** – This portion of the analog circuit (drawing A320-VG) provides the X and Y ramps necessary to draw a vector on the CRT (Paragraph 2.2.10). Inputs to the vector generators are the BRM ANALOG X H and BRM ANALOG Y H pulses that are asserted until the Down Count Register = 0 (VC1 DOWN COUNT ZERO L) and PCC ANALOG CLOCK H which is derived from the system clock.

The X and Y circuits operate identically; only the X Vector Generator is described in the following paragraphs.

PCC ANALOG CLOCK H, a 10 MHz clock, is applied to the toggle input of a J-K flip-flop, E48. The J input and Q output of E48 are connected to a D flip-flop, E49, in such a fashion as to produce two clocked toggles of E48 following a preset of E49. (If the vector goes beyond the digital edge of the CRT flip-flop, E48 is held clear to prevent unnecessary analog movement outside the screen area.) When E49 is preset by a 50 ns BRM ANALOG X pulse, the next two clock pulses generate a 100 ns output pulse. The 100 ns pulse is applied to an inverter E42. The output of E42 drives the base of Q1. The emitter of Q1 is returned to ground through R11. R12 and R13 form a voltage divider that biases Q1's emitter via D3. When the base voltage of Q1 exceeds its emitter bias by the base to emitter turn on voltage, Q1 turns on and reverse biases D3. The magnitude of Q1's emitter current is $(V_{BASE}-V_{BEon})/R11$. D1 and D2 clamp Q1's collector voltage two diode drops below the Zener voltage developed by D44 and its bias resistor R152. Q1 operates in its active region when turned on. The on voltage of D1 cuts off Q2, reverse biasing Q2's base to emitter junction. When A1 is turned on and Q2 cut off the voltage across R5 is $(V_Z-V_{DIODE})$ or approximately +5.6 V. When E2 drives the base voltage of Q1 lower than the emitter set bias, Q1's base to emitter junction becomes reversed biased and Q1 is cut off. When Q1 cuts off, its collector uses the voltage set by the divider consisting of R4 and R3, turning Q2 on. When Q2's base-to-emitter becomes forward biased, D1 becomes reversed biased. When Q2 is turned on it operates in the active region; its emitter voltage is then a base-to-emitter drop below the voltage set at its base. When Q2 is on, its output voltage reverse biases D2 and Q2's current is limited by R5 to $(V_{BASE}-V_{BEon})/R5$. When Q1 is cut off and Q2 is turned on, the voltage across R5 is $+15V(R3)/(R3+R4)-V_{be}$, or approximately +12 V. The arrangement of Q1 and Q2 is such as to transform the 100 ns output pulse of E48 from logic levels to a 100 ns pulse that switches between +5.6 V and +12 V.

D27 and E31 provide a stable Zener reference. R6 and R7 feed back to E31's inverting terminal an attenuated version of the voltage at the junction of R6, R8, R9, and R10. E31 tends to correct for voltage variations at this junction, thus stabilizing the current through R9. With a fixed load across D27 the bias current through D27 will be stable.

The Zener reference created by D27 is applied to the inverting terminal of the amplifier composed of E26 and Q3. Note that this is the noninverting terminal of E26 but the inverting terminal of the composite amplifier [E26 and Q3]. The noninverting input of E26 and Q3 is connected by R15 to a variable offset voltage R131, R17, and R16 from an adjustable attenuator that effectively behaves by varying the voltage at the inverting terminal end of R14, thus varying the voltage drop across R14. When the voltage across R14 is varied the current flowing through R14, supplied by Q3's collector, is varied. A forward-biased, anti-latchup diode (D37) and R19 complete the feedback loop to Q3's base. Q3's emitter is returned to +15 Vdc via R20, a resistor that is equal in value to R14. The voltage drop across R20 will be nearly equal to the voltage drop across R14. Q4's base is connected to Q3's base and Q4's emitter is returned to +15 Vdc through R21. If the $V_{BEon}$ drops of Q3 and Q4 match and R21 equals R20, the voltage drop across R21 will equal the voltage drop across R20 when Q4 is on. Because the voltage drops across R21, R20 and R14 are equal and the resistor values are equal, Q4's collector current will be approximately equal to the current through R14 when Q4 is on. Q4's emitter is also connected via D4 to the source of the 100 ns pulse that switches between +5.6 V and +12 V. When the pulse level is at +5.6 V, D4 becomes forward biased and drives Q4's emitter voltage lower than its base voltage; this action reverse biases Q4's base to emitter junction and cuts off Q4. When the

Table 2-13
Type A6000 DAC Specifications (VT11 Configuration)

| Specification | Parameter |
|---|---|
| Current Output | ±0.5 mA (offset binary) |
| Resolution | 10 bits |
| Linearity | ±1/2 LSB |
| Voltage Accuracy | ±1/2 LSB (0.0122% of FSR)* |
| Zero Offset | ±1/4 LSB |
| Impedance | 1k (nominal) |
| Settling Time (to within 1/2 LSB for FS Step) | 750 ns for 10 bits |
| Power Supply Sensitivity | 0.005% of FSR/1% change in either supply |
| Temperature Coefficient | ±25 ppm/°C max of FSR |
| Inputs | 1 = +2.75 to +5.5 Vdc @ 50 mA max (current into DAC)<br>0 = 0.0 to +0.6 Vdc @ 0.8 mA max (current out of DAC) |
| DC Power | +15 Vdc ± 1% @ 35 mA max<br>-15 Vdc @ 25 mA max |
| Operating Temperature | +10 to +50°C ambient |
| Coding (Offset binary)<br>MSB LSB<br>1 1 1 1 1 1 1 1 1 1<br>1 0 0 0 0 0 0 0 0 0<br>0 0 0 0 0 0 0 0 0 0 | <br><br>+0.5 Vdc<br>0 Vdc (0 mA)<br>-0.5 Vdc |

*FSR – Full Scale Resolution.

**NOTE**

**Care should be exercised in maintaining the +15 Vdc supply at the correct level. This supply should not be operated lower than 1 percent below its nominal value, i.e., +14.85 Vdc, to prevent the current switches from saturating. The input logic levels are a function of the +15 Vdc supply. The worst-case low logic level varies with the +15 Vdc supply as follows: maximum logic 0 voltage = 0.75V + ($V^+$ -15V). Likewise the worst-case high logic level also varies with the +15 Vdc supply: minimum logic 1 voltage = 2.55V + ($V^+$ -15V).**

pulse level is at +12 V D4 reverse biases and Q4's base to emitter junction becomes forward biased; therefore, Q4 turns on. The 100 ns pulse source, together with D4 and Q4, forms a switchable current source. This switchable current source drives C32. Each pulse of current linearly charges C32 a voltage increment that is: $V = (I_{source}) \times (T_{pulse})/C$, or approximately 5 mV. The continuously incremental charging of C32 is the source of an "X" vector deflection.

C32 is discharged by three parallel FETs, Q7, Q8, and Q9. E42 drives the base of Q5. Q5's emitter is biased by the voltage divider of R24 and R23. When VC1 UNLATCH H is not asserted, the output of E42 is high. This causes the base-emitter junction of Q5 to be reverse biased, and Q5 is cut off. With Q5 not conducting, Q6 will have -15 V at its base, and will also be cut off. Diode D5 will be reverse biased, bringing the gates of the FETs to the same voltage as their sources. This will allow the FETs to conduct, thereby discharging C32. When VC1 UNLATCH H is asserted, it causes Q5 to conduct. This turns on Q6 and brings its collector voltage to -15 V. This forward biases D5, and -15 V is applied to the gates of the FETS. Since the sources are at ground potential, the FETs will be pinched off, allowing C32 to charge.

C32, which is the X vector deflection source, is buffered by a voltage follower, E12. R135 provides for offset trim of E12, allowing the output voltage of E12 to be set to zero when the input voltage is zero. The amplifier E10, following the buffered X vector deflection source, provides for a means to alter the polarity of the X vector deflection. FET switches Q12 and Q15 operate in a series shunt fashion to provide a gain from E10 of either +1 or -1. Drive for the anode of D26 and D6 is provided by circuits that are identical to the drive circuit for the D5 anode. When D26's drive forward biases it, D6's drive holds it reverse biased. With D26 forward biased, Q12's gate is at -15 V while its source is at the same potential as the X vector deflection (A 0 to +5 V signal) causing Q12 to be pinched off. When D26 is forward biased, D6 is reversed biased and R35 pulls the gate of Q15 to the same potential as Q15's source (ground), turning Q15 on. When Q15 is on and Q12 is off, the noninverting terminal of E10 is at ground, and the X vector deflection signal is applied to E10's inverting terminal via R33 with R36 providing feedback from the output of E10, which operates in the inverting mode with a gain magnitude of R36/R33 or approximately one. When D26's drive reverse biases it, D6's drive holds it forward biased. With D6 forward biased, Q15's gate is at -15 V while its source is at ground, pinching Q15 off. When D6 is forward biased D26 is reversed biased and R32 pulls the gate of Q12 to the same potential as its source, turning Q12 on. When Q12 is on and Q15 is off, the X vector deflection is applied to both the noninverting terminal via Q12 and the inverting terminal via R33. R36 provides feedback from the output of E10, which operates in the noninverting mode with a gain magnitude of one. The output of E10, VG VECTOR X, is the horizontal (X) vector deflection signal.

**2.2.13.5 X and Y Summing Amplifiers and Output Drivers** – These circuits allow several distinct analog signals to be "added" to produce a single analog deflection voltage for controlling the electron beam in the VR14/VR17 CRT. The X and Y circuits are nearly identical. The Y summer receives one extra input, CCL2 DESCEND (0) H, which is used to offset several lower case characters (Paragraph 2.2.12.8). Otherwise, they operate in the same manner; only the X circuit will be described.

The typical summing amplifier configuration, shown in Figure 2-46, is a current summing amplifier that is used in applications where several current sources are monitored to yield an output voltage that is proportional to the sum of the inputs. Only three inputs are shown in Figure 2-46 but, theoretically, an infinite number of inputs could be summed. (Thus in the case of the VT11, the X summer has 3 inputs and the Y summer has 4 inputs.)

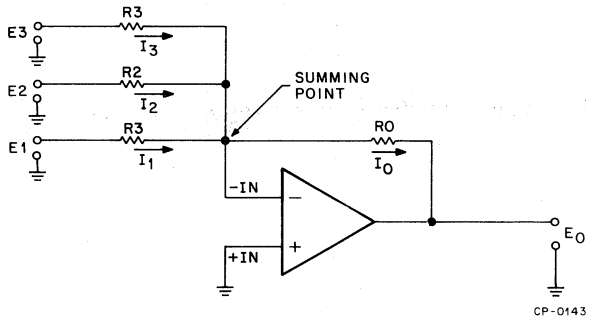



Figure 2-46 Summing Amplifier Configuration

If all of the input resistors are of equal value, the circuit functions as a scaling ladder; by selecting various resistance values, the circuit can provide an output that is a weighted average of the inputs. (A description of how the current summing amplifier is used in digital-to-analog applications is provided in Paragraph 2.2.12.3.)

Since the +IN is at ground, the -IN input to the op amp is also virtually at ground. The current drawn by the input is negligible; thus, the total amount of current flowing through R1, R2, and R3 also flows through R0, and the output voltage is:

$$EO = IO \times R0$$

Assume that resistors R0, R1, R2, and R3 all have a 1K value. Also, assume that E1, E2, and E3 are +2 V inputs; I1, I2, and I3 each have a value of 2 mA, and IO has a value of 6 mA (total). With these defined values, a -6 V output will be present at EO (the sum of E1, E2, and E3).

To illustrate how the inputs can be weighted, assume that the resistance values are: R1 = 1K, R2 = 2K, R3 = 3K, R0 = 1K. Apply +2 V at E1, E2, and E3. The result will be: I1 = 2 mA, I2 = 1 mA, and I3 = 0.67 mA. Therefore, IO = 3.67 mA and EO = 3.67 V.

The X Deflection Summing Amplifier receives inputs from the X DAC, X vector and character deflection circuits, and an attenuated version of Y character deflection signal. These inputs are summed at the inverting input of the summer, E4 (drawing A320-CSG). The summers output is buffered by an output driver E3 with feedback provided (R47) to the summers inverting input. The summers noninverting input is returned to ground via jumper W3. E4 and E3 function as an inverting mode summing amplifier and driver. The gain assigned to each summer input is determined by the ratio of the feedback resistor to the input resistor as previously described. Table 2-14 lists the components and gain for each input.

**Table 2-14**
**X Deflection Gain**

| Summer Input | Input Resistor | Gain |
|---|---|---|
| X DAC | R38 = 422Ω | $\frac{R47}{R38} \approx 5$ |
| X Vector Deflection | R37 = 2 kΩ | $\frac{R47}{R37} = 1$ |
| X Character Deflection | R39 = 2 kΩ | $\frac{R47}{R39} = 1$ |

Note: Feedback resistor (R47) = 2 kΩ.

# CHAPTER 3
# MAINTENANCE

Corrective maintenance procedures that apply to the VT11 Graphic Display Processor are discussed in this chapter. The most important point in maintenance philosophy is that the user understand the normal operation of the VT11 as described in Chapter 2. A thorough comprehension of this information, plus the maintenance procedures included in this chapter, are the best tools the user has to isolate and correct malfunctions.

## 3.1 VT11 DISPLAY PROCESSOR ADJUSTMENTS

### 3.1.1 Character Display Adjustments

Two adjustments are provided in the character generator. The first is R9, a 10-turn potentiometer in the E slot of the M7013 module (drawing D-CS-M7013-0-1, sheet 2). It is used to adjust the delay from the time the analog Y ramp and X step circuits are started until the actual intensity pulse is generated. Optimum linearity of character rows and columns is obtained with a properly adjusted R9.

The second character display adjustment is the Y ramp character adjust potentiometer, R134, on the A320 module (Figure 3-1). This control ensures that the positive and negative Y ramps will have the same slope (Figure 3-2).

An adjustment procedure for these controls is provided in the following paragraphs. Although the two adjustments do not actually interact, they appear to do so on the CRT screen.

1. Display a Rubout character (ASCII code $177_8$, Figure 3-3) either by running Instruction Test No. 2, MAINDEC-11-DDGTB (Paragraph 3.2.2) or by loading the following program into the PDP-11.

| LOC | Contents | Remarks |
|---|---|---|
| 1000 | 12737 | MOV |
| | 2000 | Display File Addr to |
| | 172000 | Display Prog. Cntr |
| | 000001 | Wait |
| 2000 | 117600 | Non-Intensified Pt, Level 7 |
| | 01000 | (1000,1000) |
| | 01000 | |
| | 100000 | Character Mode |
| | 177 | Rubout |
| | 160000 | Display JMP |
| | 2000 | |

2. Place 1000 in the Switch Register (SR); press LOAD ADRS (Load Address) and START.

3. Adjust R9 on the M7013 module until the top dots in each of the five columns line up horizontally.

4. Adjust R134 on the A320 module until the bottom dots in each of the five columns line up horizontally.

5. Repeat steps 3 and 4 until both the top and bottom dots of the character are lined up satisfactorily.

6. Examples of correct and incorrect Rubout display are shown in Figure 3-4. Additional information can be found in Paragraph 3.2.3.

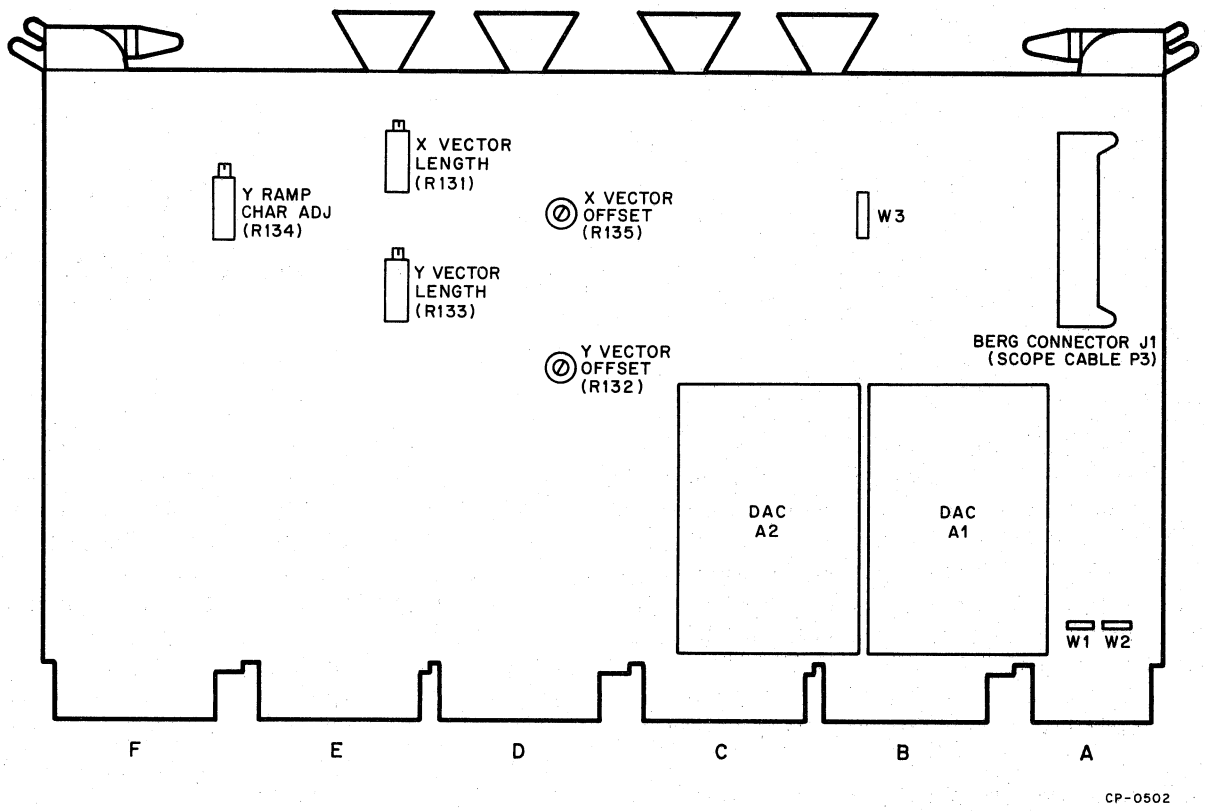



Figure 3-1 Adjustment Locations, A320 Module

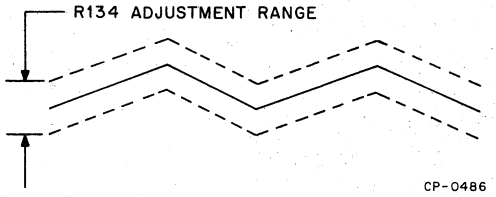



Figure 3-2 Y Character Ramp

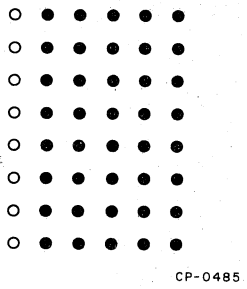
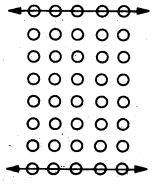
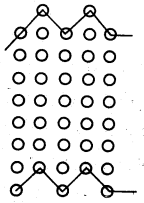



Figure 3-3 Rubout Display Pattern

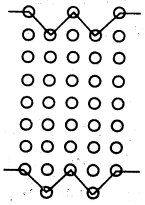


Correct alignment of character dots.



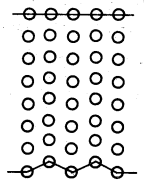
(P) Intensity delay is too long.

(S) Decrease the period of the delay single shot until dots align. Adjust R9 (M7013 module).



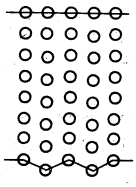
(P) Intensity delay is too short.

(S) Increase the period of the delay single shot until dots align. Adjust R9 (M7013 module).



(P) Positive ramp slope is less than negative slope.

(S) Decrease slope of negative ramp using adjustment provided. Adjust R134 (A320 module).



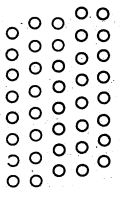
(P) Positive ramp slope is greater than negative slope (see Note).

(S) Increase slope of negative ramp using adjustment provided. Adjust R134 (A320 module).

**NOTE**

Should the difference between the slope of the positive and negative ramp generators become more extreme than shown, the character may appear to walk up as shown below.

Key: (P) = Problem; (S) = Solution



Character Walks Up

CP-0754

Figure 3-4 Incorrect Character Display

### 3.1.2 Vector Display Adjustments

There are four adjustments in the vector generator on the A320 module (Figure 3-1). Two are for corrections in the X axis and two are used to correct Y axis problems. In each axis a 10-turn potentiometer adjusts the vector length and a 1-turn potentiometer adjusts the offset value of the analog switch. An adjustment procedure for both vector axes follows.

1. Load and start the Visual Display Test, MAINDEC-11-DDGTC (Paragraph 3.2.3). Display the Horizontal Vector Length Pattern (Figure 3-14).

2. Adjust R131 until the ends of the vectors meet the vertical line.

3. Display the Vertical Vector Length Pattern (Figure 3-15). Adjust R133 until the ends of the vectors meet the horizontal line.

4. Display the Squares Pattern (Figure 3-12). Adjust R135 until the vectors in the upper right quadrant meet.

5. Adjust R132 until the vectors in the upper left quadrant meet.

6. Display the Octagons Pattern (Figure 3-11) and check for symmetry.

7. Additional information can be found in Paragraph 3.2.3.

## 3.2 DIAGNOSTIC MAINTENANCE PROGRAMS

The purpose of diagnostic software is to exercise the VT11 components, to provide the operator with a visual indication of system capability, to help isolate malfunctions, and to aid in adjusting the CRT and display processor. The available software is divided into several functional tests, some operating automatically, once started, while others require operator intervention during the program run.

The applicable programs (Table 3-1) should be run periodically. General operating instructions are contained in the following paragraphs; however, they may not reflect current procedures due to program operational changes. Therefore, it is recommended that the more complete instructions contained in the program write-ups be referred to if difficulty is encountered, or if more detailed information is desired when running the programs.

**Table 3-1**
**VT11 Diagnostic Programs**

| Program | Description |
|---|---|
| GT40/GT44 Instruction Test 1 (MAINDEC-11-DDGTA) | Using the two maintenance switches on the M7013 module, this logic test evaluates all functional registers and interrupt vectors. Consisting of two parts, it performs both basic and complex logic tests in an automatic single-step mode. |
| GT40/GT44 Instruction Test 2 (MAINDEC-11-DDGTB) | Similar to Instruction Test 1, this examines more closely the registers and interrupt logic; the maintenance switches are not used. It also displays several patterns on the CRT. |
| GT40/GT44 Visual Display Test with VR14 Display (MAINDEC-11-DDGTC) | This test causes a series of patterns to be displayed on a VR14 that can be used when aligning and adjusting the display. It should *not* be used to make adjustments in conjunction with a VR17 CRT. |
| GT40/GT44 Visual Display Test with VR17 Display (MAINDEC-11-DDGTG) | This test causes a series of patterns to be displayed on a VR17 CRT that can be used when adjusting the display. It should *not* be used to make adjustments in conjunction with a VR14 CRT. |

### 3.2.1 Instruction Test 1 (MAINDEC-11-DDGTA)

This test is a preliminary test of the display processor. Instruction Test 1 makes extensive use of the display stop and display resume features of the VT11. The program is automatically executed in the single-step mode. A check is made of all functional registers and interrupt vectors in the alphagraphic display control.

In this test, the maintenance switches on the M7013 module are used; satisfactory single-step execution of this diagnostic requires that they be correctly positioned. Figure 3-5 shows their location on the M7013 module. The OFF position of the switches is toward the "top" of the module. Note that a white dot is visible when a switch is in the OFF position.

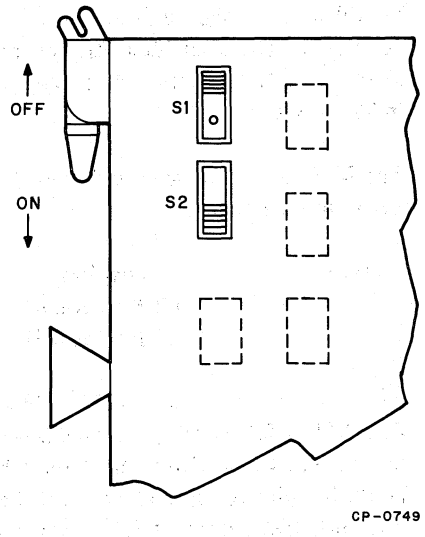



Figure 3-5 Maintenance Switches, M7013 Module

In running Instruction Test 1, the following procedure should be adhered to:

1. Set the M7013 module maintenance switches as follows:

| Switch | Position |
|---|---|
| 1 | ON (Maintenance) |
| 2 | OFF (Normal) |

2. Load Instruction Test 1 into the PDP-11.

3. With the HALT/ENABLE switch in the HALT position, place $174_8$ in the SR. This selects the Basic Logic Test [Bus Request (BR) only].

4. Press LOAD ADRS, set the HALT/ENABLE switch to ENABLE, and press START. Termination of an error free pass will be indicated by a tone signal from the Teletype® or LA30 DECwriter; press HALT and perform step 6.

5. In the event of an error, the program halts with PC+2 (or PC if the central processor is a PDP-11/15 or 20) of the failing routine displayed in the address lights.

   - If the operator desires to continue the test, in order to see what type of errors the display processor makes, press CONT. This approach may help isolate the display processor malfunction.

   - If the operator desires the program to restart and loop on the previously failed test, place SR switch bit 14 to a 1 and press CONT. The program will loop and then halt at the same location. This indicates that the program can successfully loop in the failing routine. At this time insert a NOP ($240_8$) in the ERROR HALT (000000) location and press CONT. The program will now loop in the failing test until HALT is pressed. An oscilloscope may be used to examine VT11 internal signals while the CPU is in the loop.

6. Set the M7013 module maintenance switches as follows:

| Switch | Position |
|---|---|
| 1 | OFF (Normal) |
| 2 | ON (Maintenance) |

7. Place $200_8$ in the SR to select the Complex Logic Test (BR, NPR, Interrupt).

8. Press LOAD ADRS, set the HALT/ENABLE switch to ENABLE, and press START. Completion of an error free pass is indicated by a tone signal from the Teletype or LA30 DECwriter; press HALT and then position both M7013 module maintenance switches in the OFF position.

9. Refer to step 5 if any errors are encountered.

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### 3.2.2 Instruction Test 2 (MAINDEC-11-DDGTB)

This test is an extention of Instruction Test 1. A complex test, it provides a more detailed examination of the VT11 registers and interrupt operations. Correct positioning of the maintenance switches should be observed. The operating procedure is as follows:

1. Ensure that the M7013 module maintenance switches (Paragraph 3.2.1) are set as follows:

| Switch | Position |
|---|---|
| 1 | OFF (Normal) |
| 2 | OFF (Normal) |

2. Load Instruction Test 2 into the PDP-11.

3. With the HALT/ENABLE switch in the HALT position, place $200_8$ in the SR to select the complex Logic Test (BR, NPR, Interrupt).

4. Press LOAD ADRS, set the HALT/ENABLE switch to ENABLE, and press START. Termination of an error free pass is indicated by a tone signal from the Teletype or LA30 DECwriter; press HALT switch and perform step 6.

5. In the event of an error, the program halts with PC+2 (or PC if the central processor is a PDP-11/15 or 20) of the failing routine displayed in the address lights.

   - If the operator desires to continue the test, in order to see what type of errors the display processor makes, press CONT. This approach may help isolate the display processor malfunction.
   - If the operator desires the program to restart and loop on the previously failed test, place SR switch bit 14 to a 1 and press CONT. The program will loop and then halt at the same location. This indicates that the program can successfully loop in the failing routine. At this time insert a NOP ($240_8$) in the ERROR HALT (000000) location and press CONT. The program will now loop in the failing test until HALT is pressed. An oscilloscope may be used to examine VT11 internal signals while the CPU is in the loop.

6. Place $204_8$ in the SR and press LOAD ADRS to select the Basic Visual Display Patterns Test. This is a check of the VT11 analog circuits that provides a visual indication of equipment condition. The individual display patterns are selected by SR switches 00 through 02 as listed in Table 3-2.

7. The M7013 maintenance switches should be in the following positions:

| Switch | Position |
|---|---|
| 1 | OFF (Normal) |
| 2 | OFF (Normal) |

8. Ensure that the CRT ON/OFF – BRIGHTNESS switch is rotated 3/4 of the way in the clockwise direction. The VR14/VR17 POWER indicator should be lit. If the indicator does not light, check CRT power connections and the LINE fuse at the rear of the CRT. If the fuse is blown, refer to the *VR14 and VR17 CRT Display User's Manual* (DEC-12-HVCRT-D-D).

**Table 3-2**
**Instruction Test 2 Display Patterns**

| Pattern | SR Switches | | | Display |
|---|---|---|---|---|
| | 02 | 01 | 00 | |
| 0 | 0 | 0 | 0 | Positive Horizontal Line From Screen Center |
| 1 | 0 | 0 | 1 | Negative Horizontal Line From Screen Center |
| 2 | 0 | 1 | 0 | Positive Vertical Line From Screen Center |
| 3 | 0 | 1 | 1 | Negative Vertical Line From Screen Center |
| 4 | 1 | 0 | 0 | Rectangle |
| 5 | 1 | 0 | 1 | Octagon Pattern in Relative Point & Short Vector |
| 6 | 1 | 1 | 0 | Character Set |
| 7 | 1 | 1 | 1 | Light Pen Test |

9. Set SR switches (00–02) to display pattern 0, set the HALT/ENABLE switch to ENABLE, and press START. Proceed to step 10 if the display appears as shown in Figure 3-6.

10. Set SR switches (00–02) to display patterns 1 through 7. Display pattern 7, the Light Pen Test, is shown in Figure 3-7.

11. If any of the patterns do not display, refer to VT11 Troubleshooting Procedures, Paragraph 3.3. If the patterns displayed indicate that there is a need for display adjustments, perform the adjustments when running the Visual Display Test (Paragraph 3.2.3).

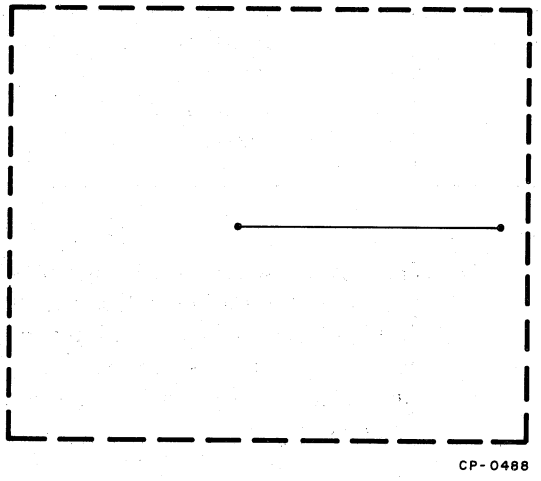



Figure 3-6 Display Pattern 0

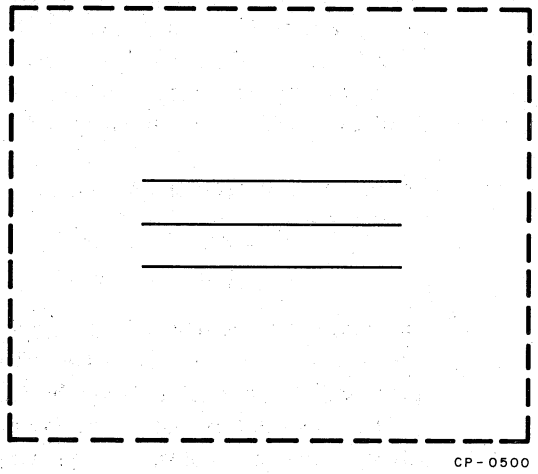



Figure 3-7 Display Pattern 7

12. With pattern 7 displayed on the CRT screen, turn up the front panel BRIGHTNESS control a moderate amount and point the 375 Light Pen at each vector in succession. Light pen hits should be obtained only from the top two vectors; any additional hits are the result of a failure condition. A light pen hit is indicated by the words LIGHT PEN HIT appearing above the three vectors. Press HALT to stop the program. If a failure in the light pen circuitry is indicated, refer to the troubleshooting procedures in Paragraph 3.3.3.

### 3.2.3 Visual Display Test

This test provides the user with a visual indication of VT11/CRT functions, and is used in adjusting the VT11 and CRT.

**NOTE**

**The Visual Display Test comes in two versions; one to be run using a VR14 Display Monitor (MAINDEC-11-DDGTC); the other for use with a VR17 Display Monitor (MAINDEC-11-DDGTG). Be sure to use the proper diagnostic when making adjustments.**

1. Load the VT11 Visual Display Test.

2. With the HALT/ENABLE switch in the HALT position, set the SR to $200_8$.

3. Press LOAD ADRS.

The Visual Display Test diagnostic allows for 3 modes of display control; with SR switch bits 7 = 0 and 8 = 0, the diagnostic assumes control and will step through all the display patterns, except Light Pen Follow and Keyboard Echo, automatically. Each pattern will be displayed approximately 10 seconds. With SR switch bits 7 = 0 and 8 = 1, display patterns may be selected by SR switch bits 00 through 03. With SR switch bits 7 = 1 and 8 = 0 or 1, display patterns are selected by the keyboard. Table 3-3 lists the display patterns and the corresponding keyboard keys and SR switches necessary to call them in.

4. Put the HALT/ENABLE switch in the ENABLE position and press START. The program will commence running. Since the address $200_8$ is still in the SR switches (bit 7 = 1, 8 = 0), the Teletype or DECwriter keyboard can now be used to select the individual tests that make up the Visual Display Test. Each test displays a distinct pattern on the CRT.

Table 3-3
Visual Display Test

| Test | Keyboard Control (Press Character) | SR Control (Set SR Switches to Equal) |
|---|---|---|
| Directory | A | $000400_8$ |
| Repeatability | B | $000401_8$ |
| Box with X (Pincushion) | C | $000402_8$ |
| Octagons or Squares | D | $000403_8$ |
| Character Set | E | $000404_8$ |
| Dash Lines and Blink | F | $000405_8$ |
| Horizontal Vector Length | G | $000406_8$ |
| Vertical Vector Length | H | $000407_8$ |
| Horizontal Phosphor | I | $000410_8$ |
| Vertical Phosphor | J | $000411_8$ |
| Intensity Levels | K | $000412_8$ |
| Edge Test | L | $000413_8$ |
| Short Vector and Relative Point | M | $000414_8$ |
| Graphplot Increment | N | $000415_8$ |
| Light Pen Follow | O | $000416_8$ |
| Keyboard Echo | P | $000417_8$ |

5. Under keyboard control, pressing RUBOUT after selecting a test will lock-on the display pattern; pressing CR after selecting a test will select a subpicture or stop the display motion. Under SR control the display patterns lock-on automatically. (There is a short delay, however, before the selected pattern appears on the CRT screen.) Setting SR switch bit 6 = 1 will select a subpicture or stop display motion.

   a. Subpictures can be displayed in the following tests:

      - Octagons or Squares
      - Intensity Levels (SYNC)
      - Graphplot Increment
      - Light Pen Follow

   b. Stop display motion is applicable to the following tests:

      - Horizontal Vector Length
      - Vertical Vector Length
      - Horizontal Phosphor
      - Vertical Phosphor

6. Press A on the keyboard to select the Directory display and RUBOUT to lock-on the display. Examine the characters for column and row continuity.

7. Press B to select the Repeatability display pattern and RUBOUT to lock it in. Check the display (Figure 3-8) for spot jitter and spot size using a spot microscope (type 29-20273 or equivalent). Jitter should be $<\pm$½ spot diameter.

8. Press C to select the Box with X (Pincushion), display pattern (Figure 3-9). Press RUBOUT to lock it in. Using a spot microscope, check the display for line closure [overshoot/undershoot <0.06 in. (0.1524 cm)] and vector noise [<0.01 in. (0.0254 cm)]. The vectors should appear as single lines; multiple vectors (Figure 3-10) are considered a faulty display.

   Check the vectors for straightness and curvature at the beginning and end.

9. The box should extend to the corners of the screen. On a VR14 the box should be rectangular, while on a VR17 it should be a square. If the box does not extend to the corners of the screen, check and adjust the following in the VT11 and VR14/VR17: (For CRT adjustments refer to the *VR14 and VR17 CRT Display User's Manual*).

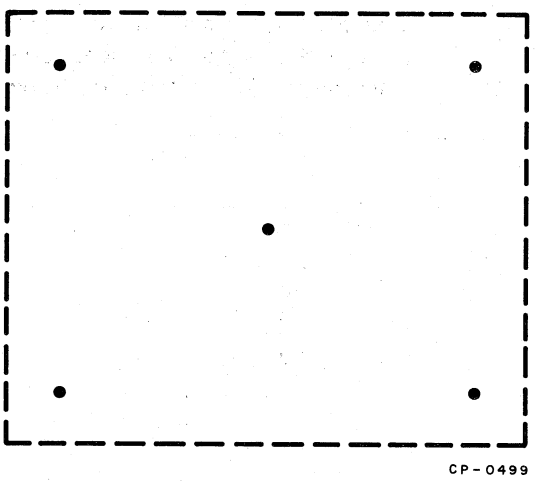



Figure 3-8 Repeatability Display Pattern

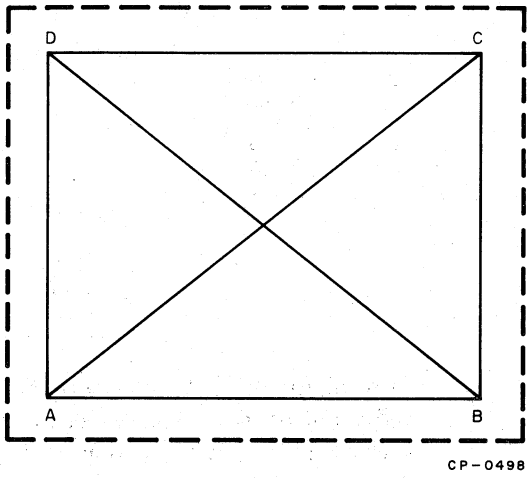



Figure 3-9 Box with X Display Pattern

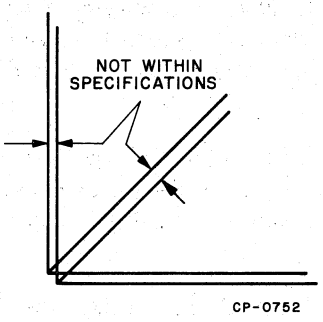



Figure 3-10 Faulty Box with X Display

a. The yoke must be positioned as far forward as possible on the neck of the CRT. If it is not, the electron beam is not correctly deflected and incomplete patterns exhibiting a shadow effect are displayed.

b. Adjust X and Y gain potentiometers on the A225 Deflection modules in the VR14/VR17 to extend the box to the corners of the screen.

c. Adjust the X and Y position potentiometers on the A225 Deflection modules in the VR14/VR17 to center the box on the screen.

d. Adjust the X (R131) and Y (R133) vector length potentiometers on the A320 module (Figure 3-1) if the vectors are too long or too short. Adjustments should be made according to the procedure in Paragraph 3.1.2 to meet VT11 specifications.

e. If multiple vectors (Figure 3-10) are present, the X (R135) and Y (R132) vector offset potentiometers on the A320 module also require adjusting. These controls compensate for unwanted voltage across the deflection yokes so that when voltage is removed from the yokes they are not slightly above or below 0 V.

10. Alternately display Box with X and Repeatability to provide an evaluation of vector position, length, and crossover.

11. Press D to select the Octagons test and RUBOUT to lock on the display (Figure 3-11). All vectors are drawn counterclockwise; this should be kept in mind when making adjustments.

12. Check the display using the criteria described in step 8 for the Box with X test.

13. The Squares test (Figure 3-12) can be selected by pressing CR. Evaluate the display, particularly the center squares, for optimum vector quality and note any deviation from the specifications described in step 8.

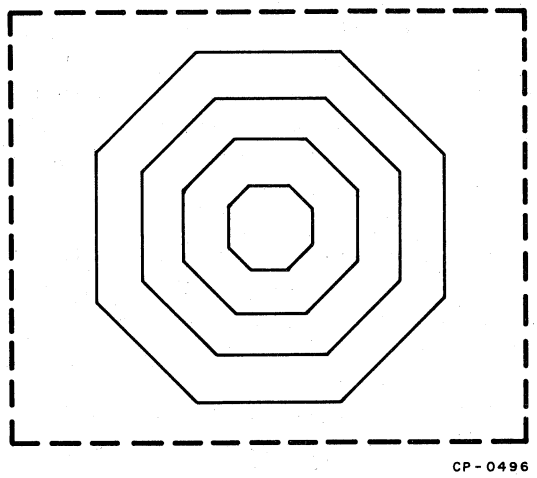



Figure 3-11 Octagons Display Pattern

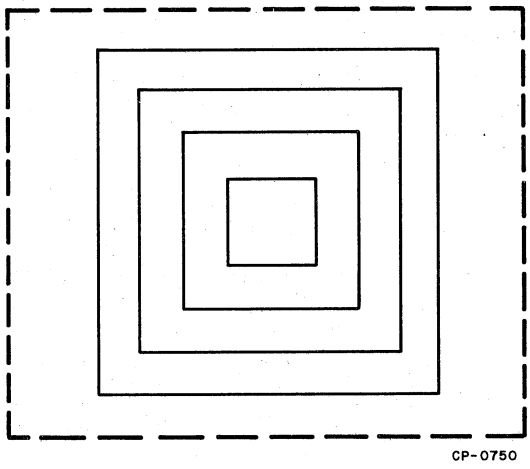
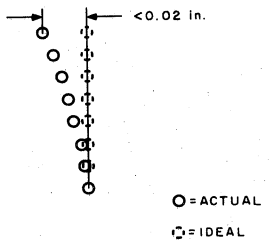



Figure 3-12 Squares Display Pattern

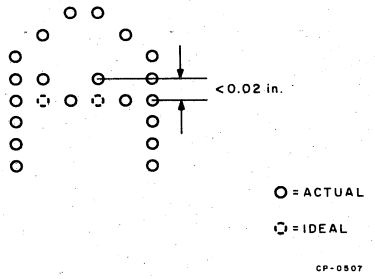
14. Press E to select the Character Set display; press RUBOUT to lock on the display. The character set is divided into four sets of 4 lines each. Characters are displayed normally on the left side of the screen, while on the right side they are italicized.

    Check the column and row lineup of all characters

    Rubout (Figure 3-3) is considered to be the worst case character because all dots in columns 2 through 6 are intensified. To meet VT11 specifications the centers of all dots in any one column in a character should be less than 0.02 in. (0.0508 cm) from a line running through the center of an ideal display of the same column. This is illustrated below.




    The requirement for a row within a character is similar:




    Two adjustments, R9 on the M7013 module and R134 on the A320 module, control character display. Their function is described in Paragraph 3.1.1.

15. Press F to display the Dash Lines test and RUBOUT to lock on the display. The VT11 is capable of displaying four line types: solid, long dash, short dash, and dot dash. All are displayed in this test (Figure 3-13).

16. Two sets of the four line types are shown on the screen. The right-hand set flashes on and off as a test of the BLINK function.

17. Press G to display the Horizontal Vector Length test pattern (Figure 3-14); RUBOUT locks on the display. This test draws vectors from the lower corner to the right side of the screen. Vector angles vary from 0 to 45°.

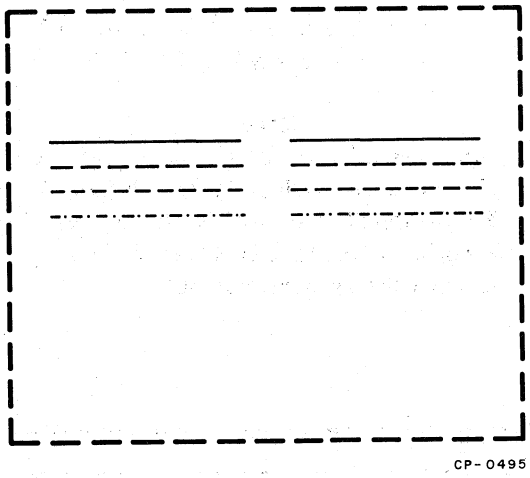



Figure 3-13 Dash Lines and Blink Display Pattern

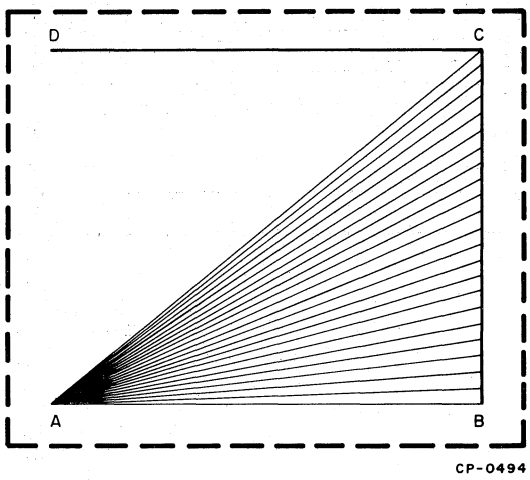



Figure 3-14 Horizontal Vector Length Display Pattern

18. A vertical vector is drawn from point B to point C to assist in the adjustment of the X vector length; a negative horizontal vector is displayed from point C to point D as an aid in adjusting X offset.

19. The following items should be checked:

    a. The distance between vectors should be equal.

    b. The horizontal vectors should not overshoot or undershoot the vertical vector more than 0.06 in. (0.1524 cm).

    c. Display motion can be halted by pressing CR.

20. Press H to select the Vertical Vector Length test; press RUBOUT to lock on the display. This test, shown in Figure 3-15, draws vectors from the lower left corner to the top of the screen. Vector angles vary from 90 to 45°. The horizontal vector (C to D) is used to assist in the adjustment of the Y vector length; the vertical vector from C to B aids in adjusting the Y offset control.

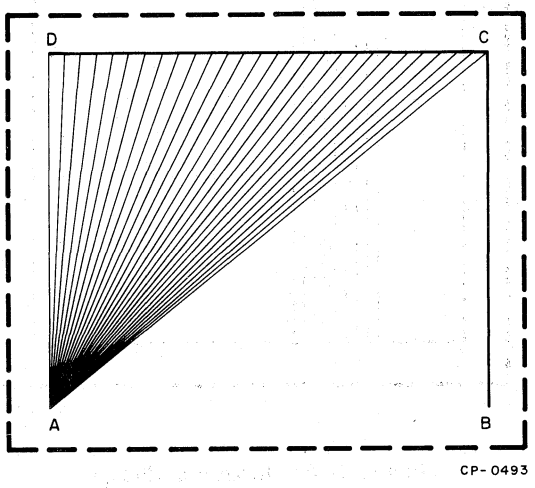



Figure 3-15 Vertical Vector Length Display Pattern

21. Refer to step 19 for observations required to ensure proper vector adjustments.

22. Press I to display the Horizontal Phosphor test and RUBOUT to lock on the display. This test draws a group of vertical vectors (Figure 3-16) and moves them horizontally across the screen. Vector motion can be stopped by pressing CR.

23. Inspect the display for the following discrepancies:

    a. Burn spots, glass defects, etc. Note and report any deficiencies.

    b. Digital to Analog Converter (DAC) (A6000) crossover distortion. This distortion is evident at the horizontal and

vertical centers of the screen as a variation in intensity. The unit should be rejected if the intensity increases by a factor of two or more at any point on the screen where the intensity should be constant. Since the DACs are bipolar, ranging from -0.5 to +0.5 V, nonlinearity may exist at the 0 V crossover. This shows as a slight variation in image brightness at this point.

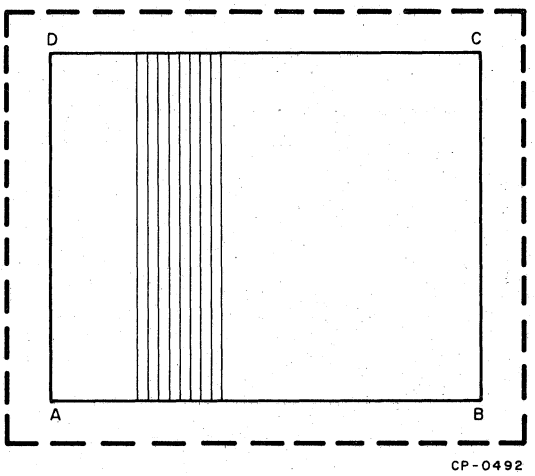



Figure 3-16 Horizontal Phosphor Display Pattern

24. Press J to display the Vertical Phosphor test. Press RUBOUT to lock on the display. This test draws a group of horizontal vectors and moves them vertically up the screen (Figure 3-17). Refer to step 23 for required observations.

25. The Intensity Levels test is initiated by pressing K. Pressing RUBOUT locks on the display. Characters, vectors, and relative points are drawn by this test; intensity 0 should be adjusted so that it is barely visible (Figure 3-18).

26. Check the following light pen characteristics:

    a. A vector light pen hit should be obtained at intensity levels 4 through 7.

    b. A character light pen hit should be obtained at intensity levels 6 and 7.

    c. A point light pen hit should be obtained at intensity level 7.

**NOTE**

**Light pen hits are obtainable on all vectors, characters and points in this display, if the BRIGHTNESS control is turned up high enough. Do not turn brightness up too high, as this may damage screen phosphors.**

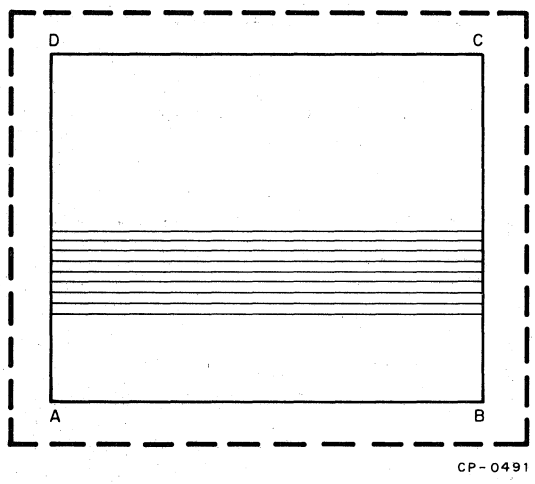



Figure 3-17 Vertical Phosphor Display Pattern

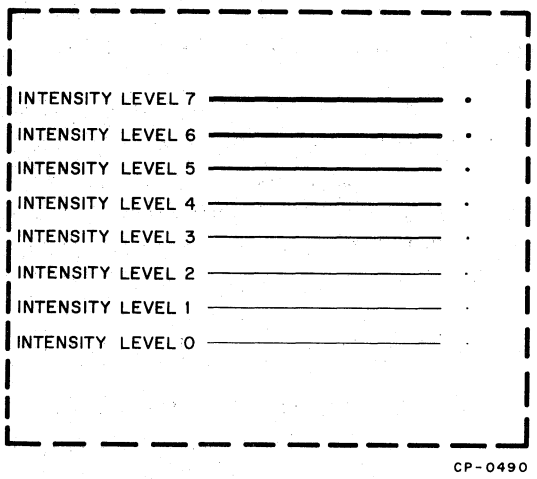



Figure 3-18 Intensity Level Display Pattern

27. Check "sync" by pressing CR. The entire display should become dimmer because a display instruction, following a Status A instruction in the display file, is being synchronized with the line frequency.

28. Press L to select the display pattern for the Edge test. RUBOUT will lock on the display. In this test a rectangle is drawn around the screen edges. Smaller rectangles are then superimposed symmetrically on each leg of the larger rectangle as shown in Figure 3-19.

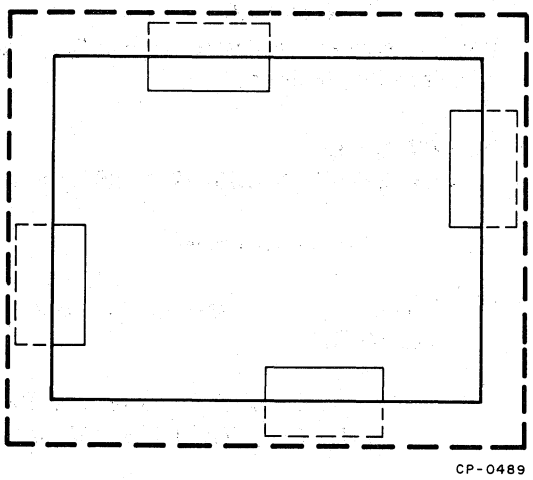



Figure 3-19 Edge Display Pattern

29. Those portions of the four smaller rectangles that are outside the larger rectangle should be blanked.

30. Press M to select the Short Vector and Relative Point test. RUBOUT will lock on the display (Figure 3-20).

    Make the following observations:

    a. In each octagon group, the middle octagon, formed by the relative points, is mid-way between the inner and outer octagons.

    b. The vertical vectors are distinct.

    c. Only one horizontal line (actually a series of relative points) is displayed.

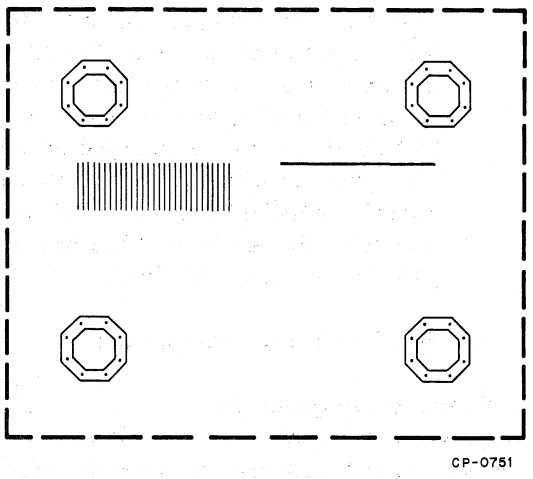



Figure 3-20 Short Vector and Relative Point Display Pattern

31. Press N to select the Graphplot Increment test and RUBOUT to lock on the display. A series of points are plotted at each possible value in the Graphplot Increment Register from 0 through $77_8$. The resulting display should appear as a series of points at an increasing angle.

32. Press O to select the Light Pen Follow test and RUBOUT to lock on the display. A "bug", consisting of a cross inside a diamond is displayed in this test. When a light pen hit is sensed on any portion of the cross or diamond, the configuration will move until its common center is positioned at the point of the light pen hit. The current location of the "bug", in raster units, is displayed in octal on the upper-left portion of the screen.

33. Check the following test functions:

    a. Light pen hits should be generated without respect to where on the cross or diamond the light pen is aimed.

    b. The center of the "bug" should move in the direction of the light pen hit.

34. Move the "bug" around the edges of the screen to determine that correct edge blanking takes place.

35. Press P to select the Keyboard Echo test. Keys pressed on the keyboard result in the display of their respective characters on the CRT screen. Determine that all characters in Appendix A, including the 31 special characters (except for CONTROL C), can be displayed on the CRT. The octal representation for each character printed is displayed near the top of the screen. Exit from the Keyboard Echo test is accomplished by pressing CONTROL C.

36. Press HALT to stop the program.

### 3.2.4 Operational Programming

Although VT11 programming is not within the scope of this manual, several examples are presented (Tables 3-4, 3-5, 3-6, 3-7) to introduce the user to software control of the VT11. They are limited in the results obtained and are not meant to illustrate full VT11 capability.

**3.2.4.1 Display Large Rectangle** – A program that will draw a large size rectangle is presented in Table 3-4. This program is also used as the basis for the program extensions described in Paragraphs 3.2.4.3 through 3.2.4.4. Load the program and place 1000 in the SR; press LOAD ADRS and START. Press HALT if the display is satisfactory and proceed to Paragraph 3.2.4.2.

**3.2.4.2 Display Large Rectangle with Vector** – This is a modification of the display generated by the program in Table 3-4. A blinking dot-dash vector is drawn diagonally from the lower left corner of the rectangle to the upper right corner. With the basic program still in memory, load the additional steps (Table 3-5), place 1000 in the SR, and press LOAD ADRS and START. Note that the display jump in the previous program was deleted; however, the program still concludes with a jump instruction. Press HALT if the display is satisfactory and proceed to Paragraph 3.2.4.3.

**3.2.4.3 Display Large Rectangle with Vector and Graphic Data** – The program currently in memory is again modified to display several graphic characters. Load the additional steps (Table 3-6) and press LOAD ADRS and START with 1000 in the SR. Press HALT if the display is satisfactory and proceed to Paragraph 3.2.4.4.

**3.2.4.4 Display Large Rectangle with Vector, Graphic, and Graphplot Data** – The final modification to the program started in 3.2.4.1 causes graphplot data to be displayed in addition to the previously programmed data. Load the additional steps (Table 3-7) and press LOAD ADRS, and START with 1000 in the SR. Press HALT if the display is satisfactory.

## 3.3 VT11 TROUBLESHOOTING PROCEDURES

This section provides procedures to help isolate and correct malfunctions in the VT11 Display Processor. In order to troubleshoot the VT11, the user should understand the normal operation of the display processor as described in Chapter 2.

The following test equipment is required:

- Type 453 Tektronix oscilloscope or equivalent
- Triplett Multimeter, DEC part no. 29-13510 or equivalent
- Module Extender boards (3). Type W900.

**CAUTION**

**Do not remove or insert cables, fuses, or modules with power on.**

### 3.3.1 No CRT Picture

1. Check ON/OFF–BRIGHTNESS control.
   a. Turn up brightness.
2. Check the 3 fuses at the rear of the VR14/VR17.
   a. Replace if faulty, and refer to *VR14 and VR17 CRT Display User's Manual.*
3. Check scope cable.
   a. Ensure that it is properly seated at the VR14/VR17 and at the A320 module.
4. Check maintenance switches (Paragraph 3.2.1) on the M7013 module.
   a. Ensure that they are both OFF.
5. Check VT11 module seatings and Unibus connections to the VT11 backplane.
   a. Ensure that they are proper.
6. Run Instruction Test 1 diagnostic program (Paragraph 3.2.1).
   a. Isolate DPU fault and repair.
7. Run Instruction Test 2 diagnostic – subtest 1 (Paragraph 3.2.2).
   a. Isolate DPU fault and repair.

**Table 3-4**
**Large Rectangle Program**

| Address | Instruction/Data | Mnemonic | Comments |
|---|---|---|---|
| 1000 | 12737 | | Move starting address of display file to Display Program Counter (DPC). |
| 1002 | 2000 | MOV#2000,@#172000 | |
| 1004 | 172000 | | |
| 1006 | 000001 | WAIT | Wait for interrupt (used here to keep CPU running) |
| 2000 | 117224 | | Set point mode, no blink, solid line, intensity 5 |
| 2002 | 0 | | Unintensified point at 0,0 X=0 |
| 2004 | 0 | | Y = 0 |
| 2006 | 110000 | | Set long vector |
| 2010 | 041777 | | X = $1777_8$, intensify |
| 2012 | 000000 | | Y = 0 |
| 2014 | 40000 | | X = 0, intensify |
| 2016 | 1377 | | Y = 1377 |
| 2020 | 061777 | | X = -1777, intensify |
| 2022 | 0 | | Y = 0 |
| 2024 | 40000 | | X = 0, intensify |
| 2026 | 21377 | | Y = -1377 |
| 2030 | 160000 | | Display JMP to beginning of display file |
| 2032 | 2000 | | |

**Table 3-5**
**Large Rectangle with Vector Program Modification**

| Address | Instruction Data | Comments |
|---|---|---|
| 2030 | 110037 | Long vector, dot-dash, blink |
| 2032 | 041777 | X = $1777_8$, intensify |
| 2034 | 1377 | Y = 1377 |
| 2036 | 160000 | Display JMP to beginning of display file |
| 2040 | 2000 | |

**Table 3-6**
**Large Rectangle with Vector and Graphic Data**

| Address | Instruction Data | Comments |
|---|---|---|
| 2036 | 114024 | Point mode, no blink |
| 2040 | 1050 | Unintensified point, X = 1050 |
| 2042 | 577 | Y = 577 |
| 2044 | 100000 | Character mode, no blink |
| 2046 | 42506 | E F |
| 2050 | 42105 | D E |
| 2052 | 46440 | M (sp) |
| 2054 | 105 | E |
| 2056 | 160000 | Display JMP to beginning of display file |
| 2060 | 2000 | |

**Table 3-7**
**Large Rectangle with Vector, Graphic, and Graphplot Data**

| Address | Instruction Data | Comments |
|---|---|---|
| 2056 | 114000 | Point mode |
| 2060 | 40000 | X = 0, intensify |
| 2062 | 577 | Y = 577 |
| 2064 | 174150 | Load Status B, increment = 50 |
| 2066 | 124000 | GRAPH Y mode |
| 2070 | 700 | Y data |
| 2072 | 1000 | Y data |
| 2074 | 1100 | Y data |
| 2076 | 1200 | Y data |
| 2100 | 1100 | Y data |
| 2102 | 1000 | Y data |
| 2104 | 700 | Y data |
| 2106 | 600 | Y data |
| 2110 | 160000 | Display JMP to beginning of display file |
| | 2000 | |

8. Run Instruction Test 2 – subtest 2 (Paragraph 3.2.2). Set SR switches to select pattern 0.

   a. Check that the following signals are present at the circuit card connector block of the VR14/VR17 CRT:

      - Z input (GM INTENSITY OUT L, the unblanking signal) at location VR14/VR17 A4J. A low level is needed to unblank the CRT.

      - X input (X deflection) at location VR14/VR17 A2B. A changing voltage (0 V → ≈ −1.75 V) should be ovserved because a horizontal line is being displayed.

      - Y input (Y deflection) at location VR14/VR17 A3B. A nonchanging voltage (≈ −0.56 V) should be observed because a horizontal line is being displayed. If the 3 signals are present the fault is isolated to the VR14/VR17 CRT. Refer to the VR14/VR17 manual previously mentioned.

        If any of the above signals is absent, VT11 failure is indicated. Using the wire run list (Drawing K-WL-VT11-0-1), circuit schematics, extender boards, and the 453 oscilloscope, trace back the signals to isolate the faulty module and replace.

### 3.3.2 Faulty Pictures

1. If *all* displays generated are in poor focus, have half or a quarter of the picture missing, or are affected by picture swim (60 Hz) or oscillations, CRT problems are generally indicated. The following may be the causes:

   Poor Focus:

   Adjustment of focus potentiometer on G836 circuit board in the VR14/VR17.

   Half or Quarter of the Picture Missing:

   One or two of the CRT deflection transistors may be inoperative.

   Swim or Oscillation:

   Improper input signal grounding or a faulty A225 circuit board in the CRT.

   Refer to the VR14/VR17 Manuals.

   Jitter may be due to an intermittent connection or noise. Check modules and scope cable for proper seating. Make sure that the electromagnetic interference shield (DEC no. 17-00021-00) is in position between the A320 and M7014YA modules.

2. If some displays are faulty while others are satisfactory, VT11 failure is indicated. Run the Visual Display Test diagnostic, (Paragraph 3.2.3) and Instruction Test 2 – subtest 2 (Paragraph 3.2.2). Observe the displays to determine the nature of the fault; do the vectors distort or "wrap-around"? Are negative vectors drawn? Are the four line types generated? Is the problem with vectors and relative points or absolute points? Are characters generated? Are italics generated? Does the Graphplot feature operate?

   Once the nature of the problem is determined, select a faulty pattern for display on the CRT, and use the wire-run list, circuit schematics, extender boards, and oscilloscope to check the implicated circuitry (Chapter 2). Isolate the faulty module and replace.

### 3.3.3 Light Pen Malfunction

1. Run Instruction Test 1 and Instruction Test 2 – subtest 1, to determine that the VT11 registers and interrupt logic are operating properly.

2. Ensure that the scope cable connectors are properly seated. and that the light pen is plugged into the VR14/VR17 front panel.

3. Run Instruction Test 2 – subtest 2, selecting display pattern 7 (Figure 3-7).

4. Aim the light pen at the top vector and observe the following:

   a. Does "LIGHT PEN HIT" appear above the top vector?

   b. Does the vector intensity, at the point the light pen is aimed, increase?

5. If neither A or B is true, check for light pen pulses at pin AP2 of the VT11 backplane. The light pen must be aimed at a sufficiently intensified point on the screen or other light source. If no LP pulses are present, check continuity from pin AP2 to the VR14/VR17 side of the scope cable (pin 19 of the scope cable connector plug). With continuity confirmed, no LP pulses indicates 375 Light Pen or G840 Light Pen Amplifier failure. Refer to the light pen engineering drawings listed in Chapter 4. Appendix B contains a description of the G840 Light Pen Amplifier circuit.

6. If LP pulses are present on the A320 module, use the wire-run list and the circuit schematics to trace the pulses down to the failing circuitry. Replace the faulty module. Some possible areas of failure are:

   a. Light pen hit logic (drawing M7014YA-LEI).

   b. Light pen hit intensity logic (drawing M7013-GM).

   c. Load DAC logic (drawing M7014YA-VC1).

   d. Interrupt address logic (drawing M7014YA-BRL).

   e. Signal routing on the backplane and modules.

# CHAPTER 4
# VT11 ENGINEERING DRAWINGS AND RELATED DOCUMENTS

## 4.1 APPLICABLE ENGINEERING DRAWINGS

A complete set of drawings is supplied with each VT11 Graphic Display Processor. If any discrepancies are noted between the description in this manual and the drawings supplied with the equipment, consider the drawing set supplied with the equipment as reflecting the most accurate equipment representation.

## 4.2 DRAWING CODE

DEC's engineering drawings are coded to designate drawing type, major assembly, and series. A drawing number such as D-CS-M7013-0-1 reveals the following information:

| | |
|---|---|
| D | – Drawing Size |
| CS | – Drawing Type (Circuit Schematic) |
| M7013 | – Equipment Type |
| 0 | – Equipment Variation |
| 1 | – Drawing Number of a Series |

## 4.3 VT11 ENGINEERING DRAWINGS

Table 4-1 lists the major drawings for the VT11. Refer to the current Drawing Directory for a complete, up-to-date listing.

**Table 4-1**
**VT11 Engineering Drawings**

| Drawing Number | Title |
|---|---|
| B-DD-VT11-0 | Drawing Directory |
| A-PL-VT11-0-0 | VT11 Display Processor Parts List |
| K-WL-VT11-0-1 | VT11 Wire List |
| D-AR-VT11-0-2 | VT11 Configuration |
| C-IA-7009450-0-0 | Wired Assembly |
| D-IA-7009099-0-0 | Power Harness |
| C-IA-7009248-0-0 | Cable Keyed Interlock |
| D-IA-7009449-10-0 | Scope Connector Cable |
| D-CS-A320-0-1 | VT40 Display Generator |
| D-CS-M7013-0-1 | VT40 Display Control |
| D-CS-M7014-YA-1 | Bus Control and Bootstrap |
| D-CS-5410094-0-0 | Backplane Circuit Schematic |
| D-SP-GT40-0-2 | Base Diagrams |
| D-BD-GT40-0-4 | Display Processor Block Diagram |
| D-FD-GT40-0-5 through -14 | VT11 Flow Diagrams |
| D-TD-GT40-0-16 | Character Generator Timing |

## 4.4 RELATED DOCUMENTATION

Table 4-2 lists publications that contain related information of interest to the VT11 user.

**Table 4-2**
**Related Documentation**

| Title | Number | Subject |
|---|---|---|
| Light Pen Assembly Drawing Directory | B-DD-375-0 | |
| Light Pen Assembly | C-UA-375-0-0 | |
| Light Pen Amplifier | D-CS-G840-0-1 | |
| VR14 and VR17 CRT Display User's Manual | DEC-12-HVCRT-D-D | Maintenance |
| PDP-11 Processor Handbook | | Programming |
| PDP-11 Peripherals Handbook | | Interfacing |

# APPENDIX A
# CHARACTER CODES

| 7 Bit (octal) | ASCII Representation | Keyboard | VT11 Printing | VT11 Printing When Preceded By Shift-Out = 016 |
|---|---|---|---|---|
| 000 | NUL | CTRL @ | | λ |
| 001 | SOH | CTRL A | | α |
| 002 | STX | CTRL B | | ϕ |
| 003 | ETX | CTRL C | | Σ |
| 004 | EOT | CTRL D | | δ |
| 005 | ENQ | CTRL E | | Δ |
| 006 | ACK | CTRL F | | ∼ |
| 007 | Bel | CTRL G | | ϑ |
| 010 | BS | CTRL H | Backspace | ∩ |
| 011 | HT | CTRL I (TAB) | | ψ |
| 012 | LF | CTRL J (LF) | Line Feed | ÷ |
| 013 | VT | CTRL K | | o |
| 014 | FF | CTRL L | | ∴ |
| 015 | CR | CTRL M (CR) | Carriage Return | μ |
| 016 | SO | CTRL N | | £ |
| 017 | SI | CTRL O | | Shift In |
| 020 | DLE | CTRL P | | π |
| 021 | DC1 | CTRL Q | | ‖ |
| 022 | DC2 | CTRL R | | Ω |
| 023 | DC3 | CTRL S | | σ |
| 024 | DC4 | CTRL T | | ϒ |
| 025 | NAK | CTRL U | | ϵ |
| 026 | SYN | CTRL V | | ← |
| 027 | ETB | CTRL W | | → |
| 030 | CAN | CTRL X | | ↑ |
| 031 | EM | CTRL Y | | ↓ |
| 032 | SUM | CTRL Z | | ⌜ |
| 033 | ESC | CTRL [ (ALT) | | ⊥ |
| 034 | FS | CTRL \ | | ≠ |
| 035 | GS | CTRL ] | | ≈ |
| 036 | PS | CTRL | | ∨ |
| 037 | US | CTRL – | | □ |
| 040 | SP | SPACE BAR | Space 1 character | |
| 041 | ! | SHIFT 1 | ! | |
| 042 | " | SHIFT 2 | " | |
| 043 | # | SHIFT 3 | # | |

| 7 Bit (octal) | ASCII Representation | Keyboard | VT11 Printing | VT11 Printing When Preceded By Shift-Out = 016 |
|---|---|---|---|---|
| 044 | $ | SHIFT 4 | $ | |
| 045 | % | SHIFT 5 | % | |
| 046 | & | SHIFT 6 | & | |
| 047 | ' | SHIFT 7 | ' | |
| 050 | ( | SHIFT 8 | ( | |
| 051 | ) | SHIFT 9 | ) | |
| 052 | * | SHIFT : | * | |
| 053 | + | SHIFT ; | + | |
| 054 | , | , | , | |
| 055 | - ( minus) | - | - | |
| 056 | . | . | . | |
| 057 | / | / | / | |
| 060 | 0 | 0 | 0 | |
| 061 | 1 | 1 | 1 | |
| 062 | 2 | 2 | 2 | |
| 063 | 3 | 3 | 3 | |
| 064 | 4 | 4 | 4 | |
| 065 | 5 | 5 | 5 | |
| 066 | 6 | 6 | 6 | |
| 067 | 7 | 7 | 7 | |
| 070 | 8 | 8 | 8 | |
| 071 | 9 | 9 | 9 | |
| 072 | : | : | : | |
| 073 | ; | ; | ; | |
| 074 | < | SHIFT , | < | |
| 075 | = | SHIFT - | = | |
| 076 | > | SHIFT . | > | |
| 077 | ? | SHIFT / | ? | |
| 100 | @ | @ | @ | |
| 101 | A | SHIFT A | A | |
| 102 | B | SHIFT B | B | |
| 103 | C | SHIFT C | C | |
| 104 | D | SHIFT D | D | |
| 105 | E | SHIFT E | E | |
| 106 | F | SHIFT F | F | |
| 107 | G | SHIFT G | G | |
| 110 | H | SHIFT H | H | |
| 111 | I | SHIFT I | I | |
| 112 | J | SHIFT J | J | |
| 113 | K | SHIFT K | K | |
| 114 | L | SHIFT L | L | |
| 115 | M | SHIFT M | M | |
| 116 | N | SHIFT N | N | |
| 117 | O | SHIFT O | O | |
| 120 | P | SHIFT P | P | |
| 121 | Q | SHIFT Q | Q | |
| 122 | R | SHIFT R | R | |
| 123 | S | SHIFT S | S | |
| 124 | T | SHIFT T | T | |

| 7 Bit (octal) | ASCII Representation | Keyboard | VT11 Printing | VT11 Printing When Preceded By Shift-Out = 016 |
|---|---|---|---|---|
| 125 | U | SHIFT U | U | |
| 126 | V | SHIFT V | V | |
| 127 | W | SHIFT W | W | |
| 130 | X | SHIFT X | X | |
| 131 | Y | SHIFT Y | Y | |
| 132 | Z | SHIFT Z | Z | |
| 133 | [ | [ | [ | |
| 134 | \ | \ | \ | |
| 135 | ] | ] | ] | |
| 136 | ^ | ^ | ^ | |
| 137 | - | - | - | |
| 140 | ` | SHIFT @ | ` | |
| 141 | a | A | a | |
| 142 | b | B | b | |
| 143 | c | C | c | |
| 144 | d | D | d | |
| 145 | e | E | e | |
| 146 | f | F | f | |
| 147 | g | G | g | |
| 150 | h | H | h | |
| 151 | i | I | i | |
| 152 | j | J | j | |
| 153 | k | K | k | |
| 154 | l | L | l | |
| 155 | m | M | m | |
| 156 | n | N | n | |
| 157 | o | O | o | |
| 160 | p | P | p | |
| 161 | q | Q | q | |
| 162 | r | R | r | |
| 163 | s | S | s | |
| 164 | t | T | t | |
| 165 | u | U | u | |
| 166 | v | V | v | |
| 167 | w | W | w | |
| 170 | x | X | x | |
| 171 | y | Y | y | |
| 172 | z | Z | z | |
| 173 | | SHIFT [ | { | |
| 174 | | SHIFT \ | \| | |
| 175 | | SHIFT ] | } | |
| 176 | ~ | SHIFT ^ | ~ | |
| 177 | RUB OUT | R.O. | ■ | |

# APPENDIX B
# LIGHT PEN AMPLIFICATION

The input from the 375 Light Pen that results from detection of beam intensification is not usable in its analog form; it must first be converted to a TTL compatible signal. This is the prime function of the G840 Light Pen Amplifier module (drawing D-CS-G840-0-1 and Figure B-1).

In relation to the G840, the light pen phototransistor acts as a variable resistor that presents a low-going signal at the input (J1, pin 3) to the module when screen intensification occurs within the light pen's angle of acceptance. This negative-going analog signal is inverted by Q1, and peaked by the circuit at the collector of Q1. The signal, now positive-going with a greatly decreased rise time (about 1 $\mu$s), is differentiated before being input to the LM 306 Comparator.

The LM 306 is a high-speed voltage comparator designed to produce a sharp-edged, TTL compatible output when the input attains a predetermined threshold voltage. In this application, the (+) input to the LM 306 (pin 2) is held at about 400 mV. When the differentiated input at the (-) input reaches this threshold, a negative-going output signal

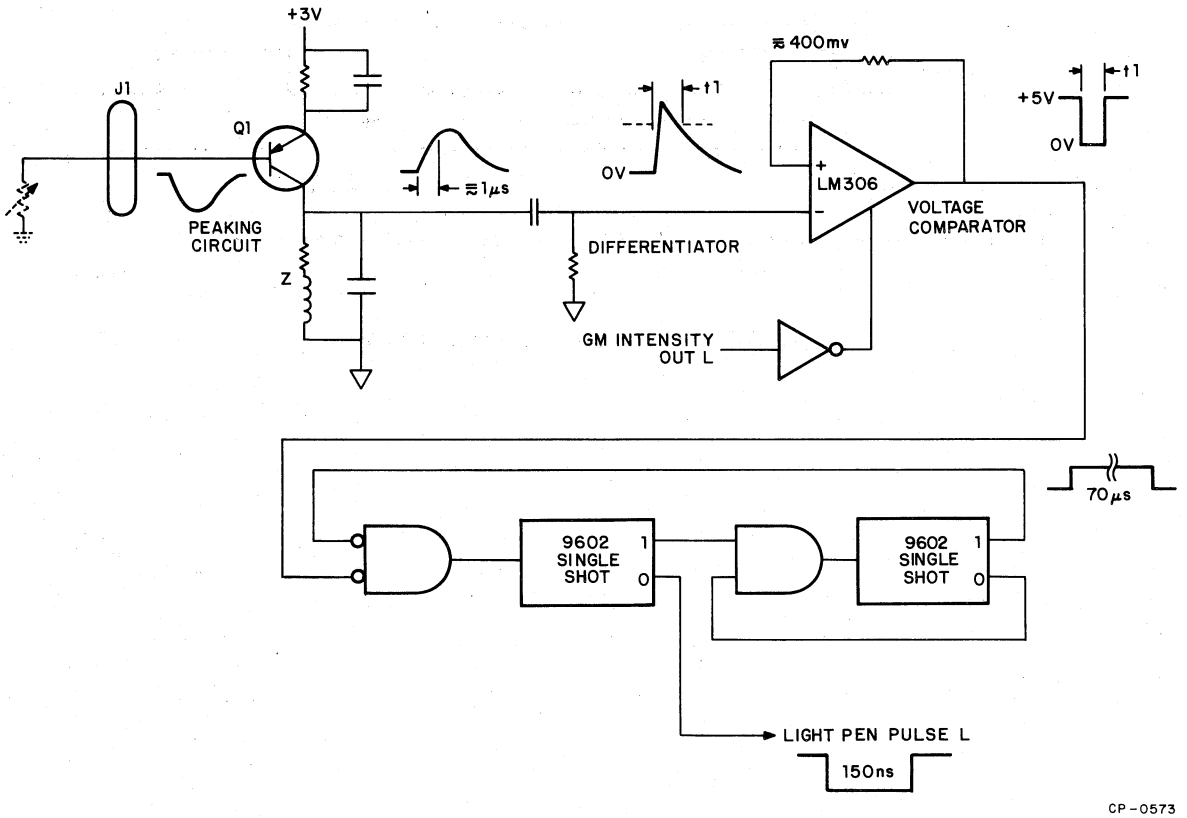



Figure B-1 Light Pen Amplifier

is produced at pin 7, provided the signal GM INTENSITY OUT L is present at E3 pin 13. This qualifying signal ensures that all light pen "hits" (LIGHT PEN PULSE L) from the G840 are valid, inhibiting those hits that might be generated by spurious noise from the light pen. The LM 306 output occurs about 30 ns after the two input voltages compare (fall time is approximately 20 ns) and remains low as long as the (-) input stays above the 400 mV threshold. This assertion time is indicated in Figure B-1 as t1. Positive feedback is provided from the output to the (+) input to assist the input signal comparison.

The negative-going output from the LM 306 triggers one stage of a 9602 Monostable Multivibrator, which, in this application, functions as a single-shot to produce a 150 ns output signal, LIGHT PEN PULSE L. Coincident with this signal from the 0 output, the 1 output from the first stage of the 9602 triggers the second stage, also configured as a single-shot. The 1 output of the second stage, high for 70 μs, inhibits a second light pen hit immediately following the first one. Timing for this operation is shown in Figure B-2. The comparator output assertion time is unimportant because only the negative-going transition is needed to initiate LIGHT PEN PULSE L.

In the event of a failure of either the +22 V or -22 V supply, deflection ceases and a bright spot occurs on the CRT resulting in a burn. To prevent this, the circuit on the G840 module that produces +5 V for the W684 intensity module will be disabled if either the +22 V or -22 V goes to 0 (in the case of a short circuit or blown secondary fuse). Referring to drawing D-CS-G840-0-1, if +22 V fails, Q3 loses forward bias (at the emitter) and turns off, shutting down the +5 V. If the -22 V goes to 0, Q2 loses emitter voltage and the base of Q3 goes high. This causes Q3 to turn off and +5 V drops.

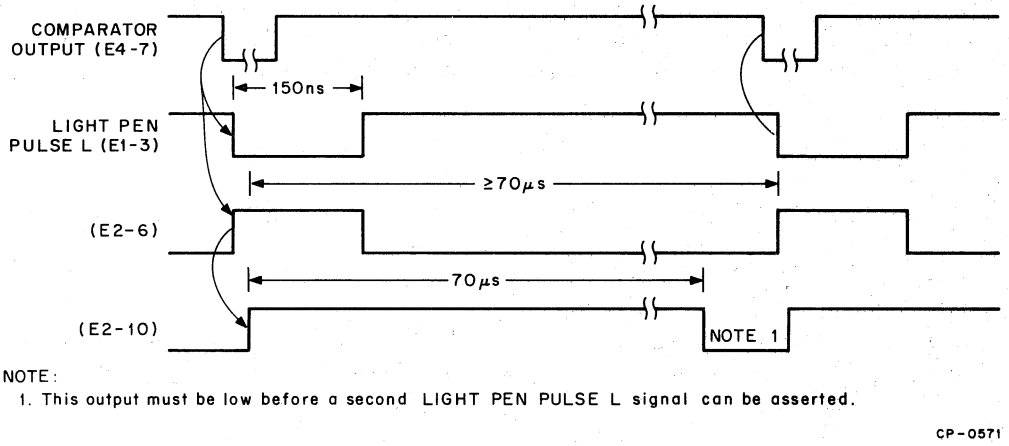



Figure B-2 Light Pen Pulse Timing, G840 Module

VT11 GRAPHIC DISPLAY PROCESSOR
DEC-11-HVTGA-A-D

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