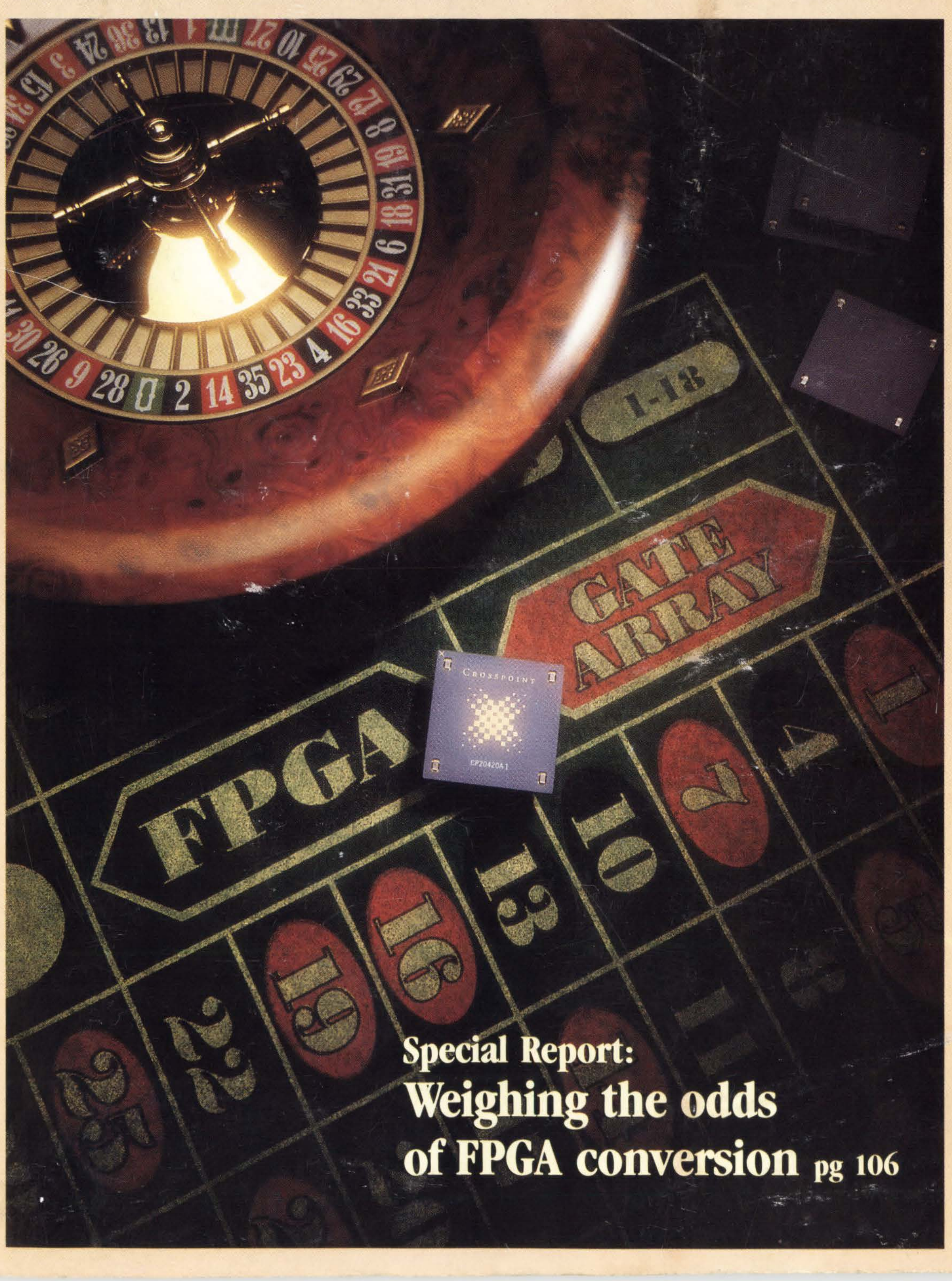
PROCESSOR UPDATES PG 89

EDN®

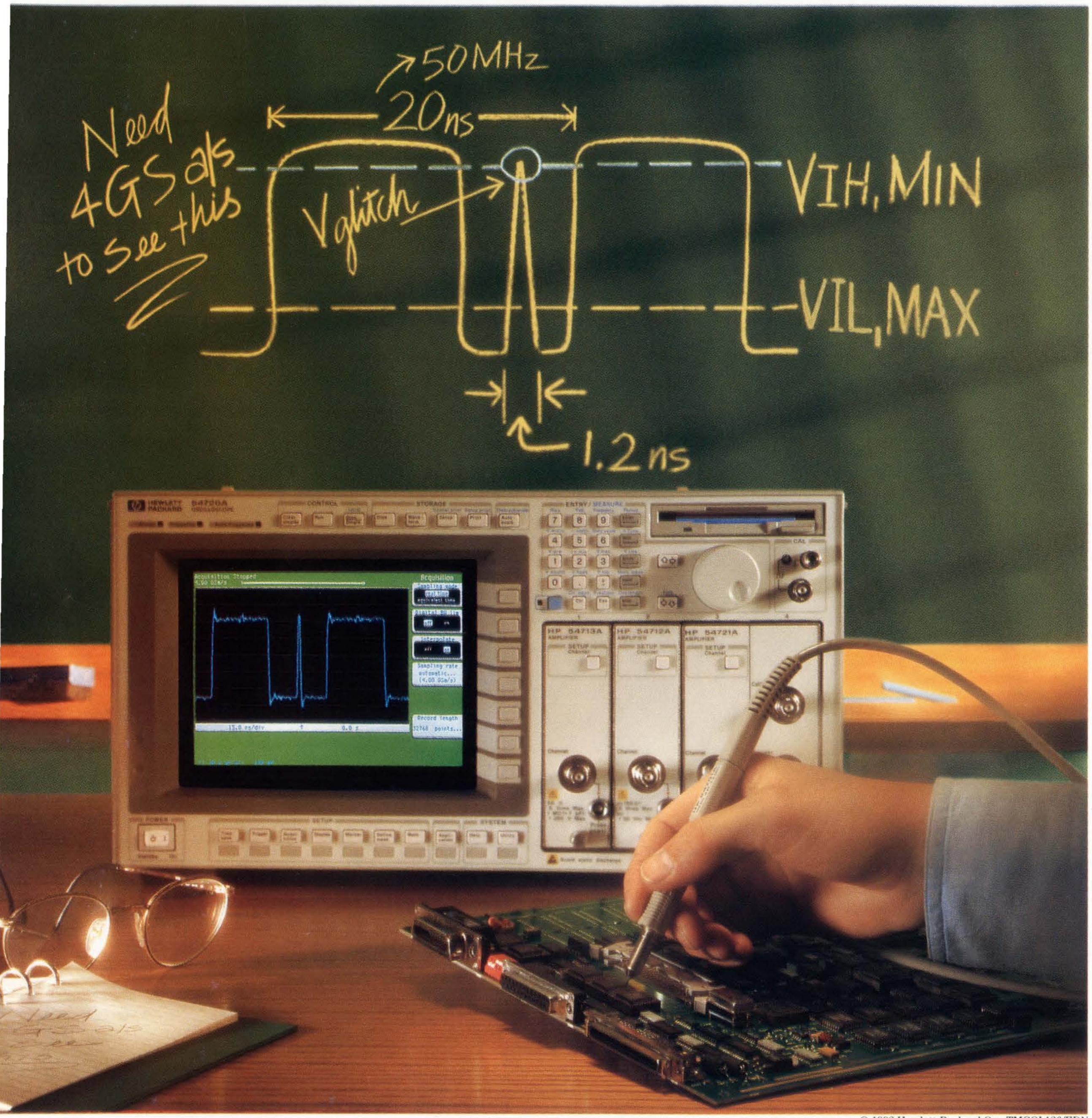
ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS WORLDWIDE

A CAHNERS PUBLICATION
June 4, 1992



Special Report:
Weighing the odds of FPGA conversion pg 106

HP's new 4 GSa/s scope helps you capture high-speed glitches.



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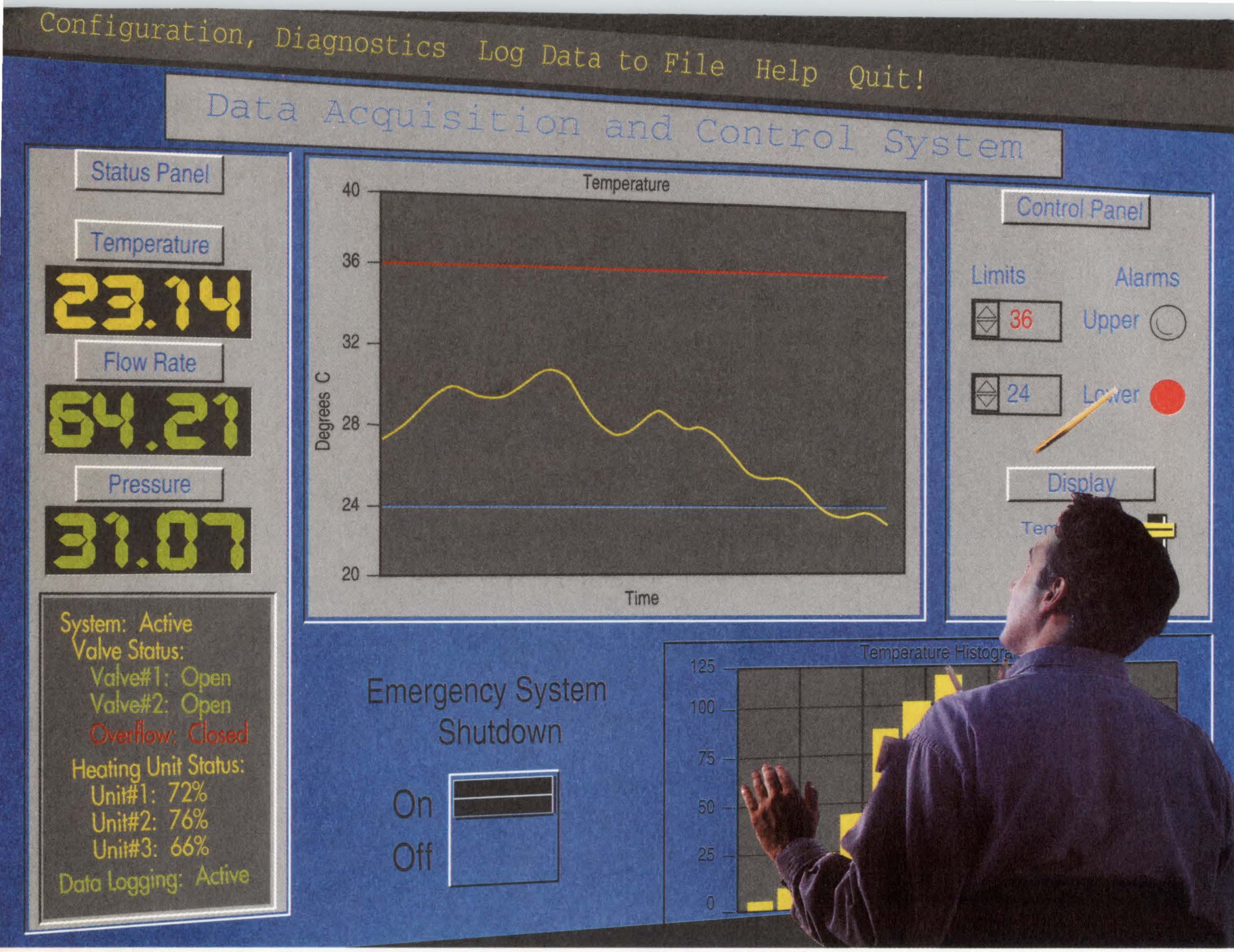

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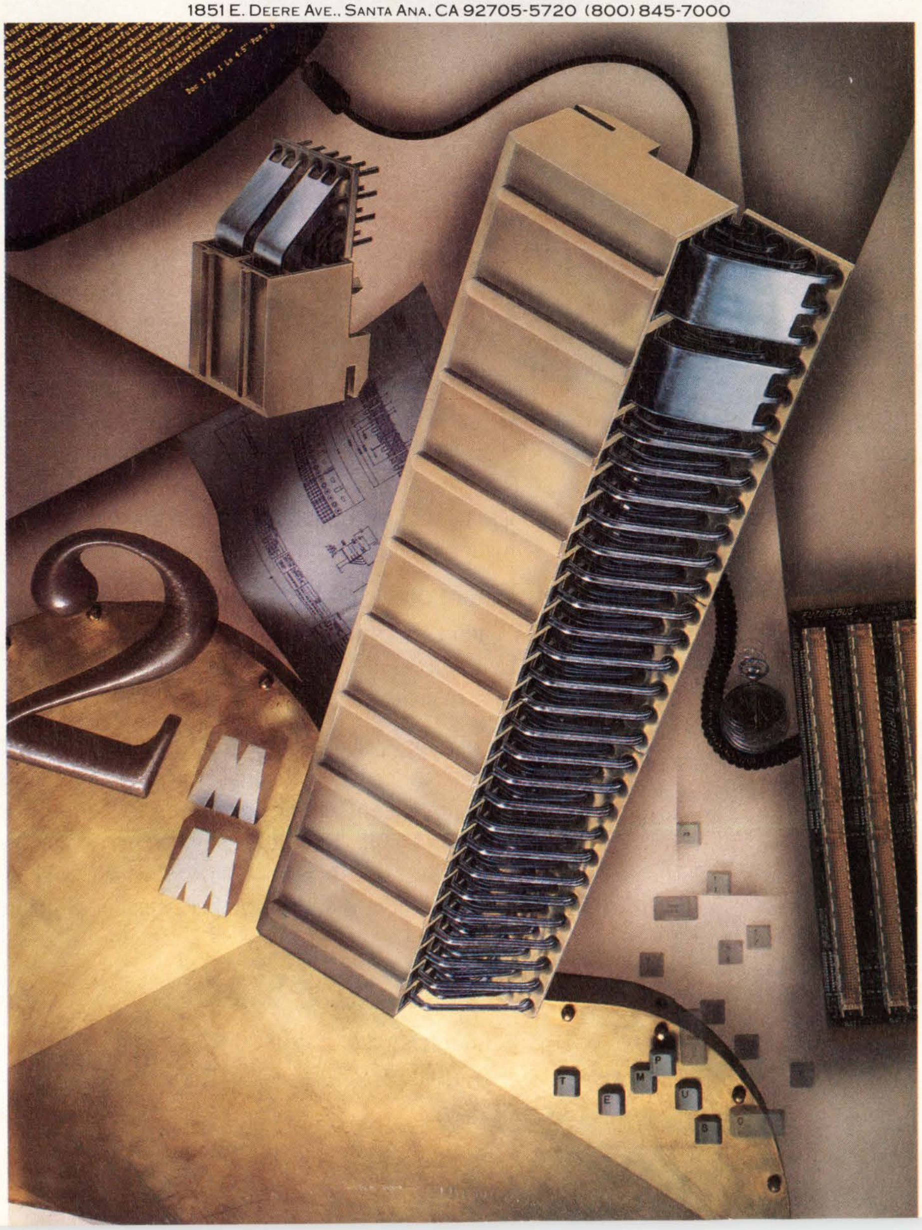

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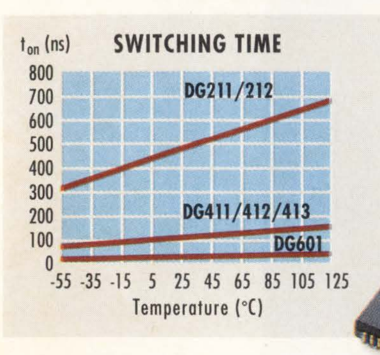

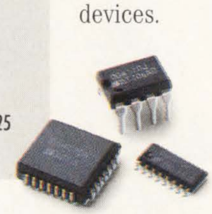

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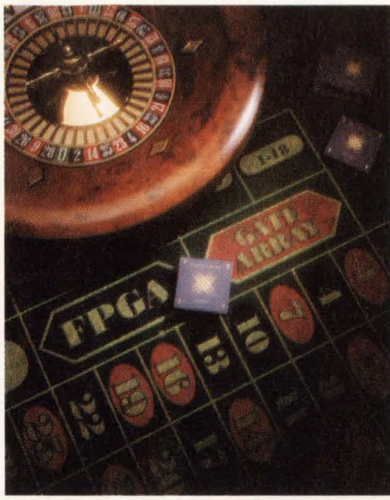
EDN
MAGAZINE EDITION

JUNE 4, 1992 VOLUME 37, NUMBER 12

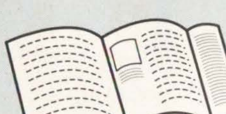
ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS WORLDWIDE



On the cover: Programmable-logic designers now have the chance to convert their field-programmable-gate-array designs to mask-programmed gate arrays. Before placing your bets on this design process, check out its potential risks and rewards. (Photo courtesy Crosspoint; concept and design by Curtin, Emerson, Ransick; photography by David Campbell Photography) . . . . **PAGE 106**

Foldout contents

Turn to the last information-retrieval service card in the back of this magazine and you'll find a foldout table of contents. Now, instead of flipping back and forth from this table of contents to the articles you want to read, you can have the convenient foldout open at all times while you're reading EDN. Use the foldout contents to mark off articles you'd like your colleagues to read or to remind yourself to copy stories for your files.



Continued on page 7

EDN®(ISSN 0012-7515, GST Reg. #123397457) is published 48 times a year (twice monthly with 2 additional issues a month, except for March and October, which have 3 additional issues and July and December which have 1 additional issue) by Cahners Publishing Company, A Division of Reed Publishing USA, 275 Washington Street, Newton, MA 02158-1630. Terrence M McDermott, President/Chief Operating Officer; Frank Sibley, Executive Vice President; Jerry D Neth, Senior Vice President/Publishing Operations; J J Walsh, Senior Vice President/Finance; Thomas J Dellamaria, Senior Vice President/Production and Manufacturing; Ralph Knupp, Vice President/Human Resources. EDN®is a registered trademark of Reed Properties Inc., used under license. Circulation records are maintained at Cahners Publishing Company, 44 Cook Street, Denver, CO 80206-5800. Telephone: (303) 388-4511. Second-class postage paid at Denver, CO 80206-5800 and additional mailing offices. **POSTMASTER: Send address changes to EDN®, PO Box 173377, Denver, CO 80217-3377.** EDN® copyright 1992 by Reed Publishing USA; Robert L Krakoff, President and Chief Executive Officer. Annual subscription rates for nonqualified people: USA, $119.95/year; Mexico, $169.95/year; Canada, $181.85/year; all other nations, $207.95/year for surface mail and $329.95/year for air mail. Single copies are available for $20 USA and $25 foreign. Please address all subscription mail to Ellen Porter, 44 Cook Street, Denver, CO 80206-5800.

CIRCLE NO. 7

EDN
MAGAZINE EDITION

JUNE 4, 1992

Continued from page 5

EDITORS' EDN CHOICE

EDN's technical editors selected the SuperSPARC μP as the innovative new product of the issue, naming it the Editors' Choice. Turn to the Processor Update section to learn about this first superscalar SPARC RISC μP, which can execute as many as three instructions in parallel each clock cycle . . . . **PAGE 89**

TECHNOLOGY UPDATES

PRODUCT UPDATE

PROCESSOR UPDATES

DESIGN IDEAS

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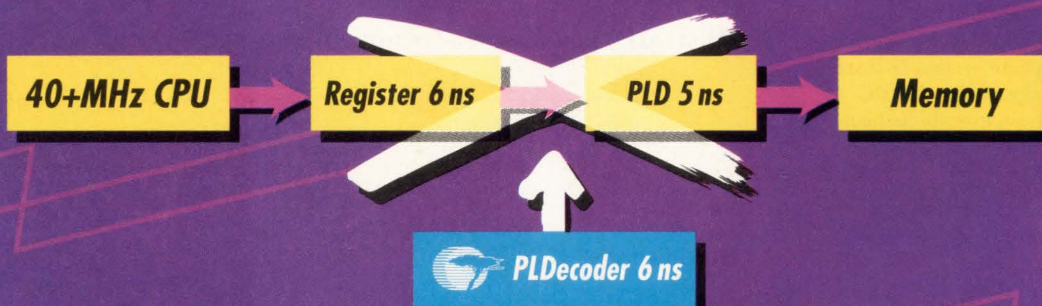

Introducing PLDecoders.

Taking systems to 40 MHz and beyond has become a whole lot simpler with these new, function-specific BiCMOS Decoder PLDs. For RISC, including our highest performance SPARC processors, choose the input-registered versions to capture addresses quickly. For CISC, such as 80X86, we offer output-latched versions that optimize system performance. Choose simple addressing versions at 6 ns for fastest performance, or 7 ns bank select or byte-write versions to suit your application precisely.

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Design is eased by PLDs developed specifically to implement memory decoding. Easier than using standard PLDs. Much easier than gate arrays.

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EDN
MAGAZINE EDITION

JUNE 4, 1992

Continued from page 7

EDITORIAL

PROFESSIONAL ISSUES

NEW PRODUCTS

DEPARTMENTS

INSIDE EDN

A summary and analysis of articles in this issue

Thanks to Electro '92, this issue of EDN comes to you packed with feature articles. But before you dig into these technical treatises, you might want to read about the winners of this year's **Design Ideas Grand Prize.** Moshe Gerstenhaber and Mark Murphy are splitting the $1500 prize for their entry, "Synchronous system measures $\mu\Omega$s." Upon learning he had won, Murphy said "I think I'll go to Disneyland." You could be next year's winner, but only if you send us a Design Idea. How 'bout it?

Meanwhile, you'll find plenty of information in this issue to help you with your own design ideas. In his Special Report, Senior Technical Editor Charles H Small discusses the advantages and problems associated with **converting FPGA designs into ASICs.** Every design engineer wants the safety cushion that conversion provides, but FPGA vendors say few companies actually exercise this option. If you want help in making that decision, Charles has made the work much easier for you. You'll find a spreadsheet with the appropriate financial calculations on EDN's electronic-bulletin-board system, and you'll find the details in his article.

One reason to convert FPGAs into ASICs might be to create a part that runs on 3.3V. You'll have a tough time finding 3V FPGAs right now, but you can find 3V ASICs, as well as a number of other logic parts. In his Technology Update on **3V circuits**, Technical Editor Dave Pryce explores the growing number of parts available for low-voltage logic circuits. If you are designing battery-powered products, or systems that have heat-related problems, you must read this article, if only to learn the difference between parts designed for 3V operation and 5V parts that have been recharacterized for 3V operation. Dave also discusses the interoperation of 5 and 3V logic.

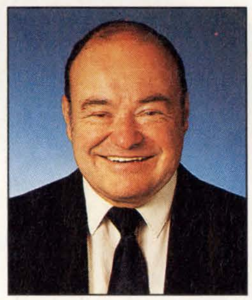
Technical Editor John A Gallant looks at the problems of **interoperability for LANs** in his Technology Update. LAN standards tell you what equipment should do, but not how to do it. Consequently, vendors create products that implement these standards in a variety of ways. John says that compatibility doesn't necessarily result in interoperability. He also says that one of the best techniques used to ensure interoperability is the use of implementers' agreements, often struck because vendors have agreed to demonstrate interoperability at a trade show. As the trade-show opening day approaches, compatibility transforms into interoperability.

Finally, if you've wanted to experiment with DSP μPs but don't know where to start, you might want to take a look at my Technology Update on **DSP μP evaluation kits.** Many of these kits give you all of the software and hardware you need (except for a PC) to start learning about DSP.

Steven H Leibson
Executive Editor

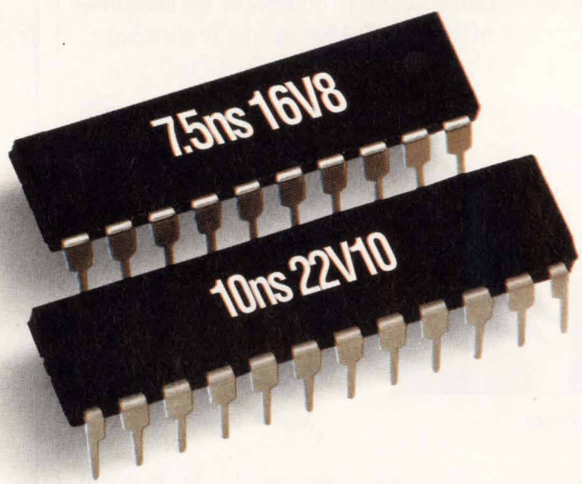
Charles H Small

Dave Pryce



John A Gallant

Low Delays.



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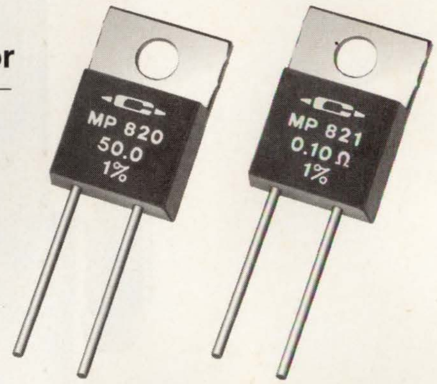

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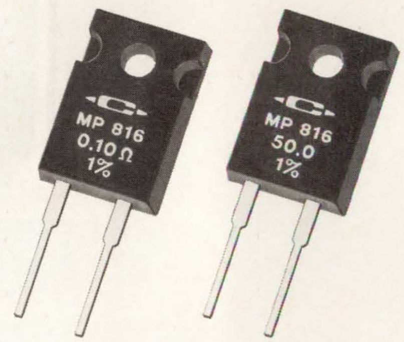

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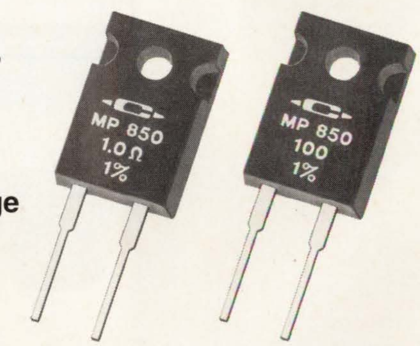

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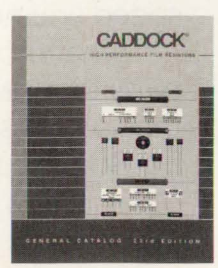

CIRCLE NO. 17

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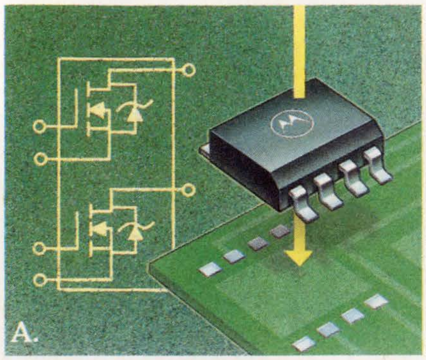
Power Design News

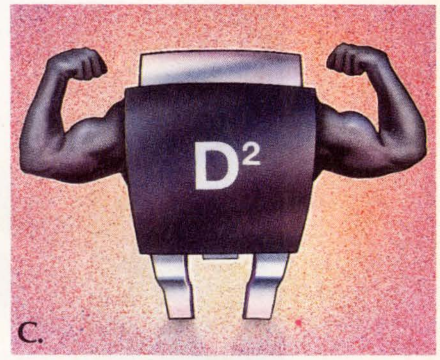


Two new dual TMOS surface mount MOSFETs simplify circuit design.

Motorola's two new dual TMOS surface mount MOSFETs simplify circuit design through component count and board space reduction. The MMDF3C05 consists of a pair of complementary N- and P-channel TMOS MOSFETs in a half bridge configuration in the SO-16 package, while the MMDF4N02 is a dual N-channel device in an SO-8 package. These are standard SOIC packages which fit the same footprints as standard SOIC packages. Ideal uses include low voltage, low power motor control applications such as disk drives, tape drives, optical drives, printers and plotters.

Cure non-isolated power packaging headaches.

Motorola's fully isolated TO-220, TO-218 Type and ICePAK™ power packages eliminate the need for hardware, physical inventory and labor costs associated with isolating a non-isolated package. You can also improve productivity and yields by reducing assembly line errors that can cause premature failures. The new UL-recognized isolated TO-220 and TO-218 packages—available in Motorola rectifiers, Bipolar power transistors and TMOS® Power MOSFETs—replace the non-isolated packages and associated isolating hardware required when mounting them directly to a heatsink or chassis.



Surface mount package power champ.

Motorola has developed a new package believed to have higher power capabilities than any existing surface mount package. The D²PAK is rated at a PD of 2.5 watts at TA=25°C when mounted on G10/FR-4 printed circuit board using the recommended footprint. D²PAK, available in Motorola rectifiers and TMOS power MOSFETs, can house the same size chips as the industry standard TO-220, and enable manufacturers to produce their surface mount products with a higher degree of reliability. D²PAK has the ability to handle a large die, thus allowing it to be used in surface mount applications requiring components with higher current capabilities and lower conduction losses, such as the 50 amp, 60 volt MTB50N06E MOSFET with an $R_{DS(on)}$ of .028 ohms max.

The advantages of our Bipolar Power Transistors for audio amplifier applications are loud and clear.

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Extra! Extra! Read all about Motorola's new TO-247.

Rounding out Motorola's complete portfolio of isolated and non-isolated power packages is our new partially-isolated TO-247 package for Motorola rectifiers, TMOS power MOSFETs and Bipolar power transistors. Thanks to this packaging innovation, less mounting hardware is required because the screw hole is isolated from the tab. This eliminates the need to use an insulating bushing around the mounting screw, thus facilitating installation.

Get more information.

To learn more about any of these Motorola products, contact your local Motorola sales office, complete and return the coupon below to Motorola Semiconductor Products, Literature Distribution Center, P.O. Box 20912, Phoenix, AZ 85036, or call us toll-free any weekday, 8:00 a.m. to 4:30 p.m. (MST), 1-800-441-2447.

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- ☐ C. Surface Mount Power Package (D²PAK PAK/D)
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16R6
48N22
16R8
18V8Z
20L8
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Innovators present check to Portland State

On April 7, 1992, Paul Gulick and Arlie Conner, EDN's 1992 Innovators of the Year, donated their $10,000 award to Portland State University and the MOS IC Design Program. The school plans to use the donation to fund a graduate-student scholarship during the next academic year. "To a small university program such as ours, this contribution is, of course, important to the graduate-student recipient," said W Robert Daasch, Assistant Professor in the MOS IC Design Group at Portland State, "but it also provides encouragement to other companies in high technology and other industries to get in on the fun." Gulick and Conner were named Innovators of the Year for a technology they developed for Infocus Systems for triple supertwist nematic displays. The pair chose Portland State University because the university's current research program is similar to the work of Conner and Gulick.

—Susan Rose

The 1992 Innovators of the Year donated the $10,000 prize money to Portland State University. Pictured from left to right are Innovation winners Paul Gulick and Arlie Conner of Infocus Systems, EDN Editor Jon Titus, and Robert Daasch and Rolf Schaumann of Portland State University.

Mentor takes first step to Verilog compatibility

In step one of a 3-phase product plan, Mentor Graphics introduced a translation program, called V-Net, that converts designs from the company's own Design Architect format into Verilog hardware descriptions. This $5000 product will let existing Verilog users design products using Mentor's design tools while preserving existing design models written in Verilog. In addition, the company has modified its Timebase delay calculator so that it emits timing information in a Verilog-compatible format in addition to the company's proprietary simulator format. Timebase computes path delays in ASIC designs. Mentor Graphics Corp, Wilsonville, OR, (503) 685-7000.

—Steven H Leibson

SBus card adds data acquisition to SPARCstations

The ADDA data-acquisition subsystem for SBus systems can perform real-time A/D and D/A functions with no host-CPU intervention. The 18-in.^{2} card includes a 16-channel input section to a 14-bit A/D converter, and a 4-channel output from an 18-bit DAC. The board can use a maximum sample rate of 166 kHz to capture data. A 128-kbyte array of dual-ported RAM stores captured data. Software support for the board includes a Unix driver that's provided as source code and as an executable program file. The package also includes a control program, called Adview, and a digital oscilloscope and function-generator program, called Digosc. The ADDA subsystem costs $2495, and you can buy A/D- or D/A-only versions for $1895. Analyx Systems Inc, Fremont, CA, (510) 656-8017, FAX (510) 657-0927.

—Maury Wright

12-bit quad DAC has serial interface

The Max514 quad 12-bit DAC can replace four 16-pin DACs. It comes in a 24-pin narrow DIP or a 28-pin small-outline package with commercial (0 to 70°C) and extended-industrial (−40 to +85°C) temperature ranges. The device dissipates 10 mW max; it has 1.5-LSB gain accuracy, guaranteed monotonicity, 1-LSB relative accuracy, 1-μsec output settling time to 0.5 LSB, and a 5V power supply. Each DAC has its own reference input. Production quantities for the $15.79 (1000) units will be available in June. Maxim Integrated Products, Sunnyvale, CA, (408) 737-7600.

—Susan Rose

X-server software performance jumps 10×

Version 1.5 of Xoftware for Windows is 4 to 30× faster than the preceding version. The $495 software package runs under Microsoft Windows and implements an X-Window server. It uses the Microsoft Windows network drivers for LAN communications. Similar products are available for PC systems running DOS or DOS with graphics adapters that implement Texas Instruments' TIGA specification. Age Logic Inc, San Diego, CA, (619) 455-8600.

—Steven H Leibson

ISA board bundles LAN, disk, graphics, modem, and I/O

Integrators or end users who need to get the most from a single 16-bit ISA bus slot for a PC should consider the Sigma Six. The full-length adapter card includes an Ethernet LAN interface, a super-VGA graphics controller, 2400-bps data and 9600-bps fax modems, hard- and floppy-disk controllers, and parallel and serial I/O ports. The Ethernet interface includes connectors to 10Base-T twisted-pair and coaxial media. The graphics capability supports noninterlaced resolutions as high as 1024 × 768 pixels. The board also includes a Flash EPROM socket that you can configure to store MS-DOS on board. The Sigma Six costs $695, or you can buy a version without Ethernet support for $550. AMT Computers Inc, Pomona, CA, (714) 598-6120, FAX (714) 598-7716.—Maury Wright

Use a single chip for notebook computers

The ML4860 single-chip power controller replaces the five chips normally required for power conversion and regulation in notebook and laptop computers and portable instruments. The chip has a built-in dc/dc converter and regulator, which ensures that a computer's battery voltage is regulated to 5V by the µP and other digital logic. You can configure the chip for 3.3V. A technique, called synchronous rectification improves the efficiency of the process that regulates a battery's voltage down to 5 or 3.3V, thus extending battery life by 5%.

The chip can also disconnect a computer's battery when an ac adapter is plugged in. The chip uses an n-channel MOSFET transistor as a switching element, rather than the standard p-channel MOSFET. In sleep mode, the chip draws 75 µA; in full-power mode, it draws 4 mA. Users can also customize the chip, which costs $4.95 (1000) in a 28-pin plastic leaded chip carrier. Samples are available now. Micro Linear Corp, San Jose, CA, (408) 433-5200.—Susan Rose

Wireless-LAN-module samples available

GEC Plessy Semiconductors is currently sampling 1-Mbyte/sec wireless-LAN-module prototypes to key customers. The modules operate at 2.4 GHz, have a range of roughly 100 ft, and use frequency-hopping spread-spectrum techniques that conform to FCC Part 15 regulations. Consequently, the modules won't require operating licenses. By early 1993, the company plans to reduce the modules to credit-card-sized OEM products that draw 250 mW and cost less than $100 (10,000). GEC Plessy Semiconductors, Scotts Valley, CA, (408) 438-2900, FAX (408) 438-5576, contact Bob Zavrel.

—Steven H Leibson

Create analog behavioral models without equations

The Analog Model Synthesis software from Analogy automatically creates behavioral models using graphical data from previous simulations or from lab instruments. The behavioral analog models run on the company's Saber simulator. The behavioral models can simplify and speed-up simulation for a previously simulated circuit block. Using lab-instrument data entry you can create behavior models directly from circuits or components. The software works with both time- and frequency-domain data. The software costs $2000 and will be available in July. Analogy, Beaverton, OR, (503) 626-9700.—Doug Conner

GPS board set costs less than $500 in quantity

You can add GPS (global-positioning-system) navigation to your design for less than $500 (1000) with the GPS-10 board set. Samples cost $1000. The set includes a 4 × 2.65-in. circuit board, an antenna, and an antenna cable. The board can determine its location anywhere on Earth by tracking as many as eight GPS navigation satellites to within 15m—or 100m, depending on the US DoD's whim—if it already knows approximately where it is, the time, and the date. If you're completely lost and don't have a convenient timepiece, the board can determine your position in 15 minutes. The product supplies velocity data in addition to providing the time and 2- or 3-D position information once/sec. Bidirectional communication with the board is in ASCII over an asynchronous serial link at rates of 1200 to 9600 bps. The board runs on 5V and consumes 200 mA. Garmin International, Lenexa, KS, (913) 599-1515, FAX (913) 599-2103.

—Steven H Leibson

Controller doubles data-transfer rates

Zilog's Z16C32 integrated universal serial-communications controller runs at 20 Mbytes/sec, which is double the data-transfer rate of the company's Z16C31. The higher rate meets T1, Ethernet, and European E1/E2 standards, as well as other proprietary protocols that have 20-Mbyte/sec operating speeds. Status and control handling improve

Continued on pg 22

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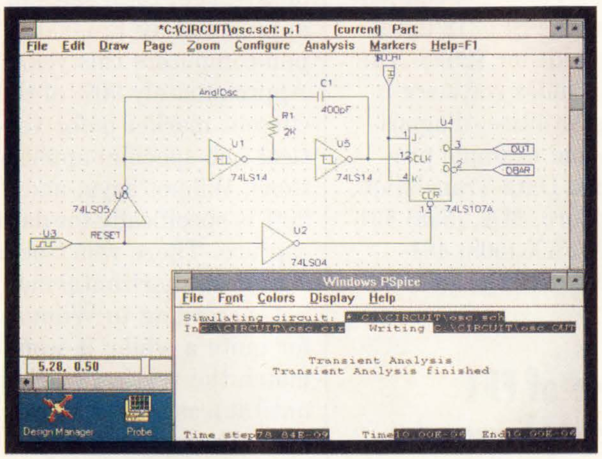

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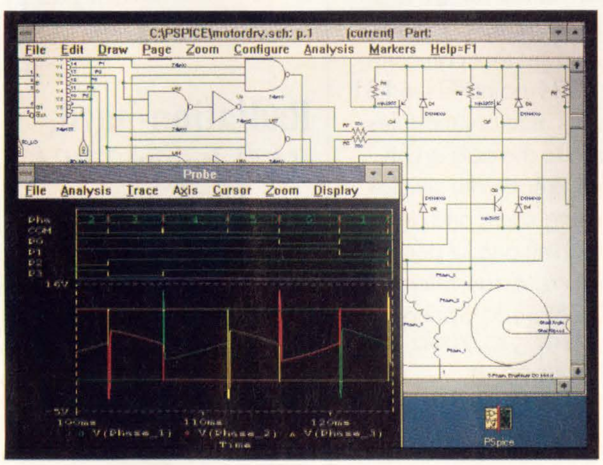

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CIRCLE NO. 24

IC-analysis system integrates verifier and prober

A family of IC-analysis stations from Integrated Measurement Systems provides ASIC designers and semiconductor quality-assurance engineers with the kind of circuit-faults information that was previously available only to designers of discrete-component circuits. The stations combine an IC-verification system, a submicron-resolution mechanical wafer prober, a laser for cutting through passivation layers, a fixturing system, and navigational software that helps you find your way around an IC as you view a small portion of it through a microscope or on a video display. Typical pricing of an analysis station is $500,000.

The vendor regards analysis stations based on mechanical probers as complementary to those based on electron-beam (E-beam) probing. First of all, the mechanical-prober-based systems cost approximately $250,000 less than the E-beam systems. In addition, the mechanical-prober technology permits probing multiple circuit nodes simultaneously, making absolute voltage measurements and injecting stimuli into internal nodes. E-beam probing systems can't directly stimulate internal nodes. Integrated Measurement Systems, Beaverton, OR, (503) 626-7117, FAX (503) 644-6969.—Dan Strassberg

Continued from pg 20

data handling and reduces CPU overhead. The controller can write critical frame status and length information into the array tables in DMA modes. Locating stored data is therefore not dependent on finding the end of the frame, which eliminates the need for large onboard status FIFO buffers and lets you scatter and gather an unlimited quantity of frames in a 4-Gbyte address range. A 16-Mbyte/sec version in a plastic leaded chip carrier is $7 (1000), and a 20-Mbyte/sec version is $8.50. Zilog Inc, Campbell, CA, (408) 370-8056.

—Susan Rose

DSP-based ATE boards provide multiprocessing

Suitable for dynamic test-and-measurement applications that require real-time data processing, the DT3801 Series ISA plug-in boards can operate at speeds reaching 320 kHz to capture 1 Msample/sec. The engine driving these boards is a Texas Instruments TMS320C40 DSP processor, which provides six communications ports and a 6-channel DMA engine to provide simultaneous and independent operation of all I/O devices as the chip processes signal data. The DT3801-G is a 12-bit board that runs at 250 kHz and sells for $7595. The $7195 DT3808 is a 160-kHz, 16-bit board with simultaneous sample and hold capability. The 12-bit DT3809 lets you selectively run all channels at 320 kHz or a single channel at 1 MHz and costs $7495. You can purchase the SP0312 developer's kit for $2995. The kit includes software tools, utilities, diagnostics, and example programs. Data Translation, Marlboro, MA, (508) 481-3700, FAX (508) 481-8620.—J D Mosley

Price of FFT parts plummets

The a66DK1 design kit puts $5500 worth of FFT parts in your hands for $1495. The kit includes a 40-MHz a66 chip set that can compute 1024-point FFTs in 131 μsec, six memory modules tailored to the a66 architecture, a software simulator, user guides, and data sheets. Limit one kit per customer site. Array Microsystems, Colorado Springs, CO, (719) 540-7999, FAX (719) 540-7950.

—Steven H Leibson

Pen computers aim at smaller, narrower markets

The forecast market for pen computers is shrinking by leaps and bounds. According to Dr Robb Wilmot, chairman of Fujitsu Personal Systems, market-forecasting firms have reduced their projections, on average, by a factor of four in the past two years. The forecasts now reflect reality, according to Wilmot; the original predictions were unrealistically rosy. Seven current forecasts predict, on average, total sales of approximately 125,000 pen computers this year. Approximately 90% of the current market is for vertical (job-specific) applications, Wilmot says, and 80% is specifically for data capture. There won't be a significant horizontal market, according to Wilmot, for quite a while; it won't match the vertical market until at least 1994, he predicts. For more information on pen-based computers, see the April 23, 1992, issue of *EDN*, page 137.

—Gary Legg

Radiation-hard, RAM-based FPGA on the horizon

Military and aerospace designers can obtain radiation-hard field-programmable gate arrays (FPGAs) as a result of an agreement between Harris Semiconductor and Xilinx Inc. The agreement calls for Harris to rework Xilinx's FPGAs and produce fully tested, radiation hardened, Class-S parts. The parts will be 100% pin and logic compatible with the Xilinx MIL-STD-883

Continued on pg 24

Continued from pg 22

FPGA and Xilinx development tools.

Lead times for space-related products, such as satellites, are shrinking to two or three years. FPGAs provide space-equipment designers additional flexibility to meet shorter deadlines. In addition, engineers can start their designs now using standard Xilinx parts and then plug in the radiation-hard parts when they're available. The first parts are scheduled for release in the second quarter of 1993, starting with the Xilinx XC30208, an 1800-usable-gate FPGA in a 100-pin quad flatpack. Harris will use its 1.25-μm proprietary silicon-on-sapphire technology. Harris Semiconductor, Melbourne, FL, (800) 442-7747, ext 7013. Xilinx Inc, San Jose, CA, (408) 559-7778, FAX (408) 559-7114.—Ray Weiss

PC-board-design software embodies top-end features

Cadstar 7 from Racal-Redac is a single-user PC DOS-based EDA tool for designing pc boards. The basic package includes schematic capture, pc-board layout, and automatic routing. An optional advanced-feature router extends performance to include gridless layouts, simultaneous multilayer routing, and manufacturing enhancements.

The software can design pc boards with 10,000 connections, 2000 components, 16 layers, multiple power and ground planes, and SMT components on both sides. The user interface reduces operator intervention by anticipating and defaulting to your next command. User-defined function keys for common commands or macros further simplify operation. In schematic-capture mode, a graphical symbol and a component library browser let you display data on the selected part. For critical analog layouts, you can position some parts manually and then let automatic placement complete the work. Other automatic routines swap equivalent gates or pins or rename all components in a single operation. The automatic router in the basic package lets you select grid increments down to 0.01 in.

The advanced router supports gridless layouts for high-density designs and simultaneously routes 16 layers. A single-pass mode lets you assess potential routing success. Rip-up and retry, and shove-aside algorithms offer further assistance to route difficult traces. To ease pc-board manufacture, the advanced router also features layout enhancements such as acid-trap removal, staircase elimination, segment minimization, and trace spacing equalization.

The tool costs £4850; the advanced router costs £2750. Purchased together, the combination costs £6995. Racal-Redac Ltd, Reading, UK, 734-782158; in the US, Racal-Redac Inc, Mahwah, NJ, (201) 848-8000.—Brian Kerridge

Chip provides convolutional-code interleaving

The SRT32INT performs interleaving and deinterleaving for forward error-correcting codes. When coupled with a 1k × 1-bit SRAM, the chip implements an (I,J) convolutional interleaver and deinterleaver. You program the size of the interleaver by using one of 12 possible (I,J) parameter pairs ranging from (4,32) to (32,4096).

Convolutional interleaving expands burst error-correction capabilities for forward error-correcting codes. For example, when you use the chip with the company's (24,12) triple error-correction-code chip (the SRT 241203), the combination can correct burst errors as long as 12,285 bits.

The chip also performs synchronization for deinterleaving operations. The IC costs $16.50 in a 44-pin LCC (1000). Space Research Technology Inc, Houston, TX, (713) 782-2244.—John Gallant

Get power-factor correction and battery backup

The P1204 switching power supply delivers 1200W of power-factor-corrected power with built-in battery backup. The unit delivers as much as 200A from the main output and as much as 500W from auxiliary outputs. Main output voltages are 2 to 48V dc from the main, and 2 to 24V dc from the auxiliaries. Power-factor correction is 0.995. Conversion efficiency is 73% at 230V ac. Supply input voltage can range from 90 to 264V ac.

The 5×8×16-in. supply has a battery-backed module that hooks to an external 48V-dc battery. The module charges the battery when power is available. An on-line converter converts battery power into system power. Supply features include current sharing, remote margining and programming, soft start, overload and thermal protection, remote sensing on all outputs, and reverse air flow. Jeta Power Systems Inc, Signal Hill, CA, (310) 427-0095.—Ray Weiss

5V IC includes RS-232C and RS-422 drivers

An on-chip charge pump lets the $3.75 (1000) AD7306 multiprotocol driver/receiver run on 5V and provides two RS-232C and one RS-422 drivers. The chip also includes one RS-232C receiver and one receiver that you can configure for RS-232C or RS-422 operation. The charge pump requires external 0.1-μF capacitors, and you can tap some of the pump's energy to power other circuits. The RS-232C channels will operate at 100 kbps, and the RS-422 channels can operate at 5 Mbps. Analog Devices, Norwood, MA, (617) 329-4700.

—Steven H Leibson

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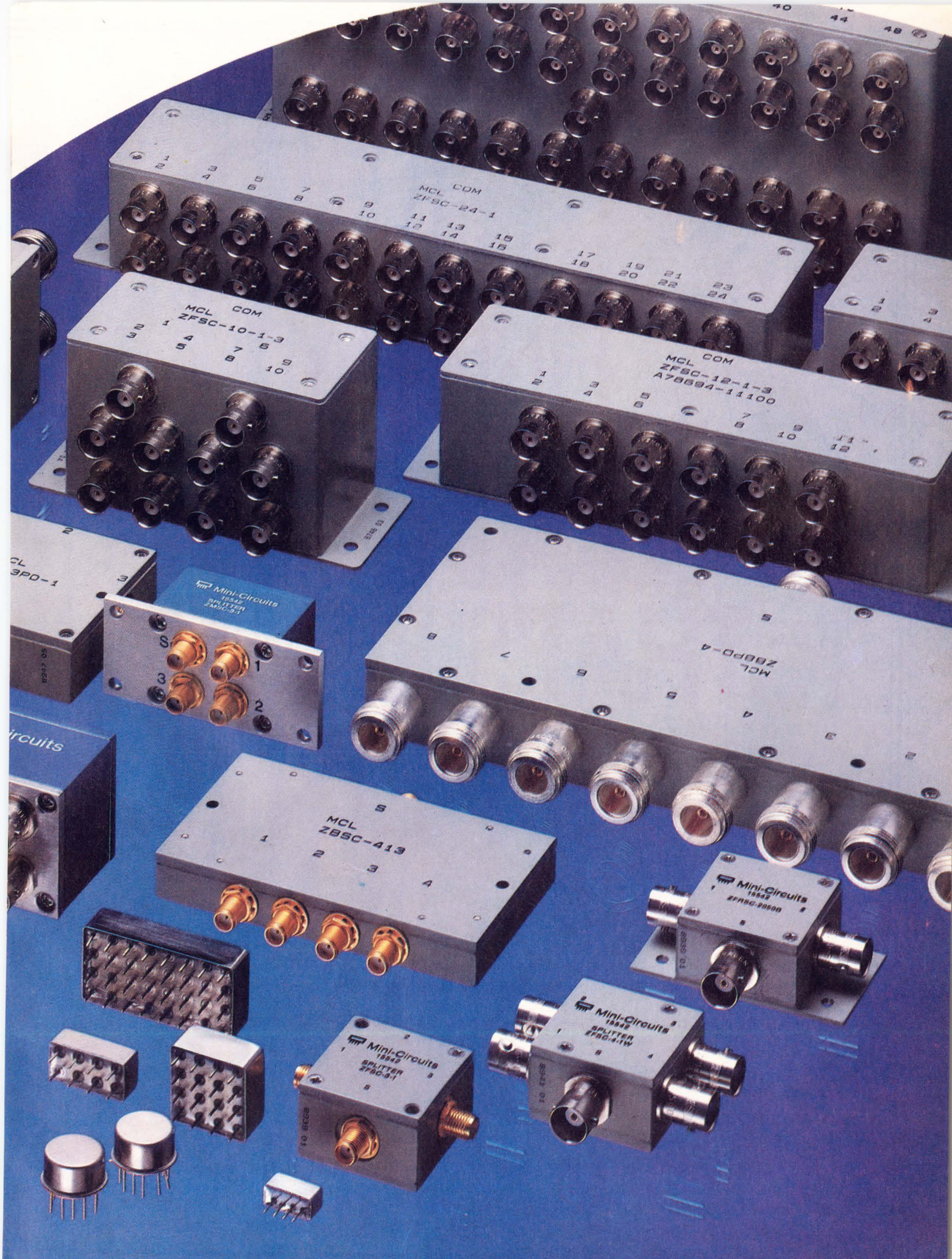
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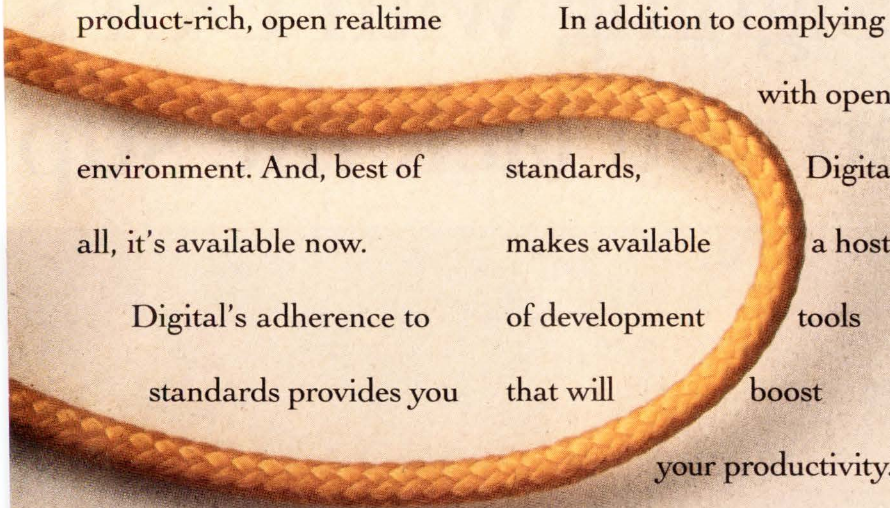

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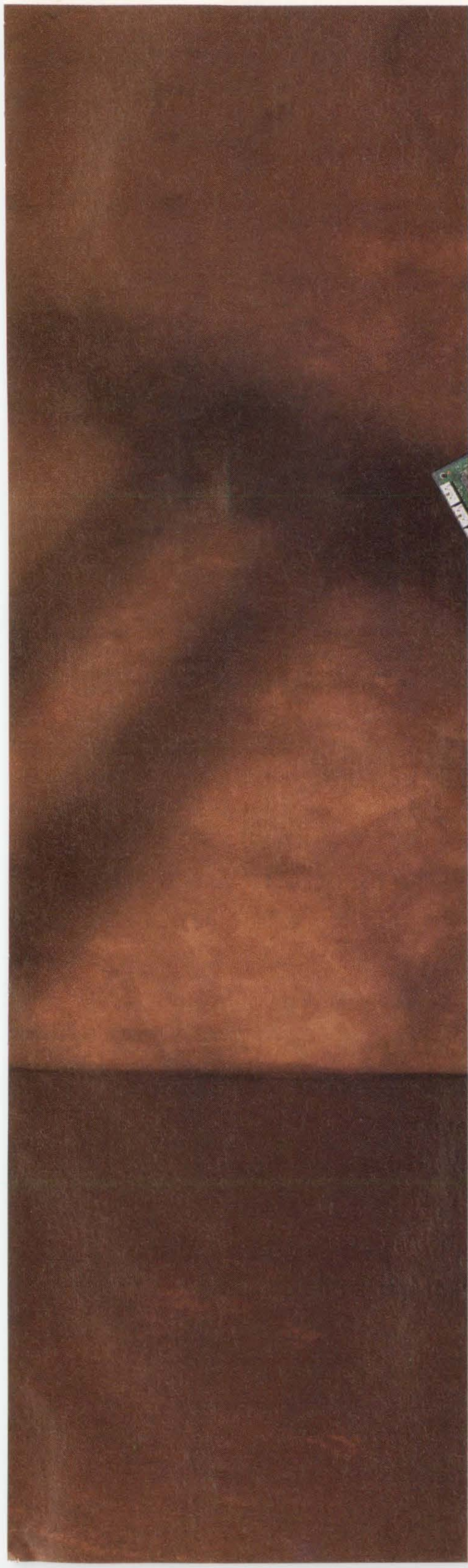

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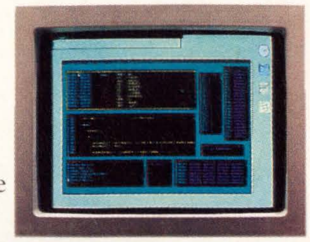

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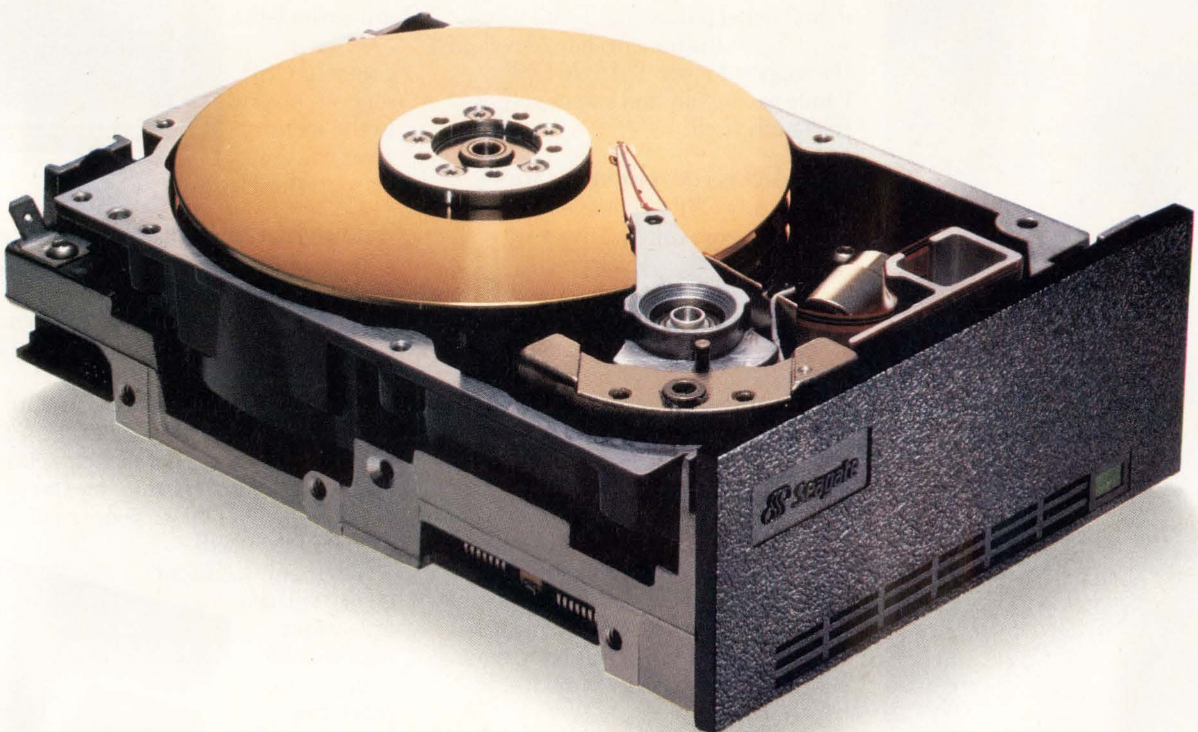

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Tax policies affect "prosperity" of all

In Dan Strassberg's editorial "Where have all the investments gone?" (EDN, February 17, 1992, pg 55), he says that like most engineers he is no expert on economics. As another engineer, I say there *are* no experts on economics.

Economics is not a science. It is nonrepeatable and, therefore, not predictable. The economists who do occasionally forecast the economy accurately owe their expertise more to luck than astute deciphering of the vagaries of economics.

The most significant influence on where investment money goes is government tax policy. During the eighties, investment rewards were slanted toward real estate, particularly industrial and commercial real estate. Tax policies made it a good investment even though overbuilding was rampant. The 1986 and 1990 tax reforms scuttled real-estate-investment advantages, destroying the market for real-estate investment. The so-called S&L scandal is a direct result of government tax policy that encouraged high risk and reckless investment in real-estate boondoggles.

This is a nation of entrepreneurs. Millions of individuals are ready and willing to invest in potentially profitable enterprises. All that's needed to open the floodgates is favorable tax policies that permit investors to earn rewards proportional to the risk involved.

The stock market is near an all-time high because stocks are perceived as the best investment around. To a degree, that is indirectly favorable because any company that offers a good return on investment or growth potential can raise capital through the stock market. A more favorable tax policy for investment in R&D, plant, and equipment would produce a torrent of funds pouring into those areas. Advances in technology, skilled jobs by the millions, and economic prosperity would result.

The approach of politicians and bureaucrats is that "we," meaning the government, must do something to help the economy. The best thing they can do is remove the investment tax penalties and stay out of the way. The right tax policies will create investment, jobs, and prosperity. Wrong tax policies will and do create depression, unemployment, and economic turmoil as investors try to select prudent and worthwhile investments.

E V Gustavson
Glendale, CA

Reader points out another player in multimedia

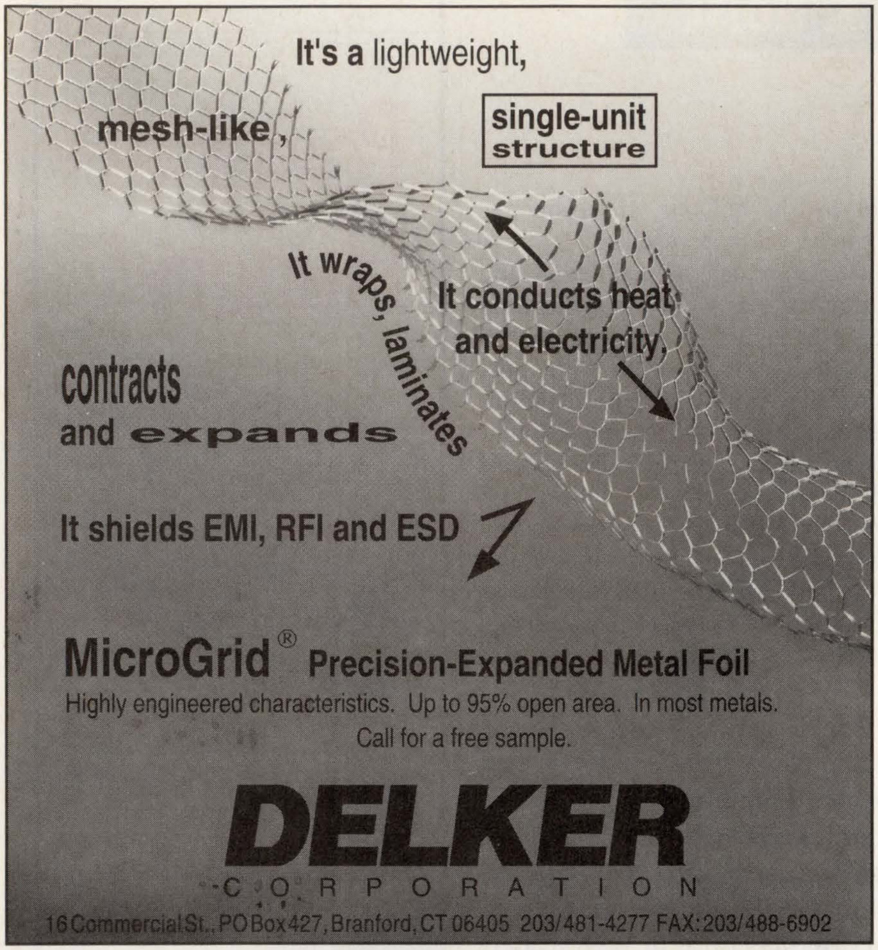
The Special Report on multimedia (EDN, March 16, 1992, pg 100) does a grave disservice to your readers by assuming that the standards developed by IBM and Apple are the be-all and end-all of multimedia. There is another player in the multimedia game—one that has been there longer, functions better (if you go by the company it keeps), and costs much less—Commodore's Amiga.

Commodore hasn't pushed the Amiga to make it a household name, like Apple or IBM, but with the addition of Newtek's Video Toaster, the Amiga works just as well, if not better, than any of the systems noted.

Aaron Minner
Software Engineer
Motorola Inc
Schaumburg, IL

Small companies *can* order small quantities

I read Julie Anne Schofield's editorial, "Companies can still profit while fostering innovation" (EDN, March 16, 1992, pg 33), with much interest and circulated it among my sales and customer-service colleagues. Being a budding microelec-



CIRCLE NO. 33

CIRCLE NO. 34

tronics company ourselves, we've experienced the "big guy/little guy" syndrome. We've developed [the following] customer-service policies that accommodate all customer requests, regardless of their corporate size or the potential of their future business:

- Apex is a manufacturer of hybrid and monolithic power amplifiers and hybrid dc/dc converters. We sell our parts in quantities as small as a single piece. We take Mastercard and Visa.
- When a company or individual wishes to place an order with us for the first time, and they are not rated with Dunn & Bradstreet, we set them up with a $1000 line of credit so they can make a purchase while we run a credit check.
- We have an evaluation unit-purchase plan. This allows the customer to order and receive small quantities for evaluation, which can be returned within 30 days with no obligation to purchase. If we receive the units back within the 30 days and they are in proper working condition, the customer is not charged.

Every customer is important, no matter how big or small. Those companies that have forgotten this customer-service principle need help remembering this from time to time.

Marie G Rivera
Product Marketing Specialist
Apex Microtechnology Corp
Tucson, AZ

WHAT'S NEXT IN EDN

The June 8 EDN News Edition—a special CAE issue—will provide details of an annual EDA survey in a bound-in supplement. In the Careers section, the staff will describe how object-oriented programming is affecting CASE development. Look, too, for DAC hot products.

EDITED BY JULIE ANNE SCHOFIELD

Root-sum-squared calculation justified

In the February 3 issue of EDN, Gary Altman requested a justification for using root-sum-squared tolerance analysis. In the April 9 issue, we printed a response from James A Kuzdrall, who urged using the utmost caution in using the root-sum-squared method to predict system error based on the errors of individual components. This next letter provides the theoretical justification for the root-sum-squared calculation.

Root-sum-squared analysis gives you the wrong answer if you want the maximum possible overall tolerance. Suppose we have a 10V voltage reference with 1% tolerance, followed by a 10:1 voltage divider of 2% accuracy, and we measure the output with a meter of 3% accuracy. Obviously, we should read 1V from the meter. If we are unlucky and the reference is 1% low, the divider divides 2% too much, and the meter reads 3% low, we will get a figure that is (1%+2%+3%)=6% low. This figure represents the worst-case tolerance. The root-sum-squared method yields $\sqrt{1^2+2^2+3^2}\%=3.74\%$. In real life, we'd expect some tolerances going one way to be canceled out by other tolerances going the other way.

Suppose our circuit consists of components whose values can deviate, as in our example, from their nominal values by 1%, 2%, and 3%. Further suppose that the manufacturing processes are such that the actual values are uniformly distributed; that is, our 1% voltage reference could be anywhere from 9.9 to 10.1V with equal probability. Although the 1% figure represents a maximum possible deviation, over a large sample, the average deviation from the nominal value will be ½%.

In statistics, it's easiest to use the rms deviation (the statisticians call it the standard deviation). For our uniform distribution, the standard deviation is actually $(1/\sqrt{2})\%$, or 0.71%. Similarly, our voltage divider has a standard deviation of $(2/\sqrt{2})\%$ and our meter $(3/\sqrt{2})\%$. The deviation in the number the meter reads is the algebraic sum of the individual deviations; if our reference is ½% high, our divider 1% low, and our meter reads 2% high, then the figure displayed has an accuracy of ½%−1%+2%=+1½%.

In statistics, the Central Limit Theorem states that (1) if a random variable is the sum of a lot of other random variables independent of each other, then the mean of the "big" random variable is the sum of the means of the "little" random variables; (2) the variance of the big variable is the sum of the variances of the little ones (or the standard deviation of the big variable is the root of the sum of the squares of the standards of deviation of the little random variables); and (3) the distribution of the big random variable is approximately normal and gets better the more little random variables there are.

We can use this theorem in our discussion because the deviation of our meter reading (our "big" variable) is the sum of the individual deviations. Also, our "little" random variables are independent of each other. (We would be surprised if our voltage-reference tolerance affected our divider manufacturing process.) Apply-

ing the theorem, we find that (1) the meter reading averages out at the nominal if we make lots of circuits, and (2) the standard deviation of the meter reading is

$$\sqrt{[(1/\sqrt{2})^2+(2/\sqrt{2})^2+(3/\sqrt{2})^2]}=2.65\%.$$

By looking at the root-sum-squared method carefully, we'll see that it yields a tolerance that is $\sqrt{2}$ times the standard deviation of the output reading; 3.74% is $\sqrt{2}$ times the standard deviation of 2.65%. We now invoke the last part of the Central Limit Theorem and use the fact that the output reading has a normal distribution. Using normal distribution tables, we see that the probability of a random variable being more than 1.414 standard deviations away from the mean is 0.158. Thus, the probability of our actual reading being on or within 3.74% tolerance is $1-0.158$, or 0.842, which is pretty good.

Summarizing, I can say that if the circuit satisfies the assumptions I've stated (you should check the independence of components that come in batches, such as resistors), to get a worst-case tolerance you add the individual tolerances. To get a tolerance that will be equaled or bettered by 84.2% of production units, take the root of the sum of the squares.

I hope this is useful.

Peter F Vaughan
Aero Transformers Ltd
Barnstaple, Devon, UK

Mac owner wants CAE packages

I am a Macintosh owner and am looking for equivalents to some of the CAE packages you have on the EDN Bulletin Board System. I'd like to find versions of these packages that my machine could run natively. I am looking for a Gerber file editor/viewer, a Macintosh version of Spice, pc-board layout and autorouting tools, and any cross compilers that would work.

Gregg Vallan
Sharon, MA

We don't have any Macintosh equivalents of the CAE packages available on the EDN BBS. However, the following two companies offer CAE software, such as that you seek, for Macintosh computers:

Douglas Electronics
2777 Alvarado St
San Leandro, CA 94577
(415) 483-8770
FAX (415) 483-6453

Vamp Inc
Box 411
Los Angeles, CA 90028
(213) 466-5533
FAX (213) 466-8564.

Technical-article database to appear on EDN BBS

Help! Sometime in late 1990 to the middle of 1991, EDN ran an excellent short article about ADC antialiasing filter specsmanship. The article discussed the various tradeoffs in filter selection, as well as providing a filter/

ADS primer. During the course of several job transitions I lost the issue and now find myself in need of the information it contained. I have not been able to locate the article in the company library and need your help to determine in which issue it was published.

An annual index would be a great help in locating articles and design ideas. There are pathologically organized individuals out there who diligently keep track of each morsel of information in every journal they receive, but most of us have neither the time nor the inclination to do so. Since publishers maintain such a database as part of doing business, how about providing it to us overburdened readers either annually or on the bulletin board?

Greg Hardy
McDonnell Aircraft Co
St Louis, MO

First, the article you describe is Technical Editor Dan Strassberg's "Avoid overspecifying antialiasing filters." The story starts on page 76 of the July 18, 1991 issue of EDN.

Second, your idea of putting an article index on the EDN BBS was so good that we recently came up with it ourselves. In the next month or so, we will upload a technical-article database. The database will include articles that appeared from November 1989 to October 1991 in EDN Magazine and News Editions, Electronic Design, Electronic Products, Computer Design, and Electronics.

Socket lets you modify IC pinouts

In response to Clancy Sloan's request for 8233 quad digital multiplexers in the March 2, 1992, Ask EDN, I submit the following two possible solutions, both of which I have used with success.

Although I was not able to find data sheets on the 8233, its function could be similar to other available parts such as the 74xx157 or 93xx22. If this is the case and only the pinouts are different, Sloan should contact Aries Electronics and request information on its Correct A Chip product. This programmed socket can reroute circuit paths so that an existing footprint on a pc board can accept a substitute IC.

If no part can be found that performs the required function, perhaps a programmable logic device could be used in conjunction with the Aries socket to fulfill the 8233's task.

Aries Electronics Inc
Box 130
E Frenchtown, NJ 08825
(908) 996-6841
FAX (908) 996-3891

Mark Henry
Telenex
Mount Laurel, NJ

Be on the lookout for emulator manual

I have an old Intel blue box called a Prompt 48, which is used to program and emulate the MCS 48 family of mi-

crocontrollers. Can anyone point me towards a copy of a manual?
Robert E Bober
Framingham, MA

If anyone happens across such a manual, please contact Ask EDN.

Closed-caption encoder IC found

I need to find out if there is an IC that will encode closed-caption information in the NTSC vertical blanking interval.
Mathew John
NAWC-WPNS
Point Mugu, CA

Motorola sells the MC144143 closed-caption encoder IC for $2.47 (100).

Motorola Semiconductor Products Inc
Box 20912
Phoenix, AZ 85036
(800) 521-6274
FAX (602) 952-4190

Music explains use of octave

Why is it that in electronics we use the word "octave" to designate a frequency ratio of 2:1? Octave is defined in the English language as a group or series of eight. It is derived from the Latin word "octavus," which means eighth. What happened to the six in between?
Ana-Maria Dias
Application Engineer
Datel Inc
Mansfield, MA

The Western musical scale has traditionally had eight notes defined by whole-number ratios based on the fundamental. The proportional scale intervals repeat every eight notes, and the eighth note has a 2:1 ratio to the fundamental. Since the time of J S Bach, the scale has been fudged slightly to allow key changes and "chromatic" notes. Now, notes no longer have whole-number ratios. They are all $1{:}\sqrt[12]{2}$ apart. Nonetheless, we still refer to a doubling of frequency as an octave.

Have you been stumped by a design problem? Can't interpret a spec sheet? Ask EDN. Our editors are ready to help.

The Ask EDN column serves as a forum to solve nagging problems and answer difficult questions. EDN's editors will provide the solutions. If we can't solve a problem, we'll find an expert who can, or we'll print your letter and ask your peers for help.

Address your questions and answers to Ask EDN, 275 Washington St, Newton, MA 02158; FAX (617) 558-4470; MCI: EDNBOS. Or, send us a letter on EDN's bulletin-board system; you can reach us at (617) 558-4241. You'll need a 9600-bps (or less) modem and a communications program set for 8,N,1. From the Main System Menu, enter SS/ASK_EDN and select W to write us a letter.

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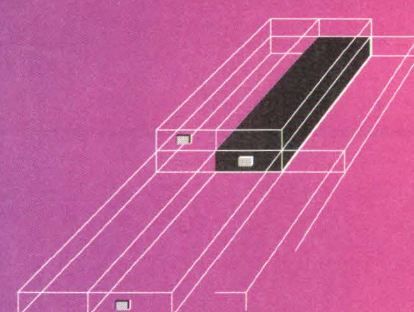
Model	Nominal Voltage (V)	Capacity (mAh) at 0.2C rate	Standard Charge: Charging Current (mA)	Standard Charge: Time (Hrs.)	External Dimensions (including tube): L (mm)	External Dimensions (including tube): W (mm)	External Dimensions (including tube): T (mm)	Weight (approx.g)
KF-A600	1.2	600	60	14-16	67.0	17.0	6.1	23
KF-A900	1.2	900	90	14-16	67.0	17.0	8.1	30
KF-A1200	1.2	1200	120	14-16	67.0	17.0	10.3	38
KF-B600	1.2	600	60	14-16	48.0	17.0	8.1	21
KF-B400	1.2	400	40	14-16	48.0	17.0	6.1	16



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CIRCLE NO. 38

Everyone wins

The results of a recent international study would have you believe that young students in the United States have little interest or aptitude in science and math. The results of a recent competition at a small New England high-school gymnasium would seem to belie that conclusion.

Several hundred feet from the gym, I could already hear the partisan cheers from the kids in the overflowing bleachers. Inside, an outlandish array of miniature tethered robots, built with specified components by teams of engineers and high-school students, were engaged in a contest designed to promote one elementary, yet influential, idea: learning is fun, and fun is good.

The concept went like this: members of high-tech corporations would fund and team up with local high-school students to design and construct remote-controlled machines, which would gobble up tennis balls having different point values. Each team received identical raw materials and had six weeks to construct a robot to compete head-to-head in qualifying heats against the other teams' machines. Within certain guidelines, the design of each machine was limited only by each team's imagination and engineering skill. The competition mimicked real engineering situations: some of the designs were inspired, while others never made it out of the starting gates.

The competition was the brainchild of US First (For Inspiration and Recognition of Science and Technology), a Manchester, NH-based, nonprofit organization founded by entrepreneur Dean Kamen. US First points out that the US spends more money on education than any other nation in the world. Therefore, there's no shortage of educational *supply*. Instead, there's a lack of *demand* for education by our students. US First's goal is to arouse kids' interest in science, in turn creating that demand and raising scientific literacy.

What did the kids get out of the competition? You could see the excitement and pride in their faces when they fired up their robots for head-to-head competition. They got to see and learn from real engineers—not preconceived caricatures or stereotypes. They got a feel for the essence of engineering, and they got to see that it's cool to be part of a team that solves problems by using intellect and instinct, rather than brute force.

What did the companies—IBM, Motorola, AT&T, Raytheon, and Boeing, to name a few—get out of it? The competition didn't radically change any corporate worlds. But by getting involved on an extremely personal level, the companies made a small step toward ensuring an ample supply of technically literate employees and customers—people that they'll depend on in the future.

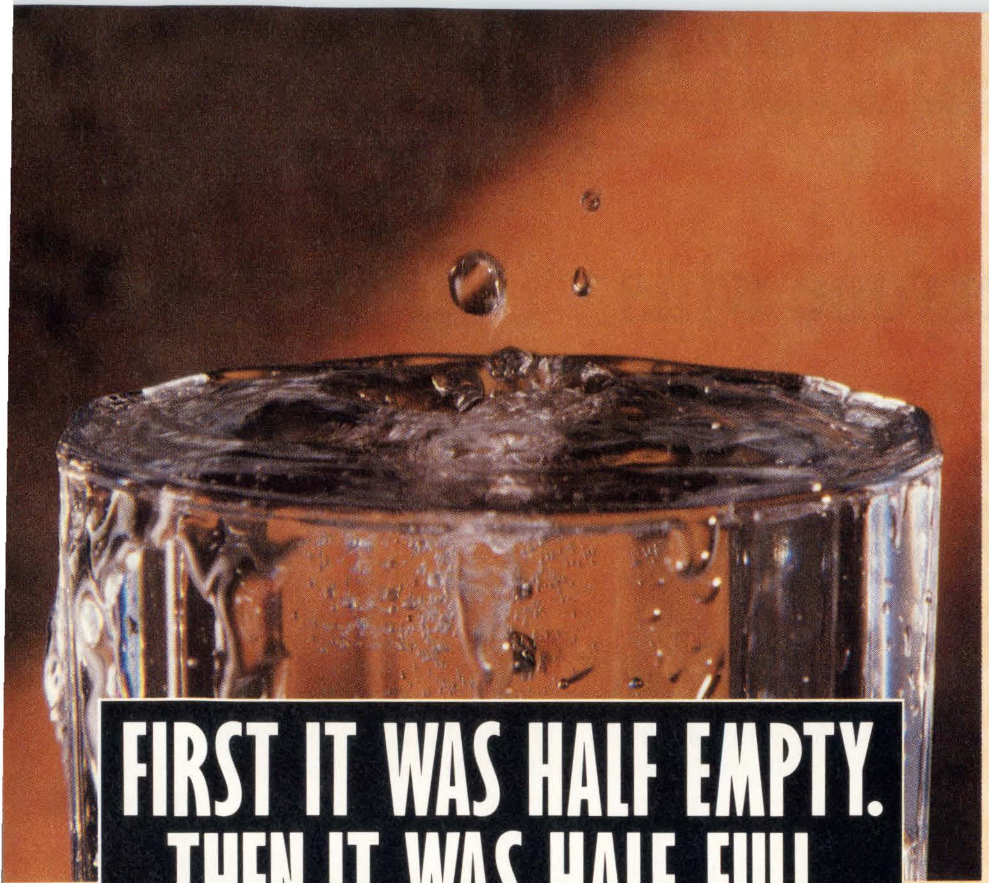
If your company would like information about next year's competition, contact US First at 340 Commercial St, Manchester, NH 03101. Phone (603) 666-3906.

Joan Morrow Lynch
Managing Editor

Jesse H. Neal
Editorial Achievement Awards
1990 Certificate, Best Editorial
1990 Certificate, Best Series
1987, 1981 (2), 1978 (2), 1977, 1976, 1975

American Society of Business Press Editors Award
1991, 1990, 1988, 1983, 1981

Send me your comments via fax at (617) 558-4470, or on the EDN Bulletin Board System at (617) 558-4241 300/1200/2400, 8,N,1; on 9600-bps modems, try (617) 558-4580, 4582, or 4398.



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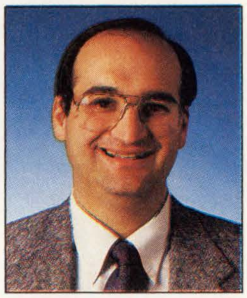
THE REST IS HISTORY

CIRCLE NO. 39

DSP EVALUATION KITS

Learn to use DSP chips with a minimum of pain

STEVEN H LEIBSON, Executive Editor



The architectural diversity of DSP µPs makes them unusually tough to use. Evaluation kits ease your educational burden by giving you an operational piece of hardware and the software you need to make the hardware do something useful.

Design engineers suffer from an embarrassment of riches with regard to processor architectures, and digital signal processing is no exception. The dropping prices of low-end DSP chips and the ever-improving performance of high-end DSP chips makes these parts candidates for a growing number of designs. This rapidly expanding universe of potential DSP designs creates a tremendous knowledge burden for you. If you want to use the most cost-effective design approach and if you want to complete your design quickly, you're going to have to learn fast. Recognizing the tremendous need for DSP education, semiconductor vendors offer a variety of evaluation kits to help you adopt their DSP chips more quickly.

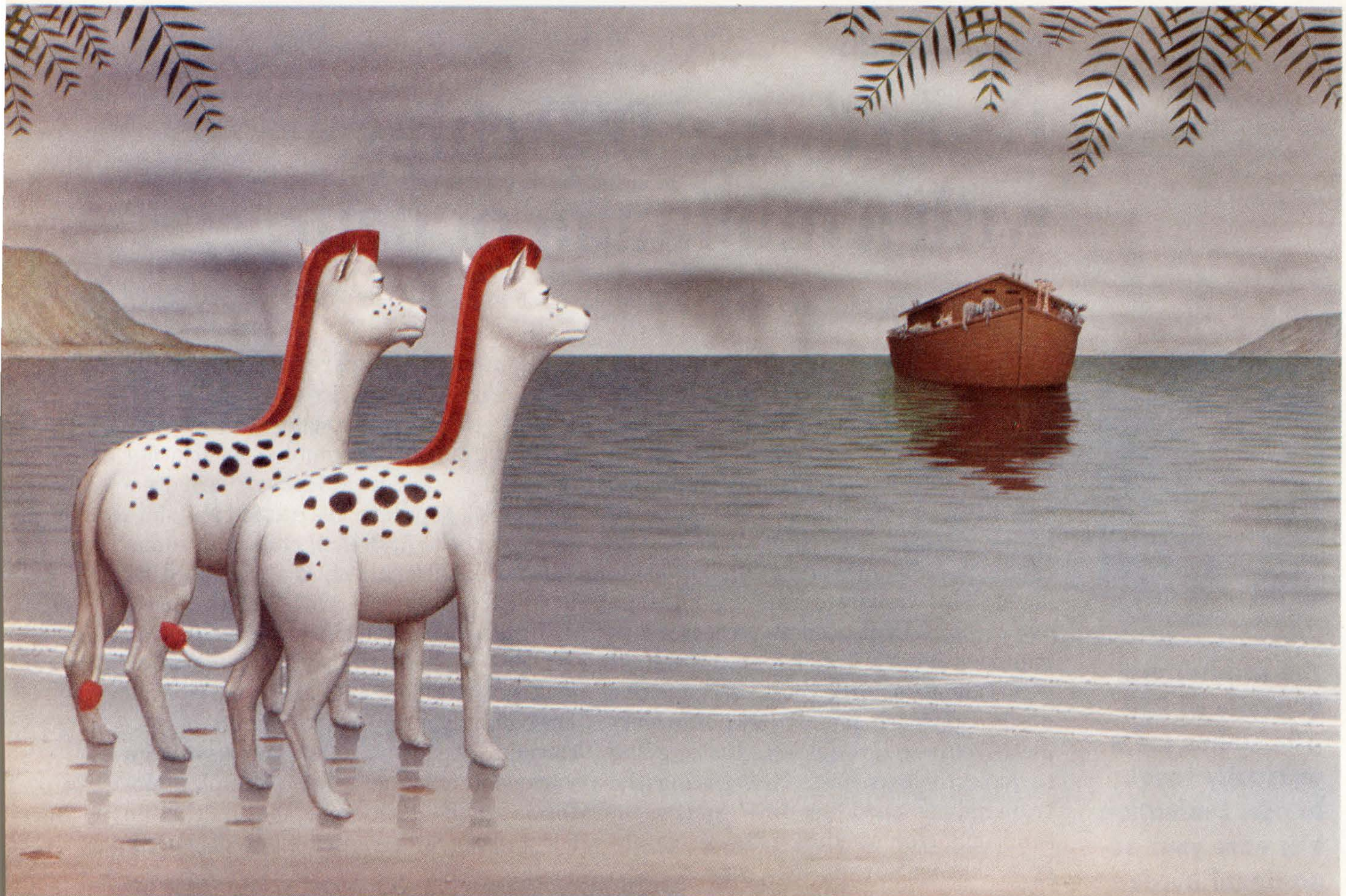
These DSP-chip evaluation kits bundle a DSP board with appropriate software. Most of these kits include a board with a processor chip, some memory, and an assembler. Some also include high-resolution ADCs and DACs, C compilers, debuggers, signal-processing libraries, and DSP operating systems. The differences in kit features and prices indicates that some DSP-chip vendors recognize the need to provide early educational support if they want to get their chips designed into products. Other vendors haven't yet figured this out. Educational help, which plays a large role in determining ease of use, may well be the deciding factor when you pick a DSP chip.

Diverse DSP-chip architectures really make direct comparisons difficult. Although they had varying word sizes, early DSP chips resembled each other externally; most used Harvard architectures with separate instruction and data spaces. These first DSP chips had somewhat conventional ALUs augmented by hardware accelerators such as barrel shifters and fast multiplier/accumulators.

DSP chips in the latest generation look nothing like the early parts, and DSP-chip vendors have made breakthrough performance advances through various techniques. For example, Motorola's 68HC16 merges the instruction set and register complement of a DSP

Kits of evaluation boards and software help you learn DSP-chip technology quickly. (Photo courtesy Texas Instruments)

Opportunity Lost



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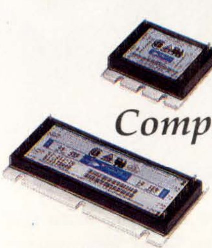

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CIRCLE NO. 40

DSP EVALUATION KITS

chip and a 16-bit enhanced version of its 68HC11 microcontroller (μC). AT&T Microelectronics' ATT93C010 and Zilog's Z86C95 and Z89C66 processors meld conventional μC cores—an 80C31 and a Z8, respectively—with a DSP processor. Unlike the 68HC16, the μC and the DSP processor run in tandem on these chips. Texas Instruments' TMS320C40 DSP chip has six bidirectional parallel ports coupled to DMA controllers, and is expressly designed for complex signal-processing arrays. Star Semiconductor's SPROC-1000 DSP-chip family incorporates as many as four digital-signal processors on one chip, giving you a range of software-compatible choices in terms of both price and performance.

Learning to use any one of these DSP chips will not help you much with the others. Hence the need for evaluation kits. Because of the available architectural diversity, you'll probably want to experiment with several DSP chips, but you won't want to design a new board for each one. DSP-chip evaluation kits put operational boards in your hands so that you can spend time learning to *use* the processors instead of wasting time on a balky prototype board. In general, these kits also include most or all of the software you need to start programming.

Targeting specific applications

Some of the evaluation kits listed in **Table 1** use DSP chips that are targeted at specific applications. For example, AT&T Microelectronics' ATT93C010 DSP chip is designed for hard-disk applications and Zilog's Z89C66 was created for modems. Although these intended applications shouldn't limit your own creativity in applying these DSP chips, the associated evaluation kits reflect the IC designers' intent. Two of the evaluation kits—the AT&T Microelectronics' MP3210 and Texas Instruments' Multimedia Developers Toolkit—use nonapplication-specific DSP chips, but the evaluation kits are specifically targeted at multimedia applications. The AT&T and TI kits are also available from board vendors, respectively Ariel Corp and Atlanta Signal Processors.

Table 1 lists a number of DSP-

Table 1—Representative DSP evaluation and development kits

Manufacturer	Evaluation kit	Price	DSP chip	Included software
Analog Devices	EZ-Kit	$499	ADSP-2101	C compiler, simulator, and demo programs for DTMF, FFT, filter, speech processing, graphics, and music applications.
Array Microsystems	a66550/8K	$9900	a66111	Control software, code generator, and an assembler.
AT&T Microelectronics	ATT93C010EK	$2499	ATT93C010[1]	Two assemblers (microcontroller and DSP chip), sample disk-servo and head-actuator code.
	MP3210	$4995	Two DSP3210[2]	C host drivers, demos, and utilities. An optional Multimedia software package with a C compiler, simulator, and applications library costs $3000.
GEC Plessy	FFT Processor Evaluation System	$5380	PDSP16510	Graphics-based software control program, C-routine library.
Motorola	DSP56156 Application Development System	$3000	DSP56001	Assembler, linker, and simulator cost $495 for a PC or Apple Macintosh; $5500 for Sun3 workstations.
	M68HC16Z1EVB	$375	68HC16Z1	Control software, macro assembler, filter-design package, real-time kernel, floating-point routines, and a C compiler demo.
SGS-Thomson	ST1893X HDS	$10,000	ST18932	Macro assembler, emulation-control software.
Star Semiconductor	SPROClab Development System	$8950	SPROC-1400	Block-diagram editor and compiler, signal-processing and filter-design libraries, loader, and a debugger.
Texas Instruments	Multimedia Developer's Toolkit	$5000	TMS320C31[3]	C compiler; debugger; and algorithms for image and speech compression/decompression, music functions, and fax.
	TMS320C1XEVM	$795	TMS320C16	Assembler, linker, and demo software.
	TMS320C2XEVM	$995	TMS320C26	Assembler, linker, and demo software.
	TMS320C3XEVM	$995	TMS320C30[4]	Assembler, linker, and demo software.
	TMS320C5XEVM	$995	TMS320C50	Assembler, linker, and demo software.
Zilog	Z86C9500ZC0 Evaluation Kit	$200	Z86C95[1]	Sample assembly-language routines; assembler available from third-party vendors.
	Z89C66 V.22bis Modem Kit	$200	Z89C65 or Z89C66[1]	2400-bps modem or speech-compression firmware.

Notes:
1. This procesor contains both a general-purpose microcontroller and a DSP chip.
2. Also available from Ariel Corp.
3. Evaluation board also works with TMS320C31 and TMS320C40 DSP chips.
4. Also available from Atlanta Signal Processors Inc.

chip evaluation kits available from the DSP semiconductor vendors with prices ranging from $200 to $10,000. Each kit includes a board with the DSP chip and some software. Almost all of the software provided runs on DOS-based PCs. (**Table 1** notes the exceptions.)

Although the prices somewhat reflect the number and the complexity of the components in the kit, they also reflect the DSP chip vendors' eagerness to win your design. Some semiconductor vendors are obviously willing to lose money on an evaluation kit with the expectation of recouping that investment over the long haul. Here are overview summaries of the kits listed in **Table 1**:

Analog Devices' EZ-Kit

Analog Devices offers a very complete DSP μP evaluation kit at a very aggressive price. The kit includes the company's EZ-Lab board with an ADSP-2101 DSP chip running at 12.288 MHz, an 8-bit codec, and four 8-bit DACs. You store your code on the board's 64-kbyte EPROM. The ADSP-2101 has 2k words of 24-bit program RAM and 1k word of 16-bit data RAM on the chip. The kit's software includes an assembler, a linker, and a software simulator.

Besides these components, the company also includes two introductory DSP texts: **Digital Signal Processing Applications Using the ADSP-2100 Family** with a diskette of source code and the workbook, **Digital Signal Processing Laboratory Using the ADSP-2101 Microcomputer** that contains some introductory experiments.

Array Microsystems' a66550/8K

The Array Microsystems a66111 DSP μP has only 16 instructions, including a single-instruction FFT. Consequently, the chip doesn't need much support software. The a66550/8K frequency-domain array-processor board for 16-bit ISA bus PCs uses a 25-MHz a66111 with its companion, the a66211 memory controller IC, and enough fast RAM to compute 8k-point complex or 16k-point real FFTs. A 1k-point real FFT takes 125.9 μsec and a 1k-point complex FFT takes 209.9 μsec. The included ArraysoFFT software package consists of an assembler, a code generator, a disassembler, and a control program for the board.

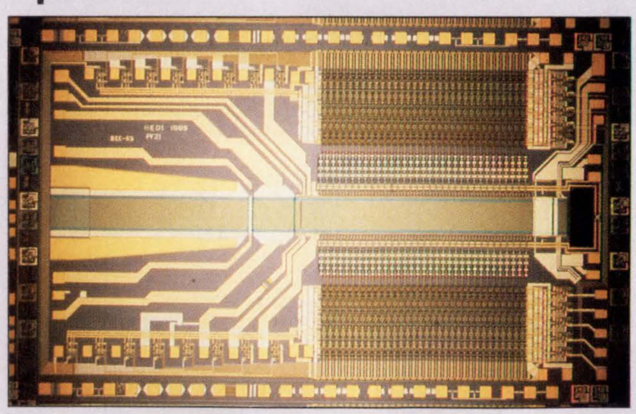
AT&T's ATT93C010EK

This evaluation kit includes the company's 93C020 Reach2 read-channel and 91C611 Spin1 servo processor ICs in addition to the 93C010 multiprocessor DSP chip. These chips comprise a chip set for controlling hard-disk drives. The board includes a prototyping area for drive-specific electronics, and the software includes routines for

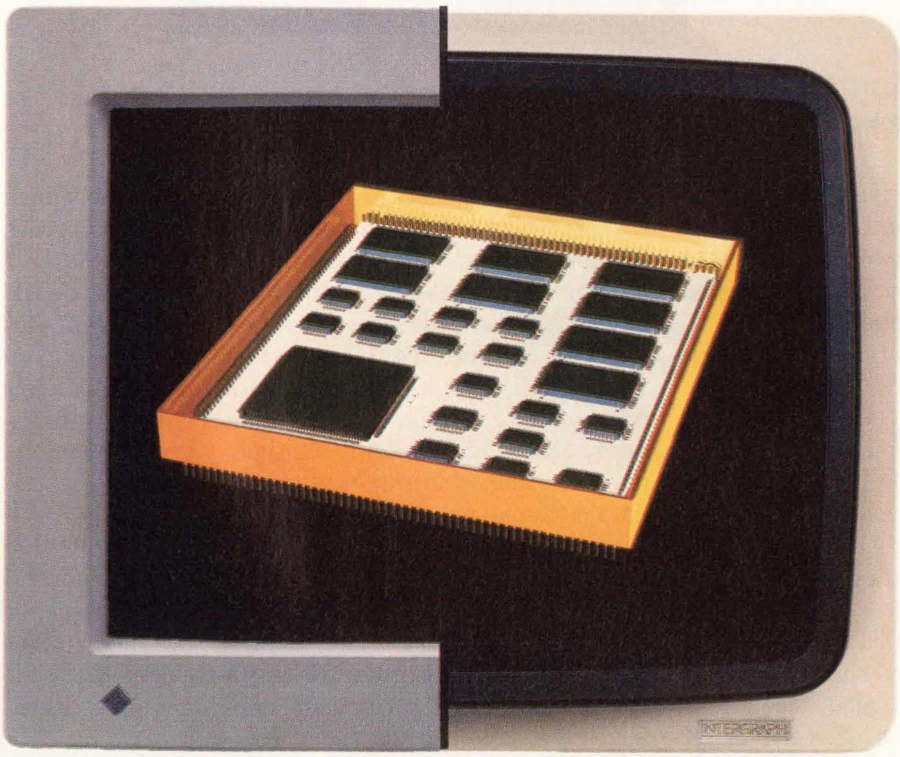
Dropping the digital makes a fast signal processor

In simpler times, analog and digital signal-processing techniques were clearly different. Digital signal processors used sampling and analog processing didn't. Acoustic-charge-transport (ACT) technology, almost ready to go commercial, blurs that distinction. ACT devices do sample signals, but they do not digitize them. The samples are electron packets with a charge that's proportional to the sampled signal voltage. These electron packets travel down the surface of the GaAs ACT chip so that the time-sampled signals become spatially spread. Electrodes deposited on the ACT device's surface detect these packets and convert the charge back into voltage without causing charge loss. A summing amplifier combines the electrode voltages through an array of programmable attenuators. The net result is a convolution or transversal filter.

ACT devices developed under military contracts over the past decade operate at sample rates measured in hundreds or thousands of MHz. You can't yet purchase commercial ACT chips, but you will be able to buy them later this year. Meanwhile, you can obtain an evaluation kit called the PTF (programmable-transversal-filter) Development Station with a prototype 128-tap, 360-Msamples/sec ACT device and associated software for $8500 from Comlinear Corp (Fort Collins, CO, (303) 225-7435, FAX (303) 226-0564).



Surface acoustic waves carry electron-packet samples down the center of this GaAs ACT (acoustic-charge-transport) device where evenly spaced electrodes sense the packets and convert the charge into voltages. A summing amplifier combines the electrode voltages, thus creating a sampling (but not digitized) convolution filter that operates at 360 MHz with 8-bit equivalent accuracy.



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DSP EVALUATION KITS

controlling the drive's head actuator and spindle motor. Because the 93C010 merges two processors, a 30-MHz 80C31 and a digital signal processor, you need two assemblers. The evaluation kit includes both.

AT&T's MP3210

Ariel Corp actually designed the MP3210 evaluation board, but you can buy it from either Ariel or AT&T. The card plugs into a 16-bit ISA bus and it incorporates one or two of AT&T's DSP3210 floating-point DSP chips running at 55 MHz. The board also accepts as much as 2 Mbytes of static RAM (SRAM) and 64 Mbytes of dynamic RAM (DRAM). It has two 16-bit ADCs and two 16-bit DACs with maximum sample rates of 50 kHz.

AT&T also offers a $3000 VCOS (visible caching operating system) multimedia development environment, which includes the company's VCOS real-time operating system for the DSP3210; a C compiler with an assembler, a linker, and a simulator; Microsoft Windows' multimedia extension drivers for fax and data modems, image and audio compression/decompression, and speech coding; and a DSP algorithm library.

GEC Plessy's PDSP16510

It's specialized, but GEC Plessy's PDSP16510 FFT processor performs 64-, 256-, or 1024-point complex FFTs on continuous 20-MHz data streams. The evaluation system uses the FFT-processor IC with the company's PDSP16330 Pythagoras processor and PDSP16540 bucket buffer ICs. The board also includes 20-MHz, 8-bit ADCs and DACs. Software bundled with the kit lets you control the board's operation. The software also includes a library of C routines that programs running on the host PC use.

Motorola's 56156 Application Development System

Motorola's 56156 development system uses a DSP56001 DSP μP running at 20.48 MHz. It also includes 8k 24-bit words of RAM and a debug ROM. The debug ROM gives you the traditional μP debugging commands and a 1-line assembler. For additional software abilities, you'll need the company's DSP56100CLAS assembler, linker, and simulator package. (See **Table 1** for software prices.)

The DSP56001 processor has serial channels that interface to analog converters. There are no such converters on the evaluation board, but the company offers a companion board with ADCs and DACs.

Motorola's M68HC16Z1EVB

Practically an entire evaluation board on a chip, the 68HC16 merges DSP registers and instructions into a 16-bit expanded version of the 68HC11 μC. The μC runs internally on a 16.78-MHz clock, which it synthesizes from a 32,768-Hz watch crystal. Also on chip are an 8-channel ADC with a programmable resolution of 8 or 10 bits (you can choose higher speed or resolution), 1 kbyte of RAM, a complex timer section, and the usual assortment of μC peripheral functions. Consequently, the evaluation board needs little more than the DSP μP and 64 kbytes of RAM. There's also a socket for an optional DAC. One very nice feature of the board is its built-in logic analyzer interface via seven connectors.

The evaluation kit also includes

For more information . . .

For more information on the DSP μP evaluation kits discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you read about their products in EDN.

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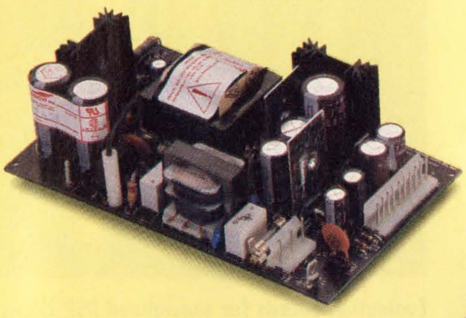

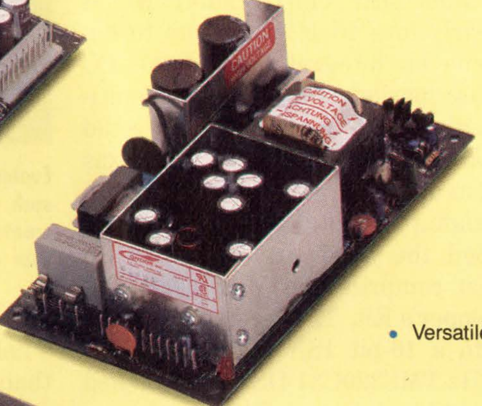

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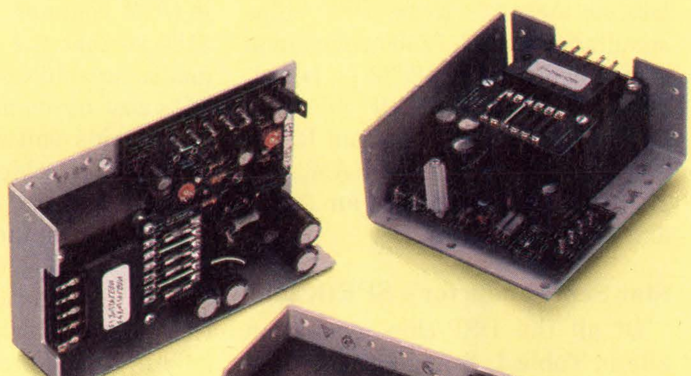

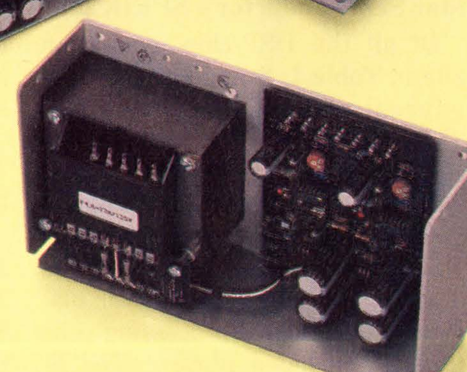

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CIRCLE NO. 42

a huge amount of software including a macro assembler, a debugger, the MCX-16 real-time kernel from A T Barret Associates (Houston, TX, (713) 728-9688, FAX (713) 728-1049), Gofast floating-point routines from US Software (Portland, OR, (503) 641-8446, FAX (503) 644-2413), a filter-design and -analysis package from Momentum Data Systems (Costa Mesa, CA, (714) 557-6884), and a demo C compiler and source-level debugger from Intermetrics Microsystems Software (Cambridge, MA, (617) 661-0072, FAX (617) 868-2843).

SGS-Thomson's ST1893X HDS

The ST1893X HDS is actually a development system instead of an evaluation kit. It includes a macro assembler, a linker, a debugger, and a library of macros and basic DSP routines. The system can emulate as many as three DSP chips simultaneously. A $2500 companion card, called the ST18932 pc board, couples the ST18932 DSP chip with 32k words of 32-bit program RAM, 8k words of 16-bit data RAM, two 2k-word FIFO buffers, an ADC, and a DAC.

Star Semiconductor's SPROClab

Of all the DSP-chip evaluation kits in **Table 1**, Star's has the most unusual set of features. The SPROC-1000 family of DSP ICs incorporate one to four processors on each chip. Instead of programming the company's multiple-processor DSP chips with assembly language or C, you draw functional block diagrams using signal-processing cells from an included library. The library presently contains more than 50 functional building blocks including amplifiers, multipliers, PLLs, filters, detectors, and arithmetic functions.

A block-diagram compiler converts the block diagrams into code that runs on any of the SPROC DSP chips. Programs just run proportionately faster on the chips with multiple processors. The SPROClab also includes a filter-design package for creating IIR and FIR filters.

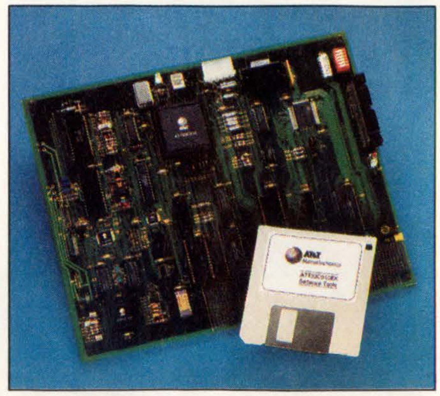
Texas Instruments' Multimedia Developer's Toolkit

Most DSP chip vendors would dearly love their processors to become an integral part of the PC mass market, and they view multimedia as the application that could make that wish come true. Texas Instruments, in conjunction with Atlanta Signal Processors, developed the hardware and software that comprise the Multimedia Developer's Kit. The card, which plugs into a 16-bit ISA bus, uses a 33-MHz TMS320C31 DSP chip coupled to 16-bit A/D and D/A converters, 1 Mbyte of RAM, and a telephone-line interface. The key criterion for this design was that the part cost, in OEM volumes, was not to exceed $125 so that the addition of multimedia capabilities would increase a PC's cost by no more than $500.

The kit's software consists of a C compiler; a high-level debugger; and object code for 16 multimedia functions, including six speech-compression/decompression algorithms, six music-processing algorithms, three fax algorithms, and an image-compression/decompression algorithm.

Texas Instruments' TMS320 Series Evaluation Modules

TI recently revamped its line of DSP-chip evaluation kits for what is undoubtedly the broadest line of DSP chips in the industry. The company's processor family includes the TMS320C1x and TMS320C2x fixed-point DSP processor series, the TMS320C3x floating-point DSP processor series, the TMS320C4x series of floating-point DSP chips designed for parallel-processing applications, and the TMS320C5x series of enhanced-performance fixed-point DSP μPs. The new evaluation kits provide a board, an assembler, a linker, and demo software for less than $1000.



Evaluation boards for specialized DSP chips, such as the AT&T Microelectronics 93C010 created for hard-disk applications, give your embedded design a real head start.

Zilog's Z86C9500ZC0

Zilog's 20-MHz Z86C95 processor teams a Z8 8-bit μC core with a 16-bit slave DSP processor on one chip. Also on the chip are 8-bit A/D and D/A converters, a pulse-width modulator, and several other μC-style peripheral functions. The Z86C95ZC0 applications board adds an 8-kbyte EPROM containing a monitor program, 32 kbytes of RAM, sockets for external A/D and D/A converters, and 12 LEDs. The company includes a disk with sample source code but the kit does *not* include an assembler. You must purchase that separately.

Zilog's Z89C66 V.22bis Kit

This evaluation kit doubles as a 2400-bps full-duplex modem. It uses a Z89C66 mixed-signal processor, which combines a Z8 processor core with a DSP slave processor. The firmware included on the board emulates the Hayes AT modem command set. EDN

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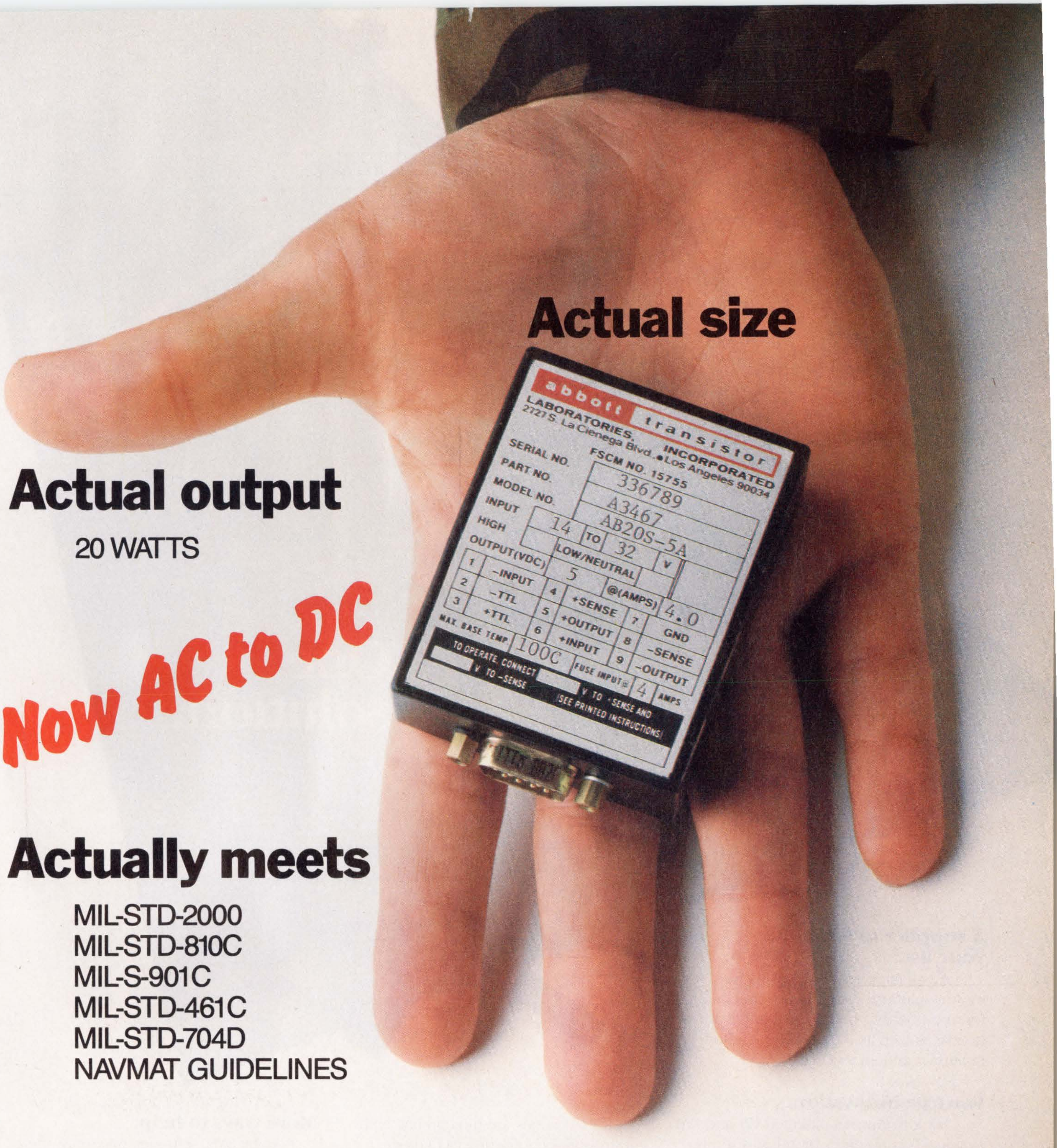

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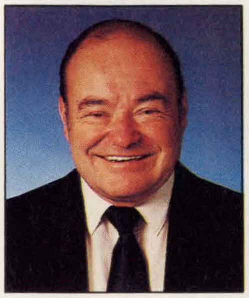
CIRCLE NO. 46

Gaining network interoperability requires more testing

JOHN GALLANT, Technical Editor



The proliferation of network standards and protocols has necessitated tests for your systems that extend beyond conformance testing. Interoperability tests are necessary to kill the bugs in recently authored specifications.

Interoperability is one of those peculiar buzz-words that has entered the engineering lexicon in the past few years. The word is particularly prevalent in local- and wide-area network (LANs and WANs) verbiage. Multivendor consortiums are constantly forming to guarantee that the vendors' products interoperate or that their products pass interoperability tests performed by an independent agency.

Interoperability in networking means that products from different vendors that conform to the same network standards can exchange meaningful data. You'd think that if every vendor followed the same procedures defined in the standard, their products would interoperate, right? Wrong. Often then standards' conformance does not guarantee communications.

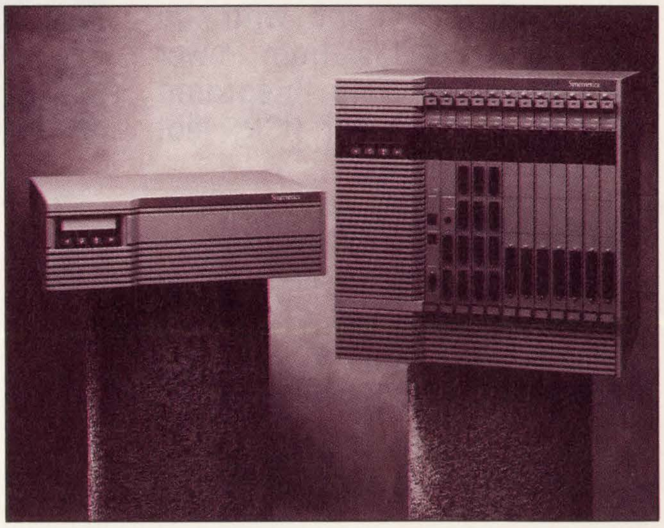
One reason standards don't truly interoperate is the way they are written. Typically standards tell you *what* you must do to conform, but don't specify *how* you must implement those conformities. For example, the ANSI X3T9.5 standard for the Fiber Distributed Data Interface (FDDI) specifies that nodes must be capable of handling 100-Mbps data. Although the standard recommends using multimode fiber-optic cable to achieve these data rates, any size cable capable of 1300-nm transmission conforms to the FDDI standard. The only criteria is that the cable meets optical power, channel bandwidth, and distance requirements.

Imprecision in the writing of the standards can lead to interoperability problems, too. Writing a standard is somewhat analogous to writing a constitution for a new nation. Because members of a standard's body often have conflicting interests, inconsistent options can often be included in the specifications. No matter how hard the framers try, it's nearly impossible to anticipate all contingencies. Essentially, interoperability tests provide a proving ground to iron out the wrinkles in the new standard.

Two network flavors

Networking standards fall into two categories: proprietary or open. Practically anything can become a standard if enough people want to use it.

Proprietary standards are sometimes called de facto, or unofficial, standards. Because one company controls the standard, you can have confidence that all of the company's products will interop-



There are endless variations to internetworking products. Synernetics calls its LANplex 5000 a multiplexer, which filters and translates packets from as many as eight Ethernet segments into FDDI packets at the MAC sublayer level.

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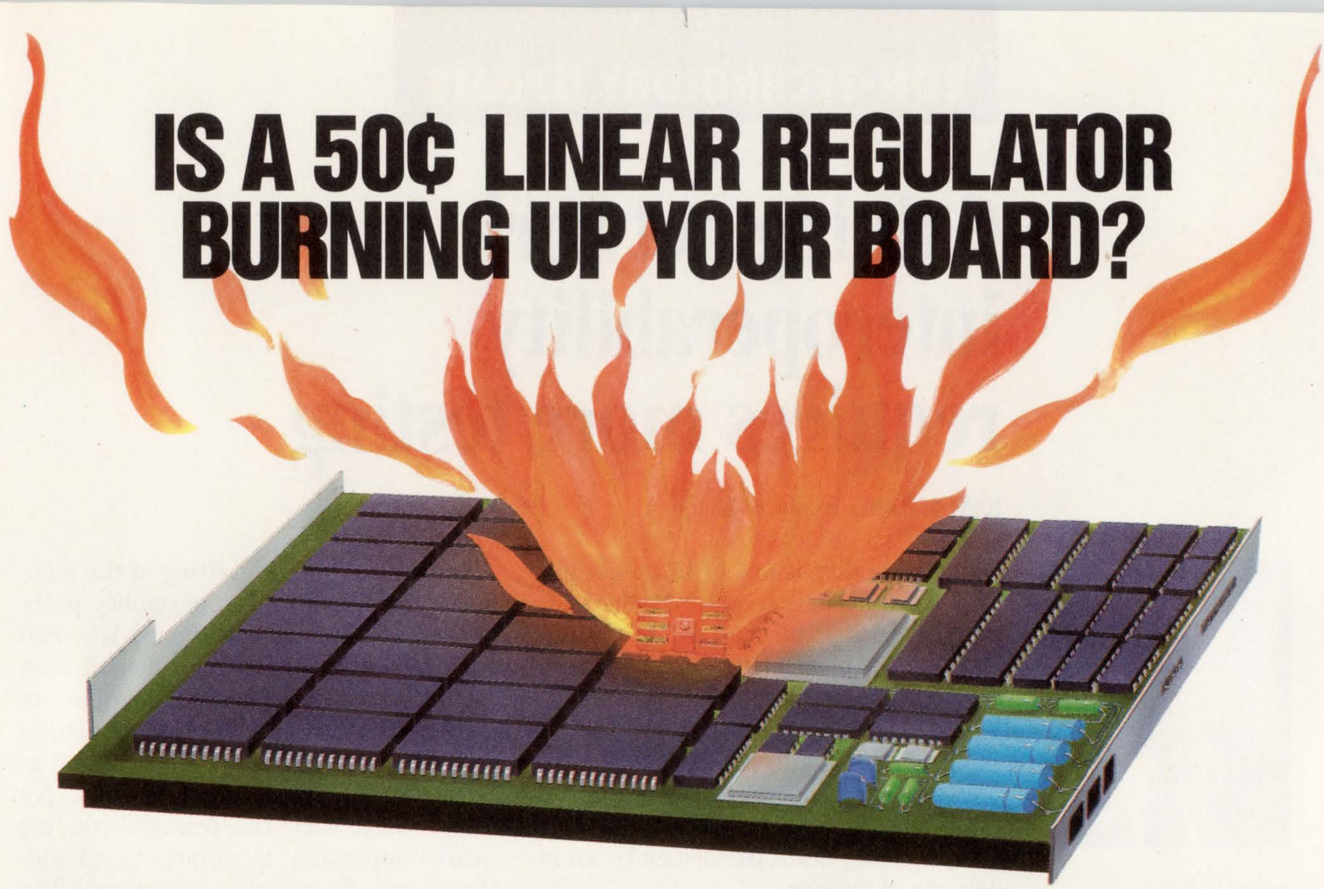

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erate. However, proprietary standards are susceptible to changes to promote the company's advantage. Therefore organizations, such as the IEEE, ISO, CCITT, and ANSI have developed all sorts of open standards, known as de jure, or official, standards.

Because open standards are not controlled by one company, they represent a consensus of industry opinions. They are preferable to proprietary standards, but often require a long development cycle before products from different vendors interoperate. Most of the wrinkles for mature open standards, such as Ethernet, Token Ring, and Token Bus, have been ironed out. However, products for the more recent FDDI standard and the 10Base-T specification for twisted-pair Ethernet communications are still undergoing considerable interoperability testing.

Interoperability issues get more complicated when computers on

The OSI Model

In 1977 the International Standards Organization (ISO) published a reference model for the operations that must take place so that computers can communicate on a network. The model, known as the Open Systems Interconnection (OSI) model, is an open standard that all vendors use when defining internetworking activities. The model partitions network operations into seven hierarchical layers, ranging from the hardware requirements for the physical signal at the bottom to the interactive computer display messages at the top (**Fig A**).

Each layer in the model makes use of the services provided by the layers below it. Within a product, each layer only communicates with the layer directly above or below it. Between products, a layer communicates with the identical layer for each product. For example, a router, which operates at the network layer, encapsulates data packets into the data fields of the data hierarchy. Essentially the model provides a division of labor for the tasks required. Each layer provides the following functions:

- Application Layer. Supplies utilities for computing applications or nodes on the network to let them communicate with other applications of nodes. File transfer and electronic mail operate at this layer.
- Presentation Layer. Controls the format of screens and files. Control codes, special graphics, and character sets operate at this layer.
- Session Layer. Responsible for binding and unbinding logical links between users. The layer manages and controls the dialogue between users.
- Transport Layer. Uses the services of the three lower layers to control the transmission of data from end to end on the network. The layer requests retransmission if the node receives garbled data and regulates the data flow so that a faster computer doesn't overflow a slower computer with data.
- Network Layer. Routes data across the network. The layer is not concerned with the destination of the data, but only with its point-to-point progress over the network. If a node on a path goes down, the layer is responsible for determining another path.
- Data Link Layer. Controls access to the physical medium. The layer assembles messages into packets and coordinates their flow over the network. The layer also performs error detection and correction. The IEEE version divides the layer into two sublayers—the Medium Access Control (MAC) and Logical Link Control (LLC) layer. The MAC layer controls the actual physical medium, and the LLC layer controls logical connections.
- Physical Layer. Specifies the type of medium for the network, such as coaxial, fiber optics, or twisted pair. The layer also defines the network's operating specifications, such as signal levels, bit-error rate, and maximum distance between nodes.

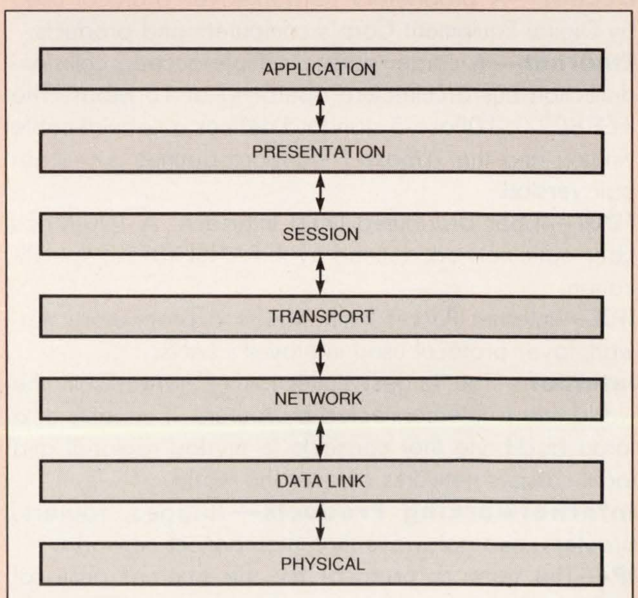


Fig A—The OSI model consists of seven hierarchical layers that vendors use to exchange data between computers on a network.

heterogeneous LANs must communicate. The goal of networking is to let computers running on Apple Talk, SNA, DECnet, Novell's IPX, or any network you can think of, communicate seamlessly. To achieve this goal, software and hardware vendors for internetworking products use the Open Systems Interconnection (OSI) model.

OSI organizes the activities that must take place into seven hierarchical layers (see **box**, "The OSI Model"). Because the upper layers make use of the functions performed at the lower layers, the interoperability problem grows exponentially as you proceed up the ladder from the physical to the application layer. To illustrate this magnification effect, consider the different issues that bridge vendors must address versus the issues router vendors must address to achieve interoperability.

Bridges relay information at the data-link layer and are independent of upper-layer protocols. They implement the physical layer and Medium Access Control (MAC) sublayer in hardware—usually an add-in board for an extension bus. The Logical Link Control (LLC) sublayer is usually in firmware. The bridge can operate as a repeater to increase the length of a LAN, or it can segment large LANs into subnets to minimize traffic congestion.

Either righties or lefties

A bridge only works on a LAN that uses the same access methods, such as Ethernet, which uses a carrier-sense, multiple-access, collision-detection (CSMA/CD) access method, or Token Ring, which passes a token for access. However, the bridge can connect LANs of different media types, such as coaxial or shielded and unshielded twisted pairs. A bridge monitors all traffic and communicates by using either source routing or transparent bridging, or by using the Spanning Tree Algorithm (see **box**, "Glossary of networking terms").

The major advantage of bridges is that they are independent of communications protocols for the transport and network layer. The bridge simply forwards packets for upper-layer protocols, such as OSI, TCP/IP, (transmission-control protocol/internet protocol) DECnet, or Apple Talk. In addition, bridges can forward or filter packets based on source or destination addresses and size.

Bridges are simpler and less expensive devices than routers. However, multivendor bridges must prove that they interoperate when using new network standards such as FDDI. Both the Interoperability

Text continued on pg 62

Glossary of networking terms

Apple Talk—Apple Computer's proprietary network.

DECnet—A proprietary network-layer protocol used by Digital Equipment Corp's computers and products.

Ethernet—A carrier-sense, multiple-access, collision-detection bus architecture operating at 10 Mbps. The IEEE 802.3, 10Base-5 standard defines a coaxial-cable version and the 10Base-T standard defines a twisted-pair version.

FDDI—Fiber Distributed Data Interface. A 100-Mbps fiber-optic network defined by the ANSI X3T9.5 specification.

IPX—Internet Packet Exchange is a proprietary network-layer protocol used in Novell's LANs.

Internet—The largest collection of networks in the world that is interconnected by routers. It consists of a large backbone that connects to myriad regional and local campus networks all over the world.

Internetworking Products—Bridges, routers, brouters, and gateways that interconnect networks.

IP—The network protocol for the Internet protocol suite.

Local Talk—A 230-kbps carrier-sense, multiple-access, collision-detection scheme defined by the data link and physical layer for Apple Computer's LANs.

PPP—Point-to-Point protocol. An Internet protocol used to route IP packets over serial links, such as a telephone line or an RS-232C line.

Protocol—A set of rules and conventions that govern an orderly exchange of information.

SNA—IBM's proprietary Systems Network Architecture.

Spanning Tree Algorithm—A bridging method that maintains a tree topology without loops for networks having redundant paths.

Source routing—An addressing scheme whereby the transmitting node learns and remembers the best route to a destination node.

Subnet—A portion of a network that is partitioned by a bridge or router.

TCP—Transmission control protocol. The major transport protocol in the Internet suite of protocols that provides reliable connection-orientated data.

Token Ring—A token-passing-ring architecture defined by the IEEE 802.5 specification.

Transparent bridging—Compares frame destination addresses on the network with an address table to determine whether to forward or ignore (filter) a message.

Table 1—Representative internetworking products*

Company	Model	Product type	Network type	Routing protocols	Data-link protocols	Network management	Price	Comments
Ascom Timeplex	Time/LAN	Brouter[1]	Ethernet, Token Ring, FDDI	TCP/IP, Xerox XNS, Novell IPX, OSPF	HDLC, Frame Relay (optional), IEEE 802.1, PPP	SNMP, SMT	$7995 to $26,800	Forwards 14,000 packets/sec. FDDI dual-homing mode. Source-routing transparent bridging.
Cisco Systems	IGS Routers	Brouter	Token Ring, Ethernet	TCP/IP, DECnet, IGRP,RIP, Novell IPX, Xerox XNS, OSI, RTMP, OSPF, SDLC Transport	HDLC, X.25, Frame Relay, PPP, SMDS	SNMP, Telnet, MOP	$4995 (local), $5495 (remote), $6995 (Token Ring)	Two Ethernet ports (IGS/local) One Ethernet and one synchronous serial port (IGS/remote) One Token Ring and one synchronous serial port (IGS/Token Ring)
	AGS+ Router	Brouter	Token Ring, Ethernet, FDDI	TCP/IP, DECnet, IGRP, RIP, Novell IPX, Xerox XNS, OSI, RTMP, OSPF, SDLC Transport	HDLC, X.25, Frame Relay, PPP, SMDS	SNMP, Telnet, MOP	$12,300	WAN interfaces for 9.6, 56, or 64 kbps, T1, E1, fractional T1, D53, and E3 communication rates. Forwards 14,800 Ethernet packets/sec. Forwards 10,000 Token Ring packets/sec.
	MGS Router	Router	Ethernet, Token Ring, Serial Interfaces	TCP/IP, DECnet, IGRP, RIP, Novell IPX, Xerox XNS, OSI, RTMP, OSPF, SDLC Transport	HDLC, X.25, Frame Relay, PPP, SMDS	SNMP, Telnet, MOP	$9275	Connects as many as 11 network and serial ports. Security for network access.
Computer Communications Inc	Interop/ 7010	Brouter	Ethernet, SNA	SDLC Transport, TCP/IP, ARP	HDLC	SNMP	From $10,000	Connects SNA LANs to TCP/IP WANs.
	Interop/ 7020	Router	Ethernet, SNA	SDLC Transport, TCP/IP, ARP	HDLC	SNMP	From $10,000	Connects multiple Ethernet LANs to an SNA backbone.
Digital Equipment Corp	WANrouter 250/500	Router	Ethernet	TCP/IP, DECnet, OSI, RTMP, Novell IPX, Integrated IS-IS, RIP	HDLC, X.25, IEEE 802.1, PPP, Frame Relay	NCL, DECmcc, CMIP	$4000 to $6500	One Ethernet port plus two 64-kbps or eight 19.2-kbps serial ports (model 250) One Ethernet port plus one T1/E1, two 384-kbps, three 256-kbps, or four 64-kbps serial ports (model 500).
	DECnis 500/600	Router	Ethernet, X.25 Gateway	TCP/IP, DECnet, OSI, RTMP, Novell IPX, Integrated IS-IS, RIP, OSPF, EGP	HDLC, X.25, IEEE 802.1, PPP, Frame Relay	NCL, DECmcc, SNMP, CMIP	$14,000 to $30,000	Rack-mount and seven slots (model 600). Table-top and two slots (model 500). Two Ethernet or four T1/E1 ports (model 500). Seven Ethernet or 14 T1/E1 ports (model 600). Hot-swap insertion cards.
Network Systems Corp	6000 Series	Brouter	FDDI, Ethernet	TCP/IP, DECnet, Novell IPX, RTMP, Xerox XNS	Frame Relay, PPP	SNMP, FDDI, MIB, SMT	$23,000 to $46,000	Forwards 15,000 Ethernet packets/sec. Dynamically learns packet addresses.

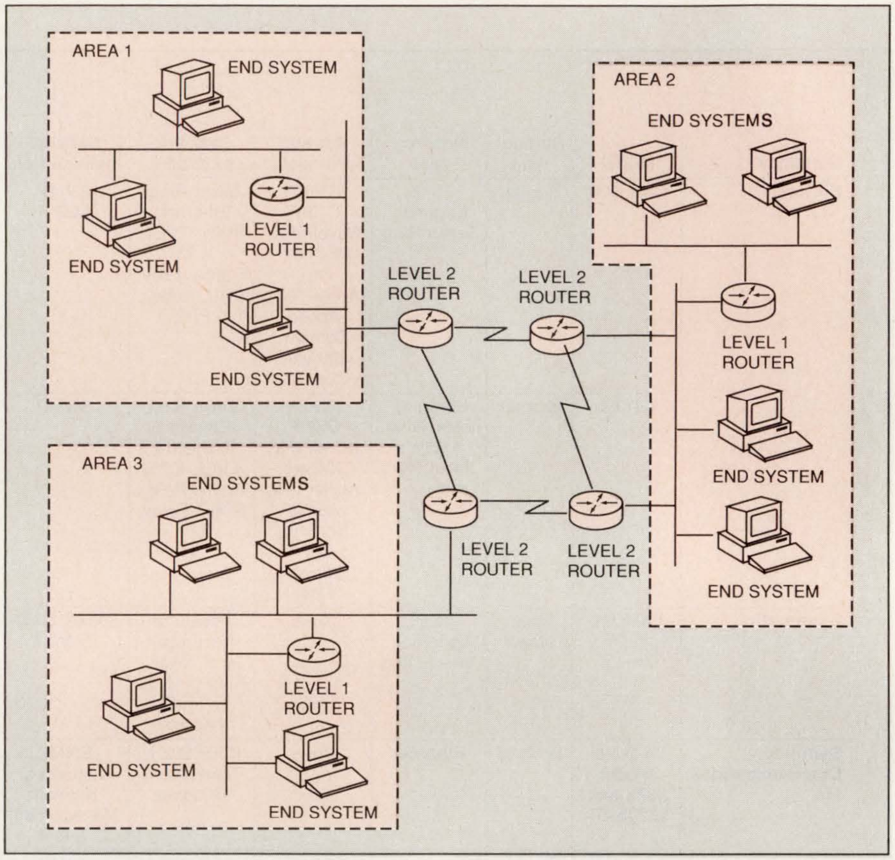
Company	Model	Product type	Network type	Routing protocols	Data-link protocols	Network management	Price	Comments
Proteon	CNX 500	Brouter	FDDI, Ethernet, Token Ring	TCP/IP, OSPF, Novell IPX, DECnet, OSI, Apple Talk, Apollo Domain, Banyan Vines, SNA	Token Ring, Ethernet, FDDI, T1/E1, X.25, Frame Relay, SDLC Relay, PPP	SNMP MIB II	$7995	Forward 25,000 packets/sec. Employs AMD's 29000 RISC CPU, which processes packet headers at 800 Mbps. Supports service routing, spanning-tree, and source-routing transparent bridging.
	p4100t	Brouter	Ethernet, Token Ring, Apollo's Token Ring	TCP/IP, OSPF, Novell IPX, DECnet, Apple Talk, Apollo Domain, OSI, Banyan Vines	Token Ring, Ethernet, ProNet-10, T1/E1, X.25, Frame Relay, SDLC Relay, PPP	SNMP	$5495	Supports IBM's source-route bridging. Interconnects Apollo Token Ring and Ethernet networks. Connects networks to a 16-Mbps Token Ring backbone.
Synernetics	LANplex 5000 family	Multi-plexer	FDDI, Ethernet, Token Ring	None	Translates Ethernet, and Token Ring packets to FDDI packets	SNMP, CMIP, SMT,	$32,900 LANplex 5012	Three FDDI, three Ethernet, and three Token-Ring paths connect to a VMEbus. Connects 24 Ethernet segments to an FDDI backbone. Hot-swap insertion cards.
Synoptics Communications Inc	LattisNet model 3323 and 3324S-ST	Bridges	Ethernet	None	IEEE 802.1, Transparent Bridging	SNMP, LattisNet, Network Management, Telnet	$4795 to $5295	Forwards 13,600 packets/sec. FOIRL port (model 3324S-ST). AUI port (model 3323S).
	LattisNet model 3383 and 3384-ST	Routers	Ethernet	TCP/IP, DECnet, Novell IPX, RTMP, IGRP, RIP, RTMP	IEEE 802.1	SNMP, LattisNet, Network Management, Telnet	$6395 to $6795	Transparently route DEC LAT protocols between LANs. Forwards 5000 packets/sec. FOIRL port (model 3384-ST) AUI port (model 3383).
Ungermann-Bass	Access/One ASM-6500	Bridge	Token Ring	IEEE 802.5	HDLC, IEEE 802.1	Network-Management Console, IEEE 802.5	$5250	Full-duplex synchronous T1 rates. IEEE 802.5 network management monitors data-link statistics.
	Access/One ASM-6300	Bridge	Ethernet	None	IEEE 802.1, HDLC	Network-Management Console	$4995	Full-duplex synchronous T1 rates. Forwards 2600 packets/sec. Provides load-sharing between bridges. Hot-swap insertion cards.
	Access/One ASM-5361	Brouter	FDDI, Ethernet	OSPF, RIP, Novell IPX, Xerox XNS, RTMP, DECnet, TCP/IP, ARP	IEEE 802.1, X.25, HDLC	SNMP, SMT, Network-Management Console	$19,995	Forwards 50,000 packets/sec. Routes as many as five protocols simultaneously. Dual-RISC processors.

Notes: 1. Brouter—A cross between a bridge and a router. See text for explanation.

*Acronyms used in this table:
Apple Talk—Apple Computer's proprietary network
ARP—Address Resolution Protocol
AUI—Attachment Unit Interface
CMIP—Common Management Information Protocol
DECnet—Digital Equipment Corp's proprietary network
DECmcc—Digital Management Control Center
EGP—Exterior Gateway Protocol
FDDI—Fiber Distributed Data Interface
FOIRL—Fiber-Optic Inter-Repeater Link
HDLC—High Level Data Link Control
IGP—Interior Gateway Protocol
IGRP—Interior Gateway Routing Protocol, Cisco Systems' proprietary routing protocol
Integrated IS-IS—Integrated Intermediate System-to-Intermediate System
IPX—Internet Packet exchange, Novell's proprietary routing protocol
MOP—Maintenance Operation Protocol
NCL—Network Control Language
OSI—Open Systems Interconnection
OSPF—Open Shortest Path First
PPP—Point-to-Point Protocol
RIP—Routing Information Protocol
RTMP—Routing Table Maintenance Protocol, Apple Talk's proprietary routing protocol
SDLC—Synchronous Data Link Control
SNA—Systems Network Architecture, IBM's proprietary network
SNMP—Simple Network Management Protocol
SMDS—Switched Multimegabit Data Service
SMT—Station Management, FDDI supervisory function
TCP/IP—Transport Control Protocol/Internet Protocol, open suite of protocols for the Internet network
XNS—Xerox Network Systems
X.25—CCITT recommendation for communicating in packet mode on public data networks

NETWORK INTEROPERABILITY

Lab of the University of New Hampshire (Durham, NH) and the Advanced Networking Test Center, which Advanced Micro Devices sponsors, have test centers that run a suite of interoperability tests on products connected to an FDDI network, including bridges and routers. Vendors form consortiums and supply products to these facilities to guarantee their products interoperate.

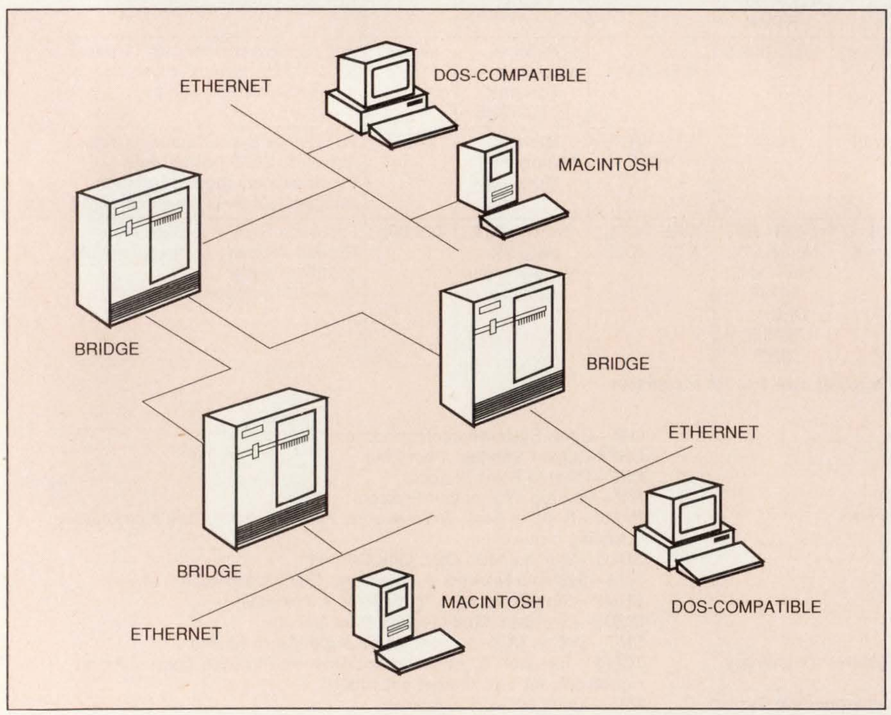


Routers operate at the network layer to transmit data between LAN clusters. The internetworking products use a variety of proprietary and open protocols to route the data.

Routers choose the best path

Routers operate at the network layer of the OSI model, and as such, use routing protocols for this layer to deliver packets from source to destination. Some popular suites of protocols for the network layer are TCP/IP, OSI, Novell's IPX, DECnet, and Apple Talk. The TCP/IP protocols and the OSI protocols are open standards and the others are proprietary standards.

The TCP/IP protocols were developed in the 1970s and, because of their maturity, require less interoperability testing. Some parts of the OSI protocol suite are still in draft form, however, and require considerable testing. The Corporation for Open Systems (COS) is a vendor of OSI protocols and supports user groups for conformance testing, certification, and promotion of OSI products. COS also underwrites OSI interoperability tests being performed at the OSInet Corp (McLean, VA) by placing a COS Mark stamp on all products that pass testing.



Bridges can extend the maximum LAN distance by acting as repeaters, or segment large LANs into smaller LANs to relieve traffic congestion. The tree topology guarantees that there aren't any loops in the network.

Routers can join heterogeneous networks such as FDDI, Ethernet, Apple Talk, and Token Ring. In addition, routers can determine the best subnet path to deliver a message and ensure the network can handle the traffic.

Because the data-link layer can have different formats to accommodate X.25, FDDI, Ethernet, Token Ring, or other networks, a router must handle different address

schemes, maximum frame lengths, and data rates. Routers overcome the maximum-frame-length problem by segmenting packets into smaller fragments. The router gives each fragment a sequence number and sends them as separate packets.

Two classes of routers

Routers forward traffic based on routing protocols. There are basically two classes of routing protocols. Interior gateway protocols (IGP) route traffic between networks that share a common network administrator, such as a corporate network. Exterior gateway protocols (EGP) route traffic between autonomous networks, such as a corporate network and a WAN.

Multivendor routers must interoperate using a variety of open and proprietary routing protocols. For example, the routing information protocol (RIP) is a widely used open-standard IGP protocol for the open TCP/IP packets. The Inter-Gateway Routing Protocol (IGRP) is a proprietary standard developed by Cisco Systems and is an enhanced version of RIP. The Open Shortest Path First (OSPF) is an open standard to replace RIP and IGRP for routing TCP/IP packets.

In addition, SNA, Novell's IPX, DECnet Phase IV, and Apple Talk have special routing protocols to propagate information on proprietary networks. In fact, router interoperability on serial links was not possible until the Internet community established the point-to-point protocol (PPP) for the data-link layer of TCP/IP. The PPP also has specifications for DECnet and OSI compliant networks.

The variety of protocols for the network-link layer makes interoperabilty for a router more complicated than for a bridge. Some routers implement multiple-routing protocols to serve specific open and proprietary networks. However, separate multiple-routing protocols increase overhead, bandwidth, and network-management resources. The Integrated Intermediate-Systems-to-Intermediate-Systems (IS-IS) open protocol integrates the activities of multiple-routing protocols into one routing protocol that can be shared.

The Integrated IS-IS routing protocol uses a link-state algorithm to transfer DECnet, TCP/IP, or OSI data packets. The algorithm determines the cost for a router to communicate with each of its neighbors and propagates data on the

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For more information on the internetworking products, standards committees, and testing sites discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you read about their products in EDN.

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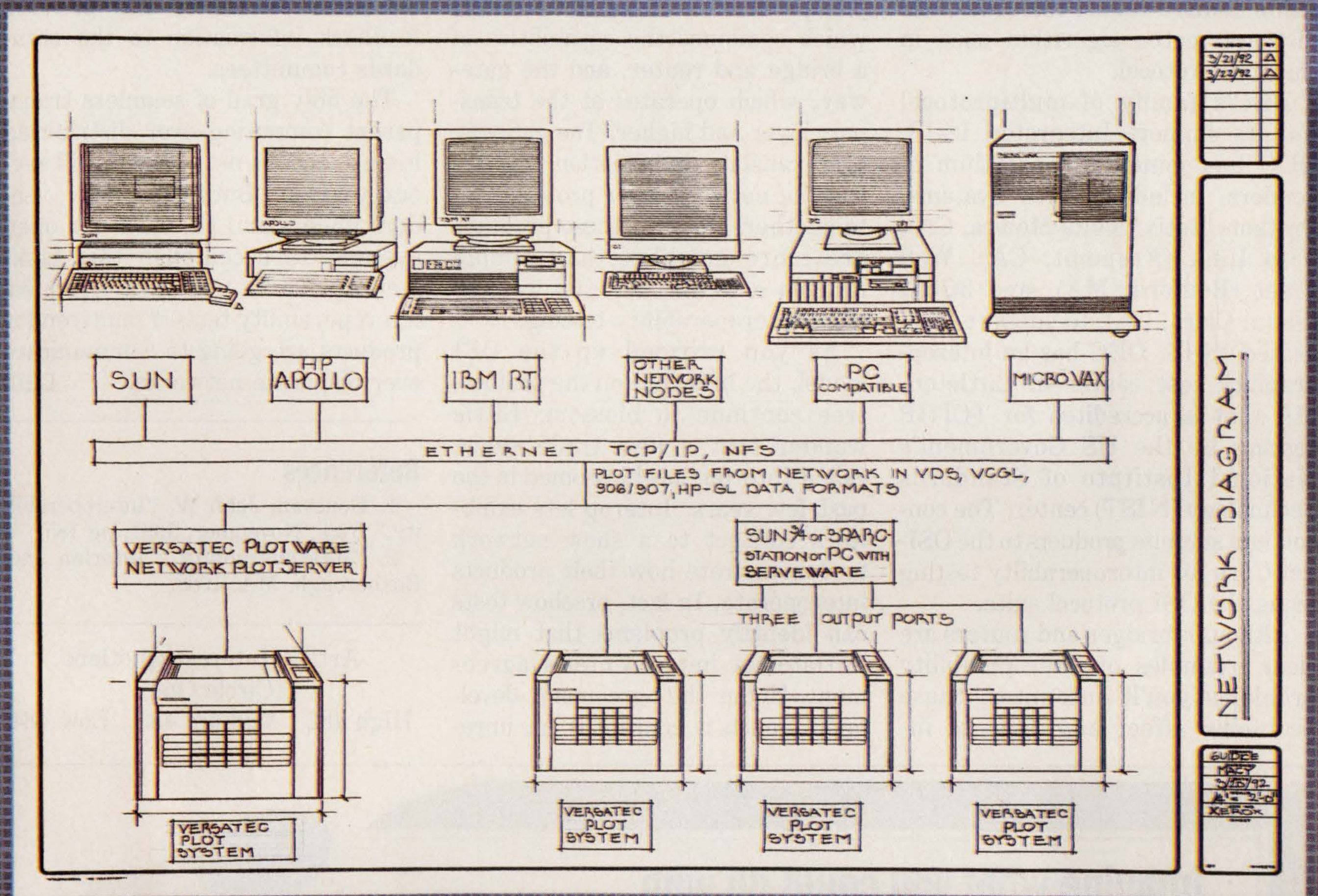
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most cost-effective path. The algorithm is more robust than the older distance-vector algorithm used in the RIP protocol.

DEC's family of multiprotocol routers support Integrated IS-IS. DEC has joined a consortium of vendors, including Cisco Systems, Proteon, Retix (Santa Monica, CA), Vita Link (Fremont, CA), Well Fleet (Bedford, MA), and 3COM (Santa Clara, CA), to support Integrated IS-IS. DEC has an interoperability test center in Littleton, MA that is accredited for TCP/IP testing by the US Government's National Institute of Standards Technology (NIST) center. The consortium submits products to the OSI-net Corp for interoperabilty testing using the OSI protocol suite.

Although bridges and routers are clear examples of interoperability problems you'll encounter, these problems affect any type of internetworking products. For example, products such as the brouter, which combines the capabilities of a bridge and router, and the gateway, which operates at the transport layer and higher. The gateway can translate information for one suite of network-layer protocols into another. Because these products are more complex than simple bridges and routers, they require more interoperability testing.

As you proceed up the OSI model, the branches on the protocol tree continue to blossom. Little wonder that a new trade show, called Interop, has blossomed in the past few years. Interop lets exhibitors connect to a show network to demonstrate how their products interoperate. In fact, preshow tests can identify problems that might initiate an implementer's agreement. Under the agreement, developers reach a consensus on unresolved issues to ensure future product interoperability and provide feedback information to the standards committees.

The holy grail of seamless transparent computing over distributed heterogeneous networks is still several years off. But increasingly, vendors understand the need for open systems to accomplish this task. New standards will always require interoperability tests if multivendor products are going to communicate over disparate networks. EDN

References

1. Donovan, John W, "Interoperability," *Byte*, November, 1991, pg 185.

2. "Interoperability," Interlan Inc, Boxborough, MA, 1988.

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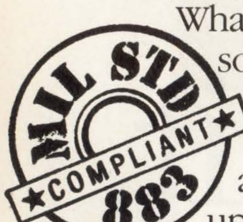

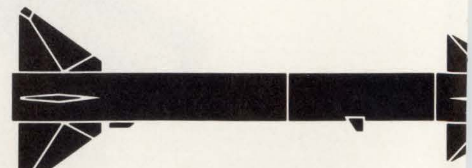

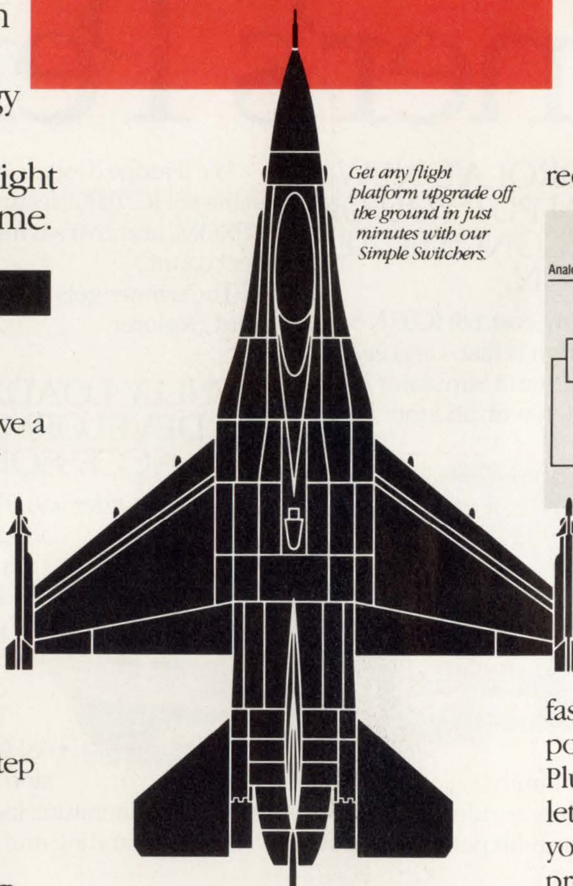

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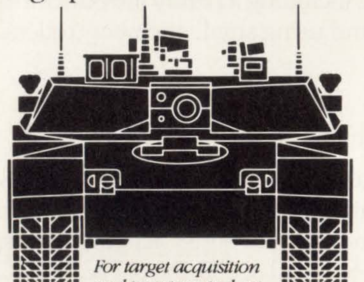

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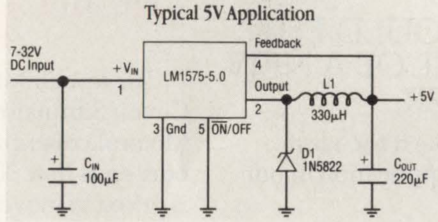

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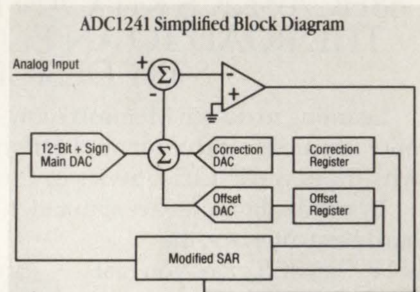

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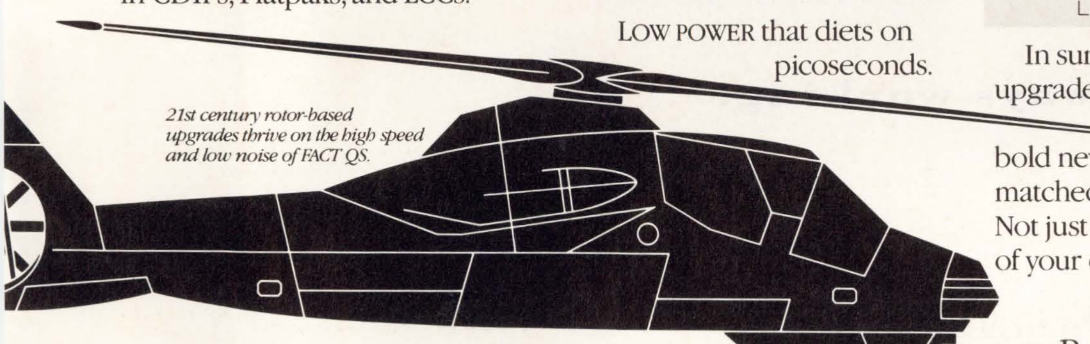

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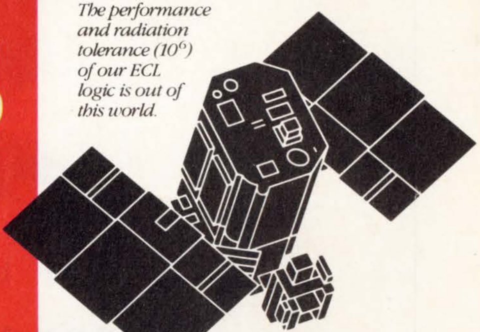

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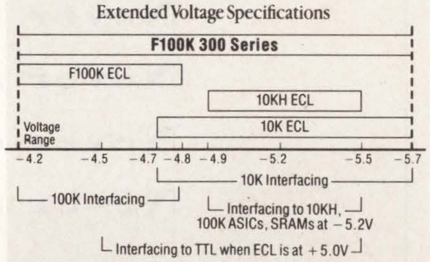

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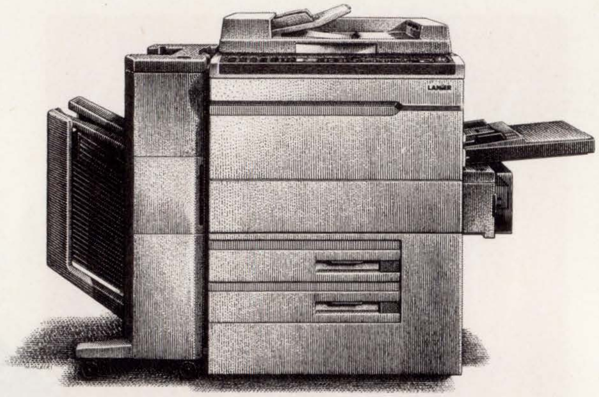

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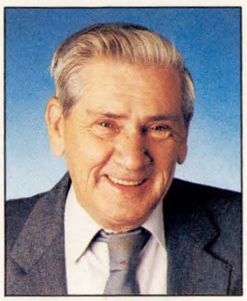
3V circuits cut power and boost speed

DAVE PRYCE, Technical Editor



Driven by manufacturers' need for higher speeds and lower power consumption, IC vendors now offer devices that can operate at supply voltages of 3.3V or less.

As equipment manufacturers strive to cram complex processors, denser memories, and high-capacity disk drives into workstations and high-performance desktop computers, the need to reduce power drain—and heat generation—has intensified. Manufacturers of laptop and notebook computers also need to minimize power consumption to extend the operating time between battery replacements or recharging intervals. Lowering the operating voltage is of great benefit to the system designer who has to cope with heat-dissipation or power-management problems. For example, most digital circuits consume less than 40% as much power operating at 3V than they do at 5V.

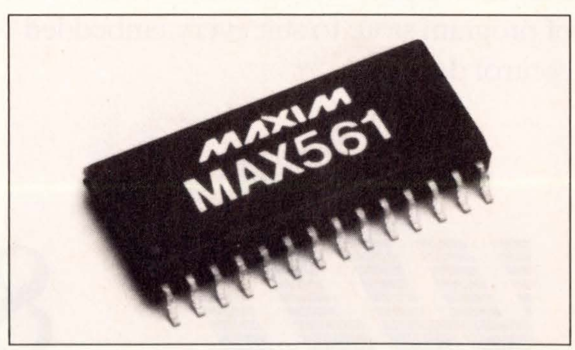
In response to equipment manufacturers' need for faster speeds, greater circuit density, and lower power consumption, increasing numbers of IC vendors are producing circuits that operate at low supply voltages. Advanced Micro Devices (AMD) inaugurated the 3V revolution about nine months ago when it announced a 3.3V version of the industry-standard 386 microprocessor. Operating at typically half the power of the 5V original, this 3.3V CPU found instant acceptance in battery-powered computers. Since then, the rush toward 3V devices has intensified to the point where dozens—if not hundreds—of circuits are available.

Complementing this trend, IC manufacturers are reducing chip geometries to ever smaller line widths and feature sizes. Lower voltages let IC designers pack more components on a chip and—because of less power dissipation—use inexpensive plastic packages instead of costly ceramic ones. Indeed, lower voltages are helping unlock the potential of submicron processing technologies, which result in chips that offer fast speeds but can't always operate reliably in 5V systems. The problem is the tendency of submicron chips to punch through or suffer damage when subjected to the stress of high voltages.

Voltage rating vs performance

Many high-density chips are specifically designed to operate at 3.3V. In other cases, IC vendors are characterizing existing 5V parts for operation at lower voltages. However, recharacterized parts can suffer from reduced performance. For example, recharacterized 5V DRAMs (dynamic RAMs) and SRAMs (static RAMs) typically drop one speed grade when operating at 3V. In a DRAM, this speed loss might represent a shift from 60 to 80 nsec; an SRAM might slow from 15 to 20 nsec.

Exactly how the rush toward 3V circuits will shake out in the long term is



This RS-232C transceiver from Maxim Integrated Products implements the new EIA/TIA-562 standard, which guarantees operation with output voltages as low as ±3.7V. The device can operate at voltages as low as 3.0V at a data rate of 20 kbps.

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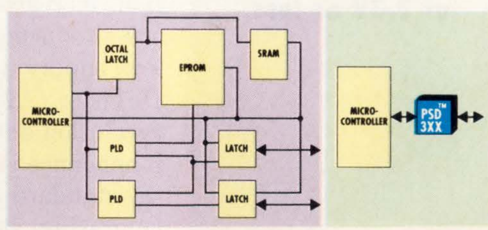

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a topic of much debate. At last February's International Solid-State Circuits Conference (ISSCC), panelists at the evening session, "The Evolution of a 3V Standard," agreed on the market-driven need for 3V devices, but disagreed as to how the progression from 5 to 3V would take place.

One panelist said that, at least initially, computer suppliers may just reduce the battery voltage and let 5V parts run at 3.3V. Despite the likely degradation in performance, this approach might be satisfactory for many applications. Although a JEDEC 3.3V standard that sets interface thresholds at the TTL level is in the works, another panelist said that the industry needs a 3.0V high-performance standard. Such a standard would set the switching threshold at midway between the rails. Someone else proposed a set of standards whereby the voltage would decrease with each new DRAM generation until it reached 0.9V. This scenario seems unlikely at less than about 2V, however.

Mixed-voltage considerations

Most panelists agreed that CPUs and memories are the enabling technologies and—for the immediate future—designers will have to develop systems with a mix of 3 and 5V components. According to Richard Quinnell, an EDN editor who attended the conference, the biggest concerns about this approach were driving 3V parts with 5V parts, whether 3.3V parts running at 5V would be reliable, and whether running 5V parts at 3V would degrade their performance.

Anne Swager, another EDN editor who attended the conference, points out that the analog folks don't view this low-voltage situation as nearly as much of a problem as do the digital folks, who are closely tied to standard logic levels. The analog people mentioned the possibility of using high-efficiency switching regulators that can convert a battery voltage to an IC's optimal operating voltage. Other analog designers pointed out that previous ISSCC papers presented analog designs that worked from supplies as low as 1.5V (as did a paper from this year's batch). Regardless of the ability of many analog circuits to work at low voltages, using the new 3V circuits will be primarily a digital problem intrinsic to computers.

Multiple scenarios likely

Micron Technology, a DRAM and SRAM supplier, expects that manufacturers of low-voltage memory chips may follow a course that offers as many as four different voltage ratings:

- 3.3V ±5%
- 3.3V ±10%
- 3.0V ±10%
- 2.7 to 3.6V.

As an interim solution, Micron offers 3.3V ±5% chips in the form of 1- and 4-Mbit DRAMs. These chips are enhanced versions of existing 5V devices processed for 3.3V operation. The advantages of this type of low-voltage DRAM are its ability to work in dual-voltage systems and its early availability for 3.3V system development. Micron is also developing DRAMs that can operate over the 2.7 to 3.6V range, and the company will provide either 3.0V ±10% or 3.3V ±10% opera-

Table 1—Representative 3V circuits

Manufacturer	Typical circuits offered
AT&T Microelectronics	Low-power LP900C 3.3V CMOS standard-cell library. Includes memory elements, logic functions, linear cells, and high-level macrocells for 3V ASIC designs.
Cirrus Logic	CL-GD6412 VGA controller. Combines LCD graphics control with a mixed-voltage operating capability. The chip's internal logic operates at 3.3V, but the other sections can operate at either 3.3 or 5V.
Integrated Device Technology	16-bit buffers, transceivers, latches, and flip-flops. Octal bus-interface and support logic. 16-bit, 3.3V/5V bidirectional bus translator.
Maxim Integrated Products	The MAX561 RS-232C transceiver operates at voltages as low as 3.0V at a data rate of 20 kbps while maintaining EIA/TIA-562 signal levels of ±3.7V.
Micron Technology	1-Mbit (256k×4) and 4-Mbit (1M×4) extended-refresh DRAMs. 256-kbit (16k×16) synchronous SRAM. 288-kbit (16k×18) latched SRAM.
Motorola Inc	32-bit 68340V (3.3V) microprocessor and compatible 3.3V CMOS and BiCMOS logic. Also, two 3.3V versions of the 68HC11 8-bit microcontroller.
National Semiconductor Corp	Low Voltage Quiet (LVQ) series of 3V logic circuits. The 10-nsec LVQ series includes gates, flip-flops, multiplexers, and transceivers. The first of these devices are recharacterized 5V parts.
Philips/Signetics	HLL (High-speed, Low-voltage, Low-power) and LV-HCMOS (Low-voltage, High-speed CMOS) logic families. Devices from either family can operate from 1.2 to 3.6V supplies. At 3.3V, the devices consume only half the power of equivalent 5V CMOS types.
Samsung Semiconductor	3V 1024-bit serial EEPROMs. Organized into 64 registers of 16 bits each. Operate at 2 mA (30 μA standby).
Silicon Systems	32C9301 disk controller. Operates from 2.7 to 5.5V supplies. At 2.7V, the chip transfers data at 30 Mbps. At 5.5V, the data rate is 48 Mbps. The controller features Reed-Solomon error correction and DRAM or SRAM buffer support.
S-MOS Systems	3.0V gate-array and standard-cell libraries operate at voltages as low as 2.7V. Power consumption for gate arrays ranges from 2 μW/gate/MHz to 5 μW/gate/MHz.
Toshiba America	TC163G family of 3.3V gate arrays, ranging in size from 2500 to 200,000 usable gates. The I/O interface can operate at 3.3 or 5V; the core logic operates at 3V.

LOW-VOLTAGE ICs

tion from the same devices. Other memory suppliers are following roughly parallel courses, but the consensus is that the proposed 3.3V ±0.3V JEDEC standard may be the most viable on a long-term basis.

Although numerous suppliers of microprocessors, memory chips, and other logic circuits are jumping on the 3V bandwagon, there will be a lengthy transition period during which system designers will have to deal with two issues: selecting "3V" devices that may have been designed for operation at slightly different voltages and—most important—mixing 3 and 5V devices in the same design. For the most part, TTL/CMOS logic compatibility will not be a major problem. As **Fig 1** shows, when both devices are operating at 5V, a TTL output can drive a CMOS input, and a CMOS output can drive a TTL input.

Choosing a device

Choosing a specific 3V part is largely a function of the application and is also not a major problem. For example, designers of inexpensive palm-top computers powered from pen-light batteries might choose logic devices that can operate over a range of voltages such as 2.7 to 3.6V to extend the useful battery life. Conversely, designers of expensive laptop computers powered by regulated, rechargeable battery supplies might opt for 3.0 or 3.3V devices having a ±10% tolerance.

The major problem arises when designers must use both 3 and 5V devices in the same system. As Wayne Yoshimoto, a marketing engineer with Integrated Device Technology (IDT) points out, there is no interface problem for a 3.3V device driving a TTL-compatible 5V device. The input thresholds for a 5V TTL part are 0.8V for a logic 0 (low) and 2.0V for a logic 1 (high). A 3.3V device can drive a low less than 0.4V and a high greater than 2.4V at the rated output-load currents. This action provides ample noise immunity at both ends, making the interface essentially problem free.

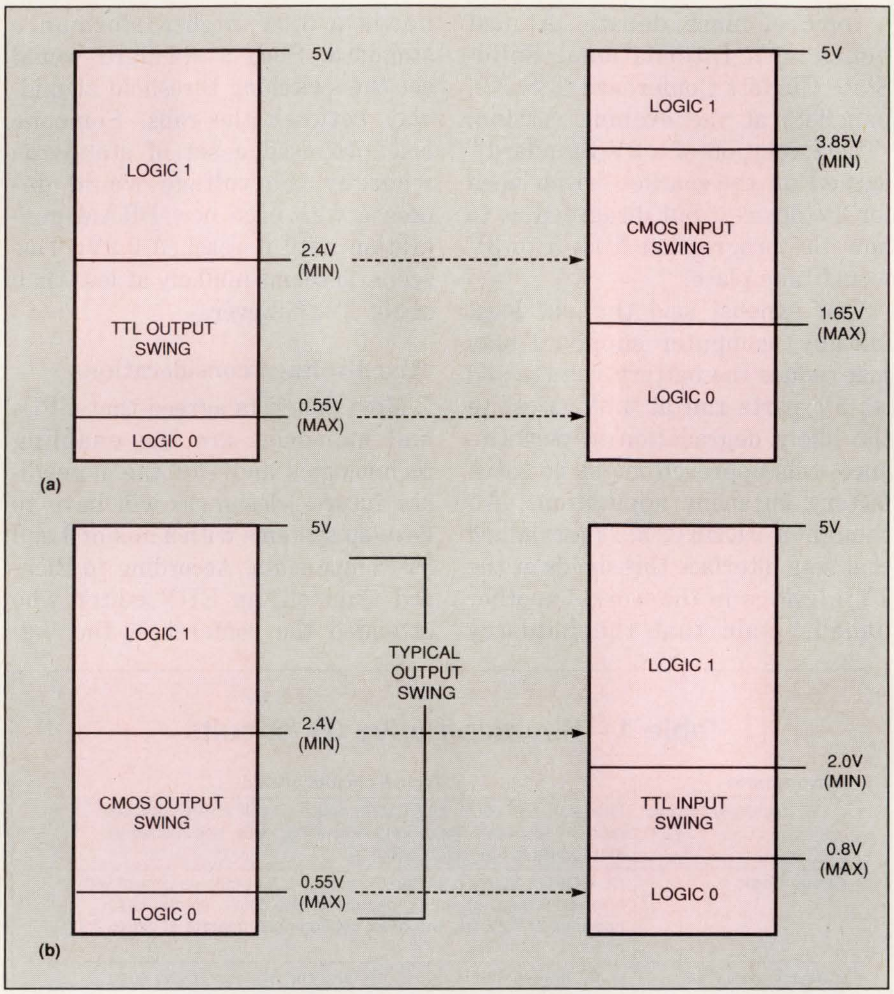
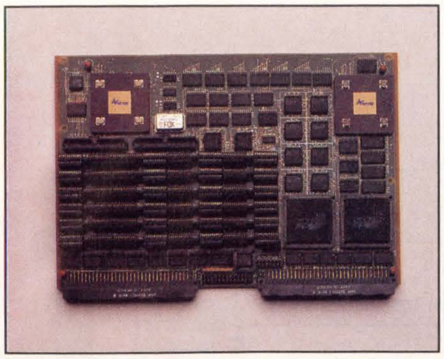


Fig 1—When both ICs are operating at 5V, TTL/CMOS logic compatibility is not a major problem. A TTL output can drive a CMOS input (a), and a CMOS output can drive a TTL input (b).

A 5V device driving a 3V device, however, is usually problematic. For ESD protection, most bus-interface and support-logic devices have an internal clamp diode connected between V_{CC} and the input, output, or I/O pin (**Fig 2**). In this case, directly driving a 3V part from a 5V part can forward bias the clamp diode and damage the 3V device.

The exception to this situation is a device such as IDT's 3.3V family of 16-bit bus-interface devices. Having 5V logic driving the 3.3V inputs of these devices is no problem because there is no clamp diode to V_{CC}. IDT has been able to provide ESD protection by other means. On an input, the absolute maximum rating of 7.0V is the same for both the 3.3 and 5V parts. However, outputs and I/O ports do have a clamp diode. In this case, a logic high on the 3.3V part is limited to $V_{CC}+0.5V$. Directly driving the 3.3V part from a rail-to-rail part can forward bias the clamp diode.

Devices that provide bidirectional translation between 3 and 5V buses help ease mixed-voltage interface problems. At least two de-



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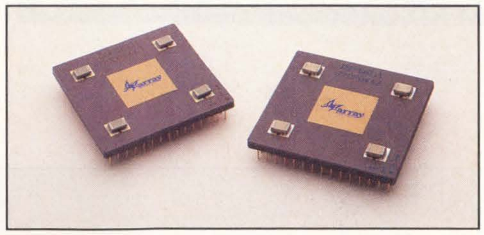

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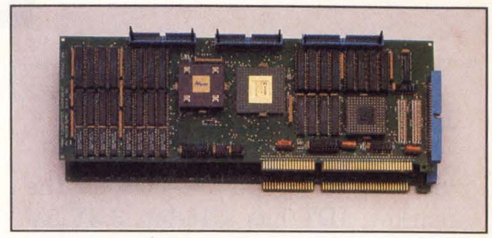

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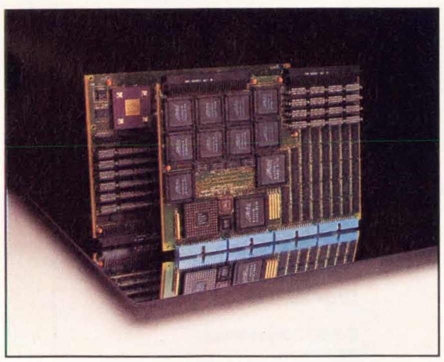

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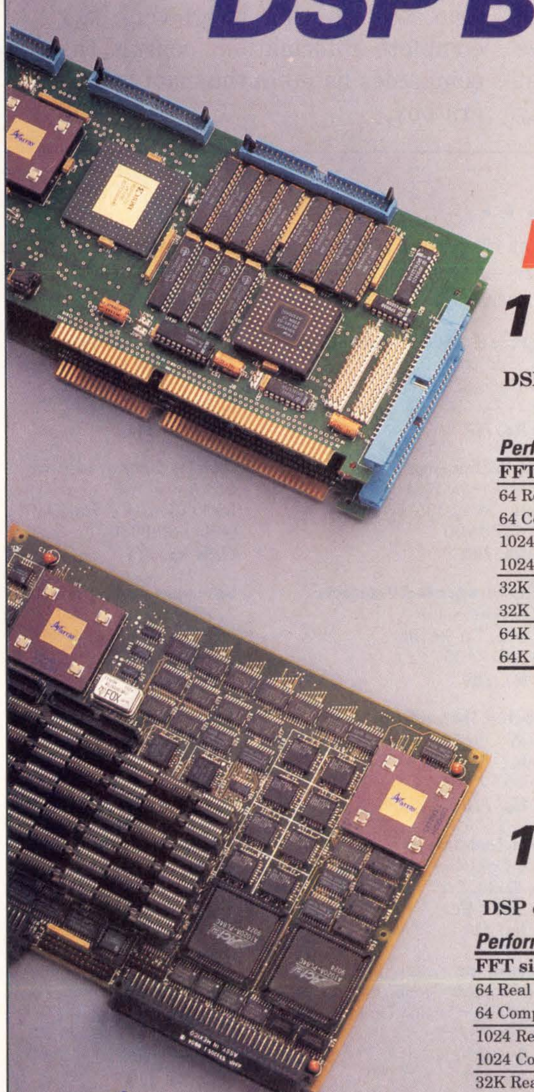

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Performance Benchmarks

FFT size	a66550/32K @25MHz
64 Real	7.2 µs
64 Complex	10.9 µs
1024 Real	125.9 µs
1024 Complex	209.9 µs
32K Real	5.90 ms
32K Complex	10.49 ms
64K Real	15.73 ms
64K Complex	N/A

VME DSP

1K FFT/79.6µs

DSP engine for industry-standard VMEbus

Performance Benchmarks

FFT size	a66540A @40MHz	a66540A Cascade Sys.
64 Real	5.1 µs	2.9 µs
64 Complex	5.0 µs	3.7 µs
1024 Real	79.6 µs	29.6 µs
1024 Complex	132.7 µs	59.1 µs
32K Real	3.69 ms	0.91 ms
32K Complex	6.56 ms	1.82 ms
64K Real	7.37 ms	1.82 ms
64K Complex	13.11 ms	3.64 ms

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vices of this type are now on the market. IDT has a 16-bit, 3.3V/5V bus translator, and Quality Semiconductor has a bus switch that provides 5 to 3V logic conversion with essentially zero delay. Other manufacturers of interface devices will likely introduce similar devices as the drive to 3V circuits continues.

In addition to AMD, Quality Semiconductor, Micron Technology and IDT, a host of other IC vendors offer devices that operate at 3.3V or less. **Table 1** (see pg 75) lists many of these vendors along with a brief description of representative devices. Keep in mind that this list is not all inclusive. A seemingly endless variety of 3V chips is available, and the list is growing. For complete information, consult the companies listed in the manufacturers box.

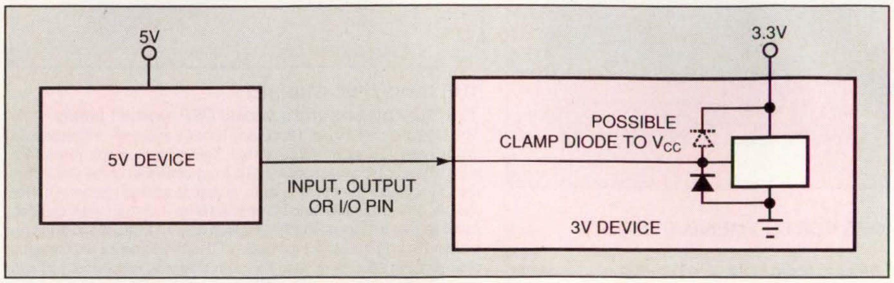

Fig 2—Problems can arise when a 5V device drives a 3.3V device. If the 3.3V circuit has a clamp diode to V_{CC} (the usual case), the likelihood exists that the output of the 5V device will forward bias that diode and damage the 3.3V device.

Article Interest Quotient
(Circle One)
High 473 Medium 474 Low 475

For more information . . .

For more information on the 3V devices discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you read about their products in EDN.

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Sunnyvale, CA 94086
(408) 737-7600
Circle No. 709

Microchip Technology
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(602) 963-7373
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Micron Technology
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Motorola Inc
Microprocessor Group
6501 William Cannon Dr W
Austin, TX 78735
(512) 891-2000
Circle No. 712

National Semiconductor Corp
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Santa Clara, CA 95052
(408) 721-5000
Circle No. 713

Oki Semiconductor
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Sunnyvale, CA 94086
(408) 720-1900
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Quality Semiconductor
851 Martin Ave
Santa Clara, CA 95050
(408) 450-8080
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Samsung Semiconductor
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San Jose, CA 95134
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Semiconductor Group (SC-91080)
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Dallas, TX 75380
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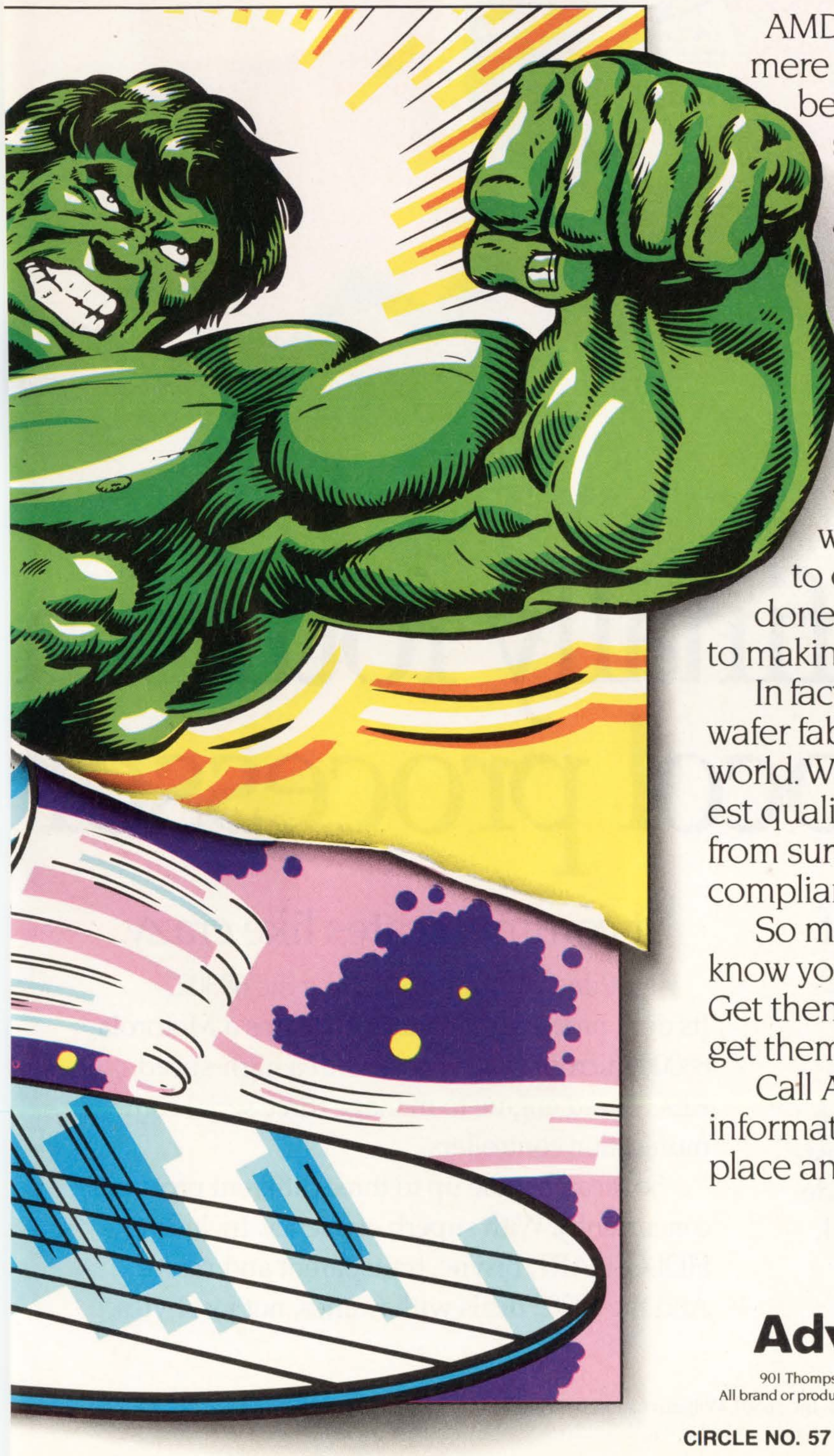

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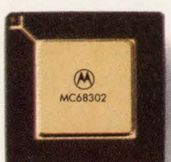

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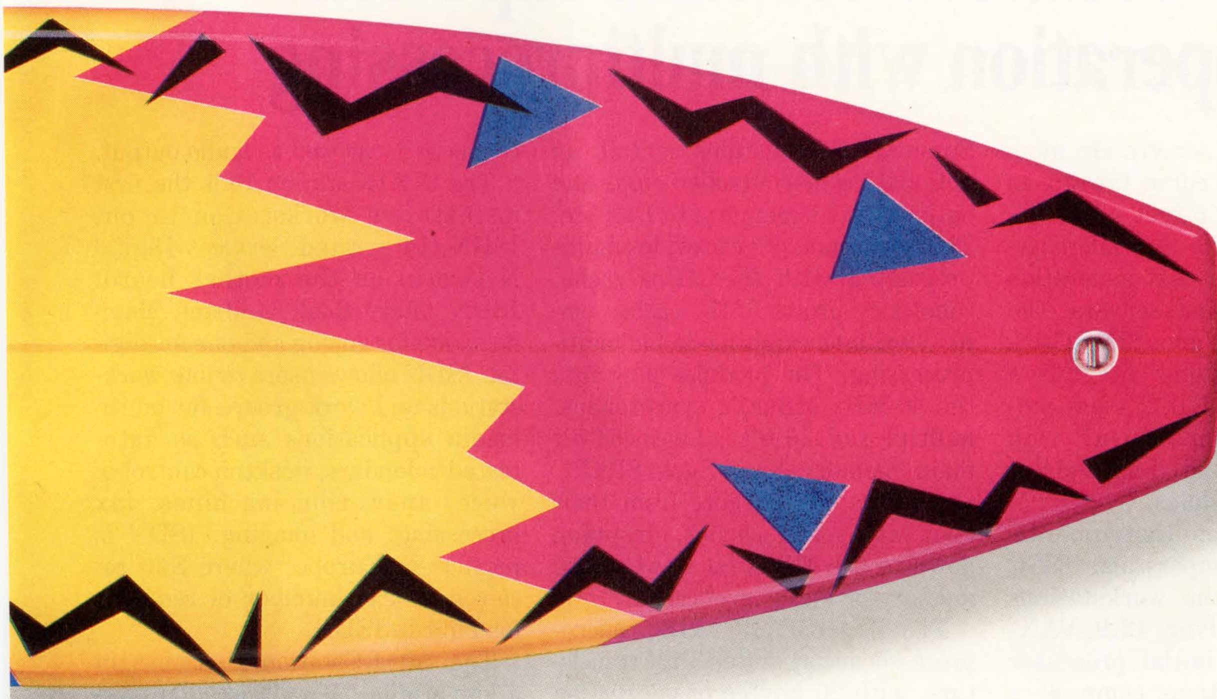

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Workstations combine superscalar operation with multiprocessing

Workstations and servers are moving up the power curve toward an end-of-the-decade target of 2000+ desktop VAX-MIPS. Sun Microsystems is fielding its next generation of workstations and servers, the SPARCstation 10 and SPARCserver 10. These systems integrate a third-generation RISC (reduced-instruction-set computer) μP with multiprocessing and field-replaceable processor modules.

Based on Texas Instruments' SuperSPARC, a superscalar RISC microprocessor, the workstations and servers deliver 42.9 VAX-MIPS. The two initial processor module configurations comprise a 40-MHz SuperSPARC with a 36-kbyte on-chip cache or a 45-MHz SuperSPARC having as much as 1 Mbyte of additional cache. Later versions will increase clock rates to 50 MHz and beyond. The SPARCstation and server 10 handle as many as two SuperSPARC modules, each having its own processor, in a multiprocessor configuration.

These products employ the Sun-developed MBus, which has been passed to SPARC International as a proposed industry standard. Multiprocessor Sun servers (the SPARCserver 600MP was introduced last year) first used MBus modules for multiprocessor replacement. Developed by Cypress Semiconductor, the modules used a second-generation SPARC RISC processor.

Sun engineers are pursuing the processor/cache module approach, a technology first pioneered for RISC processors by Fairchild/Intergraph for its Clipper RISC chip and Motorola with its 88000 RISC family. The MBus processor modules are 3.3×5.78 in. with a standard 100-pin, microstrip connector. Besides a TI SuperSPARC processor, the SuperSPARC modules contain an optional cache-controller chip, and optional cache memory, to 1 Mbyte. The cache controller provides multiprocessing with the MBus cache-coherency protocol; the caches employ write-through mode for multiprocessing. The modules plug into the 40-MHz MBus, a synchronous, multiplexed 36-bit address/64-bit main memory bus. SuperSPARC processors can execute from their own high-speed caches, dropping down to the MBus for slower main memory or lower-level cache.

TI's SuperSPARC RISC microprocessor incorporates 3.1M transistors, with 20 kbytes of instruction cache and 16 kbytes of data cache. The CPU is superscalar; it can issue as many as three instructions as a group for parallel execution.

The SPARCstation 10 is a high-end, desktop workstation with multimedia graphics processing capabilities. It integrates multimedia software with mother board hardware, such as a microphone pickup, digital-audio-tape-quality audio output (to 40 ksample/sec), and ISDN for voice and digital data. A special chip provides ISDN connectivity as well as audio output.

The SPARCstation 10 is the first mainstream workstation to put ISDN (Integrated Services Digital Network) on the mother board. ISDN offers dual 64-kbaud channels, one for analog and one for digital. ISDN allows users to link workstations and work groups for multimedia applications such as automated calendars, desktop control of voice, answering machines, fax processing, and imaging. ISDN is popular in Europe, where Sun received a large number of requests for built-in ISDN.

The SPARCstation 10 comes in a low-profile "pizza" box. The system provides a standard, twisted-pair Ethernet connection, as well as ISDN. Users can cram as much as 128 kbytes of 4-Mbit-based RAM (72 bits wide with parity) into the workstation box, or 0.5 Gbyte of 16-Mbit-based RAM. The system has four SBus slots for plug-in peripherals. The mother board employs SCSI-2, with its 10-Mbps data rate. (SCSI-1's rate is 5 Mbps.)

The workstations and servers run with Sun's Solaris Unix operating system V1.1. The software includes

SPARCstation 10 is the first Sun workstation to use MBus modules for multiprocessing.

Sun SPARCstation 10 and SPARCserver 10

- Multiprocessor with 1 or 2 TI SPARC modules
- CPU(s) on MBus module, 3.30×5.78 in., 40-MHz multiplexed bus
- TI SPARCmodule, 40-, 45-MHz clock, 42.0 SPECmarks at 40 MHz, 20-kbyte instruction cache on chip, 16-byte data cache on chip, as much as 1-Mbyte secondary cache
- Redesigned desktop "pizza" box
- 32- to 512-Mbyte ECC main memory, 16- or 64-Mbyte SIMMs (72 bits), holds 8 SIMMs
- Max disk storage: 848-Mbyte internal, 26-Gbyte external
- 4 SBus card slots
- 2 serial ports
- 1 parallel port
- 16-bit audio (40 kHz)
- External speaker connection Twisted-pair Ethernet
- ISDN on mother board
- Sun GX, GXplus, GT graphics accelerators as options
- 19-in. gray, 16/19-in. color monitor
- 10 Mbyte/sec SCSI-2

a desktop environment based on Open Windows. The compilers support the SuperSPARC architecture.

The SPARCserver 10 is a server aimed at work groups. It provides superscalar RISC multiprocessing in a non-VME-based system. It directly supports as many as 34 terminals, with as much as 2-Gbyte internal, or 26-Gbyte external, hard-disk storage. A 5-Gbyte tape is available for backup. Prices for the server start at $18,000 for a base system with 16 Mbytes of RAM, GX graphics, a floppy-disk drive, and a monochrome monitor.—**Ray Weiss**

Sun Microsystems, 2550 Garcia Ave, Mountain View, CA 94043. Phone (415) 960-1300. FAX (415) 969-9131. **Circle No. 738**

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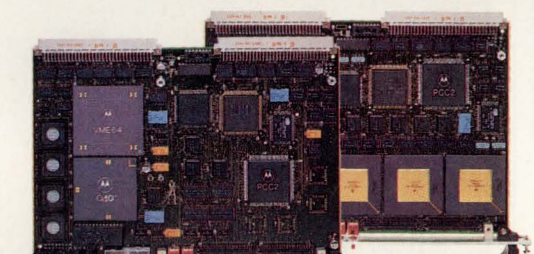

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Superscalar SPARC executes as many as three instructions in parallel

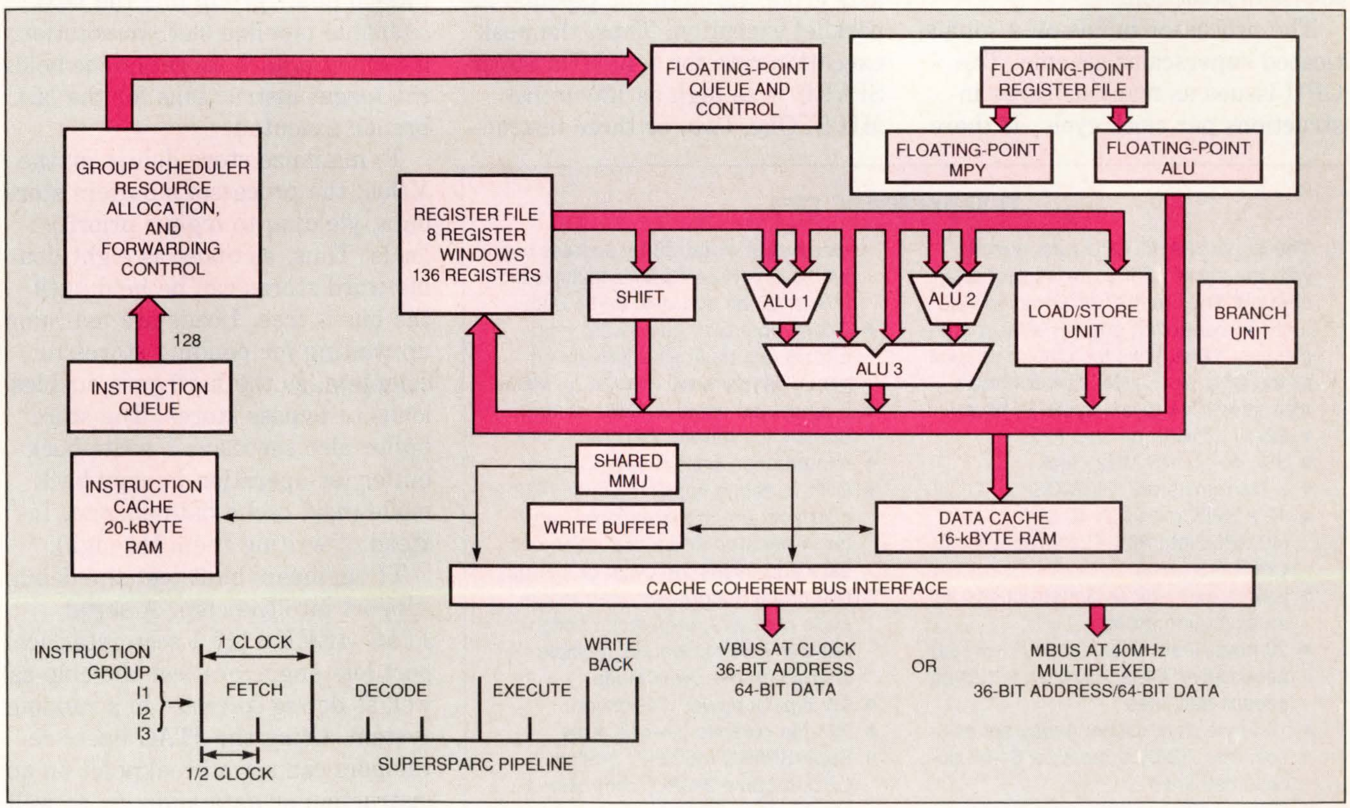
The Texas Instruments' third-generation RISC microprocessors (μPs) are the first superscalar implementation of the SPARC RISC (reduced-instruction-set-computer) processor. SuperSPARC has a 3.1M transistor chip (0.8-μm BiCMOS) with 36 kbytes of internal cache. The processor can execute as many as three instructions in parallel each clock cycle.

SuperSPARC's development is the result of a joint Sun and TI project. The first chips will chug along at 40 and 45 MHz, with later versions hitting 50 MHz—and eventually 100 MHz. A simulated SuperSPARC at 40 MHz delivers 42.9 SPECmarks (40 SPECint and 45 SPECfp), which is the equivalent of 42.9 VAX-MIPS (a VAX 11/780 is considered a 1-MIPS machine). SPEC benchmark programs run on the target CPU and compare to program performance on a VAX.

Engineers can design in the TMS 390Z50 processor two different ways: Either it operates as a stand-alone processor, interfacing directly to Sun's MBus (system memory bus); or it operates as part of a chip set, with its own cache controller and fast cache static RAM (SRAM). TI furnishes SuperSPARC in two MBus modules: a stripped-down module, with only the processor running at 40 MHz, or an integrated module with the processor running at 45 MHz, a cache controller, and 1 Mbyte of pipelined SRAM cache.

TMS390Z55, the cache controller, supports a private synchronous bus, the VBus, which comprises a 36-bit address bus and a 64-bit data bus. The VBus provides a module-level secondary cache with as much as 1 Mbyte of fast SRAM running at the CPU clock rate. The cache controller also links to the system MBus, a 40-MHz, synchronous multiplexed bus (36-bit address/64-bit data). VBus supports multiprocessing with hardware bus snooping and cache write-through, ensuring system cache coherency. Also, a generalized packet-based system interface matches other multiprocessing buses; the VBus supports an 8-bit peripheral bus as well.

This superscalar chip provides two extremely large on-chip caches: a 20-kbyte, 5-way set-associative program cache and a 16-kbyte, 4-way set-associative data cache. Currently, these are the largest on-chip caches available for a RISC μP (the Intel i860 RISC has a 32-kbyte cache). Large caches enhance RISC performance because larger pro-



SuperSPARC is the first superscalar SPARC μP. It issues as many as three instructions per clock cycle, moving them through the 8-stage pipeline as an execution group.

gram chunks and data sets stay on chip, minimizing cache-miss penalties that drag down CPU performance. The caches are physically addressed—an on-chip SPARC Reference Memory Management Unit (standard MMU) translates the virtual addresses. The high-speed MMU translates both data and instruction accesses in one clock cycle.

Large cache sizes are particularly important for superscalar processors that require *n* instructions per clock cycle, where *n* is the CPU's superscalar degree—the number of instructions issued in parallel. For SuperSPARC, three instructions can be issued at each clock cycle. At 40 MHz, that necessitates a sustained instruction bandwidth of 480 Mbytes/sec (40 MHz × 3 instruction × 4 bytes/instruction) to meet peak execution rates. To feed that rate, the processor's cache interface is 128 bits (16 bytes) wide, which is buffered by an 8-instruction prefetch queue that holds instructions for issue selection.

The processor builds on a sophisticated superscalar scheme. The CPU issues as many as three instructions per clock cycle. If there are no data dependencies or other interlocks, these three instructions can execute in parallel. In contrast, a second-generation RISC processor can, at best, issue and execute only one instruction per clock cycle—although they generally achieve less than that. Typically, a RISC processor takes 1.2 to 1.6 cycles per instruction (CPI) because of data dependencies (input data is not ready), branch and load/store delays, and cache misses (the time to locate and retrieve the missing code or data).

This RISC processor is pipelined, with eight stages, each of which executes in a ½ CPU clock cycle. The pipeline is fixed, but unlike earlier RISC architectures, hardware operations may use one or more stages. For example, instruction fetch takes two stages; instruction decode, three stages; execute, two stages; and write-back, one stage. Three instructions are plucked simultaneously and, if OK, are sent as a group through the pipeline for parallel execution. Thus, the peak execution rate for a 40-MHz SuperSPARC is as high as 120 native MIPS. One, two, or three instructions are issued simultaneously; object-code instruction order is maintained, and no instruction will be issued before its predecessor, although it can finish earlier.

Superscalar processors generally have a number of separate functional units, each of which executes a distinct set of instructions. These functional units can execute in parallel, providing superscalar execution engines. The SuperSPARC has eight functional units, including three adders.

Branches tend to slow RISC processors; many second-generation RISC CPUs use branch delay slots (empty pipeline slots to be filled by other instructions) to compensate for the longer time needed to process branches. SuperSPARC uses the branch delay technique coupled with a branch target cache to minimize branch delays. Many branches will have no pipeline stalls or delays. When a group of instructions with a branch is issued, a branch delay group fills the next available pipeline slot. In addition, a 4-entry branch target queue holds the target instructions for the last branch executed.

To minimize store delays on the VBus, the processor's buffers store data, yielding to higher priority loads. Thus, as many as eight double-word stores can be held until the bus is free. Loads are not hung up waiting for pending stores to complete, as the hardware enables loads to bypass stores. The store buffer also serves as a write-back buffer for operation in copy-back mode (hold cache data changes instead of writing them through).

TI engineers built test and debug support into the chip. A serial JTAG (IEEE 1149.1 scan interface) port lets engineers test the chip as well as debug software in a running system. Using the JTAG lines, developers can set a breakpoint on an instruction or data address, as well as on cycle or instruction counts. For critical debugging, users can

TI SuperSPARC CPU

The SuperSPARC CPU runs directly with the system MBus or as part of a chip set. The chip set includes the CPU, a cache controller, and SRAMs. A special bus, VBus, links the chips and runs at the CPU clock rate. The controller also interfaces to the system MBus.

- 32-bit μP with on-chip FPU
- 33-, 40-, or 45-MHz clock
- 3.1M transistors, BiCMOS
- 42.9 SPECmarks at 40 MHz (40 SPECint); 96 SPECthruput for 2 CPUs (45 MHz)
- Issues as many as 3 instructions as an execution group
- 20-kbyte instruction cache: 5-way set associative; 64-byte line size; 128-bit access half lines
- 16-kbyte data cache: 4-way set associative; 32-byte line size; 64-bit access half lines
- 8-stage pipeline (2× clock/stage)
- 2 external bus interfaces: VBus private bus at clock; 36-bit address bus; 64-bit data bus; 40-MHz multiplexed MBus; 36-bit address; 64-bit data
- Cache controller chip: 2.2M transistors; as much as 2 Mbytes on VBus; as much as 1 Mbyte on MBus
- 8 functional units: 3 ALUs: shifter, branch, load/store; FPU MPY, DIV
- 4-instruction branch-target queue
- Built-in debug support; serial JTAG interface; on-chip breakpoint register; 1 breakpoint on instruction or data addresses, on cycle or instruction count underflows; instruction, cycle counters; breakpoint action register sets strobe pin, multiple instruction per cycle mode
- 8W typical power dissipation
- 293-pin ceramic pin-grid array
- SuperSPARC modules: module 1-CPU, module 2-CPU, controller; 1-Mbyte static RAM

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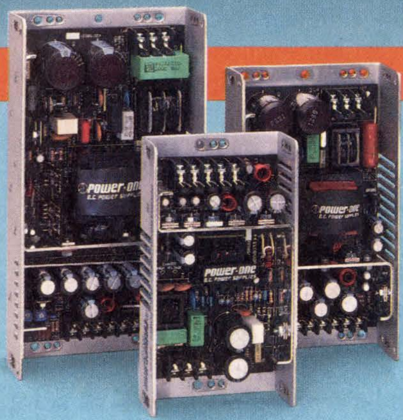

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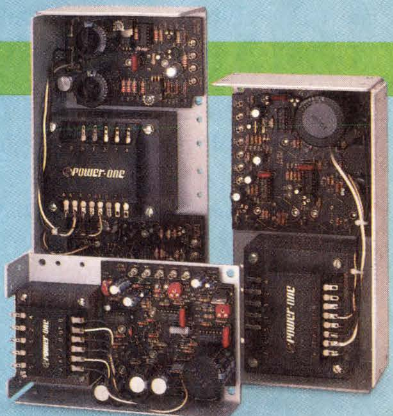

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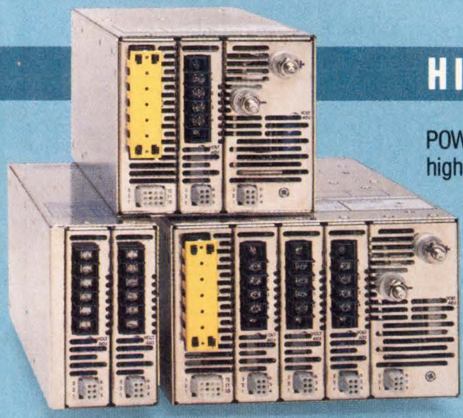

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turn off superscalar operation, making it easier to track instruction execution. The cache controller also has JTAG test and debug features, including event counters to track cache performance.—**Ray Weiss**

Texas Instruments Inc, Box 809066, Dallas, TX 75380. Phone (713) 274-2379. **Circle No. 739**

Superscalar SPARC RISC integrates CPUs, cache controller, and SRAM

Single-chip implementations are not the only form for a superscalar RISC SPARC microprocessor (µP). Cypress Semiconductor's approach is a multichip module that tightly integrates a CPU chip with a cache controller and fast static-RAM (SRAM) memory. Running at 66.7 MHz, the CY7C620 processor chip issues as many as two instructions per clock cycle. It features an 8-kbyte local instruction cache, supplemented with as much as 256 kbytes of zero-wait-state RAM.

The hyperSPARC chip set—the CY7C620 CPU, CY7C625 cache controller, and CY7C627 SRAM—fits on a SPARC Level 2 MBus module. This module drops right into the Sun SPARCstation 10 or SPARCserver 10 boxes, or other Sun servers. Unlike the TI SuperSPARC module, which holds one CPU, Cypress modules hold two processor combinations.

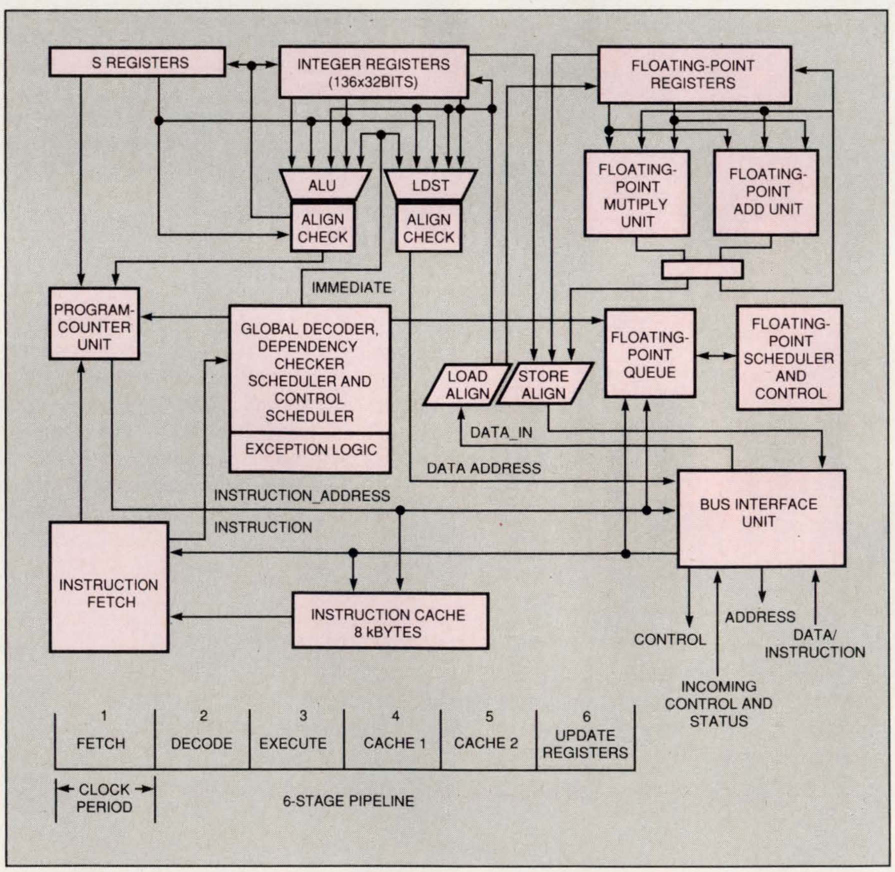
Each Cypress processor has an Inter Module Bus (IMB), linking the CPU with its cache controller and SRAM caches. The IMB runs at the CPU clock rate. Each cache controller holds the processor memory-management unit (MMU), maintaining CPU access to the module cache as well as the motherboard MBus memory. The cache controller supports multiprocessor cache coherency via physical bus snooping and a write-through cache strategy.

Initially, CPU clock rates are 55.5 MHz, but designers expect rates to move as high as 80 MHz. At 55.5 MHz, the hyperSPARC delivers 52 SPECmark performance (simulated). That performance will increase to 85 SPECmarks at 80 MHz. In contrast, TI's hyperSPARC delivers 42.9 SPECmarks at 40 MHz. However, these are simulated benchmarks, and the relative performance may change under real system conditions.

The CPU pays a 1-clock-cycle penalty in accessing off-chip cache, but that penalty is factored into the pipeline. The processor has a 6-stage pipeline; each stage takes one processor clock to execute. Some of those stages, the cache1 and cache2 are used for loads and stores to the cache. If the next instruction pair is not in the on-chip cache, there is a 1-cycle penalty in loading from the module cache. In effect, the CPU acts as a 7-stage pipeline machine. Thus, hyperSPARC trades a 6- or 7-deep pipeline for access to a large module cache. The SPECmarks show that approach to be a viable tradeoff, exchanging a cycle delay for smaller chip size and larger caches.

The chip can issue two different instructions each clock cycle. Four function or execution units include an integer unit, which does integer arithmetic, shifts, and logical operations; a load/store unit; a branch/call unit, which handles program address changes for branches and subroutine calls; and a floating-point unit (FPU), which has FPU-add and FPU-multiply units.

Two instructions (64 bits) are both launched if no hazards or data dependencies exist. One or both instructions stall until the hardware



A superscalar RISC processor, the hyperSPARC issues as many as two instructions per cycle. Rather than relying on limited on-chip caches, the processor uses large, fast off-chip caches integrated with a cache controller on an MBus module.

Cypress hyperSPARC CY7C620 CPU

Part of a chip set. The CPU interfaces to an Inter Module Bus, linking to a cache controller and special SRAM cache chips. The cache controller interfaces to the mother-board main memory MBus.

- 32-bit μP with on-chip floating-point unit
- 66.7-MHz clock (later 80-MHz)
- 1.1M transistors (0.65-μm CMOS)
- 52 to 85 SPECmarks (simulated), 0.9 CPI, 61 sustained native MIPS (55.5 MHz)
- Inter Module Bus interface links CPU, cache controller, 32-bit external address bus, 64-bit external data bus, 3.3V for speed at chip clock
- 8 register windows (136 32-bit registers)
- Issues as many as 2 instructions/cycle
- 6-stage pipeline
- 8-kbyte instruction cache: 5-way set associative; 32-byte line size
- off-chip unified cache supported by CY7C625 cache controller chip; 128 or 256 kbytes; 1 clock off-chip access penalty; direct-mapped unified cache; 64-byte line size; interfaces to MBus; 40-MHz multiplexed bus; 32-bit address/64-bit data; 32-byte read and 64-byte write; buffers to main memory; special SRAM chip (CY7C627) pipelines cache writes, 16k × 32-bit structure
- 4 functional units: Integer, Branch/Call, Load/Store, and FPU (Add, MPY)
- Branch prediction—always fetch branch target instruction
- 20W max module power dissipation (1 CPU)
- Packaged as MBus module with CPU(s), cache controller, SRAM CYM6221K: 1 CPU 128-kbyte cache; CYM6222K: 2 CPUs 128 kbytes/CPU; CYM6226K: 2 CPUs 256 kbytes/CPU
- $3500 (100) for CYM221K; samples, 3rd quarter of 92; OEM qty, 4th quarter of 92

is ready for execution. No further instructions are issued until pending instructions execute.

The FPU operates with its own queue. The queue buffers floating-point instructions and passes them to the FPU-add and FPU-multiply units. The scheduler issues only one instruction to the floating- point unit per clock cycle. The units are pipelined and therefore can handle multiple instructions.

To minimize branch delays, the chip uses a branch-taken algorithm.If all branches are assumed taken, the hardware will fetch the branch-target instruction for execution. If the branch turns out to be not taken, a 2-cycle penalty incurs while the hardware fetches and decodes the next sequential instruction. A high number of program branches are jumps to continue a loop (branches taken).

The cache controller incorporates the processor's MMU and cache-data tags for fast cache operation. The controller also serves as an interface between the processor and the system MBus. On the MBus side, the controller provides read-and-write buffering, minimizing hang-ups between the systems. It supports the SPARC MBus Level 2 cache-coherency protocol and can move data in transaction sizes of 1, 2, 4, 8, and 32 bytes. The cache controller supports burst or non-burst transactions, as well as cache-to-cache data transactions and block-copy or fill operations. The MMU translates between the CPU's virtual-memory addressing and the MBus's physical addressing. The module SRAM cache comprises special SRAMs with a 2-stage pipeline for writes.—**Ray Weiss**

Cypress Semiconductor, 3901 N First St, San Jose, CA 95134. Phone (408) 943-2653. FAX (408) 370-8092. **Circle No. 740**

Chip mixes μP/DSP for fax, modem, and voice processing

Yesteryear's microcontrollers (μCs) couldn't ante-up the power that desktop fax, modem, and voice processing demand. Today's μCs, on the other hand, team up an 8- or 16-bit CPU with high-performance DSP engines for algorithmic horsepower. Targeting low- to midrange fax, voice, and modem applications, Zilog's Z89120 integrates a Z8, 8-bit μC with a 16-bit DSP processor.

The Z89120 combines a low-cost μC for base control and I/O with a 16-bit DSP engine for fast algorithmic processing. The Z8 is a Z80 derivative; it supports 24 kbytes of program ROM and uses a register file of 256 × 8-bit RAM for dynamic memory. Processing is register based, with the register file organized into separate, easily addressed register banks for fast context switching. In addition, the Z8 supports off-chip data and program memory.

Supplementing the 8-bit Z8 μC is a 16-bit DSP processor. Unlike many μC/DSP combinations, the Z89120 DSP engine operates independently, running its own set of I/O peripherals. It can generate a PWM (with 10-bit accuracy), as

Zilog Z89120 mixed-signal processor

- 20.48-MHz clock (10.24 MHz internal)
- Z8 μC core: 24-kbyte ROM; 10 clock cycles/instruction; 64-kbyte address space with off-chip memory if needed; 262 × 8-bit registers (RAM); two 8-bit counter/timers with 6-bit prescaler; 2 comparators; 6 I/O ports (47 I/O pins); 6 vectored interrupts
- 16-bit DSP processor: 24-bit ALU, accumulator, shifter; pipelined, single-cycle execution; 4k × 16-bit program ROM; two 256-byte data RAMs; 4 RAM pointer registers with automatic indexing; 6-deep stack; 3 vectored interrupts; 2 timers; 10-bit PWM; 8-bit A/D (to 128-kHz sampling)
- Brownout protection (detects power drop and resets chip)
- Power-down mode (200-mW typical dissipation)
- Software library: fax, voice, modem, phone functions
- 68-pin PLCC
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well as take in analog signals and convert them to digital values. Thus, the DSP processor doesn't depend on the μC for I/O processing, which speeds up the DSP response and frees the μC for control and I/O.

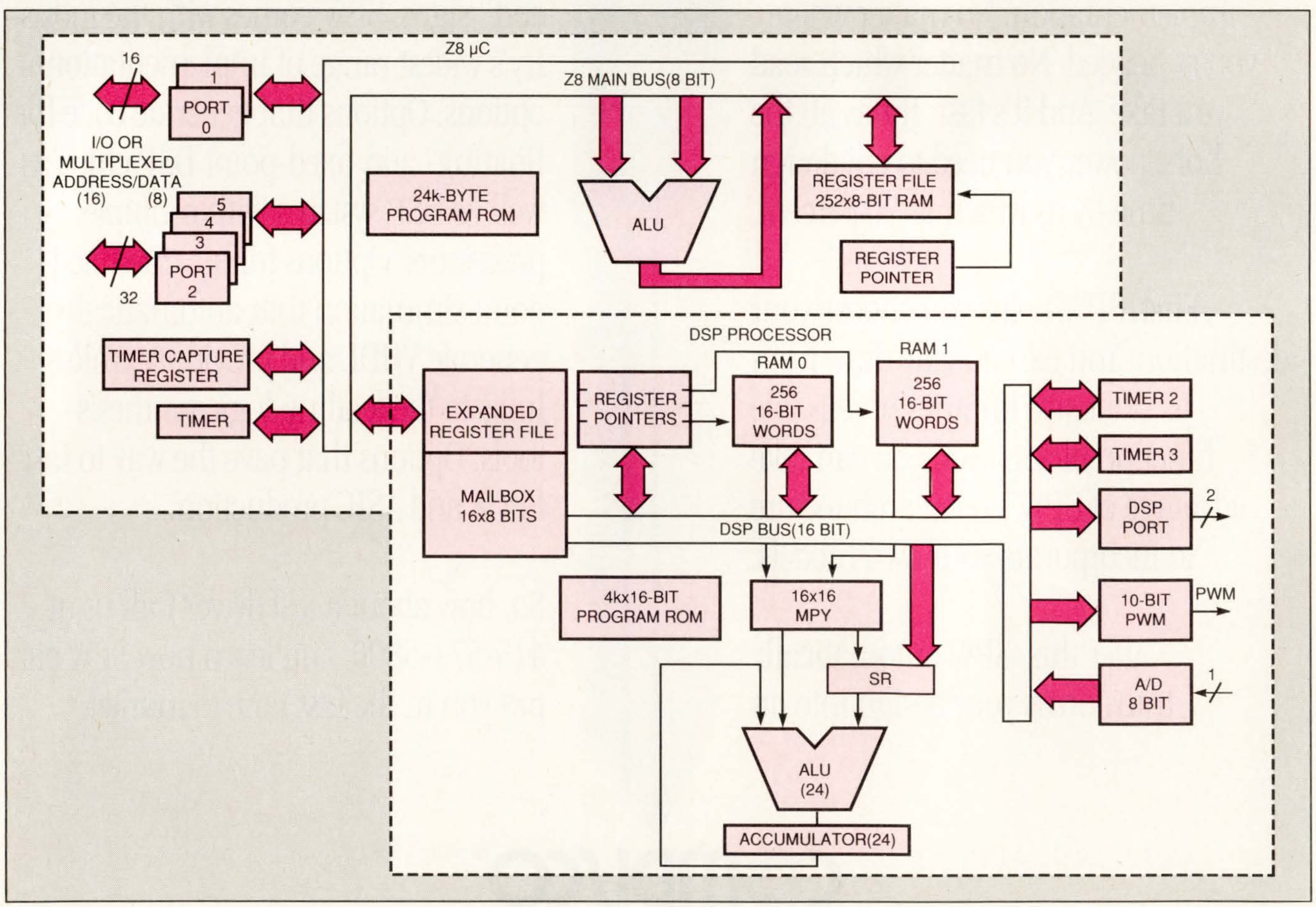
The DSP processor is pipelined, delivering single-cycle execution for multiplies, shifts, and arithmetic operations. Two 256-word RAM areas hold processing parameters for multiply/accumulate processing. The DSP engine incorporates automatic loop controls, which index pointers to RAM. In the DSP, a program can walk the data areas with zero addressing overhead—the next RAM parameters are automatically accessed for each multiply/accumulate (MAC) cycle.

The two processors—the 8-bit Z8 and the 16-bit DSP CPU—are loosely coupled. They communicate via a register mailbox. Either processor can read or write to this mailbox, which serves as a mechanism for exchanging data. The mailbox is accessible via sixteen 8-bit registers (Z8) or eight 16-bit registers (DSP). Either processor can interrupt the other; on receiving an interrupt, the receiving CPU can check the mailbox for parameters passed by the sending CPU.

The Z89120, however, is not the only μC/DSP combination. National Semiconductor's HPC46100 integrates a 16-bit μC with a DSP-like MAC unit. Motorola added DSP functions, and a multiply/accumulator to its 16-bit 68HC16 μC. Zilog, however, was the first to integrate a DSP processor with an 8-bit μC. Zilog produced a number of Z8/DSP combinations that target different application areas, including the Z86C99, which integrates an 8-bit μC and 16-bit DSP with peripherals like the Reed-Solomon ECC, a disk signal interface, and a dynamic-RAM buffer controller.

In the world of 32-bit processors, National Semiconductor has combined a 32-bit embedded CISC (complex-instruction-set-computer) processor with a specialized DSP processor; this combination suits desktop applications. The latest release, the 32FV16/X164, when combined with a special ASIC chip, handles a range of desktop processing, including voice synthesis and fax processing.

Zilog has also developed a software library for fax, voice, and modem processing. This library sup-



The Z89120 integrates a Z8 μC with a 16-bit DSP processor. The processors are independent, each with its own peripherals; they communicate via a register mailbox and internal interrupts.

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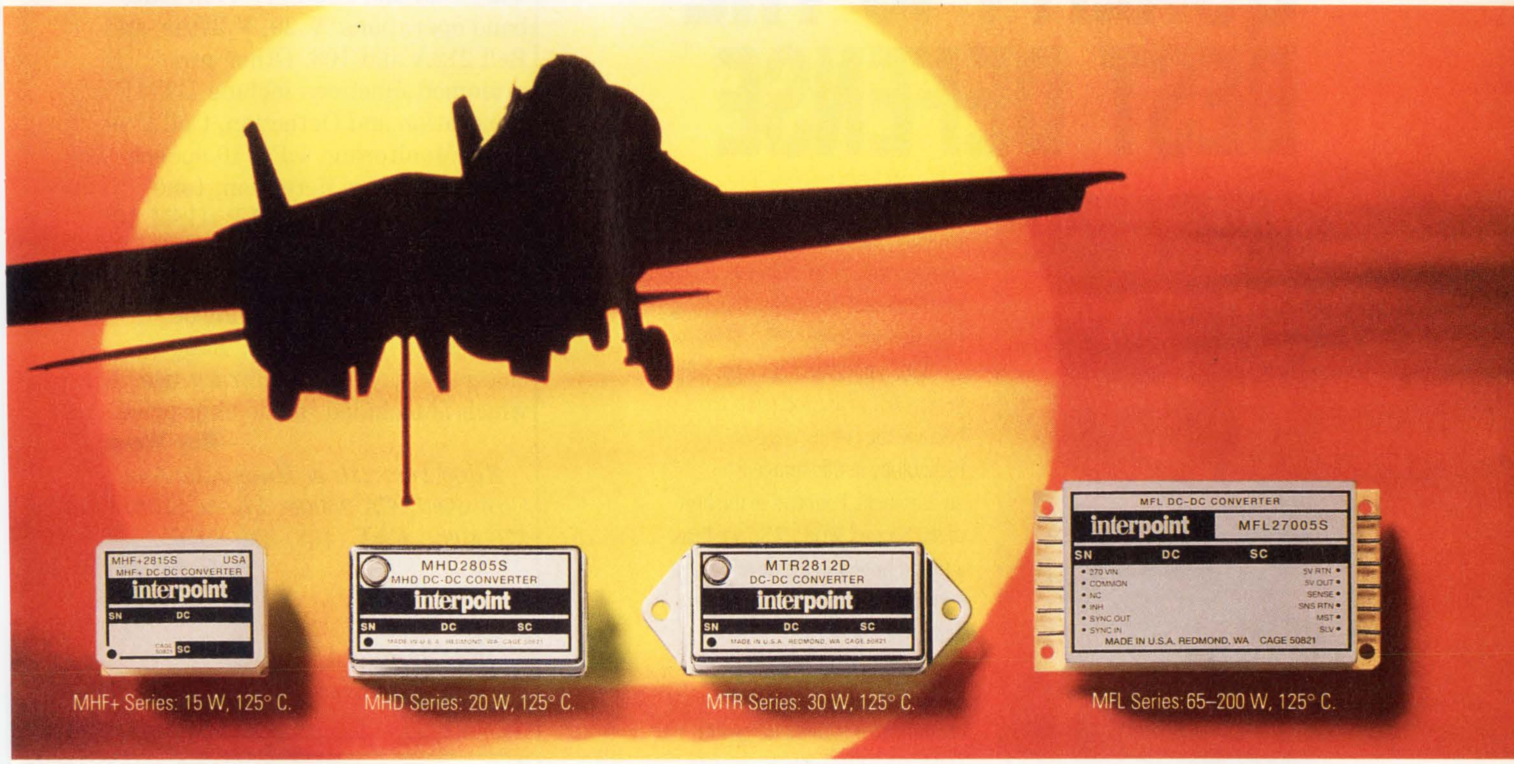

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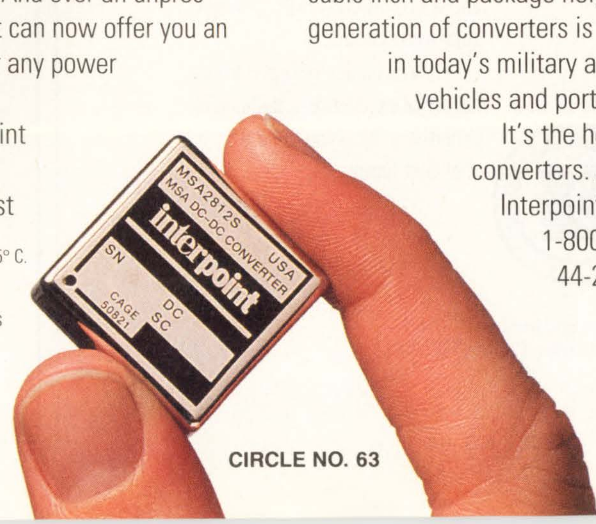

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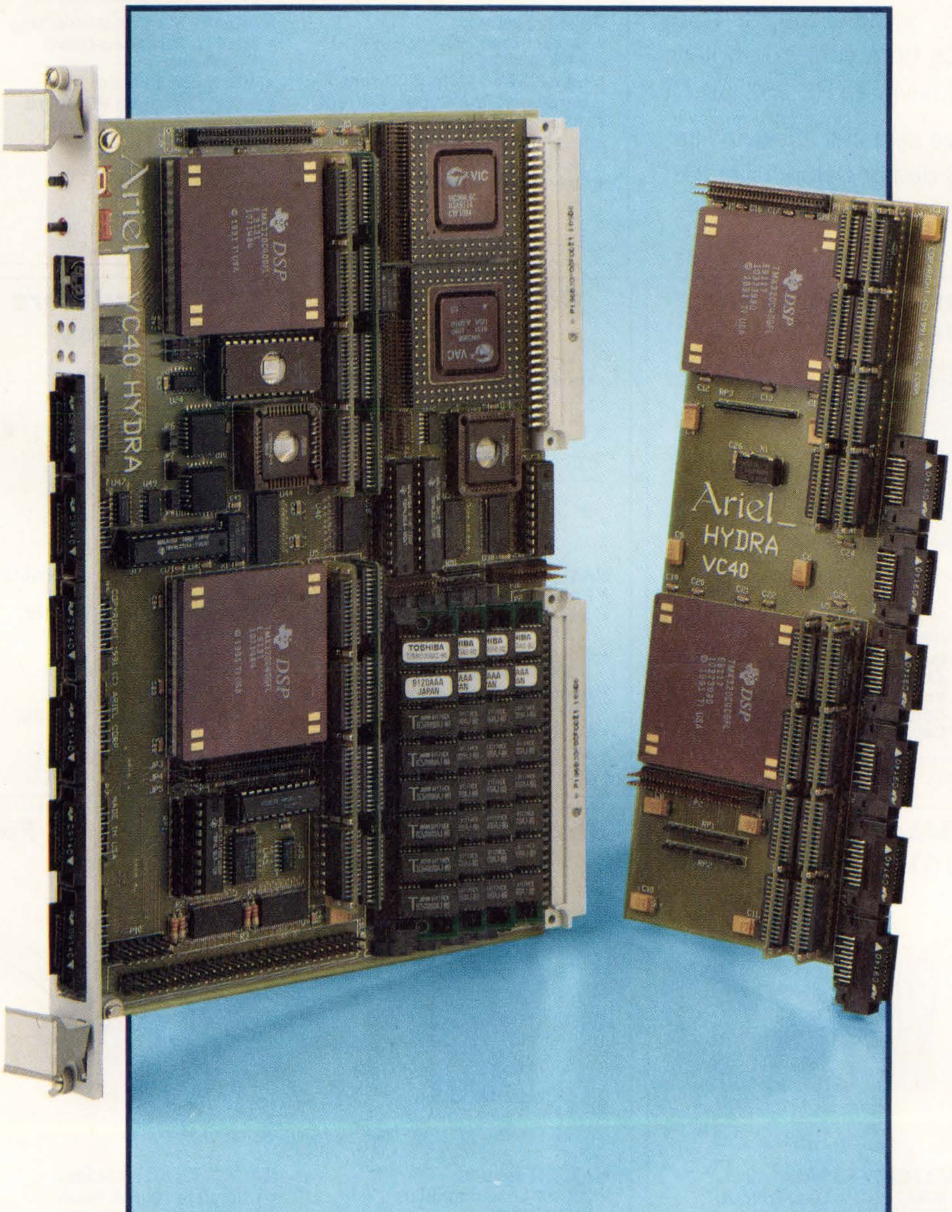

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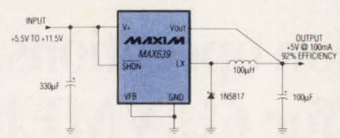

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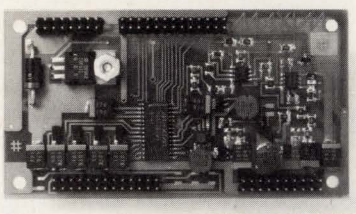

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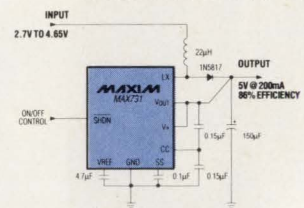

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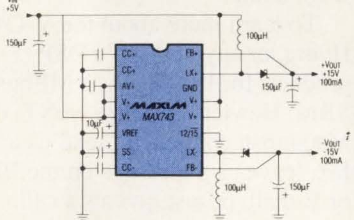

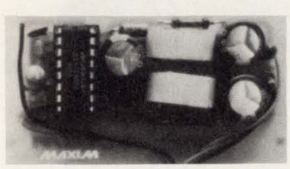

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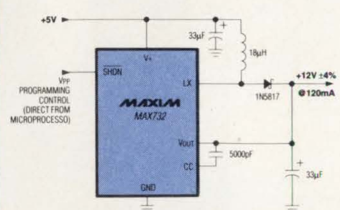

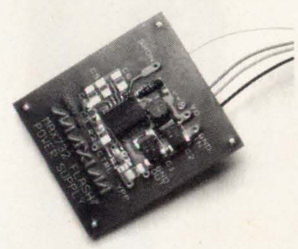

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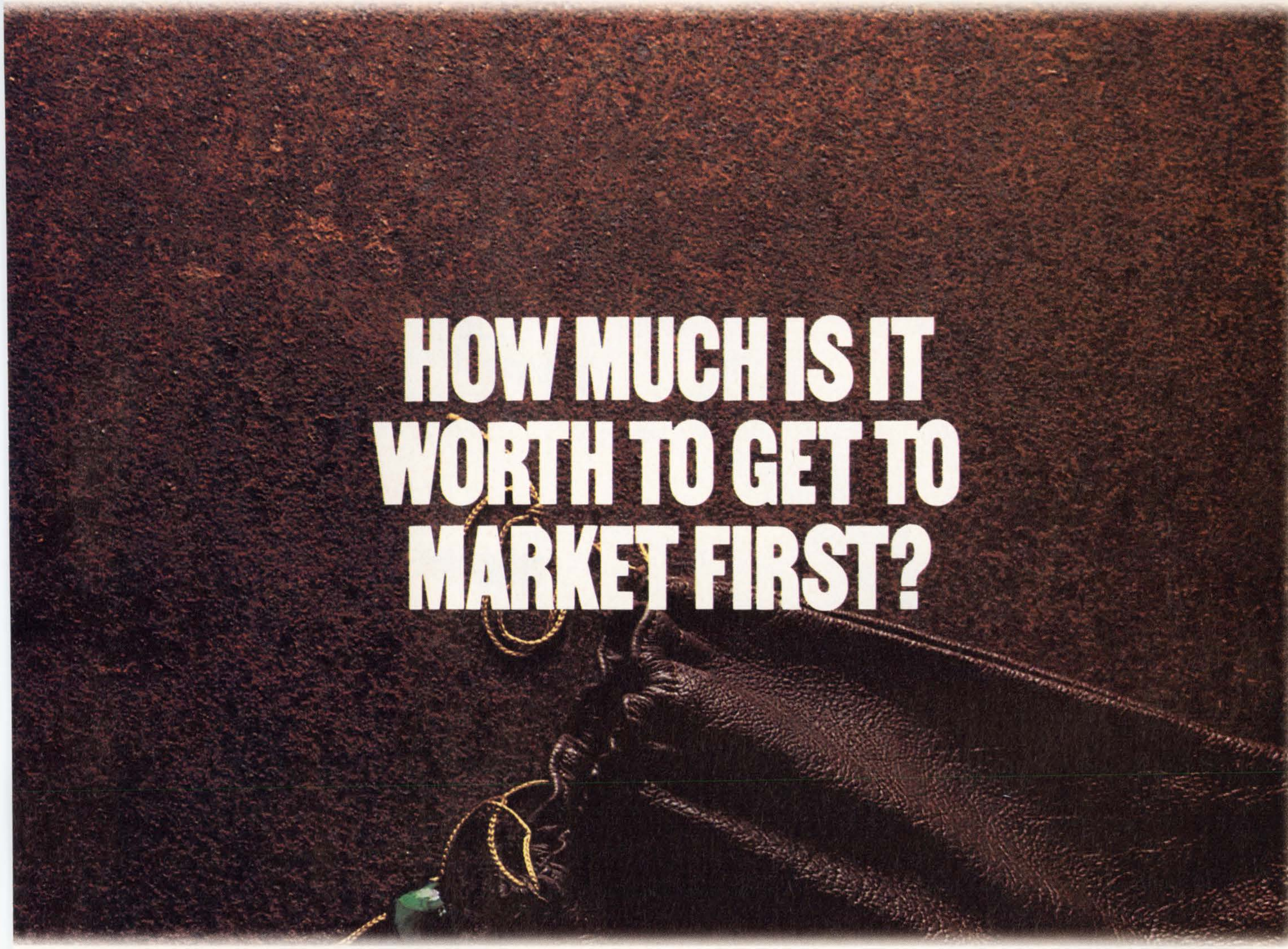

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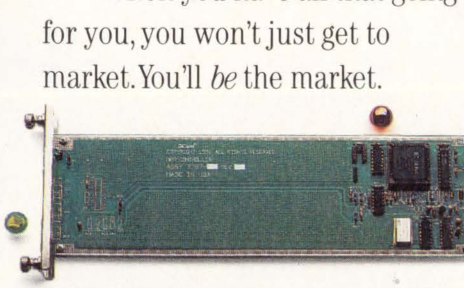

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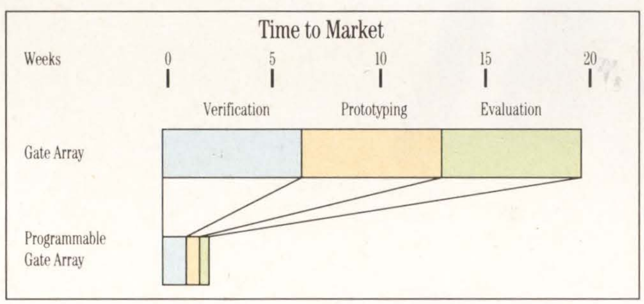

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You've got to sort through a welter of pros and cons in deciding whether you should convert your FPGA to a mask-programmed gate array. (Photo courtesy Lattice Semiconductor)

FPGA CONVERSION

Knowing that you could convert a field-programmable gate array to a mask-programmed device may be reassuring, but it doesn't guarantee that conversion will happen.

Charles H Small, Senior Technical Editor

Two worlds are colliding: programmable logic and ASICs. The two were once like island continents upon which unique flora and fauna evolved. Now their tectonic plates have rammed together and the populations of the two worlds are intermingling. Programmable-logic designers are now seriously considering converting their FPGA (field-programmable-gate-array) designs to mask-programmed gate arrays.

However, the two continents aren't exactly Eden and Atlantis; doing an FPGA and mask-programmed gate-array design presents a host of problems. Field-programmable and mask-programmed gate arrays differ far more than their names suggest. Physically, with one or two exceptions, FPGAs do not resemble mask-programmed gate arrays in the slightest. Their physical differences manifest in the form of significantly dissimilar electrical and mechanical properties: speed, delays, power consumption, and pinouts. In fact, the only similarity between the two classes of devices is their ability to hold large amounts of digital logic.

Programmable logic is familiar to every logic designer. Slowly and surely, it has been getting more flexible, faster, and denser. Early PAL devices gave birth to larger and more flexible devices such as the now ubiquitous 22V10. Next came devices, called "EPLDs" (erasable programmable logic devices) by some, that held the equivalent of multiple 22V10s. Now FPGAs are available that can vacuum up, into one package, logic circuitry equivalent to multiple EPLDs. Although no single accepted method for

The FPGA spreadsheet in this article is available on EDN's computer bulletin-board system (BBS). Phone (617) 558-4241 with modem settings 300/1200/2400/9600,8,N,1. From the Main System Menu enter *ss/freeware*, then *rk#469* to keyword search for "SR #469."

measuring FPGAs' capacity exists, capacity estimates range from 1000 to 10,000 gates for currently available FPGAs.

Meanwhile, a tiny cabal of logic designers has been working with mask-programmed gate arrays. Most logic designers have never done a mask-programmed gate array. Indeed, the fact that programmable-logic makers could get away with calling their largest devices FPGAs (field-programmable "gate arrays") shows how unfamiliar the average logic designer is with gate arrays. A few leading-edge designers are working with mask-programmed gate arrays that comprise 200,000 logic gates. However, a large chunk of mask-programmed gate arrays actually shipping are in the 1000- to 10,000-gate range—well within the capacities of FPGAs.

Thus, you *could* realize a given logic design either in an FPGA or a mask-programmed gate array—or both. But to formulate a convertible design, you would have to keep several factors in mind. First, a regular, fully synchronous design is best. Many designers think they are doing fully synchronous designs, forgetting that they have an asynchronous element here and there.

Second, squeezing your design down so that it uses up the last two percent of available gates is not a good idea. Mechanical compatibility, such as matching power, ground, signals, programming, and test pins, is not trivial. You will have to incorporate your gate-array vendor's design-for-testability criteria from the start.

Third, clock structures are always a headache in conversions. FPGAs have dedicated clock structures, whereas mask-programmed gate arrays have a clock tree. Converting clock structures can mean expensive hand work.

But far more important than the physical differences between FPGAs and mask-programmed gate arrays are the divergent design methods the two camps use. While programmable-logic tools are well known, widely used, and resemble engineers' traditional paper-and-pencil methods, gate-array design methods are worlds apart from the usual run of logic design.

Simply put, mask-programmed gate-array designers formulate an abstract design, simulate it to death, and then send their design off to a silicon foundry. Several weeks typically elapse between the time a mask-programmed gate-array designer sends a design to the supplier and when the supplier returns working devices. One key element in this transaction is an exhaustive set of test vectors supplied by the design engineer. The supplier must have these test vectors to weed out bad devices. Mask-programmed gate-array designers

Editor's analysis

Adopting a hardware-description language (HDL) to do your logic designs means changing your mind—literally. Computerized scans of the brains of people performing various tasks reveal that people use distinct and separate areas of their brains for visual and textual tasks. Recent discoveries in physiology and cognitive psychology, as well as the history of engineering, suggest that for most good engineers, the visual area is significantly stronger than the textual. Because engineers certainly can't exchange their visual brains for more textual ones, those who are advocating HDLs should take note.

If you want to bring yourself up to speed in the current wisdom, you should add the **references** listed on pg 116 to your summer reading list. Begin with Howard Gardner's *Frames of Reference* (**Ref 1**). Gardner is a must read. His theory of multiple intelligences is essential to understanding the chasm that separates visual and textual design methods.

Next, Thomas G West's *The Mind's Eye* (**Ref 2**) documents the unfortunate correlation between extraordinary visual intelligence and mild-to-severe dyslexia. West profiles well-known scientists and engineers from history who, while they were in school, were thought to be stupid because they had mediocre textual intelligences. Examples are well-known dummies such as Michael Faraday, Thomas Edison, and Albert Einstein.

Gardner's theory suggests that good engineers may have extraordinary visual intelligence. Certainly, engineers are already notorious for not writing well. So if Gardner's and West's theses are true, then engineers may be uniquely unqualified to use textual design tools.

Henry Petroski's *The Pencil* (**Ref 3**) is a historical look at engineering. Petroski bases his history on the pencil because it was perhaps the first engineered, mass-produced product. Petroski hammers home the point that the pencil is also the tool of the engineer. Engineers have historically produced a drawing of what a device is, not a textual description of what it does.

Because HDLs so resemble software, the record of software projects should concern you. Max Schindler's (**Ref 4**) book on CASE (computer-aided software engineering) is on the list because Schindler makes a damning case against normal software practice. After reading the book, you may agree that the most telling question to ask about software is, how do programmers get away with doing such a consistently bad job? According to Schindler, large programs have historically had error rates in the percentages (parts per *hundred*), spend about 40% of their total design time formulating these vectors.

Programmable-logic designers, on the other hand, waste no time simulating a design before compiling it. Instead, they formulate a design, program a part, and test the part immediately in a prototype. This very common sequence goes by the name of the "blow and go" method. Programmable-logic designers typically do not produce exhaustive test vectors simply because they do not need them; in-circuit testing in a prototype confirms the design.

Although the sequence of design steps for programmable logic and mask-programmed logic are different, until recently the design software was somewhat similar in principle, albeit incompatible in format. Both types of designers could express their designs as schematics, truth tables, Boolean equations, or finite-state machines. Various logic compilers or logic synthesizers would translate these specifications into a working piece of silicon.

The two types of design software were even converging in price. Originally, PAL-device software was free, whereas mask-programmed gate-array software cost hundreds of thousands of dollars. Now programmable-logic software ranges in cost from $2000 to $30,000, and some mask-programmed gate-array software has dropped below $20,000 for IBM PC versions.

Despite this convergence of tools and prices at the low end of the gate-array field, both mask-programmed gate-array designers and FPGA designers may be heading toward a radical change in design methods. Leading-edge mask-programmed gate arrays have capacities measured in the hundreds of thousands of gates, and FPGAs are sure to follow in their tracks, but somewhere around the 10,000- to 20,000-gate level, current design methods run out of gas. The tools for high-capacity gate arrays are radically different from all other engineering tools—computerized or manual (see **box,** "Editor's analysis"). Designing large gate arrays using a hardware-description language (HDL) resembles programming far more than it does engineering.

Does doing the doable pay?

Examining the compatibility of FPGAs and mask-programmed gate arrays, and their respective software, may be a technological red herring. The real question is how many FPGA designs are actually valid candidates for conversion? Mask-programmed gate-array and FPGA makers surveyed by EDN pulled numbers out of the air that averaged about 5%. If only 5% of all FPGA designs are actually candidates for conversion to mask-programmed gate arrays, why then

whereas engineers shudder at error rates in the parts per *million*. Programmers actually spend considerably more hours performing "maintenance" (programmerese for that portion of the design and debug that gets done after the program ships to customers) than they do on the initial design.

Proponents of HDLs would turn engineering into programming. Instead of drawing a symbolic representation of what an electronic device is, they would have you enter a text description of what it does. The reason they cite for the switch from diagrammatic to textual methods is the false imperative that current symbolic systems are too cumbersome for large designs. Therefore, they reason erroneously, engineers must shift to a form of programming. And, *of course*, programming means entering long strings of ASCII text into bottomless files.

This idea that doing "high-level" work on a computer necessarily involves typing in language statements is merely a holdover from the era of early, primitive computers. Early computers with their crude user interfaces and rudimentary operating systems, such as Unix, could handle only ASCII text. Now, even inexpensive personal computers have powerful visual user interfaces and sophisticated operating systems. **Ref 5** is a roundup of diagrammatic-programming systems with which you can draw, instead of write, your program. Not surprisingly, most of these diagrammatic systems are aimed at engineers.

Engineers prefer visual design tools because a drawing can mimic, or symbolize, the actual structure of a device that has parallel paths or feedback loops; a linear string of text is inherently a poor way to represent such structures, as anyone who has ever tried to write a real-time program knows.

If language is so unsuited to engineers' purposes, then why do HDLs exist at all? HDLs are not designed with *you* in mind. A passing familiarity with the arcane class of tools known as "compiler compilers" would reveal that the consumer for whom HDLs are designed is the HDL compiler, not the engineer. In short, HDL proponents have taken the easiest path for themselves that they can to concoct a user interface to their logic synthesizers.

Luckily, the availability of inexpensive but powerful PCs and the rapidly increasing capacity of FPGAs mean that a terrific opportunity exists for someone to come up with a visually oriented, logic-design program that really suits the way engineers work and think.

do one-third of FPGA designers say that such a conversion is important?

FPGA designers are probably checking-off conversion on their specification sheets on faith because they believe in their hearts that their current project will take off like wildfire and sell in the millions. So too does every play that a football coach diagrams on a blackboard end up with the ball in the end zone. The sad truth is that in both football and electronics, most plays garner only short yardage. Thus, only a tiny fraction of all FPGA designs will be valid candidates for conversion because only a few electronics designs sell more than 2500 units per year.

The history of programmable devices offers two earlier instances where mask-programmed versions of field-programmable devices offered an anxiety-reducing check-off item for specifying engineers but precious little sales volume for device makers. PAL-device (programmable-array logic) makers offered mask-programmed versions called HALs (hard-wired array logic). The theory was that if your product began to ship in high volumes, you could get mask-programmed versions of field-programmable PAL devices at a substantial cost savings. Nonetheless, HAL sales never amounted to more than 2 or 3% of PAL-device shipments.

The humble EPROM had a similar career. Touted as a prototyping device, EPROMs had a tendency to stay in a design and get shipped as a production part. When the cost of one-time-programmable EPROMs hit about a 3:1 ratio with mask-programmed PROMs, the impetus to convert from EPROMs to PROMs evaporated. Note that the cost of FPGAs is dropping in a similar fashion (**Fig 1**).

Programmable devices are not the only realm where a strong financial reason to migrate results in surprisingly little movement. In the ASIC world, migrating a proven design to the next-generation technology can result in increased performance and lower costs. But ASIC engineers seldom upgrade their old designs.

Additional considerations intrude

Another important factor involved in the decision to convert—or not—is the scarcity of engineering resources. Unless a designer is committed to conversion from the beginning, the impetus for conversion usually comes from the production department. The production department will want to convert to lower manufacturing costs. So now the designer's company has to answer the political question: who is to do the conversion, design or production? Often, the answer is that limited engineering resources are best applied to designing new projects, not upgrading old ones, so neither department does the conversion.

Conversions involve uncertainties and extra costs. You can incur additional charges for items such as test vectors or testability circuitry that will push the break-even point out further. The highest-anxiety factor is the chance that the mask-programmed gate array will not work, necessitating another cycle through design, simulation, test-vector generation, . . . and the mask-programmed gate-array maker's NRE.

Uncertainties about mask-programmed gate arrays in your inventory are hard to put a dollar figure on, but they can hit you two ways: if your supplier runs into a snag, you can be caught without an adequate supply of your custom devices; or, if you have to change your design, you can be stuck with a stock of unusable custom parts.

A 1:1 conversion is relatively easy to justify and may not require any design expertise. If your company uses one of the mask-programmed gate-array companies that will do the entire conversion for you, price is the basis for most of your decision.

But not all conversions need be 1:1. That is, replacing a single FPGA exactly with a mask-programmed gate array is not the only type of conversion possible. Because mask-programmed gate arrays lead FPGAs in capacity by more than an order of magnitude, you can economically combine an FPGA and some random logic—or even multiple FPGAs—into a single

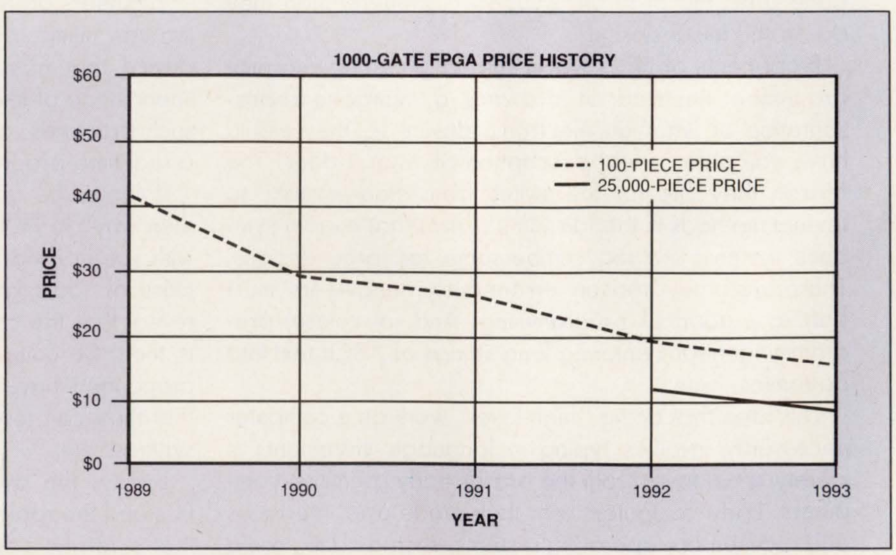


Fig 1—The price history of an older 1000-gate FPGA, which currently sells for 3 to 4 times the price of an equivalent mask-programmed gate array, indicates that the currently very high prices for newer FPGAs will probably drop drastically too.

mask-programmed gate array. In such cases, the conversion will necessitate engineering time and a pc-board revision, further increasing NRE costs. And don't forget standards and government regulations: an upgrade may entail an expensive requalification. Because of the extra design time required, a many-to-one conversion may buy you only 10 to 15% more in cost savings—hard to sell to management.

Mature, nascent considerations

Consider also that by the time a product has become mature enough for the production department to want to reduce productions costs, the marketing department may want to enhance the product's features. So, here too, the company has to decide whether to do a simple conversion or to do a redesign.

However, bean counting does not determine when conversion makes sense. Keeping in mind that mask-programmed gate arrays are faster, have more packaging options, more features, and are more capacious than FPGAs, logic designers have several conversion paths they could embark upon:

- Do an FPGA design, reserving the option to convert the FPGA to a mask-programmed gate array later.
- Do a multiple-FPGA design (plus perhaps a few PAL devices and some random logic), reserving the option to convert the FPGAs (and other logic) to a single mask-programmed gate array at a later time.
- Do an FPGA/multiple-FPGA and masked-programmed gate-array design in parallel, using the FPGA(s) for prototyping or initial production runs.

The last option, doing designs in parallel, makes sense for several reasons. Your mask-programmed gate-array-based system may have subsystems that you cannot simulate. An example would be a printer. Because simulators for the mechanical parts of the printer do not mate up with the mask-programmed gate-array simulator, you will need prototype electronics early in the design cycle. Or, in other cases, you might need a prototype system quickly so that the programmers can begin working on software as early as possible. Or your marketing department might be willing to incur the increased cost for FPGAs to get a new product out as early as possible. **Fig 2** shows the advantages, using a sophisticated analysis in relation to time rather than a simple steady-state analysis. The earlier the product is available, the earlier your company starts accumulating profits.

Simple, but tedious costing

Simple math, involving two costs—one favorable and one unfavorable—can determine the point at which a conversion becomes economical. First, FPGAs cost more than mask-programmed gate arrays. The least expensive FPGAs cost at least three times as much as a corresponding mask-program-

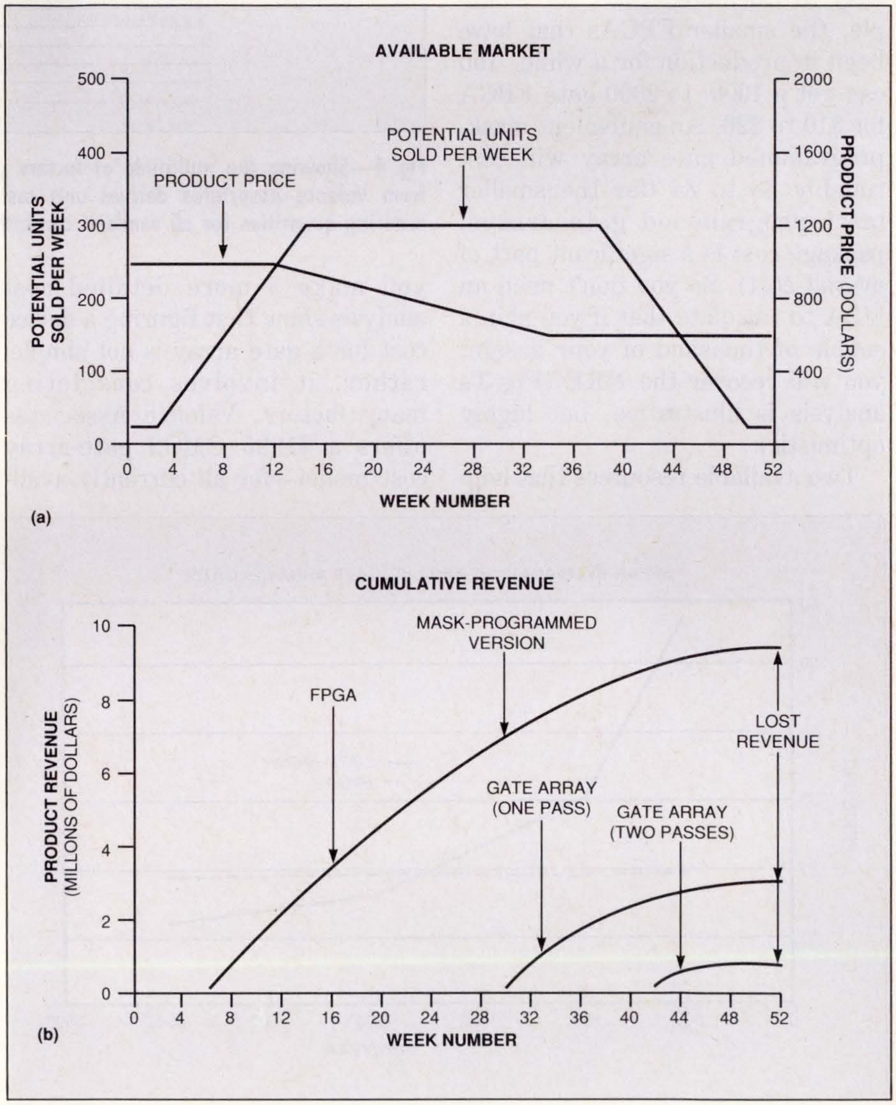


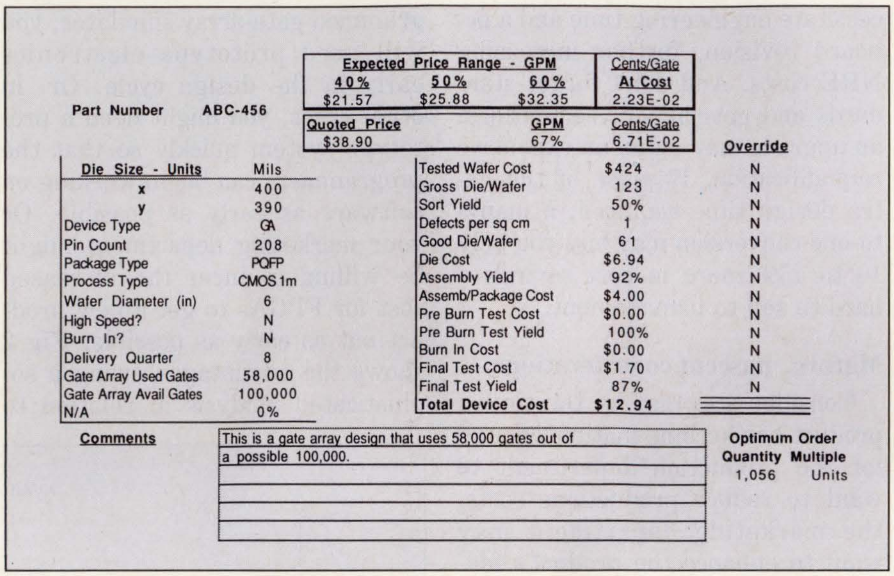
Fig 2—Your marketing department may be willing to trade the higher cost of an FPGA for an earlier product launch. This example from Altera depends on several variables: the shape of the product-sales curve and price curve in (a) and the development leadtimes in (b). Obviously, your analysis could vary significantly. Notice that the price curve also assumes a shift to a mask-programmed part.

FPGA CONVERSION

med gate array. And leading-edge FPGAs can cost 15 to 40 times as much as a corresponding mask-programmed gate array. On the other hand, mask-programmed gate-array vendors charge a $10,000 to $15,000 service fee—or NRE (non-recurring engineering) cost—for each iteration of a design.

The break-even point, where the savings from lower-cost mask-programmed gate arrays recoup the attendant NRE cost, seems pretty easy to calculate. Take, for example, the smaller FPGAs that have been in production for a while. You can get a 1000- to 2000-gate FPGA for $10 to $20. An equivalent mask-programmed gate array will cost roughly $3 to $4 (for the smaller mask-programmed gate arrays, package cost is a significant part of overall cost). So you don't need an MBA to calculate that if you ship a couple of thousand of your design, you will recover the NRE (**Fig 3**'s analysis is illustrative, but highly optimistic).

Two available resources that help you make a more detailed cost analysis show that figuring a device cost for a gate array is not simple; rather, it involves considering many factors. Valence Associates offers a $1995 CMOS gate-array cost model—for all currently available mask-programmed gate arrays from various vendors—that can give you a more accurate cost estimate (**Fig 4**). The model is an Excel 3.0 spreadsheet. **Fig 5** is a spreadsheet format, courtesy of Lattice, into which you can plug both FPGA and mask-programmed gate-array numbers. You can find this spreadsheet on the EDN bulletin-board system (BBS) at (617) 558-4241, posted on the /freeware Special Interest Group as SR #469.



Part Number ABC-456

Expected Price Range - GPM			Cents/Gate At Cost
40%	50%	60%	
$21.57	$25.88	$32.35	2.23E-02

Quoted Price	GPM	Cents/Gate
$38.90	67%	6.71E-02

Die Size - Units	Mils
x	400
y	390
Device Type	GA
Pin Count	208
Package Type	PQFP
Process Type	CMOS 1m
Wafer Diameter (in)	6
High Speed?	N
Burn In?	N
Delivery Quarter	8
Gate Array Used Gates	58,000
Gate Array Avail Gates	100,000
N/A	0%

		Override
Tested Wafer Cost	$424	N
Gross Die/Wafer	123	N
Sort Yield	50%	N
Defects per sq cm	1	N
Good Die/Wafer	61	N
Die Cost	$6.94	N
Assembly Yield	92%	N
Assemb/Package Cost	$4.00	N
Pre Burn Test Cost	$0.00	N
Pre Burn Test Yield	100%	N
Burn In Cost	$0.00	N
Final Test Cost	$1.70	N
Final Test Yield	87%	N
Total Device Cost	$12.94	

Comments: This is a gate array design that uses 58,000 gates out of a possible 100,000.

Optimum Order Quantity Multiple 1,056 Units

Fig 4—Showing the multitude of factors you must consider, this ASIC-cost spreadsheet from Valence Associates derives unit costs, GPMs (gross profit margins), and optimal ordering quantities for all vendors' currently available mask-programmed gate arrays.

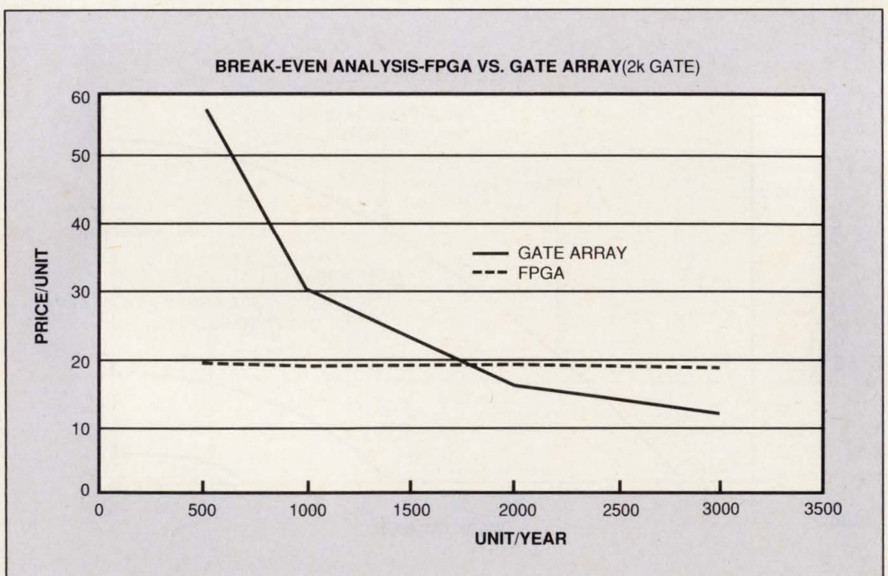


Fig 3—This simple break-even analysis begins with the following assumptions: the FPGA total engineering cost is $5300; the mask-programmed gate-array NRE cost is $27,300; an FPGA costs $0.013/gate; a mask-programmed gate array costs $0.0007/gate; and the package for both types of devices is a 68-pin plastic leaded chip carrier. By this analysis, mask-programmed gate arrays become economical at approximately 2000 devices/year.

Mask-programmed gate-array makers cite a surprisingly wide range for the minimum number of devices per year that makes economic sense. Fujitsu says 2000, Gould AMI declares 3500 to 4000, Texas Instruments (an Actel second source) suggests 5000, GEC Plessey and Atmel chorus 10,000, and Oki wants 10,000 to 25,000. Keep in mind that silicon foundries operate on a large scale that is compounded by the lilliputian size of their products. One 6-in. silicon wafer will yield more than a thousand good devices. Thus, a company willing to gear up for a production run of only 2000 mask-programmed gate ar-

FIXED COSTS	GATE ARRAYS	iepE^{2}CMOS	E^{2}CMOS	SRAM	UVCMOS	ANTI-FUSE
NRE Charges (masks)	$10,000	$0	$0	$0	$0	$0
Design						
Hardware Tools	$15,000	$5,000	$5,000	$5,000	$5,000	$5,000
Software & Development Tools	$10,000	$1,390	$1,390	$5,000	$9,950	$9,690
EngineeringTime (Man Weeks @ $2K/Man Week)	4	2	2	2	2	2
Simulation						
Tools NRE	$5,000	$0	$0	$0	$0	$0
Engineering Time (Man Weeks @ $2K/MW)	4	0	0	0	0	0
Device Test Program Generation (Man Weeks @ $2K/MW)	2	0	0	0	0	0
Design Change Iterations	1	1	1	1	1	1
NRE Cost / Iteration	$5,000	$0	$0	$0	$0	$100
Cost of Design Iteration	$5,000	$0	$0	$0	$0	$100
Engineering Time (Man Weeks @ $2K/MW)	2	0.5	0.5	0.5	0.5	0.5
Programming Equipment Cost	$0	$395	$5,000	$2,000	$5,500	$5,000
TOTAL FIXED COSTS	$69,000	$11,785	$16,390	$17,000	$25,450	$24,790
OPPORTUNITY COST						
TTM Cost/Day	$25,000	$25,000	$25,000	$25,000	$25,000	$25,000
Days for Silicon Turns	20	0.5	1	1	1	1
TOTAL OPPORTUNITY COST	$500,000	$12,500	$25,000	$25,000	$25,000	$25,000
VARIABLE COSTS						
Unit Price	$50	$125	$100	$100	$100	$100
Support Chip Cost	$0	$0	$0	$2	$0	$0
Number of Units / Board	3	3	3	3	3	3
Number of Boards	100	100	100	100	100	100
Total Device Cost	$15,000	$37,500	$30,000	$30,600	$30,000	$30,000
Inventory Cost / Item	$1,000	$1,000	$1,000	$1,000	$1,000	$1,000
Number of Items	3	1	1	1	1	1
Total Inventory Cost	$3,000	$1,000	$1,000	$1,000	$1,000	$1,000
%Programming Yield	n/a	100%	100%	100%	98%	95%
Adminstrative and Reprogramming Cost Factor	n/a	1.20	1.20	1.20	1.50	2.00
Cost of Programming Yield Lost	$0	$0	$0	$0	$918	$3,158
%Functional Yield	95%	100%	100%	100%	98%	95%
Adminstrative Cost Factor	1.20	1.20	1.20	1.20	1.50	2.00
Cost of Functional Yield Lost	$947	$0	$0	$0	$918	$3,158
%Board Failures	1.00%	0.00%	0.00%	0.00%	0.50%	1.00%
Board Rework Cost Factor	10	0	10	10	10	10
Cost of Board Failures	$1,500	$0	$0	$0	$1,500	$3,000
%System Failures	0.15%	0%	0%	0.00%	0.10%	0.15%
System Repair Cost Factor	100	0	100	100	100	100
Cost of System Failures	$2,250	$0	$0	$0	$3,000	$4,500
TOTAL VARIABLE COSTS	$22,697	$38,500	$31,000	$31,600	$37,337	$44,816
TOTAL COST	$591,697	$62,785	$72,390	$73,600	$87,787	$94,606

Fig 5—Instead of focusing solely on device costs, this spreadsheet format courtesy of Lattice Semiconductor attempts to factor in all the costs of mask-programmed gate arrays and various FPGAs.

rays—two wafers—is being remarkably flexible.

A few FPGA makers offer alternatives to going directly to a mask-programmed gate-array supplier. Whereas most FPGA companies direct you elsewhere for conversion, Altera has written its own logic synthesizer to keep conversion under the company's own roof. This synthesizer will accept FPGA designs created with the company's proprietary design software and generate a mask-programmed gate-array design. In the process, the synthesizer optimizes for timing, making sure the structure of the mask-programmed gate array is adjusted to match the inherently different timing of the FPGA. The company guarantees that the resulting mask-programmed gate array will be an exact, drop-in replacement for the original FPGA. Furthermore, if you use the company's proprietary software to partition your design over multiple FPGAs, the logic synthesizer can coalesce the multiple FPGAs into a single, functionally equivalent mask-programmed gate array.

Who supplies the vectors?

In return for a $15,000 service charge, Altera will deliver prototype mask-programmed gate arrays within five weeks and production quantities in 10 to 12 weeks. The company supplies test vectors, guaranteeing 95% fault coverage for both synchronous and asynchronous designs. Mask-programmed gate-array vendors, on the other hand, prefer that *you* supply a comprehensive set of test vectors.

Although many mask-programmed gate-array vendors will cheerfully take on converting Xilinx designs, Xilinx itself sees its FPGAs as production parts, not as an intermediate step to mask-programmed gate arrays. Consequently, Xilinx does not offer a conversion service like Altera's. Xilinx does have mask-programmed versions of its FPGAs, however. The mask-programmed versions retain the logic blocks of their field-programmable cousins but have hard-wired interconnections where the field-programmable versions have transistor switches. Consequently, the timing of the connections between logic blocks can be significantly different for the same design realized in the two different devices.

Crosspoint is betting the farm on compatibility between FPGAs and mask-programmed gate arrays. The company's FPGAs are structurally the most similar to mask-programmed gate arrays of all currently available FPGAs. Furthermore, the company's $17,000 design software deliberately mimics mask-programmed gate-array software. Even the company's macro libraries are the same as standard mask-programmed gate-array libraries.

Actel, like the remaining FPGA makers, leaves conversion up to mask-programmed gate-array companies such as Gould AMI. Gould

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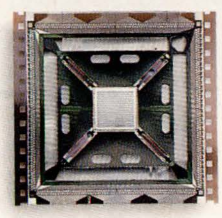

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AMI also sells conversion software for both FPGA and mask-programmed gate-array designers. The company's Netrans software costs \$15,000 and will convert Actel, Altera, or Xilinx FPGAs (each additional FPGA type adds \$5000). The company also converts mask-programmed gate-array designs to FPGAs for a \$3000 to \$8000 service charge, depending on FPGA type.

Most mask-programmed gate-array companies will do a conversion from your FPGA's netlist, but they prefer to work with a completely synchronous design and want a complete set of test vectors. For example, Fujitsu accepts no FPGA conversion without test vectors that achieve a certain level of fault coverage. GEC Plessey, on the other hand, works from a netlist and/or a schematic and can generate test vectors. However, the company does have ground rules it would like you to follow in your FPGA design.

Atmel can take standard programmable-logic JEDEC files for Xilinx, Altera, or Actel FPGAs and map them over to its mask-programmed gate arrays. The company needs functional vectors but can figure the fault coverage for you. The company uses a logic synthesizer to add scannable test circuitry to your design. Hitachi too, starting with your EDIF 2 0 0 netlist, can add test circuitry and generate test vectors. Of course, the extra circuitry results in a larger, more expensive device, and the extra services entail extra service charges. EDN

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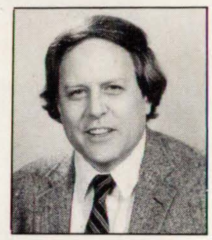

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Manufacturers of FPGAs, mask-programmed gate arrays, and software packages

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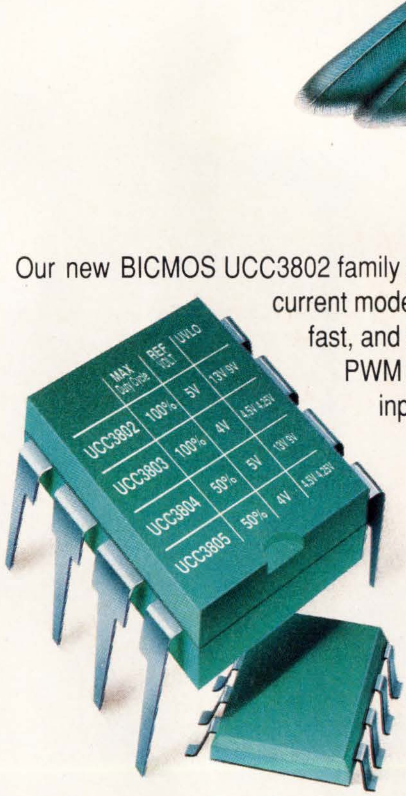

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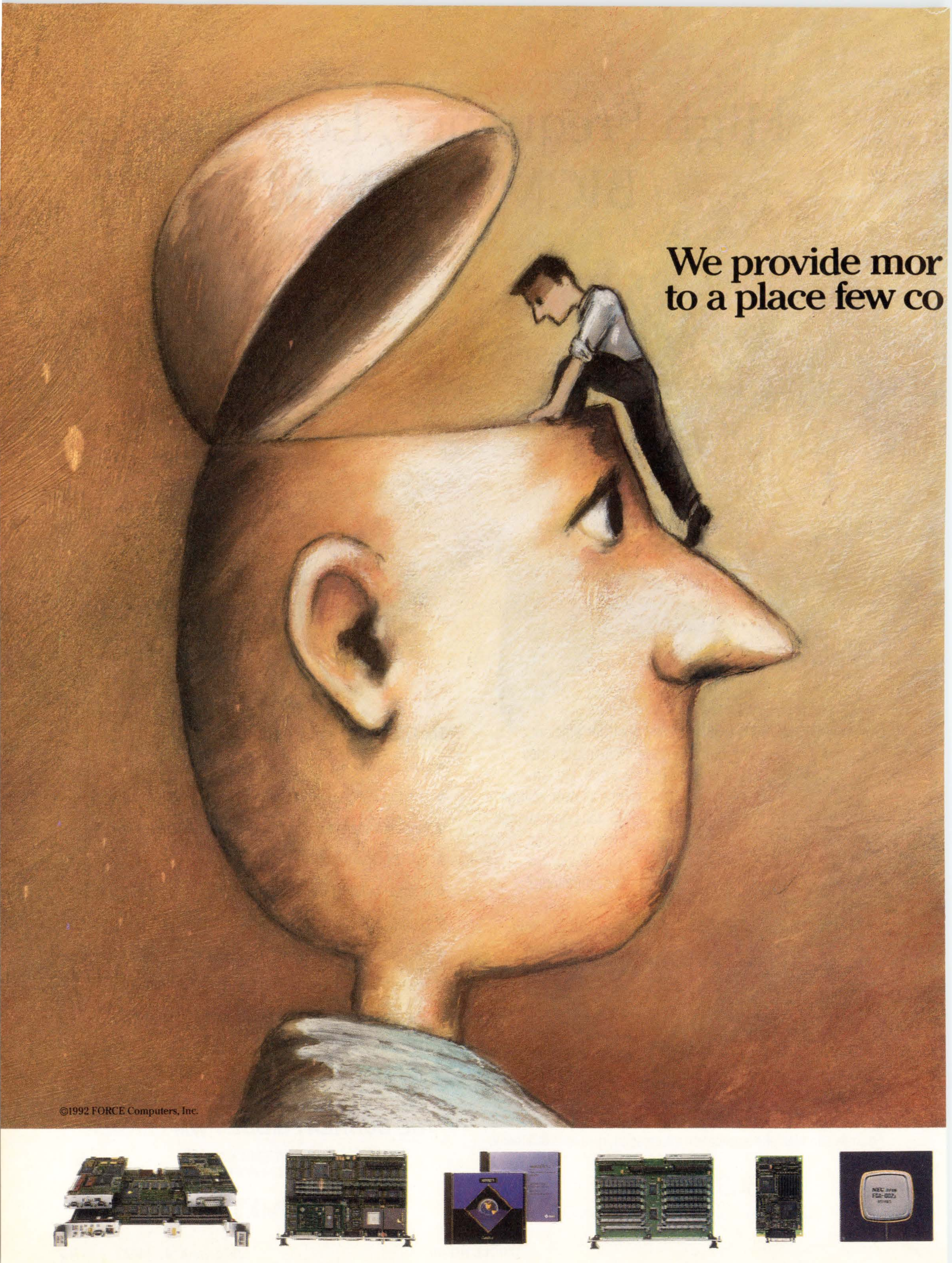
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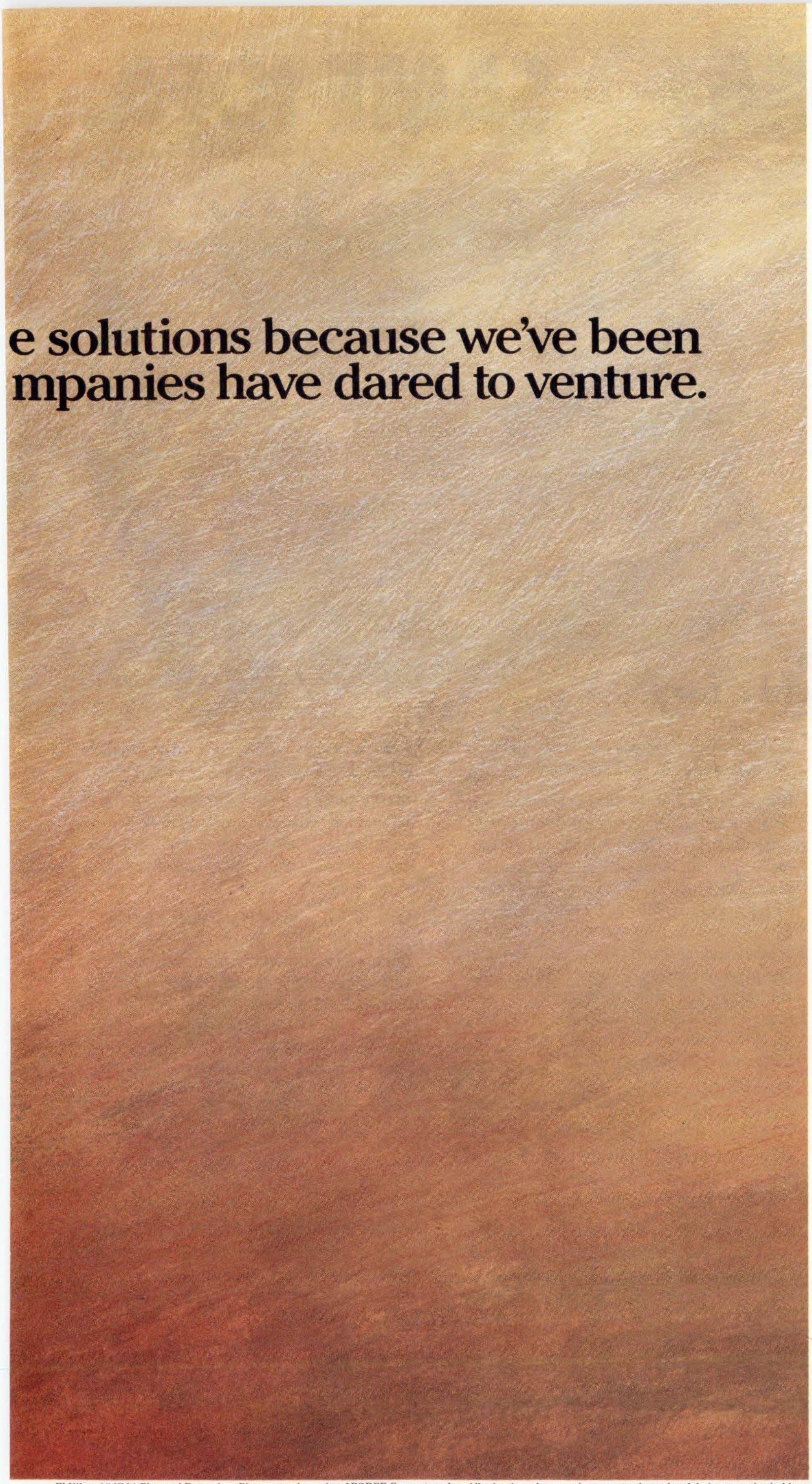

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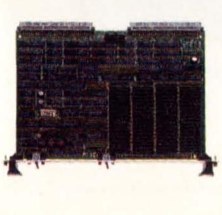
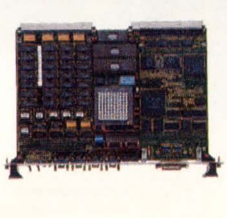


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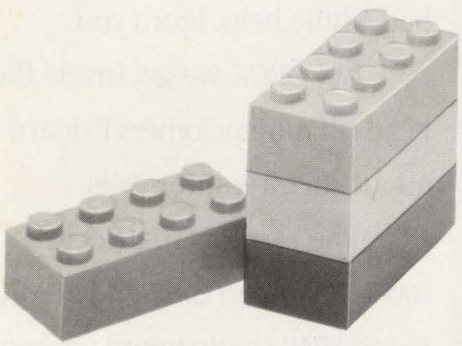

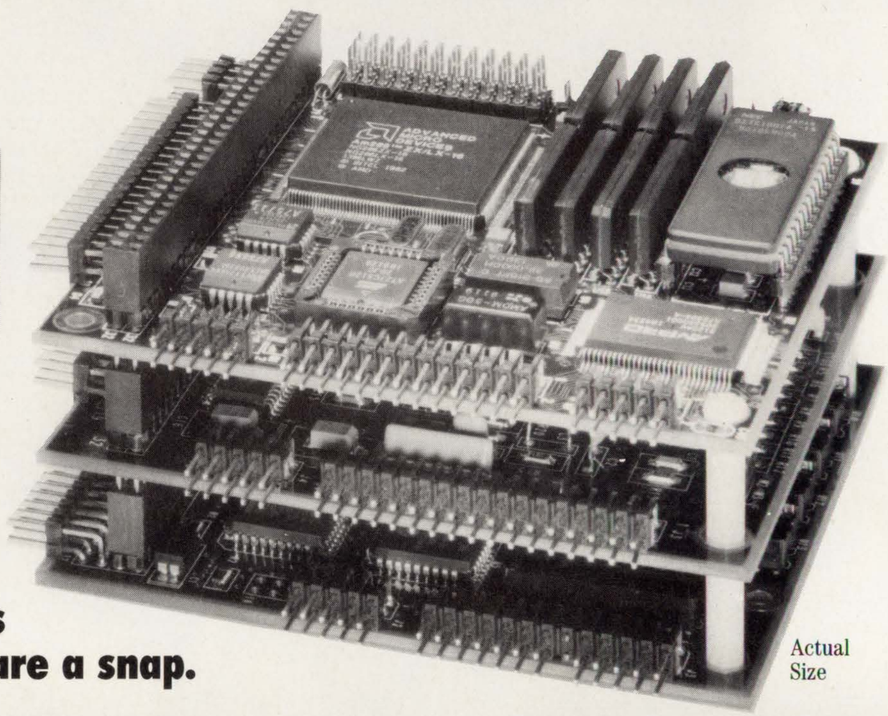

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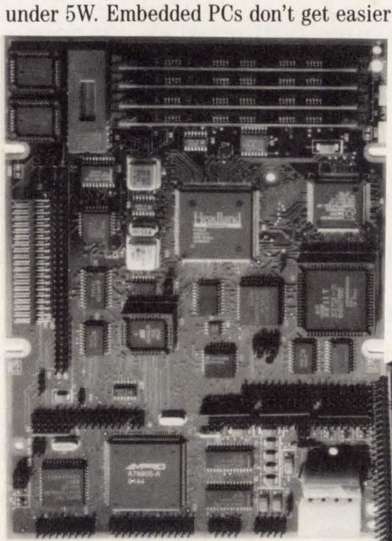

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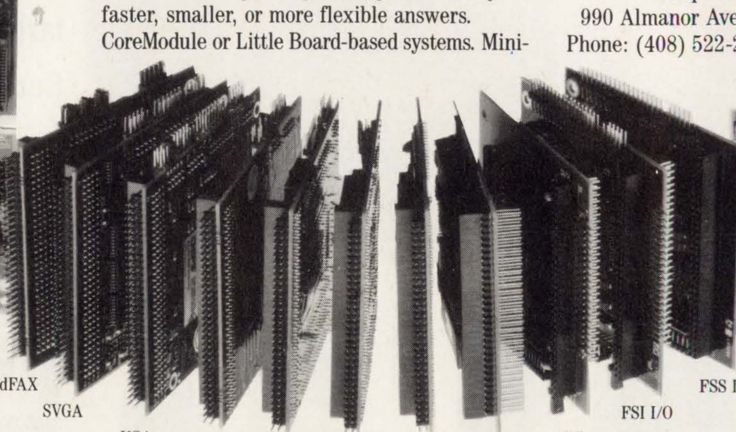

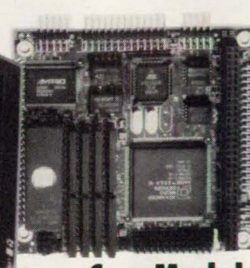

CoreModule
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CIRCLE NO. 81

Team approach improves user interfaces for instruments

Sandra J Grossmann, Gene Lynch, and Mark O Stempski, Tektronix Inc

To create a successful instrument, you must create a successful interface. One way to do that is to take a team design approach that seeks customer input at regular stages of the product design cycle and uses that input to keep the project focused on the user's needs.

In today's marketplace, functional performance specifications are only one of the purchase criteria for corporate electronic-equipment buyers. In an increasingly competitive world market, ease-of-use has become one of the most important considerations. This increased emphasis on usability creates new demands on the traditional design team—demands that are difficult to satisfy without modifying the structure of the traditional design team and the product design methodology. Consider for a moment what's behind this drive for better usability.

With the technological improvements of the last two decades, electronic equipment has become considerably more complex. As a result, users now expect advanced functions, sophisticated measurements, and automated features. Yet these advances in technology have not been matched by advances in human memory or attention span. Compounding the problem is the pressure on today's users to manage more information and solve more complex problems than 20 years ago. Customer demands for more effective user interfaces are a direct result of the increased sophistication of today's instruments.

The challenge for today's product-design team is to tame the underlying complexity of the equipment by strategically layering the user interface, presenting users with only the necessary information and choices at each level. Meeting this challenge requires input from users about their problem-solving strategies and their needs.

It is true, of course, that the customer is seldom the source of design innovation, and any process that depends solely upon customers for innovation is likely to fail. However, the customer is always the source of design validation—either before or after a product hits the marketplace. The key issue is in knowing when and how to integrate customer opinion with the realities of technology.

Redefining the design process

Traditionally, a product development team consisted of hardware and software engineers, with marketing providing filtered information about the customer. Often there was considerable tension between engineering and marketing about design goals or implementation strategies.

The fundamental structure of the traditional product team, therefore, presented a subtle barrier to good user-interface design—it separated the design engineers from the users. Engineering tended to regard the user as an abstraction and consequently presented their design ideas to each other—not to customers—for validation. This isolation from customer input often resulted in ineffective user interfaces.

Few engineers have experience soliciting customer input and analyzing the resultant data, and fewer still can simultaneously perform that role and the role of design engineer. User-interface specialists, however, can add such expertise to the product team. In addition to their experience with customer interactions, interface specialists perform task analysis, experimental design, statistical analysis, human behavior modeling, and system abstraction. Usually, they have an advanced degree in human factors, computer science, industrial engineering, psychology, or a combination of degrees.

The user-interface specialist mainly studies customers one by one, drawing conclusions about customers in general. Marketing's approach is to study the marketplace and draw conclusions about individual customers. Both perspectives are essential for a focused, strategic product development, so both are included in the product team.

Customer contact isn't limited to marketing and the user-interface specialist, though. As shown in **Table 1**, the project team's engineers are involved in customer interviews early in the project and interact with them throughout the product-development cycle. In this way, the customer is actually incorporated into the project. Redefining the team removes barriers to customer input, which leads to improved interface designs and reduced tension within the team. And, all members of the team have direct access to customers and each other.

Accompanying the changes to the team's composition are changes to the design process itself. The new design methodology has two goals—decrease the time, effort, and complexity involved in product development by implementing a proven solution and increase sales by building a customer-proven product.

Table 1—Design-team responsibilities

	Responsibilities	
Phase	**Coordinators**	**Contributors**
Product idea	Marketing, engineering	Industrial design, user-interface specialist, and customers
Customer interviews	User-interface specialist, marketing	Engineering, customers
Major specifications and logical groupings	Project leader	Engineering, user-interface specialist, marketing and customers
Initial product design and usability goals	Project leader	Engineering, user-interface specialist, marketing, and industrial design
"Conceptual walk through"	User-interface specialist	Engineering, marketing
Simulation	User-interface specialist	Engineering, industrial design, marketing, and customers
Functional specification (including usability goals)	Engineering	Marketing, user-interface specialist
Iterative product design and testing	Engineering, user-interface specialist	Marketing, customers
Beta-site verification	User-interface specialist, marketing	Engineering, customers

The new design process specifies milestones for customer involvement, uses customer preferences to guide product specification and functional groupings within the product, and incorporates the notion of evolving design and customer feedback into the actual product plan. This approach enhances and complements current design methodologies.

Itemizing the process

To create an effective interface, you must have customer input. You must let the customers describe the types of problems they are trying to solve and the way they want to solve those problems. In addition, you must listen to any constraints that they feel will hinder their problem-solving ability. The product team must hear the customers' ideas before they can design a product to fit the customers' needs. This is especially true of the user interface.

The user interface is, after all, the window to an instrument's capabilities. If customers cannot effectively navigate through the interface, you have a poorly designed instrument regardless of how much functionality it might contain. The first step in structuring a successful product, therefore, is to meet with representative users.

Although some companies rely on market-research firms to learn about customer preferences, others find it more productive to complement these methods with direct, in-depth customer interactions. The direct approach provides detailed, specific information at a modest cost.

The results of interviewing customers are most helpful for the next step in the interface design—developing the instrument's feature set. Members of the product team use tools such as customer interviews and surveys to gather input about requested features and capabilities. Combining their technical knowledge with customer input, the team members propose and present a feature set for the product to the entire product team. The feature set includes traditional specifications (for example, input impedance, accuracy, resolution, frequency range), statements about input, output, and display technology, definitions and descriptions of new technology, and product features. The feature set does not include any organizing principles about menu layout or front-panel arrangement—it simply establishes the basic functionality for the instrument.

Once the project team establishes the feature set, they must then organize a method of presenting instrument features and operations to the user. At this point, the team's most immediate concern is ranking the relative importance of the operations from the user's point of view. Once the operations are ranked according to perceived importance, the natural structure of the interface becomes more apparent. The project leader assigns the user-interface specialist, and at least one other team member, to establish this ranking.

Putting things in order

To establish a ranking, team members first compile a list of the features and operations. The user-interface specialist then works with representative customers to gain their perspective on ranking and other concerns. Customer input is then combined with any previously gathered data and the team's technical knowledge. A hierarchy emerges, with each operation classified as either essential, important, occasionally required, or specialized. **Table 2** shows how the relative importance of the operation determines the optimal type of access.

After the operations are grouped and classified, the user-interface specialist verifies the results with representative customers. After incorporating any necessary changes, the groupings of **Table 2** are presented to the entire product team. The groupings provide the basis for proposing usability metrics and for designing the interface.

Many companies include engineering metrics in their projects' design specifications. However, writing usability metrics into the specification ensures that the user interface is accorded the same rigorous examination as all other parts of the system. In most cases, usability metrics are targeted at those operations that the customer has classified as essential.

For example, many customers indicate that setting an oscilloscope's trigger level is an essential operation, and appropriate information should be available immediately. A usability metric for that operation might be stated as "On first use of the instrument, Level II technicians can acquire test waveform 3 and stabilize the signal by adjusting the trigger level within 1 minute of attaching the probe." Note that the metric specifies the test condition, type of user, stimulus, and operation along with a quantitative limit that defines whether the metric is met or not.

The customer's perceived importance of the operations, along with the usability metrics, help determine the basic structure for the user interface. At this point, the product team understands the type of access that the customer must have for each of the operations. However, the interrelationships between the operations have not been defined. The user-interface specialist can design and conduct a short experiment to discover which operations customers group together as related items. Alternatively, the product team can go through the same grouping exercise. The user-interface specialist can submit those groupings to customers for verification.

When the basic groupings are established, it is important to bring in an industrial designer as a consultant to provide aesthetic input and ergonomic expertise. The industrial designer works in concert with the product team to produce a mockup of the physical instrument. Part of the team works in parallel on menu structure and also calls upon the industrial designer for help in aesthetically arranging the basic menu display and creating mockups of the displays for discussion.

Conducting a conceptual walkthrough

Once the team proposes an initial design, it is time to use the product in representative tasks. Obviously, the product doesn't exist yet, but the entire product team needs to step through basic operations in the same way that customers would use the product. This process of formally stepping through representative tasks is termed a conceptual walkthrough.

During the walkthrough, the user-interface specialist presents each task. One of the design engineers shows, step-by-step, the actions required to complete the task,

Table 2—Operations and their required access

Relative importance	Ease of use required	Access
Essential (Example: setting trigger level on an oscilloscope.)	**Intuitive** Operation is obvious and customers can use it automatically.	**Immediate** (Example: dedicated front-panel knob.)
Important (Example: storing a digitized waveform on an oscilloscope.)	**Discoverable** Operation is clear and customers can easily locate it with minimal thought. When customers have located the feature, operation becomes automatic.	**Convenient** (Example: first-level menu.)
Occasionally required (Example: running diagnostics.)	**Discoverable** (See above.)	**Readily available** (Example: second-level menu.)
Specialized (Example: calibrating signal-path compensation.)	**Learnable** Operation is sensible and customers can locate it with the aid of on-line help or through limited exploration. When customers have located and used the function, operation is easily recalled.	**Available and recallable** (Example: third-level menu.)

using the physical mockups provided by the industrial designer. The walkthrough has a number of advantages. First, it lets the entire product team understand the instrument from a user's point of view. The walkthrough also identifies terminology and operation ambiguities and reveals and clarifies any misunderstandings of software and hardware interactions. Finally, the walkthrough provides the design team with a yardstick of customer requirements; the team can use this information to evaluate the instrument design prior to expending significant engineering effort.

Simulating the interface

Once the initial concept for the interface is proposed, and the conceptual walkthrough is satisfactory, it's time to test the design with customers. This is a crucial step in the product-design process. The strategy is to confirm the soundness of the overall design before investing significant time and money in development. Instead of building a complete working model of the system, the user-interface specialist or the software engineer simulates the way the instrument responds to user input.

With the simulation, the design team examines navigational and task-oriented performance issues. Are the basic front-panel controls grouped correctly and clearly? Can customers perform each of the essential and important operations? Do design innovations actually improve customer performance?

When team members feel they have addressed all issues, they begin a test of the simulated interface. The user-interface specialist prepares a scenario of likely tasks that customers would perform with the instrument, and goes through the set of tasks with another member of the product team. At a minimum, the scenario should include each of the operations that were classified as essential or important. When consensus is reached that the task set is reasonable and that the user-interface specialist understands the correct solutions for each task, testing begins.

Bring the customer on board

A number of manufacturers use a technique called directed dialogue when interacting with customers at this testing stage. The directed-dialogue technique involves a customer and an experimenter. The experimenter (usually the user-interface specialist) presents a scenario of tasks to the customer, and the customer completes the tasks by using the simulation and mockup as if they constituted an actual instrument. When the customer encounters difficulty in completing a task, the experimenter probes for information. For example, if the customer pushed the wrong menu button, the experimenter might ask "What should have happened when you pressed that?" The customer's response provides clues about his or her ideas about the instrument.

The experimenter conducts tests of the simulation with six to 12 customers, videotaping each session for later analysis. After analyzing the tapes and synthesizing the information, the experimenter presents results to the product team along with recommendations for fixing any problems. Excerpts from the video tapes are often helpful in explaining to the team the types of problems users had with the design.

Issuing the user-interface specification

The product team can now issue a formal user-interface specification. It is often convenient and advisable to refer to the simulation within the specification, since many complex interactions are best understood when viewed dynamically. The specification is the definition of the product and is a necessary component in the design process. If a process or feature is not explained in the specification, it will be problematic. In the absence of a stated model, individual interpretations will differ.

As instrument design progresses, innovations as well as implementation difficulties surface that require additions or changes to the specification. When a number of additions or changes affect the user interface, it is advisable to build and test another simulation to ensure that the proposed changes are advantageous or acceptable to the customer.

Simulations also simplify the task of choosing between two good design alternatives. For example, in many design meetings, two or more engineers may have strong, substantially different ideas about how to implement a certain innovative feature. Rather than tie up the entire team in an argument of relative advantages, the project leader can assign the problem to the user-interface specialist. The specialist builds two simulations to represent the two design models, and runs a brief experiment that tests the feature. One of the implementations will likely end up creating the least amount of difficulties for customers. In the final analysis, the customer arbitrates the design decision.

Verifying the design at the beta site

When prototypes become available, it is important to verify the user-interface design at an actual customer site. While the simulations help resolve design issues, beta-site testing actually uses the design in real-life settings. For best results, beta-site testing should include a learnability test, an extended-use period, and a usability test.

INSTRUMENT INTERFACES

The user-interface specialist conducts the learnability test on-site when dropping off the instrument. The learnability test measures how accessible the instrument is and how easy a customer can learn its basic operations. The videotaped test includes the task scenarios developed for the simulation tests.

During the extended-use period, the customer agrees to use the instrument for at least one hour each day. This period lets the customer thoroughly explore the instrument and use it in the context of everyday work. The customer fills out a logbook for each day, describing the type of work performed and any surprises or difficulties encountered. The customer has technical support available via telephone, and the user-interface specialist calls the customer occasionally during the extended-use period. For extremely complex systems, one of the product engineers stays at the customer site during the entire period.

The user-interface specialist conducts the usability test on site when picking up the instrument. This test measures how automatic the customer's basic use of the instrument has become and how well the customer can use the instrument to solve complex problems. The test contains more involved and specialized tasks than the learnability test. During this phase, it is also advisable to have the customer demonstrate any problematic operations. The user-interface specialist videotapes both the usability test and the customer demonstration.

When the user-interface specialist picks up the beta-site instrument, the customer fills out a survey. In the survey, the customer indicates the frequency of feature usage and his feelings about instrument performance. The customer also lists desired changes or additions in instrument design. The data gathered at the beta site helps the product team identify any remaining bugs and lets management schedule enhancements for future releases. EDN

Authors' biographies

Sandra J Grossmann is a human-factors engineer at the Software Technology Research Lab of Tektronix Inc (Beaverton, OR). A user-interface specialist, Sandra consults with product groups, investigates user-interface issues for proposed products, conducts research on task analysis and user preferences, and develops methodologies for incorporating users into the design process. She has a BA from Metropolitan State College, has studied mechanical engineering at Portland State University, and is currently working on an MS in Applied Psychology.

Gene Lynch is a principal scientist in the Software Technology Research Lab at Tektronix. Gene manages the user-interface research group and consults with design teams on product concepts and user interfaces. Gene has a BS, MS, and PhD in engineering science from the University of Notre Dame.

Mark O Stempski is a senior scientist in the Software Technology Research Lab at Tektronix. Mark designs, develops, prototypes, and tests user interfaces for test and measurement instruments. He has a BA from Metropolitan State College and an MA and PhD from the University of Arizona.

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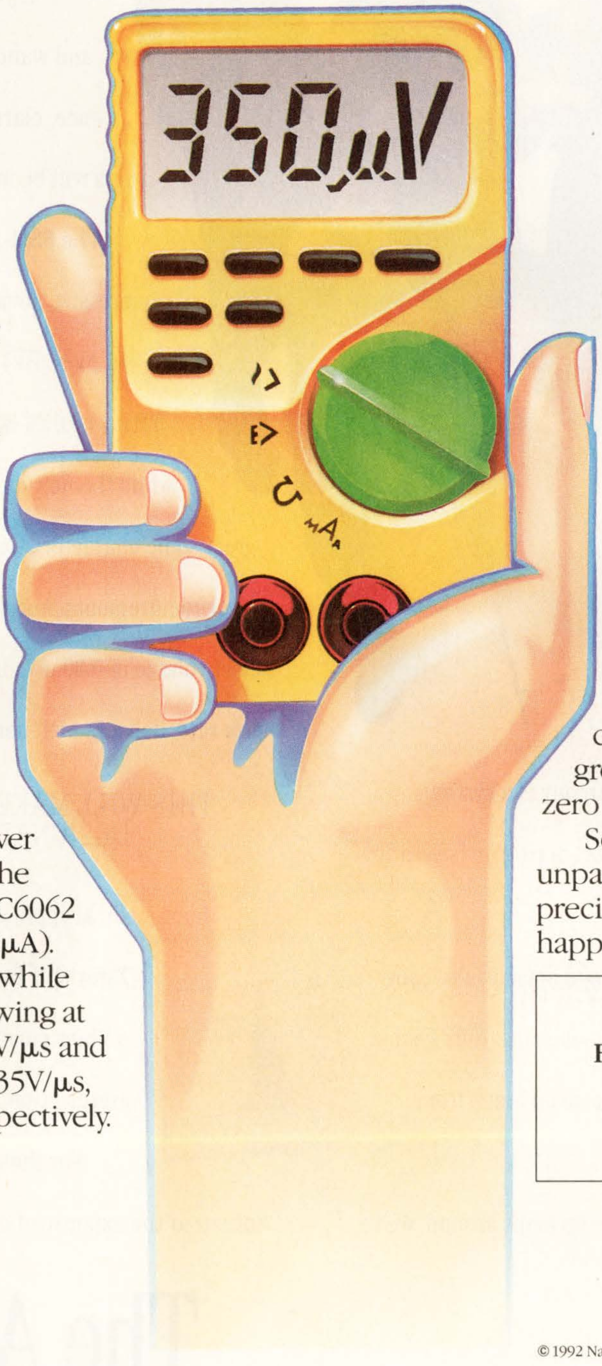

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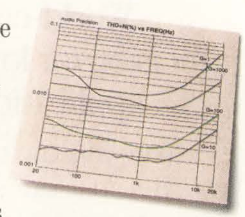

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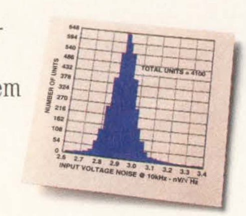

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AD743/745	3.2	6.9	0.5	8	250 pA	2.8/12.5
OP-275 (dual)	6	1500	1	4	350 nA	22
AD645	9	0.6	0.25	3	1.5 pA	2.0
AD712 (dual)	18	0.01	0.7	5	75 pA	20
AD548/648 (dual)	30	1.8	0.25/0.3	.34	10 pA	1.8
AD549	35	0.11	0.5	.60	60 fA	3

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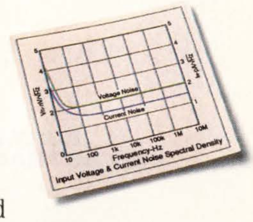

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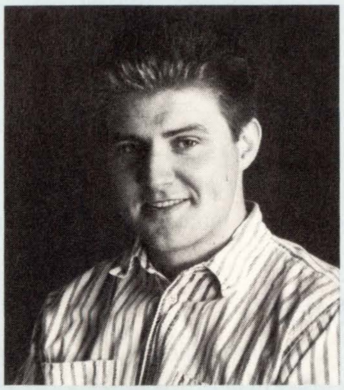
CIRCLE NO. 77

Teamwork pays off for Design Ideas Grand Prize winners



Mark Murphy

Moshe Gerstenhaber

You don't need a partner to win the annual Design Ideas Grand Prize, but it doesn't hurt. Moshe Gerstenhaber of Analog Devices (Wilmington, MA) has been teaming up with different partners to submit design ideas to EDN for 10 years. Now, he and colleague Mark Murphy have won the 1991 Design Ideas Grand Prize of $1500 for "Synchronous system measures μΩs" (EDN, May 9, 1991, pg 175).

"It's a great honor," said Gerstenhaber. "There's a message there [in winning the prize] that you worked hard and earned it." He and Murphy are looking forward to the recognition the award will bring them. Gerstenhaber says that engineers read Design Ideas religiously.

Murphy agrees. "Design Ideas has got to be the most-read part of the magazine." They both thought about winning the prize, but, as Murphy says, "you never expect to win it." Murphy adds, "Moshe thought the idea was great. Actually, it was his idea." Gerstenhaber returns the compliment: "He's the handsomer of the bunch."

In the Design Ideas circuit, a synchronous-detection scheme measures low-level resistances. As Design Ideas Editor Charles H Small described it, other low-resistance-measuring circuits can introduce unacceptably large currents into the system under test. The prize-winning circuit synchronously demodulates the voltage drop across the system under test and can therefore use extremely low currents while measuring resistance. So the idea might be applied to situations where the resistances to be measured are as low as those found in superconducting devices.

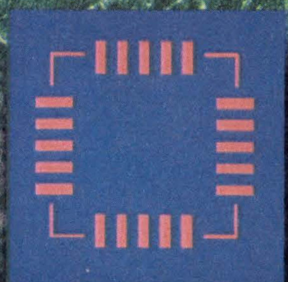
The two winners will split the prize money, but Murphy says "the money is unimportant. We still would have done it without [the possibility of] the money. The money isn't even secondary." On the other hand, he adds, "Hopefully we'll win it again some year . . . I think I'll go to Disneyland now."

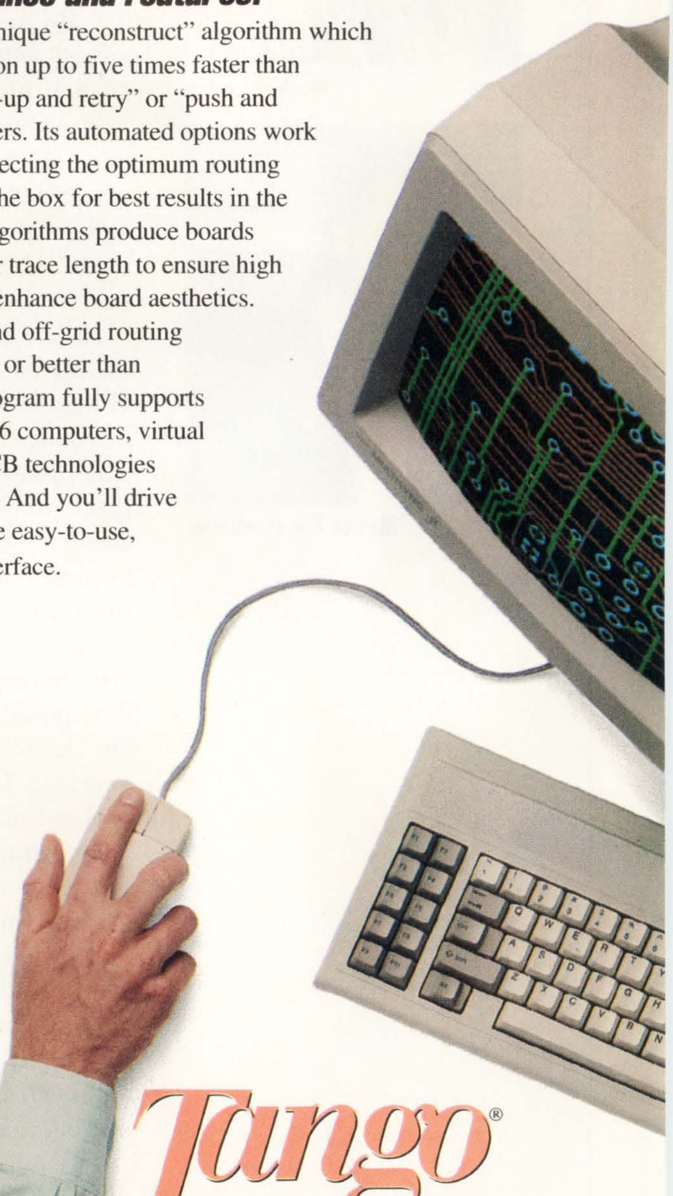
Gerstenhaber came to this country from Israel after the 1973 Arab-Israeli War. He graduated from Rensselaer Polytechnic Institute and has been with Analog Devices for 14 years. He started there as a designer, moved to product engineer, and now is a product engineering manager responsible for 17 people. He is married and has three children. He enjoys playing soothing classical music on his piano.

Murphy came to Analog Devices four years ago from Ireland and is an amplifier designer. His outside interests include rowing, soccer, and beer brewing.

Brian Tobey
Production Editor

Design Ideas are continued on pg 143





Simple filter quiets power line

James Wong, Analog Devices, Santa Clara, CA

Using the simple filter in **Fig 1** and some sensible connection techniques, you can clean up a 5V digital-logic rail enough to power analog circuitry. The noisiest place in a digital-logic system is right around the digital circuitry. Therefore, you should tap off your analog supply as close as possible to the 5V power supply's terminals. The supply's low-impedance terminals will cancel most of the nanosecond-wide current spikes from the digital logic. The filter will cancel any residual noise. Garden-variety capacitors will suppress glitch noise down to less than a couple of millivolts. For high-precision applications, low-ESR (effective series resistance) capacitors filter even more effectively.
EDN BBS /DI_SIG #1132

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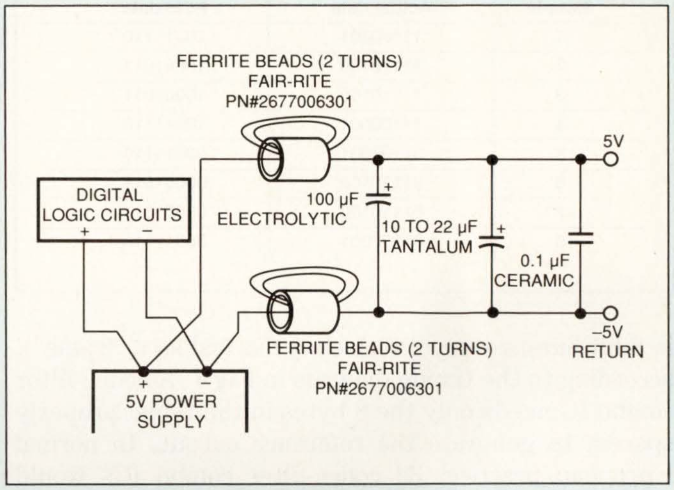

Fig 1—This simple filter will cut the noise on digital-logic power lines down to less than a couple of millivolts, allowing you to power sensitive analog circuitry.

Test pattern calibrates codecs

Patrick L McGuire, Dianatel Corp, Santa Clara, CA

The test pattern in **Table 1** is an 8-bit PCM sequence that, when applied to a codec-filter combo IC's digital input at 8000 sample/sec, will produce an analog 1-kHz sine wave having an output amplitude of 0 dBm (774.6 mV rms into 600Ω). **Fig 1** shows a ripple counter driving a 16R6 PAL. The PALASM program in **Listing 1** will program the PAL to produce the proper bit sequences and timing signals. The **listing** is also available on the EDN BBS.

The PAL outputs the 8 bytes of test pattern in **Table 1**

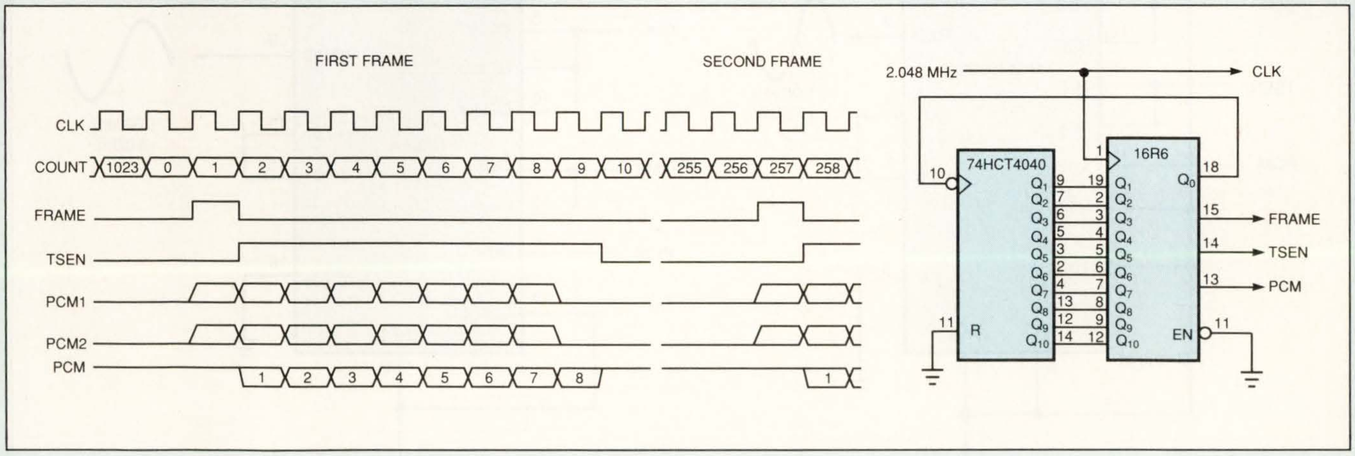

Fig 1—The PAL decodes the output of the ripple counter to produce a burst of eight bytes, during the proper time-multiplexed "frame," that a codec-filter combo IC can convert into a reference 1-kHz, 0-dBm analog output. Refer to Listing 1 for the definition of some of the signals in the timing diagram.

Table 1—Codec-filter IC test pattern

Sample	Actual data	PCM data
1	11100001	10011110
2	11110100	10001011
3	11110100	10001011
4	11100001	10011110
5	01100001	00011110
6	01110100	00001011
7	01110100	00001011
8	01100001	00011110

in 8-bit bursts every 256 clock cycles (called a "frame"), according to the timing diagram in **Fig 1**. A codec-filter combo IC needs only the 8 bytes in the table, properly spaced, to generate the reference output. In normal European practice, 32 codec-filter combo ICs would be looking at the same time-multiplexed input stream. Each codec-filter combo IC would pick off the appropriate 8 bits from the stream, demultiplexing the input stream and converting one signal from digital to analog. But in this test setup, only one codec-filter IC is present. Therefore, the PAL only has to output data 1/32 of the time.

Fig 2 shows two test circuits for codec-filter combo ICs using different timing schemes.

EDN BBS /DI_SIG #1133

To Vote For This Design, Circle No. 747

Listing 1—Digital-milliwatt PALASM program

```
TITLE           Digital mW PAL
PATTERN         DMW
REVISION        1.0
AUTHOR          P.L.McGuire
COMPANY         Dianatel
DATE            30 November 1991

CHIP            DMW PAL16R6

;       1       2       3       4       5       6       7       8
        CLK     Q2      Q3      Q4      Q5      Q6      Q7      Q8

;       9       10      11      12      13      14      15      16
        Q9      GND     /OE     Q10     PCM     TSEN    FRAME   /PCM2

;       17      18      19      20
        /PCM1   Q0      Q1      VCC

; CLK is 2.048 MHz; it also drives the various CODEC clock inputs.

; Q0 is the LSB of the frame counter; it drives the external ripple
; counter (74HCT4040) clock input.

; PCM1 and PCM2 create the digital milliwatt PCM data sequence. They
; are ORed together to produce the PCM signal. The ORing process
; causes a 1-bit time delay which is compensated for by delaying
; the FRAME and TSEN signals. (Inverted PCM is summed and inverted so
; that all 1's, u-Law silence, is output during inactive time slots.)

; FRAME is active for one bit time and goes active just before the
; time slot. TSEN (time slot enable) is active during the time slot.
; Both occur every 125 us.

;                               actual PCM      inverted
;
; Digital Milliwatt sequence:   00011110  -->   11100001
;                               00001011        11110100
; (u-Law)                       00001011        11110100
;                               00011110        11100001
;                               10011110        01100001
;                               10001011        01110100
;                               10001011        01110100
;                               10011110        01100001

STRING  BIT1    '/Q2*/Q1*/Q0'
STRING  BIT2    '/Q2*/Q1*Q0'
STRING  BIT3    '/Q2*Q1*/Q0'
STRING  BIT4    '/Q2*Q1*Q0'
STRING  BIT5    'Q2*/Q1*/Q0'
STRING  BIT6    'Q2*/Q1*Q0'
STRING  BIT7    'Q2*Q1*/Q0'
STRING  BIT8    'Q2*Q1*Q0'

STRING  TSLOT1  '/Q7*/Q6*/Q5*/Q4*/Q3'
STRING  TSLOT2  '/Q7*/Q6*/Q5*/Q4*Q3'

STRING  SAMPLE1 '/Q10*/Q9*/Q8'
STRING  SAMPLE2 '/Q10*/Q9*Q8'
STRING  SAMPLE3 '/Q10*Q9*/Q8'
STRING  SAMPLE4 '/Q10*Q9*Q8'
STRING  SAMPLE5 'Q10*/Q9*/Q8'
STRING  SAMPLE6 'Q10*/Q9*Q8'
STRING  SAMPLE7 'Q10*Q9*/Q8'
STRING  SAMPLE8 'Q10*Q9*Q8'

EQUATIONS

/Q0:=           Q0

PCM1:=          TSLOT1 * ((SAMPLE1+SAMPLE4)*(BIT1+BIT2+BIT3+BIT8) +
                (SAMPLE5+SAMPLE8)*(BIT2+BIT3+BIT8))

PCM2:=          TSLOT1 * ((SAMPLE2+SAMPLE3)*(BIT1+BIT2+BIT3+BIT4+BIT6) +
                (SAMPLE6+SAMPLE7)*(BIT2+BIT3+BIT4+BIT6))

/PCM:=          PCM1+PCM2

/FRAME:=        /(TSLOT1 * BIT1)

/TSEN:=         /(TSLOT1 * (BIT2+BIT3+BIT4+BIT5+BIT6+BIT7+BIT8) +
                TSLOT2 * BIT1)
```

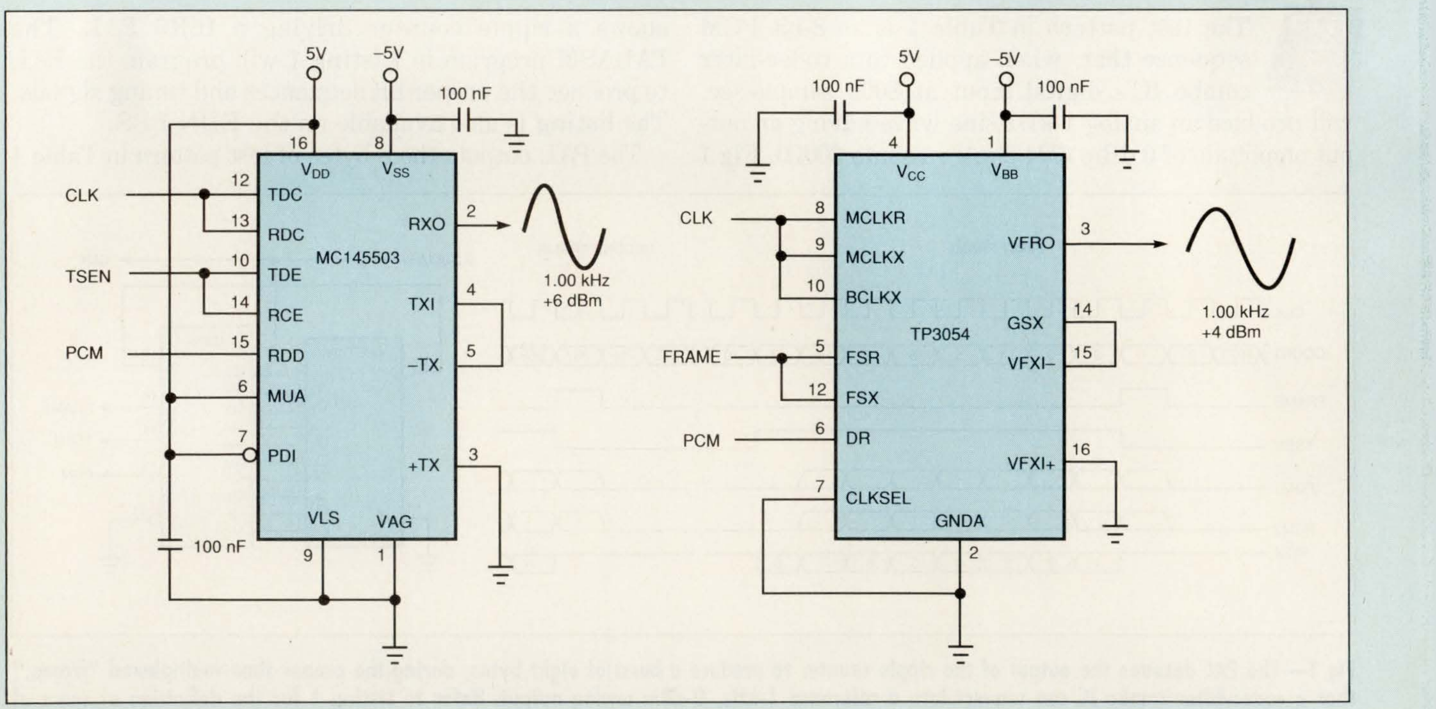

Fig 2—The test circuit in Fig 1 can excite two types of codec-filter combo ICs.

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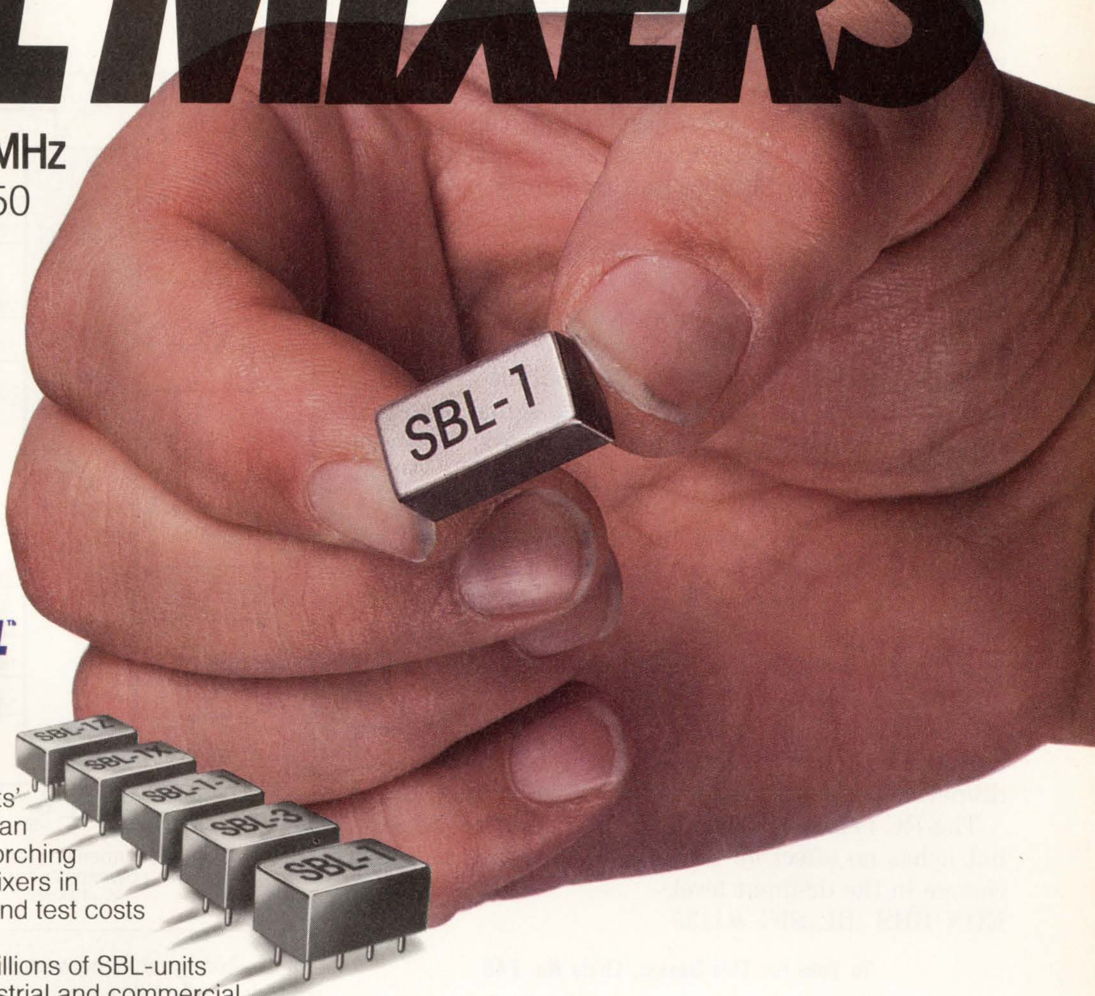

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• SBL-1X	10-1000	6.0	40	40	+7	6.25
SBL-1Z	10-1000	6.5	35	25	+7	7.25
SBL-1-1	0.1-400	5.5	35	40	+7	7.25
SBL-3	0.025-200	5.5	45	40	+7	7.25
• SBL-11	5-2000	7.0	35	30	+7	18.75
SBL-1LH	2-500	5.8	68	45	+10	5.50
SBL-1-1LH	0.2-400	5.2	64	52	+10	8.25
• SBL-1XLH	10-1000	6.0	40	55	+10	7.25
SBL-2LH	5-1000	5.9	61	54	+10	8.25
SBL-3LH	0.07-250	4.9	60	53	+10	8.25
• SBL-11LH	5-2000	7.0	45	30	+10	19.75
SBL-1MH	1-500	5.5	45	40	+13	9.80
SBL-1ZMH	2-1100	6.5	40	25	+13	11.70

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CIRCLE NO. 83

F143 REV. ORIG.

RC network restores dc accuracy

Martin Tomasz, Maxim, Sunnyvale, CA and Rune Domsten, Exatec, Denmark

Adding one more RC network to a lowpass filter restores perfect dc accuracy. Without such an added network, the filter in **Fig 1**, for example, would have an offset of about 50 mV.

To adapt the technique to your circuit, choose values for R and C that determine a pole frequency three decades below the filter's cutoff frequency, f_C:

$$\frac{1}{2\pi RC} = f_C/1000.$$

You can buffer the RC network's output with a low-offset op amp, if desired.

At dc and low frequencies, the output tracks the unfiltered input because R provides a signal path that bypasses the filter. At higher frequencies, C begins to conduct, allowing the output to track the filter's lowpass output (LPO).

Provided the lowpass filter has unity gain and low ripple, the RC network has virtually no effect on the filter's gain or phase response; the input signal and lowpass output swing together throughout most of the passband. The RC filter's attenuation is sufficient to maintain the active-lowpass filter's shape for frequencies between f_C and the stopband. At higher frequencies, the RC network sets the filter's rolloff rate at 20 dB/decade.

The RC network slows the nulling of offsets to zero, but it has no effect on the circuit's response to a step change in the dc-input level.

EDN BBS /DI_SIG #1135

To Vote For This Design, Circle No. 748

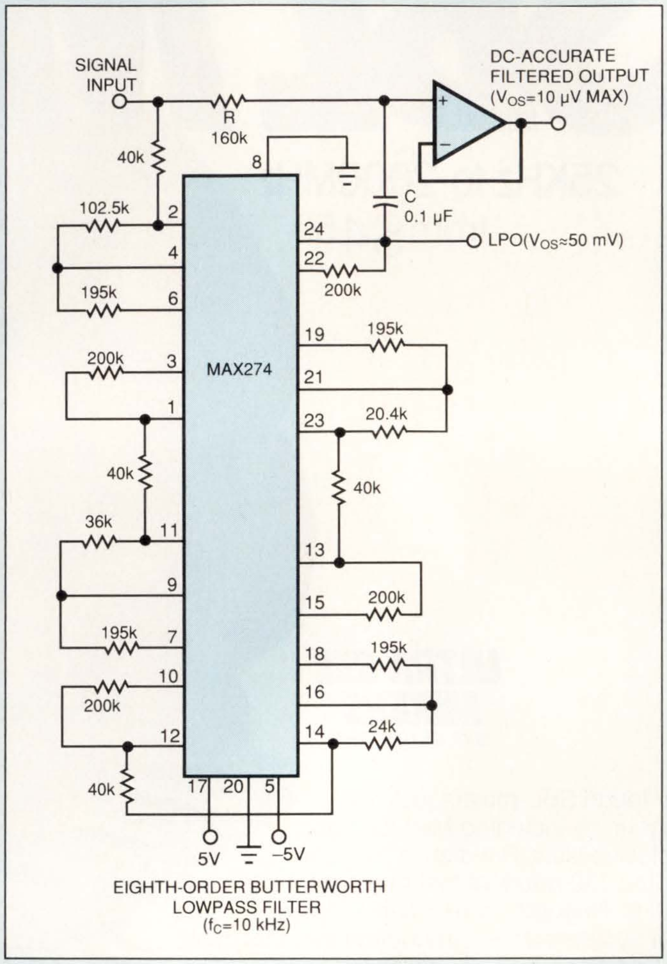


Fig 1—Adding an RC network to a lowpass filter removes offsets, restoring perfect dc accuracy.

PROM state machine decodes data

Dmitrii A Loukianov, Academy of Science, Moscow, Russia

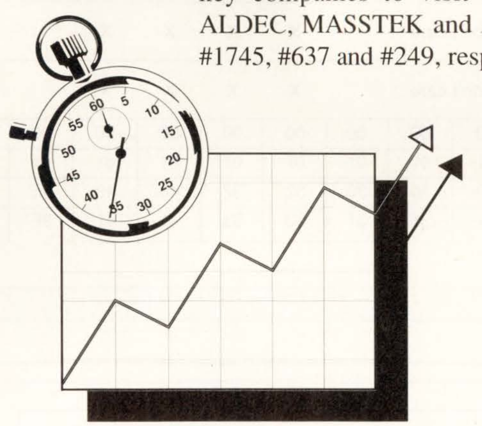
Cypress Semiconductor's CY7C225/235/245 (0.5-/1-/2-kbyte) registered PROMs are fast enough to function as microcoded sequence generators or finite state machines. You must feed back an output to its same row or column decoders' input if you want maximum speed.

Fig 1 shows a registered PROM functioning as a digital phase-locked loop (PLL) that decodes a Manchester-II data stream. **Table 1** shows the PROM's program. When you apply power, the PROM comes up in state HUNT PAGE. The PROM state machine goes through state HUNT END to the SYNCH states

CAE Technology Report

NEW CAE PRODUCTS SAVE TIME

To save on design time, the CAE industry is now promoting the Real-Time (electronic) Breadboarding Machine or RTBM™. The RTBM is a schematic capture that also works like a hardware breadboard. Each time the user enters a new gate or flip-flop on the schematic, that IC instantly outputs signals. The major benefit of this technology is that the user is automatically warned about all timing problems as the circuit is drawn, and not weeks later, during the verification phase. Combining the design entry and design verification phases into one operation saves over 80% of the design time and makes work much easier. The first industrial implementation of this time saving product will be shown at the DAC conference by ALDEC Co. (Booth #1745). **CIRCLE NO. 11**



IF CUTTING DESIGN TIME IS AN ISSUE...

With the latest CAE tools, the user can cut design time to less than 20%. First, the user can create a perfect electronic design breadboard within seconds, saving weeks of the hardware breadboarding. Second, the user can dynamically partition the design into manageable pieces with an electronic "exacto-knife" that operates with microsecond speed. Third, if any circuit output does not "look right", the user can instantly correct it on the screen and then resimulate the entire design with the hand-corrected output waveform. This eliminates a need for design modifications till the desired circuit output is confirmed. A typical example of such a design environment is SUSIE™ simulator from ALDEC. **CIRCLE NO. 12**

TOP CAE VENDORS GATHER TOGETHER

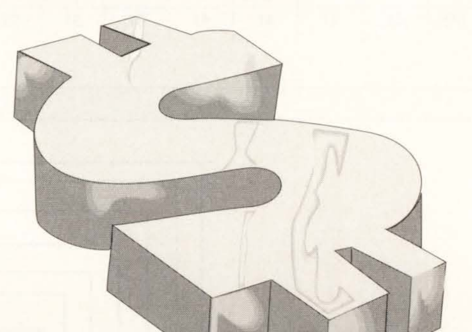
The 29th Design Automation Conference (DAC) is taking place in Anaheim, California (June 8 - June 11, 1992). Smart buyers will be looking for means to cut design time and improve product quality at the lowest cost. For this reason, Windows 3.1 based products will be the theme of the conference. They offer high resolution graphics, excellent speed and superb user interfaces at the lowest prices. The key companies to visit at DAC are ALDEC, MASSTEK and ALS (Booths #1745, #637 and #249, respectively).

BEST CAE CHOICES

Only two years ago PC-based CAE products were viewed by corporate gurus as toys. With the introduction of Windows 3.1, and the new fast 386/486 PCs, the PC-based products perform as well as their RISC-based counterparts, however, at a fraction of the cost. Since the new 100 MIPS ALPHA workstations will operate under Windows NT, a sister to Windows 3.1, the new low-cost Windows 3.1/NT products will outperform the traditional workstation-based products by a wide margin. If anyone wants to make a safe bet and save money in the process, the best choice are products that run under Windows 3.1/NT. They offer a wide selection of hardware platforms from low cost 386 PCs, to the super fast ALPHA workstations. ALDEC, MASSTEK and ALS are the leaders in the Window 3.1/NT-based products. **CIRCLE NO. 13**

LOWEST COST FPGA TOOLS

When the NRE (non-recurring engineering) on ASIC designs was over $100K, paying $50K for a CAE tool was quite acceptable. However, with the FPGA NRE dropping to the $4K to $10K range, new and low cost tools have been developed to serve these applications. Today as a rule-of-thumb, you should pay around $2K for the most advanced, fully automated, multifamily/single chip FPGA simulator. Similarly, you should pay around $7K to $8K for a simulator with unlimited system level design capabilities. Taking advantage of user confusion, some CAE vendors still charge from four to ten times more than a leading brand FPGA simulator may cost. The best buys on the market are highly automated SUSIE logic simulators. Some of them cost less than $2K, yet they simulate Xilinx, Actel, AMD, Altera, etc., designs with top speed and accuracy. **CIRCLE NO. 14**



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when data begins to come in. The SYNCH PAGE state adds or subtracts count steps to keep the state machine in phase with the incoming data. The circuit's 20-MHz clock allows the PROM to track 4-MHz data. If a data transition occurs outside a window that is ±25% of nominal, the PROM transitions through the ERROR REPORT state back to the HUNT states.

The EDN BBS has a packet of files containing **Table 1** along with two more examples of this technique (a digital tester and a stepper-motor controller), an assembler **listing**, and HP-format drawings.

EDN BBS /DI_SIG #1136

To Vote For This Design, Circle No. 749

Table 1—Data-decoding PROM program

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
00:	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	HUNT
01:	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01	01	PAGE
02:	22	44	26	28	2A	2C	2E	30	32	34	36	78	3A	3C	3E	3E	SYNC
03:	23	45	27	29	2B	2D	2F	31	33	35	37	79	3B	3E	3F	3F	PAGE
04:	80	80		X	X	X	X	Don't care			X	X	X	X			ERROR
05:	81	81															REPORT
06:				X	X	X	X	Don't care			X	X	X	X			
07:																	
08:	20	20	00	00	00	00	00	00	00	00	00	00	00	00	00	00	HUNT
09:	21	21	01	01	01	01	01	01	01	01	01	01	01	01	01	01	END
0A:	40	40	40	40	30	30	2E	30	30	30	32	32	40	40	3E	20	SYNC
0B:	41	41	41	41	31	31	2F	31	31	31	33	33	41	41	3F	21	FOUND

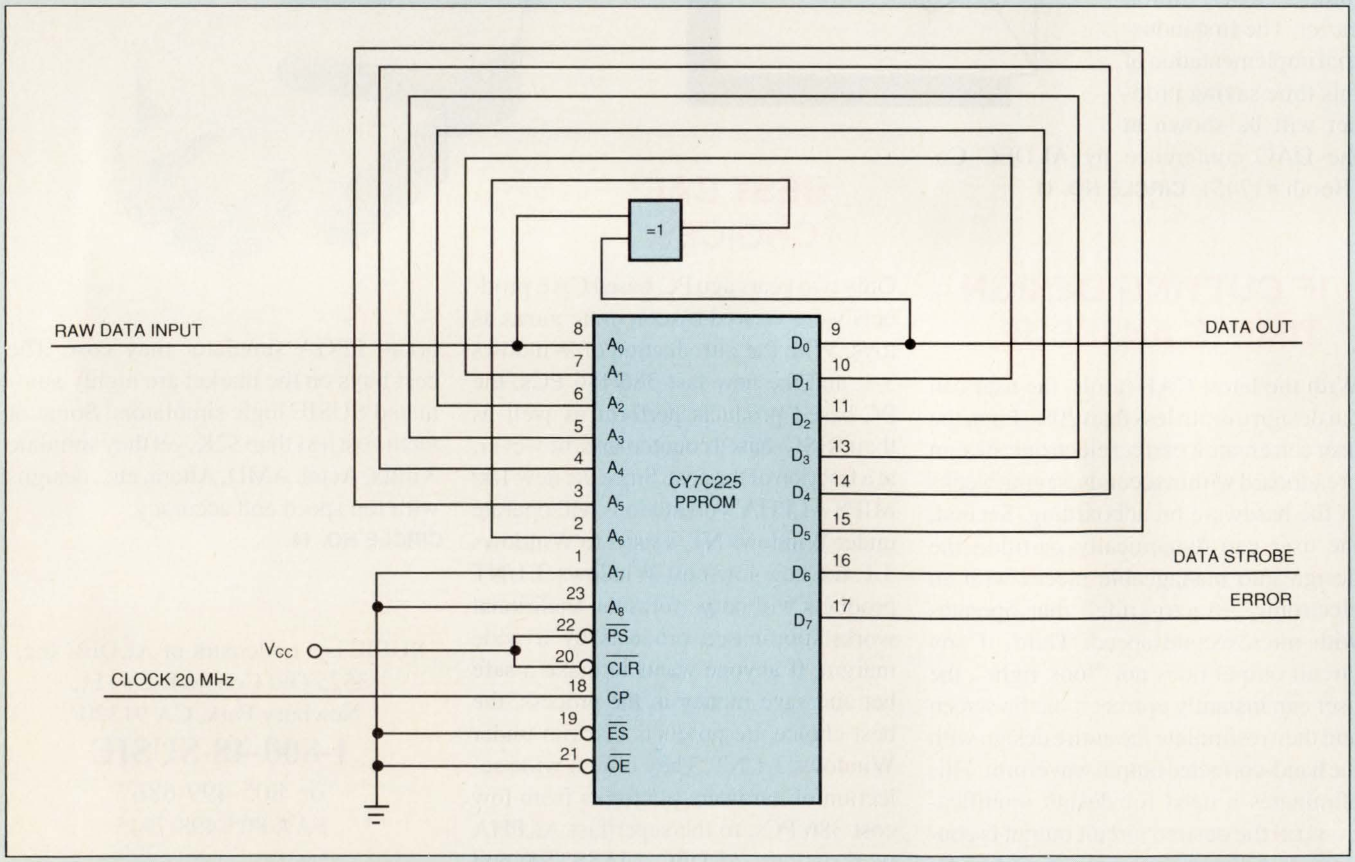

Fig 1—A registered PROM can function as a high-speed finite state machine. Here, the PROM is a phase-locked loop (PLL), operating at 20 MHz, that can decode a 4-MHz Manchester-II data stream.

Feedback & Amplification

Readers question "political correctness"

Why you Americans not put yourselfs first? I read your magazine in University library where in March 2, 1992, column, man from Sweden say everybody equal. Not so in Japan! Japanese will always be better in Japan. If Koreans or others complain, we tell them to go home if not like what Japan offer. In America, when African or Mexican yell the American jumps! America like big dragon with no fire in tongue. Everybody pulls on tail and laughs!

Makeo Sushira
University of Portland
Portland, OR

I have traveled from Northern Europe to Southern Africa. And *everywhere* residents of those countries think that *they* are in some way "superior" to all others (including Americans). The Swedish folk think they are socially "superior" and "more enlightened" than others in matters of sexual liberty (others would call it decadence). My "two cents worth" is that we would be better served sticking to electronics. I thought your original reply to "Name Withheld" was sufficient. Just because someone sends you a letter doesn't mean you have to print it.

Bill Smith
Electronic Design Associates
Box 2162
Vancouver, WA 98668

I believe that Name Withheld is absolutely right (EDN, September 2, 1991). Yes, Americans lived much better and were way better off without these newfangled foreign inventions. As a matter of fact, it is probably an insidious global plot against US to dump all this so-called progress here by bringing ideas or people full of them. Just think how much better life was before A G Bell came out with this noisy, ringing intrusion. And then some Marconi made this wireless. Candlelight was so much nicer, before this Tesla started distributing electricity. And one did not have to be bothered by radio or TV until Sarnoff brought in the dark ages. The transportation modes were peaceful and quiet before Sikorsky raised the noise levels and you Americans got into your Corvettes (Who was Zora-Duntov, anyway?).

Robert Walker
99 Conklintown Rd
Wanaque, NJ 07465

My, my—turning the EDN Design Idea section into a forum for pushing the "politically correct" views of the left-wing Eastern Establishment, are we? I suspect that what NWBR had in mind was that most people consider it an honor to see some of their work published, and that it sure seems strange that what has been up to now basically an American magazine would begin to *honor* and prefer foreigners over their own people. While our politicians have been especially good at doing this during the past decade, who would want to emulate them? I don't think our competitors, the Japanese and Germans, fall all over themselves trying to promote foreign interests over those of their own people.

Actually, the recent unedifying interchange in EDN has changed my view on the whole subject. While before I did not take offense at the occasional idea authored by a foreign engineer, I now think that EDN should print *only* those Design Ideas articles submitted by foreigners. That way, we Americans can mooch off of foreigners for a while, stealing their ideas and manufacturing products using those ideas in Third World countries using slave labor, and, as a result, causing unemployment to increase in the foreign authors' own countries.

Steve Ross
Flight Dynamics
16600 SW 72nd Ave
Portland, OR 97223

Correction

The title of Dana W Davis's "High-voltage regulator has low dropout," EDN, March 16, 1992, p 136, should read "High-power regulator . . . ".

How to use our bulletin board

This icon identifies those Design Ideas that have computer-readable material posted on EDN's bulletin-board system (BBS). Call our free BBS at (617) 558-4241 (300/1200/2400/9600 8,N,1). Not every Design Idea has downloadable material, but each one does have a BBS number printed at the end of it. Once you get into the system, you can use that number to find more information on a particular idea. If you'd like to comment on any Design Idea, include the number in the subject field of your message.

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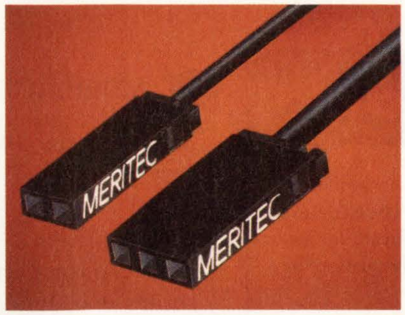

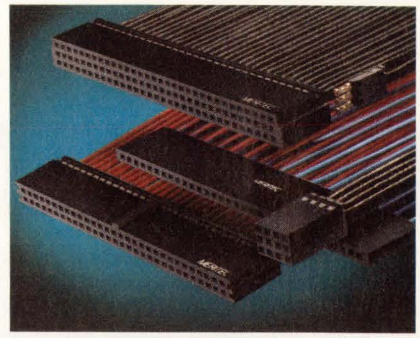

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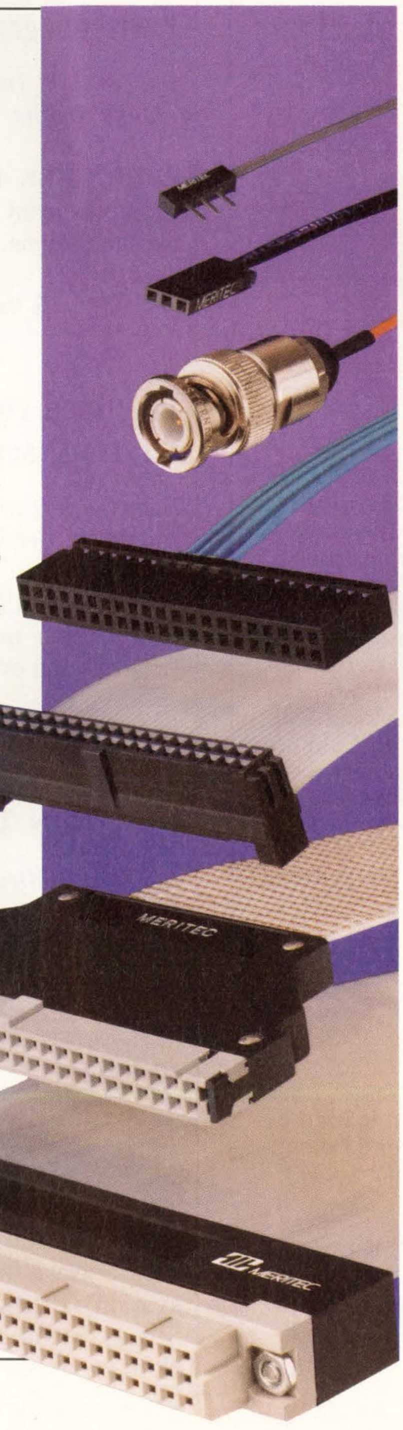

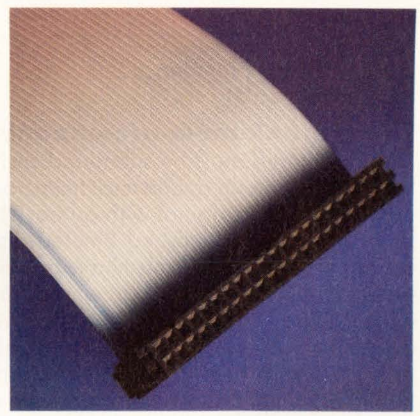

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Design Entry Blank

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Entry blank must accompany all entries.
Design entered must be submitted exclusively to EDN, must not be patented, and must have no patent pending. Design must be original with author(s), must not have been previously published (limited-distribution house organs excepted), and must have been constructed and tested. Fully annotate all circuit diagrams. Please submit software listings and all other computer-readable documentation on a 5¼-in. IBM PC disk in plain ASCII.

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ISSUE WINNER

The winning Design Idea for the March 2, 1992, issue is entitled "Tester checks capacitors on loaded pc boards," submitted by Nathan B Price and Peter J Kindleman of Congruent Design Inc (Guilford, CT).

ISSUE WINNER

The winning Design Idea for the March 16, 1992, issue is entitled "Multipliers implement tunable filters," submitted by Tom Napier of Aydin Computer and Monitor Div (Horsham, PA).

Software Shorts

PC simulates encoder

Ralph Ursoleo, Inovec Inc
Eugene, OR

The program in **EDN BBS /DI_SIG #1143** allows a PC's printer port to simulate the output of linear and rotary encoders.

To Vote For This Design, Circle No. 742

Basic program plots waveforms

Dai Jin Kun, Tianjin Institute of Metrological Technology
Tianjin, China

In **EDN BBS /DI_SIG #1141**, the Basic program and examples print out waveform diagrams of simple digital simulations.

To Vote For This Design, Circle No. 743

Pipelined routine speeds 8051 µC serial communication

Hans-Herbert Kirste, Sensycon GmBH
Hannover, Germany

In **EDN BBS /DI_SIG #1093**, the serial-communication routine pipelines data fetches to reduce serial-transmission overhead.

To Vote For This Design, Circle No. 744

PC debugs Transputer

James C Vandiver, Vandiver Electronics
Huntsville, AL

The Basic program in **EDN BBS /DI_SIG #1142**, along with a short Transputer program, allows you to debug a Transputer from your PC (via an Inmos link adapter).

To Vote For This Design, Circle No. 745

These Software Shorts listings are too long to reproduce here. You can obtain the listings from the Design Idea Special Interest Group on EDN's bulletin-board system (BBS): (617) 558-4241, 300/1200/2400/9600 8,N,1. From Main Menu, enter ss/DI_SIG, then rk*nnnn*, where *nnnn* is the number referenced above.

LINEAR TECHNOLOGY
DESIGN NOTES

5V High Current Step-Down Switchers – Design Note 59

Ron Vinsant and Milton Wilcox

Low Cost High Efficiency (80%), High Power Density DC-to-DC Converter

The LT1241 current mode PWM control IC can be used to make a simple high frequency step-down converter. This converter also has low manufacturing costs due to simple magnetic components. This circuit exhibits a wide input range of 30V to 60V while maintaining its 12A 5V output. It has short circuit protection and uses minimal PC board area due to its 300KHz switching frequency.

Figure 1 shows the LT1241 being used to drive the switching transistor Q1 through a ferrite pulse transformer T2. This transformer is built on a high μ material resulting in an 11 turn bifilar wound toroid that is only 0.15 inches in diameter and can be surface mounted. T1 acts as a current sense transformer whose volt • second balance is assured by the duty cycle limit of 50% inherent in the LT1241. The output inductor (L1) is made of Magnetics Kool-Mu material and is only 0.7 inches in diameter.

Short circuit protection is provided through bootstrap operation of the LT1241. If the output is shorted the LT1241 limits its pulse width to ≤ 250ns. Because there is not enough current supplied to make the aux winding on the output inductor 15V, the LT1241 stops operation. It will then try to start by C11 charging through R4. If the output is still shorted it will stop again. Thus in a short, the circuit starts and stops, protecting itself from overload.

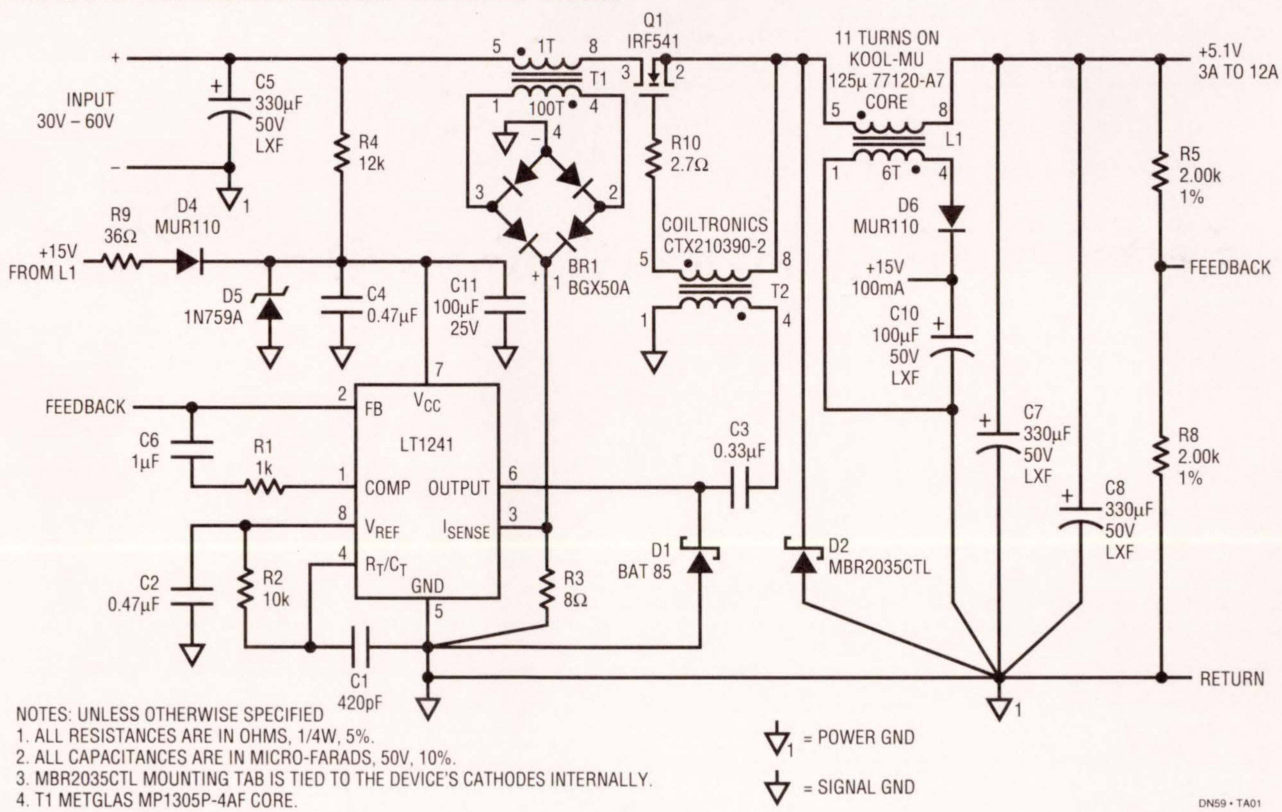


Figure 1.

Synchronous Switching Eliminates Heatsinks in a 50W DC-to-DC Converter

The new LT1158 half bridge N-Channel power MOSFET driver makes an ideal synchronous switch driver to improve the efficiency of step-down (buck) switching regulators. The diode losses in a conventional step-down regulator become increasingly significant as V_{IN} is increased. By replacing the high-current Schottky diode with a synchronously-switched power MOSFET, efficiencies well over 90% can be realized (see Figure 2).

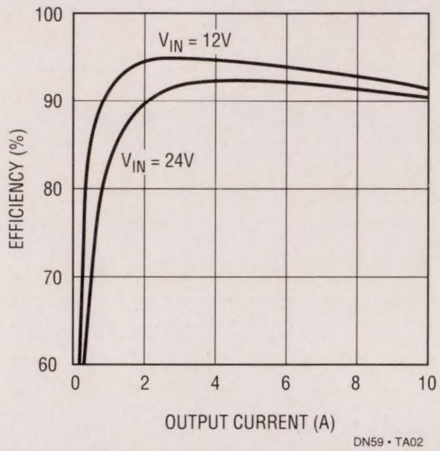


Figure 2. Operating Efficiency for Figure 3 Circuit

In the Figure 3 circuit an LT3525 provides a voltage mode PWM to drive the LT1158 input pin. The LT1158 drives (2) 28mΩ power MOSFETs for each switch, reducing individual device dissipation to 0.7W worst case. This eliminates the need for heatsinks for operation up to 10A at a temperature of 50°C ambient. The inductor and current shunt losses for the Figure 3 circuit are 1.2W and 0.7W respectively at 10A.

An additional loss potentially larger than those already mentioned results from the gate charge being delivered to multiple large MOSFETs at the switching frequency. This driver loss can only be controlled by running the oscillator at as low a frequency as practical — in the case of the Figure 3 circuit, 25kHz. A very low ESR (<20mΩ) output capacitor is used to limit output ripple to less than 50mVp-p with 2.5Ap-p ripple current.

The LT1158 also provides current limit for DC-to-DC converter applications. When the voltage across R_S exceeds 110mV, the LT1158 $\overline{\text{fault}}$ pin conducts, and assumes control of the PWM duty cycle. This provides true current mode short circuit protection with soft recovery. The Figure 3 regulator current limit is set at 15A which raises the dissipation in each bottom MOSFET to 1.7W during a short. Therefore 30°C/W heatsinking must be added for the bottom side MOSFETs if continuous short circuit operation is required. Care should also be taken when routing the sense+ and sense− leads to prevent coupling from the inductor.

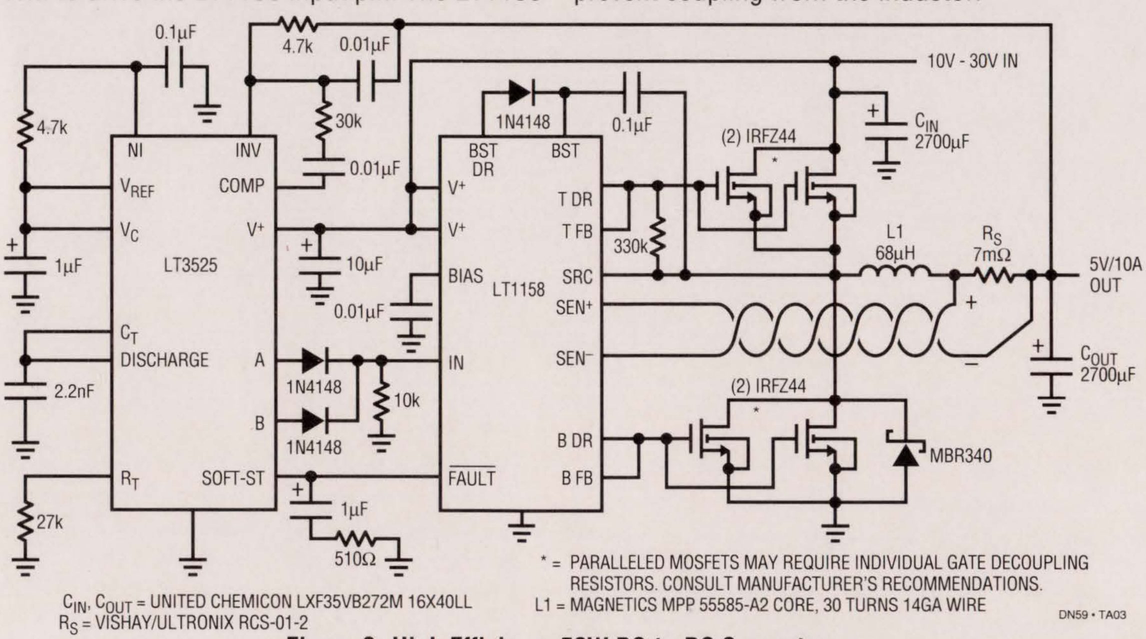
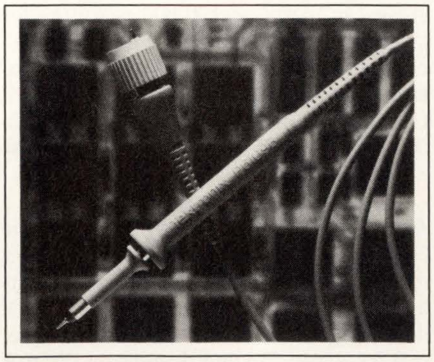


Figure 3. High Efficiency 50W DC-to-DC Converter

For literature on our Switching Regulators, call **(800) 637-5545**. For applications help, call (408) 432-1900, Ext. 456

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7487
(408) 432-1900 • FAX: (408) 434-0507 • TELEX: 499-3977

BA/GP 0492 190K



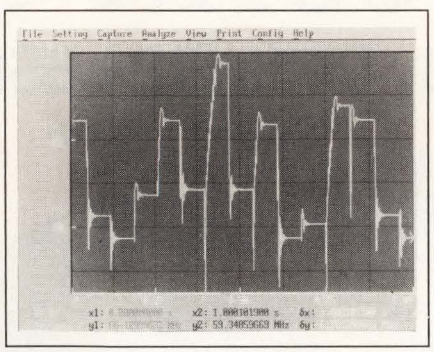
Scope probes. B-Series molded probes offer bandwidths to 100 MHz. They are UL-certified, and their removable tips can withstand forces as high as 50 lb. The probes can compensate for scope input capacitance from 15 to 35 pF. The 10× unit that works with scopes whose input resistance is 1 MΩ has a series resistance of 9 MΩ ±0.25%. The probes' internal components are surface mounted on multilayer pc boards, which are encased in metal cylinders that provide electrical and mechanical shielding. From $50. **Tektronix Inc,** Box 1520, Pittsfield, MA 01202. Phone (800) 426-2200. **Circle No. 374**

Test system for mixed-signal ICs. The Vistavision system is a high-throughput tester for mixed-signal ICs that have as many as 448 pins. Included in this class are devices that incorporate both analog circuits and fast, complex digital functions. The system achieves its high performance by using a tester-per-pin architecture and by locating an unusually large percentage of its critical test circuits within inches of the device under test. Modular design facilitates reconfiguring the tester to handle new IC families. From $1 million. **Credence Systems Corp,** 47211 Bayside Ave, Fremont, CA 94538. Phone (510) 657-7400. FAX (510) 623-2560. **Circle No. 375**

Fast transient/burst simulators. The E410 and E420 simulators are µP-controlled units. They use a thyratron circuit to provide pulses of the 50-nsec duration prescribed by IEC 801-4 into widely varying loads—not just to the calibration load. You can control the units from their panels, which provide 8×40-character LCDs, or from a PC via an optional fiber-optic link. From $20,000. Delivery, 60 to 90 days ARO. **Keytek Instrument Corp,** 260 Fordham Rd, Wilmington, MA 01887. Phone (508) 658-0880. FAX (508) 657-4803. **Circle No. 376**

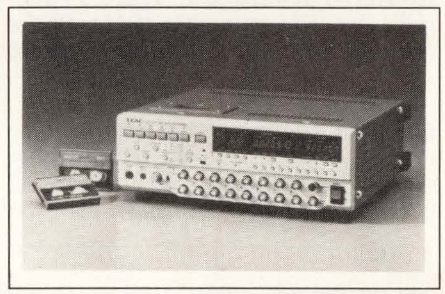
Diskless, Unix and 68040-based VXI controller. The HP 9000 V/382 is a double-width VXIbus module. You use it on networks where a server provides hard-disk storage. The controller includes RS-232C, IEEE-488, Ethernet, SCSI, and parallel interfaces. The choice of color-graphics support includes resolutions ranging from 640×480 to 1280×1024 pixels. $13,300 with 8 Mbytes of RAM and a 640×480-pixel display. **Hewlett-Packard Co,** 19310 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 752-0900. **Circle No. 377**

MS-Windows-based software. SnapMaster for Windows lets you define custom virtual instruments. The software supports ADCs operating to 1 Msample/sec. It handles cards from several vendors and can control several cards at one time. Frequency-analysis capabilities include spectrum-analyzer functions. Each of the three software modules is usable separately or in combination with either or both of the others. Data-acquisition module, $995; general and frequency-analysis modules, $495 each. **HEM Data Corp,** 17336 12 Mile Rd, Suite 200, Southfield, MI 48076. Phone (313) 559-5607. FAX (313) 559-8008. **Circle No. 378**



Time-interval-analysis software. Timeview software, in conjunction with the vendor's PM 6680 timer/counter, lets you measure how frequencies and time intervals change vs time (modulation-domain measurements). Such measurements have heretofore been the province of much more expensive instruments called time-interval analyzers (TIAs). The PM 6680's ability to take 2000 readings/sec makes it one of the fastest counters available, but it is slow compared with TIAs, some of which take 10 million readings/sec. However, the software implements a mode which, for repetitive signals having stable trigger points, in effect increases the counter's rate to 10 million readings/sec. Counter plus software, less than $3000. **John Fluke Mfg Co Inc,** Box 9090, Everett, WA 98206. Phone (800) 443-5853; (206) 347-6100. FAX (206) 356-5116. **Circle No. 379**

Turnkey VMEbus-based data-acquisition systems. These systems are based on the vendor's MD-CPU330 board, which includes 8 Mbytes of RAM and runs the Vxworks real-time OS. Systems can include a 2-Gsample/sec waveform digitizer as well as an assortment of array processors, display controllers, and instruments. $50,000 to $150,000. **Matrix Corp,** 1203 New Hope Rd, Raleigh, NC 27610. Phone (800) 848-2330; (919) 231-8000. FAX (919) 231-8001. **Circle No. 380**

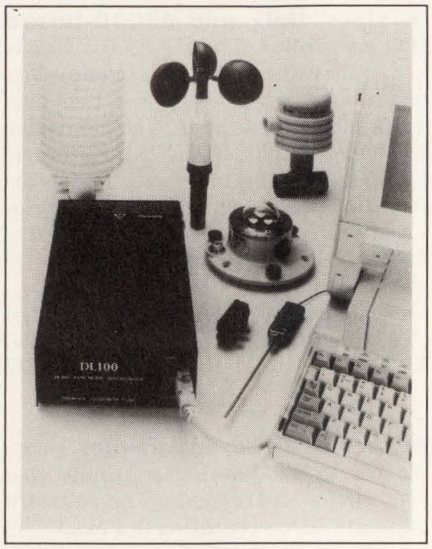


Portable instrumentation tape recorders. The RD-125T and RD-135T use digital-audio-tape (DAT) technology. They offer two speeds—standard and double speed. In the double-speed mode, the frequency response is twice that of standard DAT recorders. The RD-125T records 4 channels of 20-kHz data; the RD-135T records 8 channels of 10-kHz data. You can use one channel on either unit to record 14 digital signals instead of an analog signal. $10,500. **Teac America Inc,** 7733 Telegraph Rd, Montebello, CA 90640. Phone (213) 726-0303. FAX (213) 727-7621. **Circle No. 381**

Design-for-testability software. TDS Release 4.1 provides additional support for inputs from simulators and for stimulus generation. It handles a wider range of test-program-generation methods than did earlier versions. It also provides additional support for the Wavemaker and Wavebridge modules. Simulator support enhancements include linkages to additional products from Cadence, GenRad, and Mentor, as well as a converter for TI's test-description language. Tester support enhancements include additional linkages to Teradyne board testers and LTX/Trillium digital IC testers. The software now runs under X Windows on HP 9000 series 300 workstations, as well as on the Sun, Solbourne, and HP Apollo. From $10,000. **TSSI,** 8205 SW Creekside Pl, Beaverton, OR 97005. Phone (800) 642-9281; (503) 643-9281. FAX (503) 646-4954. **Circle No. 382**

Synthesized signal generator. The HP 83731A delivers precise, modulated signals for testing communications, radar, and electronic-warfare receivers in the 1- to 20-GHz range. It delivers +14 dBm to −90 dBm with ±2-dB accuracy. Harmonics are below −55 dBc and spurious signals are below −60 dBc. The generator offers logarithmic amplitude modulation and incorporates a programmable pulse generator. $28,500. Delivery, eight weeks ARO. **Hewlett-Packard Co,** 19310 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 452-0900. **Circle No. 383**

Portable analog data logger. The DL100 battery-powered data-logging system has 24 analog inputs, each of which has a full-scale range that you



can set in 10 steps from 30 mV to 30V. After you set up the logger, an operation that requires a PC-notebook PC works fine—you can remove the PC and leave the logger unattended for as long as 300 hours in a location where ac power is inaccessible. The logger, which supplies transducer excitation, uses an integrating ADC to minimize noise and stores as many as 100,000 readings for later uploading to a host PC. $1500; 16-channel version, $1200. **Interface Instrument Corp,** 37845 Soap Creek Rd, Corvallis, OR 97330. Phone (503) 745-5620. FAX (503) 745-7470. **Circle No. 384**

Auto/manual-ranging DMM. The 380501 DMM has a 0.77-in.-high $3\frac{1}{2}$-digit LCD. The unit measures ac voltage (2 to 750V full scale, ±0.75% error); dc voltage (200 mV to 1 kV full scale, ±0.5% error); ac and dc current (20 mA to 20A full scale); and resistance. It also checks diodes and provides an audible continuity indication. A data-hold button lets you freeze readings. $79. **Extech Instruments Corp,** 335 Bear Hill Rd, Waltham, MA 02154. Phone (617) 890-7440. FAX (617) 890-7864. **Circle No. 385**

Data-acquisition and graphics software. MS-DOS-based Easyest AG uses an icon interface to minimize setup and configuration time, yet it does not sacrifice flexibility. The package allows the use of ten 16-channel data-acquisition boards but does not impose constraints on the boards' speed. The software supports linearization and cold-junction compensation for seven types of thermocouples. It provides for calibration and performs functions such as converting data to engineering units. $95 when purchased with a Keithley Metrabyte data-acquisition board. **Keithley Asyst,** 440 Myles Standish Blvd, Taunton, MA 02780. Phone (800) 348-0033; (508) 880-3000. **Circle No. 386**

Extender for Micro Channel Architecture boards. By incorporating programmable overcurrent detection and protection, the UME lets you insert Micro Channel Architecture bus boards and remove them without powering the computer down or reloading the operating system and application software. The unit also prevents faulty boards from damaging the computer. A breadboard area provides easy access to eight data lines, I/O read and write lines, and power. $480; after June 30, 1992, $600. **Az-com,** 12 Rose Lane, Orinda, CA 94563. Phone (510) 254-5400. **Circle No. 387**

20-MHz emulator for 80186. The 20-MHz UEM for the 80186 includes both a full-featured in-circuit emulator (ICE) and the vendor's source-level debugger. The ICE includes 131,072 hardware breakpoints, as much as 1 Mbyte of overlay RAM, and a hardware performance analyzer. The package also includes a memory-access monitor for finding wild pointers. "Never-stop" emulation aids in debugging interrupt service routines. $8500. **Softaid Inc,** 8300 Guilford Rd, Columbia, MD 21046. Phone (800) 433-8812; (410) 290-7760. FAX (410) 381-3253. **Circle No. 388**

Automatic-test system for Macintosh software. The Testrunner package consists of a hardware accelerator and software that automates testing of software applications written for the Apple Macintosh. The package translates keyboard and mouse inputs into test scripts that you can modify. Just as a human operator would, the scripts provide inputs to the application under test only when the application calls for them. With this capability, you can automate the repetitive operations that occur in software testing. From approximately $20,000. **Mercury Interactive Corp,** 3333 Octavius Dr, Santa Clara, CA 95054. Phone (408) 987-0100. FAX (408) 982-0149. **Circle No. 389**

8-channel, 12-bit DAC card for ISA bus. In addition to DACs, the DAC-812 offers 24 channels of digital I/O. You can update the DACs either sequentially or simultaneously at rates to 200 ksamples/sec/DAC. High-level-language libraries are included. $599. **Analogic Corp,** 360 Audubon Rd, Wakefield, MA 01880. Phone (508) 977-3000. FAX (617) 245-1274. **Circle No. 390**

Nubus-based TMS320C30 DSP coprocessor board. The NB-DSP2305 uses a 40-MHz TMS320C30 DSP µP and 64k words of zero-wait-state memory to achieve a processing speed of 40 Mflops. The board can act as the bus master, directly accessing boards in the Apple Macintosh. The Real-Time System Integration bus carries serial data to the board from the vendor's acquisition boards at the same time that the Macintosh uses the bus. $4995; memory-expansion board providing 320k words, $1995. **National Instruments Corp,** 6504 Bridge Point Pkwy, Austin, TX 78730. Phone in US and Canada, (800) 433-3488; (512) 794-0100. FAX (512) 794-8411. TLX 756737. **Circle No. 391**

Laptop-PC-compatible ADC board. The PC-126 ISA bus board fits in the shortest bus slots. It uses its own dc/dc converter to create all of the supply voltages it needs except for 5V. It's therefore compatible with all laptop PCs that have ISA bus slots. The board has a 50-ksample/sec 12-bit ADC, a 16-channel analog multiplexer, two 12-bit DACs, eight digital-input lines, and eight digital outputs. $545. **United Electronic Industries,** 10 Dexter Ave, Watertown, MA 02172. Phone (617) 924-1155. FAX (617) 924-1441. **Circle No. 392**

Horizontal socket shifter. The YS28/6-210 shifter for the Data I/O 2900 programmer permits the programmer's DIP socket to accommodate surface-mount devices. It accomplishes this by providing a stable platform for a 28-pin socket adapter that has pin rows on 0.6-in. centers. The shifter displaces the adapter from the socket by 2.1 in. horizontally, allowing room to actuate the DIP socket's lever. It is also available with the vendor's socket adapter already mounted. $25. **EDI Corp,** Box 366, Patterson, CA 95363. Phone (209) 892-3270. FAX (209) 892-3610. **Circle No. 393**

Enhanced MS-DOS data-acquisition software. Compared with its predecessors, Labwindows V2.2 offers faster-operating libraries for real-time DSP. Displayed graphs have as many as 10 cursors. You can set the cursors to move freely or to snap to the nearest trace and follow the trace when it moves. While executing, your programs can change attributes such as color, labels, fonts, and visibility. $695; with advanced-analysis library, $895; upgrades from earlier versions, $195. **National Instruments Corp,** 6504 Bridge Point Pkwy, Austin, TX 78730. Phone (800) 433-3488; (512) 794-0100. FAX (512) 794-8411. TLX 756737. **Circle No. 394**

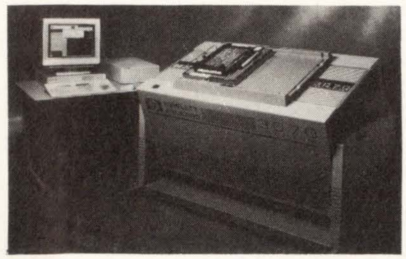
VXIbus pressure-transducer interface. The V522 works with Paroscientific Inc's Digiquatz 1000 series of intelligent pressure transmitters. The transmitters send data over an RS-232C-compatible serial link at speeds from 300 to 19,200 bps. You can connect five transmitters in a loop. The register-based interface module supports two such loops. The μP in the interface converts the transmitters' ASCII data to binary and makes both ASCII and binary information available. From $3450. **Kinetic Systems Corp,** 11 Maryknoll Dr, Lockport, IL 60441. Phone (800) 328-2669; (815) 838-0005. FAX (815) 838-4424. **Circle No. 395**

In-circuit emulator for 68EC000. The 68EC000 UEM is for debugging systems based on the embedded-control version of the 68000. The EC chip's bus structure is different from that of its general-purpose sibling. The debugging package consists of an emulator integrated with a source-level debugger that supports C and PL/M. The emulator provides 131,072 hardware breakpoints that nest to a depth of five levels.

A software performance analyzer displays the portion of time spent executing as many as 255 different functions. $7500. **Softaid Inc,** 8300 Guilford Rd, Columbia, MD 21046. Phone (800) 433-8812; (410) 290-7760. FAX (410) 381-3253. **Circle No. 396**

10V, 45-psec rise-time pulse generator. The 10,050A pulse generator produces 10V pulses with 45-psec rise time and 110-psec fall time. You can adjust the pulse duration from 100 psec to 10 nsec in 2.5-psec steps. The unit incorporates an IEEE-488 interface. The panel includes a keyboard and an LCD. Approximately $9900. Delivery, 12 weeks ARO. **Picosecond Pulse Labs Inc,** Box 44, Boulder, CO 80306. Phone (303) 443-1249. **Circle No. 397**

Low-cost, pc-board test systems. The HP 3173 and HP 3175 are priced 40% below earlier members of the HP 3070 series but are based on the same industry standards. The lowest priced system generates 6.25M patterns/sec that you can upgrade to 12M or 20M.

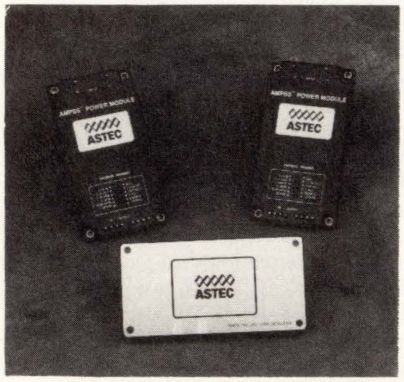


The systems include software for in-circuit testing of boards that include IEEE-1149.1 boundary-scan features. The systems test circuits that have as many as 1296 nodes. From $100,000. **Hewlett-Packard Co,** 19310 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 452-4844. **Circle No. 398**

Test-process management system. Boardwatch version 3.1 displays messages in any language that uses the Roman alphabet. The system supports translation of message screens, forms, and help screens into the language of your choice. The software, which is based on the Oracle database-management system, incorporates the advanced features of Oracle version 6. From $30,000. **Teradyne Inc,,** 321 Harrison Ave, MS L-57, Boston, MA 02118. Phone (617) 422-3567. **Circle No. 399**

24-channel ISA bus ADC board. The AIP-24 short card accepts 24 differential input signals. Its ADC has 12-bit resolution and makes conversions in 25 μsec. A programmable-gain amplifier offers gains of 1, 10, and 100. $495. **Global Specialties,** 70 Fulton Terrace, New Haven, CT 06512. Phone in US and Canada, (800) 572-1028; (203) 624-3103. FAX (203) 468-0060. **Circle No. 400**

Differential scope probe. The ADF15 offers 15-MHz bandwidth and allows differential measurements on a single scope channel, rather than forcing you to tie up two inputs for a single measurement. You can switch the attenuation between ×20 and ×200. The unit operates from four AA cells or from an external ac adapter. $375. **Test Probes Inc,** 9178 Brown Deer Rd, San Diego, CA 92121. Phone (619) 535-9292. **Circle No. 401**



DC/DC converters. AMPSS AM80 dc/dc converters provide a 5V at 40A output from inputs of either 48 or 300V. The devices feature a 1-MHz switching frequency, 84% efficiency, and a 36W/in.^{3} power density. You can program maximum output current over a 20 to 115% range. When the output voltage exceeds 15 to 45% of rated output, you can program an overvoltage circuit externally to shut down the unit. The unit will also shut down if internal temperature exceeds 110°C. The converter has nominal line and load regulations of 0.02 and 0.1%, respectively. Output ripple and noise are less than 1%. $245. **Astec Standard Power,** 401 Jones Rd, Oceanside, CA 92054. Phone (619) 757-1880. FAX (619) 439-4243.

Circle No. 351

LED indicators. Prism CBI indicators feature a surface-mount LED mounted in an upward-facing direction. A right-angle prism and clear lens combination bends the light 90° so that it exits parallel to the circuit board. The units are available in T-¾, T-1, and T-1¾ sizes. Super-bright red and high-efficiency red, yellow, and green colors are available now. $0.85 (1000). Delivery, stock to eight weeks ARO. **Dialight Corp,** 1913 Atlantic Ave, Manasquan, NJ 08736. Phone (908) 223-9400. FAX (908) 223-8788.

Circle No. 352

Solid-state relays. Series CA spst NO solid-state relays are rated for 1A at 250V rms for resistive and inductive loads with power factors as low as 0.2. The internal design ensures low EMI performance by virtually eliminating commutation spikes. Optical techniques provide 1500V rms of isolation between control and load circuits. The relays are CMOS and TTL compatible and are housed in a ceramic DIP. The units are available to the W and Y screening levels of MIL-R-28750. Less than $50 (OEM qty). **Teledyne Solid State,** 12525 Daphne Ave, Hawthorne, CA 90250. Phone (213) 777-0077.

Circle No. 353

Pressure transducers. PDCR 130 series transducers are available in ranges of 1 through 10,000 psig or psia. Combined accuracy equals 0.1 or 0.05%. The units operate from a 10 to 30V supply and have a 10V dc output. Reversal protection and I/O isolation are standard features. $480. **Druck Inc,** 4 Dunham Dr, New Fairfield, CT 06812. Phone (203) 746-0400. FAX (203) 746-2494.

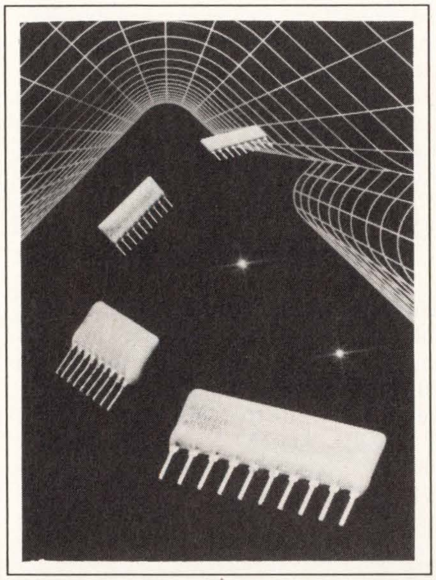
Circle No. 354

Membrane keyboard. Keyboard 101 matches the conventional enhanced AT keyboard's key location and functionality but replaces the full-travel keys with

a flat, washable membrane. Standard computer-interface options include keyboard port (AT or PS/2 straight or Y connector), RS-232C serial (ASCII or scan code), parallel, and a universal terminal interface. $300 to $350. **Genovation Inc,** 17741 Mitchell N, Irvine, CA 92714. Phone (714) 833-3355. FAX (714) 833-0322. **Circle No. 355**

Test sockets. These SMT-PGA converters are designed for EIAJ and JEDEC devices. The top boards match the pin patterns of most surface-mount devices. For device-specific converters, the pins are configured the same as they would be for the actual pin-grid-array package. Generic converters are pin-for-pin compatible with most standard surface-mount device footprints. From $9.98 (10). **ITT Pomona Electronics,** Box 2767, Pomona, CA 91769. Phone (714) 469-2900. FAX (714) 629-3317. **Circle No. 356**

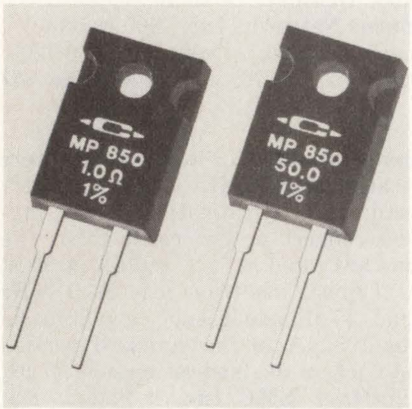
RC networks. Series 700 CMOS terminators are composed of a resistor and capacitor in series with all elements con-



nected to a common pin. Two versions are offered—701 units terminate 7, 8, or 9 lines and have a single common pin. The 702 models terminate 8 lines and have two common pins. All models are available with resistance values of 50, 68, 75, or 100Ω and capacitance values of 47, 50, 100, or 1000 pF. $1.51 to $2.03. Delivery, 14 to 16 weeks ARO. **Bourns Networks Inc,** 1400 N 1000 W, Logan, UT 84321. Phone (801) 750-7200. FAX (801) 750-7253. **Circle No. 357**

Power line filter. FN 223 series filters are available with IEC 320 ac inlet connectors and combination solder lug, quick-connect output connectors. The units are rated at 1, 3, and 6A at 250V ac. Typical insertion loss at 5 MHz equals 35 dB, and leakage current measures 195 μA in the standard version and 2 μA in the medical version. $7.97. **Schaffner EMC Inc,** 9 Fadem Rd, Springfield, NJ 07081. Phone (800) 367-5566; (201) 379-7778. FAX (201) 379-1151. **Circle No. 358**

Power resistors. Type MP850 Kool-Pak power film resistors are rated for 50W at 25°C case temperature. The package design features an integral copper heat sink molded into the TO-220 package. A noninductive design, the units are available with values ranging from 1Ω to 10 kΩ with tolerances of ±1, ±2, ±5, and ±10%. The resistor



element is electrically isolated from the molded package. $1.99 (10,000) for a 10Ω, 2% model. Delivery, six weeks ARO. **Caddock Electronics Inc,** 17271 N Umpqua Hwy, Roseburg, OR 97470. Phone (503) 496-0700. FAX (503) 496-0408. **Circle No. 359**

Ethernet transceiver. ENT-4302 fiber-optic units are housed in a 3.1×1.4×3.3-in. aluminum case. Features include a 15-pin AUI interface, ST or SMA optical connectors, and user-selectable SQE to ensure compatibility with different network configurations. The unit supports FOIRL or 10Base-FL standards through a user-selectable switch. $395. **Lancast,** 10 Northern Blvd, Unit 5, Amherst, NH 03031. Phone (800) 752-2768; (603) 880-1833. FAX (603) 881-9888. **Circle No. 360**

Surface-mount mixers. RMS-2UMH mixers are housed in a 0.25×0.31×0.2-in. plastic case. They operate over a 10- to 1000-MHz frequency range. Conversion loss for the 13-dBm LO output is 8.2 dB. $14.45. **Mini-Circuits,** Box 350166, Brooklyn, NY 11235. Phone (718) 934-4500. FAX (718) 332-4661. **Circle No. 361**

Interface module. PE-65434 modules contain the isolation transformers as well as the filtering needed to meet or exceed IEEE-802.3 and the FCC/VDE emissions requirements. The modules include both transmit and receive channels. Common-mode chokes on both the transmit and receive lines ensure maximum attenuation of unwanted emissions in multiport applications. $4.95 (1000). **Pulse Engineering Inc,** Box 12235, San Diego, CA 92112. Phone (619) 674-8100. **Circle No. 362**

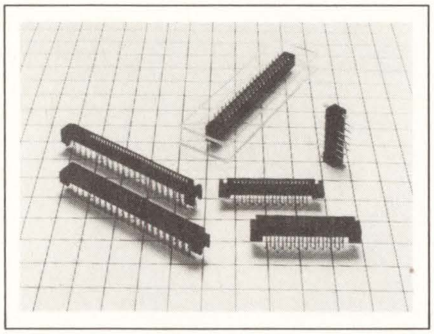
LED arrays. Series 557 LEDs come in single-color and bicolor versions. The single-color units are available in green, red, and amber and operate at 4.3, 5, 12, and 28V. The bicolor (red-green) unit operates at 5V. $4 (1000). Delivery, six to eight weeks ARO. **Dialight Corp,** 1913 Atlantic Ave, Manasquan, NJ 08736. Phone (908) 223-9400. **Circle No. 363**

Shielded cabinets. These shielded cabinets feature 50 dB of attenuation at 1 GHz and more than 120-dB attenuation at lower frequencies. The cabinets' heavy-duty frame meets MIL-STD-810D for shock and vibration and MIL-STD-901 for shock. The units can be hardened to meet seismic conditions through zone 4. From $1046. **Equipto Electronics Corp,** 351 Woodlawn Ave, Aurora, IL 60506. Phone (708) 897-4691. FAX (708) 897-5314. **Circle No. 364**

LED arrays. Series 5655F arrays are available in red, amber, green, or yellow. The nylon housings meet Bellcore flammability standards and carry a UL 94V-0 rating. Built-in standoffs simplify board cleaning processes. $0.38 (1000). **Industrial Devices Inc,** 260 Railroad Ave, Hackensack, NJ 07601. Phone (201) 489-8989. **Circle No. 365**

Power transistors. The surface-mount device (SMD) line of units includes transistors, zener diodes, triacs, and Schottky rectifiers. The transistors handle 1.2W; the 1W zeners are available with ratings of 3.3 through 33V. Triac ratings range to 800V, and the Schottky rectifiers are rated for 1A at 40V. The devices are available in SOT-89 cases. $0.24 to $0.34 (1000). **Central Semiconductor Corp,** 145 Adams St, Hauppauge, NY 11788. Phone (516) 435-1110. FAX (516) 435-1824. **Circle No. 366**

Half-pitch connectors. The FX4 series half-pitch 2-piece connectors come in heights of 5 through 11 mm. Available in 20- through 80-position versions,



the units are designed to prevent solder-wicking during assembly operations. The connector housings are made of polyimide resin, and contacts are phosphor bronze. Current rating equals 0.5A. **Hirose Electric Inc,** 2685-C Park Center Dr, Simi Valley, CA 93065. Phone (805) 522-7958. FAX (805) 522-3217. **Circle No. 367**

Terminal blocks. Model D2.5/6.D 3-level terminal blocks simplify the wiring of sensor and actuator switches to programmable controllers. All models mount on symmetrical DIN rails and are UL recognized for operation at 300V. The blocks are available in configurations of 3-input/3-output clamps with optional LED for use with shielded twisted-pair applications. From $3.56. **Entrelec Inc,** 1950 Hurd Dr, Irving, TX 75038. Phone (800) 431-2308; (800) 275-1114. FAX (214) 550-9215. **Circle No. 368**

Modular jacks. These right-angle surface-mount modular jacks measure 0.453 in. high and come in 4-, 6-, and 8-position versions. The units feature board locks to ensure secure mounting. The housings are rated at UL 94V-0. The phosphor-bronze gull-wing contacts have 50-μin. of gold plating. $0.84 (1000) for a 6-position version. Delivery, stock to six weeks ARO. **Kycon Cable & Connector Inc,** 1772 Little Orchard St, San Jose, CA 95125. Phone (408) 295-1110. FAX (408) 295-8054. **Circle No. 369**

Power transistors. LXE18300X devices work as amplifiers in Class AB transmitters. With a 24V supply and 300-mA collector current, output power

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CIRCLE NO. 90

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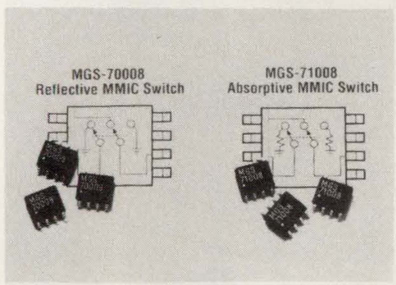
equals 32W for 1-dB compression at 1.85 GHz. At an average output power of 15W, intermodulation distortion is less than −30 dBc. Power gain equals 10 dB. $220 (1000). Delivery, 10 to 12 weeks ARO. **Philips Components,** 2001 W Blue Heron Blvd, Riviera Beach, FL 33404. Phone (800) 447-3762; (407) 881-3342. **Circle No. 370**



Switches. The MGS-70008 spdt unit is available in a reflective version, and the MGS-71008 spdt unit comes in an absorptive version. They operate from sources as low as 3.3V and have a 3-nsec switching speed. Isolation equals 37 dB at 1 GHz, and VSWR measures 1.3:1 max through 2 GHz. MGS-70008, $6.80; MGS-71008, $8.60 (1000). **Avantek Inc,** 481 Cottonwood Dr, Milpitas, CA 95035. Phone in US, (800) 282-6835; (408) 943-3038; in Canada, (416) 678-9430; in Europe, (49) 7031/14-0; in Japan, (81) 3-3331-6111; in Far East/Australia, (65) 290-6360. **Circle No. 371**

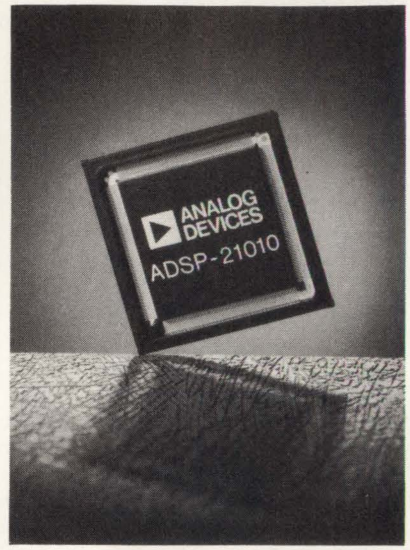
Device for socketing and probing. The EF-QFE160S-01 allows interconnection of test pins, ZIF sockets, and other functions to surface-mount pads on a target pc board. The unit's pins have the same geometry as that of an EIAJ 160-pin quad flatpack that it houses. Pins are on 0.050-in. centers. $250. **Ironwood Electronics,** Box 21151, St Paul, MN 55121. Phone (612) 431-7025. FAX (612) 432-8616. **Circle No. 372**

Terminal strips. Series 72CS single-row strips have centers spaced on 0.375-in. centers and are rated for 20A. The units are available in closed-back and feed-through designs. The strips are UL recognized and CSA certified and are made of thermoplastic that meets UL1950 and VEC 69050 standards. $0.19/terminal (500). **Vernitron Corp,** Box 10, Laconia, NH 03247. Phone (603) 524-5101. FAX (603) 524-1627. **Circle No. 373**

Integrated Circuits

Analog multiplexer. The 8-channel HV25 multiplexer can control analog signals from +14 to −12.5V that have a maximum peak current of 40 mA. The output switches can withstand ±80V, and the switch resistance for all channels is 300Ω. Off isolation is 50 dB. $9.85 to $15.48 (1000). Delivery, six to eight weeks ARO. **Supertex Inc,** 1350 Bordeaux Dr, Sunnyvale, CA 94089. Phone (408) 744-0100. FAX (408) 734-5247.
Circle No. 402

Mixed-voltage graphics controller. Designed for LCDs having VGA resolution, the CL-GD6412 controller interfaces with both 3.3 and 5V systems. The core of the device supports the JEDEC Number-8 LVCMOS operating standard (3.3V ±0.3V), and the structure of its video-memory, host-bus, panel, and clock interfaces allows the use of mixed-voltage system components without need of external level converters. The controller provides 64 shades of gray on monochrome LCD panels and direct connection to 512-color LCD panels. In 160-pin quad flatpack, $65. **Cirrus Logic,** 3100 W Warren Ave, Fremont, CA 94538. Phone (510) 623-8300. FAX (510) 226-2240. **Circle No. 403**



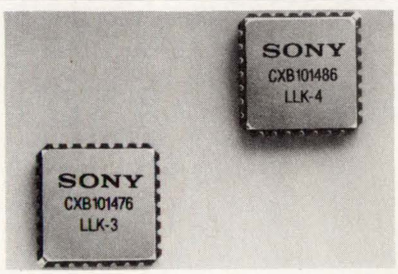
Speed-enhanced DSP chip. Featuring a 60-nsec instruction cycle (16.6 MIPS), the ADSP-2101-66 is a faster version of the established ADSP-2101, which is available in 80- and 100-nsec grades. Supporting the DSP's high-performance, fixed-point capability is the $499 EZ-Kit, which includes an applications textbook with source-code library, assembly language, simulator, and an evaluation board. The ADSP-2101-66, in 68-pin, pin-grid arrays and plastic leaded chip carriers or 80-pin plastic quad flatpacks, $61 (1000). **Analog Devices Inc,** Box 9016, Norwood, MA 02062. Phone (617) 461-3672.
Circle No. 404

ISDN dc-termination IC. Used on U-Interface Digital Subscriber Lines, the LH1465AB serves a dual role in ISDN (Integrated Services Digital Network) applications. It provides a dc termination and a high ac impedance and acts as part of the dc signaling system during line testing from the central office. The monolithic circuit integrates the functions of an inductor, a silicon-controlled rectifier, and the drive circuit for an optoisolator. In an 8-pin DIP, $4.45 (1000). **AT&T Microelectronics,** Dept 520404200, 555 Union Blvd, Allentown, PA 18103. Phone (800) 372-2447, ext 826; in Canada (800) 553-2448, ext 826. **Circle No. 405**

Programmable gain amplifiers. The AD75062 dual and AD75068 octal programmable gain amplifiers feature a constant bandwidth of −3 dB at 2 MHz at all gain settings. All programmable-gain-amplifier channels are independently programmable for gains of 1 to 128 in powers of 2. Phase shift is 2.5° from dc to 10 kHz, and channel-to-channel isolation is 73 dB min. AD75062 in 16-pin ceramic DIP, $20; AD75068 in 44-pin ceramic LCC package, $80 (100). **Analog Devices,** 181 Ballardvale St, Wilmington, MA 01887. Phone (617) 937-1248. **Circle No. 406**

Video RAMs. The HM538253 (page-mode) and HM538254 (hyper-page-mode) video RAMs (VRAMs) are 2-Mbit devices that integrate a 256k×8-bit dynamic RAM with a 512×8-bit serial-access memory (SAM). In both devices, the VRAM and the SAM operate independently, permitting either synchronous or asynchronous operation. The devices have RAM-port access times of 70-, 80-, and 100-nsec; cycle times are 130-, 150-, and 180-nsec. $30 (1000). **Hitachi America Ltd,** Semiconductor and IC Div, 2000 Sierra Point Pkwy, MS-080, Brisbane, CA 94005. Phone (415) 589-8300. FAX (415) 583-4207. **Circle No. 407**

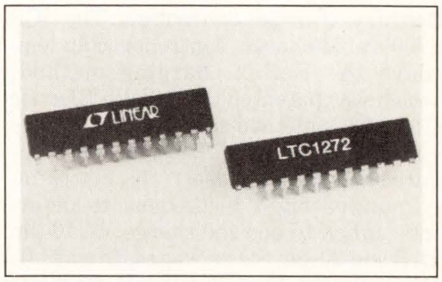
High-speed ECL SRAMs. A series of four ECL static RAMs (SRAMs) features access times of 3 or 4 nsec, depending on density. The CXB101476LLK-3 4-kbit and CXB101486LLK-4 16-kbit



SRAMs are synchronous, self-timed versions organized as 1024 words×4 bits and 4096 words×4 bits, respectively. The devices feature access times of 3 and 4 nsec and cycle times of 4 and 5 nsec, respectively. These synchronous SRAMs include input and output latches and on-chip write timing. The CXB101474D-3 and CXB101484D-4 are asynchronous versions without the latches and write-timing features. Synchronous versions come in 28-pin LCCs; asynchronous versions come in 24- or 28-pin DIPs. The 1k×4-bit devices, $80; 4k×4-bit devices, $160. **Sony Corp of America,** Component Products Co, 10833 Valley View St, Cypress, CA 90630. Phone (714) 229-4197. FAX (714) 229-4333. **Circle No. 408**

486 PC/AT-compatible controller. The VL82C486 device is optimized for 486SX- and 486DX-based computers operating at speeds to 33 MHz. It replaces nine peripheral devices, including two DMA controllers, an interval timer, a clock generator and interface, two interrupt controllers, a memory mapper and a bus controller. The IC also contains a memory-refresh controller, and bus-steering, parity-checking, and burst-mode control. In a 208-pin quad flatpack, $35 (OEM qty). **VLSI Technology Inc,** 8375 South River Pkwy, Tempe, AZ 85284. Phone (602) 752-8574. FAX (602) 752-6000. **Circle No. 409**

ADC for upgrading industry-standard devices. A substantial upgrade of the industry-standard AD7572, the LTC1272 A/D converter adds a 1-μsec



S/H circuit and features single 5V operation. In its fastest version, the LTC1272 has a 3-μsec conversion time; this time exceeds the speed of the AD7572, which lacks the S/H circuit. The LTC1272 converts 2.5× faster than the AD1674 or the MAX163 competitive devices, which have S/H circuits. Device pinout is the same as that of the 24-pin industry standard. Output data can be read as one 12-bit word or as two 8-bit bytes. The LTC1272 is available in 3-, 5-, and 8-μsec speed grades and in several linearity grades. In DIP and SO versions, from $16.90 to $38.45 (100). **Linear Technology Corp,** 1630 McCarthy Blvd, Milpitas, CA 95035. Phone (800) 637-5545; (408) 432-1900. FAX (408) 434-0507. **Circle No. 410**

Battery-charge controller. The ICS 1700 rapid-charge controller chip employs the Reflex charging method, which was patented by Christie Electric Corp. This method combines the charge current with regularly spaced, high-current negative pulses. The device incorporates eight techniques to determine when to end the charge. In 16-pin DIP and 20-pin SO packages, from $8.05 (10,000). **Integrated Circuit Systems Inc,** 2626 Van Buren Ave, Valley Forge, PA 19482. Phone (800) 220-3366; (215) 666-1900. **Circle No. 411**

Step-up regulators. The MAX731/732/733 and /752 dc/dc converters feature 80 to 95% efficiencies. The 731 accepts inputs of 2.0 to 5.25V and outputs of 5V at 200 mA. The 732 accepts inputs of 4 to 9.3V and outputs 12V at 200 mA. The 733 accepts inputs of 4 to 11V and outputs 15V at 125 mA. The 752 accepts inputs of 2 to 16V and provides an adjustable output from 2.7 to 15.75V at 200 mA. A logic-compatible shutdown pin allows direct μP control. The devices also include soft start and short-circuit protection. They are available in 8-pin DIPs and 16-pin SOIC packages. From $2.60 to $3.20 (1000). **Maxim Integrated Products,** 120 San Gabriel Dr, Sunnyvale, CA 94086. Phone (408) 737-7600. **Circle No. 412**

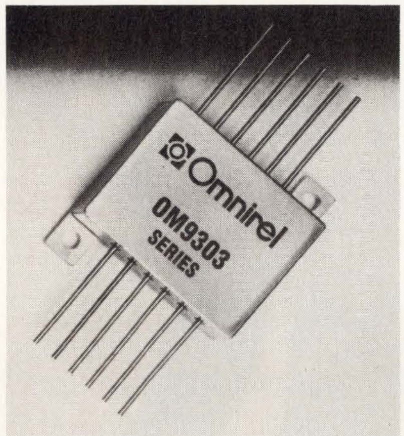
PC core-logic chip set. The Haydn chip set supports all cache or noncache Intel and AMD 386/486-based PC systems. The SL82C460 Haydn set includes a system controller and a bus controller. The optional SL82C465 is a direct-mapped cache controller. All devices function at 50 MHz and support slower speeds of 16, 20, 25, and 33 MHz. Separating the cache controller from the system logic allows greater design flexibility. $31 (1000). **Symphony Laboratories,** 2620 Augustine Dr, Suite 250, Santa Clara, CA 95054. Phone (408) 986-1701. FAX (408) 986-1771. **Circle No. 413**

Cache controller. The A38403 Microcache controller is compatible with all 486-based ISA, EISA, or Micro Channel Architecture systems at speeds to 50 MHz. You can organize the chip as a 2- or 4-way set-associative write-back cache, supporting 64, 128, or 256 kbits of memory. The device offers zero-wait-state read/write operations from cache memories organized with standard static RAMs. The A38403 comes in a 208-pin plastic quad flatpack. In 25-, 33-, and 50-MHz versions, $48.50, $54.40, and $74.10 (2500), respectively. **Austek Microsystems,** 2903 Bunker Hill Lane, Suite 201, Santa Clara, CA 95054. Phone (408) 988-8556. FAX (408) 980-6460. **Circle No. 414**

13-bit ADC for reducing noise in T1 transceiver applications. The Bt919 A/D converter is designed for next-generation High-Bit-Rate Digital Subscriber Line (HDSL) transceivers that allow T1 communications service over unconditioned and repeaterless twisted-pair copper wire. The ADC improves the S/N ratio in HDSL applications, resulting in less line noise and more reliable communications at high data rates. The ADC features 13-bit resolution and a 400-ksample/sec throughput rate. The ADC's monolithic CMOS construction reduces power consumption to 250 mW, compared with hybrid devices, which require as much as 2.8W. In an 84-pin PLCC, $60 (100). **Brooktree Corp,** 9950 Barnes Canyon Rd, San Diego, CA 92121. Phone (619) 452-7580. **Circle No. 415**

24-bit DSP chip. The DSP56002 24-bit digital signal processor (DSP) extends the company's 5600 series. Driven by a 40-MHz clock, the DSP chip delivers 20 MIPS and a 50-nsec instruction cycle time. Key features of the 56002 include two 256-word data RAMs, two preprogrammed data ROMs, and three independent execution units that operate in parallel. Also included is a PLL that accommodates almost any external system clock. $65 (1000). **Motorola Inc,** Microprocessor Group, 6501 William Cannon Drive W, Austin, TX 78735. Phone (512) 891-2030. **Circle No. 416**

Keyboard encoder. The K25C8 keycoder offers two bidirectional channels for communicating with a PC/AT/PS2 system and an 83- or 101-key IBM standard keyboard. Designed for custom keyboard applications, the chip handles scanning, debounce, and encoding of as many as 144 keys on an 8×18 matrix and can buffer as many as 122 key codes. In DIPs, plastic leaded chip carriers, and quad flatpacks, from $12.95 (2000). **USAR Systems,** 568 Broadway, #405, New York, NY 10012. Phone (212) 226-2042. **Circle No. 417**



Motor-control module. The OM9303SF is a hybrid module for 3-phase brushless dc motors rated to ⅓ hp. Needing only Hall-effect sensor ICs for commutation signals, the 1.5×0.333×0.305-in. module incorporates totem-pole output stages, an internal sense resistor, and a 9V zener reference. The module operates over a range of 10 to 30V and has a continuous output-current rating of 9.2A. The OM9303SF comes in industrial and military grades. From $240 to $285 (100). **Omnirel Corp,** 205 Crawford St, Leominster, MA 01453. Phone (508) 534-5776. **Circle No. 418**

Programmable logic sequencers. The Plus105-55 is a fully synchronous state machine with inputs that control the buried state registers and output registers. The device features a 55-MHz operating frequency and a 71-MHz clock frequency. A 45-MHz version, called the PLUS105-45, is also available. Both devices have 16 inputs, 6 buried J-K registers, and 8 J-K register outputs. Available in 28-pin plastic and ceramic DIPs and PLCC packages, from $8.80 to $14.75 (100). **Signetics Co,** 811 E Arques Ave, Sunnyvale, CA 94088. Phone (408) 991-2339; (408) 991-2000. **Circle No. 419**

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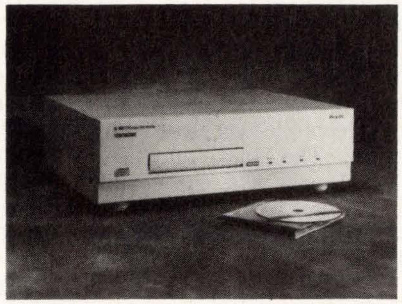
Test and Measurement

CIRCLE NO. 96

Computers & Peripherals



Desktop CD recorder. The CDD 521 records data in CD-ROM (XA), Photo CD, CD-1, and CD-Audio recording formats. A multivolume feature lets you record as many as 99 CD-ROM-format (lead-in, program-area, lead-out) volumes on a single disk. The CD-R media conforms to Orange Book specifications. A network software package from Meridian Data, called Netscribe, will be available in the fourth quarter of this year. $6000 without application software. **Philips,** Interactive Media Systems, Box 80002, 5600 JB Eindhoven, The Netherlands. Phone 31-40-736791. FAX 31-40-735772. **Circle No. 420**

40-MHz SPARCengine 2 system. The Galaxy 32+ integrates a Sun SPARCstation 2 within a rackmount VMEbus system. The system contains 16 Mbytes of RAM and doesn't require a memory upgrade to run Sun's Open Look software. An SBus-to-VMEbus adapter links the SPARCstation 2 to the VMEbus chassis. $16,595. **Ironics Inc,** 798 Cascadilla St, Ithaca, NY 14850. Phone (607) 277-4060. TLX 705742. **Circle No. 421**

Rackmount computer. The ST-4100E contains a 10-MHz 80286 through a 50-MHz 80486 μP. It runs Unix, DOS, Xenix, or OS/2 operating systems. The computer conforms to NEMA 12 specifications and withstands a 20g operating shock. Features include a 12-slot passive backplane, a 300W power supply, and a mix of three half-height disk drives. $2700 to $5900. **IBI Systems Inc,** 6842 NW 20th Ave, Fort Lauderdale, FL 33309. Phone (305) 978-9225. FAX (305) 978-9226. **Circle No. 422**

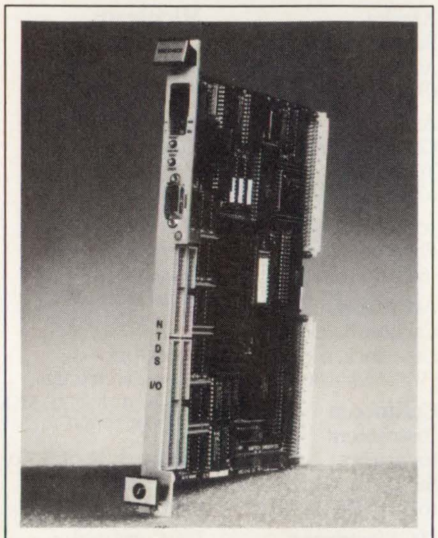
VMEbus graphics computer. The Eurocom 16 6U board provides 640×480-pixel graphics. It features a 25-MHz 68030 μP and 4 Mbytes of RAM, which is expandable to 8 Mbytes. A VGA monitor output port can drive EL-Display monitors directly. The board has three user-definable serial ports, a 20-bit parallel port, a mouse port, keyboard port, and a SCSI port. $3600. **American Eltec Inc,** 4340 Stevens Creek Blvd, Suite 204, San Jose, CA 95129. Phone (408) 244-4700. FAX (408) 244-5544. **Circle No. 423**

G-96 68030 SBC. The GESSBS-30 single-board computer contains a 32-MHz 68030 μP and 1 or 4 Mbytes of battery-backed static RAM. In addition, it can access 32 Mbytes of RAM on the bus. The board also has four sockets that accommodate as much as 2 Mbytes of EPROM, two serial ports, three 16-bit counter/timers, and a real-time clock calendar. It runs OS-9 software and has an expansion bus for attaching peripherals. $1950. **Gespac Inc,** 50 W Hoover Ave, Mesa, AZ 85210. Phone (602) 962-5559. FAX (602) 962-5750. **Circle No. 424**

Postscript printers for Mac. The IBM Laserprinters 10A and 6A attach to Apple's Macintosh. The Adobe Postscript printers provide 600×600-dpi resolution and let you adjust line widths. The printers automatically sense paper size and let you know when the output tray is full. The company's Print Quality Enhancement Technology detects and smooths angled lines and curves. Model 10A, $3995; Model 6A, $2695. **Lexmark International Inc,** 740 New Circle Rd, Lexington, KY 40511. Phone (800) 426-2468; (606) 232-6906. **Circle No. 425**

PDOS development system. The XVME-890 consists of a XVME-688 80386SX DOS-compatible VMEbus module, XVME-630 68EC030 VMEbus processor module with VMEPROM, hard- and floppy-disk systems, a 12-slot VMEbus backplane, and a 300W power supply. The backplane system lets you develop PDOS code on the XVME-688 host using DOS software and download the code to the XVME-630 target using the VMEbus instead of an RS-232C port. $12,500. **Xycom Inc,** 750 N Maple Rd, Saline, MI 48176. Phone (800) 289-9266; (313) 429-4971. **Circle No. 426**

ISDN primary-rate interface board. The PRI/211 ISA bus board provides an Integrated Services Digital Network (ISDN) Primary-Rate interface. The board features Automatic Number Identification and Dialed Number Identification Services for quick call-processing. Audiotex users can use interchange-carrier services such as AT&T's Info 2. The board contains an RJ-48C DSX-1 port and the company's PCM Expansion Bus. $2995. **Dialogic Corp,** 300 Littleton Rd, Parsippany, NJ 07054. Phone (201) 334-8450. **Circle No. 427**



VMEbus-to-NATO adapter. The NATO Hawke is a 32-bit VMEbus board that bridges NATO-4146C and MIL-STD-1397 B-, C-, and H-type interfaces for the Naval Tactical Data System (NTDS). A triple-port 512-kbyte video RAM interconnects a 68020 µP, the VMEbus, and the NATO port. You can dynamically configure the board as either a VMEbus master or slave, using A32:D32, A24:D16, or A16:D08 data transfers. Commercial version, $4931; ruggedized version, $5250. **Sabtech Industries Inc,** 5411 E La Palma Ave, Anaheim, CA 92807. Phone (714) 693-3500. FAX (714) 970-5377. **Circle No. 428**

ISA bus coprocessor board. The SPARCard 2, which contains a 40-MHz SPARC CPU, lets a computer run DOS/Windows and 3500+ SPARC applications simultaneously. It also contains 8 Mbytes of dynamic RAM (expandable to 64 Mbytes), an Ethernet controller, a SCSI controller, two SBus connectors, a serial port, and an audio port. $4145. The SPARCard 2 kit consists of the board with 8 Mbytes of RAM, a 213-Mbyte installed hard-disk drive, Solaris 1.0, and a color frame buffer, $6265. **Opus Systems,** 329 N Bernardo Ave, Mountain View, CA 94043. Phone (415) 960-4040. FAX (415) 960-4001. **Circle No. 429**

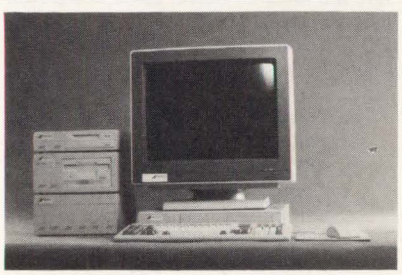
Tape storage system. The Mini-Library employs the Ciera 2.6-Gbyte tape drive and seven random-access cartridges to provide 18.2 Gbytes of tape backup for Novell networks. It transfers data at 48 Mbytes/minute. The system measures 28×17×34 in.

 CIRCLE NO. 97

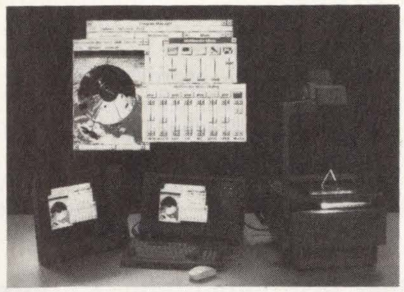
and operates from either 100 to 120V ac or 220 to 240V ac. $19,950. **Cipher Data Products Inc,** 10101 Old Grove Rd, San Diego, CA 92131. Phone (800) 862-4372; (619) 578-9100. FAX (619) 693-4430. **Circle No. 430**

External 2400-bps modem. The BOCAmodem 2400 external modem transfers modem-to-modem data as fast as 2400 bps and terminal-to-modem data as fast as 19.2 kbps. The modem conforms to CCITT V.22, V.22bis, and Bell 212A and 103 standards. Other features include a speaker with software volume control, two modular phone jacks, and an RS-232C port. $125. **Boca Research Inc,** 6413 Congress Ave, Boca Raton, FL 33487. Phone (407) 997-6227. FAX (407) 997-0918. **Circle No. 431**

Opto-22 digital I/O card. The DIO24 has 24 digital I/O lines for driving opto-22 equipment. Buffers permit an 8255 controller chip to drive 16-mA loads. A PAL device automatically configures the buffers for inputs or outputs. An optional 8254 chip provides three timer/counters. The ISA bus board has a switch-selectable base address and generates IRQ2 to IRQ7 interrupts. $149. Optional timer, $195. **Real Time Devices Inc,** Box 906, State College, PA 16804. Phone (814) 234-8087. FAX (814) 234-5218. **Circle No. 432**

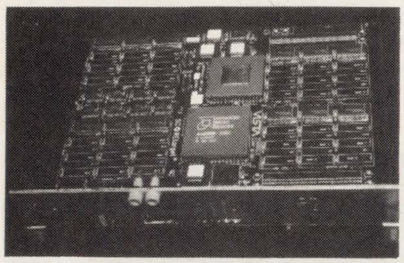


SPARCstation clones. The Solidstation 40 and 25 have 40- and 25-MHz SPARC processors, respectively. Standard configurations include a 207-Mbyte hard-disk drive; a 19-in. monitor; and three SBus expansion slots. The workstations also have from 8 to 64 Mbytes of RAM; 1 Gbyte of internal disk-drive capacity; and 20.8 Gbytes of external disk-drive capacity. The systems come with either the Solaris 1.0 or Motif/X11R4/X operating systems. $9990. **Solid Computer Corp,** 1450 Oakbrook Dr, Suite 300, Norcross, GA 30093. Phone (404) 416-6000. FAX (404) 416-6511. **Circle No. 433**



TFT projector/monitor. The Prism thin-film-resistor panel operates as an overhead projection panel or stand-alone monitor. In either mode, the panel displays 185,000 colors and accepts inputs from NTSC, PAL, VGA, or Macintosh video sources. The 7-lb display measures 15.2×12.5×2 in. $8495. **Dolch Computer Systems,** 372 Turquoise St, Milpitas, CA 95035. Phone (408) 957-6575. FAX (408) 263-6305. **Circle No. 434**

VMEbus AMD 29000 development systems. The Scoretarget features an AMD29000 or an AMD29050 and an Am29027 coprocessor. The board also contains two RS-232C ports, programmable timers, and as much as 4 Mbytes of instruction static RAM (SRAM) and 2 Mbytes of data SRAM. An optional VMEbus-card-cage system contains a power supply and fan. $9995; rack system, $14,500. **Vista Controls Corp,** 27825 Fremont Ct, Valencia, CA 91355. Phone (805) 257-4430. **Circle No. 435**



68332 single-board computer. The SBC332 has a 16.78-MHz MC68332 μP, 1 Mbyte of static RAM, and 1 Mbyte of EPROM. The embedded control board has Motorola's BCC P1- and P2-compatible connectors and measures 2.3×6.25 in. The board also contains the company's Forth kernel in EPROM. $249 (25). **Vesta Technology Inc,** 7100 W 44th Ave, Suite 101, Wheat Ridge, CO 80033. Phone (303) 422-8088. FAX (303) 422-9800. **Circle No. 436**

Fiber Distributed-Data-Interface Concentrator. The 1001 FDDI concentrator provides eight single-attached M-ports. An optional card provides A and B ports for single-attached, dual-attached, cascade, or dual-home configurations. Network management software complies with SMT 6.2. $12,995. **Crescendo Communications,** 710 Lakeway Dr, Sunnyvale, CA 94086. Phone (408) 732-5942. FAX (408) 732-4604. **Circle No. 437**

Digital-audio evaluation board. The DSP56401 lets you evaluate digital-audio applications for Motorola's DSP56401 audio receiver. It has audio input and output ports for balanced and

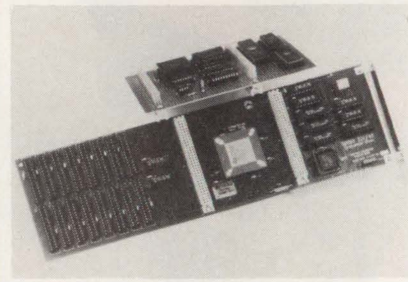
 CIRCLE NO. 101

CIRCLE NO. 110

RATING		VALUE	UNIT
OPER. VOLTAGE		5 ±0.5	V
OPER. TEMPERATURE		-10 TO 70	°C
CURRENT CONSUMPTION	OPER.	15 (MAX)	mA
	STAND-BY	2 (MAX)	μA
	BACK-UP	0.5 (TYP)	μA

unbalanced lines. It also contains ports to communicate with Motorola's DSP560001, DSP56002, and DSP56156 chips. $495. **Spectrum Signal Processing,** Suite 301, 3700 Gilmore Way, Burnaby, BC V5G 4M1, Canada.
Circle No. 438

Operator microterminals. The CTM-380 and CTM390 have a 1-line × 24-character display that is visible in low-light environments. The units have either a 51-key alphanumeric keypad or a 23-key numeric keypad. The units weigh 1.7 lbs and have an ABS plastic case that measures 9×5×1.5 in. The CTM380 communicates with a host via an RS-232C port; the CTM390 uses an RS-422 port. $795 (OEM qty). **Burr-Brown Corp,** Box 11400, Tucson, AZ 85734. Phone (800) 548-6132; (602) 746-1111. FAX (602) 889-1510. TWX 910-952-1111.
Circle No. 439



ISA bus DSP board. The Turbo 320/40 contains a 40-MHz TI TMS320C30 DSP chip and as much as 8 Mbytes of static RAM. Dual 96-pin DIN connectors accept a range of daughter boards ranging from prototype to A/D boards. The company can also build custom boards on a quick turnaround basis. The development system runs all of TI's development software. From $995. **Wintriss Engineering Corp,** 4715 Viewridge #200, San Diego, CA 92123. Phone (800) 733-8089.
Circle No. 440

Isolated power-supply board. The PC-462 delivers two outputs from 0 to 20.475V and from 0 to −20.475V at 250 mA max. The ISA bus board also delivers 0 to 6.1425V and 0 to −6.1425V outputs at 1A max. A software-programmable 12-bit A/D converter controls each output independently. The board isolates each output from the ISA bus by 250V rms. $1195. **Datel Inc,** 11 Cabot Blvd, Mansfield, MA 02048. Phone (508) 339-3000.
Circle No. 441

ARINC 629 adapter. The PC629-1 lets you develop, test, and simulate products for ARINC 629 avionics data bus using an ISA bus computer. A protocol processor and the ISA bus have access to a 128k × 8-bit dual-port RAM. Three software packages include a script compiler, a debugger, and a driver library. $4995. **Ballard Technology,** 1216 NW 75th St, Seattle, WA 98117. Phone (206) 782-8704.
Circle No. 442

Notebook computer. The NB2500 has a 25-MHz AM386DXL μP and a 128-kbyte cache RAM. It also has 4 Mbytes of RAM, an 80-Mbyte hard-disk drive, a 1.44-Mbyte floppy-disk drive, and a FAX/modem that conforms to CCITT Group 3 standards. A 9-in. supertwist backlit LCD screen provides 64 levels of gray and 640 × 480-pixel VGA resolution. $2695. **Micro Express,** 1801 Carnegie Ave, Santa Ana, CA 92705. Phone (714) 852-1400.
Circle No. 443

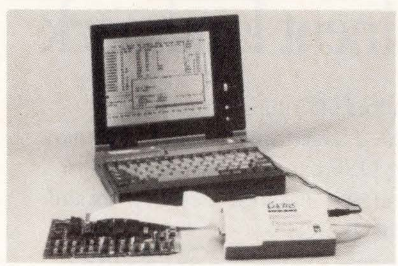
CAE & Software Development Tools

Debugger for Intel 80960. Using Codetap 960 CA, an engineer can do in-circuit debugging of code for Intel's 80960 superscalar microprocessor. The product consists of a target access probe that uses emulation technology to provide access and control for executing and debugging code; an RS-232C communications adapter that connects to PC or Sun workstations; and debugging software. The package provides transparent code execution in the target to maximum clock frequency of the i960 processor, using no wait states. It requires no target memory, I/O ports, or interrupts. No monitor linking or other code modifications are necessary to use the product. The product also supports all features of the i960 CPU, including burst mode, pipelines, and different bus widths. $7500 when bundled; available unbundled. **Applied Microsystems Corp,** 4020 148th Ave NE, Redmond, WA 98073. Phone (800) 426-3925; (206) 882-2000. FAX (206) 883-3049.
Circle No. 444

Layout tools for Xilinx FPGAs. The latest version of the Neoroute tool set runs three to five times faster than Xilinx layout routines. The software requires fewer iterations to achieve placement and routing and reduces the occurrence of clock-skew problems on Xilinx 3000 devices. The software runs on Intel 386/486 computers operating under MS-Windows and on Unix-based workstations running the X-Window System and Motif. PC version, $7500; workstation version $12,000 **NeoCAD Inc,** 2585 Central Ave, Boulder, CO 80301. Phone (303) 442-9121. FAX (303) 442-9124.
Circle No. 445

User-interface development tool. Using Open Interface tool kit, a developer builds graphical user interfaces that are instantly portable across Macintosh, DOS, OS/2, Unix, and VMS operating systems. The developer can also tailor the resulting GUIs to match the native look and feel of the major windowing environments (Macintosh, Windows, Presentation Manager, Motif, and Open Look). Open Interface consists of the Open Editor and a set of libraries for each windowing environment. The user draws the application interface using Open Editor, a "what-you-see-is-what-you-get" interface builder. The editor generates portable C code and resource files for the execution and description of the interface. The developer then customizes the C code to link in the application to the interface. Development package for Windows, $7000; runtime license, $95. **Neuron Data Inc,** 156 University Ave, Palo Alto, CA 94301. Phone (415) 321-4488. FAX (415) 321-9648. **Circle No. 446**

OTDR software for logging to disk. Waveview software for the MW9040A optical-time-domain reflectometer stores data acquired by the OTDR on a DOS PC. Users can analyze the data and print on laser or dot-matrix printers; you can also perform loss/splice calculations and zoom in to view individual data points. The software runs on any 80286 or later PC/AT using VGA graphics. $750. **Anritsu Wiltron Sales Co,** 685 Jarvis Dr, Morgan Hill, CA 95037. Phone (408) 776-8300. FAX (408) 776-1744. **Circle No. 447**



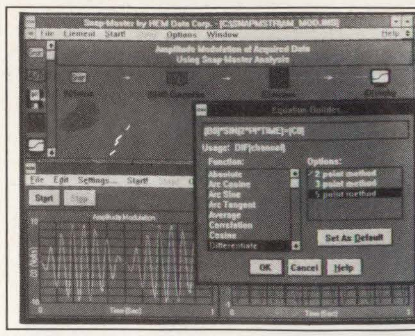
Firmware development system. Using the Integrated Development System (IDS), the designer can write, debug, and execute firmware for embedded 8-bit processors, including the 8051, the HC11, and the Z80 families. The programmer uses a menu interface to write, debug, and execute the firmware. This system works on a Cactus Logic target board (before hardware development) or on the target system itself. The system accommodates most compilers and assemblers, including Avocet and Archimedes C compilers. The software provides watch windows, as many as 100 breakpoints, simulated I/O, real-time running at all clock speeds, zero-wait states, and performance-analysis histograms. It also can use EMS or XMS memory for improved performance. Requires PC and parallel port, $2435. **Cactus Logic,** 180 N Vinedo Ave, Pasadena, CA 91107. Phone (800) 847-1998; (818) 796-1773. FAX (818) 796-6011. **Circle No. 448**

Software for PLDs. CUPL PLDMaster 4.2 provides a development environment that can map any logic design into the target architecture. The tool accepts input schematics from Viewlogic, OrCAD, and Schema and reduces the logic design to a set of Boolean expressions. The output format is a superset of Berkeley PLA format and suits Xilinx and Actel tools. The output format is also a superset of the Open-Abel output from Data I/O. Users can obtain EDIF 2.0-formatted output from the tool for back-annotation and schematic regeneration. All other original CUPL features have been retained. For MS-DOS, $1495. **Logical Devices Inc,** 1201 NW 65th Pl, Fort Lauderdale, FL 33309. Phone (305) 974-0967; in Canada, (604) 654-6861. **Circle No. 449**

ICE for 68EC000 microprocessor. The UEM emulator suits the Motorola 68EC000 processor, a 68000 derivative for embedded control. The emulator gives firmware engineers a source-level debugger, 131,072 hardware breakpoints, a real-time performance analyzer, and a memory-access monitor. $7500. **Softaid Inc,** 8300 Guilford Rd, Columbia, MD 21046. Phone (800) 433-8812; (410) 290-7760. FAX (410) 381-3253. **Circle No. 450**

Core-porting kits for real-time OS. Core-porting kits are available for the Sun SPARC II, the Mips R3000, Intel i860 CPUs, and Motorola's 68040 and 88000. Core-porting kits let developers modify the LynxOS kernel and develop the drivers required to run LynxOS on their chosen hardware. A core-porting kit includes the OS kernel and libraries for hardware-dependent modules and drivers, a development environment, system call and library test suites, a kernel debugger and utilities, and example drivers developed by the manufacturer. $25,000 to $50,000 per core-porting kit. **Lynx Real-Time Systems,** 16780 Lark Ave, Los Gatos, CA 95030. Phone (408) 354-7770. FAX (408) 354-7085. **Circle No. 451**

Analysis and acquisition software for MS-Windows. Snap-Master Analysis software for MS-Windows lets the user construct equations that operate on stored data or data acquired with Snap-Master Data Acquisition software. The software performs arithmetic, trigonometric, logarithmic, and statistical functions, as well as auto- and cross-correlation, smoothing, differentiation, and integration. The software plots data during acquisition, streams data to disk at 250 ksamples/sec, and pretests the throughput to ensure that the system can handle user requests. Software runs on PC/AT, 386, 486, or PS/2 computers with MS-Windows 3.0 or 3.1. Analysis package, $495; acquisition package, $995. **HEM Data Corp,** 17336 12 Mile Rd, Suite 200, Southfield, MI 48076. Phone (313) 559-5607. FAX (313) 559-8008. **Circle No. 452**



HDL code from graphic models. ExpressV-HDL 2.0 generates both VHDL (VHSIC Hardware Description Language) and Verilog code from the same graphic behavioral model, called a Statechart. This tool lets engineers analyze, validate, and revise state models before performing CAE simulation and synthesis. This release also provides time-based or synchronous animation of the graphic models. Another feature of the tool is bit-array and bit-manipulation extensions to Statecharts. $32,500. **i-Logix Inc,** 22 Third Ave, Burlington, MA 01803. Phone (617) 272-8090. FAX (617) 272-8035. **Circle No. 453**

Reliability prediction. Industrial Reliability Prediction Program RBC-2.1 predicts equipment reliability according to Bell Communications Research Technical Reference TR-NWT-000332, Issue 3, dated September of 1990. For communications and industrial equipment, the software provides more lenient failure models than those mandated by standard MIL-HDBK-217. The software lets you make predictions using the parts-count method, laboratory test, and field tracking data. Single license, $1700. **Powertronic Systems Inc,** 13700 Chef Menteur Hwy, New Orleans, LA 70129. Phone (504) 254-0383. FAX (504) 254-0393. **Circle No. 454**

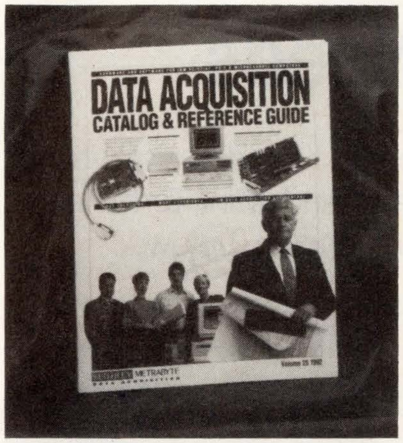
Digital-filter-design software. Digital-Filter-Design software produces filter designs that meet arbitrary response specifications. Besides meeting limits on passband-ripple and reject-band attenuation, this software designs filters having weighting factors, multiple passbands, reject bands that have uneven attenuation requirements, as well as phase equalization and envelope delay correction. The software provides on-screen editing, save and load of ASCII files, and printouts of filter specifications, parameters, and responses. The software runs on IBM PCs and compatibles; a math coprocessor is optional. $495 to $695. **Hanson Engineering,** 708 Bettyhill Ave, Duarte, CA 91010. Phone (818) 359-7036. **Circle No. 455**

Board-design software. Tango-PCB version 2.1's improvements include speeding most operations by 10 to 30%, compressing files, an Editing Polygon command, block operations allowing items on one layer to be moved to another layer, and metric conversion assistance. A partial list of other extensions includes auto-save at user-specified intervals, a see-through display of items beneath other items, and sorting of component libraries. Tango-PCB Plus, $995. **Accel Technologies Inc,** 6825 Flanders Dr, San Diego, CA 92121. Phone (619) 554-1000. **Circle No. 456**

Re-engineering tool for C. Refine/C reads C source code and produces structure charts, data-flow diagrams, variable tables, function tables, type tables, and reports of coding-standards violations. All reports can be browsed on line using a graphical interface built on the X-Window system. You can also send reports to a Postscript printer. The product can export to Software Through Pictures, and it accepts both ANSI C and K&R C. Single license, $3500. **Reasoning Systems,** 3260 Hillview Ave, Palo Alto, CA 94304. Phone (415) 494-6201. **Circle No. 457**

Gridless router for DOS. The CADstar Advanced Router, a gridless, 100% rip-up and retry, shove-aside router, is available for DOS. The router uses 0.001-in. resolution to fit more traces in a given area than a grid would allow and to route to the precise spacings required for fine-pitch pin-grid arrays and surface-mount packages. The software routes as many as 16 signal layers simultaneously. A single-pass layout lets the designer analyze the potential routing success of an initial strategy before final routing. The rip-up and retry algorithm reroutes traces that cannot be completed, and a shove-aside algorithm moves traces aside to provide more room and complete denser boards. $2750. **Racal-Redac,** 238 Littleton Rd, Westford, MA 01886. Phone (508) 692-4900. **Circle No. 458**

VLSI layout editor. The VALE (VLSI Advanced Layout Editor) aids the design of masks for complex ICs. The mask-design database created by the tool can be translated to industry-standard formats such as GDS and CIF. Users can manage hierarchical designs, edit subcells in context, and handle as many as 37 layers of mask generation. Database resolution is 32 bits. For Sun SPARCstations running X-Window graphics, $2995/end user; annual support fee/license, $400. **Phase Three Logic Inc,** 1600 NW 167th Pl, Beaverton, OR 97006. Phone (503) 645-0313. FAX (503) 645-0207. **Circle No. 459**



PC-based data-acquisition products. This 288-pg catalog describes data-acquisition hardware and software products. It includes data-acquisition boards; PC instrumentation boards; communications boards; industrial I/O systems; software for acquisition, analysis, and graphics; data-acquisition instruments; and integrated system products. A 14-pg guide helps you select the right product for your application. **Keithley Metrabyte,** 440 Myles Standish Blvd, Taunton, MA 02780. Phone (508) 880-3000. FAX (508) 880-0179. **Circle No. 692**

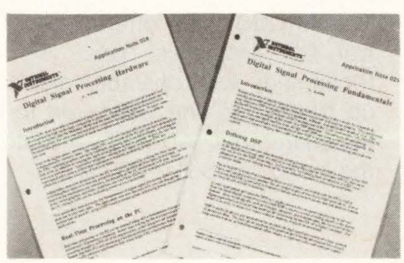
Data acquisition for lab and industry. The 74-pg booklet *How to Measure in Lab and Industry* explains data-acquisition applications for aerospace, process industry, laboratories, quality control, automotive testing, and environmental testing. Topics include types of data-acquisition hardware, connecting thermocouples, RTDs, thermistors, strain gauges, and pressure transducers. It discusses programs for analyzing and presenting data, and the advantages of each. A demo disk for IBM or Macintosh PCs is also available. **Dianachart Inc,** 101 Round Hill Dr, Rockaway, NJ 07866. Phone (201) 625-2299. FAX (201) 625-2449. **Circle No. 693**

App note on audio amplifiers. Application note AN1308 describes 100 and 200W, single-channel high-fidelity amplifiers using plastic-package bipolar transistors as outputs and drivers. It covers design philosophies for both the amplifiers and their power supplies. The note explains how the amplifiers are used for high-end and professional audio applications. **Motorola Inc,** Literature Distribution Center, Box 20924, Phoenix, AZ 85063. Phone (800) 441-2447 or contact local office. **Circle No. 694**

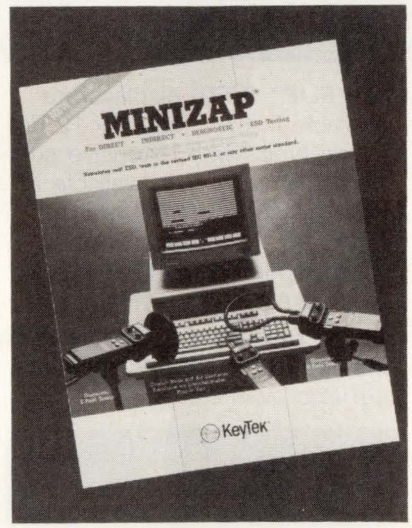
Listing of fiber-optic suppliers. The revised and updated *Worldwide Fiber-Optic Suppliers Directory* for 1992-1993 lists more than 1000 suppliers in more than 30 countries. The listing provides company name, address, phone and fax numbers, products manufactured, and marketing contacts. The publication comes in a compact 5×7-in. size to fit easily on a desk or in a briefcase for easy reference. $50 (plus $5 shipping charge outside US); disk versions for IBM or Macintosh PCs (suppliers' names and addresses only), $125; for database version with sortable fields, $500. **KMI Corp,** 31 Bridge St, Newport, RI 02840. FAX (401) 847-5866. **INQUIRE DIRECT**

Compilation of computer systems. The 96-pg source book *Computer Systems Edition I* introduces 15-slot rackmount and benchtop chassis, a rackmount chassis with a 12-in. VGA monitor, and dc-powered chassis. Other offerings include 386SX-, 386DX-, and 486DX-compatible computer systems; 486SX, 486DX, and 386DX modular mother boards; and multimedia products. **Industrial Computer Source,** 10180 Scripps Ranch Blvd, San Diego, CA 92131. Phone (619) 271-9340. **Circle No. 695**

Broadband RF instruments. This 4-pg brochure describes the vendor's line of broadband RF field-strength meters for EMF measurement in the health and safety industries. It includes recently introduced instruments and probes for measuring in compliance with the IEEE/ANSI C95.1-1992 EMF Standard. **Holaday Industries Inc,** 14825 Martin Dr, Eden Prairie, MN 55344. Phone (612) 934-4920. FAX (612) 934-3604. **Circle No. 696**



App notes on DSP fundamentals and hardware. The application note *Digital Signal Processing Fundamentals* explains how to develop PC-based, data-acquisition, and analysis systems using digital-signal-processing (DSP) technology. It elaborates on how you can use DSP not only for signal processing and FFTs, but also for very high-speed, real calculations of large amounts of data. *Digital Signal Processing Hardware,* the second application note, examines the fundamentals of DSP boards and their use in real-time tasks. It explains how you can use DSP boards to change the architecture of your PC for more processing power and improved performance. **National Instruments,** 6504 Bridge Point Pkwy, Austin, TX 78730. Phone (512) 794-0100; in US and Canada, (800) 433-3488. FAX (512) 794-8411. **Circle No. 697**



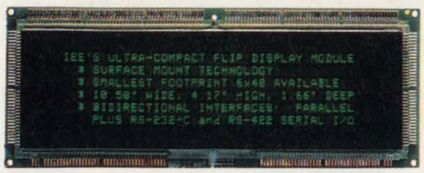
Digital ESD simulator groups. The 6-pg brochure describes how the Minizap ESD simulator model groups perform both direct and indirect ESD testing. It discusses the equipment for doing all three modes of ESD testing: direct, indirect, and diagnostic. **Keytek Instrument Corp,** 260 Fordham Rd, Wilmington, MA 01887. Phone (508) 658-0880 or contact local office. FAX (508) 657-4803. **Circle No. 698**

"How-to" newsletter for developers. *Advanced Technology for Developers* provides success stories along with tips for developers using advanced technology. Some of the upcoming articles will deal with time-series forecasting—basics, advanced techniques, application examples; building neural networks to handle unusual events; making fuzzy logic "clear"; and neuro-genetic algorithms for trading. 1-year subscription: $99, US; $179, outside US. **High-Tech Communications,** 103 Buckskin Ct, Sewickley, PA 15143. Phone (412) 741-7699. **INQUIRE DIRECT**

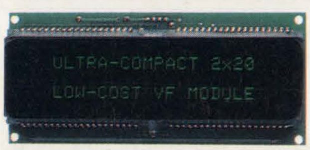
The "One-Stop" Source
For All Your Display Needs

IEE manufactures a complete line of Vacuum Fluorescent, Liquid Crystal, and DC Plasma displays as well as Interactive Touchscreens and Mini-Terminals. A few models in our extensive display family are shown below.

Vacuum Fluorescent

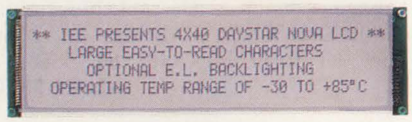


- Our **FLIP™** (VFD) displays are available in 5×7 and 5×12 dot matrix types with extensive software features. Also available in **wide-operating temperature** (−40 to +85°C) versions. Applications: industrial, medical, telecommunications, etc.
- **Highly ruggedized "ER" version modules** (with MIL components) are also available.



- The **"NO-FRILLS"™** and **"NINETY SERIES"™** are IEE's **low-cost VFDs** with a high-priced appearance and are ideal for OEM applications such as copiers, POS terminals, pay telephones, etc.
- **"Industrial Strength" FLIPs** feature 9, 11, and 15mm characters, making them easy to read from longer distances—typical on factory floors and in PLC applications.

Liquid Crystal

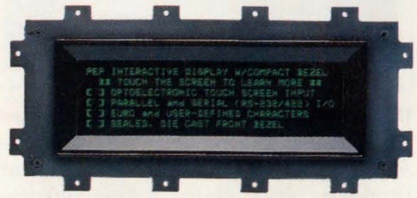


- The **DAYSTAR NOVA™** series is available in reflective, and EL- and LED-backlighted types. DAYSTAR NOVA is designed for applications where direct sunlight readability and ultra low power consumption is required. Operates on a single +5VDC supply.
- DAYSTAR NOVAs offer the **widest available operating temperature range (−30 to +85°C)**, a wide viewing angle and high contrast. Built-in temperature compensation is a **unique IEE** standard feature.

DC Plasma

- The **ARGUS™** line offers flicker-free DC plasma flat panel technology with character fields up to 480, in line widths up to 40 characters. ARGUS eliminates the need for bulky CRTs.

Interactive Touchscreen



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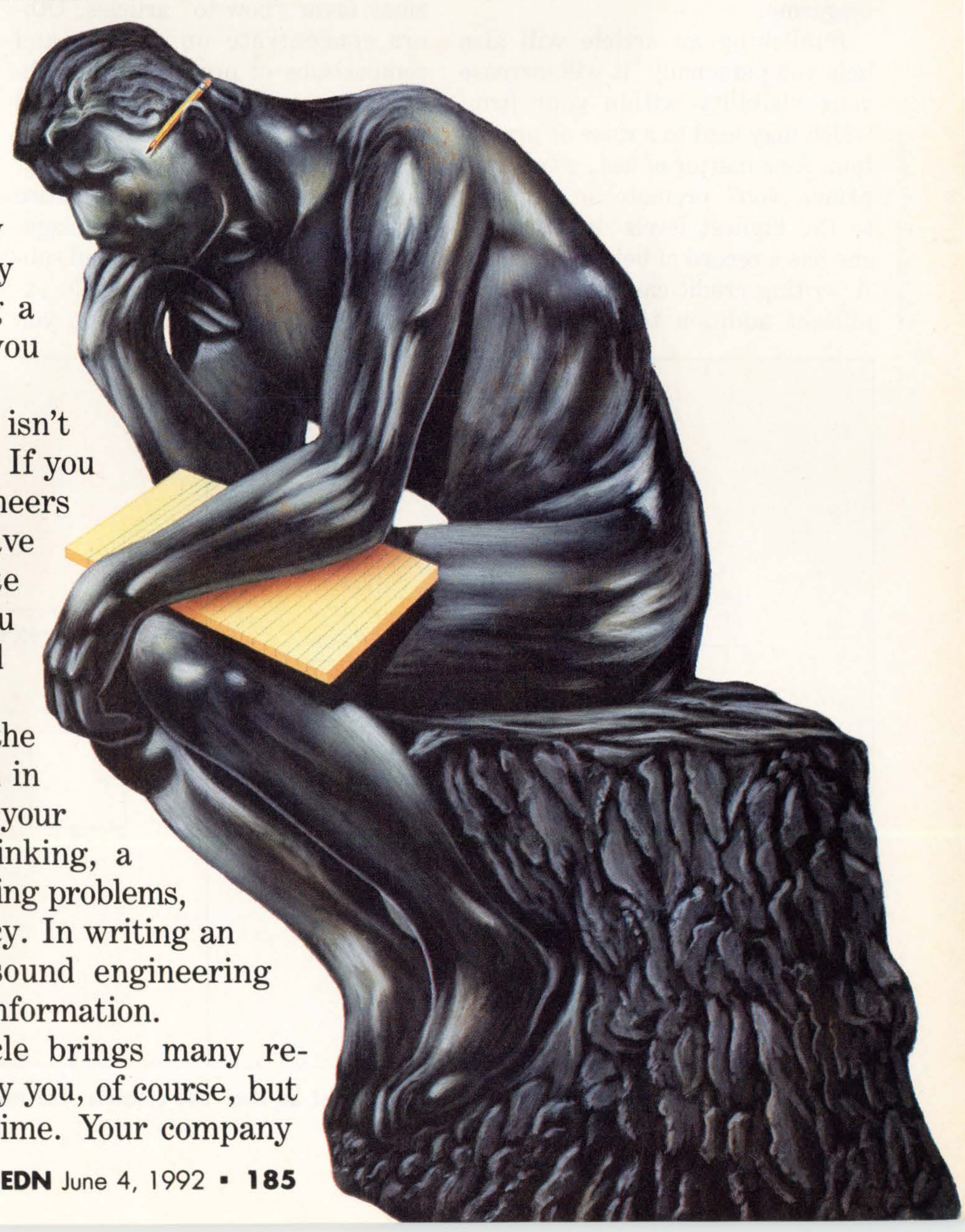
JAY FRASER, Associate Editor



Did you ever read an article in a technical magazine and say to yourself, "I could write something like that"? Even if you've felt that way many times, you probably never got around to writing a technical article because you didn't know where to start.

Writing technical articles isn't as difficult as it may appear. If you have information that engineers will find useful, and you have the ability to communicate clearly, with a little work, you could become a published writer.

Technical writing involves the same disciplines you learned in engineering school and use in your work every day—logical thinking, a step-by-step approach to solving problems, thoroughness, and consistency. In writing an article, you simply apply sound engineering practice to communicating information.

Writing a technical article brings many rewards. The magazine will pay you, of course, but you may be paid a second time. Your company may give you a bonus or other award if your name and affiliation appear on a technical article.

High-tech firms understand the importance of their employees' being published. Articles that appear in widely read magazines enhance the company's image. Readers give more credibility to articles that include a company's products than they do to advertisements for those products. Your company may grant you time off to write your article, and the people in your company's marketing or public-relations department can be helpful to you in many ways as you're writing and dealing with the editors of the magazine.

Publishing an article will also help you personally. It will increase your visibility within your firm, which may lead to a raise or promotion. As a matter of fact, some companies won't promote an engineer to the highest levels unless he or she has a record of being published. A writing credit can also be a significant addition to your resume. And, most important for some people, you'll get the satisfaction of seeing something you've written in print.

Understand your readers

The first step in publishing an article is to choose the magazine you want to write for and read it carefully. It's essential that you understand who the magazine's readers are. Most technical publications have a highly specialized audience. Make sure the article you have in mind will be aimed directly at them and will provide useful information.

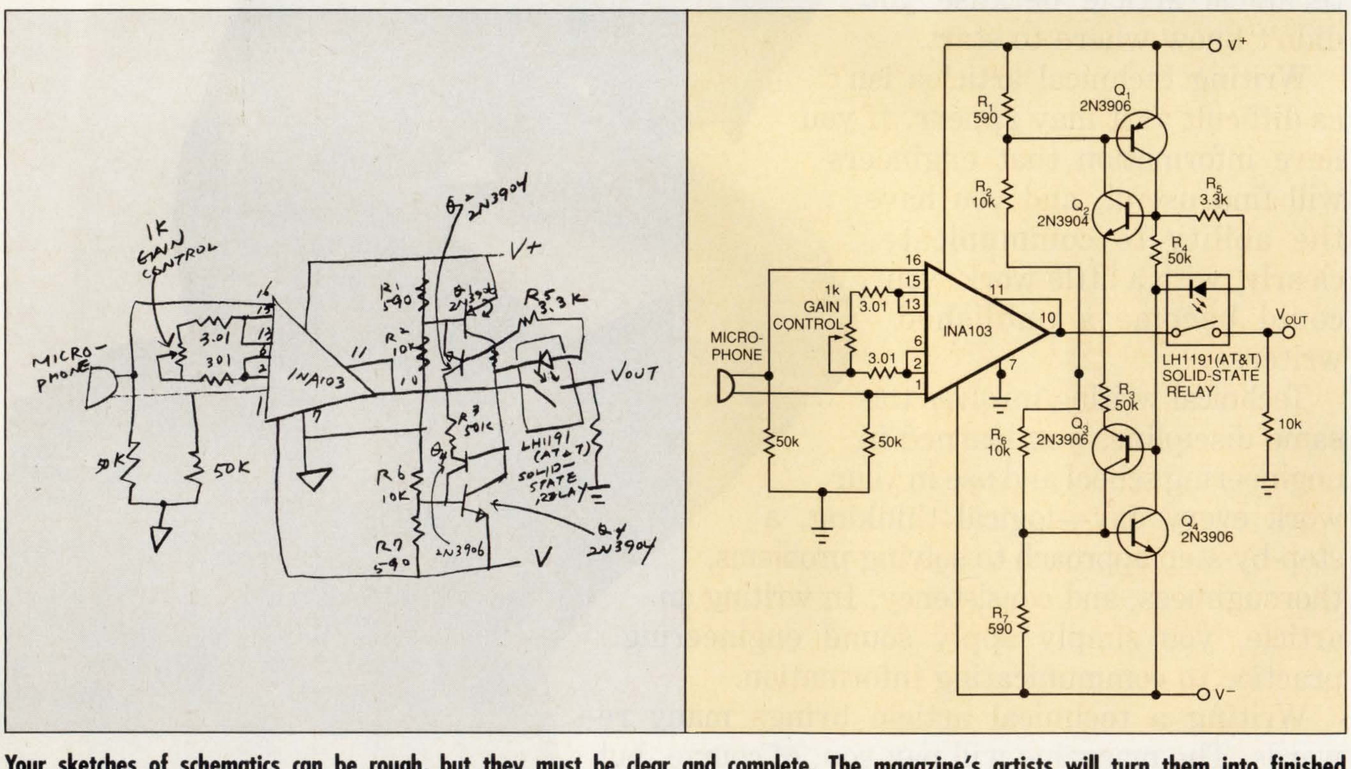
Note the types of articles the magazine publishes. Some magazines favor "how-to" articles. Others concentrate on surveys and comparisons of products. Still others print articles on nontechnical subjects such as career issues.

Having examined your target, don't research and write an entire article and send it off to the magazine. Write a proposal first and submit that. Your proposal should explain the type of information you have to offer the readers, how it will help them in their jobs, and the approach to the material you want to take. Make sure the information you want to provide isn't readily available in other publications. You should also mention any writing credentials you have, such as technical papers or application notes you've worked on.

Even if the editor likes your proposal, he or she may suggest additions or deletions or even a different approach. Don't let this discourage you. It would be unusual if your proposal were approved without any changes. Writing a proposal rather than a complete article will save you time and effort in the long run.

The editor may want to know more about what you have in mind and may ask you for a detailed outline. Working up an outline will help you determine what your article should include. You may find that you're trying to cram in too much and you'll have to trim back. On the other hand, to cover the topic thor-

Illustration by Tom Szumowski



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oughly, you may have to write a multipart article.

In addition, the editor may want to see a sample of your writing: Send something you've done recently. Don't drag out a paper you did in college. If you don't have anything new on hand, try writing the first page or two of the article you're proposing.

If you get the go-ahead for your article, start to work on it as soon as you can. Technology changes rapidly and the information you're dealing with could soon be superseded. If you delay too long, there's also the chance that someone writing for another magazine will beat you into print.

The editor may also send you some material that explains the magazine's requirements for style and format. Follow the rules closely. In the end, you will save everyone, including yourself, extra work.

Write the way you speak

You should write as if you were talking to a colleague or friend. Try to address the reader as "you," because it helps draw him or her into your article. Strive for clarity and simplicity in your writing. Don't forget that your main purpose is to convey information, not dazzle the reader with your style.

It's a good idea to tell your readers as soon as possible—in the first paragraph if you can manage it—how they will benefit from your article. Give them a reason to read on.

Try to develop your thoughts logically and sequentially. If your article lends itself to chronological organization, use it, even if you think it's old fashioned. The primary purpose of the structure of your article, like the style, should be to help the reader understand the subject matter.

Avoid jargon. Every area of engineering has its own specialized words and phrases. You probably use them every day without thinking. But that doesn't mean your readers will understand them. For the same reason, be careful about using acronyms. When in doubt, spell it out.

Also avoid using the passive voice in your writing. Instead of writing "the result can be obtained," say "you obtain the result." Changing the passive voice to active will tighten the text and make it easier to read. Engineers are constantly criticized for relying on the passive too much, and the criticism is justified for the most part. Among other sins the passive voice commits are obscuring meaning, slowing down the text, and keeping the reader at a distance.

Your main purpose is to convey information, not to dazzle the reader with your writing style.

Include all the information readers will need, such as part numbers, component values, and formulas. Make sure you cover your topic thoroughly. Don't be afraid of putting in a little too much information. Anything extraneous can be taken out by an editor. It's much easier for an editor to pare down the information you supply than to try to fill in gaps in your manuscript. But don't forget, magazines don't have unlimited space. They also don't necessarily have infinitely patient editors. Try to be concise.

Sometimes it's difficult to decide how much detail you should include. You may want to explain precisely how you solved a problem, but a detailed explanation that runs on for four of five paragraphs will bring your article to a dead stop. Consider putting information like that in a box, which is a place to refer for additional information. That way, readers who want the information will have access to it, and other readers won't lose interest.

Another part of the editor's job is to make sure that the grammar, spelling, and punctuation of your article are correct. That doesn't mean you shouldn't try to make them as accurate as possible. Many good reference books on English usage are available, and you can also ask someone in your marketing or public-relations department to proofread your manuscript before you send it in. The better job you do with the mechanics, the more the editor can concentrate on your article as a whole.

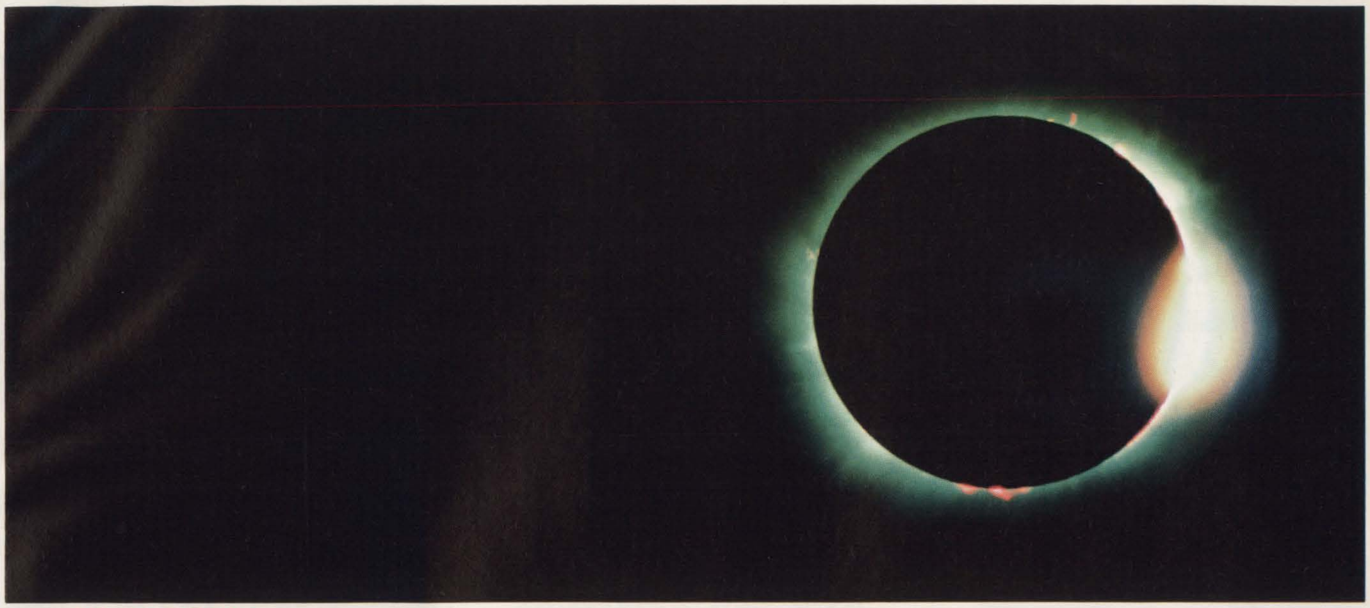
Don't write an advertisement

If you used an instrument or component in developing your article, you may have used one of your company's products because that's what you're most familiar with. However, you should make sure the focus of the article is generic, covering what an engineer would do with that *type* of product, rather than how well your company's product performed.

As you're writing, think about what you'll need to illustrate your article—schematics, photos, charts, graphs, or something else. If you have the material, send it in with your article. If you don't, include your suggestions. Always write a caption for every illustration you submit.

If you want to use schematics for illustrations, make sketches of them. The editor won't expect your sketches to be highly polished, but they must be clear and complete. Label all the components and use all the necessary symbols.

After you've completed your article, put it aside for a day or two, then read it again. You may be surprised at the errors you find and the passages that seem unclear. On the other hand, you may be unable to find troublesome spots in your article. It's not easy to step back and evaluate your own work objec-



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tively. You may want to ask a colleague to read your manuscript and get his or her suggestions about what you can improve.

After you send in your article, the magazine will direct it to a staff editor who specializes in the subject you've written about. He or she may call you up and ask you to clarify something you've written. The editor may even ask you to revise some parts of your article. This isn't unusual, even for experienced writers.

Working up a detailed outline will help you determine what your article should include.

Once your article is edited, it may be sent back to you for a final check. In this case, you should make sure any changes or additions the editor has made haven't altered the meaning you wanted to get across. Also make sure the captions are attached to the correct illustrations.

After you've completed checking your article, send it back to the magazine. You'll soon see it in print, receive your check in the mail, and reap the other rewards of being a published technical writer. EDN

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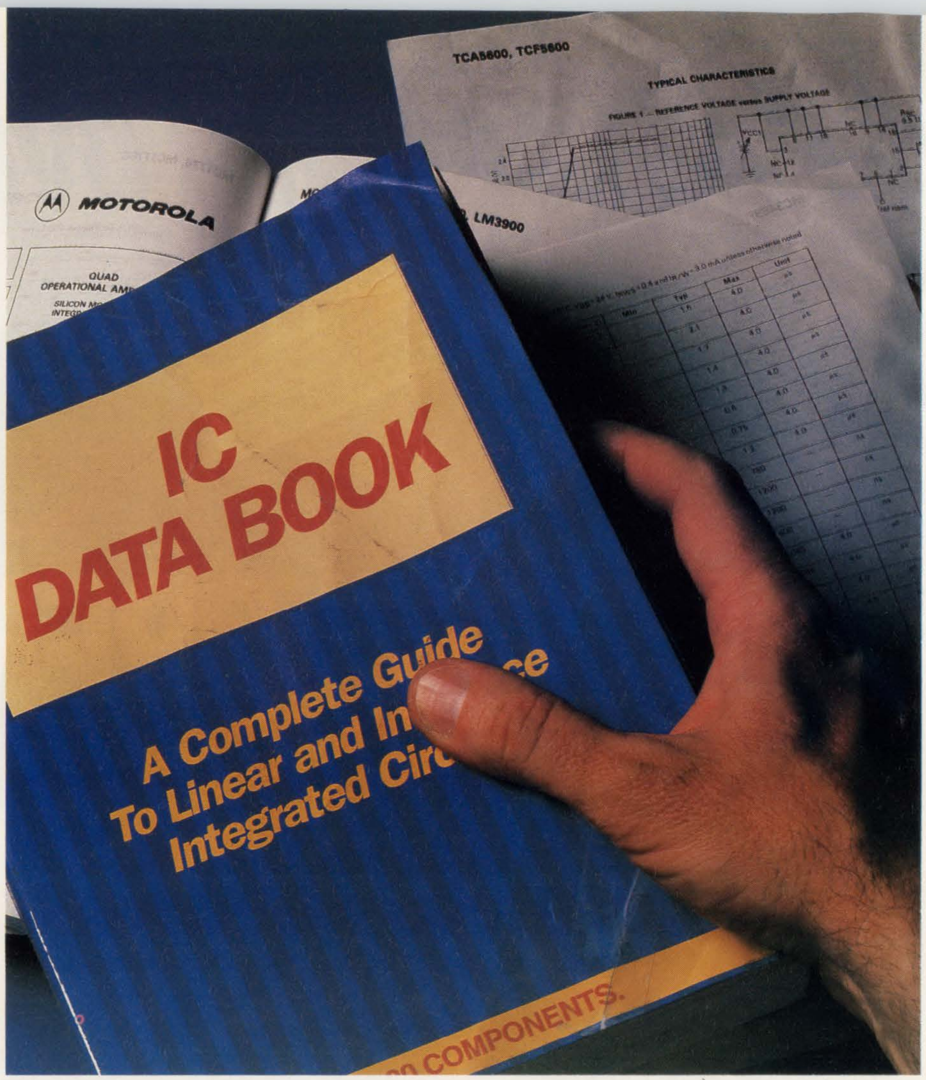

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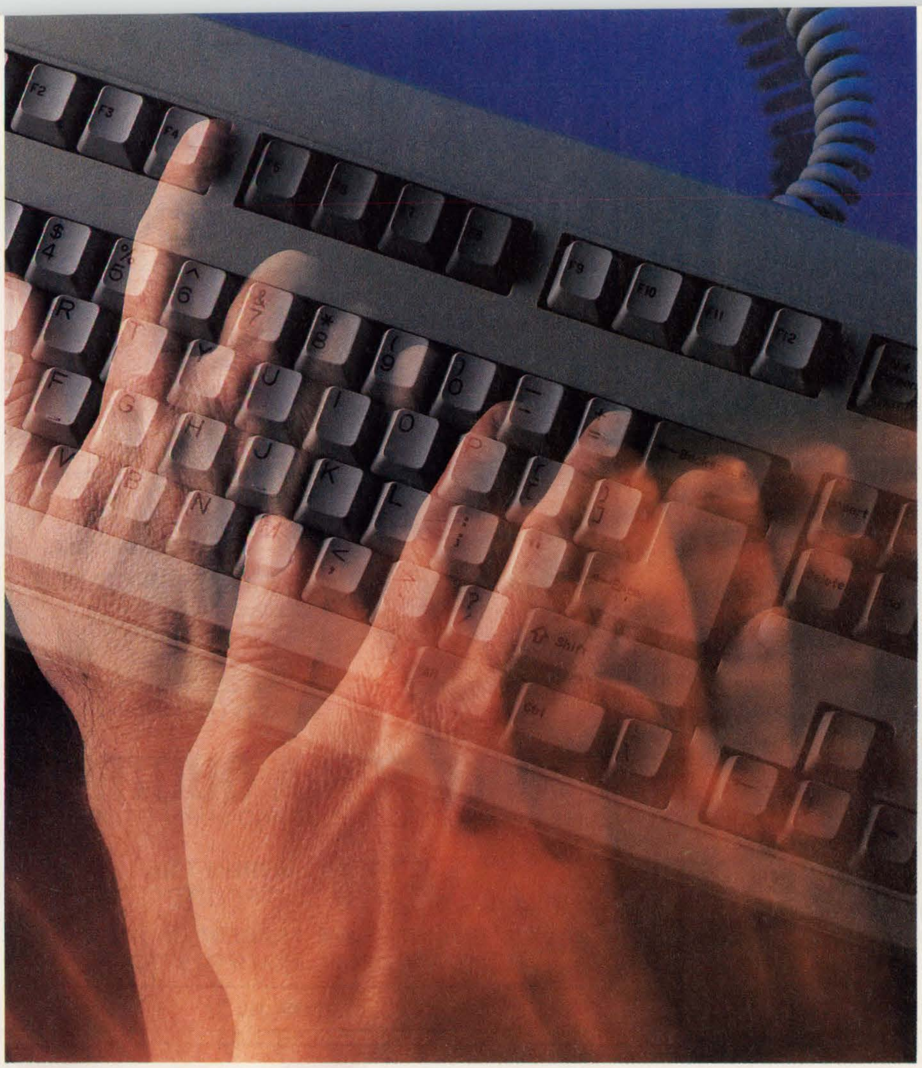

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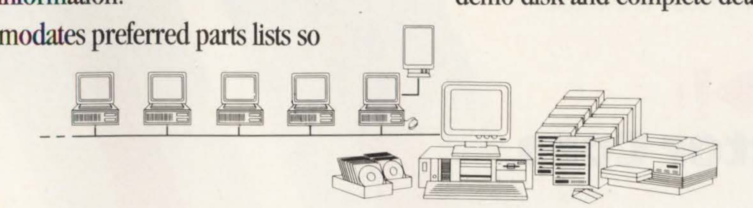

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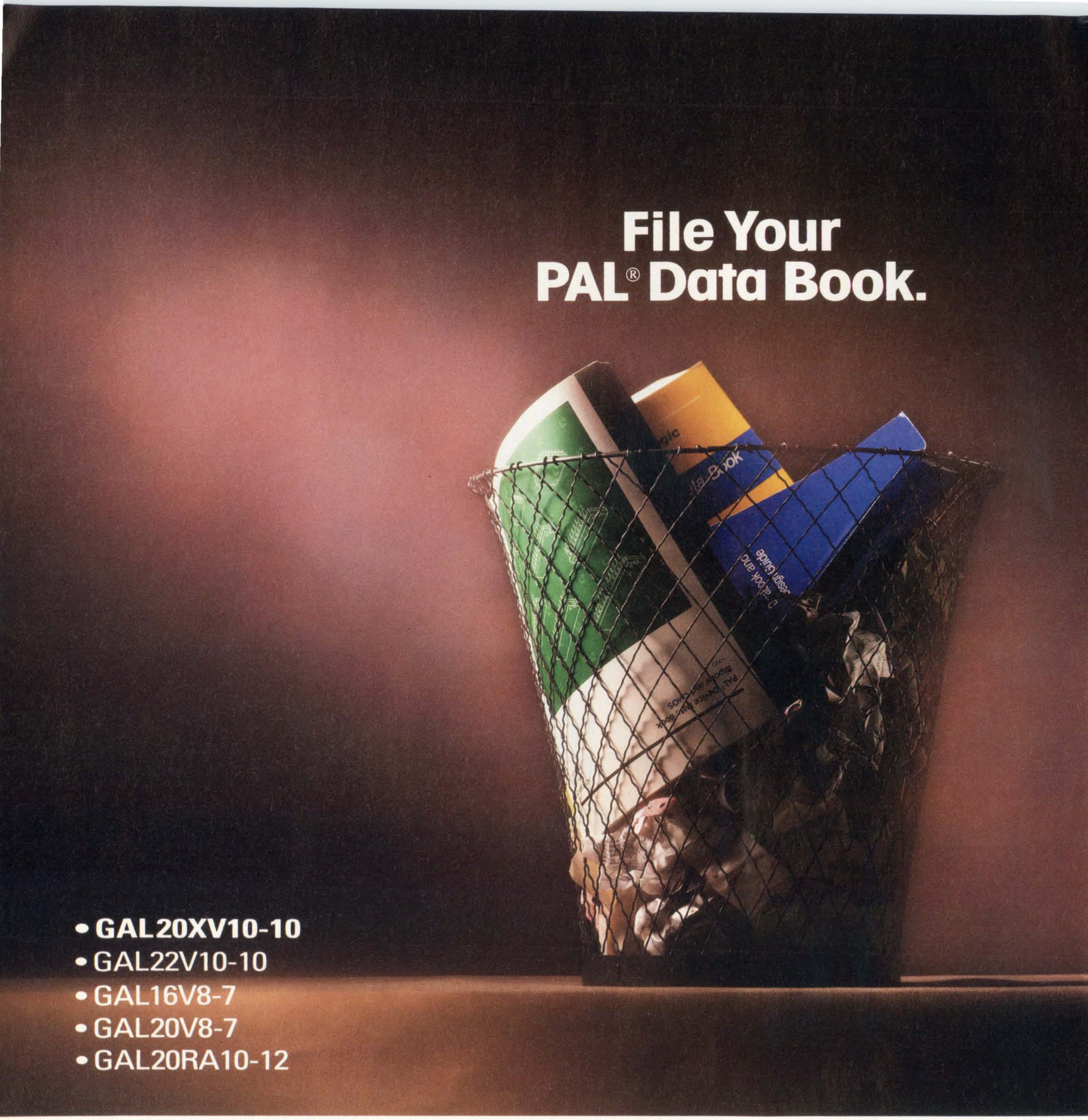

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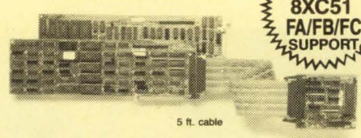

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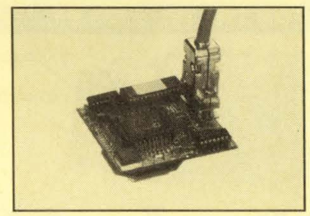

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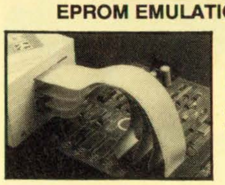

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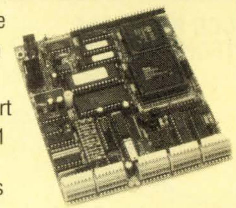

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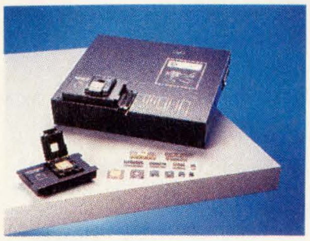

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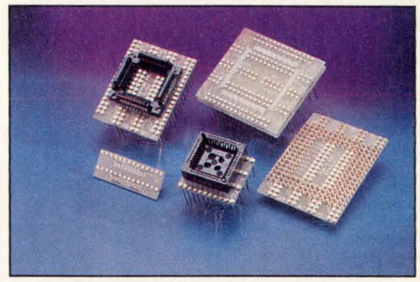

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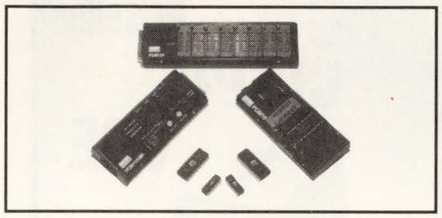

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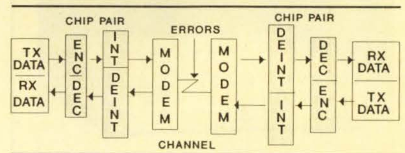

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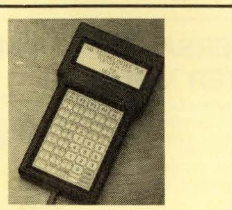

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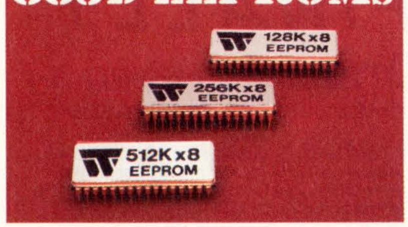

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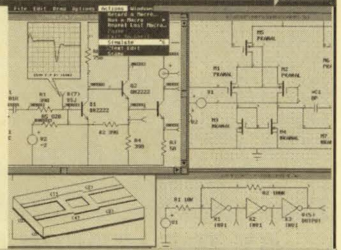

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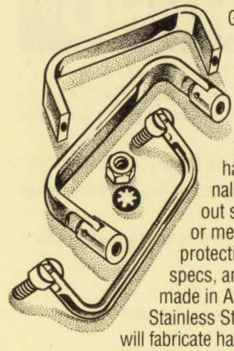

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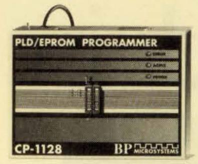

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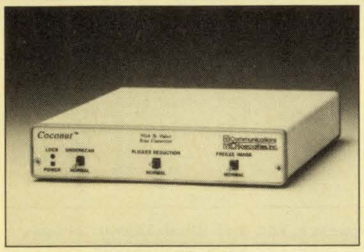

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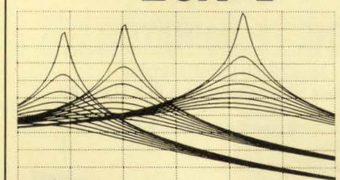

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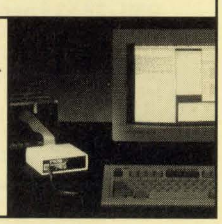

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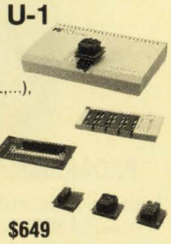

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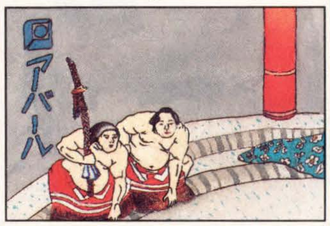

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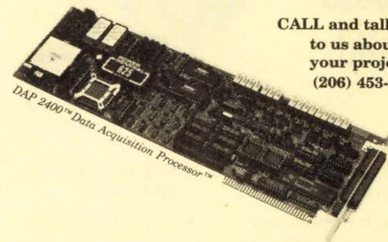

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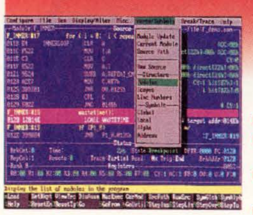

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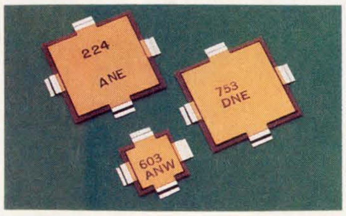

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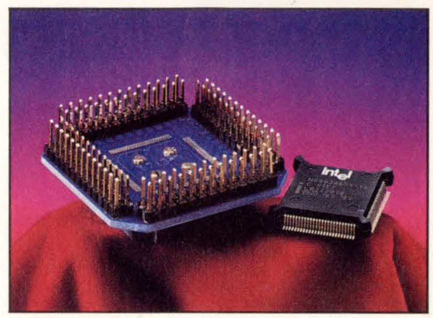

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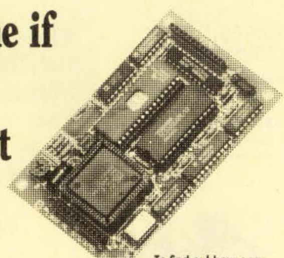

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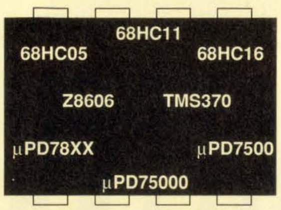

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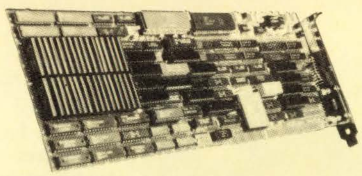

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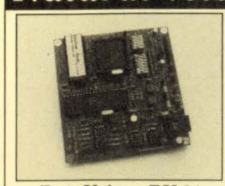

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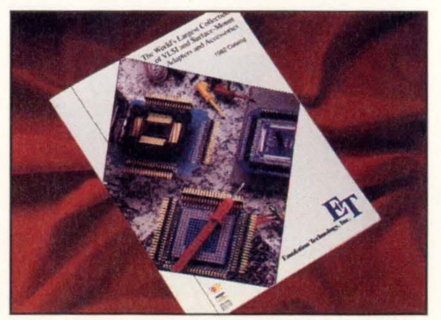

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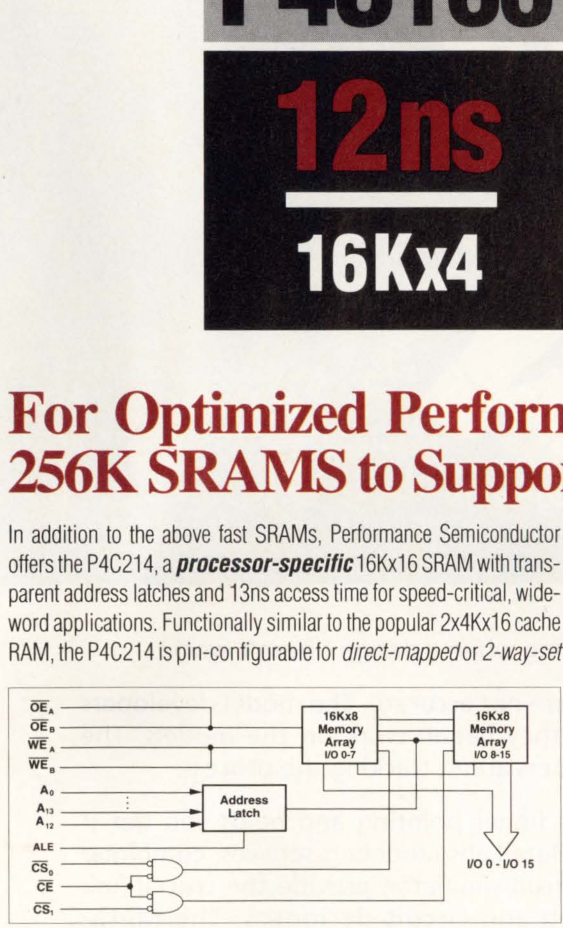
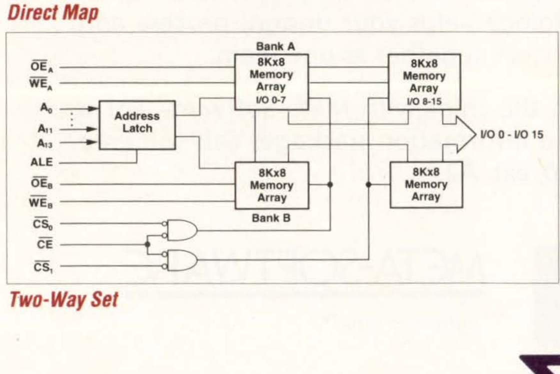


Direct Map



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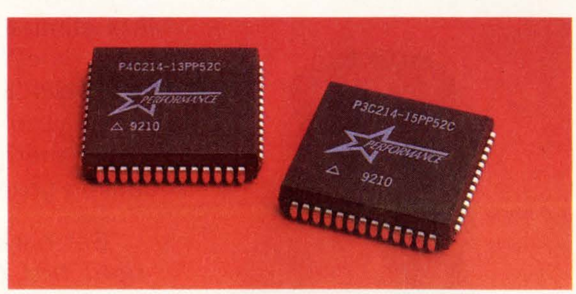

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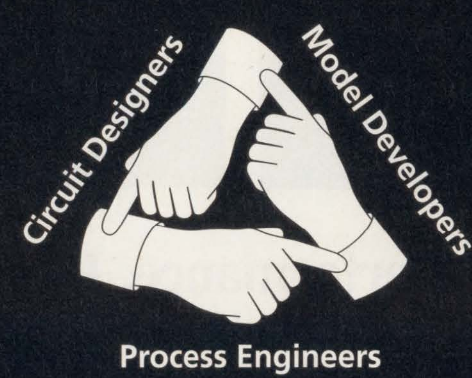

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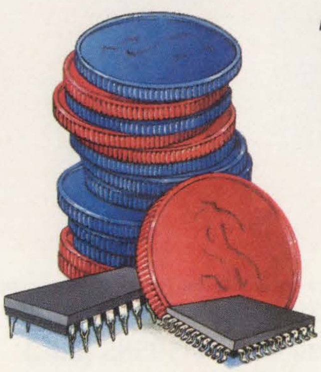

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Magazine Edition	July 6	June 11	INTERNATIONAL PRODUCT SHOWCASE—Vol. I • Hardware & Interconnect • Software • ICs & Semiconductors • Power Sources
Magazine Edition	July 20	June 25	INTERNATIONAL PRODUCT SHOWCASE—Vol. II • Computers & Peripherals • Components • CAE • Test & Measurement
News Edition	July 23	July 9	Engineering PCs & Workstations • CAE Software • SIGGRAPH Hot Products • Graphics Technology • Engineering Management Special Series • Regional Profile: Arizona, New Mexico
Magazine Edition	Aug. 6	July 16	Microprocessor Development Tools • ICs & Semiconductors • Technical Article Database Index • EDN's "Innovation Crusade"—Finalists Coverage • Reader Vote Contest: All advertisers in the issue qualify
News Edition	Aug. 13	July 30	DSP ICs • EDN's "Innovation Crusade"—Finalists Coverage • Telecom Software • Engineering Management Special Series
Magazine Edition	Aug. 20	July 30	MILITARY ELECTRONICS SPECIAL ISSUE • Military Computers Design • Test & Measurement • Memory Technology • Components
News Edition	Aug. 27	Aug. 13	Embedded Software • Software • Regional Profile: Washington DC, Maryland, Virginia
Magazine Edition	Sept. 3	Aug. 13	ASICs SPECIAL ISSUE • CAE Tools & Techniques • Computer Peripherals • Computer Buses • Sensors & Transducers • Buscon Show Coverage
News Edition	Sept. 10	Aug. 27	CAE • Test & Measurement • Diversity Special Series
Magazine Edition	Sept. 17	Aug. 27	Field-Programmable Gate Arrays • DSP Directory • Embedded Computers • CAE
SOFTWARE ISSUE	Sept. 17	Aug. 27	SOFTWARE ENGINEERING SPECIAL ISSUE (To be polybagged with the Sept. 17th Magazine Edition issue)
News Edition	Sept. 24	Sept. 10	Automotive Electronics • Sensors • Computers & Peripherals • Regional Profile: Oregon, Washington
Magazine Edition	Oct. 1	Sept. 10	TEST & MEASUREMENT SPECIAL ISSUE • European Technology Update • Data Acquisition Software • Superconductors • How to Design it Right the 1st Time Series—Part I • PLD/FPGA Directory
News Edition	Oct. 8	Sept. 24	CAE • PC/Workstation Design • Engineering Management Special Series
Magazine Edition	Oct. 15	Sept. 24	Disk Drives • Portable-Computer Design • Switching Power Supplies • Design it Right Series—Part II
News Edition	Oct. 22	Oct. 8	Data Storage Technology • Communications Technology • Regional Profile: Michigan, Illinois, Missouri
Magazine Edition	Oct. 29	Oct. 8	ELECTRONICA SHOW ISSUE • Object-oriented Programming • Chipsets for PCs • Design it Right Series—Part III • Wescon Preview Issue
News Edition	Nov. 5	Oct. 22	COMDEX/WESCON SPECIAL ISSUE • Special Supplement: Design for Portability • Microprocessors • Wescon/Comdex Hot Products • CAE Software • Diversity Special Series
Magazine Edition	Nov. 12	Oct. 22	COMDEX/WESCON SPECIAL ISSUE • Integrated Circuits • Test & Measurement • Design it Right Series—Part IV
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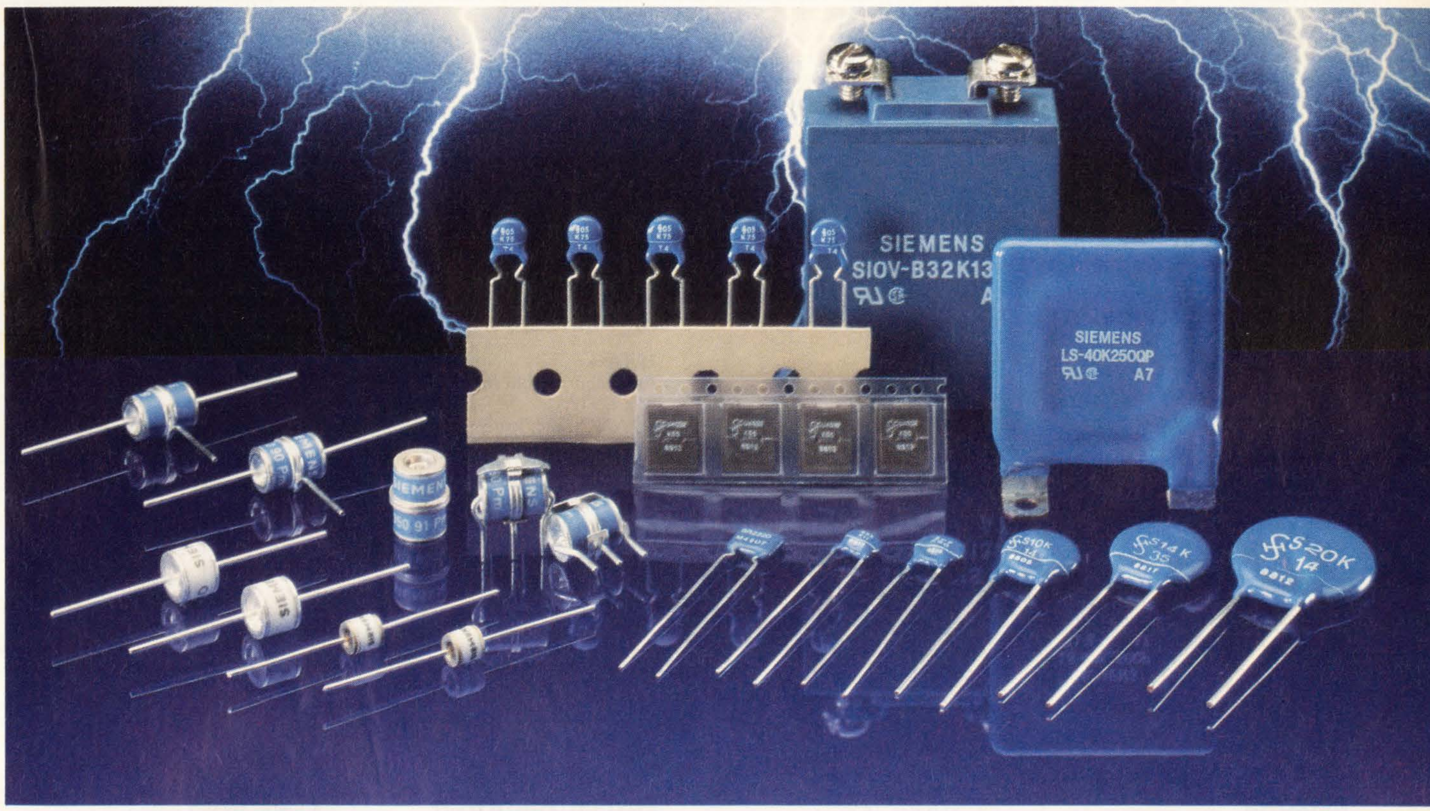

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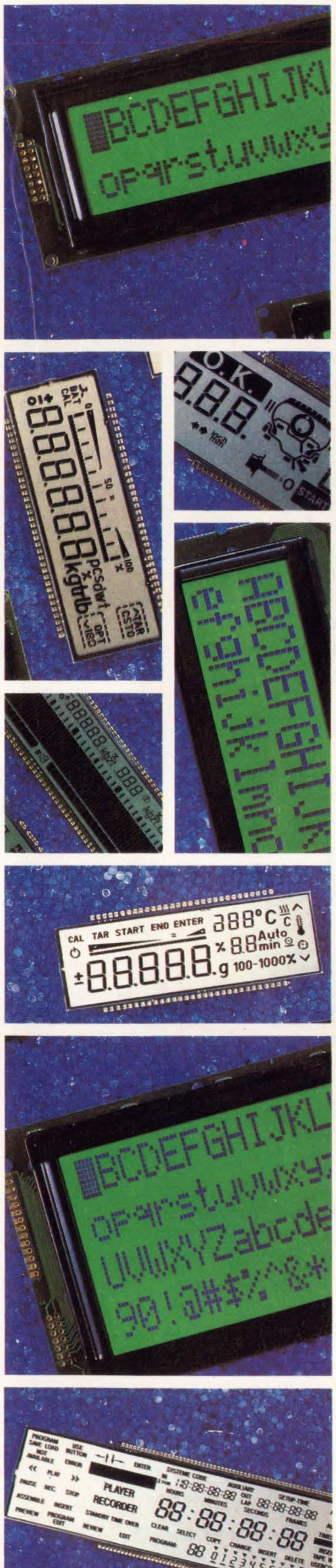

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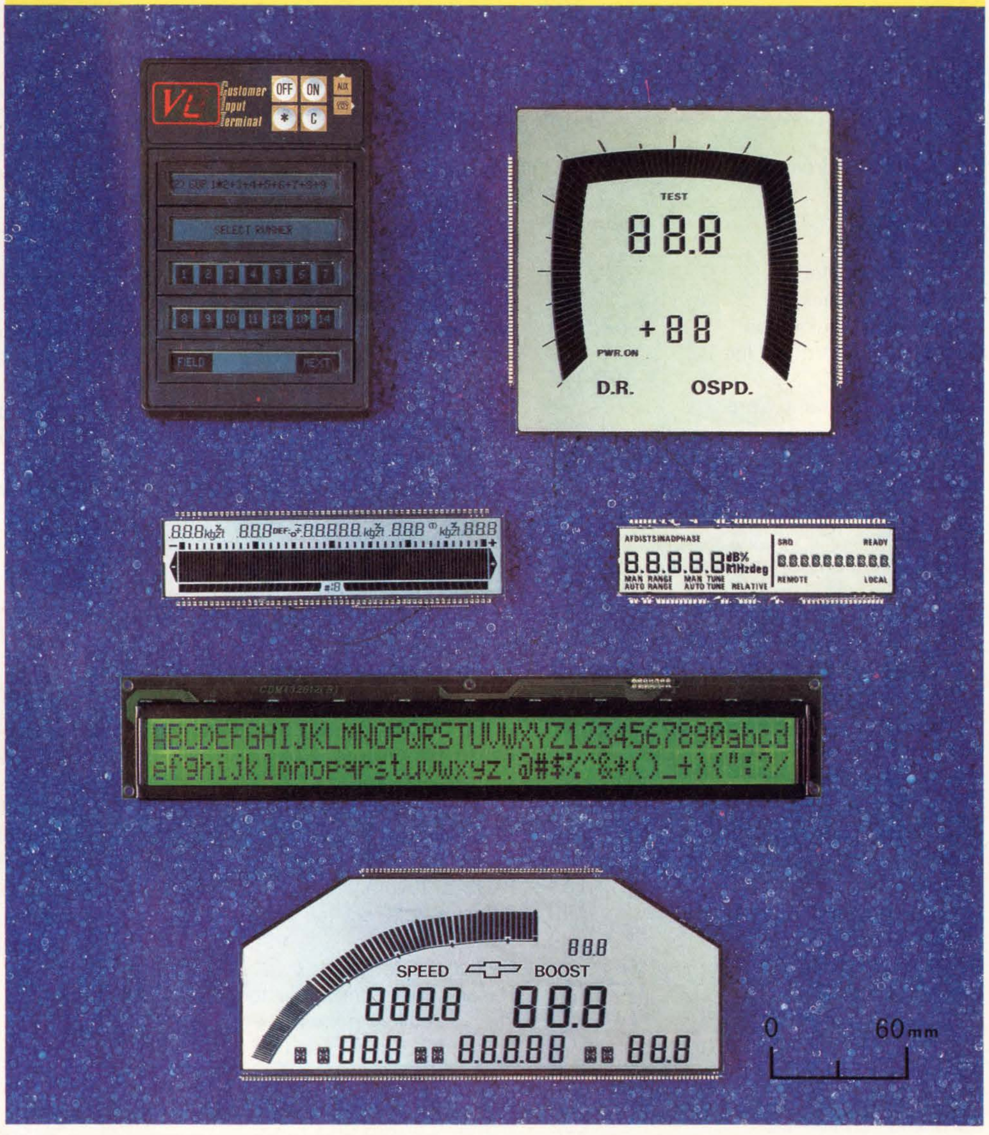

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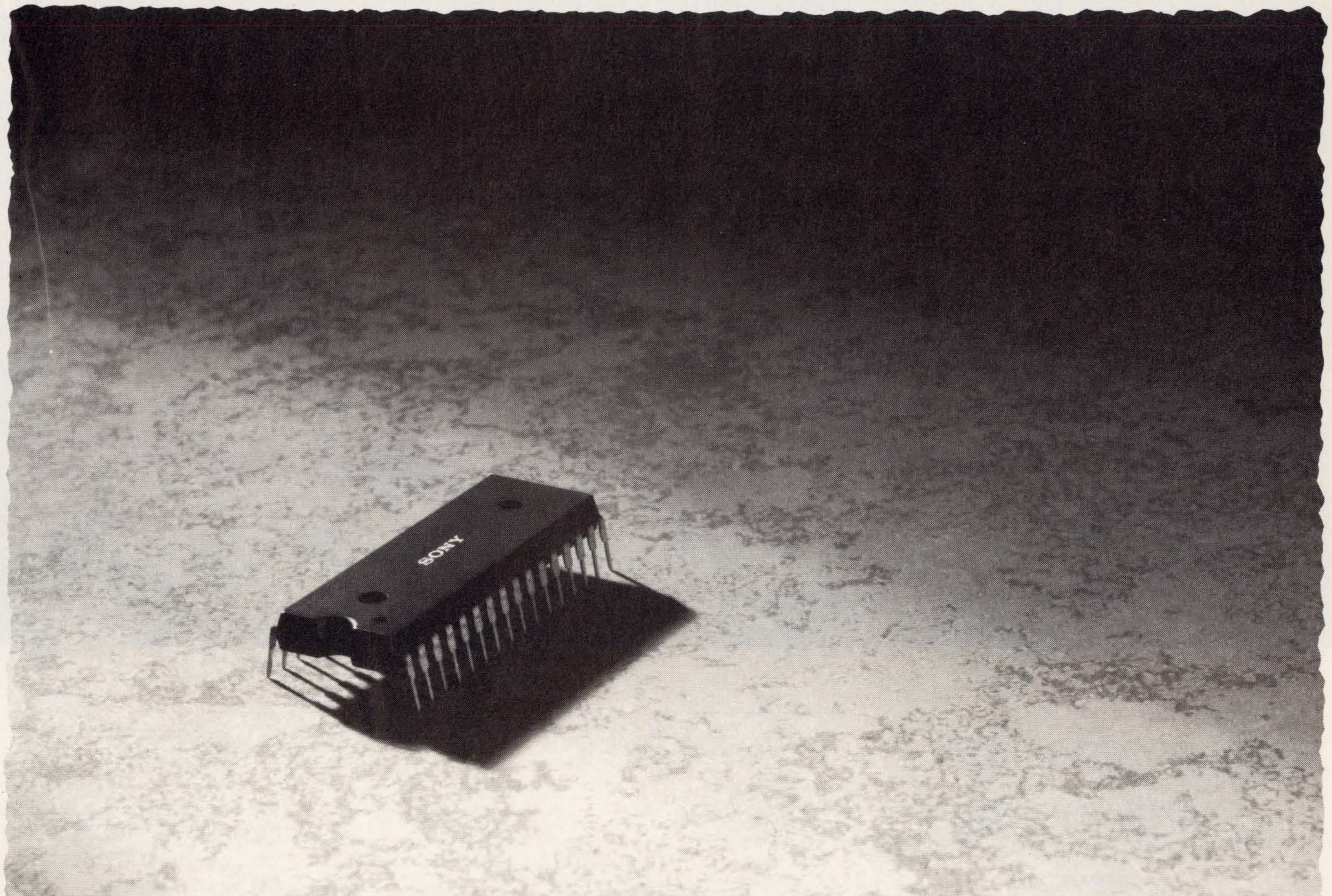

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				-40° - +85°C
CXK581100TM	100/120	TSOP	12/50	
CXK581100YM	100/120	TSOP (rev.)	12/50	
CXK581001P	70/85	DIP 600 mil	12/50	
CXK581001M	70/85	SOP 525 mil	12/50	
CXK581020SP	35/45/55	DIP 400 mil		
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0.068								A	
0.10						A_2		A	A
0.15						A_2		A	A
0.22						A_2		A	B_2
0.33						A_2		A	B_2
0.47						A_2	A	A B_2 B	B_2
0.68					A_2	A_2 A		A B_2 B	C
1.0				A_2	A_2 A		A	B_2 B	C
1.5			A_2	A_2 A	A	A	B_2 B	B_2 B C	
2.2		A_2	A_2 A	A	A	B_2 B	B_2	B_2 B C	D
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10		A B_2 B	A B_2	B_2 B C	B_2 C	C D_2	D_2 D	D	
15	A	A B_2	B_2 B C	B_2 C	C D_2	D_2 D	D		
22	A	B_2 B C	B_2 C	C D_2 D	D_2 D	D_2 D			
33	B_2	C	C D_2 D	D_2 D	D_2 D	D			
47		C D_2 D	D_2 D	D_2 D	D				
68		D_2 D	D_2 D	D					
100		D_2 D	D						
150		D							

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A_2 case	1.6 mm	.063 inch	3.2 mm	.126 inch	1.2 mm	.039 inch
A case	1.6	.063	3.2	.126	1.6	.063
B_2 case	2.8	.110	3.5	.138	1.9	.075
B case	2.6	.102	4.7	.185	2.1	.083
C case	3.2	.126	6.0	.236	2.5	.098
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EDN·ACRONYMS & ABBREVIATIONS

ACT—acoustic charge transport, a high-speed sampling technology that uses surface acoustic waves
ADC—analog-to-digital converter
ALU—arithmetic and logic unit, the computing part of a computer
ANSI—American National Standards Institute
ARP—Address Resolution Protocol
ASIC—application-specific integrated circuit
AUI—attachment unit interface
BiCMOS—bipolar complementary metal-oxide semiconductor
CCITT—International Telecommunications Union
CMIP—Common Management Information Protocol
CMOS—complementary metal-oxide semiconductor
codec—coder/decoder, a communications-oriented ADC and DAC combination IC
COS—Corporation for Open Systems International
CPU—central processing unit
CSMA/CD—collision-sense multiple-access collision detection
DAC—digital-to-analog converter
DECmcc—Digital Management Control Center
DECnet—Digital Equipment Corp's proprietary network
DRAM—dynamic random-access memory
DSP—digital signal processing
EGP—exterior gateway protocol
EIA—Electronic Industries Association
ESD—electrostatic discharge
FDDI—fiber distributed data interface
FIR—finite-impulse-response
GaAs—gallium arsenide, a material used for high-speed ICs
HDLC—high-level data-link control
HLL—high-speed, low-voltage, low-power logic
IEEE—Institute of Electrical and Electronics Engineers
IGP—interior gateway protocol
IGRP—Interior Gateway Routing Protocol, Cisco Systems' proprietary routing protocol
IIR—infinite-impulse-response
Integrated IS-IS—Integrated Intermediate System to Intermediate System
IPX—Internet Packet Exchange, Novell's proprietary routing protocol
ISA—Industry Standard Architecture, the standard 8- and 16-bit bus for PCs
ISO—International Standards Organization
ISSCC—International Solid-State Circuits Conference
JEDEC—Joint Electron Device Engineering Council
LAN—local-area network
LCD—liquid-crystal display
LED—light-emitting diode
LLC—Logical Link Control
LV-HCMOS—low-voltage, high-speed, complementary metal-oxide semiconductor logic
MAC—Medium Access Control
MOP—Maintenance Operation Protocol
NCL—Network Control Language
NIST—National Standards and Test Technology
OEM—original-equipment manufacturer
OSI—Open Systems Interconnection
OSPF—Open Shortest Path First
PC—personal computer
pc board—printed-circuit board
PLL—phase-locked loop
PPP—point-to-point protocol
RIP—Routing Information Protocol
RTMP—Routing Table Maintenance Protocol, Apple Talk's proprietary routing protocol
SDLC—synchronous data-link control
SMDS—Switched Multimegabit Data Service
SMT—Station Management, an FDDI supervisory function
SNA—Systems Network Architecture, IBM's proprietary network
SNMP—Simple Network Management Protocol
SRAM—static random-access memory
TCP/IP—transmission control protocol/internet protocol, an open suite of protocols for the Internet network
TIA—Telecommunications Industry Association
TTL—transistor-transistor logic
VGA—video graphics array
WAN—wide-area network
XNS—Xerox Network Systems
X.25—CCITT recommendation for communicating in packet mode on public data networks

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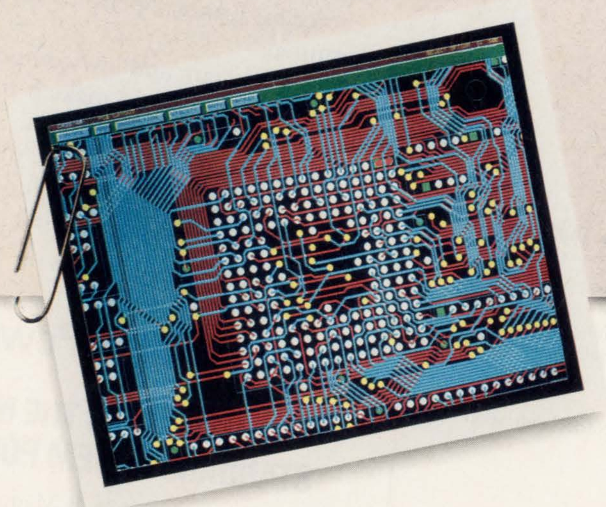

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Build multiple JTAG scan paths onto your next pc board

As multilayer pc boards become denser, JTAG boundary-scan testing is becoming a necessity to keep development cost down. The current IEEE 1149.1 JTAG (Joint Test Action Group) standard defines a 4-wire test bus. The test bus drives a chain of test-access port (TAP) controllers that internally reside on each chip on the pc board. The 4-wire JTAG bus consists of the Test Mode Select (TMS), Test Clock (TCLK), Test Data In (TDI), and Test Data Out (TDO) lines.

On dense pc boards, factors such as high fan-out, clock skew, and the tester's capabilities place a limit on the length of a single scan chain. Multiple small scan chains let you partition and isolate test paths. The smaller chains not only alleviate the problems associated with one large single chain, but they make the test code more compact and easier to write. A simple design using two ICs from Logical Solutions Technology Inc (Campbell, CA), a few glue-logic chips, and an ISA-bus JTAG-tester board from Alpine Image Systems Inc (Los Altos, CA), lets a single 4-wire JTAG bus accommodate as many as 16 scan chains on a single pc board.

You must add the two Logical Solutions chips and glue-logic chips to the board under test (**Fig 1**). The 74TC32 control chip contains a 32-bit serial-in parallel-out (SIPO) shift register and a 1-of-32 decoder. You can enable one of the chip's 32 output lines by serially clocking an appropriate bit into the serial-data input (SDI) port. By programming the chip's five address input lines, which control the decoder section, you can direct JTAG TDI data to one of the board's 16 TDI lines. When you activate the chip's real-time enable (RTEN) line, the chip sends data on its real-time data (RTD) port to the addressed output port.

The other Logical Solutions IC, the 74TV16 visibility chip, contains a 16-to-1 multiplexer. Each of the board's 16 TDO lines connect to one of the multiplexer's input pins. By programming the chip's four address inputs, you can direct data on any one of the board's 16 TDO lines to the TDO line for the JTAG 4-wire bus.

The glue chips consist of a 74xx164 SIPO register, an ALS521 8-bit comparator, and a sprinkle of 2-input OR and NOR gates. You

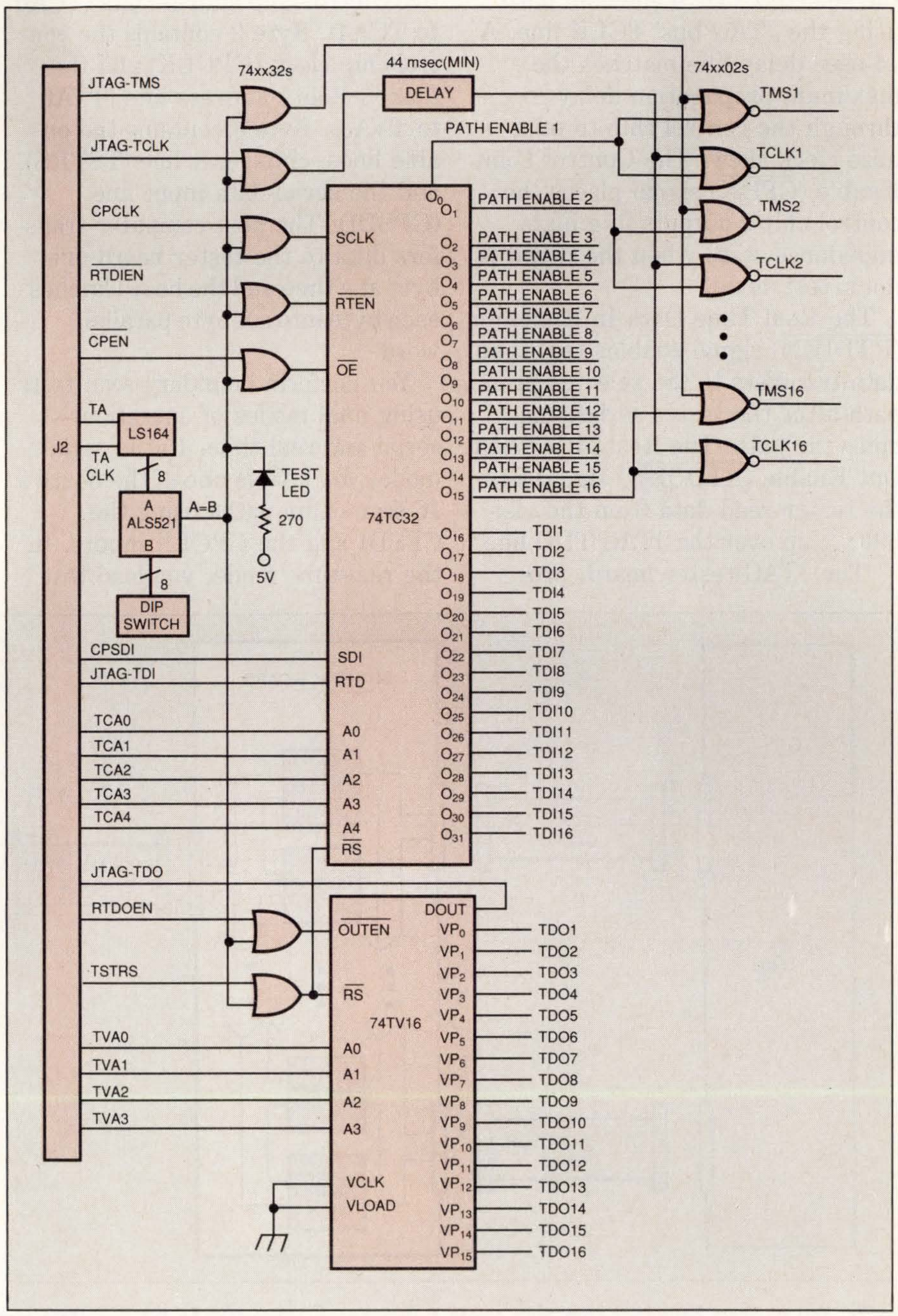

Fig 1—By adding a handful of ICs to your next pc-board design you can partition a single unwieldy JTAG scan path into 16 manageable boundary-scan paths.

can assign a board-test address using an 8-bit DIP switch. During test the JTAG-tester board serially transmits a test address (TA) to the SIPO register using the test address clock (TACLK). The comparator matches the register data with the DIP switch data. A match enables the JTAG control signals via the OR gates and turns on a test LED.

The circuits clock serial data onto the selected TDI scan-chain path using the JTAG bus' TCLK line. A 44-nsec delay line matches the maximum propagation delay through the control chip to minimize clock skew. The Control Point Enable (CPEN) signal places the control chip's outputs in a high-impedance state when the board is not in test mode.

The Real Time Data In Enable (RTDIEN) signal enables real-time data transfers to the selected scan path after the tester serially enables the path. The Real Time Data Out Enable (RTDOEN) signal lets the tester read data from the visibility chip over the JTAG TDO line.

The JTAG-tester board, proTEST-PC, has two output ports—a 4-wire IEEE 1149.1 bus and a 24-bit user-defined parallel port. You connect the board under test to both of the JTAG tester boards' output ports using an interface card containing a handful of 74XX541 octal 3-state buffers (**Fig 2**).

The 24-bit parallel port lets you divide the bits into three user-defined bytes. Byte 1 loads the board's test address (TA) and the five control-chip address bits (TCA0 to TCA4). Byte 2 contains the control-chip clock (CPCLK) and the four visibility address bits (TVA0 to TVA3). Byte 3 contains the enable lines, chip-reset line (TSTRS), and the serial-data input line (CPSDI). The host computer transfers data to the tester board one byte at a time and the board latches each byte into a 3-byte parallel word.

You perform boundary-scan tests using dual modes of operation—serial and real time. In the serial mode, you enable one of the board's 16 scan-chain paths using the CPSDI and the CPCLK inputs. In the real-time mode, you load test vectors into the respective TAP controllers via the JTAG TDI line by activating the RTDIEN line. Finally, you read and write JTAG test data in the real-time mode by activating the RTDOEN line. Actual code is available via EDN's BBS.

—Mark Casparian

The author is a staff engineer at IBM Corp, Route 52, Hopewell Junction, NY 12533. Phone (914) 894-4813.

The software listings in this article are available on EDN's computer bulletin-board system (BBS). Phone (617) 558-4241 with modem settings 300/1200/2400/9600 8,N,1. Access */freeware* SIG and specify *(r)ead* option followed by *(k)eyword* search for "JTAG.ZIP".

Observing the extreme social effects of high technology

Sometimes, the effects of all the high-tech products we're developing can truly numb your mind. *Mondo 2000* is a quarterly magazine that displays some of these socio-

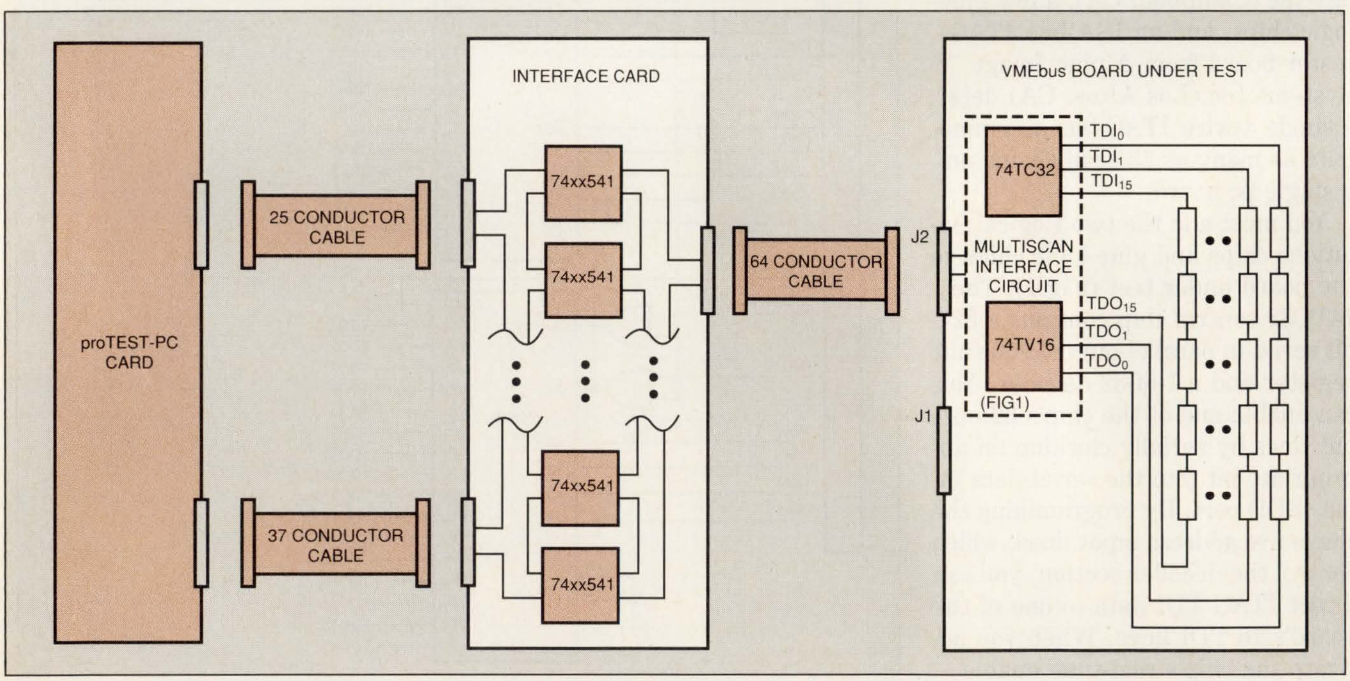

Fig 2—You perform boundary-scan tests using a DOS-based computer. An ISA bus JTAG tester board, the proTEST-PC from Alpine Image Systems has a 4-wire JTAG bus and a 24-bit parallel output port. The tester's output ports connect to the board under test via an interface card populated with 74xx541 Octal 3-State buffers.

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logical effects in a very attention-getting manner.

This magazine chronicles the exploits and product preferences of a social group that has adopted the trappings of a cyberpunk lifestyle. Cyberpunk is a subgenre of science fiction that wraps the multiple themes of avant-garde art, rock 'n' roll music, sex, industrial mercenaries, and the casual use of designer drugs around a setting permeated with networked computers, virtual reality, and multinational high-tech companies larger than countries. The magazine treats William Gibson and Bruce Sterling, two of the leading cyberpunk authors, like prophets.

I first heard about *Mondo 2000* on National Public Radio and subsequently spent about a month finding a copy. The issue I bought, number five, contains an eclectic article mix, including reviews of music albums, books, and graphics workstations. It includes round-up articles about desktop video-production equipment, cyberpunk fashions, model rocketry, and smart drugs (food supplements, additives, and prescription drugs that supposedly improve brain functions). The publication also features interviews with writers, technologists, and musicians (including an interview with astrophysicist-turned-musician Dr Fiorella Terenzi), and some truly weird opinion columns.

True to its cover banner—"Guaranteed Read Proof!"—this magazine can be hard to digest. It's chock full of unexplained slang and abbreviations that will make the cognoscenti feel right at home and leave neophytes somewhat out of kilter. For example, an article on smart drugs written by "St Jude" tosses product names such as Piracetam, Vincamine, Gingko Bilobas, and Hydergine around as though they were common household products and mixes in cyberpunk-derived slang for an extra kick. If you've been reading cyberpunk novels for the last ten years as I have, you'll feel right at home. Otherwise, try to hold on for the ride.

Even the ads and the masthead in this magazine fascinate me. Advertisers include familiar computer hardware and software companies such as Autodesk, Quarterdeck Office Systems and Logitech (although you'll never find *this* Logitech ad in a PC magazine); mainstream record companies such as Elektra Entertainment and Rhino; book publishers including the MIT Press; and (of course) mail-order purveyors of smart drugs. The masthead lists Editor-In-Chief R U Sirius, domineditrix Queen Mu, a ministress of information, and a factotum (a fancy name for a go-fer). All together, this magazine gave me a look at a very strange new world.

—**Steven H Leibson**

Mondo 2000, $24 for five issues, Box 10171, Berkeley, CA 94709. Phone (510) 845-9018. FAX (510) 649-9630.

Windows 3.0 course explains it all

I'm not wild about Microsoft's Windows 3.0. Had I wanted to see a computer screen littered with goofy little icons, I would have bought a Macintosh. But this Windows thing isn't going to go away anytime soon, so I decided to get serious about learning the software. Because I'd taken several Heathkit courses, I sent away for the company's Window's 3.0 course.

The course is divided into two sections. The first comprises eight chapters that describe how to use Windows' supposedly intuitive user interface, as well as the Program Manager and the File Manager. The last five chapters describe how to use the collection of programs supplied with Windows.

At the beginning of each chapter is a 2-page summary called Fast Track. To get a fast start on Windows, you could zip through the course book by reading only the Fast Track sections. Next to each topic in these sections is the page number where that subject is covered in the chapter, so you can quickly turn to the right page to get more information.

Each chapter has step-by-step instructions that explain how to perform specific procedures, why you'd need or want to do a procedure, and shortcuts you can use once you know what you're doing. An exam completes each chapter.

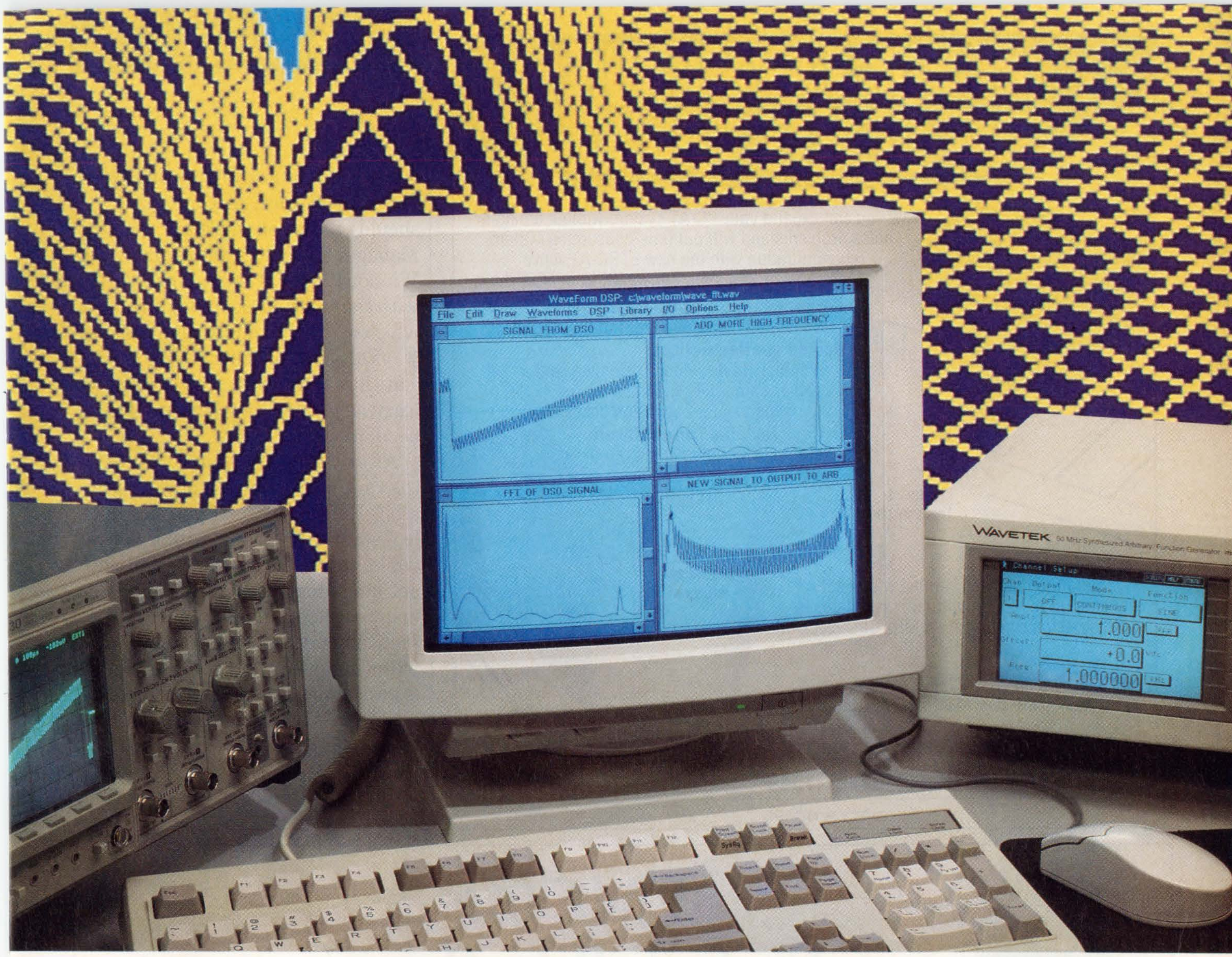
The course book has five handy appendices. Appendix A tells how to install Windows. Appendix B has troubleshooting information. Appendix C has information you might need to know if you're running Windows on a network. Appendix D has the answers to the end-of-chapter exams, and Appendix E is a list of shortcut keys for Windows and its accessories.

Two chapters that are especially useful cover installing a printer and using the Print Manager, the program that oversees and controls printing tasks in Windows applications. The material is much easier to understand than the corresponding sections of the Windows manual. The chapter about Windows' Clipboard utility also presents potentially confusing information in a clear and straightforward manner.

Once you've completed the 13 chapters, you can take the final examination and mail it to the company. Within three weeks, you'll receive a certificate indicating that you've earned 3.0 Continuing Education Units if you get a 70 or better on the exam.

I was surprised to find that I could have taken the course's final examination before doing any of the actual course work had I known how to print a screen to a file. This situation was due more to the unchallenging final exam than any deficiency of the course material.

This course would be worth taking for someone who wants to learn Windows, but isn't comfortable



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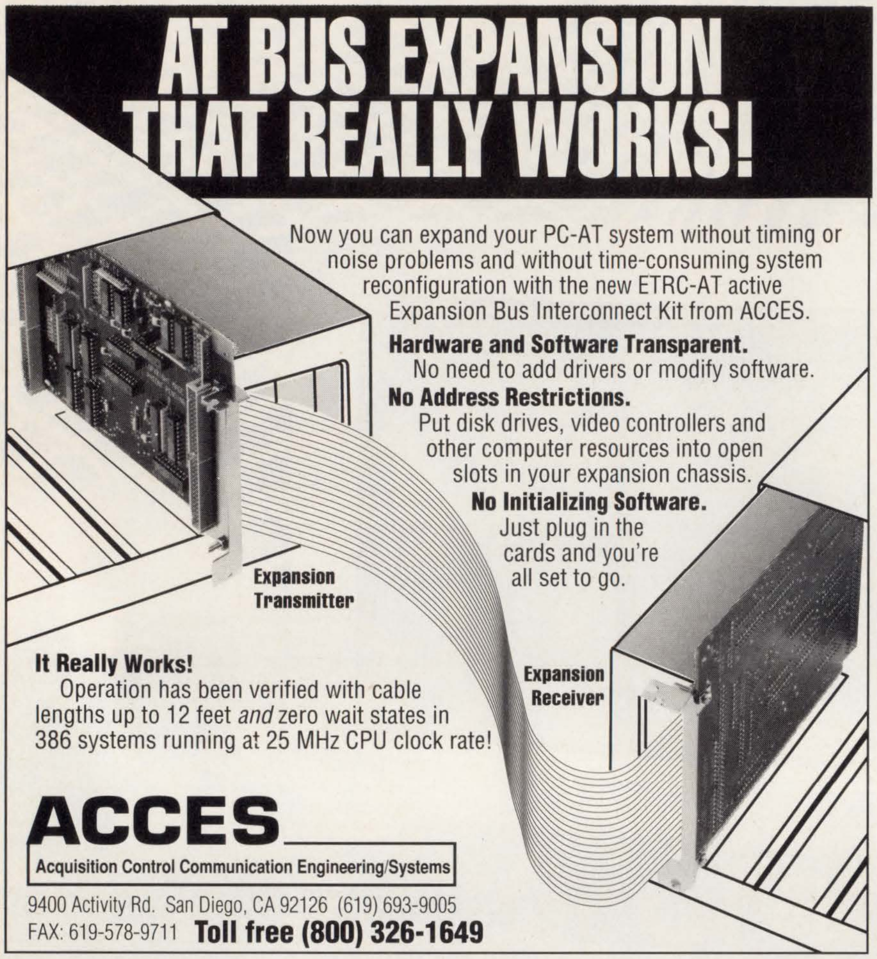
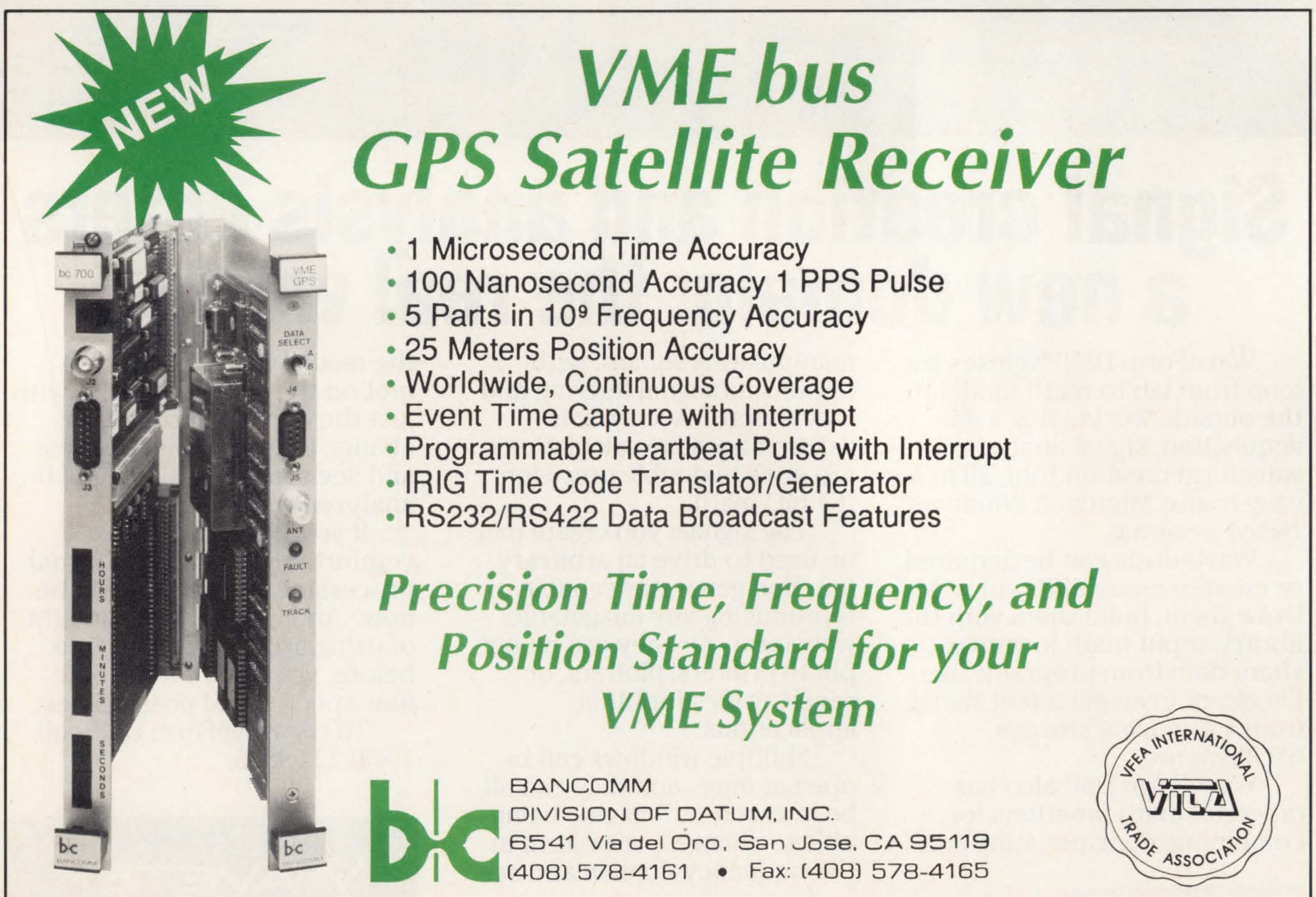
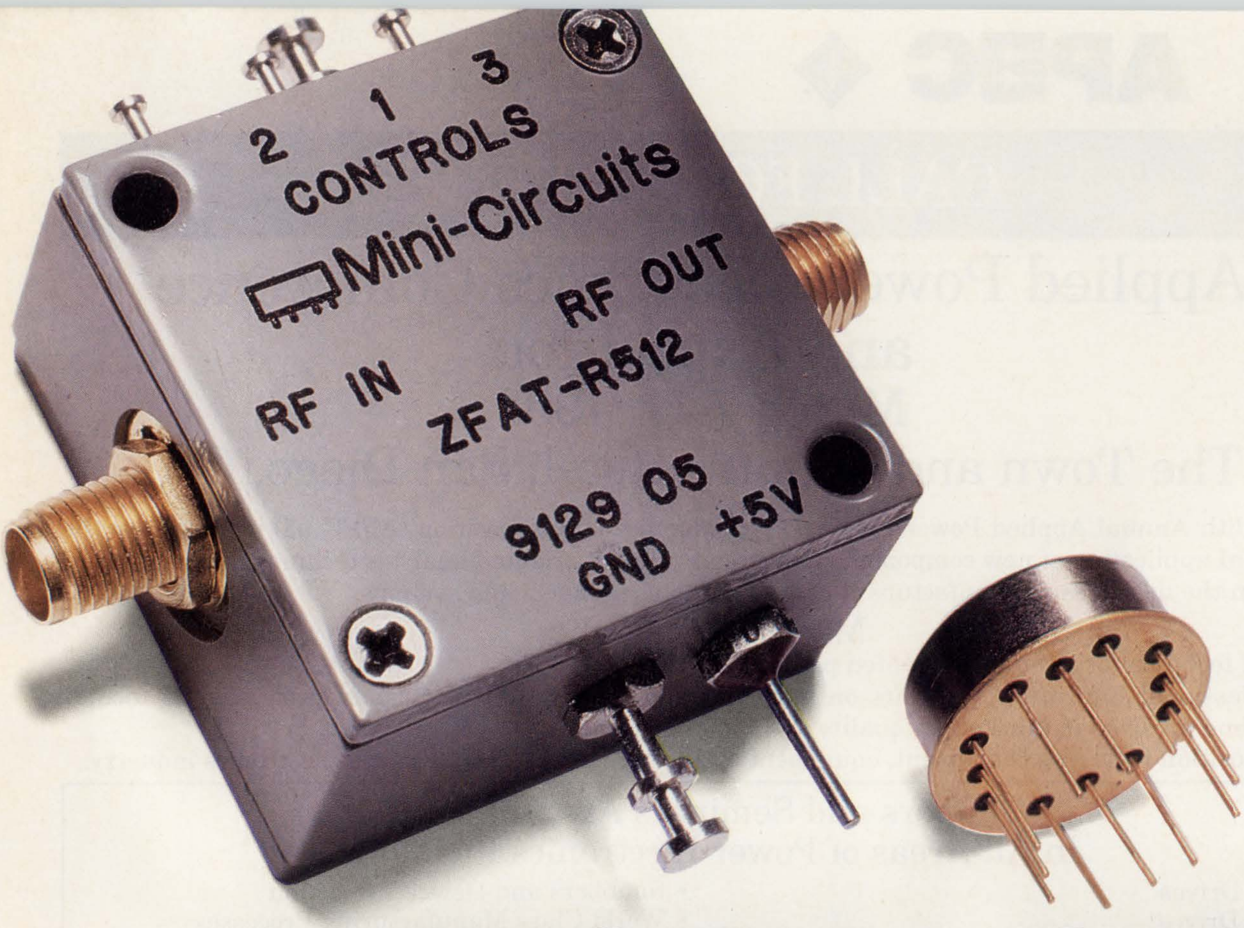


wending his or her way through unfamiliar software. Anyone else should read up on the Program Manager and File Manager in a Windows manual and then play with the software to figure out which of the seemingly countless ways of accomplishing any function suits him or her best. You can easily learn anything else when and if the need arises.

After taking the course, I'm more tolerant of Windows, and I'm still a big Heathkit fan. If you haven't looked at a Heathkit catalog for a while, give the company a call and get one. Heathkit doesn't offer many electronics kits anymore, but the company has lots of new computer and electronics courses and is getting into the home-automation business.—**Julie Anne Schofield**

Windows 3.0, Heathkit Educational Systems, Benton Harbor, MI 49023. Phone (800) 253-0570. $99.95.





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