

# EDN<sup>®</sup>

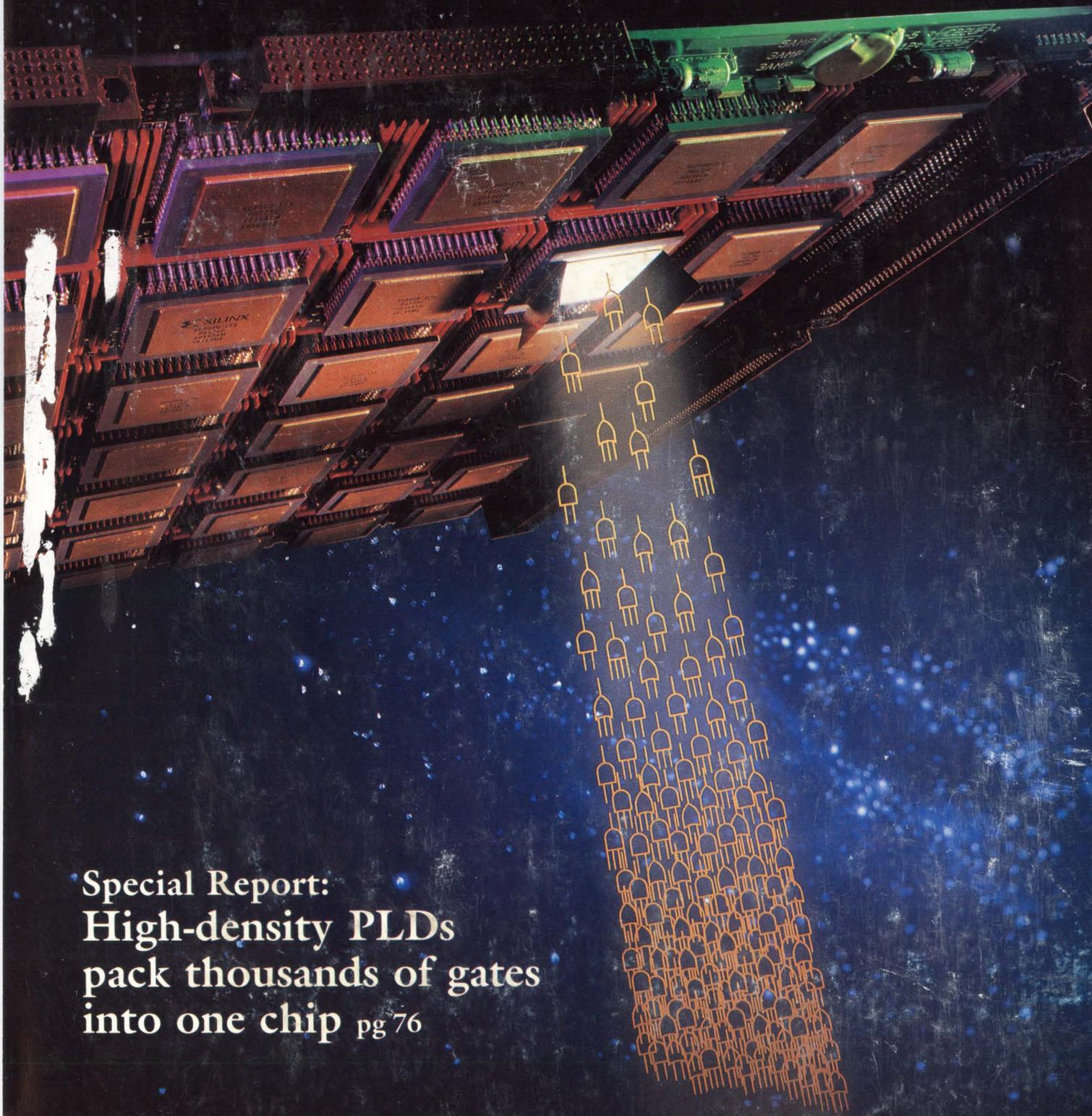
Multichip modules call for design standards pg 35

Monolithic op amps offer high speed at low cost pg 53

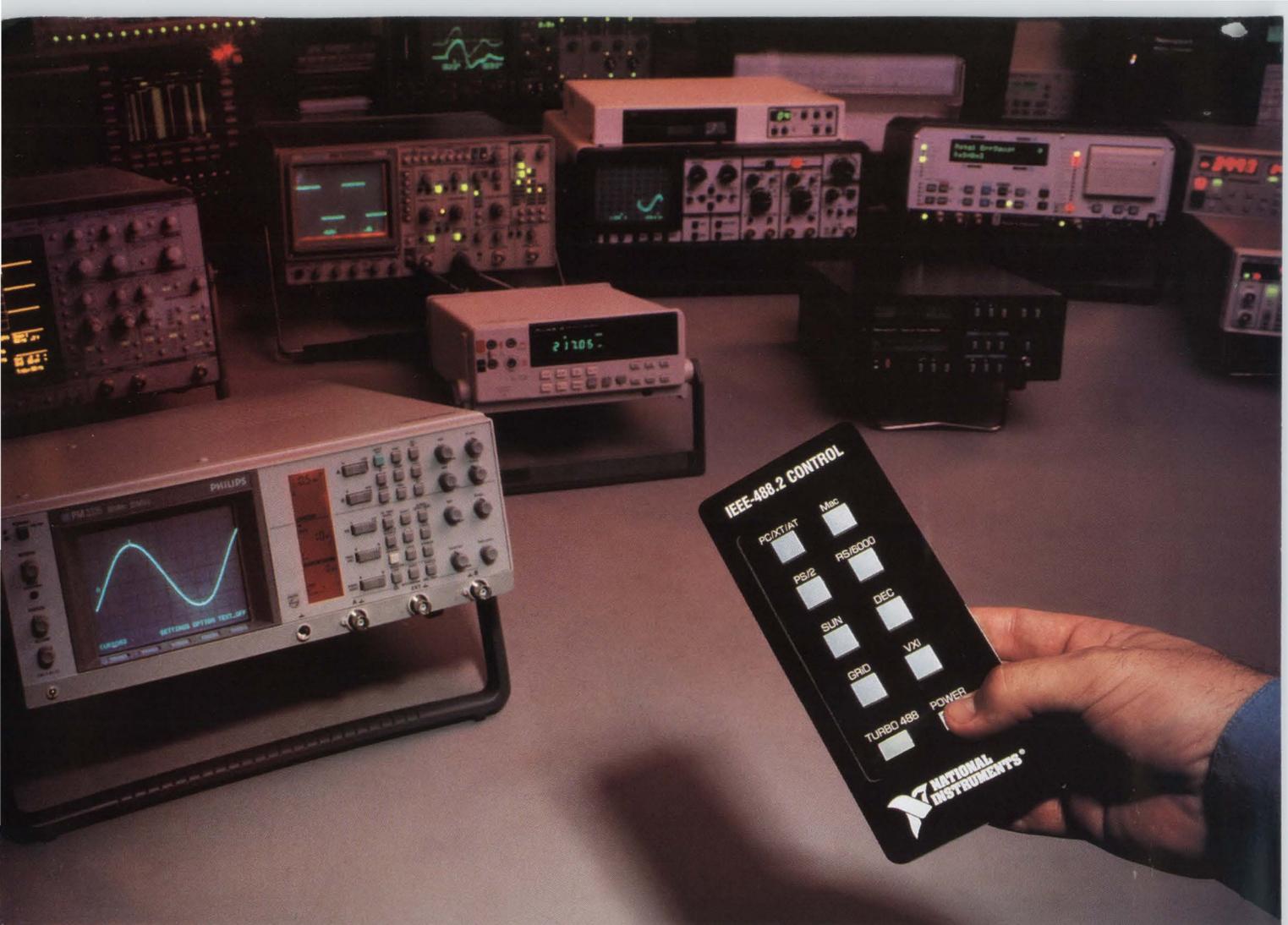
C++ combines elements of C and OOP languages pg 97

Design Ideas pg 105

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS



Special Report:  
High-density PLDs  
pack thousands of gates  
into one chip pg 76



# ULTIMATE CONTROL

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The NAT4882™ chip makes our GPIB controller boards completely IEEE-488.2 compatible. When the NAT4882 is teamed with the Turbo488® performance chip, you get the maximum IEEE-488 transfer rate of 1 Mbytes/sec for both read and write operations.

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CIRCLE NO. 79

See Us at ATE and Instrumentation, booth 108



# PROFILES IN PARTNERING

## AT&T and Dale®

**PRODUCTS:** Resistors and Inductors.

**OBJECTIVE:** Quality improvement and lowered cost of acquisition.

**UNITS INVOLVED:** AT&T, Columbus (NE), Norfolk (NE), Bradford (PA), and Yankton (SD).

"Quality Leader," "Demand-Pull" and "Cooperative Vendor" are just a few of the program titles which have helped AT&T and Dale® forge an efficient manufacturer-vendor partnership. These steadily-evolving programs are closely linked to the AT&T/Dale relationship which has, since its beginning more than 20 years ago, been directed toward continual quality improvement and lowered cost of acquisition.

Notable in this history is establishment of the first on-line Electronic Data Interchange between AT&T and a passives vendor and early participation in AT&T programs which have helped

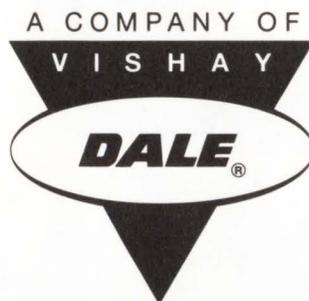
form current industry patterns for Just-In-Time delivery and Ship-To-Stock quality.

Today, Dale is ranked as one of AT&T's top 20 passives vendors. Four Dale locations supply various AT&T Works with metal film resistors, wirewound resistors and magnetic components. Depending on the parts involved, supply is often done on a "demand-pull" basis with AT&T providing a rolling-forecast to enable each location to anticipate shipping requirements. Lag time is further minimized by master purchase orders and by the fact that three Dale locations have been certified under AT&T's Quality

Leader Program. This eliminates need for source inspection by AT&T on specified parts and lot numbers.

At the same time, Dale is an active participant in AT&T's Cooperative Vendor Program. Quarterly meetings enable quality, management, engineering and procurement personnel from both organizations to discuss upcoming requirements and review performance ratings from all areas involved. According to a Dale spokesperson, "This program is extremely valuable in our inter-department and inter-plant coordination. In particular, it enables us to quickly address problem areas and to focus on upgrading our levels of certification."

For more information on how Dale's commitment to effective partnering can benefit your operation, please contact Joe Matejka, Vice President, Quality Assurance, Dale Electronics, Inc., 1122 23rd Street, Columbus, Nebraska 68601-3647. Phone 402-563-6511. Fax 402-563-6418.



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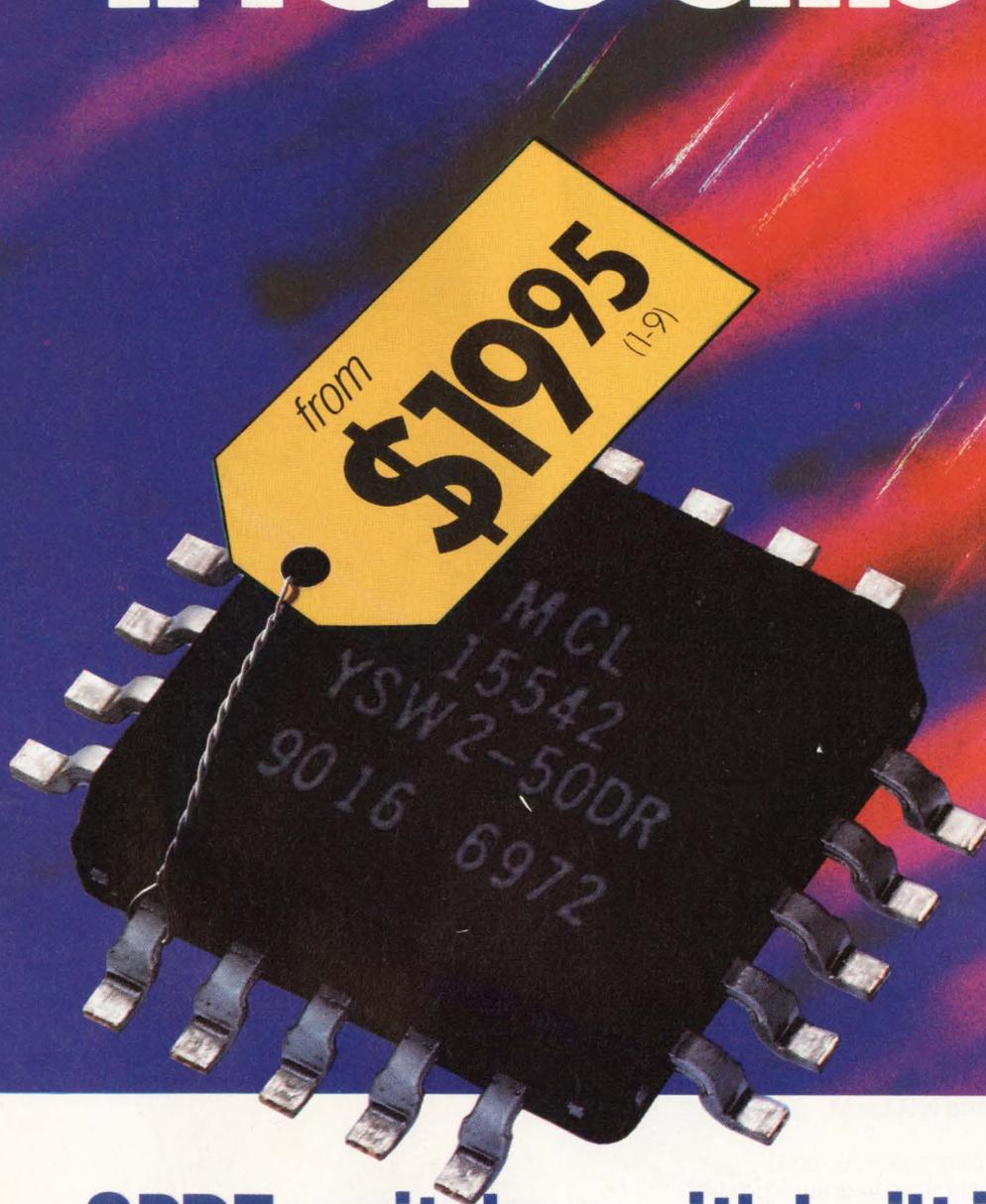


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#### SPECIFICATIONS (typ)

	Absorptive SPDT YSWA-2-50DR ZYSWA-2-50DR			Reflective SPDT YSW-2-50DR ZYSW-2-50DR		
	dc-	500-	2000-	dc-	500-	2000-
Frequency (MHz)	500	2000	5000	500	2000	5000
Ins. Loss (dB)	1.1	1.4	1.9	0.9	1.3	1.4
Isolation (dB)	42	31	20	50	40	28
1dB Comp. (dBm)	18	20	22.5	20	20	24
RF Input (max dBm)	20			22	22	26
VSWR "on"	1.25	1.35	1.5	1.4	1.4	1.4
Video Bkthru (mV,p/p)	30	30	30	30	30	30
Sw. Spd. (nsec)	3	3	3	3	3	3
Price, \$ (1-9 qty)	YSWA-2-50DR (pin) 23.95 ZYSWA-2-50DR (SMA) 69.95			YSW-2-50DR (pin) 19.95 ZYSW-2-50DR (SMA) 59.95		

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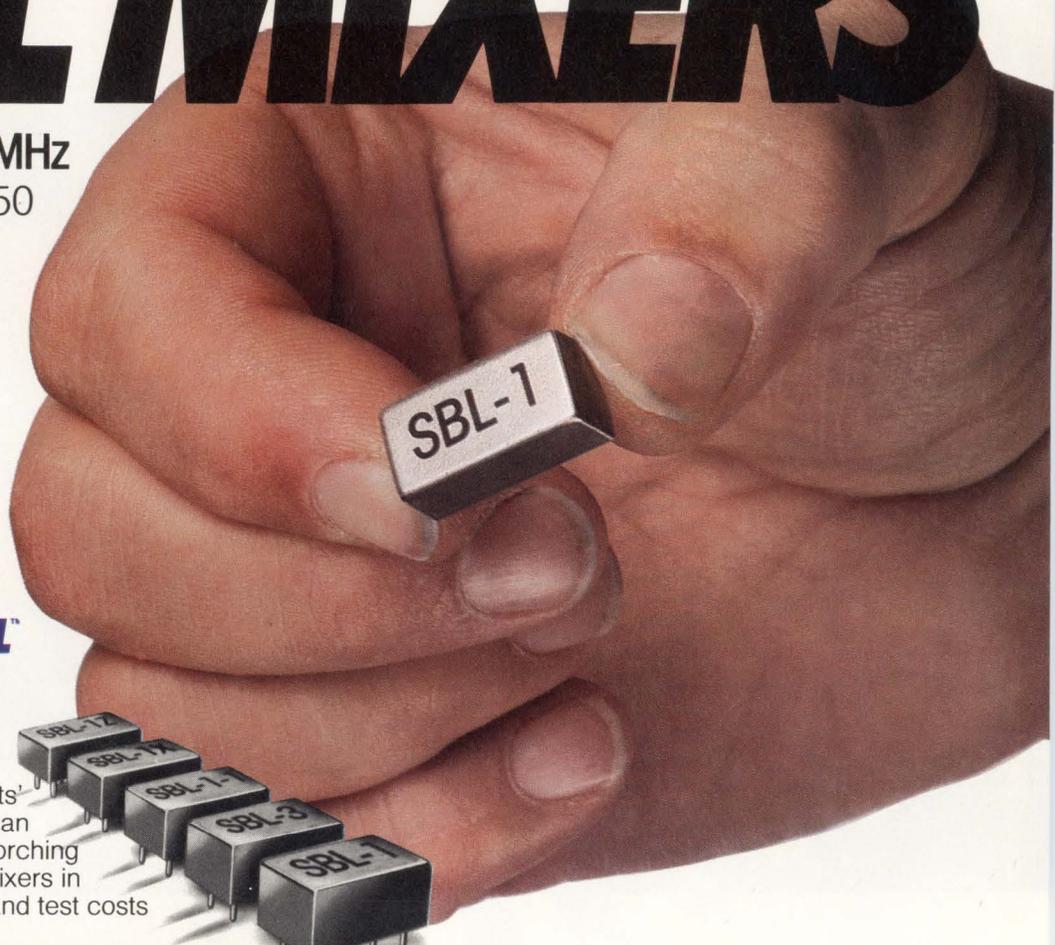
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CIRCLE NO. 3

F141 REV. C

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25KHz to 2000MHz  
from \$4.50



**ULTRA-REL™  
MIXERS**  
5-YR. GUARANTEE\*

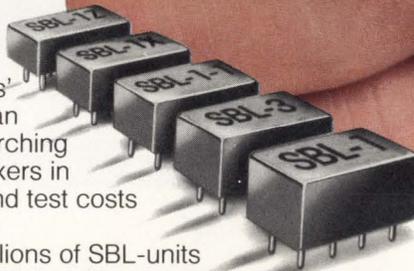
Our tough SBL-mixers just got tougher, by including Mini-Circuits' exclusive Ultra-Rel diodes that can endure 160 hours of test at a scorching 300°C. Rugged, more reliable mixers in your systems lower production and test costs and increase systems reliability.

Over the past fifteen years, millions of SBL-units were installed in formidable industrial and commercial applications. Under severe operating conditions, they have earned the reputation as the world's most widely accepted mixers, based on quality, consistent performance in the field, and lowest cost.

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Unprecedented 4.5 sigma unit-to-unit repeatability is also guaranteed, meaning units ordered today and next year will provide performance identical to those delivered last year.

Tougher SBL-mixers, spanning 25KHz to 2000MHz, with +7dBm, +10dBm, and +13dBm LO models, priced from \$4.50 (10 qty) are available only from Mini-Circuits. Don't settle for a substitute or equivalent... insist on Ultra-Rel™ SBLs.



#### SBL SPECIFICATIONS (typ).

Model	Frequency (MHz)	Conv. Loss (dB)	Isolation (dB)		LO Level (dBm)	Price, \$ ea. (10 qty)
			L-R	L-I		
SBL-1	1-500	5.5	45	40	+7	4.50
• SBL-1X	10-1000	6.0	40	40	+7	6.25
SBL-1Z	10-1000	6.5	35	25	+7	7.25
SBL-1-1	0.1-400	5.5	35	40	+7	7.25
SBL-3	0.025-200	5.5	45	40	+7	7.25
• SBL-11	5-2000	7.0	35	30	+7	18.75
SBL-1LH	2-500	5.8	68	45	+10	5.50
SBL-1-1LH	0.2-400	5.2	64	52	+10	8.25
• SBL-1XLH	10-1000	6.0	40	55	+10	7.25
SBL-2LH	5-1000	5.9	61	54	+10	8.25
SBL-3LH	0.07-250	4.9	60	53	+10	8.25
• SBL-11LH	5-2000	7.0	45	30	+10	19.75
SBL-1MH	1-500	5.5	45	40	+13	9.80
SBL-1ZMH	2-1100	6.5	40	25	+13	11.70

• IF not DC coupled

#### \*ULTRA-REL™ MIXERS 5 yr. Guarantee

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CIRCLE NO. 4

F143 REV. ORIG



**On the cover:** High-density PLDs simplify design modifications and push clock speeds of 10 to 50 MHz. Choosing from the scores of PLDs available may be the toughest part of your design. See our Special Report on pg 76. (Photo courtesy Xilinx Inc; graphics by Harold Johnson)

## SPECIAL REPORT

### High-Density PLDs

76

The flexibility of high-density PLDs makes them attractive in many applications, but the lack of a universal yardstick for comparison makes it difficult to find the best choice for your application.—*Doug Conner, Technical Editor*

## DESIGN FEATURE

### C++ has C's familiarity and OOP capability

97

C++ adds a host of new features to C, including object-oriented programming (OOP) abilities. If you program in C, you can use these features without having to learn a whole new language.—*George Ellis, Industrial Drives*

## TECHNOLOGY UPDATES

### Multichip modules: Lack of standards impedes design issues

35

Multichip modules can double your circuit's performance, but limited die availability, heat dissipation problems, and testability issues will also boost your design and production costs. Not every application can justify the extra effort and expense this new technology demands.—*J D Mosley, Technical Editor*

### High-speed monolithic op amps: Low-cost op amps break speed barriers

53

Today's \$3 monolithic op amps can outdo their \$50 hybrid cousins and contend for many discrete closed-loop designs.—*Anne Watson Swager, Technical Editor*

## PRODUCT UPDATE

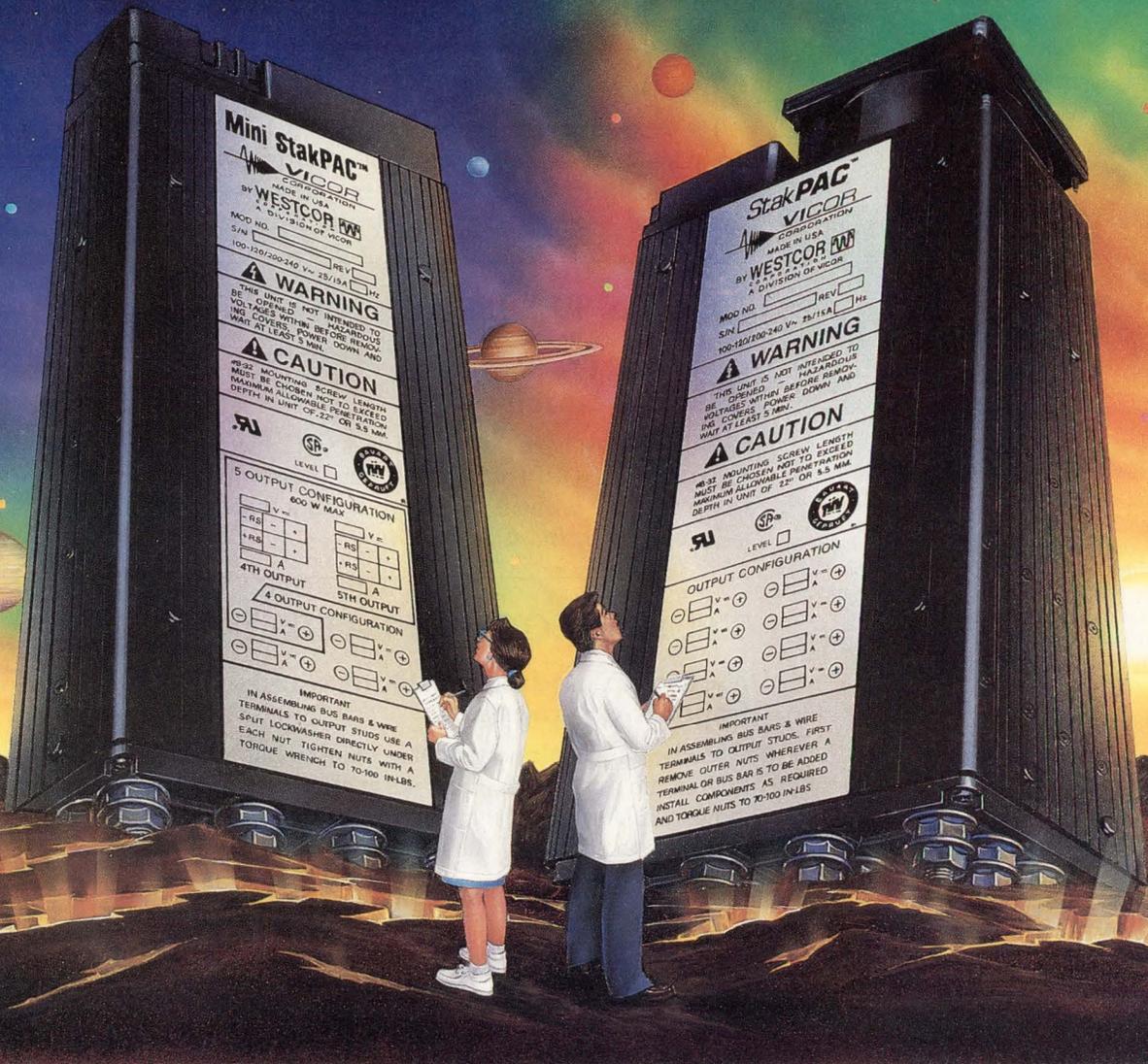
### 50-MHz synchronous cache RAMs

73

*Continued on page 7*

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# Power Revelation



Our Westcor division's family of configurable AC or DC input fan cooled StakPAC switchers reveals a new world of power density and output flexibility to the system designer...whatever your power needs. Each StakPAC is built with field proven robotically manufactured Vicor VI-200 Series power components providing you the flexibility of a customized supply combined with the off-the-shelf availability of standard catalog products...“first article” StakPACS are typically delivered in 2 weeks.

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MINI	600W	up to 5	110/220 VAC	1.9 x 5.5 x 12.2
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## DESIGN IDEAS

VFC consumes miniscule current	105
Design expands PC bus	106
Software Shorts	108

## EDITORIAL

29

Our January 20, 1992, issue will look different. Here is a quick overview of some of the things we're doing for you.

## NEW PRODUCTS

Test & Measurement Instruments . . . . .	119
Components & Power Supplies . . . . .	123
CAE & Software Development Tools . . . . .	129
Computers & Peripherals . . . . .	133
Integrated Circuits . . . . .	137

## DEPARTMENTS

News Breaks . . . . .	13
Ask EDN . . . . .	23
Career Opportunities . . . . .	145
EDN's Acronyms & Abbreviations . . . . .	151
EDN's International Advertisers Index . . . . .	151

### EDN BBS Update

EDN continues to upgrade the Bulletin Board System (BBS) to make it easier for you to access the information you need, when you need it. The BBS ((617) 558-4241) now has a 220-Mbyte drive, courtesy of Quantum.

The additional disk space accommodates 1000 new public-domain and shareware postings as well as more than 50 computerized tutorials, covering all popular programming languages and other topics. The BBS also features an expanded FORTH section. You can access the expanded scientific-calculator program library on the /sci\_calc Special Interest Group or the new math-software library on the /math Special Interest Group. Stay tuned for more.

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# FREE

Since we're one of the largest memory suppliers in the world and the Samsung SRAM program is one of the best, our advertising agency thought we should find a more dignified way to get our new fast 1-megs into your hands.

But we know that once you try them you'll buy them. And we believe these guys are, once again, overthinking. So: free SRAM it is.

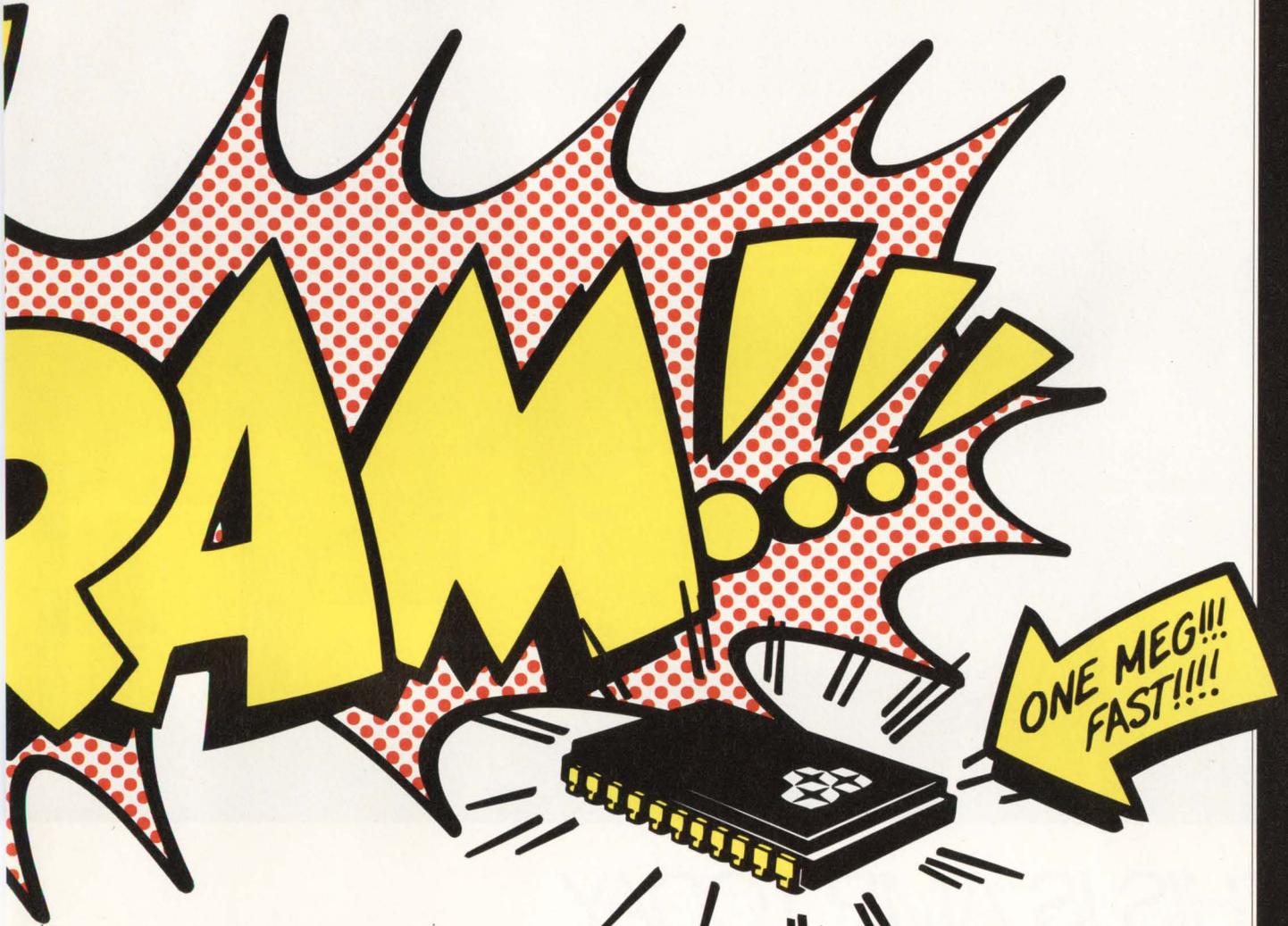
Our fast 1-megs run at 20 ns and are in full production in large quantities now.

#### 20 ns 1-MEG SRAMs FROM SAMSUNG

Part	Organization	Features
KM641005*	256K x 4	Separate I/O
KM641001*	256K x 4	
KM681001*	128K x 8	
KM611001*	1M x 1	

Like our 256K and 64K parts, which we're sampling now and will have in full production Q1 1992, they're part of our major SRAM

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commitment. We use our formidable DRAM capacity to make them.

All parts are in DIP and SOJ. Our new 256K and 64K chips run at 15 ns.

So if speed, technology, superb breadth of line, and state-of-the-art parts aren't

#### 15 ns 256K AND 64K SRAMs FROM SAMSUNG

Part	Organization	Features
KM64258B	64K x 4	Output Enable
KM64259B	64K x 4	Sep. I/O, High Z
KM64260B	64K x 4	Sep. I/O, Low Z
KM68257B	32K x 8	
KM61257A*	256K x 1	
KM64257A*	64K x 4	
KM6466B*	16K x 4	Output Enable
KM6465B*	16K x 4	
KM6865B	8K x 8	

\*Available now.

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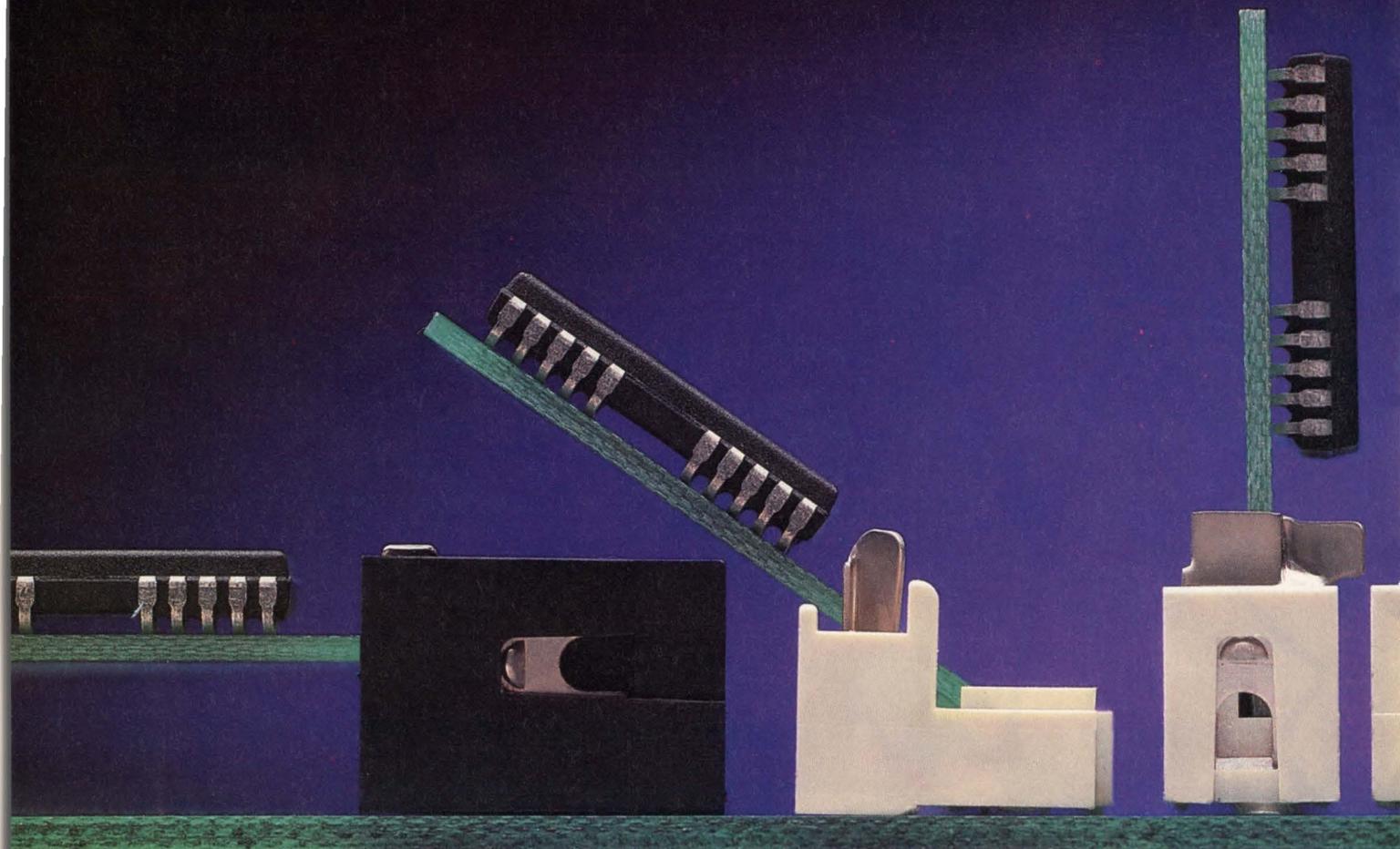


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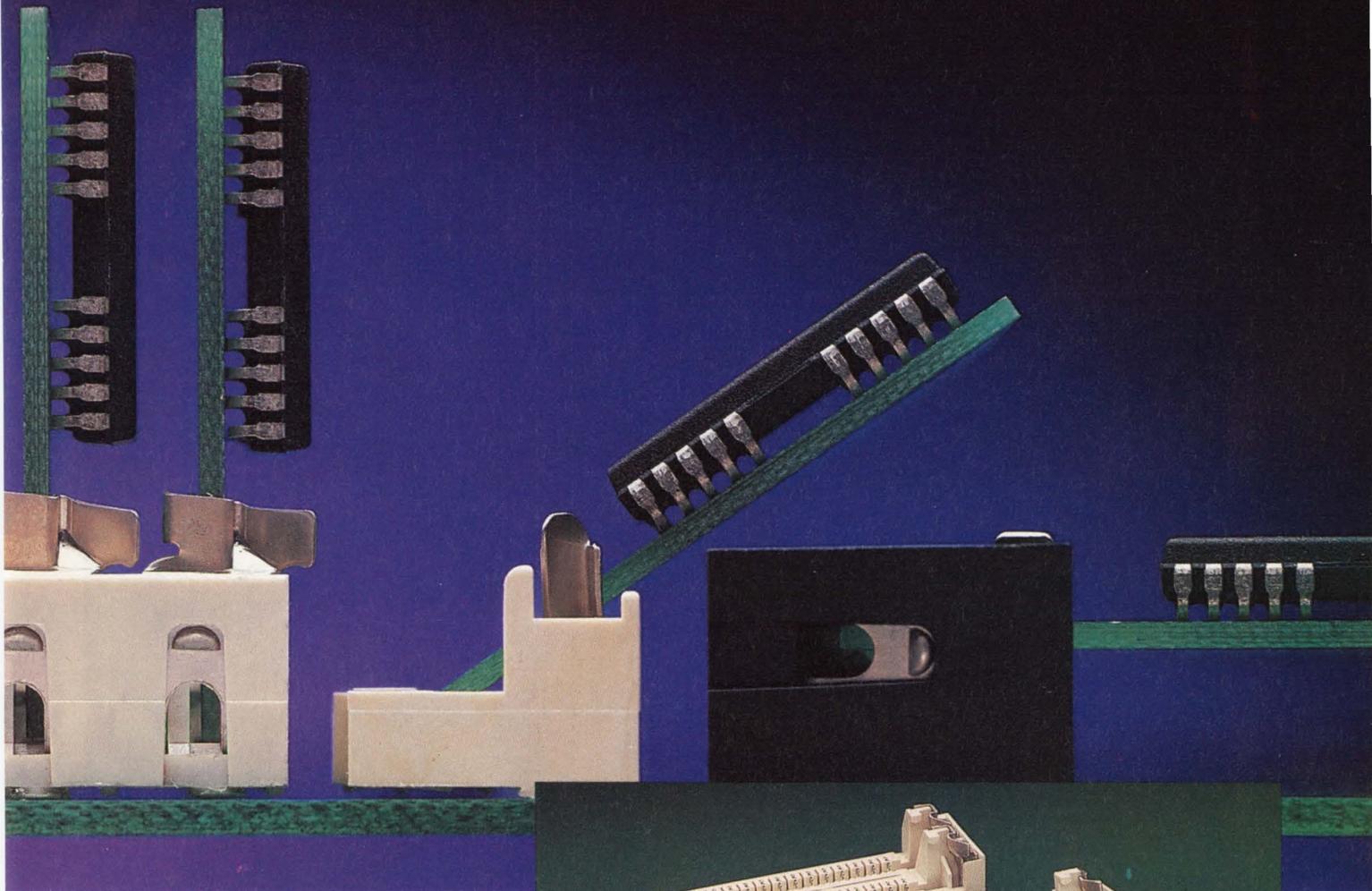
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# AMP

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# NEWS BREAKS

EDITED BY SUSAN ROSE

## **CPU LOCAL BUS EXTENDS TO PC ADD-IN CARDS**

I/O-intensive peripherals on ISA-based personal computers suffer from an 8-MHz limit on the bus speed. To bypass this bottleneck, manufacturers of ICs for functions such as video graphics and SCSI interfaces developed devices that connect directly to the CPU's local bus. The local bus solution, however, forces designers to put the peripheral interface device on the mother board, limiting design flexibility.

The situation has now changed. The DXBB AT-logic chip set from Opti Inc extends the local bus to a card-edge connector. The company has also defined the extension's pinout on an EISA-type connector, letting the connector carry both ISA and local bus-extension signals. The chip set has two parts, the 82C496 logic chip and the 82C206 peripheral controller. The logic chip works with '386 and '486 CPUs from Intel and AMD and includes an AT-bus controller and a block-interleave dynamic-RAM controller with '486 bursting support. The set costs \$27.50 (10,000). An optional write-back cache controller, the 82C497, is also available (\$17.50). Opti Inc, Santa Clara, CA, (408) 980-8178, FAX (408) 980-8860.—Richard A Quinnell

## **32-BIT RISC $\mu$ C WITH PERIPHERALS LOWERS DESIGN COSTS**

The 32-bit Am29200 microcontroller ( $\mu$ C) simplifies designs by incorporating an array of on-chip peripherals that minimizes the number of external components you must add to complete an embedded-control circuit. By attaching ROM, dynamic RAM, and electrical buffers to this  $\mu$ C, you provide all the components necessary for an embedded circuit that can control the hardcopy output of laser printers and fax servers. The RISC  $\mu$ C includes an on-chip ROM controller, RAM controller, 2-channel DMA controller, a 24-bit timer, a wait-state generator, 16 programmable I/O ports, serial and parallel ports, a peripheral interface adapter, an interrupt controller, and a video interface. The chip also contains JTAG diagnostics that decrease debug time and board-level testing. A 168-pin, 16-MHz version costs less than \$50 in OEM quantities for 5-MIPS performance. Sampling will begin in April 1992. Advanced Micro Devices, Austin, TX, (800) 292-9263, (512) 462-5651. —J D Mosley

## **SOFTWARE LETS MAC REPLACE LAB NOTEBOOK**

When you work with a scope on your lab bench, you're probably used to keeping sketches of schematics and test setups in a lab notebook, along with scope photos and hand-written notes about things you did or observations you made. GW Instruments's \$990 Superscope/488 for the Apple Macintosh lets your computer replace the lab notebook. The software lets you duplicate a DSO's (digital storage oscilloscope's) front panel and screen on the Mac's screen and lets you store and recall captured data and scope setups. By combining the software with a drawing program, such as MacDraw, and a word processor, such as MS Word, you can easily (with no programming) access all the functions you need, not merely to replace your lab notebook, but also to use your data in reports and presentations.

The company also makes IEEE-488 interfaces of the type you'll need to connect your scope to your Mac. For slotted Macs, the interfaces are Nubus boards; for the more compact machines, they are modules that plug into the SCSI port. A \$290 IEEE-488 instrumentation library includes software drivers for more than two dozen DSOs from four manufacturers as well as one for a digitizer. GW Instruments, Somerville, MA, (617) 625-4096, FAX (617) 625-1322.—Dan Strassberg

# NEWS BREAKS

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## **DSOs OFFER 1-MILLION-POINT RECORD LENGTHS**

If you have trouble getting enough timing resolution on your DSO (digital storage oscilloscope) when looking at long waveforms such as those in radar, sonar, and video applications, your troubles may be over. LeCroy has announced memory options up to 1-million points for several oscilloscope models. The 300-MHz model 9310 has two channels that independently operate at 100M samples/sec. The 1M-word memory-length instrument is \$9990. A shorter 10,000-word memory-length version of the DSO costs \$4990. The 7242B plug-in (\$22,900) for the 7200 DSO gives you a 1M-word memory while digitizing two channels at 1G samples/sec. Other DSO models and plug-ins with long memories are also available. LeCroy, Chestnut Ridge, NY, (914) 425-2000.—Doug Conner

## **ANALYZER ADDS 100-MHz CAPTURE SYSTEM AND 486 SUPPORT**

American Arium recently bolstered its ML4400 logic-analyzer family with a 100-channel, 100-MHz capture system and enhanced support for Intel's 80486  $\mu$ P. The 486-support package, Model 32I-486A, can handle all variations of the 80486 CPU, including Intel's 2-chip module that includes a second-level cache. The package offers complete disassembly of the executed instruction stream, including pre-fetched instructions, and handles segmentation and page translation. The new support package can also control the "KEN" cache-fill enable pin found on 486 CPUs. Finally, the package includes support for 10,000 downloadable symbols. Available now, the 32I-486A package costs \$2995 as an add-on to the ML4400 analyzer, or you can buy the ML4400I package that includes the 486 support and logic analyzer for \$11,985.

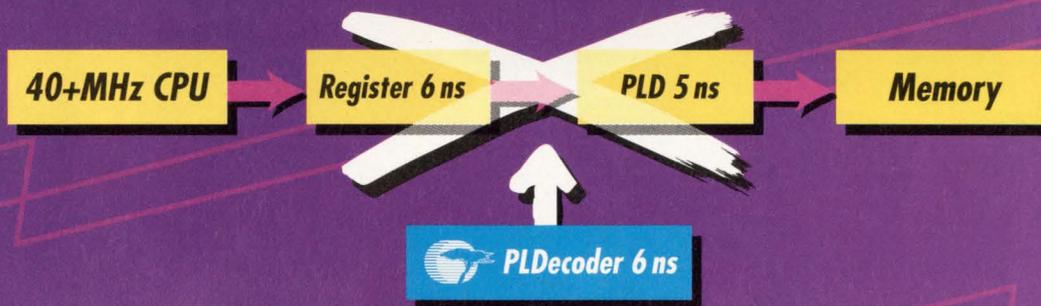
Meanwhile, the company's Paladin capture system boosts the capabilities of the analyzer family to work with the industry's fastest RISC and CISC CPUs. The system includes 100 100-MHz channels and can also be configured to provide 50 200-MHz channels. You can add multiple Paladin modules to a single logic analyzer to create more signal-capture capacity. The module provides a trace depth of 8 kbits per channel, and you can opt to expand trace depth to 128 kbits. The module includes 12 levels of triggering and 12 trigger-event recognizers. The module has probes that include signal compensation at the probe tip and that use coaxial cable. The Paladin module costs \$13,950 and will be available in February. —Maury Wright

## **POWER-FACTOR-CORRECTION IC REDUCES 3RD-HARMONIC**

The ML4821 from Micro Linear helps reduce 3rd-harmonic noise and excessive neutral-wire current in electronic power supplies. The device stores energy in an inductor or taps the stored energy as needed to maintain a sinusoidal current draw from the ac power lines. Without power-factor correction, a typical power supply only draws current during voltage peaks, causing noise spikes in the ac lines at odd harmonics of the line frequency. In a 3-phase system, the spike's 3rd harmonic can potentially add in-phase in the neutral wire, causing excessive current flow.

The device has several features that simplify its use in a system. It can accept ac input voltages from 90 to 260V, letting you use it in a variety of power systems without modifying the circuits. It offers built-in protection against brownout (reduced input voltage) and sudden load removal. The chip's output stage will drive as much as 1A. The \$3.55 (100) chip comes in an 18-pin DIP. Micro Linear Corp, San Jose, CA, (408) 433-5200, FAX (408) 432-0295.—Richard A Quinnell

# 40+MHZ MADE EASY.



## Introducing PLDecoders.

Taking systems to 40 MHz and beyond has become a whole lot simpler with these new, function-specific BiCMOS Decoder PLDs. For RISC, including our highest performance SPARC processors, choose the input-registered versions to capture addresses quickly. For CISC, such as 80X86, we offer output-latched versions that optimize system performance. Choose simple addressing versions at 6 ns for fastest performance, or 7 ns bank select or byte-write versions to suit your application precisely.

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### low pass, Plug-in, dc to 1200MHz

Model No.	Passband MHz loss < 1dB	Stopband, MHz loss > 20dB	loss > 40dB	Model No.	Passband MHz loss < 1dB	Stopband, MHz loss > 20dB	loss > 40dB
PLP-5	DC-5	8-10	10-200	PLP-250	DC-225	320-400	400-1200
PLP-10.7	DC-11	19-24	24-200	PLP-300	DC-270	410-550	550-1200
PLP-21.4	DC-22	32-41	41-200	PLP-450	DC-400	580-750	750-1800
PLP-30	DC-32	47-61	61-200	PLP-550	DC-520	750-920	920-2000
PLP-50	DC-48	70-90	90-200	PLP-600	DC-680	840-1120	1120-2000
PLP-70	DC-60	90-117	117-300	PLP-750	DC-700	1000-1300	1300-2000
PLP-90	DC-81	121-137	167-400	PLP-800	DC-720	1080-1400	1400-2000
PLP-100	DC-98	146-189	189-400	PLP-850	DC-760	1100-1400	1400-2000
PLP-150	DC-140	210-300	300-600	PLP-1000	DC-900	1340-1750	1750-2000
PLP-200	DC-190	290-390	390-800	PLP-1200	DC-1000	1620-2100	2100-2500

Price, (1-9 qty), all models: plug-in \$14.95, BNC \$32.95, SMA \$34.95, Type N \$35.95

### Surface-mount, dc to 570MHz

SCLF-21.4	DC-22	32-41	41-200	SCLF-190	DC-190	290-390	390-800
SCLF-30	DC-30	47-61	61-200	SCLF-380	DC-380	580-750	750-1800
SCLF-45	DC-45	70-90	90-200	SCLF-420	DC-420	750-920	920-2000
SCLF-135	DC-135	210-300	300-600				

Price, (1-9 qty), all models: \$11.45

### Flat Time Delay, dc to 1870MHz

Model No.	Passband MHz loss < 1.2dB	Stopband MHz loss > 10dB	loss > 20dB	VSWR 0.2fco X	0.6fco X	Group Delay Variations, ns fco X	2fco X	2.67fco X
PBLP-39	DC-23	78-117	117	1.3:1	2.3:1	0.7	4.0	5.0
PBLP-117	DC-65	234-312	312	1.3:1	2.4:1	0.35	1.4	1.9
PBLP-156	DC-94	312-416	416	0.3:1	1.1:1	0.3	1.1	1.5
PBLP-200	DC-120	400-534	534	1.6:1	1.9:1	0.4	1.3	1.6
PBLP-300	DC-180	600-801	801	1.25:1	2.2:1	0.2	0.6	0.8
PBLP-467	DC-280	934-1246	1246	1.25:1	2.2:1	0.15	0.4	0.55
▲BLP-933	DC-560	1866-2490	2490	1.3:1	2.2:1	0.09	0.2	0.28
▲BLP-1870	DC-850	3740-6000	5000	1.45:1	2.9:1	0.05	0.1	0.15

Price, (1-9 qty), all models: plug-in \$19.95, BNC \$36.95, SMA \$38.95, Type N \$39.95  
NOTE: ▲ -933 and -1870 only with connectors, at additional \$2 above other connector models.

### high pass, Plug-in, 27.5 to 2200MHz

Model No.	Stopband MHz loss < 40dB	loss < 20dB	Passband MHz loss < 1dB	VSWR Pass-band Typ.	Model No.	Stopband MHz loss < 40dB	loss < 20dB	Passband MHz loss < 1dB	VSWR Pass-band Typ.
PHP-25	DC-13	13-19	27.5-200	1.8:1	PHP-400	DC-210	210-290	395-1600	1.7:1
PHP-50	DC-20	20-26	41-200	1.5:1	PHP-500	DC-280	280-365	500-1600	1.8:1
PHP-100	DC-40	40-55	90-400	1.8:1	PHP-600	DC-350	350-440	600-1600	2.0:1
PHP-150	DC-70	70-95	133-600	1.8:1	PHP-700	DC-400	400-520	700-1800	1.6:1
PHP-175	DC-70	70-105	160-800	1.5:1	PHP-800	DC-445	445-570	780-2000	2.1:1
PHP-200	DC-90	90-116	185-800	1.6:1	PHP-900	DC-520	520-660	910-2100	1.8:1
PHP-250	DC-100	100-150	225-1200	1.3:1	PHP-1000	DC-550	550-720	1000-2200	1.9:1
PHP-300	DC-145	145-170	290-1200	1.7:1					

Price, (1-9 qty), all models: plug-in \$14.95, BNC \$36.95, SMA \$38.95, Type N \$39.95

### bandpass, Elliptic Response, 10.7 to 70MHz

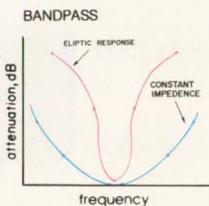
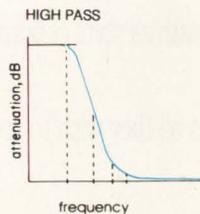
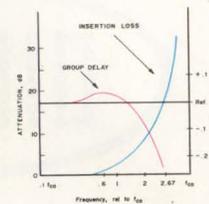
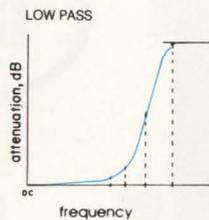
Model No.	Center Freq. (MHz)	Passband I.L. 1.5 dB Max. (MHz)	3 dB Bandwidth Typ. (MHz)	Stopbands I.L. > 20dB at MHz	I.L. > 35dB at MHz	Model No.	Center Freq. MHz	Passband MHz loss < 1dB	Stopband loss > 20dB at MHz	VSWR 1.3:1 Total Band MHz
PBP-10.7	10.7	9.6-11.5	8.9-12.7	7.5 & 15	0.6 & 50-1000	PIF-21.4	21.4	18-25	1.3 & 150	DC-220
PBP-21.4	21.4	19.2-23.6	17.9-25.3	15.5 & 29	3.0 & 80-1000	PIF-30	30	25-35	1.9 & 210	DC-330
PBP-30	30	27.0-33.0	25-35	22 & 40	3.2 & 99-1000	PIF-40	42	35-49	2.6 & 300	DC-400
PBP-60	60	55.0-67.0	49.5-70.5	44 & 79	4.6 & 190-1000	PIF-50	50	41-58	3.1 & 350	DC-440
PBP-70	70	63.0-77.0	68.0-82.0	51 & 94	6.0 & 193-1000	PIF-60	60	50-70	3.8 & 400	DC-500
						PIF-70	70	58-82	4.4 & 490	DC-550

Price, (1-9 qty), all models: plug-in \$18.95, BNC \$40.95, SMA \$42.95, Type N \$43.95

### Constant Impedance, 21.4 to 70MHz

Model No.	Center Freq. MHz	Passband MHz loss < 1dB	Stopband loss > 20dB at MHz	VSWR 1.3:1 Total Band MHz
PIF-21.4	21.4	18-25	1.3 & 150	DC-220
PIF-30	30	25-35	1.9 & 210	DC-330
PIF-40	42	35-49	2.6 & 300	DC-400
PIF-50	50	41-58	3.1 & 350	DC-440
PIF-60	60	50-70	3.8 & 400	DC-500
PIF-70	70	58-82	4.4 & 490	DC-550

Price, (1-9 qty), all models: plug-in \$14.95, BNC \$36.95, SMA \$38.95, Type N \$39.95



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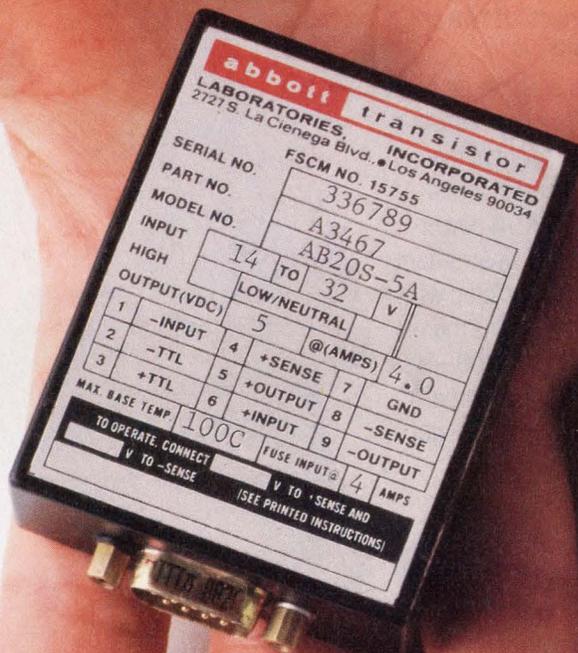
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### Compare the stats:

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<b>Frequency Range, A</b>	225 MHz	100 MHz	200 MHz
<b>Frequency Range, C (optional)</b>	2.7 GHz	1.3 GHz	1.3 GHz
<b>Single Shot Res.</b>	500 ps	2 ns	2ns
<b>Max. Reading Rate</b>	2000/s	150/s	125/s
<b>Base Price</b>	\$2,075*	\$2,305	\$5,000

\* GPIB interface optional (\$550)

Besides setting a faster pace, the PM 6680 adds new time and frequency analysis tools. Built-in mathematics and statistics functions give you stand-alone processing power that makes it easy to obtain measurements such as drift and rate of drift.

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And a host of new measuring capabilities give you the versatility to address your toughest measurement problems.



Rise time, duty factor, phase, and volt min/max measurements are all standard. Our unmatched arming flexibility enables you to measure rise time or pulse width on selected pulses within a stream. And the PM 6680 boasts six totalizing modes—including up/down counting and counting over a preset time.

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CIRCLE NO. 81

EDN January 2, 1992

# ASK EDN

EDITED BY JULIE ANNE SCHOFIELD

## LEDs still in style

In the September 2, 1991, Ask EDN, you stated that Rohm is phasing out its LED product lines. This statement is completely false. Rohm has no plans whatsoever to curtail the availability of its LED product offerings. Although there has been an international industry-wide increase in demand for LED lamps for the past 12 months, Rohm has made significant progress to comply with this demand.

The temporary international LED shortage has been a classic irony. We believe it was created, in part, by increased LED manufacturing capability. That is, as LED manufacturers strove to increase yield, several new quantity-hungry applications quickly emerged in hotly competitive markets, such as automotive and outdoor-sign industries. Many of these customers require deliveries of millions of pieces. In response to this increased demand, Rohm has increased lamp production in our main factory by 32%.

Improved LED manufacturing technology has contributed two critical benefits to lighting applications, particularly in the automotive and outdoor sign industries. The first benefit is increased brightness. With one LED contributing as much as 3 candlepower, a small cluster of these LEDs can now rival the luminous intensity of a large incandescent bulb. The second benefit is higher reliability. LEDs have typical life cycles of 100,000 hours, compared with 5000 hours typ for incandescent lamps.

The combined benefits of reduced power consumption and heat dissipation, reduced weight, shock resistance, and lower frequency of replacement are driving automotive designers to employ LEDs in place of incandescent lamps in many situations. These applications include instrumentation, dashboard lighting, and even tail lights that are easily visible from 1500 feet away. When you consider the number of primary- and after-market OEMs and multiply that by the number of applications per vehicle, the sheer volume required is enormous.

Outdoor signs are another bright spot. With signs as large as billboards each requiring tens of thousands of LEDs, demand increases with each new installation. These applications include highway signs, entertainment centers, and information displays.

Added to these new applications is the traditional industrial and consumer electronics market, whose appetite for indicator lights, displays, and graphics continues to increase faster than the overall economy.

Rohm will continue to increase its LED production. We are definitely not phasing out of the LED business.

*Ray Ponkey*  
Product Manager, Optoelectronics  
*Martin Miller*  
Market Services Manager  
Rohm Corp  
Antioch, TN

Ask EDN regrets the error and any unfortunate effects it may have had on your business.

## Star Trek tech

I have acquired my own Intel Microprocessor Development System (MDS) 231, and I am trying to locate a source-file listing of the company's famous Star Trek V2.0, which was originally written in Fortran by Matuszek and Reynolds and rewritten and expanded for the Intellec MDS by Intel's Ron Williams in 1977.

I believe I have located two bugs, and because I have only the object file on disk and the type-written "Guide to Star Trek V2.0," I presume that I need to edit the source file and recompile the object code. To do this, I guess I'll have to obtain a copy of the compiler as well.

I would also appreciate a hint or two as to how to stop the program running on the MDS. Is this possible? If anyone can help, I may yet defeat the Klingons!

*M J Garraway*  
Birmingham, UK

Have you been keeping up with "Star Trek—The Next Generation"? The Federation is now at peace with the Klingons. In fact, a Klingon, Worf, serves as the USS Enterprise's chief security officer.

However, if any reader has or knows where to get the Star Trek V2.0 source-file listing or compiler, please contact Ask EDN.

## What does BNC stand for, anyway?

In response to readers' continually asking what all those acronyms, abbreviations, and initialisms stand for, EDN has been including a box, "Acronyms used in this article," in each Special Report, Technology Update, and contributed article. Starting with the December 19, 1991, issue, we will collect all the acronyms used in the articles and what they stand for and put the information on an acronym page near the back of the magazine.

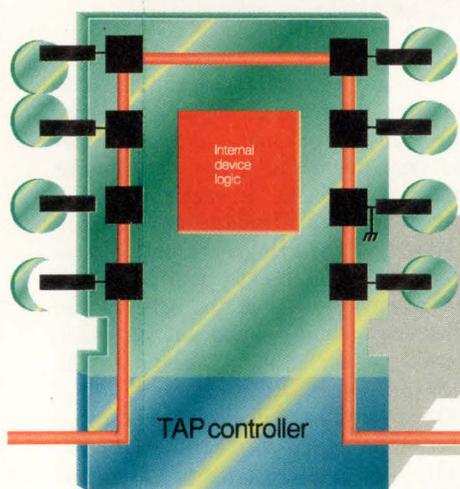
One initialism that has inspired much internal debate at EDN has been BNC connector. Some editors argued that the BNC stood for baby N connector. Others suggested British National connector and British Naval Committee connector. Still others favored bayonet N connector.

Associate Editor Dave Pryce finally laid the issue to rest when he came across a 1990 article in the *Microwave Journal*. Apparently the BNC connector was developed jointly by Neill and Concelman, who lent their initials to the connector's name. The B stands for baby because of the connector's small size.

However, we still haven't agreed on how to pronounce the prefix "giga."

Ask EDN solves nagging design problems and answers difficult questions. Address your letters to Ask EDN, 275 Washington St, Newton, MA 02158. FAX (617) 558-4470; MCI: EDNBOS. Or send us a letter on EDN's bulletin-board system at (617) 558-4241: From the Main System Menu, enter SS/ASK\_EDN and select W to write us a letter.

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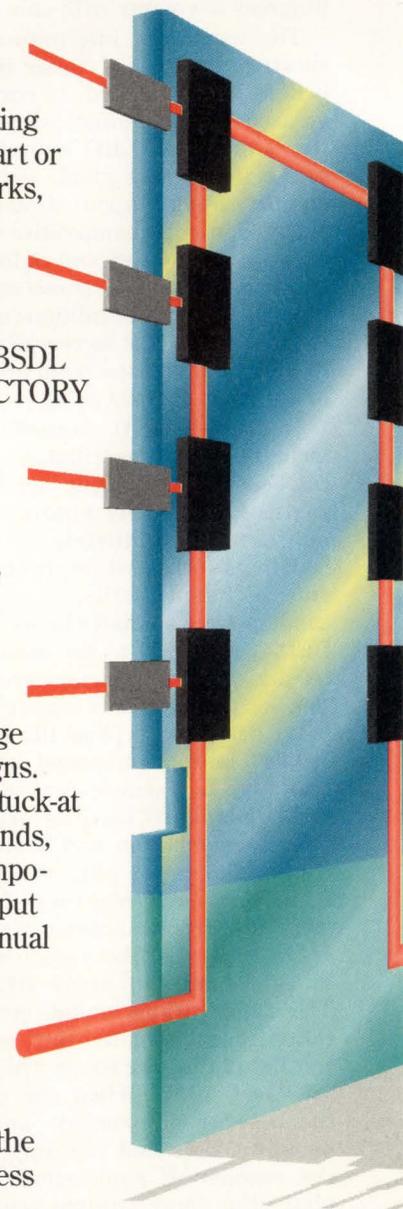
Increasing device complexity. Rising pattern development costs. High density packaging. Disappearing nodal access. These are the board test problems boundary scan was created to solve. Which is fine in theory. Only problem is there hasn't been any way to put boundary scan to the test. Until now.

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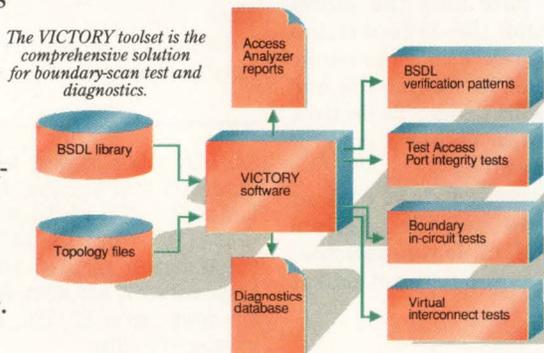
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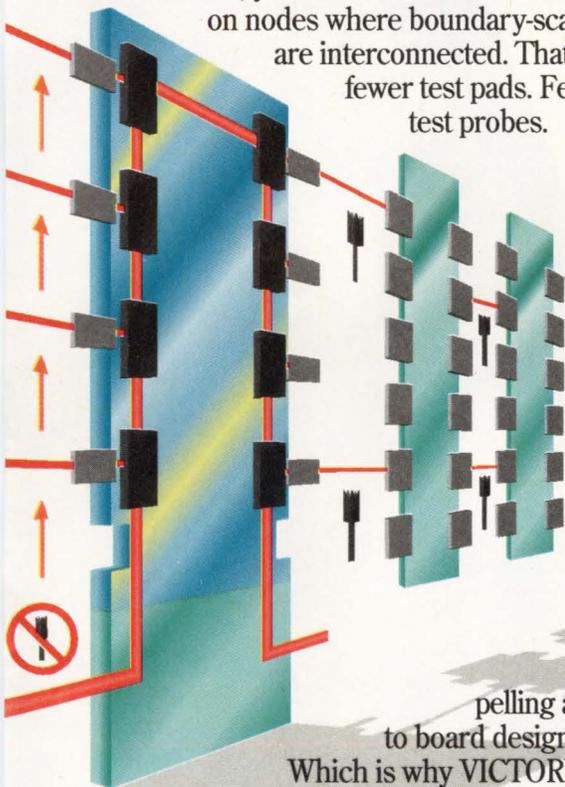
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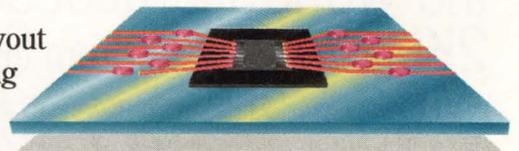
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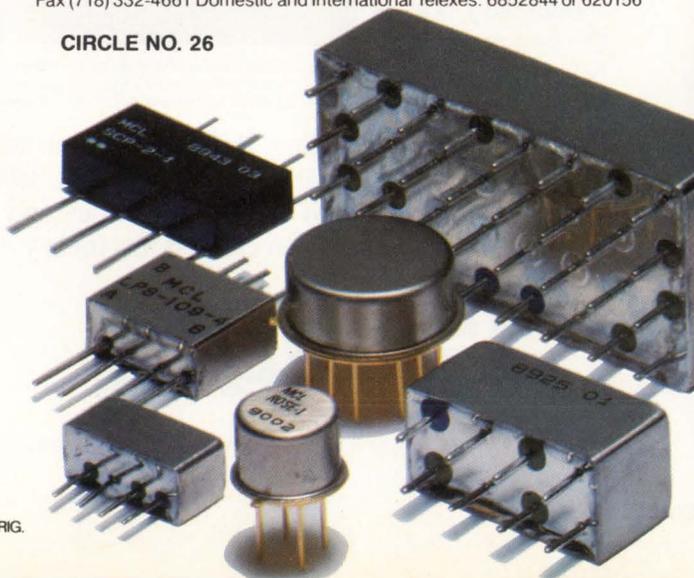
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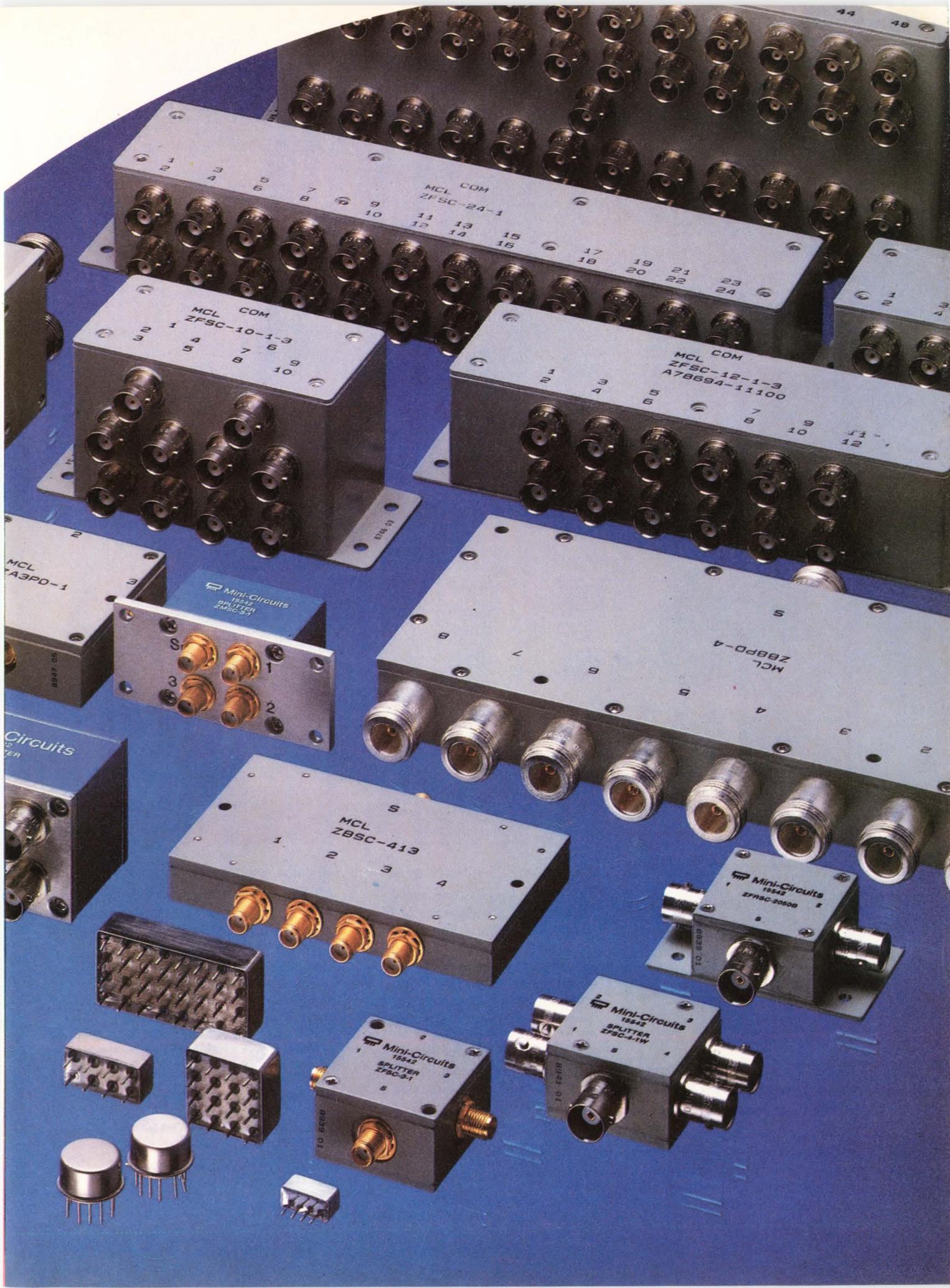
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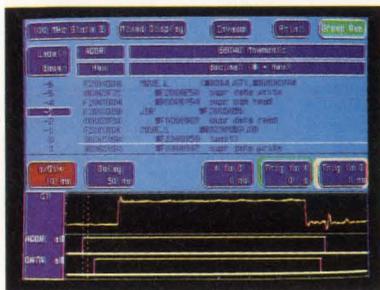
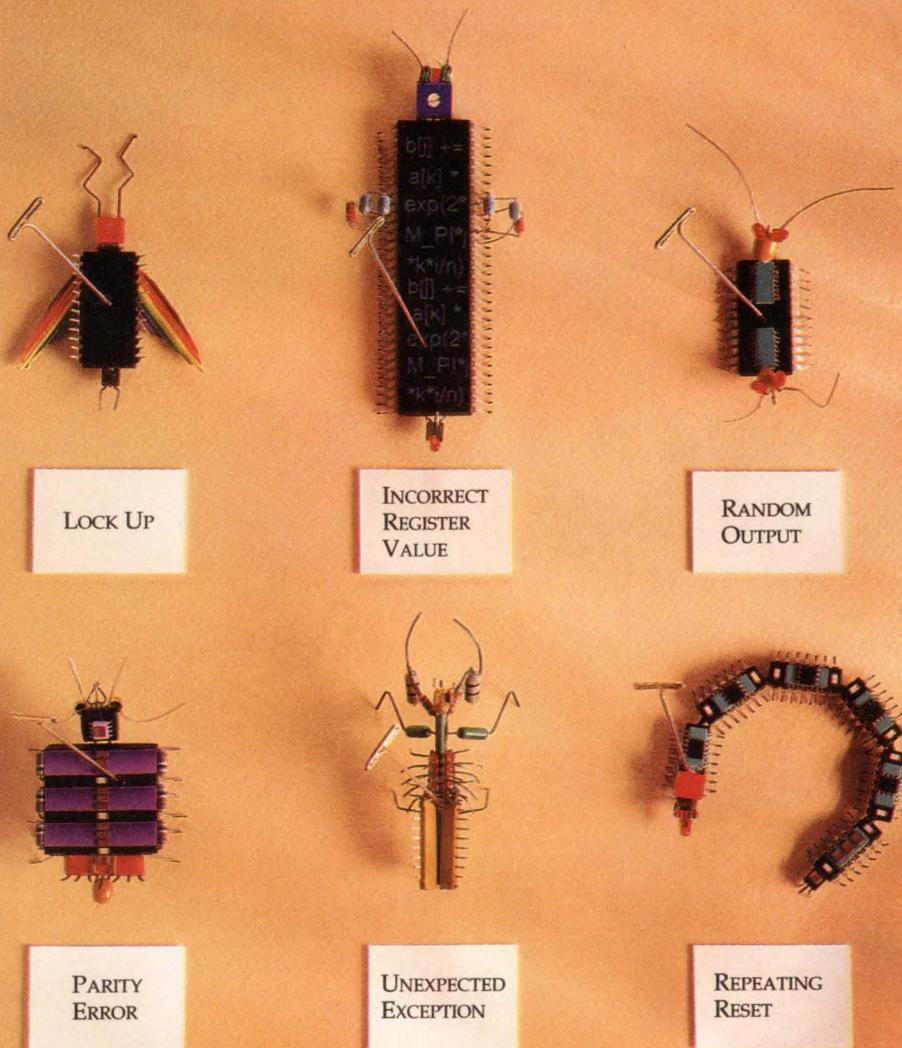
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# EDITORIAL

## More about what's coming in EDN



Last issue I gave you a hint of the changes to come in the January 20, 1992 issue of EDN. Now here is the rest . . .

We'll be running a new page called "Inside EDN" right near the table of contents. This page will tell you more about what's in the issue and why those articles are important to you. You'll also find out why we're covering these subjects and how the editors got the information for you. In some instances, we will also tell you about how we selected the products or companies that we discuss. This page will help you pick out the highlights of the issue.

You'll also notice that we're using consistent labels and formats for each section. We want to make it easy for you to find the things you're interested in. Color-coded title and section bars can help. Nothing irks me more than seeing an interesting title on a magazine's cover and then being stymied as I try in vain to find it in the table of contents. Somewhere in between, the title or subject matter changed. In EDN, we'll stay with consistent titles from the front page, to the table of contents, to the article. Also, page numbers will accompany the titles on the cover. If you see an article you like, why should you have to go to the table of contents first?

We believe in making information as available and accessible as possible. In the past, we've heard complaints about acronyms and abbreviations that go undefined or unexplained. You'll find a new acronyms and abbreviations page in EDN that compiles and spells out all the complex acronyms and abbreviations we've used. Obviously we won't spell out ac, dc, or V, but you'll find VXIbus, VHDL, and FPGA if we've used them in the issue. You'll be able to tear out the pages for later use. I expect this section will be very popular.

Because Design Ideas has always been popular, we've made it easier to find and more comprehensive. You'll notice expanded "Feedback and Amplification" and "Software Shorts" coverage. We're also tinting the Design Ideas pages light blue so that you can find them right away just by bending the magazine to expose the outer edges of the pages. You'll also find the traditional yellow News Breaks pages this way. Look to the News Breaks section for changes, too. We'll be running more items in a typeface and format that makes them easier to read.

One final thing to keep in mind is, as I said in my previous editorial, the changes we've made result from discussions with and comments from readers. Once you look through our January 20, 1992 issue, I'd like to know what you think. We'll continue to evolve and we're always open to new ideas and suggestions. Enjoy.



Jesse H. Neal  
Editorial Achievement Awards  
1990 Certificate, Best Editorial  
1990 Certificate, Best Series  
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1977, 1976, 1975

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A handwritten signature in black ink that reads "Jon Titus".

Jon Titus  
Editor

Send me your comments via FAX at (617) 558-4470, or on the EDN Bulletin Board System at (617) 558-4241 300/1200/2400, 8, N, 1.

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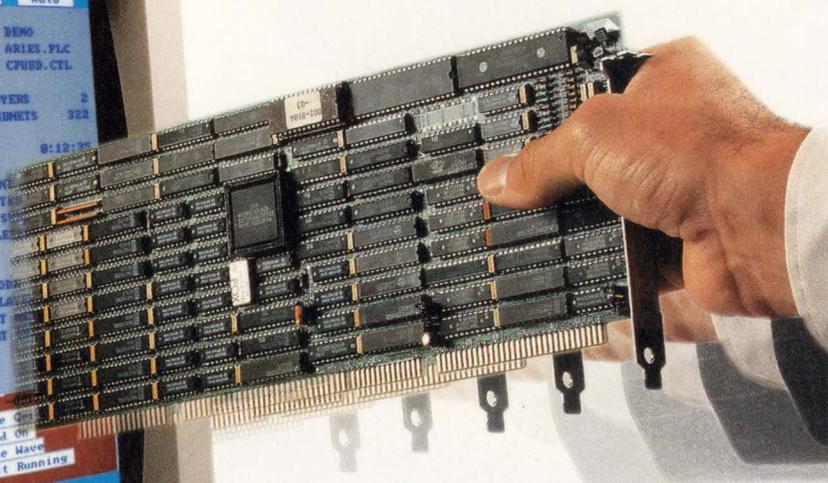
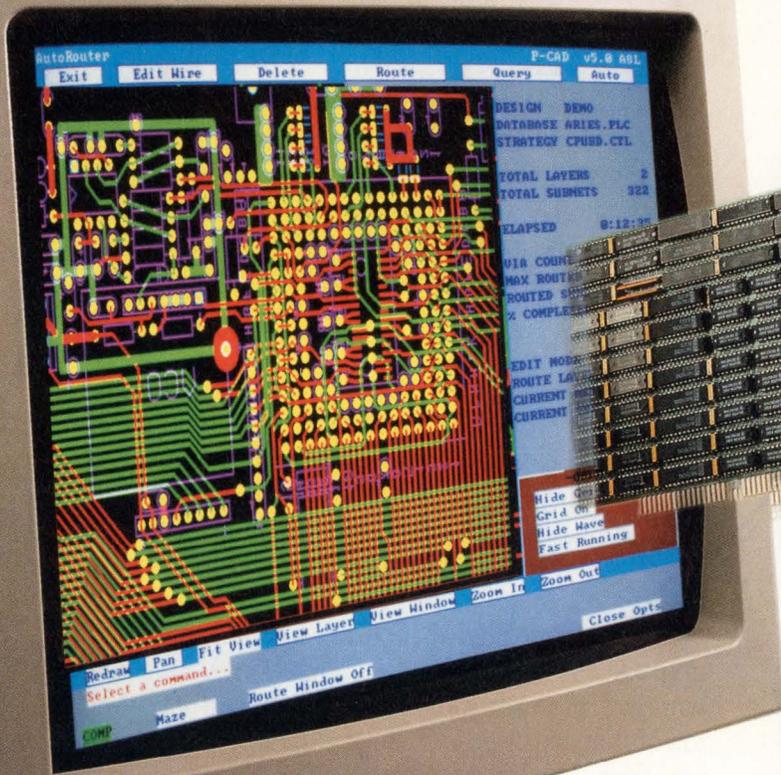


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## MULTICHIP MODULES

# Lack of standards impedes design issues

Multichip modules can double your circuit's performance, but limited die availability, heat dissipation problems, and testability issues will also boost your design and production costs. Not every application can justify the extra effort and expense this new technology demands.

**J D Mosley**  
Technical Editor

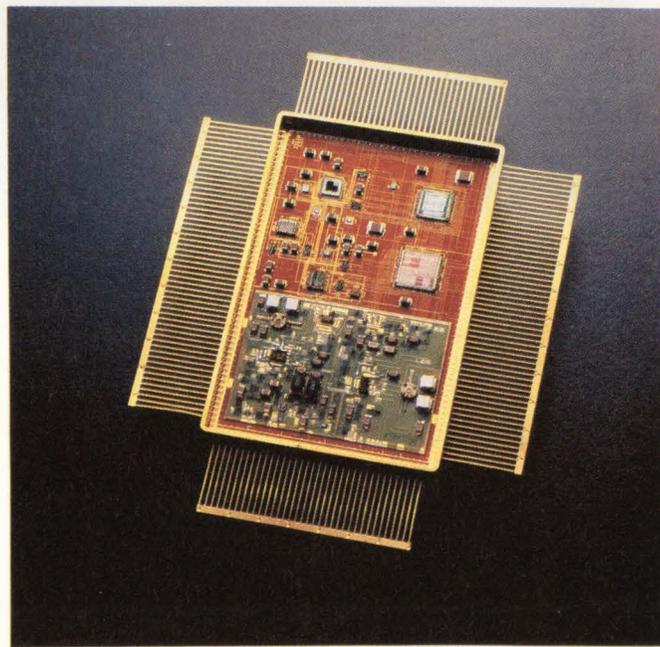
**M**ultichip modules (MCMs) are the current high-performance champions that promise to pacify designers' insatiable desire for higher-performance circuits. However, an immature infrastructure makes this a technology that your design team should approach with objective awareness and a healthy budget.

As with any emerging methodology, the early adopters will have to contend with a lack of standards, high fabrication costs, and numerous unresolved design issues. However, with powerhouses such as IBM, Texas Instruments, and AT&T announcing their support for MCM development, the technology should become an established design method within two or three years.

MCMs are conceptually simple: By placing several unpackaged ICs (or bare dies) directly upon a pc-board substrate, you can trim the length of die interconnections by 50% or more, because you can position each bare die closer to neighboring ICs. These shorter pc-board traces result in faster signal propagation times and increased signal fidelity. In addition, the lack of bulky die packages let the circuit occupy significantly less space in your product—a major consideration in avionic and portable applications.

However, the first problem encountered by MCM designers is the limited availability of fully tested bare ICs, commonly referred to as *known-good dies*. Once an MCM is assembled, if any single die on the substrate is defective, you will have to repair or even dispose of the entire module, thereby escalating costs, lowering yields, and lengthening your time to market.

Consider the case of Cypress Semiconductor's \$3200 CYM6002K dual-SPARC CPU module for which the issue of known-good die was a major concern during design. The price of reworking such an expensive module would have significantly escalated production costs. Andy Paul—president of Multichip



Providing telecommunications and networking functions at 622 MHz, this custom multichip module was designed using Valid Logic's Allegro MCM Design System.

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# TECHNOLOGY UPDATE

## Multichip modules

Technology, a Cypress subsidiary that participated in the development of the SPARC module—sees the problem of obtaining known-good dies as a major MCM stumbling block.

Paul notes that although it seems like a bare die should be less expensive than a packaged IC, most designers find they must instead pay a premium. Volume production is what lowers the price of chips, and currently the demand for bare dies isn't sufficient to offset the necessary manufacturing changes. As a result, bare dies are custom items that command a premium price.

Paul acknowledges that complex chips with 300 or more pins may actually cost less in die form. However, because of their unusually high packaging cost, you should normally expect your MCM to cost more than a comparable pc-board version. That is, unless you can populate your MCM with ICs that are routinely offered as tape-

automated-bonding (TAB) components.

TAB involves a leadframe that is etched onto a film carrier. This leadframe is then soldered or welded onto a die. TAB is superior to wirebonding the die directly to the substrate because of its  $0.017\Omega$  resistance,  $0.006\text{-pF}$  capacitance, and  $2.1\text{-nH}$  inductance. Typical wirebond characteristics are  $0.142\Omega$ ,  $0.025\text{ pF}$ , and  $2.6\text{ nH}$ , respectively. Furthermore, TAB thermal resistance measures  $8^\circ\text{C/W}$ , vs the  $79^\circ\text{C/W}$  for wirebond circuits. TAB parts can achieve signal speeds in excess of  $150\text{ MHz}$ .

TAB frames, in volume, are inexpensive and fully testable at speed. And once tested, they are relatively simple to bond to miniature boards. The TAB infrastructure is more developed than bare-die or flip-chip infrastructures, and TAB parts don't require exotic substrates. As Paul notes, substrates made from silicon and diamond grossly exceed

current performance requirements because today's  $50\text{-MHz}$  circuits "run very comfortably on high-density FR4 boards—you certainly don't need silicon substrates to do that."

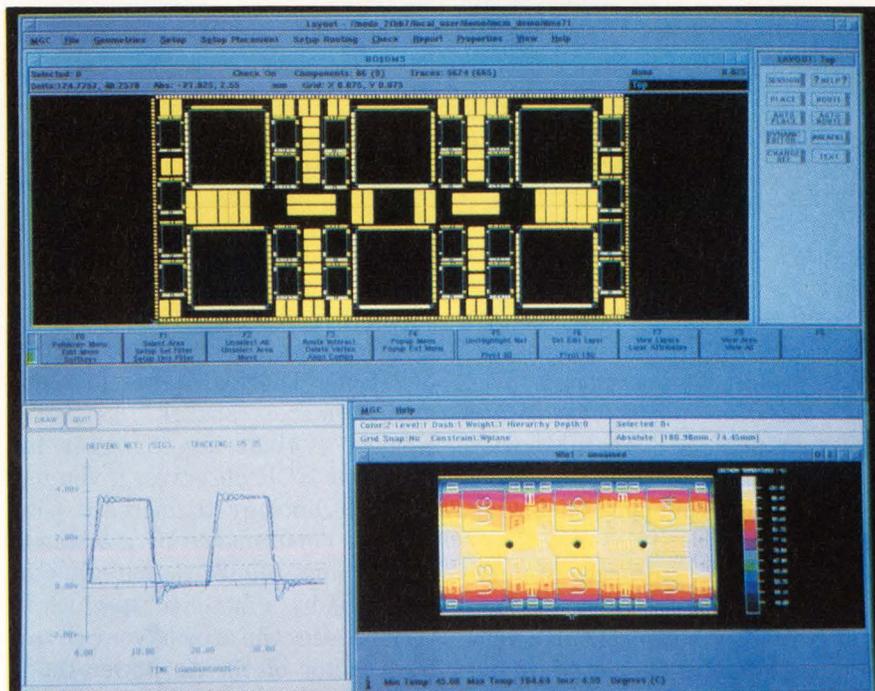
NCR's strategic products manager, Harold Crafts, observes that the OEMs can no longer sit back and wait for IC vendors to develop state-of-the-art components at rock-bottom prices. Military spending is plunging, so government dollars aren't available to fund cutting-edge technology as was true in the past.

When NCR designers require ICs that aren't available in TAB frames, they request a flip chip, perform the TAB design in-house, and obtain a subcontractor to do the TAB tape manufacturing and interlead bonding. And if a flip chip isn't available, NCR engineers will develop a TAB part from wafers—albeit reluctantly. However, the ultimate plan is to get NCR completely out of the TAB loop—a goal Crafts estimates is at least a couple of years away.

### Who will foot the bill?

The investment of getting into TAB is what is keeping the supply of TAB ICs low. The IC manufacturers face large capital expenditures in order to convert their production facilities to TAB. In addition, OEMs must develop the capability to do the trimming and forming required to utilize TAB parts. Such expenses limit the widespread use of TAB, which in turn keeps prices high and availability low.

Shiv Tasker, director of marketing for packaging and interconnect at Valid, says that companies proficient in packaging may be in a better position to drive MCM technology than IC manufacturers because such companies can act as neutral intercessors for multiple IC vendors. IBM, for example, is capitaliz-



**Multiple design windows provide a concurrent framework** within Mentor Graphics' MCM Station. The top window shows placement of the die upon an MCM substrate; the bottom right window displays a thermal map of the module, and a high-speed analysis occupies the bottom left window.

# TECHNOLOGY UPDATE

## Multichip modules

ing on its packaging and manufacturing expertise and selling that expertise to other companies. Such aggressive participation by major corporations makes the infrastructure for MCMs look better and enables less well-heeled firms to add MCMs to their products, thus further increasing demand and driving the technology.

### The right tool for the job

As IBM customers realize, designing the module itself is a process that has its own set of stumbling blocks for MCM neophytes. Fortunately, you can select from a number of first-generation electronic design automation (EDA) packages to help you layout and simulate your MCM. Valid's \$50,000 Allegro-MCM, Harris' \$30,000 Finesse MCM/CAD, and Dazix's \$18,000 MCM Engineer individual modules, and Mentor Graphics' \$128,900 MCM Station complete system are all properly termed first-generation tools because none effectively anticipate the effects of crosstalk on an MCM design. Crosstalk is an issue that each of these software vendors plans to address in the next revision of their products.

Notably, each of these EDA packages has its proponents. For example, IBM is incorporating Valid's Allegro-MCM as part of its commercial MCM marketing venture, and Mentor Graphics proudly notes that its MCM Station was used to develop Cypress' credit-card-size CYM6122L SPARC module for use in Sun's 600MP multiprocessing workstation.

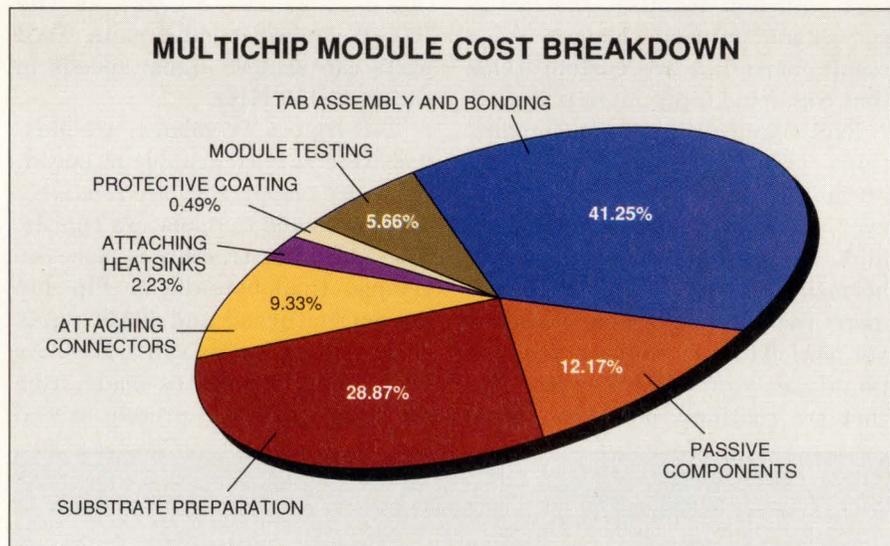
The crosstalk problem is caused in part to parallel signal paths running through the substrate. Certain rules-of-thumb involving the length of such parallel paths and trace width per layer can reduce impedance and minimize interconnect delays. Shielding and ground paths can further minimize the problem.

Regardless, engineers still frequently find themselves in a redundant loop of design-analyze-fix-analyze-fix-analyze because each design correction results in a new performance problem. And the more complex the design, the less useful simple rules of thumb are, as is the case if you attempt to minimize crosstalk when a 30-line bus spans an MCM.

John Isaac, advanced packaging product manager at Mentor Graph-

entity must either develop an IC-model translator or a unified simulation environment with standardized IC models.

For example, a layout based on timing constraints would incorporate predefined rules to control placement and routing for high-performance designs. Such a performance-driven layout would rely on physical rules for high-speed interconnect and take into consideration details such as differential-



*The cost of TAB assembly and bonding and the cost of substrate preparation constitute the two major factors affecting the price of MCMs, according to this analysis by MCC. The QTAI project and the TAB technology development project are working toward lowering these costs.*

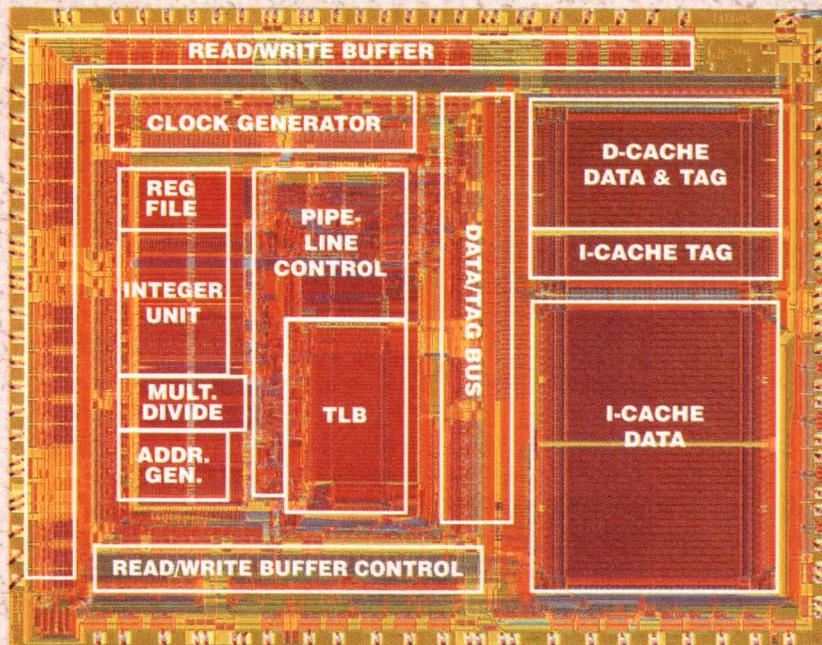
ics, says that the EDA vendors aren't merely slacking off. The lack of consistent standards among IC manufacturers for bare-die characteristics and timing models prevents the development of software that can provide signal-integrity analysis and critical-path timing analysis. "You can't aim at a moving target," Isaac notes.

Furthermore, accurate simulation requires consistent IC models. Unfortunately, different IC vendors use different simulators to develop their chips. So, even when the vendors provide models, the models aren't consistent across the industry. To achieve consistency, some

pair routing, termination assignments, net topology, and clock skew.

Another significant design issue involves the thermal characteristics of MCMs. Thermal issues increase as geometries shrink. As Steve Easley, engineering manager for MCMs at NCR observes, if you use MCM technology to increase your circuit's performance by a factor of 3, you must reduce the circuit's dimensions by a factor of 3, which in turn reduces the area of your circuit by a factor of 10. As power tends to be more linear with dimension than with area, the power per unit area tends to increase as you reduce the size of your circuit.

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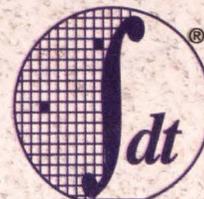
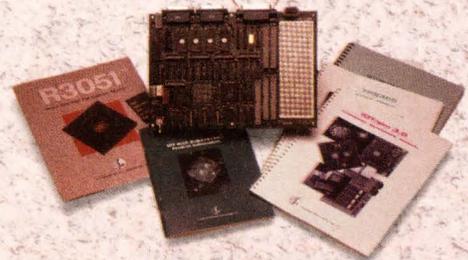
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# TECHNOLOGY UPDATE

## Multichip modules

Accordingly, you need accurate thermal modeling to design MCMs. Simulating modules in terms of heat dissipation and temperature means designing heat sinks for these devices with 3-D thermal modeling. In addition, MCMs can incorporate thermally conductive materials to help manage heat dissipation. By placing metal columns, called thermal vias, through the MCM substrate, you can draw heat away from the die and keep it from dissipating unwanted heat to neighboring devices.

Unfortunately, even after you complete your MCM design, another problem caused by the lack of standardized test strategies arises. MCMs require real-time testing with diagnostics for their components and functions. But to obtain consistent strategies for boundary testing, the IC manufac-

turers must agree upon one form of built-in system test. The agreed upon test should be a functional testing of the completed module via the I/O pins. This type of test is necessary because the bare die is too small to probe with a bed-of-nails approach.

Texas Instruments is the only US silicon manufacturer that has announced plans to incorporate the Joint Test Action Group (JTAG) self-test standard. JTAG, which is also referred to as IEEE 1149.1 or boundary scan, provides a hardware basis for implementing a basic mechanism for self-test. However, companies must still develop internal test mechanisms to utilize such on-board logic. And because JTAG is a hierarchical test structure requiring test ports at the die, module, and board levels, sophisticated software tools are needed to manage

the volume of test data generated by each of the chips in the module.

The principal functions that will evolve from standardized testing include automatic test-pattern generation and test insertion into netlists. Easley predicts test insertion and data management tools will be commercially available within the next year or so.

### A meeting of the minds

Of course all of these timetables rest upon the assumption that technical standards will emerge. Such basic factors as physical size constraints, pin assignments, substrate composition, test methodologies, and electrical specifications have to be defined before MCM design can become as straightforward as ASIC design is today.

Because the government, via military spending, has taken no

## For more information . . .

For more information on the multichip modules and design tools discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you read about their products in EDN.

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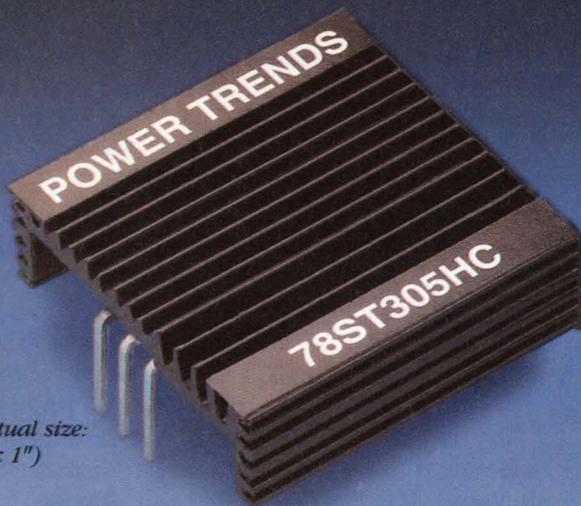
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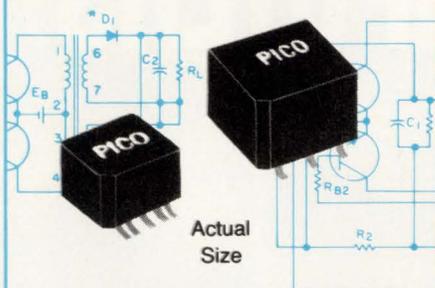
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# TECHNOLOGY UPDATE

## Multichip modules

firm stand on the issue of standards, the only other US entity with sufficient clout to facilitate acceptance of de facto standards is the Microelectronics and Computer Technology Corp (MCC). MCC is a cooperative research venture involving 55 North American companies. MCC currently has an assortment of 10 packaging and interconnect projects in progress and at least six more anticipated. The company has targeted MCM development because it encompasses key packaging technologies such as substrate design and development, bonding and assembly, testing, powering, and cooling.

In an effort to reduce cost and turn-around-time problems, MCC developed a high-density interconnect technique for programmable MCMs. The Quick Turnaround Interconnect (QTAI) technique begins with a prefabricated, blank-interconnect array in a copper polyimide (CuPi) substrate. You can mass produce such generic substrates for high-volume cost reduction.

Later, you can automatically route the substrates through thousands of interconnects via software based on a description of the chip-pad placement and a netlist. This routing personalizes the substrate according to customer orders and specific chip sets. MCC estimates that the QTAI approach can reduce turnaround time by 60 to 70%. MCC has successfully demonstrated QTAI by designing, producing, and testing a crossbar-switch MCM with 16 ICs and a 2-Mbyte nonvolatile memory card.

MCC has also begun work on an EDA tool called the Multichip Systems Design Advisor. This project is based upon Valid's Allegro-MCM design package. Other participants in this project include Apple Computer, Tandem, Hewlett-Packard, Harris, and Raychem's Advanced Packaging Systems. These compa-

nies will receive training from Valid and early copies of product enhancements in exchange for their involvement in this project. Companies not connected with MCC will be able to purchase this design system at the conclusion of this 2-year project.

So, although the current environment for MCM design may appear almost chaotic, pieces of the infrastructure are gradually falling into place. Although the development pace may not be as fast as your design team might desire, the elapse of the next two or three years may allow the market to prepare applications that will take advantage of the increased performance that low-cost MCMs will provide. **EDN**

## Acknowledgments

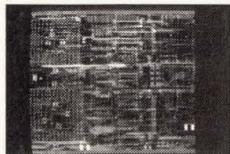
Special thanks to Professor Earl Swartzlander of the University of Texas and to John D Shea, editor-in-chief of the Multi-Chip Technology Newsletter, for their industry insights and observations. You can obtain a sample issue of the Multi-Chip Technology Newsletter by contacting the Shea Technology Group at (408) 378-4800 or via FAX at (408) 370-3155. Additional thanks to Cynthia Williams of MCC for her assistance in obtaining technical materials for this article.

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1. Burgess, Lisa, "Are Multichip Modules the GaAs of the 1990s?" *Military & Aerospace Electronics*, June 1991, pg 17.
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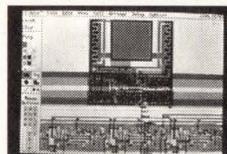
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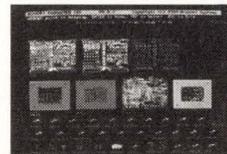
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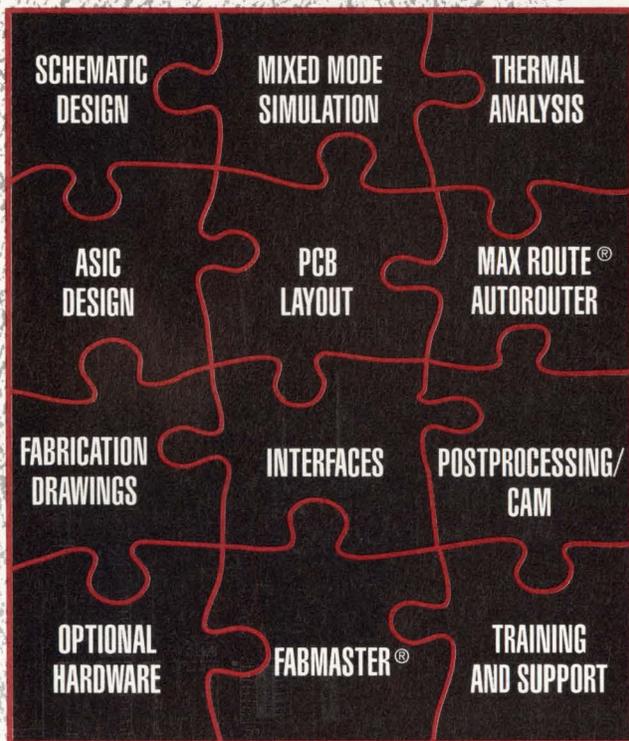
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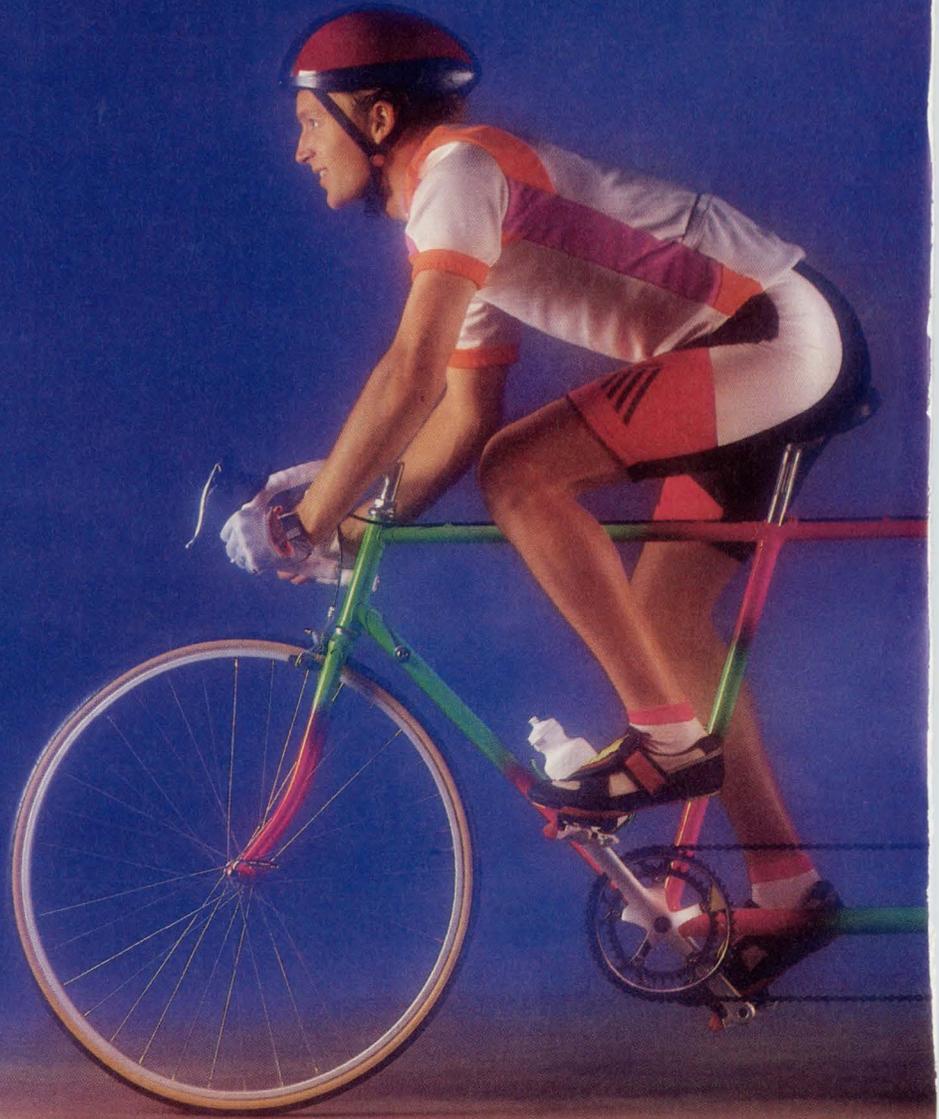
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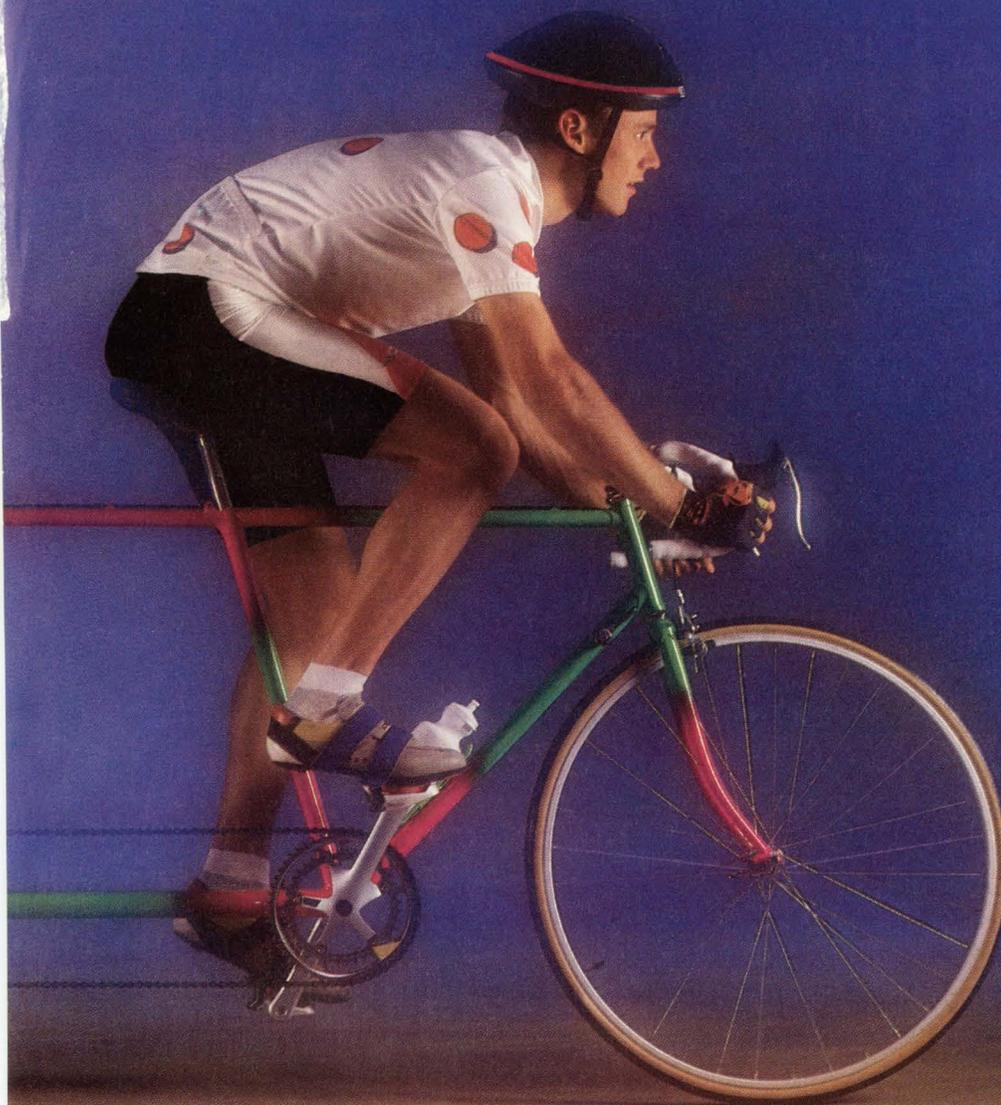


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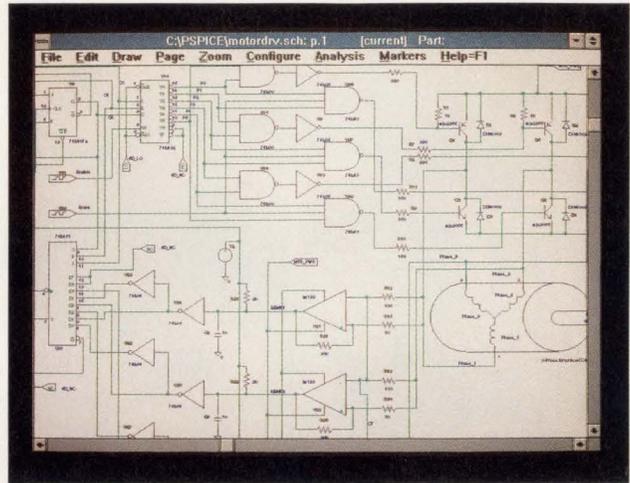
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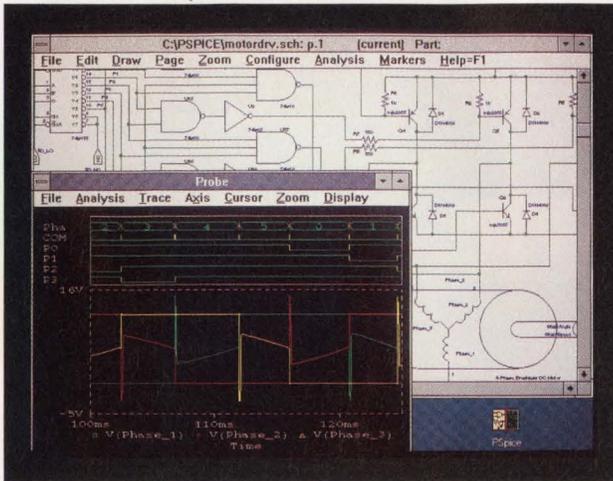
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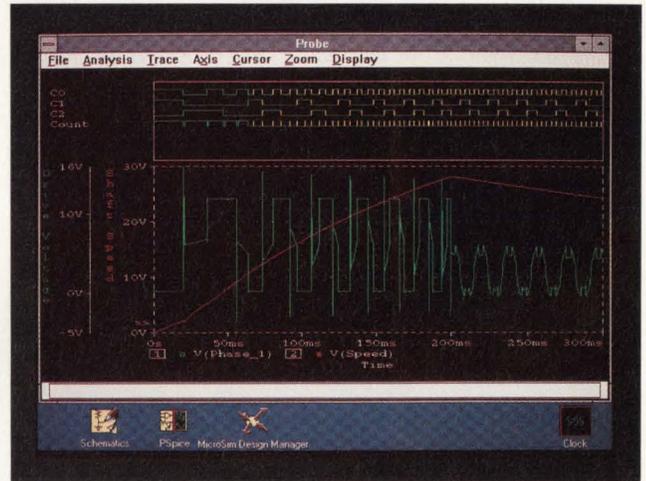
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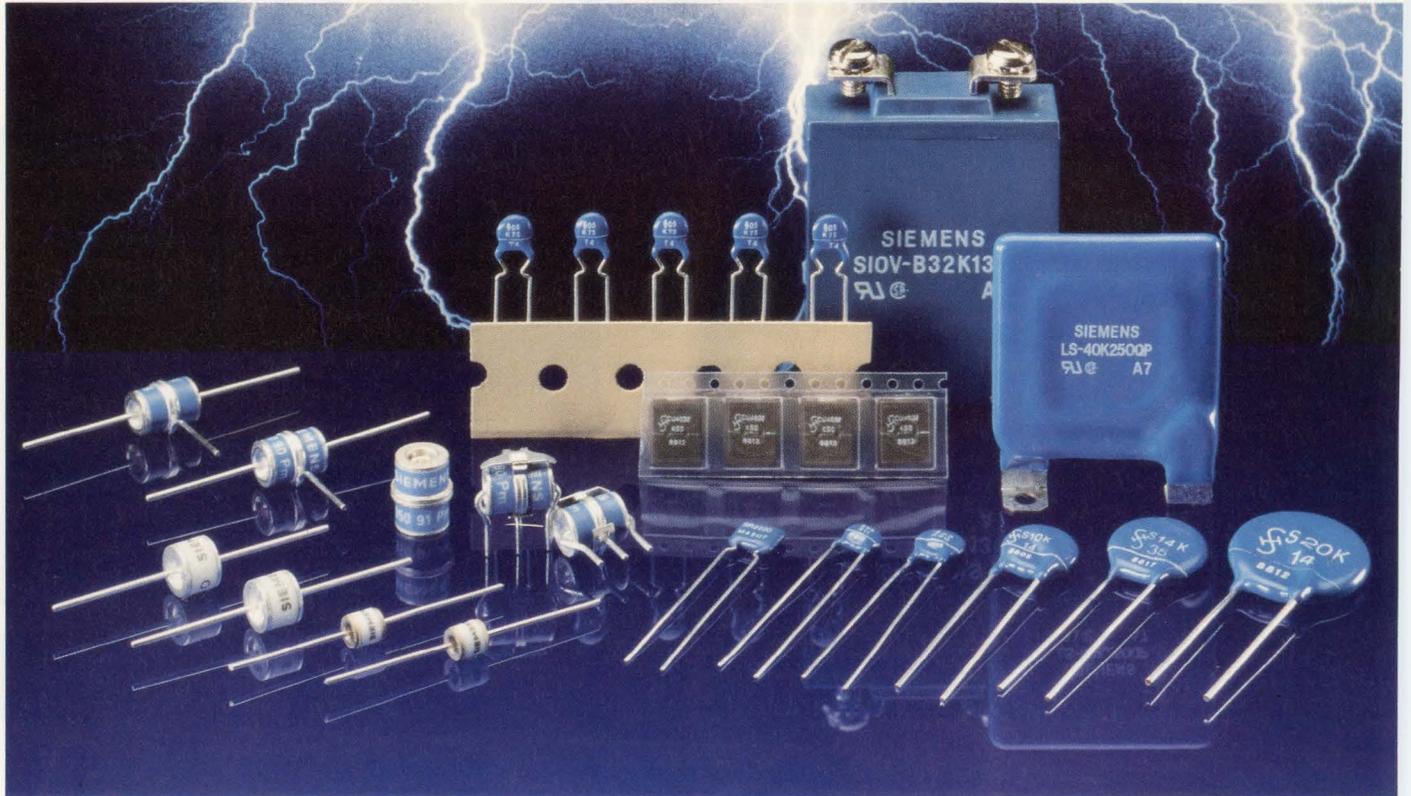


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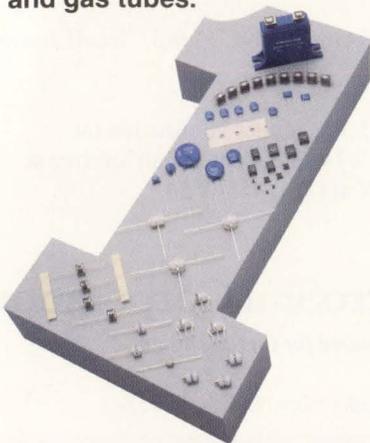
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## HIGH-SPEED MONOLITHIC OP AMPS

# Low-cost op amps break speed barriers

Today's \$3 monolithic op amps can outdo their \$50 hybrid cousins and contend for many discrete closed-loop designs.

*Anne Watson Swager,  
Technical Editor*

**H**igh-speed op amps are fast approaching commodity status as prices plummet. But don't confuse the word "commodity" with "ordinary." These low-cost devices offer unprecedented levels of monolithic-device performance. New fabrication processes and newly applied current-feedback design methods are resulting in myriad high-frequency devices that match or surpass their hybrid counterparts for a fraction of the cost. These op amps also let you apply closed-loop design techniques at frequencies that were previously impossible.

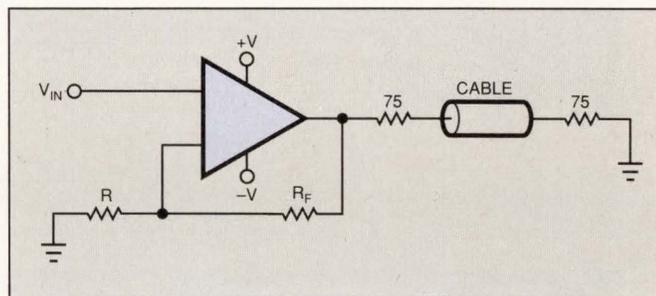
But remember that no single op amp can do it all, and these high-speed devices are no exception. High-voltage vs low-voltage process tradeoffs and ac-vs-dc performance tradeoffs will always exist. Longstanding compromises still apply; stability comes at the expense of bandwidth. Capacitive loads won't cause many of these op amps to oscillate, but that stability comes at the expense of speed.

And unlike slower amplifiers, high-speed amplifiers have "personality," as Barry Harvey, a designer at Elantec Inc, puts it. High-speed op amps can behave differently under different conditions and can be quite unpredictable. Manufacturers are attempting to strip these devices of their personality and make them easier to use and more forgiving of their environments.

But no high-speed design will ever be

free from its high-strung temperament. As tempting as it is to design in an op amp from data-sheet numbers alone, a data sheet simply can't reflect these high-speed devices' performance subtleties. Bench-level evaluation is the only way to ensure that an op amp fits your design requirements.

Because of the compromises op-amp designers are forced to make, few of these new amplifiers fit the description "general purpose." Certain op amps are better performers in certain categories



*The simplest-looking circuits can demand the highest amplifier performance. Driving cable at video speeds is one such application that new high-speed op amps can accomplish with textbook circuits.*

than in others. Even the same op amp can work well at a certain set of supply voltages but more poorly than comparable op amps at other voltages.

**Table 1** shows a sampling of the newer low-cost, high-speed devices, but this list can't come close to showing the breadth of the portfolio offered by many of these high-speed op-amp suppliers. Many vendors offer so many high-speed devices that their selection guides categorize the op amps using some secondary characteristic. Such characteristics include accurate settling, low power,

*Text continued on pg 56*

Table 1—Representative high-speed, low-cost monolithic op amps

Company	Part number	Description	-3-dB bandwidth at gain (MHz at V/V)	Slew rate (V/ $\mu$ sec typ)	Settling time to % accuracy (nsec)	Differential gain, differential phase
Analog Devices Inc	AD811	Current feedback	140 at 1	2500 (20V out)	50 to 0.1% (10V step, gain = -1) 65 to 0.01%	0.01% 0.01°
	AD829	Voltage feedback, externally compensated	50 at 1 120 at -1 (with compensation)	230 (1-k $\Omega$ load)	90 to 0.1% (10V step, gain = -19)	0.02% 0.04°
	AD845	FET input, voltage feedback	16 at 1	100	310 to 0.01%	N/S
	AD847	Low power, voltage feedback	50 at 1	300	120 to 0.1%	0.1% 0.1°
Burr-Brown Corp	OPA621	Low distortion, voltage feedback	500 at 2	500 (2V step, gain = -2)	15 to 0.1%, 25 to 0.01% (2V step, gain = -2)	0.05% 0.05°
	OPA603	Current feedback	100 at 1	1000 (10V step, gain = 2)	50 to 0.1%	0.03% 0.02°
Comlinear Corp	CLC406	Low power, current feedback	160 at 6	1500	12 to 0.05%	0.02% 0.02°
	CLC430	Current feedback	45 at 2	2000	40 to 0.1%	0.05% 0.05°
Elantec Inc	EL2044	Low power, voltage feedback	60 at 1 and 2, 120 at -1	325	80 to 0.1% (10V step, gain = 1)	0.04% 0.15°
	EL2073	Precision, voltage feedback	200 at -1	250	13 to 0.1% (2V step)	0.01% 0.015°
	EL2120	Current feedback	100 at $\pm 1$ to $\pm 10$	750	50 to 0.25% (10V step, gain = 1)	0.01% 0.01°
Harris Semiconductor	HA-2481/-2842	Low power, voltage feedback	54 at 1/ 40 at 2	250/375	90/100 to 0.1% (10V step)	0.03% 0.03°
	HA-5020	Current feedback	100 at 1	800 (20V step)	100 to 0.25% (gain = +1)	0.02% 0.03°
	HFA 1100 series	Very fast, current feedback	850 at 1	2500 (5V out, gain = 2)	11 to 0.1% (2V step)	N/S
Linear Technology Corp	LT1191	Low voltage, voltage feedback	90 at +1	450 (1-k $\Omega$ load, gain = -1)	100 to 0.1% (3V step)	0.2% 0.03°
	LT1220	Precision, voltage feedback	45 at 1	250 (gain = -2)	90 to 0.1% (10V step)	1.7% 2.9°
	LT1223	Current feedback	100 at 1	1000	75 to 0.1% (10V step)	0.02% 0.12°
Maxim Integrated Products	MAX404	Voltage feedback	66 at 2	500 (3V step)	70 to 0.1% (gain = -1, 3V step)	0.05% 0.01°
	MAX457	Voltage feedback, dual video distribution amplifier	70 at 1	300	50 to 1%	0.5% 0.2°
National Semiconductor Corp	LM6181	High output drive, current feedback	100 at 1	2000	50 to 0.1%	0.5% 0.4°
	LM6362	Low power, voltage feedback	50 at 2	300	100 to 0.1 (gain = -1, 2-k $\Omega$ load)	0.1% 0.1°
Texas Instruments Inc	TLE2037	Decompensated, voltage feedback	16 at 5	7.5	N/S	N/S

Notes: Unless otherwise stated, specifications apply to the op amp's highest operating supply voltage.

All op amps available in 8-pin DIPs and SO packages except for the AD811, OPA603, and LM6181 whose SO packages have 16 pins.

All op amps are unity-gain stable with the following exceptions: AD829, OPA621, HA-2842, MAX404, LM6362, and TLE2937.

Test conditions are included when clearly stated on the data sheet.

N/S=not specified; TBD=to be determined.

Input offset voltage		Input bias current ( $\mu$ A) at 25°C	Output		Input voltage noise (nV/ $\sqrt$ Hz)	Quiescent current (mA) at 25°C	Power-supply voltage(s)	Price (100)
at 25°C (mV)	Drift ( $\mu$ A/°C)		Voltage	Current (mA)				
3 max	5 typ	- Input: 5 max + input: 10 max	$\pm 2.8$ or $\pm 12$ V	100 typ	1.9 (f = 1 kHz)	18 max	$\pm 5$ to $\pm 15$ V	\$3.35
1 max	0.3 typ	3.3 typ, 7 max	$\pm 3.6$ or $\pm 12.2$ V (500 $\Omega$ load)	20 min	2 (f = 1 kHz)	6.8 max	$\pm 5$ to $\pm 15$ V	\$2.95
0.25 max	5 max	0.001 max	$\pm 12.5$ V (500 $\Omega$ load)	25 min	18 (f = 10 kHz)	10 typ	$\pm 4.75$ to $\pm 18$ V	\$3.25
1 max	15 typ	6.6 max	$\pm 3$ to $\pm 10$ V min (500 $\Omega$ load)	N/S	15 (f = 10 kHz)	6.3 max	$\pm 4.5$ to $\pm 18$ V	\$2.95
1 max	12 typ	18 typ	$\pm 2.5$ V (50 $\Omega$ load)	N/S	3.3 typ (f = 10 kHz)	28 max	$\pm 5$ V	\$9.95
5 max	8 typ	- Input: 25 max + input: 5 max	$\pm 10$ V min (150 $\Omega$ load)	150 peak	N/S	25 max	$\pm 5$ to $\pm 15$ V	\$4.95
2 typ	30 typ	+ Input: 5 typ - input: 3 typ	+ 3.1 to - 2.7 V	70	TBD	5	$\pm 5$ V	\$5.35
2 typ	TBD	+ Input: 3 typ - input: 3 typ	$\pm 13$ V	85	3 typ (equivalent input noise)	11	$\pm 15$ V	\$2.99
7 max	10 typ	2.8 typ, 7.5 max	$\pm 3.2$ to $\pm 13.6$ V	50 min	15 typ (f = 10 kHz)	5.2 typ, 7.6 max	$\pm 2$ to $\pm 18$ V, 2.5 to 36 V	\$1.80
0.2 typ, 1.5 max	8 typ	2 typ, 6 max	2.5 to 4 V	50 min	2.3 typ (f > 1 MHz)	21 typ, 25 max	$\pm 5$ V	\$7.95
2 typ 25 max	20 typ	+ Input: 5 typ, 15 max - input: 10 typ, 40 max	3.5 V ( $\pm 5$ V)	60 min	N/S	17 typ, 20 max	$\pm 5$ to $\pm 15$ V, 5V only	\$2.80
1 typ 2/3 max	14/13	5 typ, 10 max	$\pm 10.5/11$ V	15/100	16 (f = 1 kHz)	11 max/ 15 max	$\pm 15$ V	\$3.75/ \$4.00
2 typ 8 max	2 typ	+ Input: 3 typ, 8 max - input: 12 typ, 20 max	12 V min	30 min	4.5	10 max 7.5 typ	$\pm 5$ to $\pm 15$ V	\$2.85
2 typ, 6 max	10 typ	+ Input: 25 typ, 35 max - input: 12 typ, 40 max	$\pm 2.8$ V min	60 typ, 40 min	4 typ (f = 10 kHz)	21 typ, 24 max	$\pm 5$ V	\$9.95
1 typ	N/S	$\pm 0.5$ typ	$\pm 4$ to 7 V, 0.25 to 3.8 V	50	25 typ (f = 10 kHz)	30 typ	$\pm 5$ to $\pm 8$ V, 5V only	\$2.40
0.5 typ, 1 max	20 typ	0.1 typ, 0.4 max	13 V	40 typ	17 typ (f = 10 kHz)	8 typ, 11 max	- 15 V	\$3.85
1 typ, 3 max	N/S	1 typ, 3 max	12 V	50 min	3.3 typ (f = 1 kHz)	6 typ, 10 max	$\pm 5$ to $\pm 15$ V	\$2.85
1 typ, 8 max	20 typ	3 max	$\pm 3$ V	50	N/S	35 max	$\pm 5$ V	\$2.98
5 max	20 typ	0.001 max	$\pm 2.5$ V	15	N/S	42 max	$\pm 5$ V	\$5.00
2 typ	5 typ	+ Input: 0.5 typ - input: 2 typ	12 V (100 $\Omega$ load)	100 min	TBD	10 max	$\pm 5$ to $\pm 15$ V	\$2.95
3 typ, 13 max	7 typ	2.2 typ, 4 max	- 13.4 to 14.2 V	25 min	10 (f = 10 kHz)	5 typ	4.75 to 32 V	\$1.91
0.02 typ, 0.1 max	0.4 typ, 1 max	0.015 typ, 0.09 max	- 13 to 12.9 V	N/S	3.3 typ (f = 10 kHz)	3.8 typ, 5.3 max	$\pm 5$ to $\pm 15$ V	\$1.42

# TECHNOLOGY UPDATE

## High-speed monolithic op amps

low offset voltage and drift, low input bias current, low noise, low distortion, and high output current.

### Process technology is one key

Process-technology improvements have as much to do with these amplifiers' performance as do innovative IC design techniques. Making the connection between process technology and amplifier performance doesn't require a PhD in device physics, just a basic understanding of process implications. Lower-voltage processes lead to higher speed; higher-voltage processes lead to higher precision. Complementary processes, which result in independent and ideally well matched npn and pnp transistors, also lead to higher speed and lower quiescent power dissipation.

Complementary processes have had the greatest effect on amplifier performance. These processes lead to npn and pnp transistors with similar switching speeds, although the npn devices are still somewhat faster. Using complementary processes, designers can produce symmetrical circuits that have efficient output stages and can effectively manage the power within the amplifier. Making a device with a complementary process requires more steps than do other processes, which often—but not always—means more expensive wafers and op amps.

Although process technology has a tremendous impact on a device's performance, you shouldn't make general assumptions about an op amp based solely on its process. According to Bill Gross, design manager at Linear Technology, "There is no single appropriate process for all high-speed amplifiers, just as there is no single definition of high speed." Each company uses a variety of processes to achieve amplifiers that have the desired specifications.

Because of process advance-

ments, you also can't generalize individual device cost from overall wafer cost. Wafers produced by complementary processes do cost more, but the resultant op amps will not necessarily cost more.

Harris Semiconductor recently announced a high-speed process that the company will use to build many of its future high-speed products. Although each wafer this process produces costs much more than other wafers, the packing density of each device is much greater (Fig 1). More devices per wafer means lower cost per device. The process lets the company build ultrahigh-speed devices, such as the HFA-1110 family. At \$9.95 (100), the family costs more than many of the other devices in Table 1, but it also offers 850-MHz-bandwidth parts.

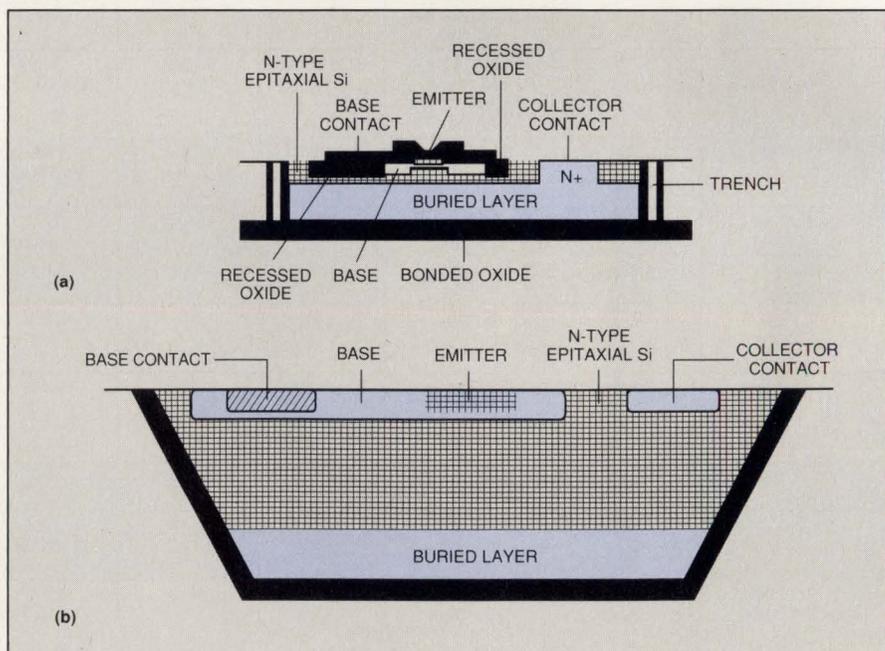
### Second sources disappear

One important impact of companies' having proprietary process technologies is the limitations placed on second sourcing. For

many years, small companies and even larger companies with their own fabrication facilities built and continue to build high-speed op amps using AT&T's high-speed, complementary low-voltage process. Because AT&T's process was open to everyone, many companies built comparable products with the process and used design tricks to enhance the performance of its own op amps. As a result, companies could easily second source a variety of op amps.

Companies will find it more difficult—but not impossible—to second source the newer low-cost, high-speed amplifiers built using proprietary processes. Thus, your relationship with and confidence in your supplier is increasingly important. Also crucial is the design support the manufacturer offers, such as evaluation boards and macro-models.

Almost all the vendors in Table 1 offer macromodels of their op amps, but be forewarned: These

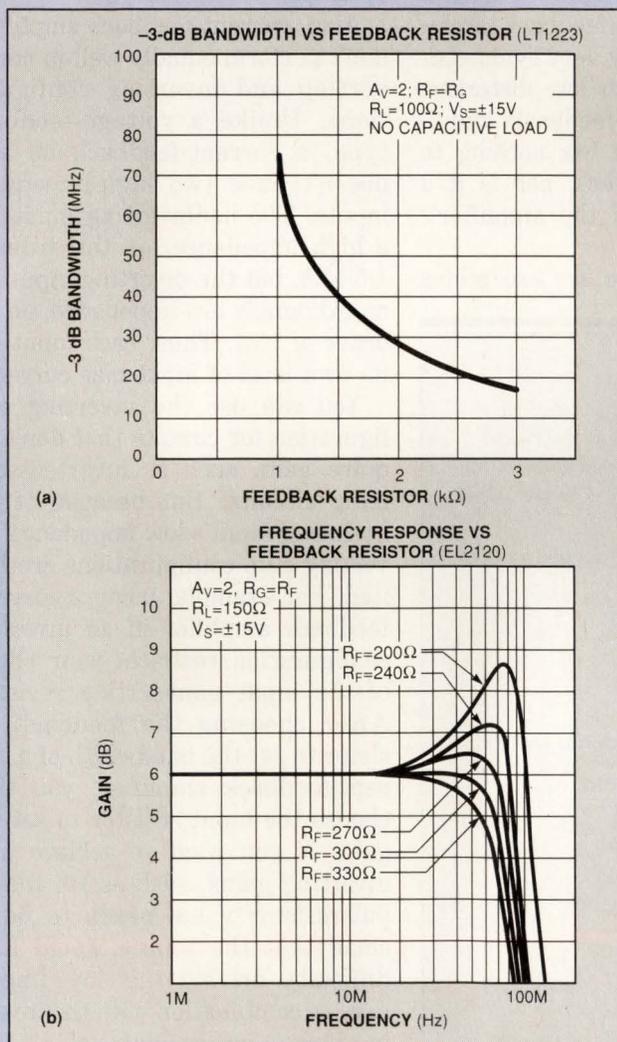


**Fig 1—You can't choose op amps on the basis of process technology alone—you need some appreciation of how the devices achieve their specifications. A high-speed process developed by Harris Semiconductor lets the company build fast op amps using a smaller die (a) than the company's older process (b). The resulting 850-MHz op amps cost \$9.95.**

## Application tips for current-feedback amplifiers

Leaving all theoretical explanations of current-feedback op-amp operation to the experts, following a few simple rules will help you successfully use current-feedback op amps.

First, the most important step in using these amplifiers is choosing the feedback resistor. The value of this resistor affects the bandwidth and peaking of the amplifier's response (Fig A). Either use the value the manufacturer suggests and has most likely specified guaranteed performance for, or select the value according to the graphs supplied in the data sheet. Most of these values will be smaller than 1 k $\Omega$ .

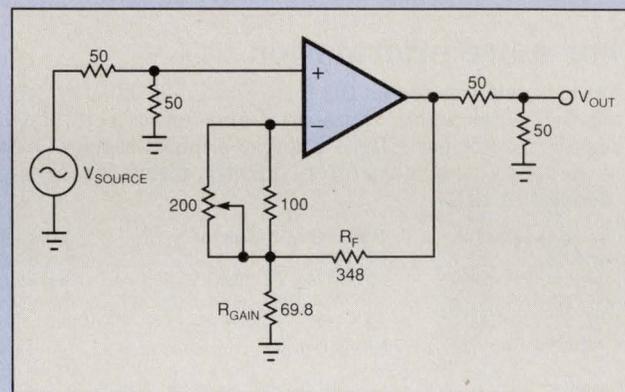


**Fig A—Choosing the exact value** of a current-feedback amplifier's feedback resistor ( $R_F$ ) is crucial. As these graphs from the LT1223 (a) and EL2120 (b) data sheets show, this resistor's value directly affects the peaking and frequency response of the amplifier. ( $A_V$  is voltage gain.)

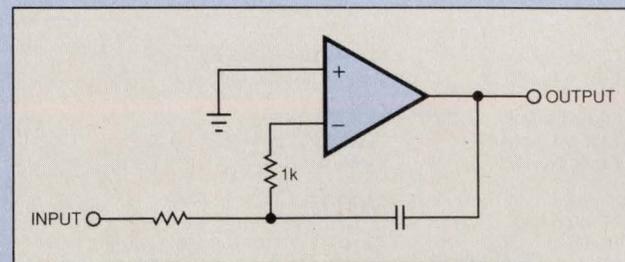
You can adjust the value of the feedback resistor to tailor the op amp's compensation for your particular signal bandwidth—no voltage-feedback amplifier provides similar flexibility. To exercise this flexibility, you must understand current-feedback amplifiers' loop-gain mechanisms, a subject Refs 1 and 2 cover in depth. If you so choose, you can use resistors to fine-tune the frequency response of a current-feedback amplifier. Michael Steffes of Comlinear Corp suggests the circuit in Fig B, which increases the amplifier's loop gain without affecting the signal gain.

Second, choose the input-resistor value to set the op amp's gain. If you're using an inverting configuration, be sure the value isn't so low that it overloads the source.

Finally, a warning: Don't place a capacitor directly from output to input. This integrating topology is common for voltage-feedback amplifiers but will cause most current-feedback amplifiers to oscillate. Instead, form an integrator using a modified topology, such as the one Fig C shows.



**Fig B—This circuit lets you decouple** the feedback resistor from the gain-setting resistor so you can tailor the op amp's frequency response. (Figure courtesy Comlinear Corp)



**Fig C—Most current-feedback op amps won't tolerate** a capacitor placed directly from output to input. This modified configuration is one suggested integrator from Ref 3.

# TECHNOLOGY UPDATE

## High-speed monolithic op amps

macromodels leave out almost as many effects as they include. Elantec clearly states its models' shortcomings on the data sheet. The models approximate frequency response and small signal transients, but not the effects of load capacitance, noise, or slew-rate limitations. You can't rely on macromodels to reveal op-amp performance subtleties.

### Current feedback proliferates

In addition to process improvements, current-feedback design techniques have also spurred the high-speed amplifier market. So many current-feedback amplifiers exist today that almost half of the op amps in **Table 1** are current-feedback types. You'll find some good explanations of the current-feedback architecture in **Refs 1** and **2** as well as in many companies' ap-

plication literature. Because of the basic architectural differences between current-feedback amplifiers and voltage-feedback types, following a few key points is crucial to applying them correctly (see **box**, "Application tips for current-feedback amplifiers").

Current-feedback amplifiers have two basic virtues: Unlike voltage-feedback amplifiers, they don't require huge gain-vs-bandwidth tradeoffs, and their freedom from slew-rate limiting makes them inherently linear at high frequencies. Also, the current-feedback architecture is generally very symmetrical, which leads to low distortion levels. A current-feedback amplifier's ac distortion has nothing to do with its dc specs, nor is it a strong function of the amplifier's bandwidth.

As always, there are exceptions

to every rule. In reality, the bandwidth of a current-feedback amplifier still varies somewhat with gain. This variation is primarily due to the op amp's low inverting input resistance. Also, some of these amplifiers still have slew-rate limitations that can affect their linearity. The higher the power-supply current—15 mA seems to be optimal—the better chance a current-feedback amplifier has to be linear. This 15-mA supply current compromises the low distortion of dual and quad op amps.

Also, current-feedback amplifiers don't perform equally well in noninverting and inverting configurations. Unlike a voltage-feedback type, a current-feedback op amp doesn't have two high-impedance inputs. The noninverting input has a high impedance, on the order of 1.5 M $\Omega$ , but the inverting input has an extremely low impedance, on the order of 15 $\Omega$ . Thus, each input has its own level of input bias current.

You can use the inverting configuration for circuits that don't require gain, such as inverted-summing circuits. But because of the inverting input's low impedance, inverting-gain configurations are limited. For example, using a current-feedback amplifier in an inverting configuration restricts your choice of the input gain-setting resistor. After choosing the feedback resistor to set the bandwidth of a current-feedback amplifier, you then choose the input resistor to set the gain. If you want to achieve high inverting gains, such as 10, the input-resistor value needs to be so small that the source would have difficulty driving this low impedance in combination with the inverting input's low impedance.

Even more vexing than the drive problem is the problem of running high-frequency signals through a length of wire or trace—which has inductance—and into the inverting

## For more information . . .

For more information on the high-speed monolithic op amps discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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# TECHNOLOGY UPDATE

## High-speed monolithic op amps

node. The combination of the inductance and low resistance limits the op amp's frequency response long before any loading effects occur.

Noninverting configurations place no such constraints on the input resistor of current-feedback op amps because of the noninverting input's high impedance. Even in positive-gain configurations, current-feedback op amps do best with moderate gains of 10 to 20, but not as high as 50. However, don't overlook other data-sheet exceptions for noninverting-configuration operation limits. Despite claims to the contrary, some current-feedback op amps do suffer from input slew-rate limits. These limitations prevent their practical use in certain

positive-gain configurations (Fig 2).

Common-mode rejection, noise, and accurate settling are not a current-feedback op amp's strong points. The current-feedback device has no differential input stage to cancel out common-mode effects. Its input voltage noise is fairly low; however, current noise on the inverting input is multiplied by the feedback resistor to produce output noise.

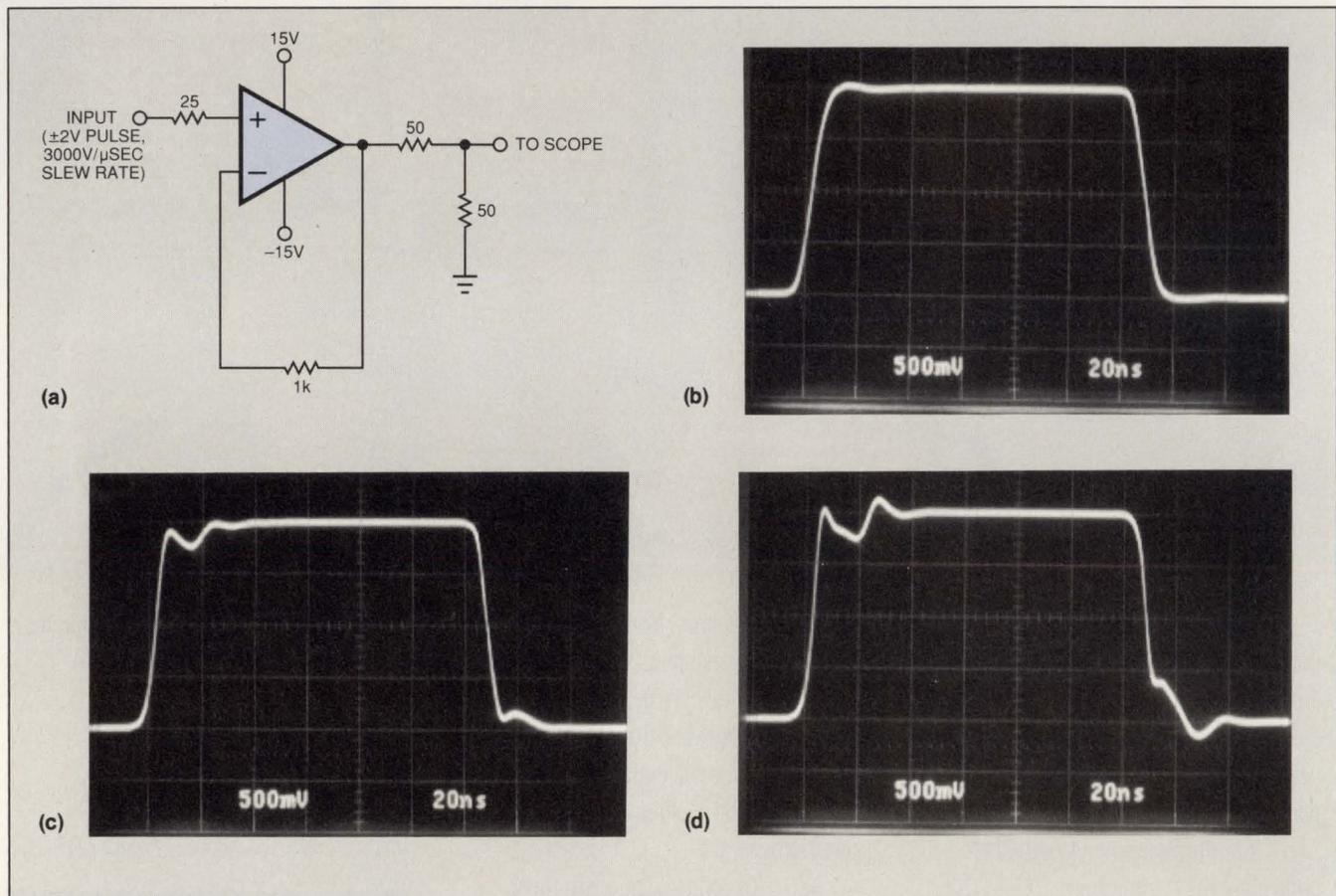
For example, the EL2120 has an input noise voltage of  $4 \text{ nV}/\sqrt{\text{Hz}}$ , but its noise current is  $20 \text{ pA}/\sqrt{\text{Hz}}$ . If this amplifier uses a  $1\text{-k}\Omega$  feedback resistor, the current noise would be  $20 \text{ nV}/\sqrt{\text{Hz}}$ , which would totally overwhelm the noise voltage. The good news is that the current noise decreases as the gain in-

creases. Manufacturers usually recommend feedback-resistor values much lower than  $1 \text{ k}\Omega$ ; for example,  $330\Omega$  for the EL2120.

Finally, although current-feedback op amps tend to have high slew rates, they also have long thermal settling tails. Thus, these amplifiers can settle very quickly to accuracies of 0.1%, but take much longer to settle to higher accuracies. This feature alone takes current-feedback op amps out of the running for instrumentation applications.

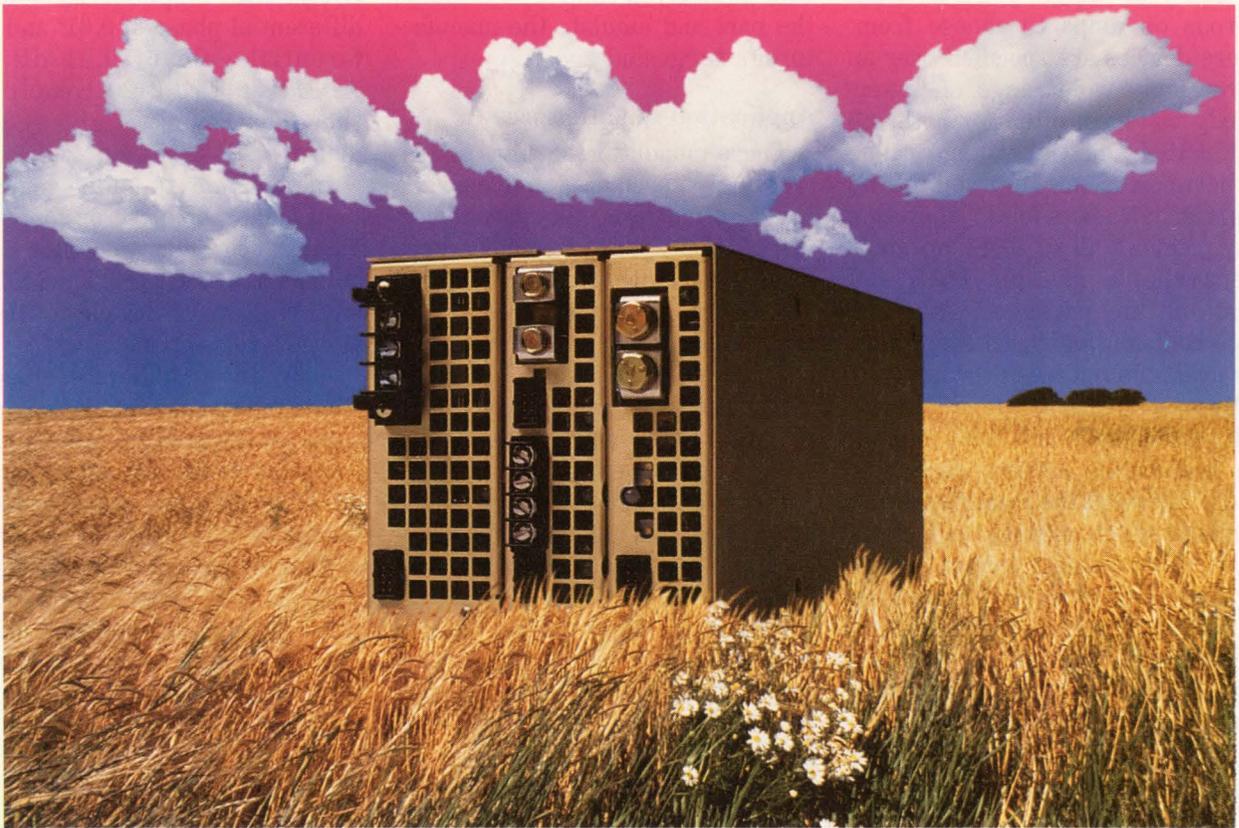
### Find the one you want

Once you focus on a few important specs and decide whether voltage- or current-feedback types bet-



**Fig 2—No two current-feedback amplifiers are alike, although they are all architecturally similar. For example, three of these amplifiers operating under the same slew-limited conditions exhibit three very different responses to a  $4V_{F.P.}$  high-speed pulse (a). The amplifier in b is well behaved, but those in c and d reveal distortion that is most likely the result of input slew-rate limitations. (Photos courtesy Elantec Inc)**

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# TECHNOLOGY UPDATE

## High-speed monolithic op amps

ter suit your design, you'll have numerous op amps to choose from. These devices are specified over an increasingly wide range of power-supply voltages, often for both  $\pm 5$  and  $\pm 15$ V and any voltage range in between. Some low-voltage op amps include specs for 5V operation only. Almost all of these op amps are available in 8-pin DIPs and small-outline packages. Most op amps come in single packages; duals are available but less prevalent.

Most all of these amplifiers are unity-gain stable, and many are stable even while driving capacitive loads. Although the amplifiers don't oscillate when driving capacitive loads, that stability comes at the expense of bandwidth (Fig 3). You should interpret the words "can drive capacitive loads" on the data sheet as "the amplifier slows down and adjusts to the load automatically." Thus, to keep the op amp running at its maximum bandwidth, you still need to keep the load capacitance as low as possible.

Keep in mind that these op amps demand the same respect as any high-speed component. All high-speed designs require extremely careful layout and power-supply decoupling. For this reason, most manufacturers provide evaluation

boards that you can use to evaluate the part and emulate the manufacturer's suggested layout.

### Application-specific specs

These monolithic op amps are increasingly specialized and specified for applications like broadcast video, HDTV, and communications. Even bandwidth is being specified with more detail than ever before. Instead of providing information on only the  $-3$ -dB bandwidth of devices, manufacturers specify gain flatness. For example, the AD811 features gain flatness to within 0.1 dB at frequencies as high as 35 MHz. The HFA1100 has a gain flatness of 0.04 dB to 50 MHz and 0.14 dB to 100 MHz.

Almost all these devices include specs for differential gain and phase, the classic measure of distortion for composite video systems. Because the amplitude and phase of a composite signal carry color information, modulating these quantities will cause color distortion. And because video systems often have chains of amplifiers, those amplifiers' specs must be that much tighter than the overall system spec.

For systems with 10 amplifiers and goals of  $0.1^\circ$  and 0.1 dB for differential phase and gain, respec-

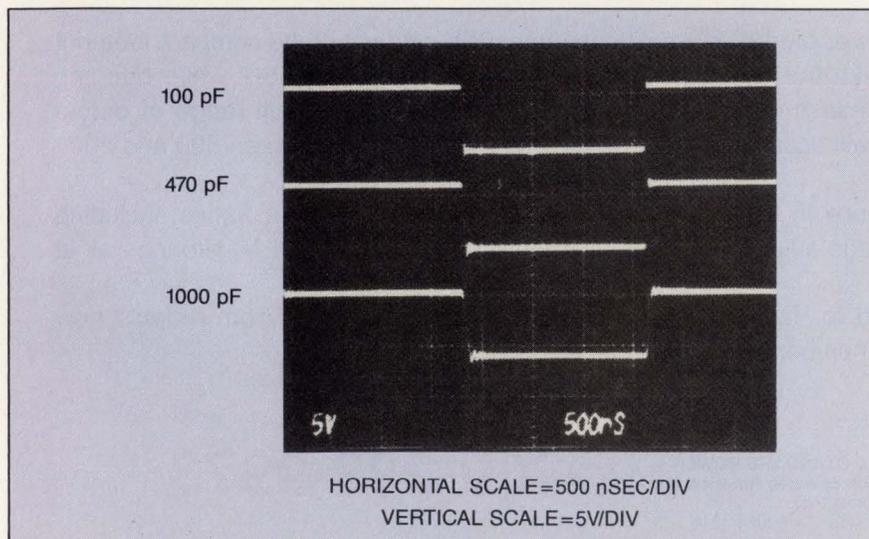
tively, each amplifier must have a differential phase of  $0.01^\circ$  and a differential gain of 0.01 dB. The AD811 and EL2120 comply with these extremely tight requirements.

In addition to video specifications, many of these op amps have video-specific features such as disable pins. The CLC430 and EL2120 have high-speed disables of 100 and 50 nsec, respectively.

As these amplifiers encroach on RF territory, communications specs, such as third-order intercept, are becoming more and more common on data sheets. Third-order intercept is a measure of the change of third-order intermodulation components. The third-order intercept point is the intersection of two plots: output vs power and output third-order intermodulation-distortion components vs input.

### Scrutinize data sheets

Despite evolving data sheets, some things never change. Manufacturers can't resist skewing specs to their advantage. The difference between bandwidth and gain-bandwidth product is especially murky for high-speed voltage-feedback amplifiers. For low-frequency amplifiers, you can safely assume that



**Fig 3—Stable operation while driving a capacitive load** is a characteristic more and more high-speed amplifiers, such as the MAX404, share. However, as the capacitance increases, the amplifier must slow down to remain stable. Note the slowest response on the bottom trace. (Photo courtesy Maxim Integrated Products)

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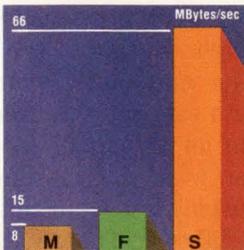


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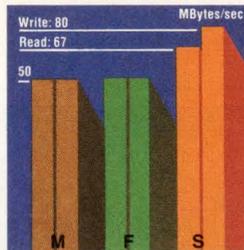
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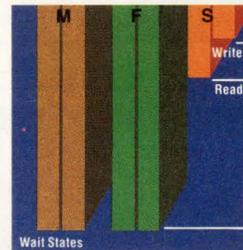


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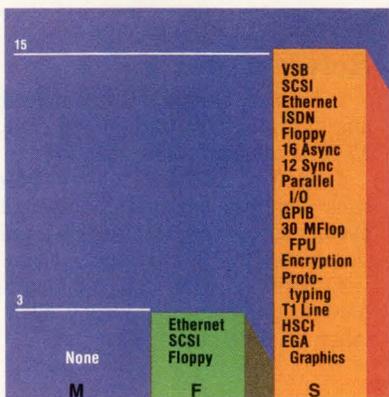
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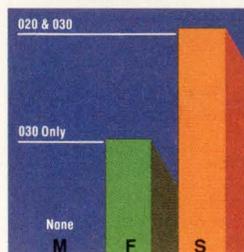


**DRAM Random Accesses**  
Non-burst '040 performance is measured in wait states. Fewer wait states mean higher performance. The SV430 is not only 66% faster than Force or Motorola, it supports twice the on-board memory—32 MB.



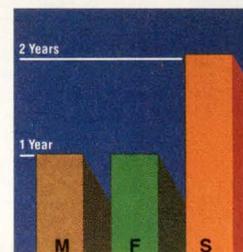
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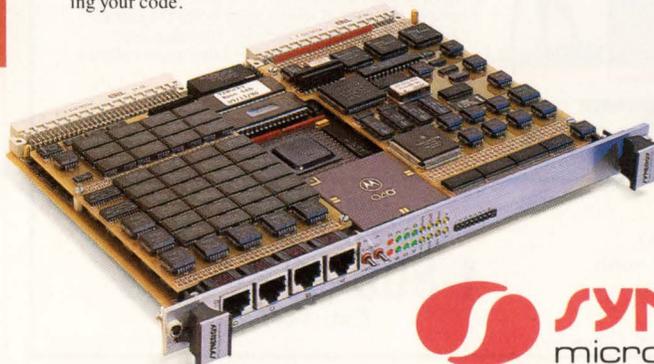


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'030 SBCs. Force offers compatibility only from the '030 level, and Motorola offers "upward migration"—a polite phrase that means rewriting your code.



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Synergy backs the reliability of its SBCs with a two year standard warranty. Force and Motorola only offer you one.



Data from Motorola MVME165 data sheet dated 2/90, and Force CPU-40 data sheet A1 Rev. 1. DRAM measurements shown are with parity. VMEbus transfers are to a 60ns slave.

VME64 is a trademark of Performance Technologies, Inc.

# UPDATE

## High-speed monolithic op amps

most unity-gain amplifiers are stable. Therefore, a gain-bandwidth product of 1 MHz implies that at a gain of 1, the bandwidth is 1 MHz.

This assumption doesn't hold true for high-frequency op amps. It's imperative to judge a voltage-feedback amplifier by both its gain-bandwidth specification and its minimum closed-loop gain. Because the gain-bandwidth product is confusing and not applicable to current-feedback amplifiers, **Table 1** shows the -3-dB bandwidth at some usable level of gain. For voltage-feedback types, don't forget that the bandwidth will be even lower for higher gains.

The low cost and wide availability of high-speed monolithic op amps lets you design circuits and systems whose costs were previously prohibitively high. But often the simplest-looking and most common-place circuits can put the greatest demands on an amplifier. A video cable driver is a classic example. Driving 150Ω loads is a difficult job, but the amplifiers in **Table 1** accomplish it using textbook circuits.

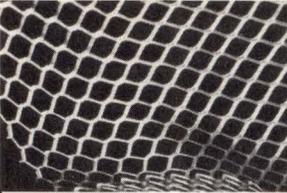
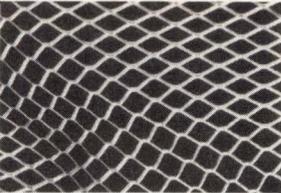
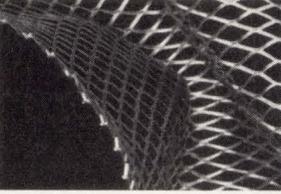
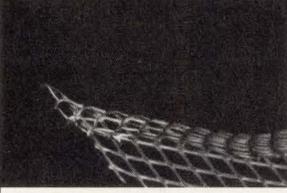
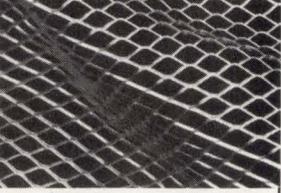
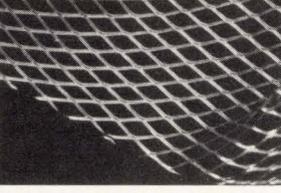
**EDN**

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2. Steffes, Michael, "Current-feedback amplifier loop gain analysis and performance enhancements," Application Note OA-13, Comlinear Corp.
3. Williams, Jim, "High-speed amplifiers in application circuits," *EDN*, October 24, 1991, pg 157.

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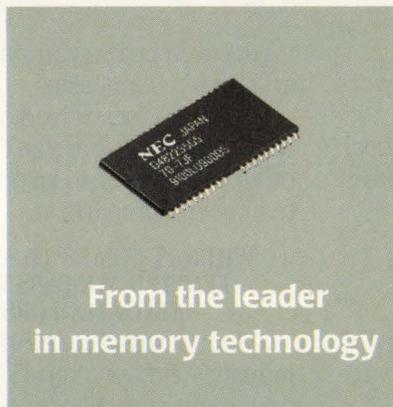
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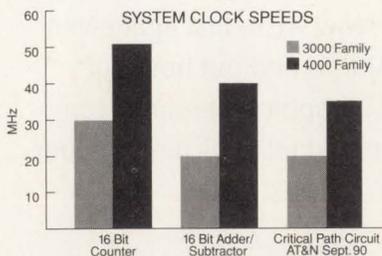
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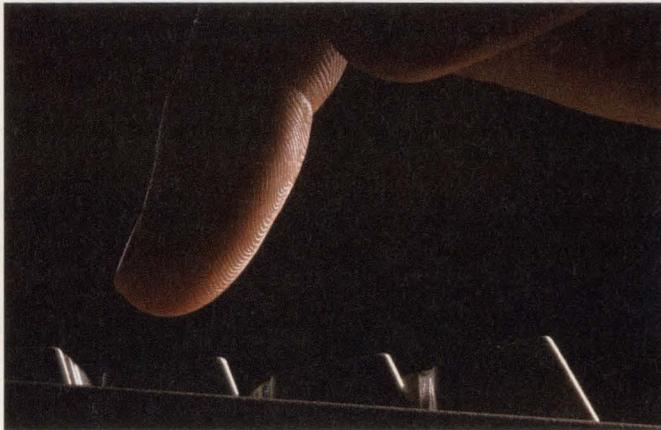


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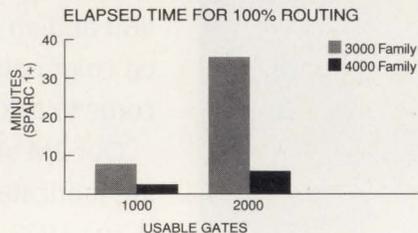
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# PRODUCT UPDATE

## Synchronous cache RAMs run at 50 MHz

The CY7B173 and CY7B174 synchronous cache RAMs operate at 50 MHz, but they offer more than just high speed. To simplify cache-memory subsystem design, the devices incorporate logic functions such as address latches and burst counters.

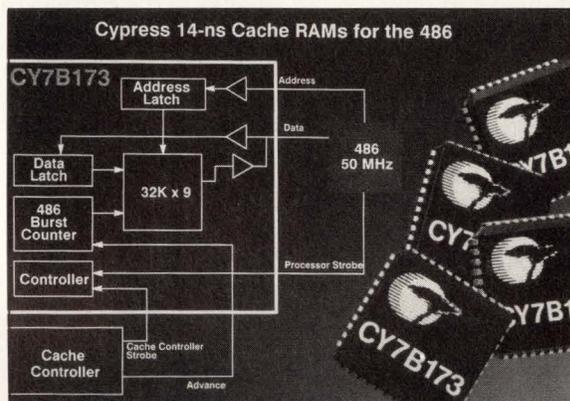
Both memories are organized as 32k x 9 bits. They operate synchronously, sampling the address, data, and control lines on the rising edge of the clock input signal. The clock's minimum cycle time is 20 nsec, allowing operation at 50 MHz. Only the output-enable line operates asynchronously, setting the data output lines to high impedance within 7 nsec of de-assertion.

For the memories to respond to a given clock cycle, both the chip select and address-strobe lines must be properly asserted. The devices have two complementary chip select lines, allowing you to use two banks of memory in your system without external decoding logic. The devices also have two address strobe lines: one for the system processor and one for the cache controller. Having two address strobe lines eliminates the need for external logic in systems with processors that don't relinquish control in the event of a cache miss.

Both address strobe lines have the same effect during a read operation. The data output becomes valid within 14 nsec of the rising clock edge. For write operations, however, the address strobes have different results. The controller's address strobe causes a write opera-

tion to complete in a single clock cycle. The processor's address strobe, however, causes the memory to delay one clock cycle before completing the write operation. This delay lets cache-tag RAM or other logic time identify a cache miss and prevent the write operation if necessary. If both address strobes are active, the processor address strobe takes precedence.

The memories support burst access for read and write operations by supplying an address latch and a built-in burst counter. The



*Running as fast as 50 MHz, the CY7B173 and CY7B174 cache RAMs also speed system design. The devices include data latches, burst counters, and other design-simplifying logic on chip.*

CY7B173 has a counter that follows the burst sequence of the Intel 80486 processor. The CY7B174 offers a linear counter. You can use the burst mode with either the processor or the controller address strobes.

The devices operate at 5V and consume 250 mA. They come in 44-pin PLCC (plastic-leaded-chip-carrier) packages and cost \$69 (100).

—Richard A Quinnell

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CIRCLE NO. 32

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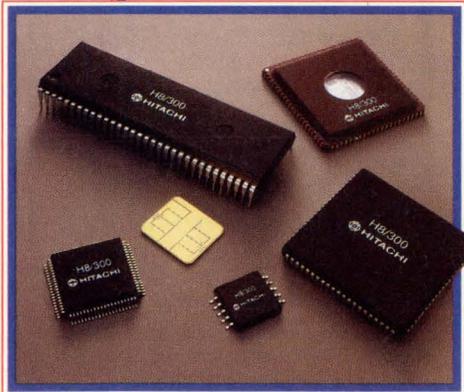
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ROM/RAM/EEPROM	10K/256/8K	8K/256/0	16K/512/0	24K/1K/0	32K/1K/0	16K/512/0	32K/512/0
Timers			3			5	10
Serial Channel			2			1	2
A/D Converter						8-Bit, 8 Channel	8-Bit, 16 Channel
Interrupts			4 External 16 Internal			9 External 19 Internal	9 External 47 Internal
I/O Ports	1-Bit I/O Common		47 I/O 4 Input Only			58 I/O 8 Input Only	50 I/O 16 Input Only
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# HIGH-DENSITY PLDs



The growth in PLD size over the past few years has presented designers with a new problem—no universal yardstick for measuring PLD performance. (Photo courtesy Altera Corp)

---

**T**he lure of programmable logic is inescapable. The technology gives you freedom to change your hardware design up until the last minute, or in some cases, even after it has shipped. The low financial risk and short development times all favor programmable logic devices (PLDs). However, the flexibility of a PLD that works for you in a design works against you when you are trying to nail down just what each product can do.

**The flexibility of high-density PLDs makes them attractive in many applications, but the lack of a universal yardstick for comparison makes it difficult to find the best choice for your application.**

Doug Conner, Technical Editor

High-density PLDs offer several thousand usable logic gates with flexibility and speed adequate for many of the same circuits as masked gate arrays. System clock speeds are generally in the range of 10 to 50 MHz, although some chips are now able to push the maximum speeds even higher for select designs. Often high-density PLDs are defined as those with more than 2000 usable gates—but different manufacturers rate usable gates differently by as much as a factor of three. For this article, high-density PLDs are devices in packages with 40 pins or more (this is an objective standard, even though it is not an accurate measure of logic capacity).

The fast-moving, high-density PLD market and its lack of universal specifications makes a marketers' paradise and an engineers' nightmare. To get a full appreciation of what you are up against, consider the following note for a device-timing specification on combinatorial delay and setup times (the company will remain unnamed):

“These limits are derived from worst-case values for a representative selection of the slowest paths through the [device] logic cell including net delays. Some paths may exhibit longer

## The great flexibility of PLDs that works for you in a design works against you when you are trying to nail down just what each product can do.

delays, although most will be shorter."

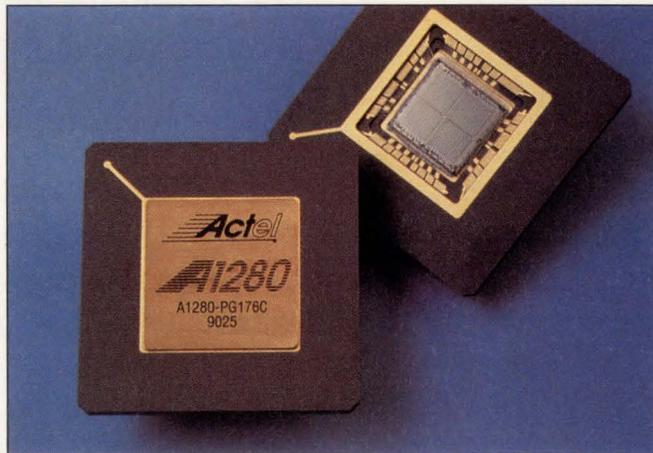
The company wants to give the specification the conservative feel of worst case without living up to the real meaning. The specification should read "typical," which is the only way a designer can safely use it.

Most high-density PLD specifications aren't misleading. But they don't go a long way toward helping you answer two of the three most important questions—will my design fit on the chip and how fast will it run. The third question, how much does it cost, manufacturers can clearly answer.

The best way to choose the optimum high-density PLD would be to try your design on all of them and see how they perform. However, with more than a dozen architectures to choose from and multiple chips within most architectures, the possibility of trying your design on each one isn't practical. The disturbing fact is, you may be unable to choose the optimum PLD architecture for your application.

Help for choosing the right architecture is on the way in two forms, but it may take a while to arrive. The first development that may prove helpful is a set of benchmark circuits that will show the speed and comparative capacity of different high-density PLDs. A total of seven PLD and PLD-tool companies are in the process of founding a nonprofit corporation for developing and regulating the benchmarks. The benchmarks will give users a quantitative measure of how the chips perform when programmed

for various functions, such as counters and accumulators. The percentage of the chip consumed for these functions and the speed at which the device runs will give a far better measure for comparing PLD performance than is currently possible. Expect to hear more on benchmarks as the effort gets underway.



*The need for I/O pins often grows with the logic available on the chip. A large device such as Actel's 1280, rated by the company at 8000 equivalent gates, is available with 176 pins in a pin-grid-array package.*

The other helpful development is in software tools that let you try your design on multiple chips. In December, Neocad released some software tools that let you design independently of a target device. After you've entered your design, the software can automatically generate programming information for the target device you choose. The tools accept inputs from many of the design-entry tools already available and outputs the program data for the PLD. The software should be a step in the right direction, but the initial release only supports Actel and Xilinx products.

Until a better solution comes along, you need to learn what you can about the available devices to make an informed decision, even if

you can't necessarily choose the optimum chip. When you start to narrow your search, there are a few objective specifications that may help (see **Table 1**).

The storage method used on a PLD may not seem critical, but the implications may be important to your application. Storage methods

break down into three main categories: one-time-programmable, erasable, and volatile memory.

One-time-programmable and erasable PLDs usually have a design security bit you can set that makes it difficult for someone to copy your design. Volatile-memory-based devices don't offer security because you always have to load them from some nonvolatile source, either an adjacent PROM or a nonvolatile-memory source connected to a computer that loads the device.

One-time-programmable devices typically offer a long operational lifetime after programming. Some erasable devices only guarantee the programming for 10 to 20 years, depending on storage and operating temperatures or other factors. If extremely long life is important, look for the fine print or ask the chip vendor exactly what the lifetime is.

Erasable PLDs, which let you try again and again until you get your design right, are usually specified for at least 100 write-erase cycles. If developing your design involves many unsuccessful cut and try attempts, you may find it less embarrassing to use an erasable or volatile memory-based device and avoid creating large stacks of useless

## High-Density PLDs

one-time-programmable devices.

The infinite ability to re-program volatile-memory-based PLDs may be a nuisance because you need to load the memory every time power is interrupted. Or, re-programming may be a feature you can't live without.

For example, Quickturn (Mountain View, CA) uses volatile-memory-based chips to emulate ASICs. The company has developed software that converts the internal design of an ASIC into a program for

a system containing a large number of Xilinx 3090 devices. The product wouldn't be possible without infinitely re-programmable devices.

Volatile-memory-based parts might also be an advantage if you want to be able to update a system in the field, either using a new PROM or software updates if the device program is loaded by a computer.

If your circuit needs to operate off battery power, you may be able to narrow your search further. Most

of the chips listed in **Table 1** have a standby current rating higher than 100 mA or lower than 10 mA. Some are lower than 1 mA.

You should note two things about the standby current rating. First, for some devices, standby current is just the rating when no inputs are changing state (usually specified at inputs of supply voltage or ground), and output loads are zero. For other devices, a standby state is a special state and reactions to changing inputs may not be as fast

**Table 1—Representative high-density PLDs**

Manufacturer	Product	Logic cells	Program storage	Program security bit	Standby current, mA (max)	System-wide clocks	Asynchronous clocks	Price (100)	Comments
Actel	1240	684	OTP <sup>1</sup> -antifuse	Yes	0.350	2	Yes	\$150	Alternate source is Texas Instruments.
	1280	1232	OTP-antifuse	Yes	0.350	2	Yes	\$300	
AMD	Mach 110	32	EE <sup>3</sup> -CMOS	Yes	150	2	No	\$9.65	
	Mach 210	64	EE-CMOS	Yes	180	2	No	\$19.31	
Algotronix	CAL 1024	1024	Volatile memory	No	Not available	2	No	£245	
Altera	MAX5064	64	UV-Erasable	Yes	125	1	Yes	\$20	Alternate sources are Cypress and Intel.
	MAX5192	192	UV-Erasable	Yes	360	1	Yes	\$142	
Atmel	ATV2500	48	UV-Erasable	Yes	5	None	Yes	\$17.90	Low-power version (\$20.40).
	ATV5000	76	UV-Erasable	Yes	40	4 (partitioned)	Yes	\$57	Low-power version (\$71.50).
Intel	5AC324	24	UV-Erasable	Yes	0.500	1	Yes	\$20	
National Semiconductor	MAPL144	27	EE-CMOS	Yes	140	1	No	\$34	
Plessey	ERA60100	2500	Volatile memory	No	30 $\mu$ A (typ)	None	Yes	\$34.56	
Plus Logic	H2010	36	UV	Yes	80	3	Yes	\$14	
	FPGA2020	72	UV-Erasable	Yes	220	2	Yes	\$34	
Quicklogic	QL8x12	96	OTP-antifuse	Yes	10	1	No	\$69(1000)	
Signetics	PLHS5501	None	OTP-fuse	Yes	295	None	Yes	\$10.60 (1000)	Folded NAND structure.
	PML2552	None	UV-Erasable	Yes	10	Partial	Yes	\$12.90	Folded NAND structure.
Xilinx	4003	100	Volatile memory	No	Not available	8	Yes	\$110	Alternate source is AT&T.
	4005	196	Volatile memory	No	Not available	8	Yes	\$292	

- Notes:** 1. OTP=One-time programmable.  
 2. Alternate sources are not necessarily for products listed.  
 3. EE=Electrically erasable.  
 4. UV=Ultraviolet.

## A logic cell on a large-granularity device is equivalent to many more gates than on a small-granularity device. The end effect is more potentially usable gates go to waste.

as when the device is fully powered.

Second, power consumption when the device is operating with many of the gates changing state at 25 MHz may increase significantly over the standby power rating. To reap the benefits of low standby current, you need to operate devices at low clock rates or have periods of low clock-rate operation. Manufacturers' data sheets show how to compute the device current requirements when operating.

### Support for clocking requirements

Another possible way to narrow your search is to examine the available clock options. **Table 1** divides the clocks into system or global clocks and asynchronous clocks.

A system clock typically means a clock input that fans out to all registers. In the case of Atmel ATV 5000, the system clock has been partitioned so that each clock is distributed to a portion of the device. A system clock usually has a relatively low-propagation time and low skew, but that varies with the particular chip architecture.

The term asynchronous clock as used for **Table 1** indicates the ability to have individual registers use a different clock for complete flexibility. You can define all asynchronous clocks to have the same input conditions, and in effect make them system clocks, although skew and propagation time may suffer.

If you will be using the PLD for a completely synchronous design, then one or perhaps a few system clocks are all you need. If you'll be performing some asynchronous clocking operations, you'll need to restrict your choices to devices that provide that capability. Although not shown in **Table 1**, some devices provide only a common set and clear

control for registers. Others give you the option of setting and clearing registers individually.

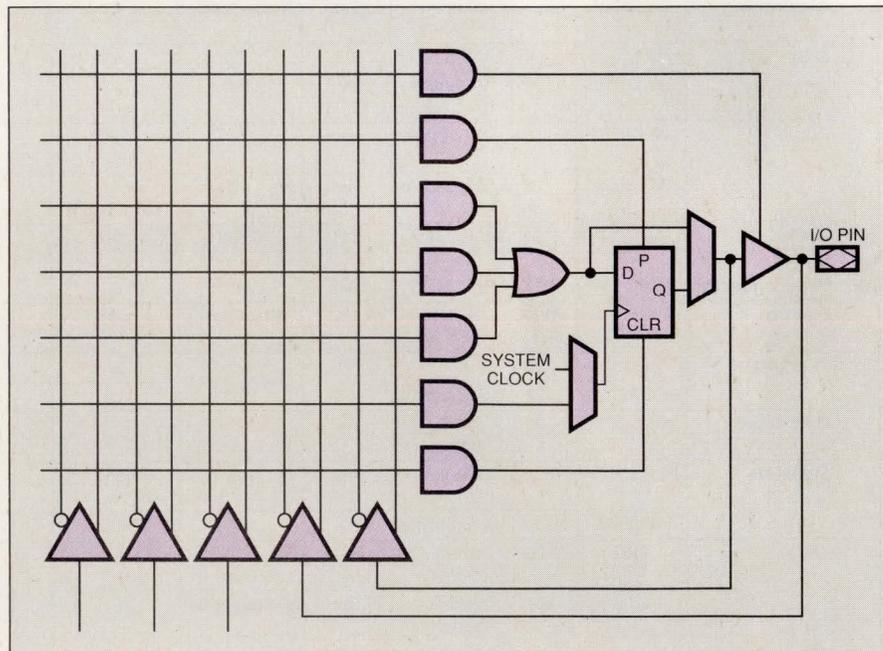
Discussing comparative features of devices is reasonably objective. But, when you try to compare PLD architectures, the task becomes considerably more subjective. You can, for example, count the number of logic cells in two devices, but deciding what the numbers mean when you are dealing with two different types of logic cells is very difficult. Until benchmarks or better methods of evaluating designs become available, trying to sort out architectural differences and what they mean to you may be your best bet.

All high-density PLDs operate as a group of logic cells with programmable connections between the cells. Many high-density PLDs let you program both the logic-cell connections and some of the functions

performed within the logic cells, rather than just connecting the logic cells. In addition, some devices offer more than one type of logic cell. Depending on the logic functions performed in each cell, you can assign architectures different granularities.

The ERA60100 from Plessey has the finest granularity, with each cell consisting of a 2-input NAND gate. A logic cell can also function as a transparent latch and two logic cells can function as a flip-flop. A series of local, short-range, and long-range interconnects provide signal routing among the 2500 logic cells on the chip. Programming the chip requires 27,320 bits of data, giving a rough measure of the flexibility of the device.

The CAL1024 from Algotronix also uses 2-input logic cells that can function as latches. Instead of just the NAND function, the logic cell



**Fig 1—The generic components of simple sum-of-products logic cells include wide programmable-AND gates feeding into an OR gate. Additional product terms may be used to control preset, reset, output enable, clocks, and other functions in the logic cell. All product terms are fixed in this example.**

## High-Density PLDs

can perform any function of two Boolean variables. The device provides two global signals, but other than that each logic cell connects only with its four nearest neighbor cells. The architecture of this device is best suited to regular logic structures, such as a shift register where the lack of medium- and long-range connections is not a drawback.

As you move up in granularity you come upon Actel's Act 2 family, which has logic cells that accept as many as seven inputs. The logic cells can perform any Boolean function of two variables, most of three variables, and some functions as high as seven variables. Actel rates its A1280 device with 1232 logic modules at 8000 usable gates, which they claim has the same logic capacity as a masked gate array with 8000 usable gates. Although the claim might be contested by some of Actel's competitors, the A1280 appears to have the largest logic capacity of any high-density PLD currently in production. With approximately 750,000 programmable anti-

fuses, the A1280 provides the most programmable connections of any PLD.

Quicklogic, a relatively new company, is shipping its first product, the QL8x12, which contains 96 logic cells. Each logic cell accepts as many as 14 inputs and performs any Boolean function of three variables and some to 14 variables. The company claims both high-speed and flexible logic capabilities. An example circuit on a portion of the chip is a 16-bit counter that can be loaded or operated at more than 100 MHz. The chip has about 76,000 programmable antifuses and is rated by the manufacturer as equivalent to a 1000-gate masked gate array.

Still higher in granularity is the Xilinx 4000 family. The company's 5000-gate 4005 is the largest member of the family currently shipping. Each logic cell in the 4000 family has two 4-input function generators, which can feed into two flip flops, be output directly, or combined to generate larger functions.

The 4000 family has a feature unique among PLDs in that you can use the function generator directly as RAM.

At the highest level of granularity you find the sum-of-products architectures. These devices typically use programmable, wide-input AND gates that feed into fixed- or variable-input OR gates (Fig 1). Although the basic structure of the sum-of-products devices may be similar, don't dismiss them as all being the same. There is considerable variation in device flexibility.

### Sum-of-product architectures

Table 2 contains data on product terms and how they are distributed within the devices that use sum-of-products architectures. The range of product terms possible in a logic cell (typically referred to as a macrocell in these devices) gives some idea of the flexibility of a particular device. If you can't get enough product terms in one logic cell, you'll pay a time penalty to cascade multiple logic cells.

**Table 2—Representative sum-of-product high-density PLDs**

Manufacturer	Product	Logic cells		Registers	Product terms		Fixed product terms per logic cell	Allocated product terms per logic cell	Shared product terms available to each logic cell	Comments
		I/O	Buried		Total on device	Per logic cell				
AMD	Mach 110	32	0	32	140	4.4	0.4	0 to 12	0	
	Mach 210	32	32	64	272	4.3	0.3	0 to 16	0	
Altera	Max 5064	28	36	64	604	9.4	7.4	0	32	Shared product terms increase propagation delay.
	Max 5192	64	128	192	1792	9.3	7.3	0	32	
Atmel	ATV2500	24	0	48	832	34.7	9	4 to 12	Limited sharing	
	ATV5000	52	24	128	1232	16.2	7.3	4 to 13	Limited sharing	52 input latches.
Intel	5AC324	24	0	24	384	16	8	0 to 16	0	10 input latches.
National Semiconductor	MLPL144	24	3	27	132	4.9	0.15	0	128	Programmable AND/OR array.
Plus Logic	H2010	30	6	36	228	6.3	5	0	12	Input latches; buried logic cells have input or output.
	FPGA2020	36	36	72	456	6.3	5	0	12	

See Table 1 for prices.

## When comparing high-density PLDs, it's a good idea to include the software in your comparison.

Most sum-of-products devices have some method to redistribute product terms. Therefore, those logic cells needing many product terms can get them, and those that don't need many don't have to waste them. The three methods of distributing product terms are fixed, allocated, and shared (see Fig 2).

Fixed product terms are locked to the input of an OR gate and cannot be redistributed. You can program allocated product terms to one of two or more logic cells. Product term allocation gives you more flexibility than fixed terms, but not as much as shared terms. With allocated product terms, two logic cells that need identical product terms will waste an extra product term to generate the same data twice. Note that when product term allocation is used, you can't have the

maximum number of product terms going to all logic cells. For each cell receiving greater than the average number of product terms, another logic cell, usually an adjacent one, must receive less.

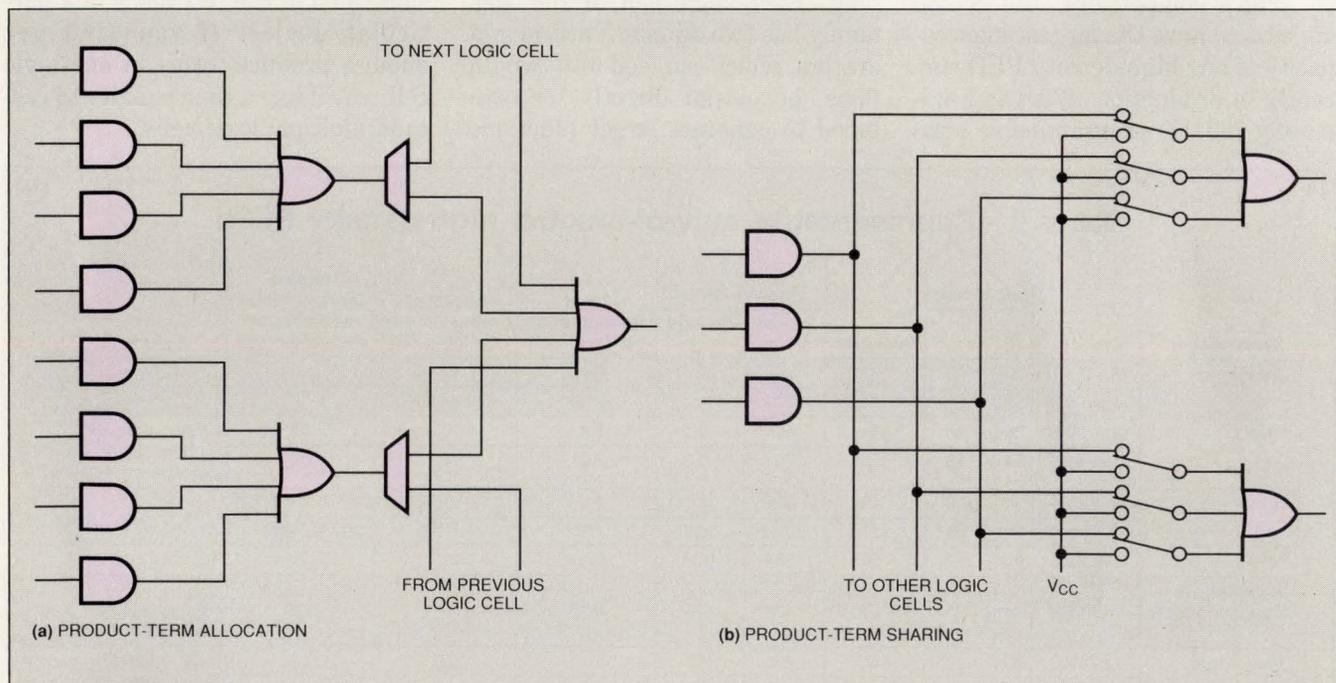
Shared product terms give you the most flexibility, requiring you to generate a specific product term only once. Because each logic cell should have *some* independent product terms, you'll usually see a few fixed product terms in addition to shared terms. The most flexible case of shared product terms is a programmable AND array that feeds into a programmable OR array, as used on National Semiconductor's MAPL144 array.

An interesting variation is the use of an XOR gate after the OR gate on Altera's logic cells (Fig 3). The XOR gate lets you invert the logic for active-high or active-low

logic applications. It also lets you apply de Morgan's theorem to use the large number of product terms for a wide sum.

You'll note from the data in Table 2 that some devices devote more product terms to secondary control functions than others. Typical uses of secondary product terms are for controlling register presets, clears, and clocks. The extra secondary-function product terms either provide flexibility that you may need, or wasted gates if you don't need them. It just depends on your application.

Another variation on sum-of-products architectures is the registers in each logic cell. Most have a single register per output logic cell, but Atmel's ATV 2500 and 5000 products offer two registers so that in some cases you can do the work of two logic cells with one.



**Fig 2—Product-term allocation or sharing** provide flexible alternatives to fixed product terms in sum-of-products architectures. Product-term allocation (a) typically lets you switch product terms in groups of four so that logic cells needing more product terms can take them from logic cells that need fewer. Product-term sharing (b) lets you use fewer product terms in a device by using a product term in more than one sum.

## High-Density PLDs

A large-granularity product that doesn't really fit into the sum-of-product architecture is the folded NAND array from Signetics (Fig 4). The PML2552 uses 96 NAND gates that fold back on themselves with 258 inputs on each gate to generate any combinatorial functions. Additional wide-input NAND gates drive latches and flip flops for sequential logic.

### Implication of device granularity

Trying to make comparisons of the architectures is difficult. Logic-cell granularity can at least help you gain an intuitive appreciation for logic flexibility vs performance.

Fig 5 shows a hypothetical comparison of the relative spread between the maximum possible gates in a particular PLD and the minimum usable gates if you were to try to use the device for many different circuits. The curve in Fig 5 is not based on real data and, obviously, the designs that result in the minimum usable gates are those for which the particular PLD is poorly

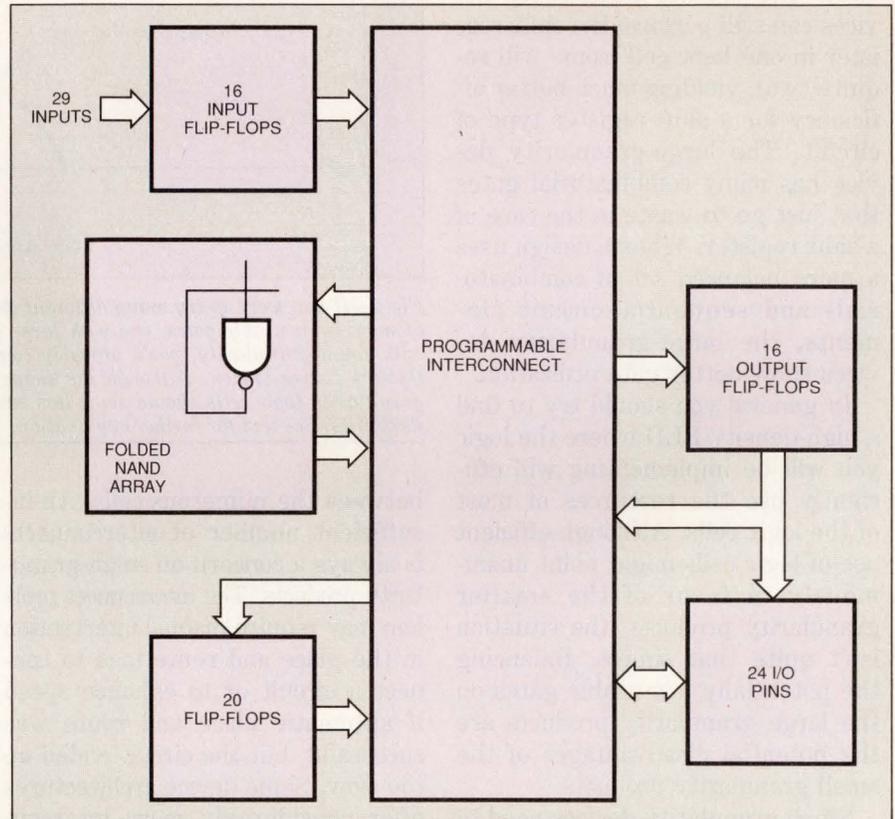


Fig 4—A folded NAND array is the basic building block of the PML2552. Ninety-six NAND gates with 258 inputs make up the basic logic element. Additional wide NAND gates drive the flip-flop inputs. The device provides flexible product sharing.

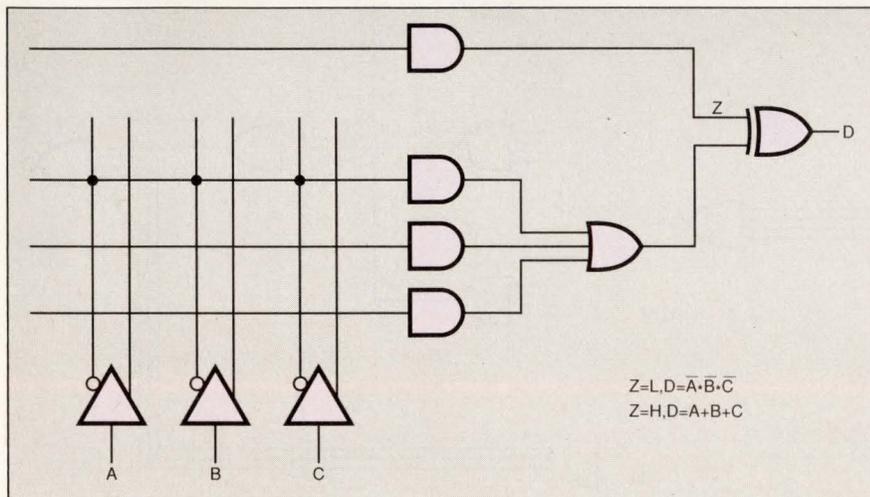


Fig 3—Using an XOR gate after the sum-of-products lets the Altera Max family change between active-high and active-low logic. Among other things, being able to invert the active state lets you use de Morgan's theorem to create wide sum terms from wide product terms. Some manufacturers provide an inversion select at the output of the logic cell, which provides a similar capability.

suited. The figure shows the relative differences between a fine-granularity device and another large-granularity device.

Assuming that both devices have the same maximum number of usable gates, the finer-granularity device should show a higher minimum-usable-gate number. The difference in minimum-usable gates happens because a simple function may consume a logic cell on both the large-granularity device and the small-granularity device. A logic cell on a large-granularity device is equivalent to many more gates than on a small-granularity device. The end effect is that more potentially usable gates go to waste.

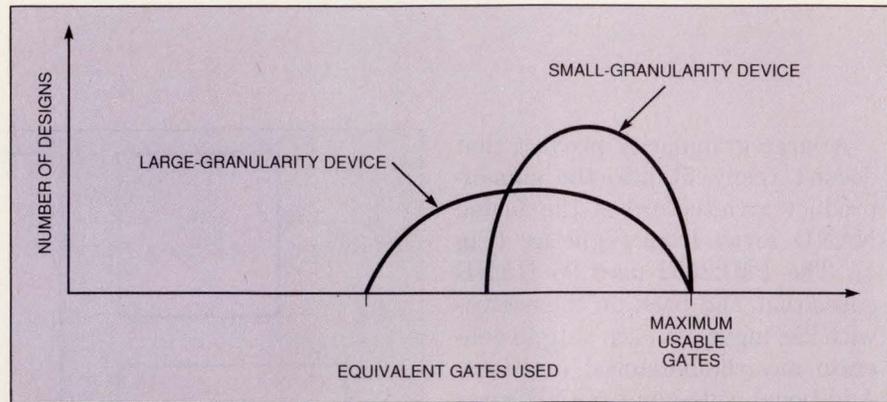
For example, consider a design

## High-Density PLDs

that uses a large shift register. Most large granularity logic cells offer one register per cell (a few offer two). The smaller granularity devices can still perform the shift register in one logic cell (some will require two), yielding much better efficiency for a shift-register type of circuit. The large-granularity device has many combinatorial gates that just go to waste in the case of a shift register. When a design uses a more balanced set of combinatorial- and sequential-circuit elements, the large-granularity devices show better gate utilization.

In general you should try to find a high-density PLD where the logic you will be implementing will efficiently use the resources of most of the logic cells. Although efficient use of logic cells might point unanimously in favor of the smaller granularity products, the situation isn't quite that simple. Balancing the potentially low usable gates on the large granularity products are the potential disadvantages of the small granularity products.

Small-granularity devices need to have many possible interconnects

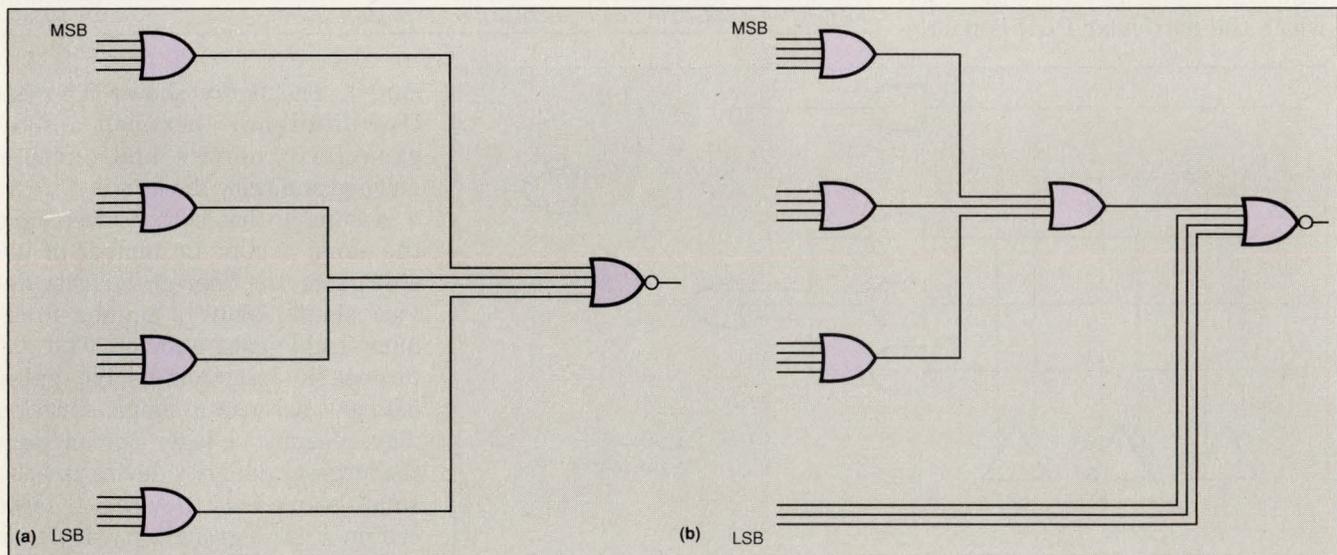


**Fig 5**—If you were to try many different designs on two PLDs with an equivalent number of maximum usable gates, one with large logic-cell granularity and another on a device with small granularity, you'd probably come up with something similar to the two hypothetical curves shown. Although the shape of the distribution is unknown, the smaller-granularity logic cells should show less variation in equivalent gates due to their greater flexibility. See text for further explanation.

between the numerous cells. An insufficient number of interconnects is always a concern on small-granularity products. The interconnect problem may require manual intervention in the place and route task to connect a circuit or to enhance speed if automatic place and route was successful, but the circuit ended up too slow. Some device architectures offer considerably more interconnects than others, easing the problem.

Another potential disadvantage of devices with small granularity logic cells is the possibility of low speed for circuits with wide-input functions. To some extent, you can counter the problem by careful design.

For example, to evaluate when a 16-bit-wide down counter reaches zero, you'd cascade the gates so that the LSB is evaluated at the last stage (**Fig 6**).



**Fig 6**—PLDs with small-granularity logic cells are often at a disadvantage when dealing with wide inputs because they require multiple levels of logic which cause longer propagation delays. Careful attention to design details can sometimes reduce or eliminate the disadvantage. Consider a circuit that evaluates the outputs of a 16-bit down-counter to determine when it has reached zero. You can design a circuit with two levels of logic delay using a logic cell capable of creating a 4-input OR function (a). With the same logic cell you can also design the circuit so that the down-count to zero is evaluated with only one logic-level delay, even though the overall circuit has three levels of delay (b).

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## High-Density PLDs

Xilinx has relatively large-granularity logic cells, although they are still small in comparison with the logic cells of many sum-of-products architectures. To improve the speed of wide decoding operations, the company's 4000 family has sixteen 40-bit-wide programmable decoders that can generate a decode in 10 nsec.

The fast, wide decoders are a specific example of a general trend for manufacturers to enhance performance in their evolving architectures by adding new logic cells or new functions to old cells. A further example is fast carry logic on Xilinx 4000 devices and on the FPGA2020 from Pluslogic.

When comparing high-density PLDs it's a good idea to include the

software you'll be using with that product and not just limit the comparison to the devices. Many of the devices let you use third party software tools for design entry, including schematic capture from major CAE vendors and design tools commonly used on low-density PLDs. Some PLDs may only be supported by the company's proprietary tools. For a rundown on PLD design entry and development tools, see **Ref 2**.

If you are accustomed to designing with low-density PLDs and using text-based design tools for Boolean equations or state-machine descriptions, you'll find you can use the same or similar tools for high-density PLDs. You might feel more at home with the sum-of-products

architectures that often let you design as though you were using multiple small PLDs with programmable connections.

If you are accustomed to designing at the schematic level, most high-density PLD families can provide macro libraries that let you make the transition from ordinary design with 7400 series TTL logic relatively easy. Don't just ask if the vendor provides a macro library, but take a good look at the building blocks you'll be designing with. Some vendors have a richer supply of macros than others. Noting how many logic cells are consumed by each macro function may give you a good idea of the logic capacity of a particular device family. Note also that as a company's device architect-

### Manufacturers of high-density PLDs

For more information on high-density PLDs such as those described in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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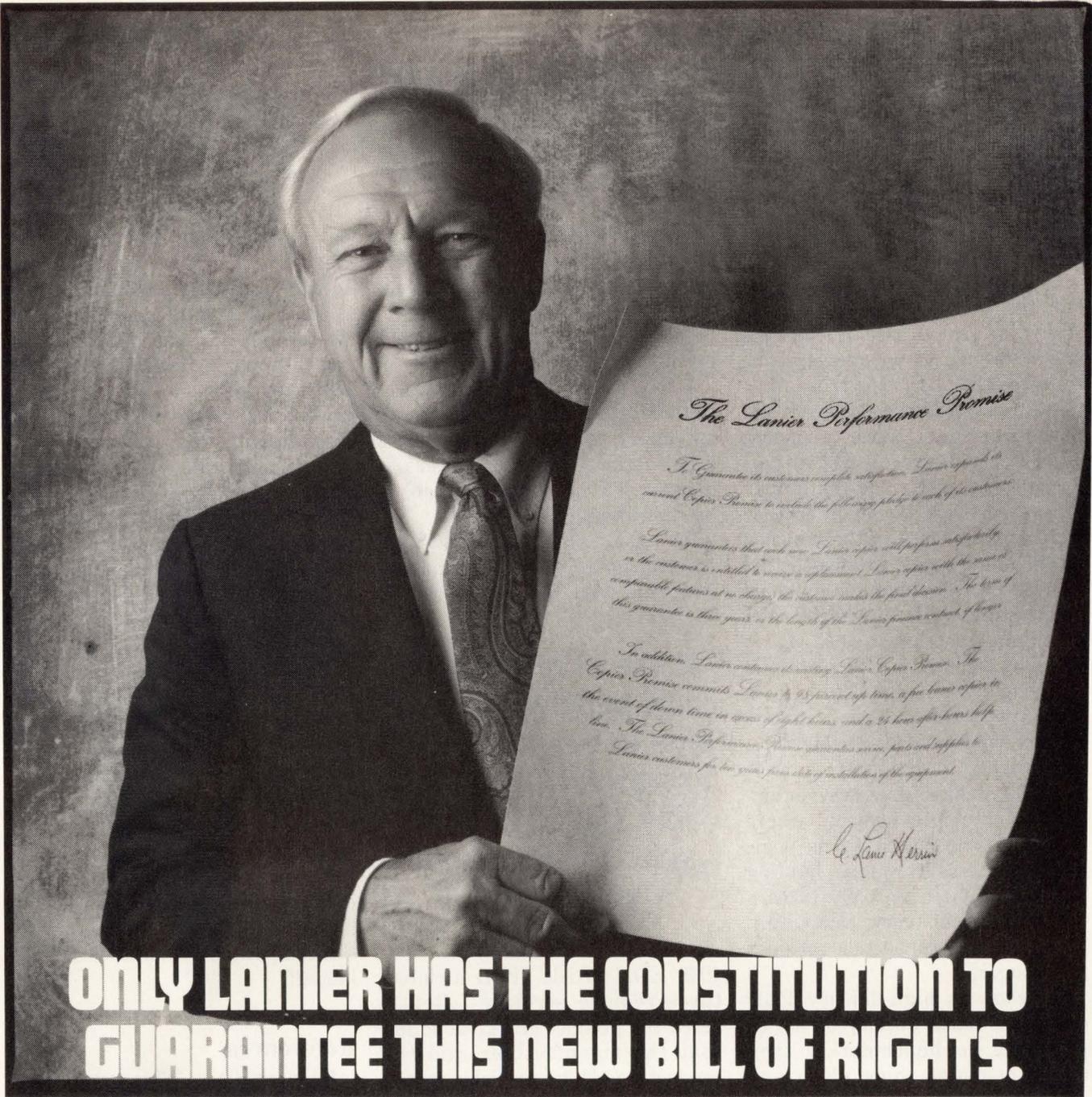
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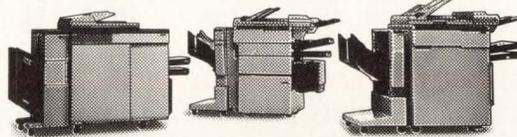
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## High-Density PLDs

ture changes, so too might their macro library.

Creating your logic design is only half the battle. Next you have to assign the logic to specific logic cells and determine the connections. The software that performs these functions are typically called fitters and place and route tools. Although automatic tools are available to perform the fit, place, and route functions, there are some differences both in the quality of the job they do and in the speed. The speeds can vary from a few minutes on some architectures to an overnight computer run on others.

The differences in the place and route operation may stem from variations in the quality of software or the flexibility of the architecture; most likely both. Many sum-of-products architectures provide universal array interconnects where any logic you can fit in the logic cell can be easily routed. Routing on these devices typically takes a few minutes on most computers. More complex connection schemes take longer.

As soon as high-density PLD companies finish working on device performance benchmarks, they might consider some place and route benchmarks. It's another hazy subject for a potential high-density PLD user.

### Stepping into the future

High-density programmable logic is seeing considerable growth right now, both as new product announcements from existing PLD companies and from new companies entering the high-density programmable logic business. Devices currently in development will more than double current logic capacity to around 20,000 gates. If all goes well, some of them might even be sampling by the first quarter of 1992.

However, you should be careful about using soon-to-be-available chips in your design. As is the case with many highly competitive electronic products, getting them to market as soon as possible is of paramount importance to the manufacturer. Unfortunately sometimes everything but the product makes it to market—the specifications, a delivery date, quantity pricing—but no silicon.

An example is the PA7040 from International CMOS Technology (San Jose, CA). The September 28,

**If the chip company can't supply a real device and a data sheet to match it, you probably should not consider the device for your design.**

1989 EDN article "PLD architectures require scrutiny" (Ref 1) listed the product in a table noting that the manufacturer said the product would be available in the first quarter of 1990 and gave a price. The PA7040 is now scheduled to be available in the second quarter of 1992. Waiting more than two years for a part in your design will probably kill your project, if not your company.

ICT is by no means the only company to have ever done this: Many IC companies that give price and delivery dates before the product is in production end up being late with the product. Some ICs, such as complex microprocessors, often need lots of pre-release information so you can build a system around them and be ready to ship your product when the first chips come

out of production. The whole concept around programmable logic is to have a flexible architecture that is quick and easy to put your circuit design into. If the chip company can't supply a device and a data sheet to match it, you probably should not consider the device for your design.

Companies should let you know what their future directions are. You also need to know that the company plans to continue the product line and what improvements they are working on. Just be sure you separate today's real silicon from tomorrow's promise.

Be extremely careful when an IC company compares its product with a competitor's. In a lot of literature, the comparisons are often today's products against the competitor's older generation product. Even worse, some comparisons are of tomorrow's products against what the competitor delivers today. Whenever a competitor's product makes a poor showing, you'd best give the competitor a chance to defend himself. **EDN**

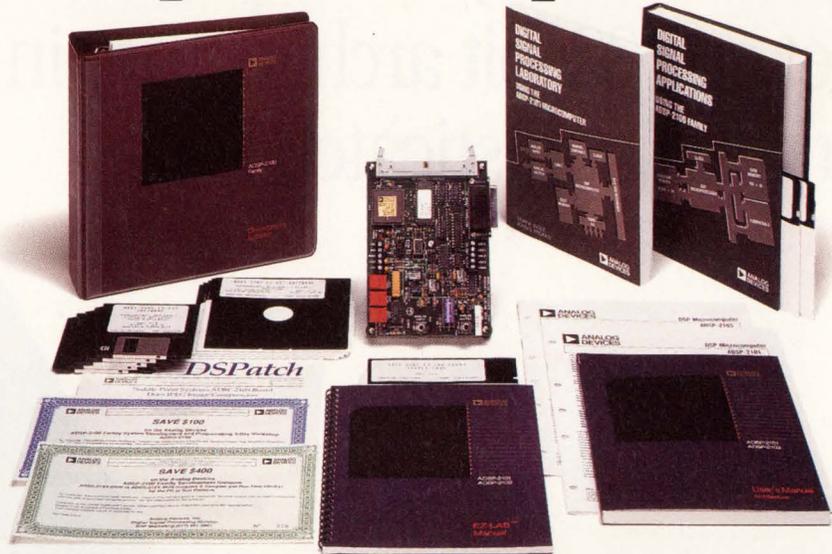
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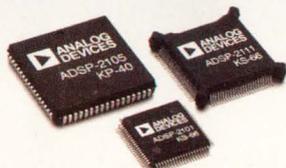


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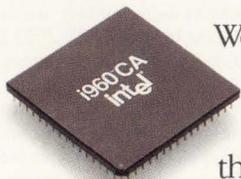
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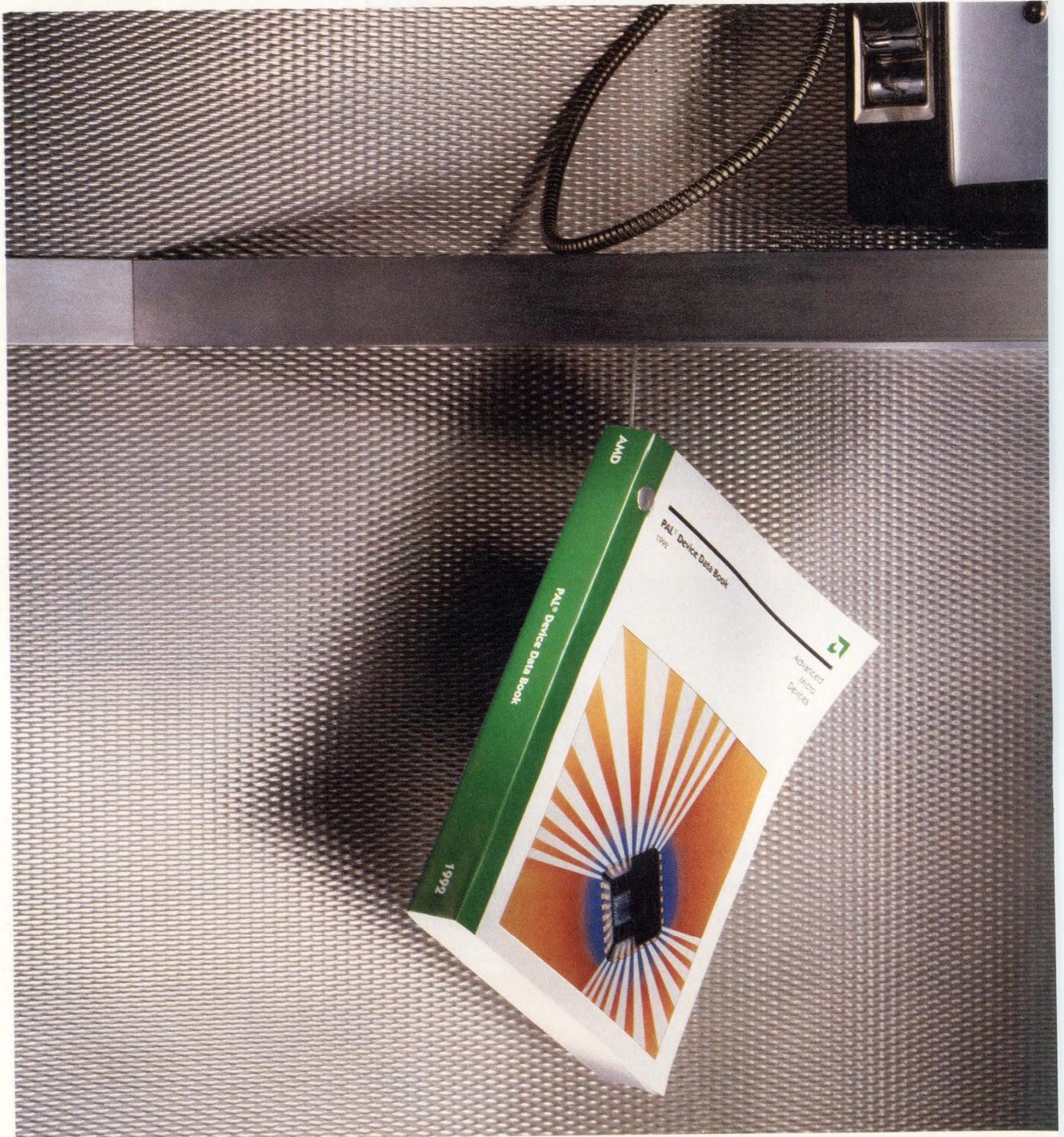
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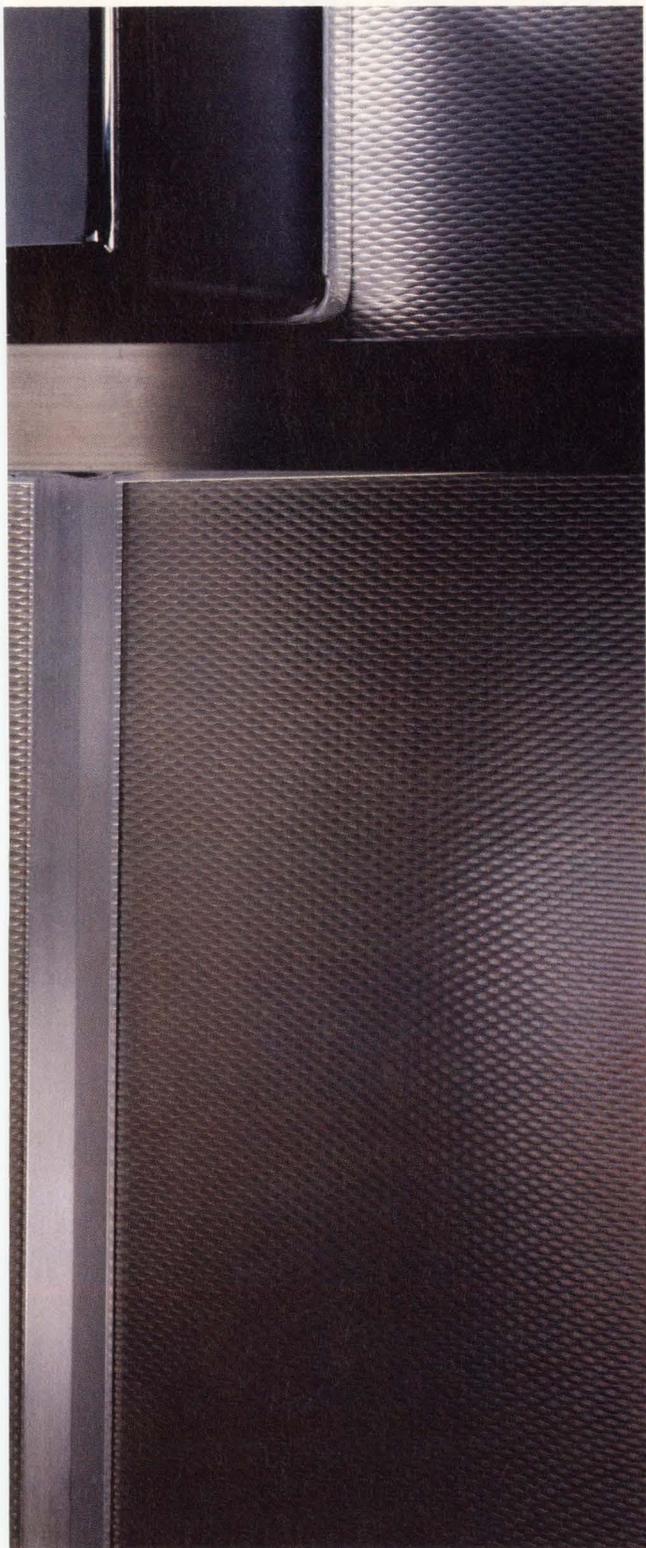
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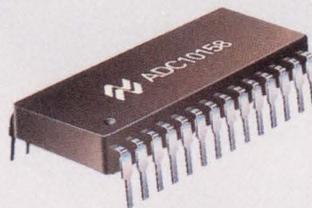
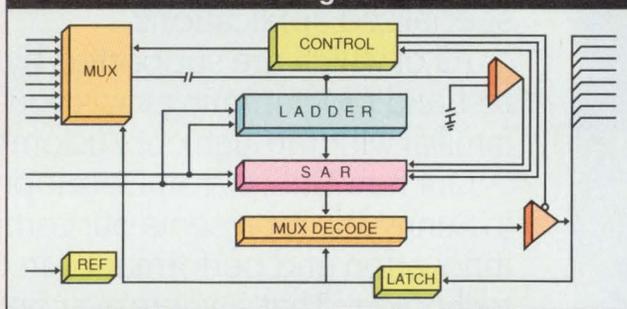
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# C++ has C's familiarity and OOP capability

---

*C++ adds a host of new features to C, including object-oriented programming (OOP) abilities. If you program in C, you can use these features without having to learn a whole new language.*

---

George Ellis, *Industrial Drives*

The C programming language is popular with engineers for a couple of very good reasons: C code is efficient, and it gives the programmer direct control of the computer. C++ maintains C's power and efficiency, yet adds object-oriented programming and other features that you can use without learning a new language. In addition, you can recompile your existing C programs in C++ with few changes, and you can link to compiled C programs and libraries without any changes at all.

The most important feature of C++ is its object-oriented programming ability. OOP offers the benefits of flexible data structures, reusable code, and operators for nonstandard data types.

For engineers who use C for scientific programming, operators for nonstandard data types may be C++'s most important feature. When you define a data type (*matrix*, for example), you can also define the effects of operators (such as \* and /). If you write programs

that manipulate nonstandard data types, such as matrices and complex numbers, this capability can be very useful.

Before delving into all of C++'s object-oriented features, however, you might want to consider the language's other features that, as a C programmer, you can use immediately. These features include:

- improved dynamic memory allocation
- single-line comments
- passing references
- overloading functions
- default values
- in-line functions.

Each of these features either adds convenience to standard C, or lets you avoid a peculiar characteristic of the language. As a group, they let you make your programs more readable, and thus easier to write, debug, and explain.

## **Improved dynamic memory allocation**

Dynamic memory allocation in standard C uses *malloc()* or one of *malloc()*'s variations. For example, if you want to allocate space for an array of x integers, you might write

```
int      *dynamic_int;  
dynamic_int = (int *)malloc(x*sizeof(int));
```

Notice that you must cast the return value of *malloc()* as an integer pointer, because *malloc()* returns a void pointer. Also, you must manually declare the size of

---

*C++ maintains C's power and efficiency, yet has object-oriented programming and other features that you can use without learning a new language.*

---

the variable being allocated (in this case, by using *sizeof*), because *malloc()* allocates memory in bytes.

In C++, you can use the operator *new* instead of *malloc()*. For example,

```
int      *dynamic_int;
dynamic_int = new int[x];
```

You do not need to cast the return value of *new* because *new* itself returns the appropriate type (in this case, an integer pointer). The operator *new* also determines the size of the variable type being allocated, making the *sizeof* operator unnecessary.

### Single lines for short comments

C++'s provisions for including comments in code retain the standard C comments and also let you use *"/"* to designate a comment that runs no farther than the end of a line. For example,

```
/*This comment works in both C and C++  */
//This comment works in C++.
```

The *"/"* is convenient for short comments. The standard C markers are probably better for long comments.

Another C++ improvement involves function arguments. In standard C, arguments of functions are passed by value, not by address; if you need a function to change the value of a variable, you must pass a pointer to that variable. C++ lets you pass references, which are simply pointers in a more readable form. **Listing 1** shows examples of C and C++ functions that change the values of an integer and two members of a structure. Notice that the C++ functions, *Cpp\_set\_int()* and *Cpp\_set\_simple()* are more intuitive than the standard C functions, *C\_set\_int()* and *C\_set\_simple()*.

Another C++ feature lets you overload functions. Function overloading means that two different functions can have the same name if they have different "signatures." A function's signature is the combination of the function's return type, the number of calling arguments, and the type of each calling argument.

Functions in both C and C++ have signatures, but in standard C, the function prototype defines a unique signature for each function name. In C++, several different functions can have the same name; the compiler differentiates between the functions by examining the signature of the function call. Overloading is particularly useful when several functions perform the same operation on different data types.

For example, consider the C++ program in **Listing**

### Listing 1—C and C++ functions

```
struct simple_struct( //define simple structure to
  int n;              //illustrate passing references
  double x;
);

void Cpp_set_int(int& i, int j);
void C_set_int(int *, int j);
void Cpp_set_simple(struct simple_struct& simple,
  int n, double x);
void C_set_simple(struct simple_struct *simple, int n,
  double x);

void main()
{
  int i = 0;
  struct simple_struct simple;

  C_set_int(&i, 1); //set i in standard C by passing a ptr
  Cpp_set_int(i, 2); //set i in C++ by passing a reference

  C_set_simple(&simple, 3, 100.); //set simple in standard
  //C by passing a pointer
  Cpp_set_simple(simple, 4, 200.); //set simple in C++ by
  //passing a reference
}

void C_set_int(int *i_ptr, int j)
{
  *i_ptr = j; //C requires you to dereference a pointer
}

void Cpp_set_int(int& i, int j)
{
  i = j; //C++ lets you pass references for more
  //readable programs
}

void C_set_simple(struct simple_struct *simple_ptr, int n,
  double x)
{
  simple_ptr->n = n; //In C, use the -> operator to
  simple_ptr->x = x; //dereference pointers
}

void Cpp_set_simple(struct simple_struct& simple, int n,
  double x)
{
  simple.n = n; //In C++, pass references to avoid ->
  simple.x = x;
}
```

2. Three functions have the name *average()*; each has a different signature, because the functions' calling arguments are of different types. When the program runs, it calls each function once. The output of the program is

```
Calling the 'integer' average...
  average of 1 and 2 is 1.500000
Calling the 'float' average...
  average of 1.0f and 2.0f is 1.500000
Calling the 'double' average...
  average of 1.0 and 2.0 is 1.500000
```

C++ also lets you specify default values in a function prototype or declaration. If you call a function without specifying all the arguments, the unspecified arguments contain default values. For example, **Listing 3** shows a program that calculates the area of an ellipse. The calling arguments are the major and minor radii. However, if a program calls the function and specifies only the major radius, the minor radius will

## Listing 2—Function overloading

```
#include <stdio.h>

double average(int first, int second){
    printf("Calling the 'integer' average()...\n");
    return( ((double)first+ (double)second) /2.0 );
}

float average(float first, float second){
    printf("Calling the 'float' average()...\n");
    return( ((double)first+ (double)second) /2.0 );
}

double average(double first, double second){
    printf("Calling the 'double' average()...\n");
    return( (first + second)/ 2.0 );
}

void main()
{
    printf(" average of 1 and 2 is %lf \n", average(1, 2));
    printf(" average of 1.0f and 2.0f is %lf \n",
           average(1.0f, 2.0f));
    printf(" average of 1.0 and 2.0 is %lf \n", average(1.0,
           2.0));
}
```

take on the default value of 0.0. The function will then treat the ellipse as a circle with a radius of the specified major radius.

So that you can avoid a normal function's call-and-return sequence—along with the associated execution-time overhead—C++ lets you declare a function as *inline*. You write source code as you would for an ordinary function, but your C++ compiler generates object code that is “in-line,” rather than in a separate, callable function. This feature is best for short functions (perhaps two or three lines) in which the call-and-return overhead of a normal function would be significant compared with the function's execution time.

To achieve the result of an in-line function in standard C, you would need to use the `#define` preprocessor command. The square function is an example (Ref 1). The C code

```
#define square(x)      ( x * x )
```

can be replaced in C++ with

```
inline double square(double x) {return ( x * x );};
```

The C++ version is more readable, especially for new C programmers.

C++ has features that do much more than add convenience and clarity to C. The object-oriented programming capabilities of C++ actually change the way you program. It is impossible in a brief space to cover OOP thoroughly, so our focus is on what OOP can do, rather than on how to use it.

## Listing 3—Functions with default arguments

```
double ellipse_area(double major, double minor = 0.0);

double ellipse_area(double major, double minor)
{
    if( minor == 0.0)
        return(2.0 * PI * major * major);
    else
        return(2.0 * PI * major * minor);
}

void main()
{
    printf("Area of ellipse with major radius = 5.0 and minor
           radius = 2.0 = %lf\n",
           ellipse_area(5.0, 2.0));
    printf("Area of circle with radius = 4.0 = %lf\n",
           ellipse_area(4.0));
}
```

An OOP language such as C++ has three basic characteristics:

- Encapsulation—mixing data and functions into one “object” (a structure or class)
- Inheritance—the ability to derive new objects from old ones
- Polymorphism—the support of virtual functions.

Encapsulation is the most basic characteristic; it is the foundation of OOP. Inheritance extends encapsulation, letting you build new objects from old ones. Polymorphism extends inheritance in order to help you write more reusable code.

Encapsulation lets you organize data and functions into one object. The data and functions can have a stronger relationship with encapsulation than they can without it. With conventional languages, the design of functions is usually the fundamental step in developing a program. In an OOP language, data and functions are so intertwined that the design of objects can become the foundation of the program.

C++ has two types of objects: classes and structures. They are so similar that they can be used almost interchangeably. Both differ from C structures in that they can have functions as members in addition to data. Member functions belong to objects, and they normally manipulate data in their own objects.

With encapsulation, you can protect both the data and function members of objects. There are two main levels of protection: public and private. If a data element or a function is public, any function can access it; if it is private, only member functions can access it.

Some form of protection is often necessary in a module to keep functions in other modules (often written by different programmers) from improperly manipulating data. For example, consider the structures that

*Instead of forcing you to pass a pointer to a variable, C++ lets you pass a reference, which is essentially a pointer, but in a more readable form.*

many C library functions use to store information about DOS files. The structure *ffblk* in Borland C++ (Borland International Inc, Scotts Valley, CA) is typical:

```

struct ffbk {
    char    ff_reserved[21];
    char    ff_attribute;
    int     ff_time;
    int     ff_date;
    long    ff_size;
    char    ff_name[13];
};

```

The user should never change the data in *ffblk* directly; Borland C++ provides *findfirst()* and *findnext()* to change data-member values.

As an experiment, redesign *ffblk* in C++. The hypothetical object, *cpp\_ffblk*, will have the same data members as *ffblk* and will protect the data from inadvertent access and manipulation. You can add *findfirst()* and *findnext()* as member functions.

The first step in adding member functions is to list the function prototype in the object:

```

struct cpp_ffblk {                //hypothetical C[+][+] object
    char    ff_reserved[21];
    char    ff_attribute;
    int     ff_time;
    int     ff_date;
    long    ff_size;
    char    ff_name[13];

    //member functions to fill the data members
    int     findfirst(const char *pathname, struct ffbk
        *this_ffblk, int attrib);

    int     findnext(struct ffbk *this_ffblk);
};

```

Notice that the first data member is the character string *ff\_reserved[]*. You may have correctly assumed that "reserved" implies you should not use or change this string. You can revise *cpp\_ffblk* and specify *ff\_reserved[]* as private, so that only the two member functions can access it:

```

struct cpp_ffblk {                //add protection for ff_reserved
private:
    //non-member functions cannot access private data
    char    ff_reserved[21];
public:
    char    ff_attribute;
    int     ff_time;
    int     ff_date;
    long    ff_size;
    char    ff_name[13];

    //member functions to fill the data members
    int     findfirst(const char *pathname, struct ffbk
        *this_ffblk, int attrib);

    int     findnext(struct ffbk *this_ffblk);
};

```

Users should be able to read the remaining data members, but not change them. To make a data mem-

ber read-only, declare it *private* and write a *public* member function that returns the data member's value. In the final version of *cpp\_ffblk*, the remaining five data members are read-only:

```

struct cpp_ffblk {                //protect all data
private:
    //non-member functions cannot access private data
    char    ff_reserved[21];
    char    ff_attribute;
    int     ff_time;
    int     ff_date;
    long    ff_size;
    char    ff_name[13];

public:
    //member functions to fill the data members
    int     findfirst(const char *pathname, struct ffbk
        *this_ffblk, int attrib);

    int     findnext(struct ffbk *this_ffblk);

    //member functions to make data "read-only"
    char    get_attribute()      return(ff_attribute);};
    int     get_time()          (return(ff_time));};
    int     get_date()          (return(ff_date));};
    long    get_size()          (return(ff_size));};
    char    *get_name()         (return(ff_name));};
};

```

Because you have defined and written the five new member functions right inside the structure, the compiler will make them *inline*.

The constructor and destructor functions of C++ are useful for allocating and deallocating memory. Each object can have both a constructor and a destructor as member functions. The constructor has the same name as the object (for example, *ellipse*), and the destructor has the same name preceded by a tilde (*~ellipse*).

Constructors execute anytime space is allocated for an object. For example, if you use the *new* operator for dynamic memory allocation, the constructor for that object is automatically called. A typical use for constructors is to initialize data members, although you can write a constructor to perform any C++ action, from printing a message on the screen to opening a DOS file.

In the following object, *ellipse*, which stores the major and minor radii of an ellipse, a constructor sets the radii to zero:

```

struct ellipse{
    double major;
    double minor;
    double area;

    //This is a simple constructor
    ellipse() {    major = 0.0;
                  minor = 0.0;
                  area  = 0.0;
                };
};

```

Now each time space is allocated for an ellipse structure, all the data members will be initialized to zero.

Destructors offer flexibility for removing objects from memory. For example, if a constructor opens a DOS file and allocates memory, a destructor can be written to close that file and deallocate memory. Destructors are used less frequently than constructors.

### Define operators for nonstandard data

Another C++ feature, operator overloading, makes programming easier by letting you define operators for your objects. Overloading lets operators invoke different functions depending on the data types of the operands. (You are probably familiar with overloading for math operators; in C, the four algebraic operators (\*, /, +, and -) perform different, albeit similar, functions depending on whether the operands are *long*, *int*, *float*, *double*, or *char*.)

Operator overloading is especially useful if you frequently manipulate nonstandard data types. For example, Borland C++ provides *complex.h*, a header file that defines a *complex* object type. You use the file for complex (as opposed to real) mathematics. *Complex.h* includes definitions of several algebraic operators for the complex object type and lets you write complex math algebraically. For example,

```
main()
{
  complex a, b;

  ...body of program fills a and b with complex numbers

  a /= b;      //use overloaded /= operator to calculate
              //a = a/b.
}
```

If you were programming in standard C, the

```
a /= b;
```

would have to be replaced by a function call such as

```
a = complex_divide( a, b );.
```

### Inheritance derives new objects from old

The second major characteristic of OOP is inheritance. Inheritance lets you derive new objects from old ones; its purpose is to help you write reusable programs. In the process of inheritance, a new object (the child) derives data and member functions from another object (the parent).

The need for inheritance is apparent in graphics routines, for example. Suppose you have a software package that includes several shapes—points, lines, squares, triangles, and so on. In standard C, if you

want to add a new shape, you might need to alter half of the existing graphics routines. With a well-written OOP graphics package, however, you should only have to write code specific to your new shape, such as expanding or shrinking the shape. An object for a point might be defined as

```
struct point{
  double  x;      //x coordinate for point
  double  y;      //y coordinate for point
};
```

A circle is similar to a point. It has x and y coordinates, but it also has a radius. You can take advantage of the similarities by making the circle a child of *point*:

```
struct circle: point{ //circle inherits point
  double  radius;    //circle adds radius
};
```

Now if you define a circle, it has the x and y coordinates from *point* along with its own radius. For example, you can write:

```
struct circle  a;
a.radius = 1.0;
a.x = 10.0;
a.y = 20.0;
```

The x and y in *circle* are inherited from *point*. Similarly, if *point* has a member function, *move()*, that moves the point by changing x and y, *circle* can inherit that function. You don't have to write a new *move()* function for the new shape.

Inheritance can continue indefinitely. For example, you can think of an ellipse as a circle with an extra radius:

```
struct ellipse: circle{
  double  minor_radius;
};
```

Now *ellipse* has a radius (assumed to be the major radius) from *circle*, x and y from *point*, and its own *minor\_radius*.

Objects also inherit overloaded operators from their parents, and they can inherit from multiple parents. For flexibility, you can override inheritance of a specific function if the function in the parent is not appropriate for the child. In general, it is easy to modify a well-written OOP program, because you have the option of using all the functions that have been written for similar objects.

The third major characteristic of OOP is polymorphism. Borland defines polymorphism as "Giving an action one name or symbol that is shared up and down a class, with each class in the hierarchy implementing

---

*In C++, several different functions can have the same name; the compiler differentiates between the functions by examining the signature of the function call.*

---

the action in a way appropriate to itself" (Ref 2).

Suppose you buy a graphics package that can draw, erase, and move a circle, and you need to modify the package so that it will perform the same functions on an ellipse. You would probably derive the code for the ellipse from the existing code for a circle, a more basic shape. You would also probably want to use function names in your new *ellipse* structure that already exist in *circle*.

But consider what happens if you rewrite a member function of *circle* to create a similar function for *ellipse*. Suppose that *move\_shape()*, a function that the graphics package calls to move any shape, calls a member function specific to each shape, *hide\_shape()*. If you rewrite *hide\_shape()* from *circle* to make *hide\_shape()* for ellipse, how will *move\_shape()* know to call this new *hide\_shape()*? Remember, *ellipse* didn't even exist when *move\_shape()* was written. The answer lies in making *hide\_shape()* a virtual function.

Virtual functions are always member functions. Each structure in a hierarchy can have as a member a virtual function with the same name as a function in another structure. When a general-purpose function (like *move\_shape()*) is called, one of its calling arguments is a pointer to the structure in the hierarchy for the particular shape (such as a circle or an ellipse) the function is to work on. Then, if this general-purpose function calls a virtual function (like *hide\_shape()*), the pointer ensures that the appropriate virtual function will execute.

All of this can be confusing, especially if you're new to OOP. The important point to remember, though, is that virtual functions let you extend programs without recompilation. The determination of which member function to call occurs at runtime, not at compile time.

Whether or not you plan on doing object-oriented programming, C++ still has many features that make programs easier to write, read, debug, and explain than C. If you want to use OOP, C++ offers the promise of better and more reusable code. In either case, if you already program in C, you won't have to learn a new language or spend much time rewriting your current C utility routines.

Making the transition to C++ needn't be expensive, either. For example, the Turbo C++ compiler from Borland International Inc (Scotts Valley, CA) costs less than \$100, supports both ANSI C and AT&T 2.0 C++, and comes as part of an integrated environment that lets you edit, compile, link, and debug C++ programs.

**EDN**

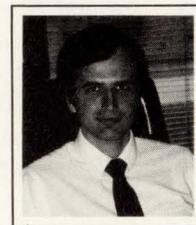
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## Author's biography

George Ellis is a Senior Project Engineer at Industrial Drives in Radford, VA, where he designs electronics and real-time software. He wrote *Control System Design Guide* (Academic Press Inc, 1991) and serves on the IEEE Industrial-Drives Committee. George holds both a BSEE and MSEE from Virginia Polytechnic Institute and State University (Blacksburg, VA).



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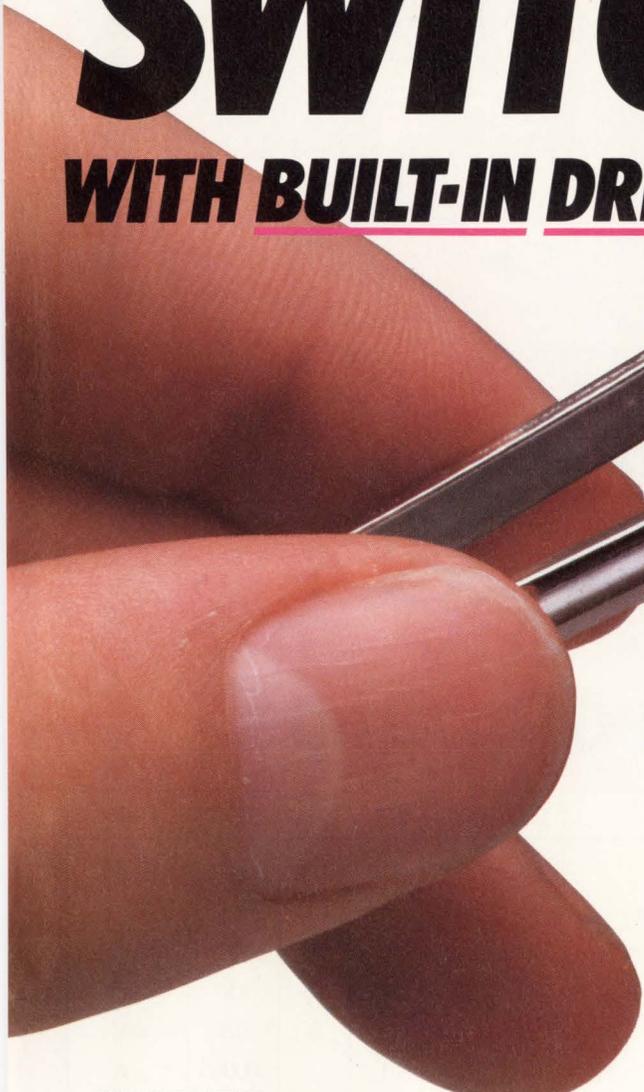
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1500-3000MHz	35	22	35	22
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100-1500MHz	27	19	27	19
1500-3000MHz	30	28	30	28
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	1.3	1.6	1.3	1.6
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G.B.W. Gain Bandwidth (Typ)	45	45	90	100	14	MHz
$t_s$ Settling Time (to 0.1%) (Typ)	90	90	100	75	340*	nsec
$AVOL$ Open Loop Gain (Typ)	50	7	45	28	450	$V/mV$
$VOS$ Offset Voltage (Max)	1	2	6	3	0.9	mV
$I_{OS}$ Offset Current (Max)	0.3	0.4	1	—	.00005	$\mu A$
$I_B$ Bias Current (Max)	0.3	8	1.7	3	.0001	$\mu A$
$e_n$ Voltage Noise ( $f = 10KHz$ )	17	22	25	3.3	15	$nV/\sqrt{Hz}$
$i_n$ Current Noise ( $f = 10KHz$ )	3	1.5	4	2.1	.002	$pA/\sqrt{Hz}$
Min Gain Stable	1	1	1	1	1	
$I_S$ Supply Current (Max)	10.5	9	40	10	11	mA
Price (100's) \$ (PDIP)	3.85	2.85	2.40	2.85	2.50	

\*12 Bit Settling Time



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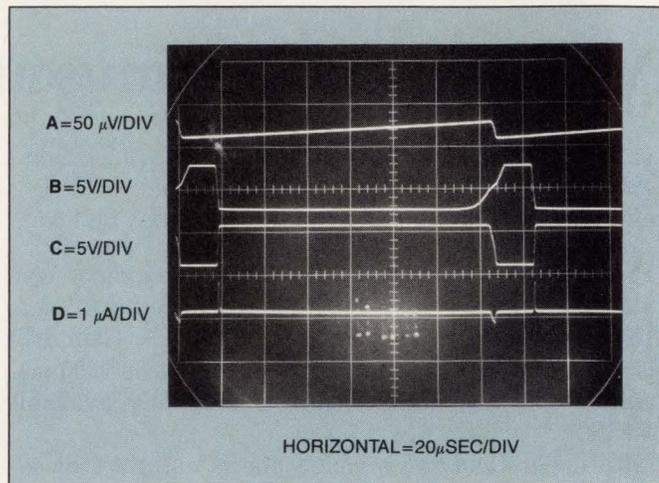
# DESIGN IDEAS

IC<sub>1</sub>'s input from seeing voltages outside its negative common-mode limit.

The circuit must carefully control Q<sub>1</sub>'s emitter voltage to get low drive. Q<sub>3</sub> and Q<sub>4</sub> compensate Q<sub>5</sub> and Q<sub>6</sub> for temperature while Q<sub>2</sub> compensates Q<sub>1</sub>'s V<sub>BE</sub>. The two LT1034s are the actual voltage reference, and the LM334 current source provides 35- $\mu$ A bias to the stack of transistors. The current drive provides excellent supply immunity (better than 40 ppm/V) and improves the circuit's temperature coefficient by using the LM334's 0.3%/°C temperature coefficient to temperature-modulate the voltage drops slightly in Q<sub>2</sub>, Q<sub>3</sub>, and Q<sub>4</sub>. This correction's sign and magnitude directly oppose that of the -120-ppm/°C polystyrene capacitor, thus aiding overall circuit stability.

The Q<sub>1</sub> emitter follower delivers charge to the 100-pF capacitor efficiently; both the base and collector currents end up in the capacitor. The CMOS inverter provides low-loss SPDT reference switching without significant drive losses. The 100-pF capacitor draws only small transient currents during its charge and discharge cycles. The 50-pF, 47-k $\Omega$  positive-feedback combination draws insignificantly small switching currents. At zero frequency, IC<sub>1</sub>'s quiescent current and the 35- $\mu$ A reference-stack bias account for all current drain. No other paths for loss exist. As the frequency scales up, the charge-discharge cycle of the 100-pF capacitor introduces a 1.5- $\mu$ A/kHz increase.

Circuit startup or overdrive can cause the circuit's ac-coupled feedback to latch. If latchup occurs, IC<sub>1</sub>'s output goes high. IC<sub>2</sub>, detecting this condition via the inverter and the 2.7-M $\Omega$ , 0.1- $\mu$ F lag, also goes high.



**Fig 2**—This scope photo captures one cycle of the VFC's action. The ramp in trace A causes IC<sub>1</sub>'s output to eventually switch (trace B), thus developing a corresponding output pulse (trace C). Trace D is a reset pulse for the ramp.

IC<sub>2</sub>'s going high lifts IC<sub>1</sub>'s negative input and grounds the positive input through Q<sub>7</sub>. These actions initiate normal circuit action.

Because the charge pump connects directly to IC<sub>1</sub>'s output, response is fast. The output settles within one cycle for a fast input step. To calibrate this circuit, apply 50 mV and select R for a 100-Hz output. Then apply 5V and trim the input potentiometer for a 10-kHz output. **EDN BBS /DI\_SIG #1070** **EDN**

To Vote For This Design, Circle No. 745

## Design expands PC bus

András Pomozi and Tibor Szép  
Technical University of Budapest, Budapest,  
Hungary

The circuit in Fig 1 shows how to configure an extension bus for an IBM PC/XT or PC/AT. The circuitry inside the dashed lines is diagrammatic; you burn this circuitry into a 22V10-25 PAL device.

IBM PC bus lines fall into three categories:

### Output signals

- Always active output signals:  $\overline{\text{DACK}}_i$  ( $i=0, 1, 2, 3, 4, 5, 6, 7$ ), AEN, CLK, RESET, BALE, SMEMR, SMEMW, T/C, and OSC.

- Signals whose direction  $\overline{\text{MASTER}}$  controls: Address lines,  $\overline{\text{IOR}}$ ,  $\overline{\text{IOW}}$ ,  $\overline{\text{MEMR}}$ ,  $\overline{\text{REFRESH}}$ , and SBHE. These signals are outputs if the PC is the bus master and inputs if an extension-bus card, such as a DMA controller, is the master.

### Input signals

- Active-high signals:  $\overline{\text{IRJ}}_j$  and  $\overline{\text{DRQ}}_j$  ( $j=3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 14, 15$ ).
- Active-low signals:  $\overline{\text{MASTER}}$  (the expansion-bus master signal),  $\overline{\text{I/OLOCK}}$ ,  $\overline{\text{I/OCHRDDY}}$ ,  $\overline{\text{MEMCS16}}$ ,  $\overline{\text{I/OCS16}}$ , and OWS.

### Bidirectional signals

- $\text{SD}_k$  ( $k=0, \dots, 15$ ).

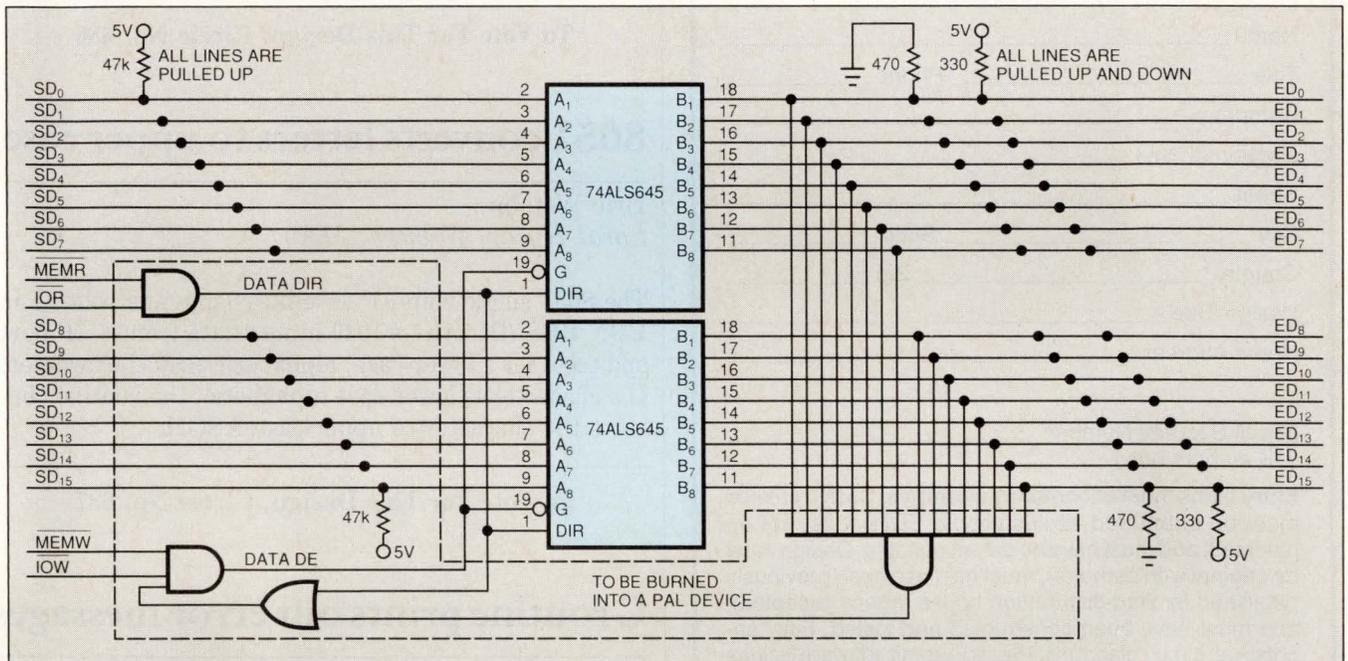
# DESIGN IDEAS

**Fig 2** shows the simple interface circuits needed to connect the various classes of PC-bus lines to the extension bus.

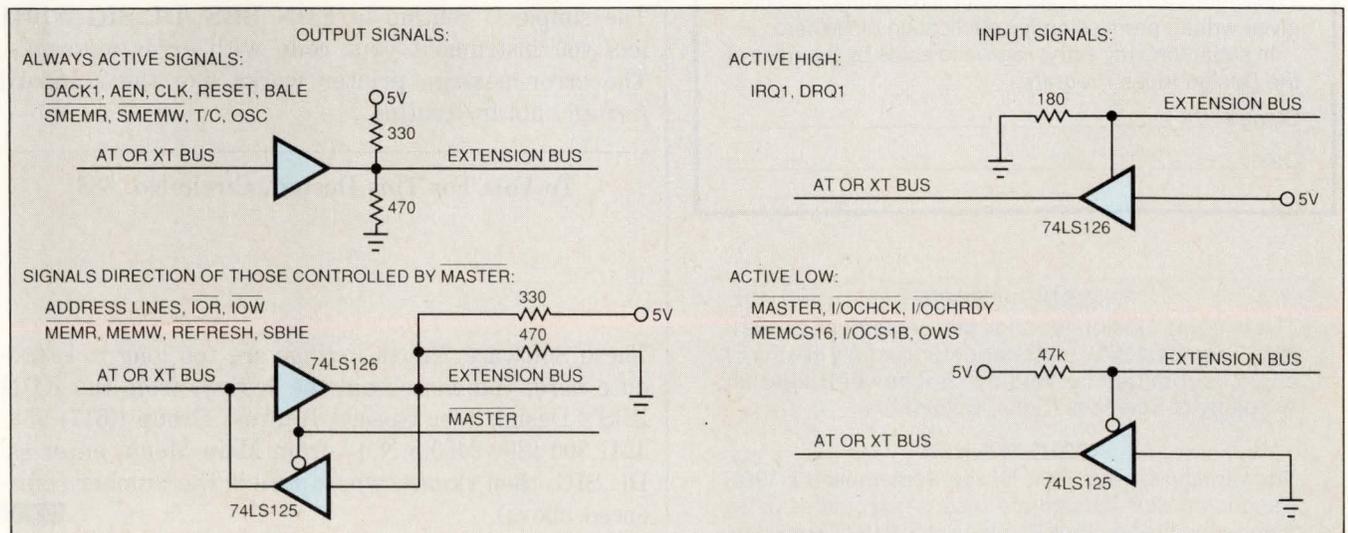
This design avoids conflicts between bidirectional signals on the PC and extension buses. The problem solves itself for both memory and I/O write cycles because writing data causes no complications as long as all bus devices have unique addresses. Read cycles are more complex. To read a device on the external bus, the output-enable pins of the bidirectional drivers must be enabled.

In **Fig 1** note that the 16-input AND gate will enable the bidirectional drivers if at least one data bit from an expansion-bus device is zero. If the expansion-bus device is not outputting data, the expansion-bus pullup resistors will disable the bidirectional drivers. If the expansion-bus device has to output FFFF<sub>HEX</sub>, the PC will read the PC-side pullup resistors as FFFF<sub>HEX</sub> anyway. **EDN BBS /DI\_SIG #1067** **EDN**

To Vote For This Design, Circle No. 746



**Fig 1**—With this simple extension-bus circuit and the drivers in **Fig 2**, you can add extra cards to your PC and provide isolation for experimentation. Note the 16-input AND gate, which handles extension-card data writes.



**Fig 2**—The four different types of PC bus signals each need a specific driver for the extension bus.

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### ISSUE WINNER

The winning Design Idea for the September 2, 1991, issue is entitled "DSP system comprises only five major chips," submitted by Valdimir Bochev of Bulgarian Academy of Sciences (Sofia, Bulgaria).

### ISSUE WINNER

The winning Design Idea for the September 16, 1991, issue is entitled "Temperature sensor produces pulse train," submitted by Jhoti Vandana of SEMP (Kalpakkam, India).

## SOFTWARE SHORTS

### 68HC05 acquires 16-bit pointers

Thomas R Hoover,  
*Valcom Inc, Roanoke, VA*

EDN BBS /DL\_SIG #1039 has assembly-language sub-routines, posted in an ASCII file, that let a 68HC05 access a 16-bit pointer for load and store operations. These routines prove handy now that the 6805 family members have large ROMs.

To Vote For This Design, Circle No. 686

### 8051 converts letters to upper case

Eric Watson,  
*Loral Hycor, Woburn, MA*

The 8051 single-chip- $\mu$ P assembly-language routine in EDN BBS /DL\_SIG #1040 inputs data from a  $\mu$ P port and tests for a lower-case, alphabetic ASCII character. If a character is lower-case alphabetic, the routine converts the character to upper-case ASCII.

To Vote For This Design, Circle No. 687

### C routine prints out error messages

Stephen Ho,  
*Hewlett-Packard, Milpitas, CA*

The simple C routine in EDN BBS /DL\_SIG #1041 lets you instrument your code with error messages. The error-message printer works like the standard *fprintf()* library routine.

To Vote For This Design, Circle No. 688

These Software Shorts *listings* are too long to reproduce here; you can obtain the *listings* from the EDN BBS's Design Idea Special Interest Group ((617) 558-4241,300/1200/2400,8,N,1—from Main Menu, enter ss/DL\_SIG, then rknnn, where nnn is the number referenced above).

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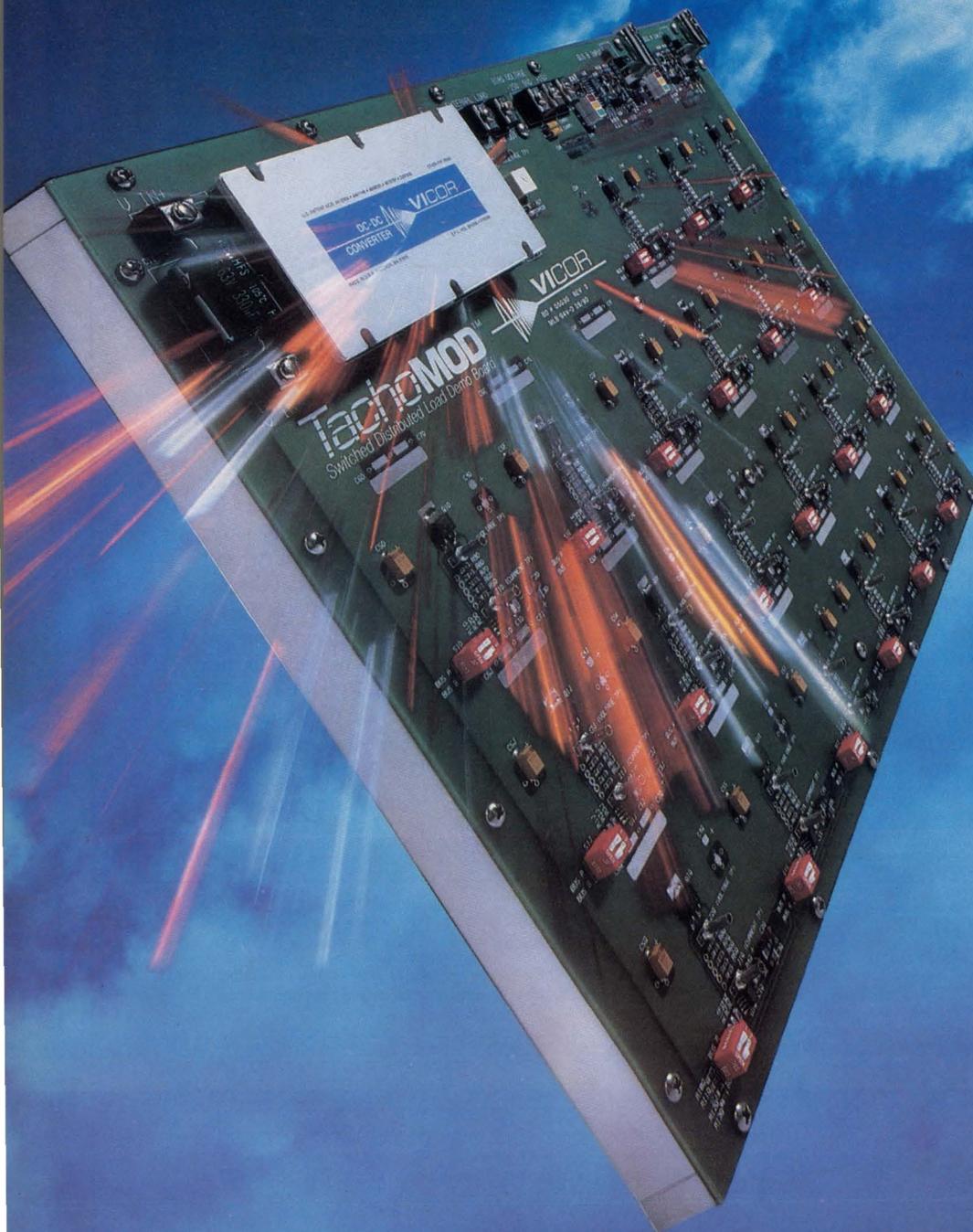
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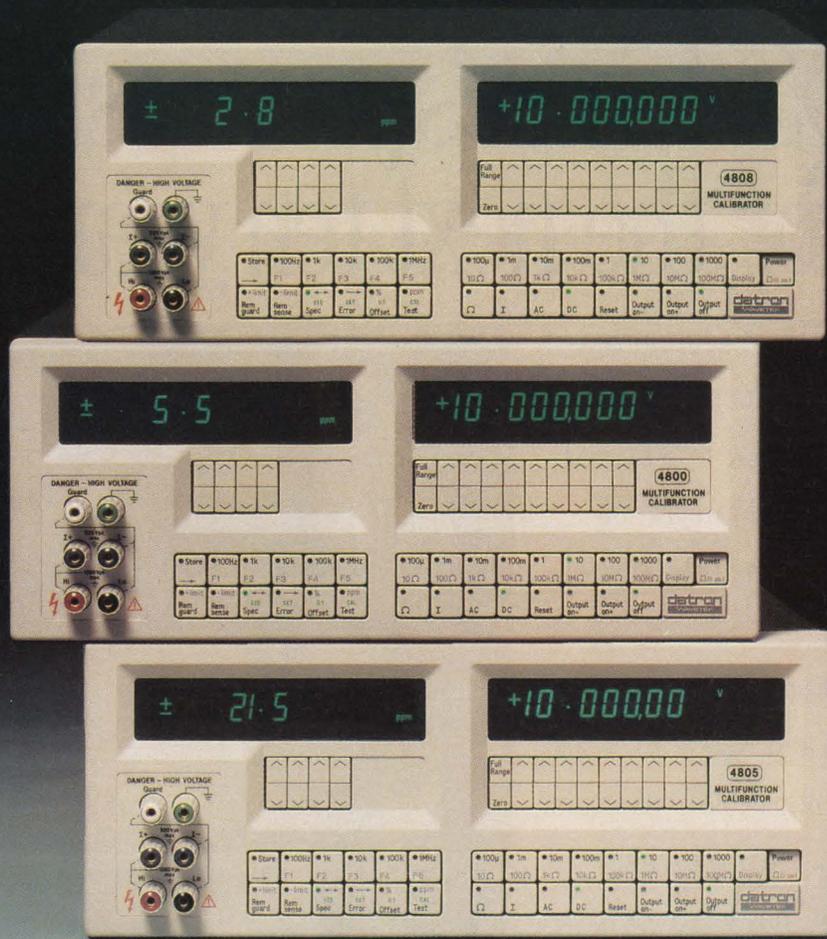
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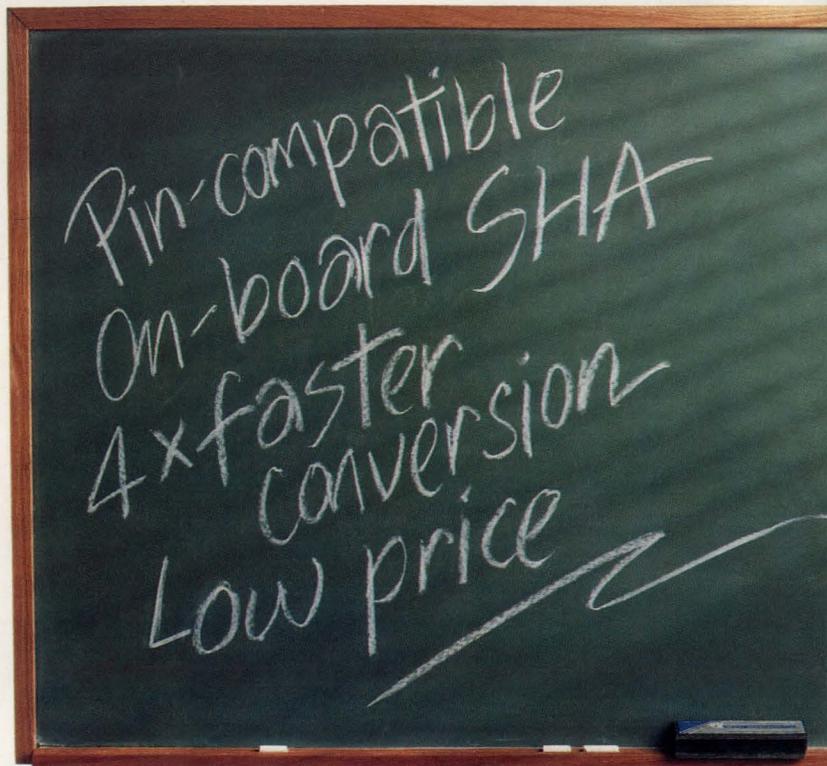
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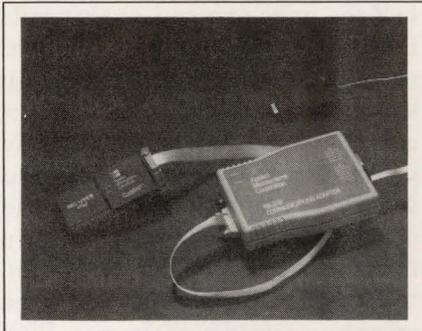
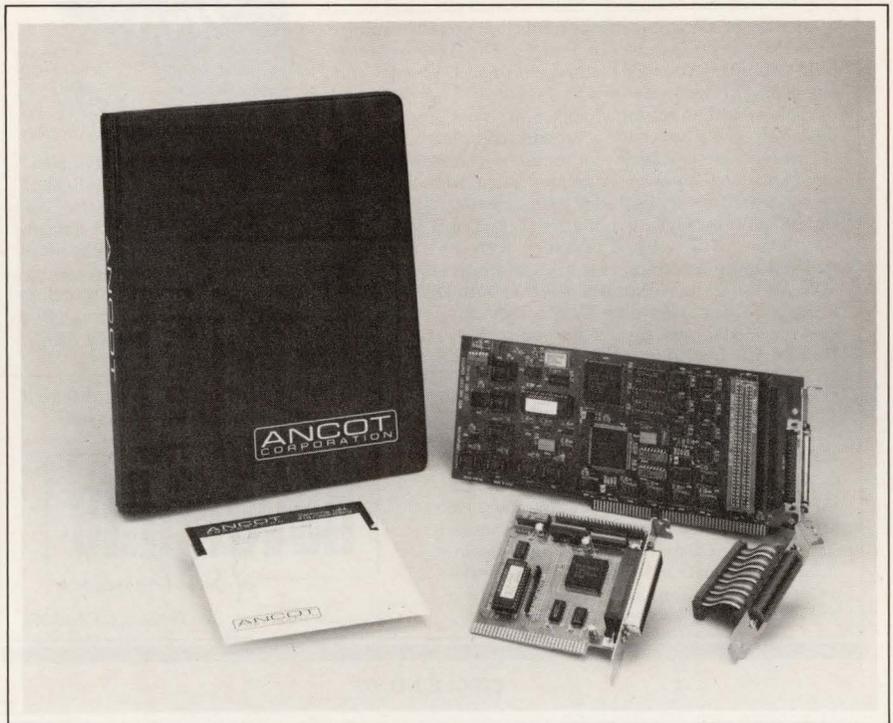
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- For runtime source-level debugging
- Support 80C186/C188EA, XL, EB, and EC  $\mu$ Ps

The Codetap C186/C188EA, XL, EB, and EC are development tools for the correspondingly named members of Intel's 80C186 and 80C188  $\mu$ P families. The hardware-based tools, which permit no-wait-state, 20-MHz operation of the target system, cost about 30% as much as full-featured, in-circuit emulators for these  $\mu$ Ps. This low cost suits

the tools for use by individual members of embedded-system-development teams. The tools work with Intel, Microsoft, and Microtec Research C compilers and include a windowed, source- and assembly-level debugger that runs under MS-DOS. \$5995.

**Applied Microsystems Corp**, Box 97002, Redmond, WA 98073. Phone (800) 426-3925; (206) 882-2000. FAX (206) 883-3049. TLX 185196.

Circle No. 352

### L64901 SPARC Development Tool

- Operates with the vendor's CLAS logic analyzers
- Supports 50-MHz versions of the IC, when available

The CLAS L64901  $\mu$ P-analysis package works with the vendor's CLAS family of configurable logic-analysis systems. The tool supports the LSI Logic L64901 SPARC  $\mu$ P. Currently, the fastest version of the

chip runs at 25 MHz, but when 50-MHz chips become available, the vendor expects the tool to support them. The tool configures the logic analyzer so that address, data, and control signals are grouped on the display. The display uses standard mnemonics and lets you represent addresses symbolically. You probe the surface-mounted IC by attaching a 5.3  $\times$  2.5  $\times$  1.3-in. card. \$4950; logic-analysis systems, from \$15,950.

**Biomation**, 19050 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 538-9320; (408) 988-6800. FAX (408) 988-1647.

Circle No. 353

### Analog I/O Card

- Plug into vendors' IEEE-488 mainframes
- Have programmable gain and 12- or 16-bit ADCs

The 2040 series 32-channel analog I/O modules plug into the vendor's 2200A family of IEEE-488 and serial-interfaced mainframes (chas-

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CIRCLE NO. 62

## INSTRUMENTS

sis). The cards incorporate 12- or 16-bit ADCs preceded by amplifiers that have gains you can program from  $\times 1$  to  $\times 500$ . The ADCs, which include S/H circuits, make 20,000 conversions/sec. To increase a system's channel capacity, you can add 32-channel analog-multiplexer cards. The multiplexer cards include a 12-bit DAC, a programmable-gain amplifier, and thermocouple cold-junction compensation. ADC cards, \$825 to \$1175; multiplexers, \$450 to \$750; 6-slot chassis, \$1095; 16-slot chassis, \$1595.

**Maxus Electronic Corp**, 2760 29th St, Boulder, CO 80301. Phone (800) 637-2832; (303) 447-1226. FAX (303) 447-1446. **Circle No. 354**

### 80386SX Emulator

- Runs at 16 MHz with no wait states
- Includes 512 kbytes of overlay RAM

The Codestalker 386SX in-circuit emulator sells for approximately half the price of many 32-bit emulators. It operates at 16 MHz with no wait states. The unit has 512 kbytes of overlay memory that you can split into two banks. Usually, you use bank 0 to define interrupt vectors in low memory (real mode) or to contain the interrupt descriptor table (protected mode). In bank 1, you can place data that, in normal operation, would go in the BIOS ROM. You can also configure the two banks as a single region of the  $\mu P$ 's memory. The emulator has four independent hardware breakpoints that you can set anywhere in the  $\mu P$ 's address space; you can also set an unlimited number of software breakpoints. The unit's trace buffer captures 4k machine cycles. The source-level debugger is compatible with many C compilers. \$9995.

**Softaid Inc**, 8300 Guilford Rd, Columbia, MD 21046. Phone (800) 433-8812; (301) 290-7760. FAX (301) 381-3253. **Circle No. 355**

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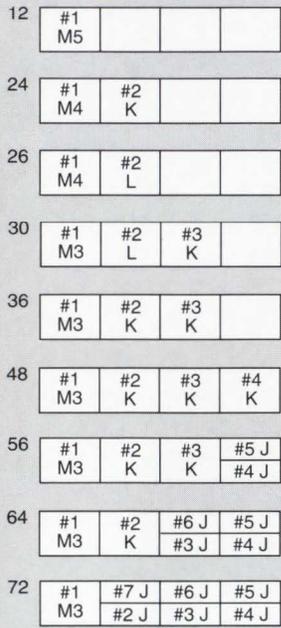


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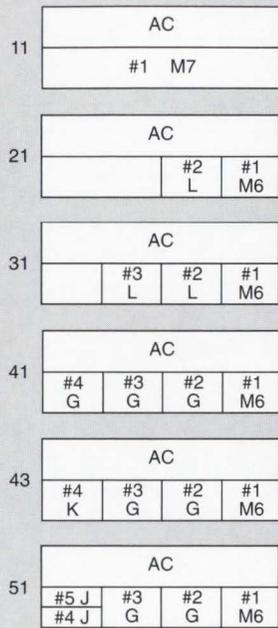
Call Toll Free 1-800-523-2332  
In PA: 215/699-9261

# OUTPUT LOCATIONS

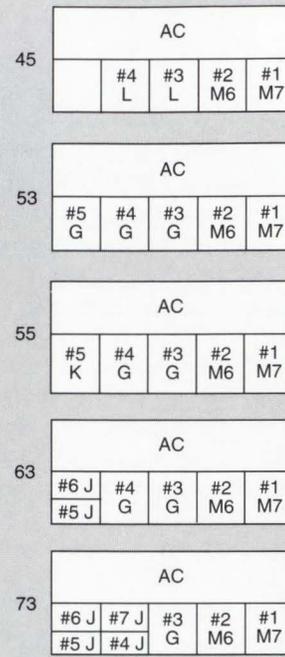
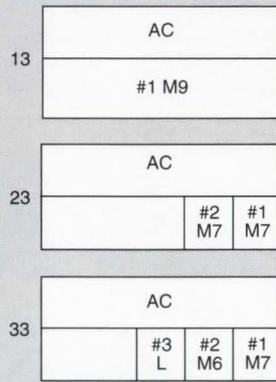
## 600 Watt FM Configurations



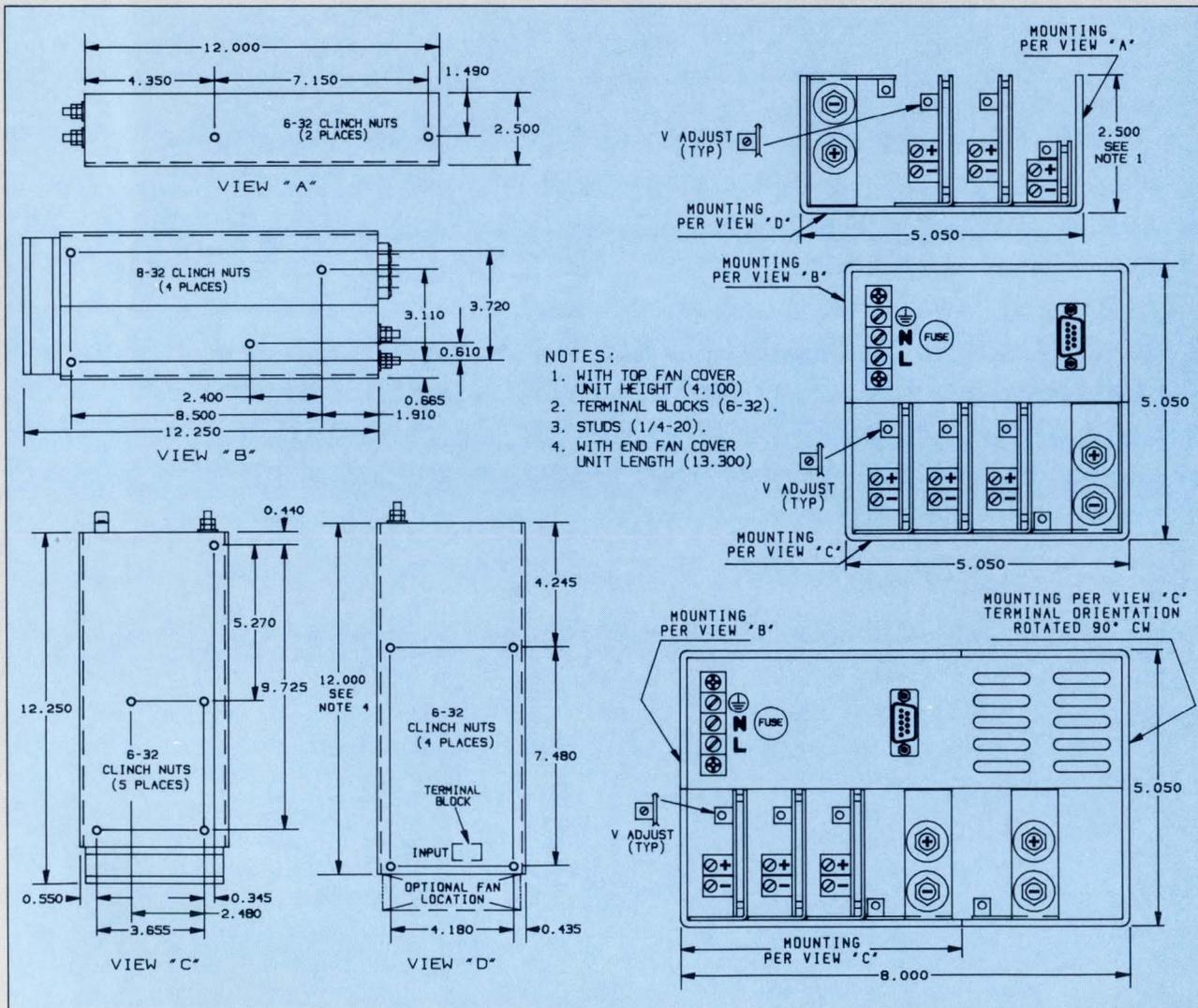
## 1000 Watt FM Configurations



## 2000 Watt FM Configurations



# FM SERIES DIMENSIONS



## DESCRIPTION

Moduflex switchers form a comprehensive line of open frame power supplies assembled from standard "off the shelf" modules. These subunits and assembly hardware are pre-approved by safety agencies so that certifications can automatically apply to custom models. Additional advantages include first piece delivery within two weeks and the elimination of engineering costs for qualified "OEM" requirements using stock modules.

FM Series are corrected to produce a 0.99 power factor. The resultant input current waveform is nearly a perfect sine wave compliant to the harmonic requirements of IEC 555-2.

Modular construction permits high volume manufacturing with an outstanding quality level and at competitive cost.

## FEATURES

- 0.99 power factor.
- 5 watts per cubic inch.
- 600-2000 watts output.
- 120 kilohertz design.
- TUV/VDE, UL, CSA.
- All outputs:
  - Adjustable*
  - Fully regulated*
  - Floating*
  - Overload and short circuit proof*
  - Overvoltage protected*
- Standard features include:
  - System inhibit*
  - Fan output*

## MODEL SELECTION

Input modules are available in ratings of 600, 1000, and 2000 watts with corresponding code letters of C, E and G. Refer to Power Code Table.

Output modules are available in ten types ranging in nominal power from 75 to 2000 watts. Refer to Output Code Table for codes and nominal power output.

Input Power Codes	
Codes	Watts
C	600
E	1000
G	2000

Output Codes	
Codes	Nominal Power
J	75
K	150
G	300
L	300
M3	400
M4	500
M5	600
M6	750
M7	1000
M9	2000

The Table of Ratings for the various types of output modules lists the maximum current for each type as a function of corresponding voltage rating.

Ratings in the shaded area are Preferred and are stocked for fast delivery.

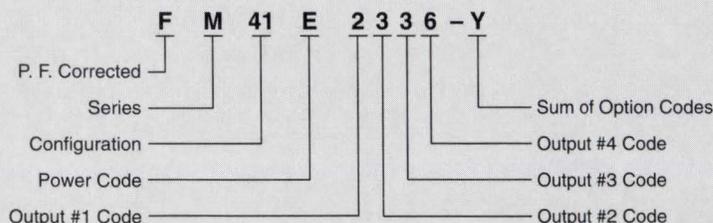
Note: When computing output load power, multiply the fraction of actual current to max. rated current by the nominal power rating of the output module.

## RATINGS OF OUTPUT MODULES

Nominal Power	75W	150W	300W	300W	400W	500W	600W	750W	1000W	2000W	
Code	Volts	J	K	G	L	M3	M4	M5	M6	M7	M9
0	2	10	20	20	30	80	100	120	150	200	400
1	3.3	10	20	20	30	80	100	120	150	200	400
2	5	10	20	30	30	80	100	120	150	200	400
3	12	6	12	20	24	34	42	50	62	84	168
4	15	5	10	20	20	26	33	40	50	67	134
5	18	4	8	16	16	22	28	33	42	56	112
6	24	3	6	12	12	17	21	25	31	42	84
7	28	2.5	5	10	10	14	18	21	27	36	72
8	36	2	4	8	8	11	14	17	21	28	56
9	48	1.5	3	6	6	8	10	12	16	21	42

## HOW TO ORDER

Select the letter F for power factor correction, then select the letter M to designate the series. Choose the desired configuration of output modules and list the configuration code. Insert the power code letter and follow with the output code numbers for each individual output. Enter a dash and from the option table insert the sum of the option codes. See example below.



OPTIONS	
Option Code	Function
1	Power Fail Monitor
2	Cover (600W only)
4	End Fan Cover (600W only)
8	Top Fan Cover (600W only)

# SPECIFICATIONS

## INPUT

90-264 VAC, 47-63 Hz.  
190-264 for 2000W units.

## POWER FACTOR

0.99 at full load.

## HARMONIC CURRENTS

Compliant to IEC 555-2.

## INPUT SURGE

230 VAC – 75A max.  
115 VAC – 40A max.

## HOLDUP TIME

20 milliseconds from loss of AC power.

## OUTPUTS

See model selection table.

## ADJUSTABILITY

±5% trim adjustment.

## OUTPUT POLARITY

All outputs are floating from chassis and each other and can be referenced to each other or ground as required.

## LINE REGULATION

Less than ±0.1% or ±5mV for input changes from nominal to min. or max. rated values.

## LOAD REGULATION

±0.2% or ±10mV for load changes from 50% to 0% or 100% of max. rated values.

## MINIMUM LOAD

Main output requires a 10% minimum load for full output from auxiliaries. Main output is #1 on 600W and 1000W units and #2 on 2000W units.

## REMOTE SENSING

On all outputs except type J modules.

## RIPPLE & NOISE

1% or 100mV pk-pk, 20 MHz bandwidth.

## OPERATING TEMPERATURE

0-70°C. - Derate 2.5%/°C above 50°C.

## COOLING

A min. of 10 LFS cooling air directed on cooling surfaces over the 600W units for full rating. Two test locations on chassis rated for max. temperature of 90°C. 1000W and 2000W models have built-in ball bearing fan.

## TEMPERATURE COEFFICIENT

±0.02%/°C.

## EFFICIENCY

70% to 80%.

## SAFETY

Units meet UL 1950, CSA 22.2 No. 234, IEC 950, EN 60 950, VDE 0804, VDE 0805, VDE 0806. Certifications in process.

## DIELECTRIC WITHSTAND

3750 VRMS input to ground.  
3750 VRMS input to output.  
700 VDC output to ground.

## SPACING

8 mm primary to secondary.  
4 mm primary to grounded circuits.

## LEAKAGE CURRENT

3.5mA max.

## EMISSIONS

Units meet FCC 20780 Part 15 Class A and VDE 0871 Class A for conducted emissions. Compliance with Class B limits by use of additional external filter.

## DYNAMIC RESPONSE

Peak transient less than ±2% or ±200mV for step load change from 75% to 50% or 100% max. ratings.

## RECOVERY TIME

Recovery within 1%.  
M3, M4, M5, M6, M7, and M9 modules – 200 microseconds.  
J, K, G, and L modules – 500 microseconds.

## UNDERVOLTAGE

Protects against damage for undervoltage operation.

## OVERVOLTAGE PROTECTION

Standard on all outputs.

## REVERSE VOLTAGE PROTECTION

All outputs are protected up to load ratings.

## OVERLOAD & SHORT CIRCUIT

Outputs protected by duty cycle current foldback circuit with automatic recovery. Auxiliaries have additional backup fuse protection.

## THERMAL SHUTDOWN

Circuit cuts off supply in case of local over temperature. Units reset automatically when temperature returns to normal.

## SOFT START

Units have soft start feature to protect critical components.

## FAN OUTPUT

Nominal 12 VDC @ 12 watts maximum.

## INHIBIT

TTL compatible system inhibit provided.

## SHOCK

MIL-STD 810-D Method 516.3, Procedure III.

## VIBRATION

MIL-STD 810-D Method 514.3, Category 1, Procedure I.

## MECHANICAL

600W – Case 1. – 2.5 x 5.05 x 12  
1000W – Case 2. – 5.05 x 5.05 x 12  
2000W – Case 3. – 5.05 x 8 x 12

## POWER FAIL MONITOR

Optional circuit provides isolated TTL and VME compatible power fail signal providing 4 milliseconds warning before main output drops by 5% after an input failure.

## FAN COVER

Optional covers with brushless DC ball bearing fan which provides the required air flow for full rating of 600W units. Choice of low profile or top mounted types.

Specifications subject to change without notice.



290 WISSAHICKON AVENUE, P.O. BOX 1369, NORTH WALES, PA 19454  
PHONE: 215/699-9261 • FAX: 215/699-2310

Int'l. Units: Delaire • Sallynoggin Road, Dun Laoghaire, Co. Dublin, Ireland. Tel: + 353-1-2851411 • FAX: + 353-1-2840267  
Delinc • Padre Mier y Dr. Mina, Reynosa, Tamps., Mexico 08866. Tel.: (892) 38723 Prefix – from USA – (01152) FAX: (892) 38776

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# NEW PRODUCTS

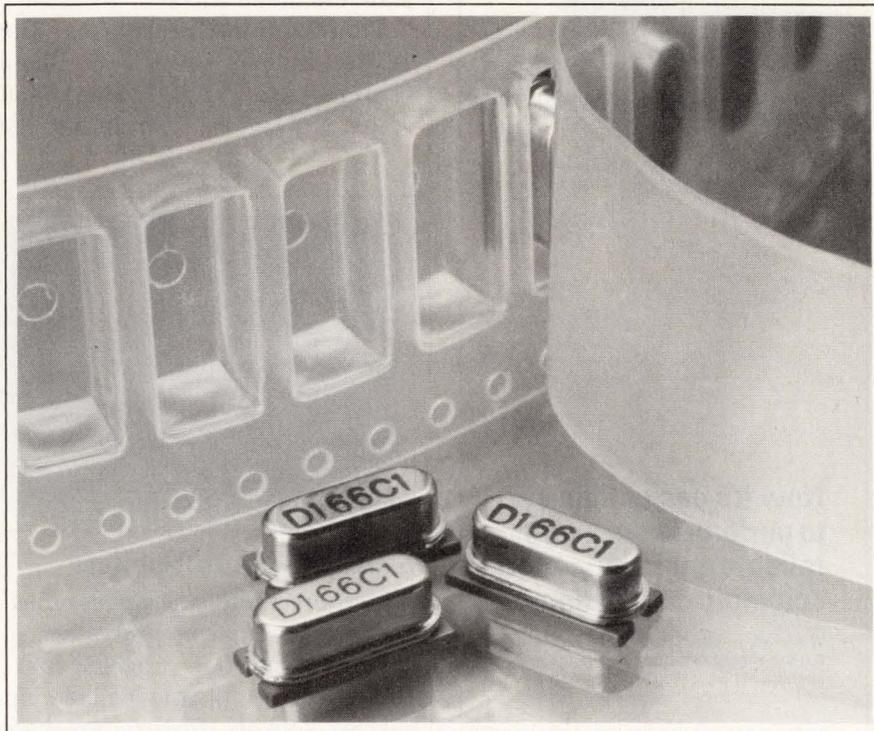
## COMPONENTS & POWER SUPPLIES

### Clock Oscillator

- Is surface mountable
- 5 mm high

The SO-49 crystal clock oscillator is compatible with HCMOS, CMOS, and TTL. The unit is housed in a hermetically sealed, resistance welded 3-leaded SIP, which measures only  $4.5 \times 11.8 \times 5$  mm. Output frequencies range from 625 kHz to 50 MHz, with frequency tolerance measuring  $\pm 50$  ppm. Rise and fall times equal 50 nsec max below 2 MHz and 20 nsec max above 2 MHz, respectively. Output symmetry equals 45 to 55%, and operating range spans  $-10$  to  $+70^\circ\text{C}$ . The oscillator operates with a single 5V supply. \$2.50 to \$3 (1000)

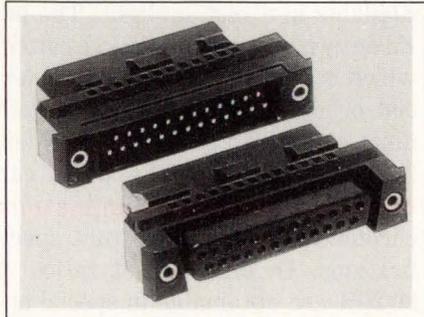
**KDS America**, 10901 Granada Lane, Overland Park, KS 66211. Phone (913) 491-6825. FAX (913) 491-6812. **Circle No. 363**



### Hybrid Connector

- Designed for pc boards
- Rated for 5A

The Model DSEB hybrid connector combines the advantages of D-subminiature and edge board designs. It's rated for 5A, and you can use it with any pc board requiring a D-subminiature connector. Available in a 25-contact version, the connector accommodates boards ranging from 0.054 to 0.071 in. thick



and measures  $2.072 \times 0.5$  in. on the D-subminiature side and  $1.588 \times 0.35$  in. on the edge board side. Design features include a molded hous-

ing for accurate pin-socket alignment and selective gold plating (contact areas) to minimize cost. The connector has a built-in locking nut. \$2.58 (500).

**Dale Electronics Inc**, Box 609, Columbus, NE 68602. Phone (605) 665-9301. **Circle No. 364**

### Optical Connector

- For applications requiring high reflectance
- Features a 0.5-dB loss

The ST II fiber-optic connector is designed for applications where high reflectance is required. An angled ceramic ferrule, which incorporates the protruding fiber polisher, ensures a higher return loss than that found in standard ST connectors. Median maximum reflectance is  $-60$  dB. When terminating 8.3/125- $\mu\text{m}$  single-mode fiber, the connector has a 0.5-dB insertion loss. The connector measures  $2.14 \times 0.375$  in. and is well suited for dense

panel arrangements. Connector couplings feature a keyed, bayonet latch and are easy to connect and disconnect. The metal couplings come in flanged, threaded, and floating configurations; plastic versions are available in threaded designs. \$48.

**AT&T Network Cable Systems**, 111 Madison Ave, Morristown, NJ 07962. Phone (201) 606-4266.

**Circle No. 365**

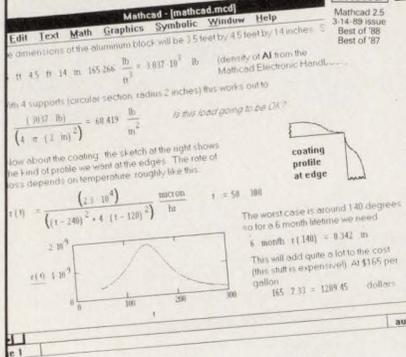
### Coaxial Attenuator

- Rated for 100W
- Operates to 1.5 GHz

The PE7021 50 $\Omega$  coaxial attenuator operates over a frequency range of dc to 1.5 GHz and offers attenuation values of 6, 10, 20, and 30 dB. The device's average power-handling capability is 100W, and it can handle a peak of 10 kW max. Maximum VSWR is rated at 1.15:1. The attenuator comes in a package featuring an extruded, black anodized alu-

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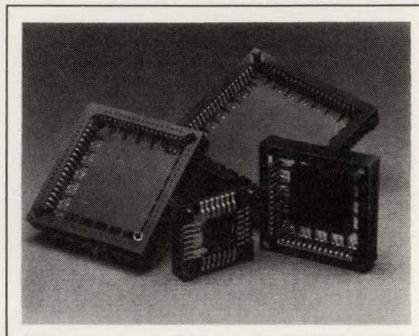
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## COMPONENTS & POWER SUPPLIES

minum heat sink and a type N connector that's made of passivated stainless steel. \$350.

**Pasternack Enterprises, Box 16759, Irvine, CA 92713. Phone (714) 261-1920. FAX (714) 261-7459.**

Circle No. 366



### Surface-Mount Sockets

- Accommodate vapor-phase and infrared-soldering processes
  - Offer 84-position capacity
- PLCC Series plastic-leaded-chip-carrier sockets feature precision stampings, high-temperature plastic construction, and a body design that has the same board footprint as the chip carrier itself. The liquid-crystal polymer housing accommodates vapor-phase and infrared soldering, and the open construction simplifies inspection of every solder fillet. The sockets are available in 28-, 32-, 44-, 52-, 68-, and 84-lead versions. The solder tails have a slot in the tail for added solder adhesion. The contact design places downward pressure on the PLCC so it remains in the socket. From \$1.60 (1000).

**Samtec Inc, Box 1147, New Albany, IN 47151. Phone (800) 726-8329. FAX (812) 948-5047.**

Circle No. 367

### Power Supply

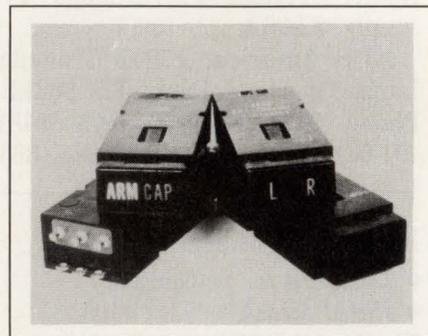
- Has a universal input
- Develops 50W

The PSA-5231 power supply is designed for international applications and features an input that continuously covers a 100 to 240V range.

An on/off switch, an IEC ac connector, and a Class B EMI filter are all housed in a 6.77 x 3.15 x 1.89-in. case. The supply develops outputs of 5V at 4A, 12V at 2A, and -12V at 0.5A. Noise and ripple are held to less than 1% of rated output. All outputs feature a load and line regulation of 2%. EMI specs are in accordance with Class B requirements of both VDE and FCC. The supply meets the safety requirements outlined in UL 1950, CSA 1402C, and VDE 0805. \$50 (100). Delivery, stock to eight weeks ARO.

**Phihong USA, 920 Hillview Ct, Suite 195, Milpitas, CA 95035. Phone (408) 263-2200. FAX (408) 263-2213.**

Circle No. 368



### Pushbutton Switches

- Feature illuminated display
- Are sunlight readable

Avionics switches and indicators come in full- and split-screen versions with either T-1 or T-1¾ lamps, which you can replace from the front of the panel. The switches are readable in direct sunlight. The basic design uses a snap-action switch, which is available in either commercial or military versions. The spdt units come with pc-board or solder-lug terminations. The units can meet a variety of illumination, chromaticity, and dead-front specifications. On/off contrast ratios of 80/20% are obtainable in special applications. From \$20. Delivery, 8 to 10 weeks ARO.

**Eaton Corp, 4201 N 27th St, Milwaukee, WI 53216. Phone (414) 449-6000.**

Circle No. 369



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Whatever the telecom product, when you seriously consider your options in passive components, you'll see we can make a difference.

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There's always individual component cost, a comparison we at Murata Erie heartily encourage. But if you stop there, you could overlook some other very important distinctions.

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any type passive your product requires.

Now consider supplier capacity. Look at our multiple plants in North America and overseas. And ask yourself what other company could routinely ship, for example, 3.5 billion ceramic capacitors per month. Or match our network of local distributors—people ready to respond not only with product but with technical expertise as well.

Finally, try to find a company with more experience. You might begin by asking

who pioneered, and continues to pioneer, electro-ceramic technology, the core of numerous electronic sub-technologies ranging from dielectrics to piezoelectrics.

All that done, we think you'll find choosing the right passive component line a simpler task. Getting started is even easier. Write or call us today. We'll show you how, for telecom OEMs, we're making things a lot better. And how we'll do the same for you.

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Tango-Schematic is the front end of the popular Tango family of PC-based electronic design software. Users execute all common functions in the same way with Tango's easy-to-use, "Windows™-like" interface. Tango takes an integrated approach to design, with sheet and component creation, post processing and hard copy generation, all executed from a single program. Our two-level menus, dialog boxes, on-line help and macro support make Tango quick to learn and simple to use.

Tango-Schematic gives you versatility and functionality with: support of homogeneous and heterogeneous components; library search and browses; autopanning and unlimited zoom levels; display of hidden pins to enable splitting power and ground nets; copy commands; and use of a unique snap-to-pin feature for guaranteed wire-to-component connections. Post-processing features include: forward and back annotation, design rule checking and sheet cleanup. Tango, EDIF 2.0, PSpice,™ P-CAD™ and other popular net list formats are supported.

Tango-Schematic's extensive device libraries are provided by SEDCO (specialists in creating electronic design libraries) and contain over 10,000 different symbols each verified for accuracy and each available in its commercial, true ANSI/IEEE and DeMorgan representation.

Make sure you're using the best tools available and experience the Tango difference. Call us toll free for more information or to request your free, functional evaluation package.

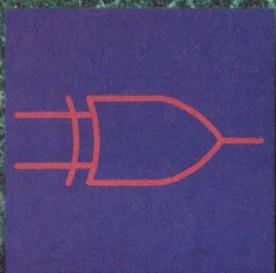


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CIRCLE NO. 68



# WHEN YOU PLUNGE INTO ASIC DESIGN, YOU WANT SUPPORT TOOLS THAT WORK.

## Oki's Advanced ASIC Tools Reduce Your Risk.

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Oki's advanced tools provide the lift you need to dive comfortably into high-level ASIC design:

**Timing-driven layout** - for an improved design-to-silicon match.

**Clock tree structures** - for optimized clock distribution.

**Power calculator** - for increased overall system reliability.

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So take the plunge. Call 1-800-OKI-6388, Dept. 050, for Oki's ASIC capabilities brochure. See how risk-free ASIC design can be.



### Oki ASIC Design Tool Support for 0.8 $\mu$ m, 1.0 $\mu$ m, & 1.2 $\mu$ m

Vendor	Platform	Operating System/Application
Cadence	Sun/Solbourne	Verilog: Simulation, fault grading, design verification
IKOS	IKOS	Simulation, fault grading
Mentor Graphics	HP/Apollo Sun/Solbourne	Design capture, simulation Parade: Layout, clock and timing structures
Synopsys	Sun-4 Interface to Mentor, Valid, Viewlogic	Design synthesis, test synthesis
Valid	Sun/Solbourne DECstation 3100 IBM RS6000	Design capture, simulation Design check GED, ValidSIM, RapidSIM
Viewlogic	Sun-4 PC386	Design capture, simulation Design check



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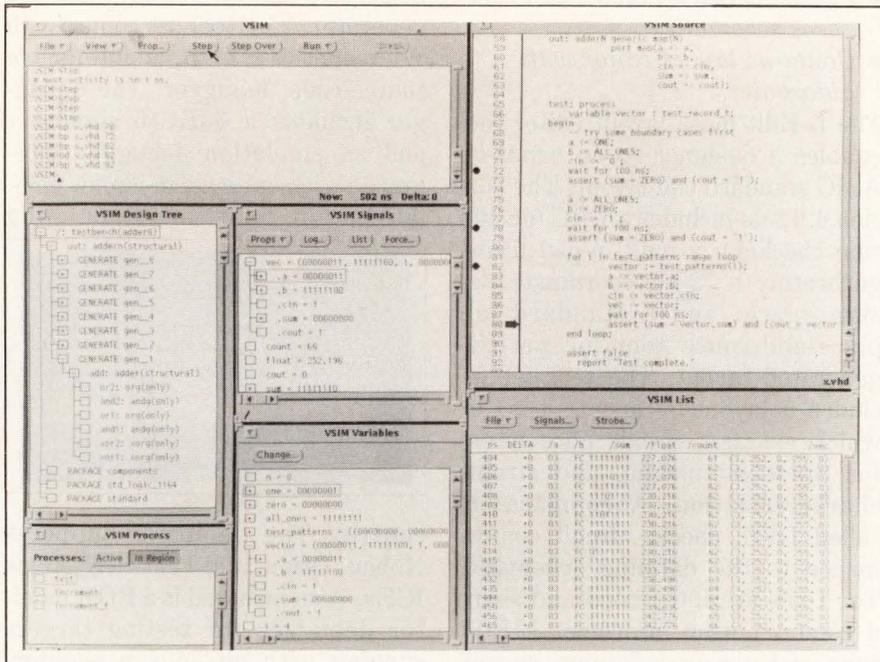
# NEW PRODUCTS

## CAE & SOFTWARE DEVELOPMENT TOOLS

### VHDL Development System For SPARCstations

- VHDL simulator and compiler
- Interactive VHDL source code debugger

V-System/SPARC is a VHDL (VHSIC Hardware Description Language) development system for the Sun SPARCstation platform. Engineers can offload their high-end VHDL development tools for initial development and verification. Subsystems can be defined and tested before integration on high-end development tools. The V-System/SPARC is integrated under Sun's Open Windows. The development environment provides six interactive windows. These windows enable users to view their design hierarchy, scroll through their VHDL source, monitor selected debugging variables and signals, control the simulator, and see the executing processes and the simulator output. You can set VHDL breakpoint directly in the code, single



step, and change values on the fly. Compile times are pegged at 15,000 lines/minute and simulation, at 10,000 RTL statements/sec on a Sun IPC. Single-user license, \$4995; for DOS and Win-

dows, \$495 and \$1995, respectively.

**Model Technology Inc**, 15455 NW Greenbrier Pkwy, Suite 210, Beaverton, OR 97006. Phone (503) 690-6838. FAX (503) 690-2093.

Circle No. 356

### Simulation Verification And Analysis Tool

- Verifies results for different simulations
- Compares behavioral and gate-level simulation

The VCAP tool enables engineers to compare different simulation runs and detect differences in performance. You can compare a simulation run against expected results, having the differences flagged for easy reference. These comparisons let you detect differences between design iterations or performance between a behavioral model and a gate-level implementation. It also detects variations between different synthesis runs on a circuit. VCAP also has a mode for timing and pin behavior, producing a report listing minimum and maximum output-pin delays, pin-transition

statistics, and input behavior. Also listed are the tester resources required to run the test vectors. VCAP runs on Sun, HP, Intergraph, and IBM PC/AT workstations. Single node license, \$3995.

**Source III Inc**, 3958 Cambridge Rd, Suite 247, Cameron Park, CA 95682. Phone (916) 676-9329.

Circle No. 357

### Unix/DOS X-Window Servers

- X-Server for 386/486 supports TIGA boards
- For DOS and SCO or Interactive Unix

X-Windows-applications users can take advantage of the TIGA (TI graphics architecture) PC graphics standard with X Servers. You can use PCs as applications servers, providing an X-Windows interface

for applications running on X-Window clients. Software for TIGA/DOS release 2.1 supports the TIGA graphics board, based on the TI 34020 graphics accelerator boards. This version supports DOS 5.0 as well as third-party networking software that links to other PCs or high-end servers. The company is also releasing Xoftware for PC Unix, release 2.1. It supports both SCO and Interactive Unix operating systems for PCs. TIGA graphics boards support workstation class resolutions: monochrome resolutions to 1600x1200 and color resolutions to 1280x1024. Software for TIGA/DOS and PC Unix, \$595 and \$495, respectively.

**AGE**, 9985 Pacific Heights Blvd, Suite 200, San Diego, CA 92121. Phone (619) 455-8600. FAX (619) 597-6030.

Circle No. 358

**ASIC Standard-Cell Layout Editor**

- System extracts layouts and compares schematics
- Contains layout editor with autorouter

The L-Edit mask-layout editor tool enables a designer to do hands-on ASIC standard cell layout. The version 4.0 tool includes a DRC (design rule checker), a built-in-pad frame generator, a 32-bit coordinate design space, and a standard-cell place-and-route tool for netlist-generated layout. The tool set includes a layout-to-Spice extractor, which extracts circuit parameters for Spice simulation and circuit characterization. A comparator, called LVS, checks circuit conformance to the defining schematic. The tools are integrated and share a common user interface. L-Edit runs on Unix workstations, as well as on IBM PCs and Apple Macintosh computers. Both CIF and GDS-II layout database formats are supported by L-Edit. The tool supports fully scalable CMOS digital and analog circuits. It handles hierarchical, cell-based design, with unlimited layers and hierarchy levels. It supports all-angle, 45°, and 90° polygons and wires. Basic L-Edit layout editor, from \$995; extractor, \$995; layout vs schematic comparator, \$995.

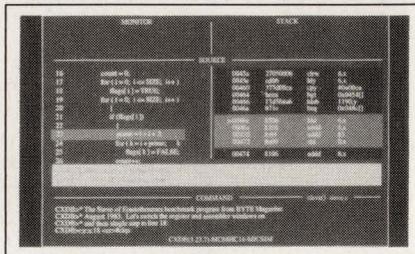
**Tanner Research Inc**, 444 N Altadena Dr, Pasadena, CA 91107. Phone (818) 795-1696. FAX (818) 795-7937. **Circle No. 359**

**Software-Development Tools For Motorola 68HC16**

- ROMable cross assembler and compiler
- Source-code debugger, ANSI runtime library

This tool set works with Motorola's 68HC16, a 16-bit microprocessor. The tool set includes an ANSI C cross-compiler, a macro assembler, and an ANSI runtime library. It also includes a set of programming

utilities: a linker, librarian, automatic data initializer, object-module inspector, and an absolute hex file generator. The tool set comes with Whitesmith's CXDB, an interactive source-code debugger. The debugger includes a 68HC16 simulator and an emulation debugger integrated with external in-circuit emulators for real-time debugging



control. The debugger supports Nohau, Orion, and Pentica Systems ICEs. Also included is a ROM monitor debugger for testing targets running with an on-chip monitor. The debugger works with standard Motorola evaluation boards. The development package runs on IBM PCs and clones, as well as on Sun, DEC/VAX, and HP workstations. Compiler/assembler/utilities package for a PC, \$1600. CXDB debugger, \$1500.

**Intermetrics Microsystems Software Inc**, 733 Concord Ave, Cambridge, MA 02138. Phone (617) 661-0072. FAX (617) 868-2843.

**Circle No. 360**

**Forth Development System For 68332 Microcontroller**

- Forth system with PROM support
- Includes a Motorola 68332 evaluation-kit board

Chipforth, for the Motorola 68332 32-bit microcontroller, is a PC-based Forth development system and a 68332 target board with a minimized Forth kernel. The board is actually the Motorola 68332 evaluation kit with 2 kbytes of on-chip RAM, 64 kbytes of board RAM (32k x 16 bits), an RS-232C (64 baud to 524 kbaud), a parallel-port host

communications link, and sockets for EPROMS and static RAM. The host Polyforth system is tightly coupled with the target operating software, which is a Forth subset. This coupling makes it easy to control and debug running target software. The target has a small 200-byte talker program, which links processors and supports interactive debugging. Utilities include a full screen editor, PROM programming support, debug utilities, a target-memory dumper, and disk/print utilities. Chipforth, \$3950, including one year of telephone support.

**Forth Inc**, 111 N Sepulveda Blvd, Manhattan Beach, CA 90266. Phone (213) 372-8493. FAX (213) 318-7130. TLX 275182.

**Circle No. 361**

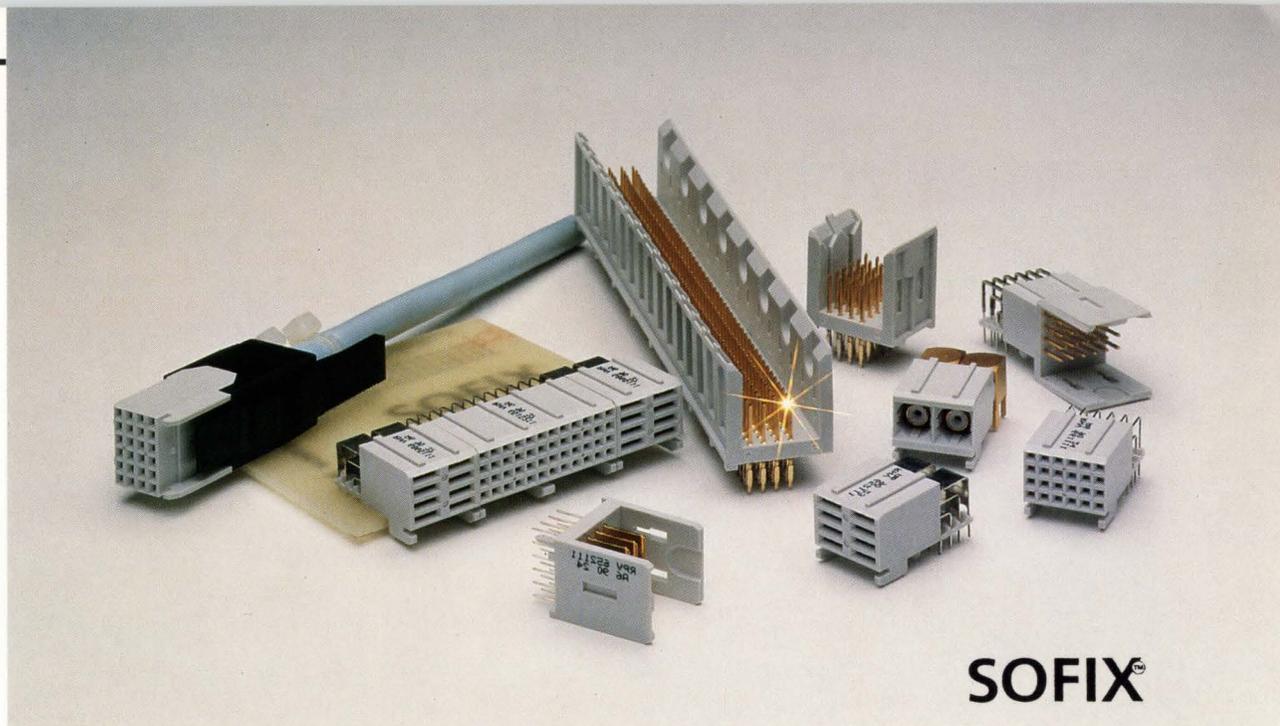
**C++/C Development Environment For Sun**

- C/C++ compiler, debugger, and editor
- Project-oriented environment

The C++/Softbench development environment for Sun workstations combines an ANSI C and C++ (version 2.1) 1-pass compiler with the underlying Softbench tool integration base. Softbench sets up a low-overhead communications mechanism for integrating development tools and provides encapsulation mechanisms for common user interfaces. With C++ Developer, users can generate a source-code template from a class for building a new instance or subclass. Softedit editor provides syntax and semantic error checking before compile time. And, Softdebug supports object-oriented debugging. Available in February, 1992, \$9950 per seat.

**Hewlett-Packard Co**, 19310 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 752-0900; (408) 746-5601. FAX (408) 746-5780.

**Circle No. 362**



## 2MM INTERCONNECTION

- \* Modularity
- \* High Density
- \* Flexibility
- \* Standardization

A NEW HIGH DENSITY modular interconnection system Sofix, based on 2mm Pin spacing, is BORN.!

### MODULARITY

- \* Stackable segments; 12, 24, 48 & 96 mm Lengths.
- \* Easy-to-assemble w/Hot Riveting tool.
- \* No unused slots at end of modules.

### HIGH DENSITY

- \* Four rows of 2 mm spacing achieves 100% more density than DIN-41612 (Euroconnector).

### FLEXIBILITY

- \* Mix signal, power coax & fiber-optics side-by-side; independent of the module size.

### STANDARDIZATION

- \* SOFIX has been standardized by IEEE 1301.1, IEC917 and accepted by FUTUREBUS+ and SCI Bus EIA IS64.

## MOUNTING & TOOLS



### HOT RIVET

\* Hot Riveting tool: To obtain END-TO-END stacking, the 90° connector is riveted from the PCB's rear side, by a plastic mounting peg which gives the connector a firm fit. The Hot Riveting tool is a very slim unit that can be modularized; 1 to 20 rivets at once.



### PRESS-FIT

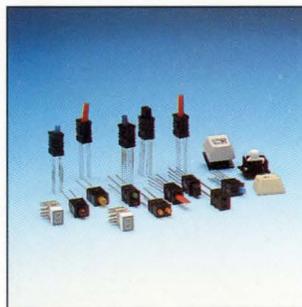
\* The Pin connectors for backpanels are available for both solder-to-board or pressfit. Tools for pressfit connectors are available as a BENCHPRESS, for small series; or Automatic Pneumatic Press, for full production.



### IDC

\* The Cable connectors are designed with IDC (INSULATION DISPLACEMENT CONNECTION) for ease of assembly. Hand tools for lab or field assembly is available, as well as Semi-automatic units for full production.

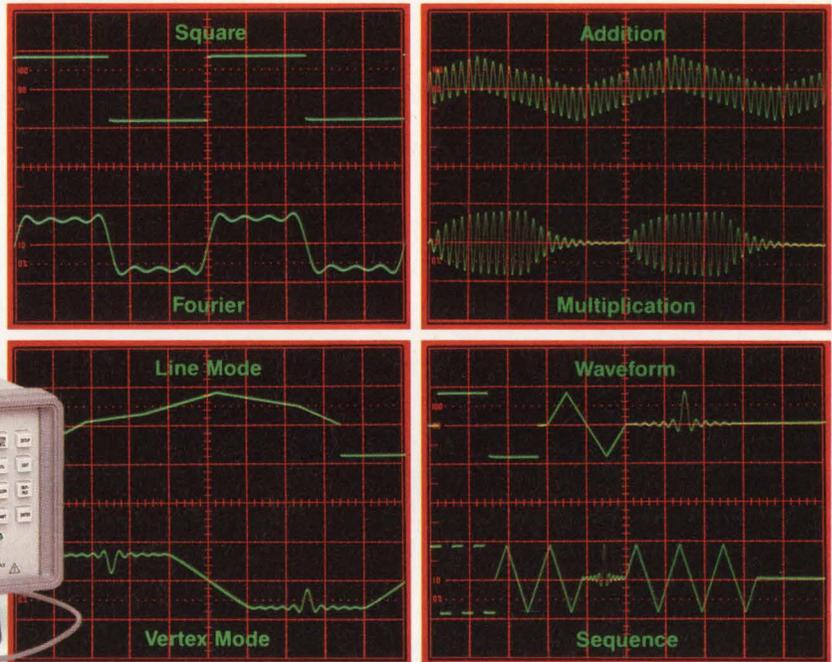
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am scm fm hsin
slin slo9 flst fls-
gaus sx/x circ nois
    
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All waveforms are digitally synthesized, with 12 bits (4095 points) of amplitude resolution and 32K of waveform memory. And the synthesized internal clock up to 20 MHz provides a wide range of output frequencies.

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Twenty standard waveshapes are preprogrammed for instant recall and modification. And you can create your own custom waveshapes – and store up to 100 – using Pragmatic's innovative line segment and vertex "draw" modes. An optional mouse makes it even

easier. And the intuitive, menu-driven display makes the 2202A extremely easy to operate.

### Optional Sequence Generator

Many different waveforms can be repeated and linked in any order for unprecedented versatility.

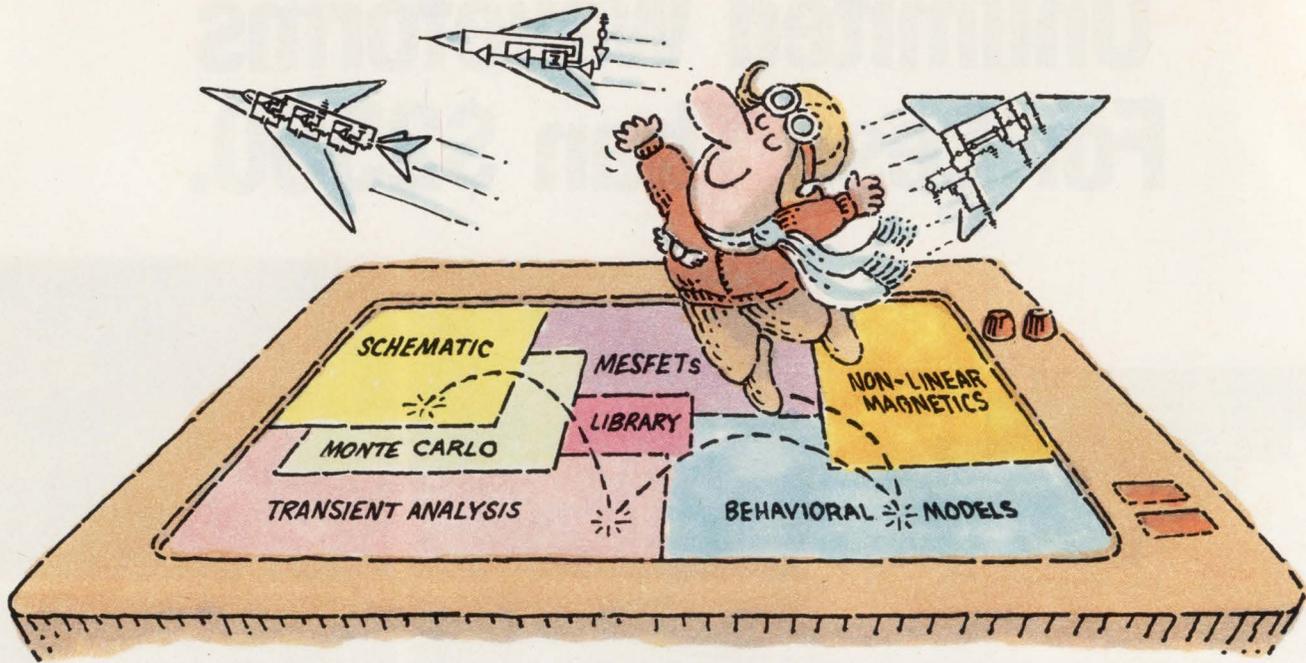
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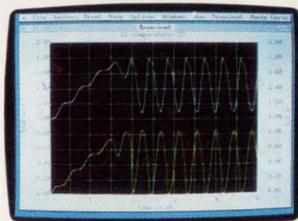
# THE NEW MICRO-CAP III.<sup>TM</sup> SO YOU CAN TEST-FLY EVEN MORE MODELS.

It wasn't easy. But we did it. Made the long-time best-selling IBM® PC-based interactive CAE tool even better.

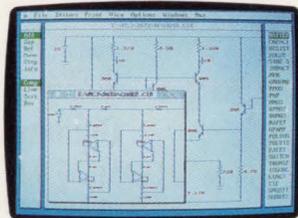
Take modeling power. We've significantly expanded math expression capabilities to permit comprehensive analog behavioral modeling. And, beyond Gummel Poon BJT and Level 3 MOS, you're now ready for nonlinear magnetics modeling. Even MESFET modeling.

Analysis and simulation is faster, too. Because the program's now in "C" and assembly language. That also means more capacity — for simulating even larger circuits.

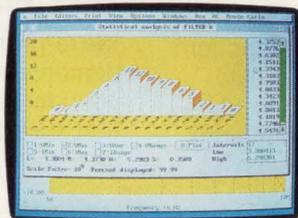
As always, count on fast circuit creation, thanks to window-based operation and a schematic editor. Rapid, right-from-schematics analysis — AC, DC, fourier and transient — via SPICE-like routines. The ability to combine digital/analog circuit simulations using integrated switch



*Transient analysis*



*Schematic editor*



*Monte Carlo analysis*

models and parameterized macros. And stepped component values that streamline multiple-plot generation.

And don't forget MICRO-CAP III's extended routine list — from impedance, Nyquist diagrams and BH plots to Monte Carlo for statistical analysis of production yield. The algebraic formula parsers for plotting virtually any function. The support for Hercules, CGA, MCGA, EGA and VGA displays. Output for plotters and laser printers.

Cost? Still only \$1495. Evaluation versions still only \$150. Brochure and demo disk still free for the asking. Call or write for yours today. And see how easily you can get ideas up and flying.

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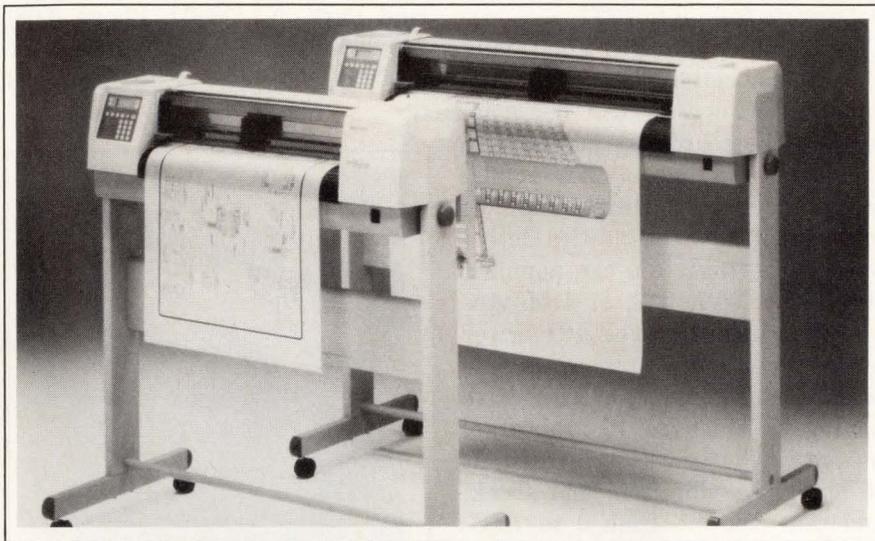
# NEW PRODUCTS

## COMPUTERS & PERIPHERALS

### Pencil And Pen Plotters

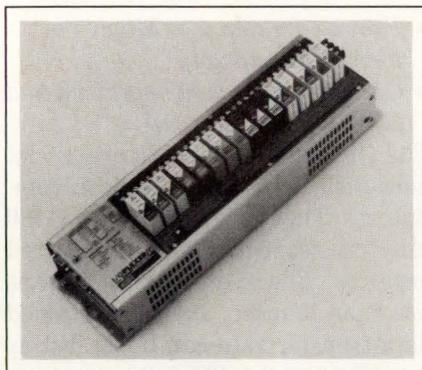
- *Fuzzy logic enhances plot speed*
- *Plot at 44.5-ips and 4.2g acceleration*

The XP-500 Series pencil and pen plotters use fuzzy logic to enhance plot speed. Utilizing a 32-bit CPU and a digital servo, the units plot at 44.5-ips and 4.2g acceleration. Fuzzy logic lets the plotters look ahead from 21 to 41 vectors, evaluating vector length and angle, and then determining the fastest, most efficient vector path to be read, sorted, and plotted. Fuzzy logic also improves circular interpolation. The units can accommodate eight pencil leads, including 0.2-, 0.3-, 0.5-, and 0.7-mm leads. They can also hold eight pens, and you can program the plotters to combine pen and pencil in a single plot. The



units contain a 1-Mbyte buffer and have an HP-GL-compatible RS-232C interface. E-size unit, \$6300; D-size unit, \$4800.

**Mutoh America Inc**, 500 W Algonquin Rd, Mt Prospect, IL 60056. Phone (708) 952-8880. FAX (708) 952-8808. **Circle No. 379**



### Industrial I/O Controller

- *Contains a 10-MHz V-20  $\mu$ P running DOS 3.3*
- *Analog and digital modules have high-voltage isolation*

The I/O PlexerPCx self-contained remote I/O controller contains a 10-MHz V-20  $\mu$ P running DOS 3.3 and 1 Mbyte of RAM. A solid-state disk drive consists of either a battery-backed RAM or Flash EPROM having a capacity as large as 256 kbytes. A COM1 port lets you download a control program from a remote host at 115.21 kbaud. A COM2 port drives an internal I/O

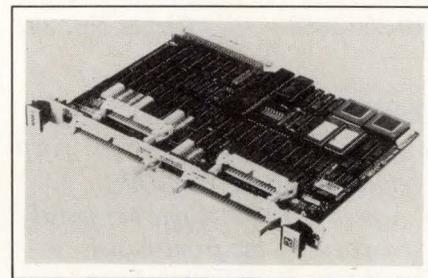
Plexer network having as many as 4000 I/O points. The unit accepts as many as 16 analog and digital I/O modules that have high-voltage isolation from module to module and module to chassis. The controller also contains a 25W power supply, a real-time clock, and a Centronics printer port. The unit measures 17.25 x 5.0 x 4.15 in. and operates from 0 to 60°C. Controller without I/O modules, \$1695; I/O modules, \$50 to \$120.

**Dutec**, 4801 James McDivitt Rd, Jackson, MI 49204. Phone (800) 248-1632; (517) 750-4700. FAX (517) 750-4740. **Circle No. 380**

### NTDS Adapter

- *Links VMEbus boards to Navy peripherals*
- *Supports NTDS type A, B, C, and H data transfers*

The NTDS-1 Navy Tactical Data System (NTDS) adapter board works with the VMEbus. It links the company's PMV 68 MIL-STD-



VME computer boards to standard Navy peripherals and provides a full-duplex parallel data path between a VMEbus and an NTDS system. The board conforms to the MIL-STD-1397 specification for type A (slow), B (fast), C (anew), and H single-ended or double-ended data transfers. A 68000  $\mu$ P and a 4-channel DMA controller control onboard functions. A 64-kbyte dual-port static RAM appears as an A24:D16 block of RAM in the VMEbus system address space. \$4425. Delivery, eight weeks ARO.

**Radstone Technology Corp**, 20 Craig Rd, Montvale, NJ 07645. Phone (800) 368-2738; (201) 391-2700. **Circle No. 381**

**Solid-State Disks**

- *Have 1, 2, or 4 Mbytes of Flash memory*

- *Operate from 0 to 70°C*

The PCF912 and PCF914 family Flash memory boards provide non-volatile memory for ISA bus computers. The boards are additions to the company's line of disk emulators. An onboard BIOS simplifies installation, and diagnostics detect power-up errors. You can populate the boards with 1, 2, or 4 Mbytes of Flash memory. The I/O driver lets you configure as many as four boards as a single physical drive having as much as 16 Mbytes of memory. The boards are resistant to humidity, vibration, and shock, and they operate from 0 to 70°C. PCF912 with 2 Mbytes of memory, \$828; PCF914 with 4 Mbytes of memory, \$1348 (100).

**Memtech Technology Corp.**, 3000 Oakmead Village Ct, Santa Clara, CA 95051. Phone (408) 970-8900. FAX (408) 986-0656. TWX 910-250-1368. **Circle No. 382**

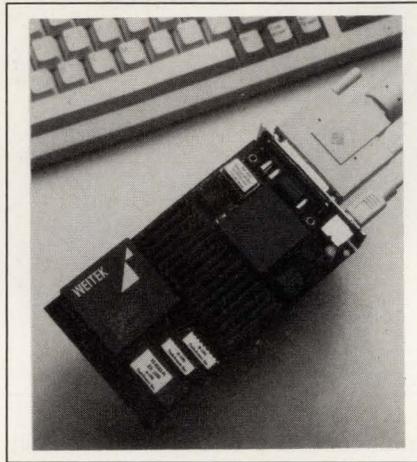
**DSP VMEbus Board**

- *Uses four TMS320C40 DSP chips to deliver 1.1 BOPS*
- *Access to 12 20-Mbyte/sec parallel ports on the front panel*

The V-C40 6U VMEbus board contains four TMS320C40 DSP chips. The four chips deliver a total of 1.1 BOPS (billion operations per second). Each chip has two independent 32-bit address buses and six 20-Mbyte/sec parallel communications ports. Twelve of these communications ports are accessible via the front panel. In addition, the board has 64 Mbytes of dynamic RAM and as much as 5 Mbytes of zero-wait-state static RAM. The board also uses the company's proprietary 24-bit parallel bus, called ADbus, to provide high-speed access to the company's I/O boards. The board has slot-1 controller functions and operates as a master or slave. DMA block transfers occur at 35 Mbytes/

sec, and the board supports D8, D16, and D32 data transfers. \$9995.

**Ariel Corp.**, 433 River Rd, Highland Park, NJ 08904. Phone (908) 249-2900. FAX (908) 249-2123. TLX 4997279. **Circle No. 383**



**Sbus Graphics Card**

- *Accelerates 2-D graphics on a SPARCstation*
- *Employs a Weitek W8720 integrated-graphics controller chip*

The GXTRA/W single-slot SBUS card accelerates 2-D graphics on a Sun SPARCstation. It uses a Weitek W8720 integrated-graphics controller chip for X Windows, Openwindows, and Sunview graphical user interfaces. The card has an 8-bit color frame buffer and a Sun-4 style keyboard and mouse port. It draws, fills, and performs bit-block transfers at 100 million pixels/sec. Different versions support 1600 x 1280-, 1280 x 1024-, and 1152 x 900-pixel resolutions. From \$3050.

**Tech-Source Inc.**, 442 S North Lake Blvd, Suite 1008, Altamonte Springs, FL 32701. Phone (407) 830-8301. **Circle No. 384**

**Short-Haul Modem**

- *Operates over two twisted-wire pairs at 19.2 kbps*
- *Has an RS-232C port switchable from DTE to DCE RO.*

The Model 205 multidrop short-haul modem operates over two twisted-

wire pairs and uses a controlled carrier, which switches the role of the master and its slaves in a polled network. You can switch the controlled carrier on manually or via the Request-To-Send (RTS) signal. The modem operates at data rates as fast as 19.2 kbps over a range of 4 miles. You can switch the unit's RS-232C connector from a DTE (data-terminal-equipment) to a DCE (data-communications-equipment) configuration. The unit derives its power from the Transmit-Data signal. Line-coupling transformers provide double isolation between communicating modems. The unit's metal enclosure measures 5.0 x 2.0 x 0.85 in. \$113.

**Telebyte Technology Inc.**, 270 E Pulaski Rd, Greenlawn, NY 11740. Phone (800) 835-3298; (516) 423-3232. FAX (516) 385-8184; (516) 385-7060. **Circle No. 385**

**2½-in. Disk Drives**

- *Provide 65 and 130 Mbytes of formatted capacity*
- *Consume 2W when operating and 5.5W during start-up*

The Go Drive 60 and 120 are 2½-in. hard-disk drives for notebook computers. They provide 65 and 130 Mbytes, respectively, of formatted capacity. The average seek time is less than 17 msec, and the sustained data-transfer rate can be as fast as 2.1 Mbytes/sec. The drives weigh 6.2 oz and consume 2W when operating and 5.5W during start-up. Go Drive 60 has a spin-up time of less than 2 sec, and Go Drive 120 has a spin-up time of less than 2.5 sec. Both drives use the company's look-ahead read cache feature, called Discache, which anticipates host requests and stores data in a 32-kbyte buffer. You can use them with the SCSI or ISA bus. Go Drive 60, \$395; Go Drive 120, \$595.

**Quantum Corp.**, 500 McCarthy Blvd, Milpitas, CA 95035. Phone (408) 894-4000. FAX (408) 894-3205. **Circle No. 386**

# How Design Work Becomes Teamwork.



The DAZIX Simultaneous Engineering Environment (SEE) turns design work into teamwork.

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What's more, with SEE, your entire team can benefit from an open-system framework. A framework that integrates DAZIX, Intergraph, and Sun products –

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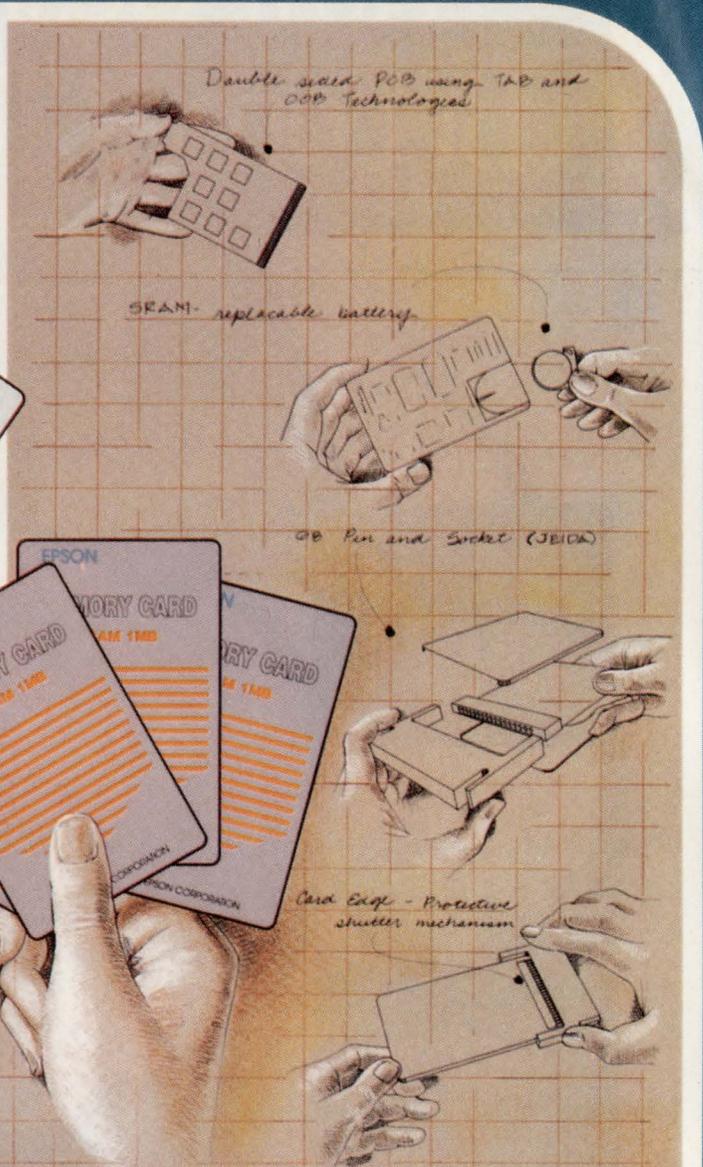
There's more you should know. Call us today at 800-239-4111 for a free copy of *Simultaneous Engineering*.

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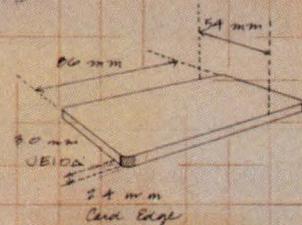
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EEPROM	16kB to 32kB

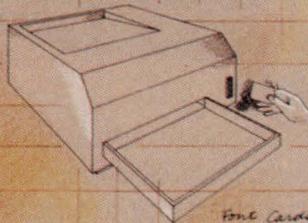
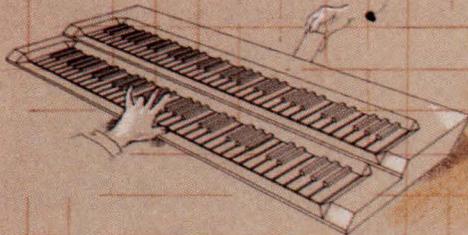


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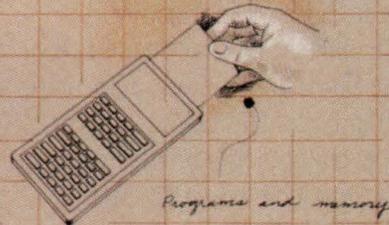
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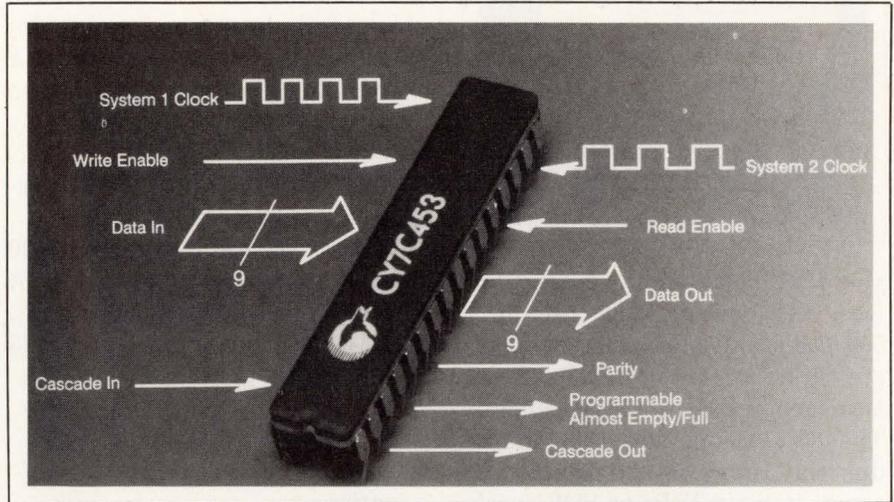
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ity generation/checking, and you can stack them in series. Available in 28-pin or 32-pin DIP and PLCC (plastic leaded chip carrier) pack-

ages, from \$25.85 to \$56.80 (100).

**Cypress Semiconductor**, 3901 N First St, San Jose, CA 95134. Phone (408) 943-2600. **Circle No. 370**

### Military Op Amp

- 185-MHz bandwidth
- Complies with MIL-STD-883

The OPA676SG/883B is a MIL-STD-883-compliant, switched-input op amp. The two independent differential inputs are selectable by means of an external TTL-compatible logic signal. The op amp features a bandwidth of 185 MHz at a gain of 10, and a settling time to 0.01% of 25 nsec. External compensation allows a range of closed-loop gains. Other specifications include a power-supply range of  $\pm 4.5V$  to  $\pm 6.5V$ , a typical output current of

comes in a 16-pin ceramic DIP that conforms to MIL-M-38510, Appendix C, Outline D-2. \$78.40 (100).

**Burr-Brown Corp**, Box 11400, Tucson, AZ 85734. Phone (800) 548-6132; (602) 746-1111. FAX (602) 889-1510. **Circle No. 371**

### Image-Compression Chip Set

- Optimized for still video cameras
- Simulates the JPEG algorithm

The 031 image-compression chip set consists of the ZR36020 discrete cosine transform (DCT) processor and the ZR36031 image-compression coder/decoder. The chip set performs compression and expansion similar to the proposed Joint Photographic Experts Group (JPEG) algorithm. Optimized for use in still video cameras, the 031 chip set includes a bit-rate control feature to ensure that a predictable number of photos can be stored on the memory card without degrading image quality. Because the chip set does not include image preprocessing functions such as color space conversion, it provides the flexibility

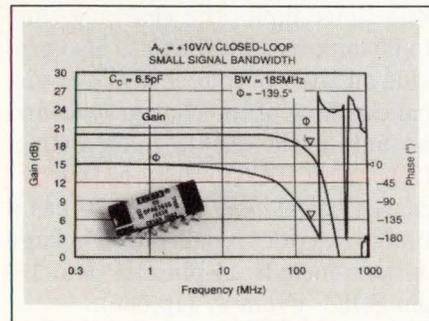
for system vendors to build differentiated, value-added products. The chip set operates at a 7.4-MHz data rate, which allows digital still video cameras to capture photos at speeds to 7.5 frames per second. The ZR36020 chip comes in either a 44-pin quad flatpack or a 48-pin ceramic DIP; the ZR36031 chip comes in either a 100-pin quad flatpack or an 85-pin PGA (pin-grid array) package. \$99 (1); \$25 (OEM qty).

**Zoran Corp**, 1705 Wyatt Dr, Santa Clara, CA 95054. Phone (408) 986-1314. **Circle No. 372**

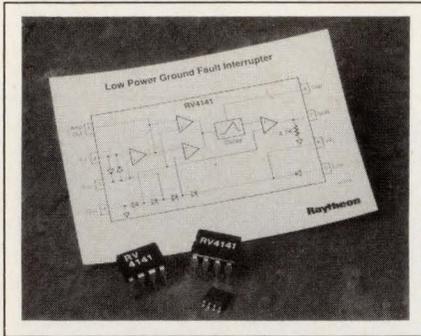
### Ground-Fault Interrupter

- Low-power operation
- Meets UL-943 requirements

Added to the company's line of ground-fault interrupter (GFI) controller ICs, the RV4141 is a low-power, 3-wire device for use in home and industrial ac receptacles and circuit panels. The RV4141 obtains its power directly from the ac line and features a built-in rectifier, a precision sense amplifier, adjust-



$\pm 30$  mA, a maximum bias current of 35  $\mu$ A, and a maximum offset voltage of  $\pm 2$  mV. The device



able time delay and an SCR interface. The device, which uses only 500  $\mu$ A of quiescent current, operates in either 110 or 220V systems and meets UL-943 requirements. The RV4141 operates over the industrial temperature range and comes in 8-pin DIPs or SOIC packages. From \$0.55 (1000).

**Raytheon Co.**, Semiconductor Div, 350 Ellis St, Mountain View, CA 94043. Phone (415) 968-9211.

Circle No. 373

### High-Speed Clock Driver

- Operates to 35 MHz
- Meets 2-nsec skew requirements

The MC74F1803 clock driver is designed for use in systems operating at frequencies as high as 35 MHz with skew requirements of 2 nsec or more. The high-speed, low-power device features separate D-type inputs and multiple synchronous outputs with closely matched propagation delays. The MC74F1803 is available in a standard 14-pin DIP or 14-pin SOIC package for surface-mount applications. \$2 (10,000).

**Motorola Inc.**, MD M538, 2200 W Broadway, Mesa, AZ 85202. Phone (602) 962-2865. Circle No. 374

### $\mu$ P Supervisory Circuit

- Resets at 1V
- Chip-enable gating is 35 nsec

The LTC1235 microprocessor supervisory circuit provides a guaranteed reset assertion down to 1V, thereby preventing  $\mu$ P malfunction at low supply voltages. The chip can also conserve battery power by con-

ditionally saving RAM contents only when necessary. Other features include a watchdog timer, power-fail detection, and chip-enable gating of 35 nsec (max). A charge-pumped FET power switch helps to limit supply current to only 1.5 mA (max). The LTC1235 is available in 16-pin DIP or SO packages. From \$3.85 (100).

**Linear Technology Corp.**, 1630 McCarthy Blvd, Milpitas, CA 95035. Phone (800) 637-5545; (408) 432-1900. Circle No. 375

### Low-Dropout Regulator

- Generates 2.85V for SCSI terminations
- Comes in small SOT-223 package

The LT1117-2.85 low-dropout regulator is for use in active terminations for the Small Computer System Interface (SCSI) standard. The device provides a regulated output of 2.85V  $\pm$ 1% from the SCSI supply and operates down to a 1V dropout voltage. Output-current capability is 800 mA and quiescent current is 10 mA (max). The regulator also features current-limiting, thermal-shutdown, and ESD protection. The LT1117-2.85 comes in a space-saving SOT-223 surface-mount package. \$1.83 (1000).

**Linear Technology Corp.**, 1630 McCarthy Blvd, Milpitas, CA 95035. Phone (800) 637-5545; (408) 432-1900. Circle No. 376

### Low-Voltage OTP Memories

- Operate at 3.3V  $\pm$ 0.3V
- Available in 512-kbit and 2-Mbit densities

Optimized for battery-powered applications, the 512-kbit Am27LV512 and 2-Mbit Am27LV020 are one-time-programmable (OTP) memories that can operate at 3.3V  $\pm$ 0.3V. The devices are available in access-time ratings of 200, 250, and 300 nsec. Maximum power consumption is 90  $\mu$ W in the standby mode and 54 mW when the device

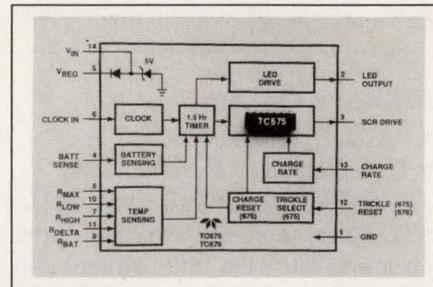
is constantly accessed at 5 MHz. Both the Am27LV512 and Am27LV020 come in 32-pin PLCC (plastic leaded chip carrier) packages. Depending on speed rating and density, \$13.51 to \$38.61 (100).

**Advanced Micro Devices Inc.**, Box 3453, Sunnyvale, CA 94088. Phone (800) 222-9323; (408) 749-5703. Circle No. 377

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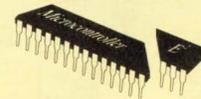
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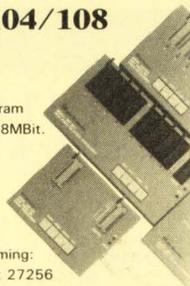
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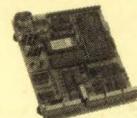
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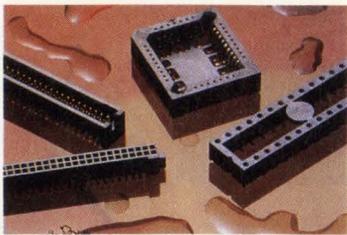
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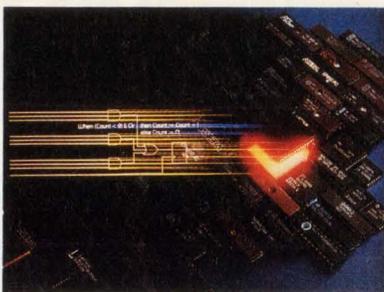
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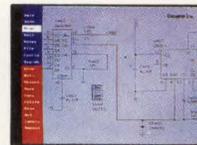
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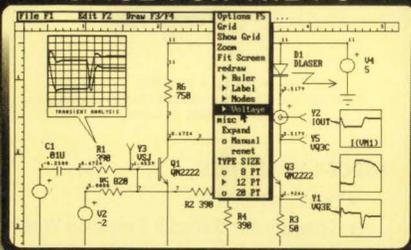
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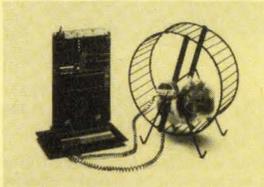
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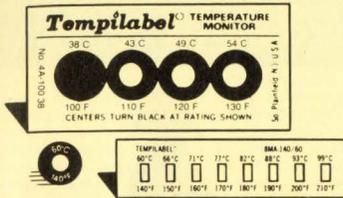
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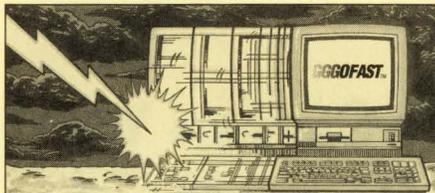
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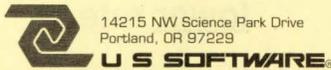


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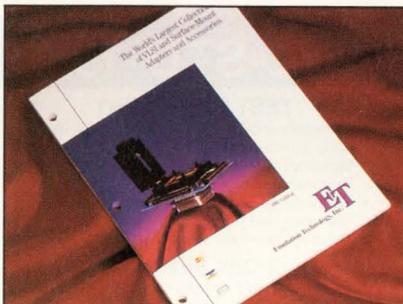


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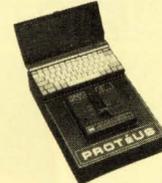
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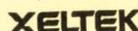
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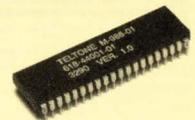


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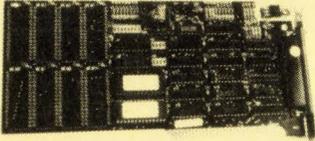
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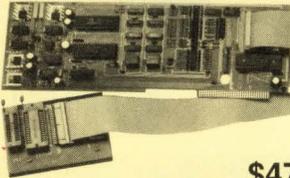
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# EDN's INTERNATIONAL ADVERTISER'S INDEX

Abbott Electronics . . . . .	21	Inlog . . . . .	144	Powertronic . . . . .	144
ABI . . . . .	151	Innovative Software Designs . . . . .	144	Pragmatic Instruments . . . . .	131
ACCEL Technologies Inc . . . . .	126	Intel . . . . .	46-49, 90-91	Safe Soft Systems . . . . .	144
Actel . . . . .	85	Intergraph Corp . . . . .	135	Samsung Semiconductor . . . . .	8-9
AMD . . . . .	92-93	Intusoft . . . . .	142	Samtec Inc . . . . .	142
AMP . . . . .	10-11	John Fluke Manufacturing Co Inc* . . . . .	22	Siemens AG** . . . . .	12, 74-75
Analog Devices Inc . . . . .	89, 118	Kepeco Inc . . . . .	44-45	Siemens . . . . .	52
Ariel . . . . .	121	Lambda Electronics Inc . . . . .	109-114	Silicon Systems Inc* . . . . .	59
Astec America . . . . .	61	Lanier/Copier . . . . .	87	Spectrum Software . . . . .	132
Aval Corp of Ireland . . . . .	143	Linear Technology Corp . . . . .	104	Synergy Computer Graphics . . . . .	36
B&C Microsystems . . . . .	143	Link Computer Graphics Inc . . . . .	144	Synergy Microsystems . . . . .	63
Belden Wire & Cable . . . . .	C4	MathSoft Inc . . . . .	124	Team Visionics . . . . .	43
BP Micro . . . . .	142	MetaLink Corp . . . . .	143	Tektronix Inc . . . . .	32-34
CAD Software Inc . . . . .	C3	Meta Software Inc . . . . .	122	Teltone Corp . . . . .	143
Capilano Computer Systems Inc . . . . .	142	MicroSim Corp . . . . .	50-51	Tempil Div . . . . .	143
Capital Equipment Corp . . . . .	120	Mini-Circuits Laboratories . . . . .	3, 4, 16-17, 26-27, 103	Teradyne Inc . . . . .	24-25
Communications Specialties Inc . . . . .	144	Mitsubishi . . . . .	65-67	Test Systems . . . . .	144
Cypress Semiconductor . . . . .	15	Murata Erie North America Inc . . . . .	125	Todd Products Corp . . . . .	142
Dale Electronics Inc . . . . .	1	National Instruments . . . . .	C2	Toshiba Corp . . . . .	30-31
Data I/O Corp . . . . .	114, 142	National Semiconductor Corp . . . . .	94-96	Tribal Microsystems . . . . .	141
Datron Wavetek . . . . .	117	NEC Corp . . . . .	70-71	US Software . . . . .	143
Delker . . . . .	64	Nepron West '92 . . . . .	115	Vicor . . . . .	116
Deltron Inc . . . . .	122A-D	Nohau Corp . . . . .	141	Westcor . . . . .	6
Design Computation Inc . . . . .	144	NordicTrack . . . . .	64	Xeltek . . . . .	143
DigiKey . . . . .	2	OKI Semiconductor* . . . . .	127	Xicor Inc . . . . .	141
Emulation Technology Inc . . . . .	143	Omaton Inc . . . . .	142	Xilinx . . . . .	72
Epson America Inc . . . . .	136	Omron Electronics Inc . . . . .	152	Zaxtek . . . . .	141
Ericsson Components . . . . .	130A-B	Orion Instruments . . . . .	143	Z-World . . . . .	141
Gespac Inc . . . . .	142	P-Cad . . . . .	18-20		
Harris Semiconductor . . . . .	68-69	Philips Semiconductor** . . . . .	108A-D		
Haverhills of San Francisco . . . . .	120	Pico . . . . .	42, 75		
Hewlett-Packard Co . . . . .	12, 28	Piher International Corp . . . . .	128		
Hitachi America Ltd* . . . . .	74-75	Planar Systems** . . . . .	108E-F		
IDT . . . . .	39	Power Trends Inc* . . . . .	41		
Incredible Tech . . . . .	141				

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- CAE—computer-aided engineering
- CMOS—complementary metal-oxide semiconductor
- CPU—central processing unit
- DIP—dual in-line package
- DOS—disk operating system
- EDA—electronic design automation
- FR4—a low-cost, epoxy-laminated substrate material commonly used with plastic surface-mount packages
- HDTV—high-definition television
- IC—integrated circuit
- JTAG—Joint Test Action Group
- LSB—least significant bit
- MCM—multichip module
- MSB—most significant bit
- npn—n-type p-type n-type
- OOP—object-oriented programming
- pc board—printed-circuit board
- PLCC—plastic leaded chip carrier
- PLD—programmable logic device
- pnp—p-type n-type p-type
- PROM—programmable read-only memory
- QTAI—quick turnaround interconnect technology
- RAM—random-access memory
- RF—radio frequency
- SOIC—small-outline integrated circuit
- SOJ—small-outline J-lead, a surface-mount integrated circuit
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CIRCLE NO. 76

EDN January 2, 1992



# **BELDEN** brings out the custom in our customers.

Belden is known worldwide as a leading supplier of wire and cable products including fiber optic cables, multi-conductor/multi-paired cables, flat cable and connectors, coaxial cables, lead wire, plenum cables, power supply cords, and molded cable assemblies. What is not so well-known is the fact that every "standard" wire and cable in our Master Catalog started out as a custom design for a specific application.

#### **World's largest wire and cable engineering facility.**

In May, 1990, Belden dedicated the most progressive and innovative cable development facility in the world today: the Belden Engineering Center (BEC). Housing over 100 engineers and technicians, this 70,000 square foot facility is committed

to keeping our OEM customers on the leading edge of technology with product development samples, process capabilities equipment, compound materials analysis, and testing and evaluation labs.

The BEC is where Belden brings out the custom in our customers with custom design or co-development of new products, custom modification of standard products, and all the technical assistance you need to keep you ahead of your competition.

#### **Quality you can stake your reputation on.**

As a leading edge manufacturer, Belden's mission is continuous improvement toward a goal of 6-Sigma quality. Total Quality Control is the central theme in

all of our processes, from vendor quality assurance through customer service. That's why original equipment manufacturers (OEMs) like IBM, Black & Decker, Motorola, DEC, Skil, Makita, and Milwaukee Electric Tool rely on Belden for wire, cable, cords, and assemblies they can count on for flawless performance and exceptional reliability.

**For more information about how Belden can turn your dreams into reality, call:**

**1-800-BELDEN-4**

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In 1986, CAD Software, Inc. introduced PADS-PCB, our first circuit board design system. Since then, our product philosophy of easy-to-use, cost-effective CAD tools has made PADS-PCB the world leader in PCB design.

In 1990, we extended the PADS product philosophy with PADS-2000, the first CAD system to truly use the 32 bit power of advanced personal computers.

Today, with the introduction of PADS-2000/UX, we offer user-friendly, high performance PADS design tools for UNIX workstation users. And, because PADS has become the recognized leader in PCB CAD, we are changing our name to PADS Software, Inc.

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