

EDN[®]

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ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

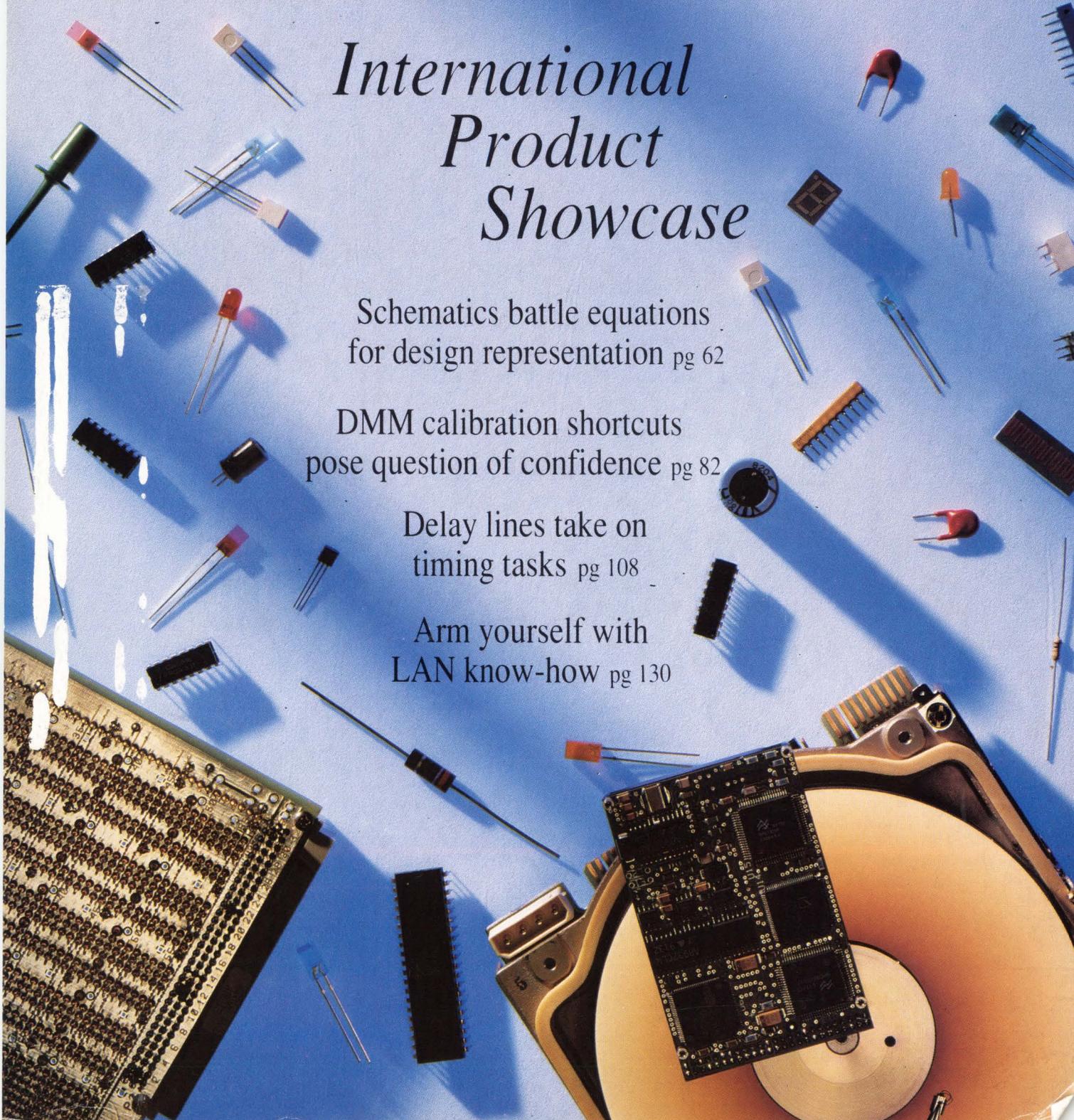
International Product Showcase

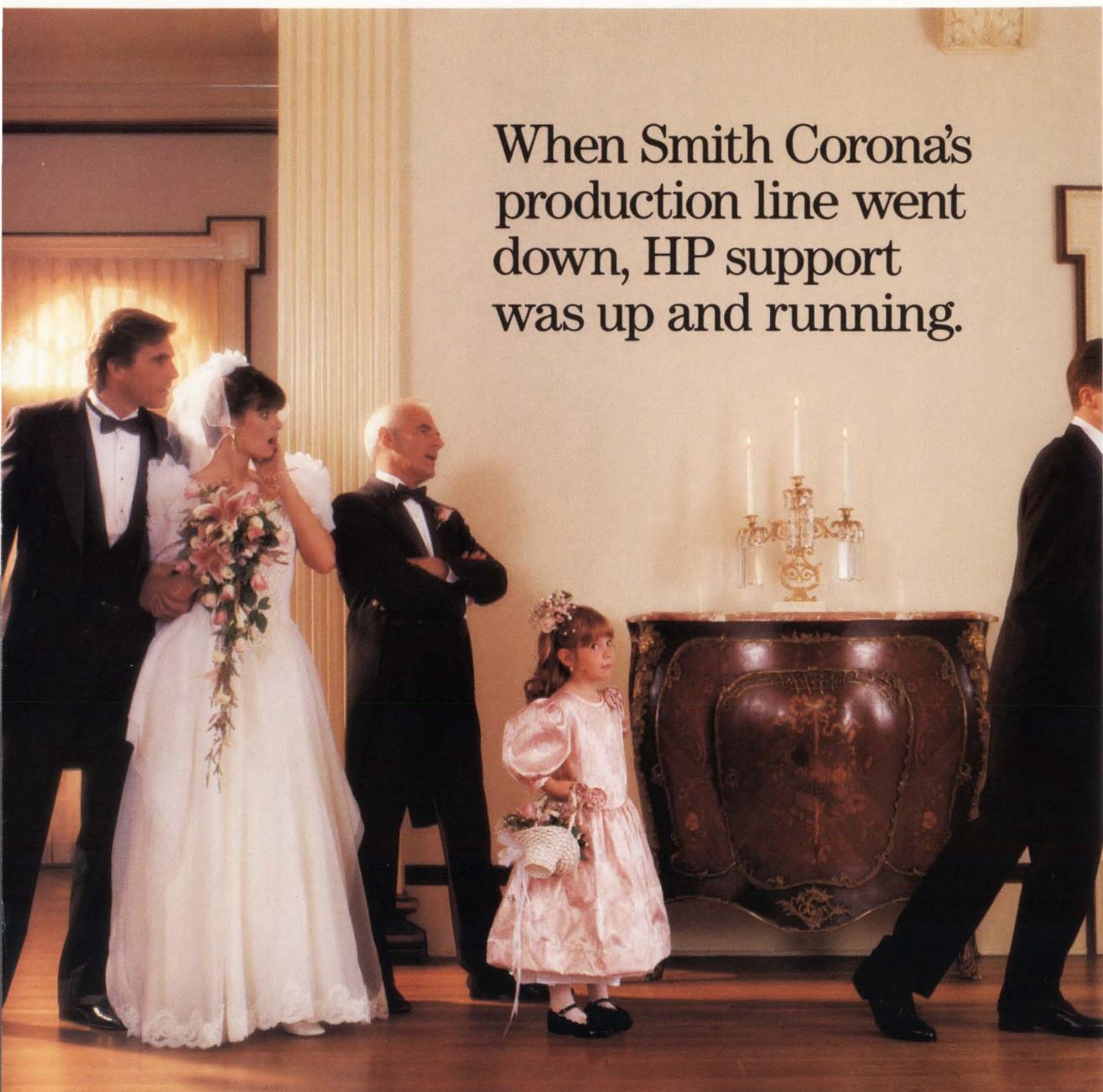
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for design representation pg 62

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pose question of confidence pg 82

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timing tasks pg 108

Arm yourself with
LAN know-how pg 130





When Smith Corona's
production line went
down, HP support
was up and running.

It happened on a freezing Saturday in February.

Joe Reiley, a Hewlett-Packard test and measurement support engineer, was at a wedding in Pottstown, Pennsylvania. The office was the furthest thing from his mind, when suddenly his beeper went off.

In minutes, Joe was on the phone to Travis Field, the support engineer for Smith Corona in Cortland, New York. An HP test system crucial to Smith Corona's production line had gone down. Suddenly, Joe's thoughts turned to figuring out how to get Smith Corona's production line back up. Joe bid the other

guests goodbye and ran to his car.

After driving through a blinding snow storm over icy mountain roads, Joe pulled into Smith Corona at 10:30 pm. A thorough analysis of the problem made it clear they needed extra parts, so Joe called another HP support engineer, Pete Nahrgang, in Valley Forge. Working through the early morning, Pete took parts from a back-up HP system, then flew them to Cortland by special courier. By Sunday afternoon, just 24 hours after Joe's beeper first went off, Smith Corona's production line was up again.

True stories like this prove HP's dedication to responsive customer support throughout the world. We'll tailor our hardware, software and education services to your test and measurement needs. With one of the largest support organizations in the industry, we're committed to keeping your production line up and running. For more information, call your local HP sales office or circle the reader service number.

There is a better way.



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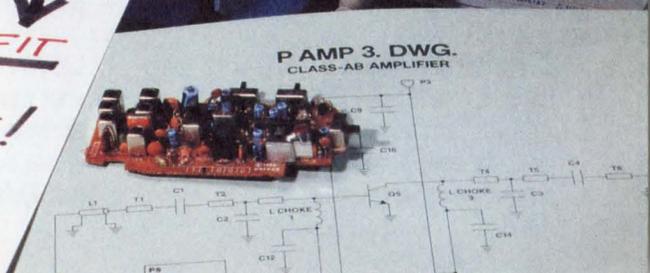
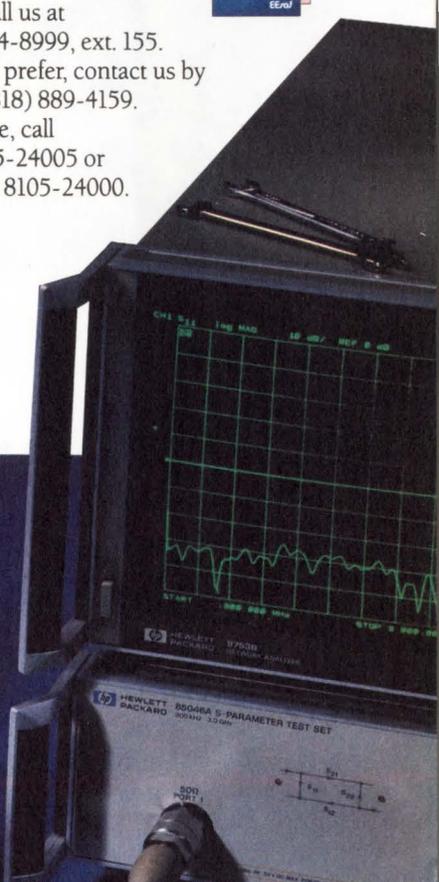
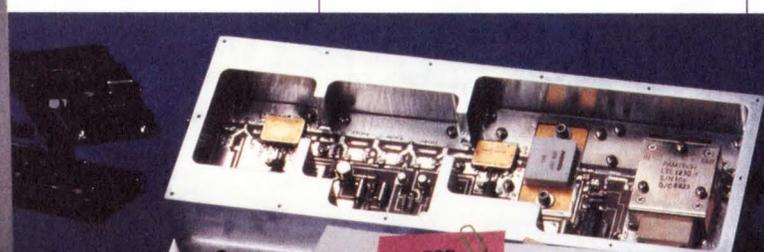
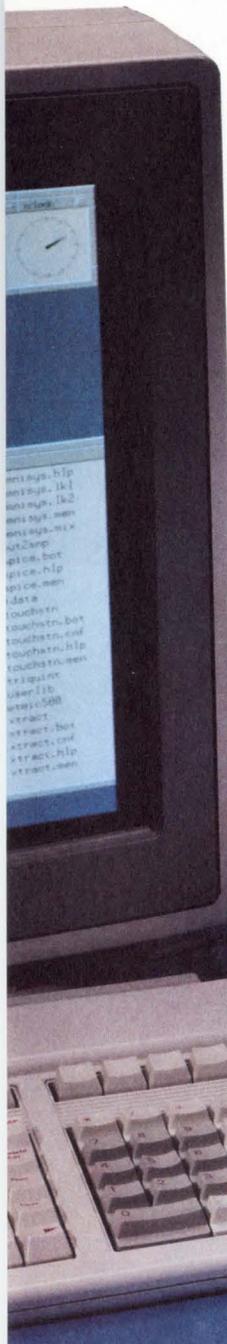
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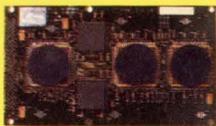
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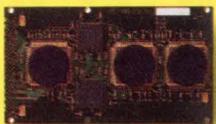
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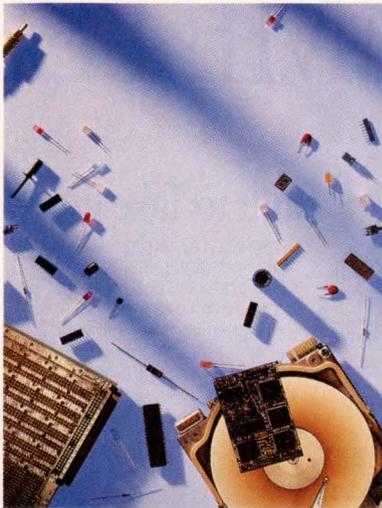
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On the cover: EDN Magazine's International Product Showcases review new products and analyze trends in eight technology areas that affect you and your work. This issue wraps up the showcase coverage with computer-aided engineering (pg 62), instruments (pg 82), components (pg 108), and computers & peripherals (pg 130). (Cover concept and art direction by Cathy Madigan; photography by Jon Chomitz; 1.8-in. hard-disk drive courtesy Intégral Peripherals Inc)

DESIGN FEATURES

Computer-Aided Engineering

Schematics battle equations for design representation

62

Debates have raged for years over whether equations or logic schematics are the best design form. Today, that debate is overshadowed by a shift toward synthesis—mapping design representations into silicon.—*Ray Weiss, Technical Editor*

Instruments

DMM calibration shortcuts pose question of confidence

82

Simpler methods of calibrating 7.5- and 8.5-digit digital multimeters let you adjust the overall accuracy of an instrument using as few as two external standards—or no standards at all. The methods are innovative but depart from principles the calibration community has cast in stone.—*Brian Kerridge, Technical Editor*

Components

Delay lines take on timing tasks

108

As system designs get more complex and operating speeds get faster, timing must be extremely precise. Programmable delay lines offer designers a way to make adjustments in circuit timing and maximize the performance of today's high-speed systems.—*Tom Ormond, Senior Technical Editor*

Computers and Peripherals

Arm yourself with LAN know-how

130

Setting up a local-area network is complicated—especially if you've never done it before. A clear idea of what you want to accomplish as well as a basic understanding of your hardware and software alternatives will help you deal with vendors and consultants.—*Dan Strassberg, Technical Editor*

Continued on page 7

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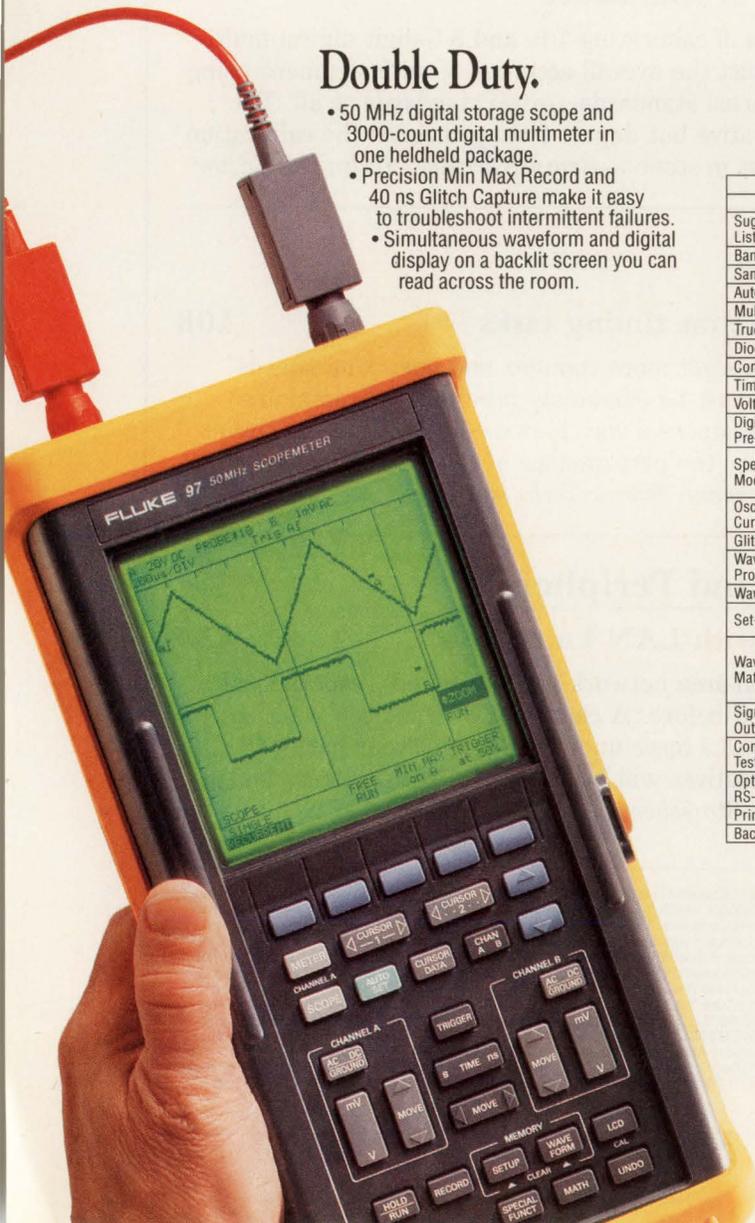
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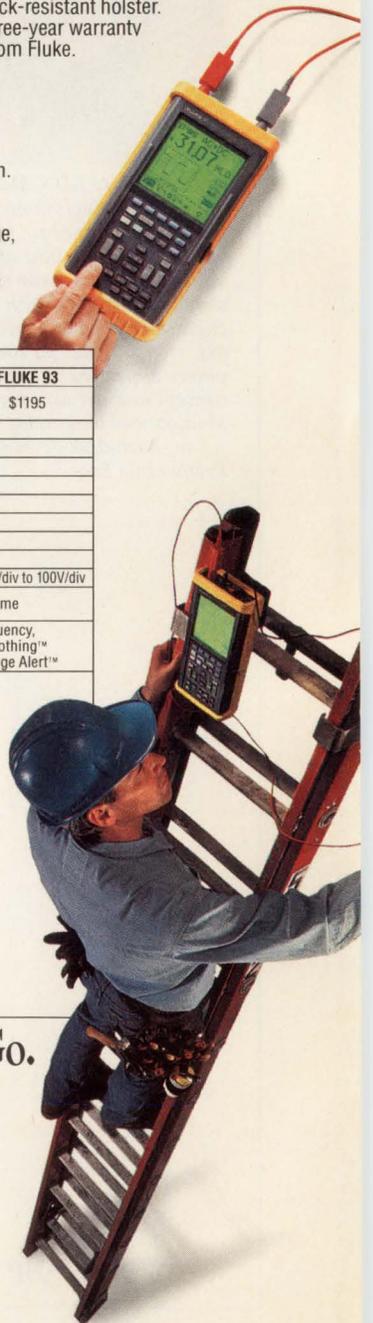
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Autoset	Automatically sets Voltage, Time and Trigger		
Multimeter Display	3 2/3 digits (>3000 Counts)		
True RMS Volts	AC or AC+DC up to 600V (1700V Pk-Pk)		
Diode Test	Up to 2.8V		
Continuity Beeper	Yes		
Time/Division	10 ns/div to 60 sec/div		
Volts/Division	1 mV/div to 100V/div	5 mV/div to 100V/div	
Digital Delay or Pre-Trigger	By Number of Cycles, Events, Time, or Zoom Mode		By Time
Special Multimeter Modes	Min Max Average Record, Relative (zero), dBm, dBV, dBW, Audio Watts, % Scale, Frequency, Smoothing™ Change Alert™		Frequency, Smoothing™ Change Alert™
Oscilloscope Cursors	12 Measurements, Display 5 Simultaneously		
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Waveform Processing	Average, Variable Persistence, Min Max Record		
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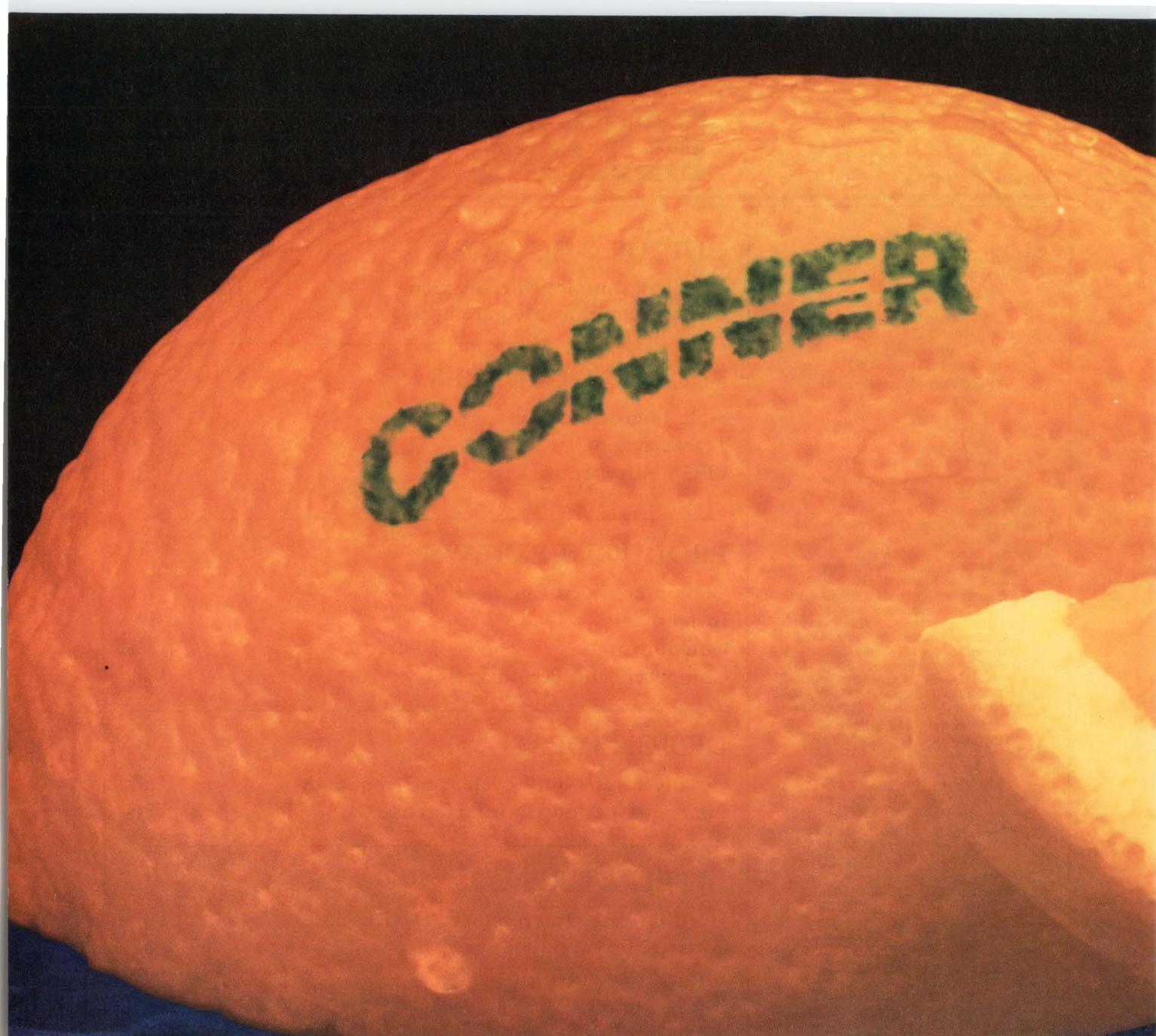
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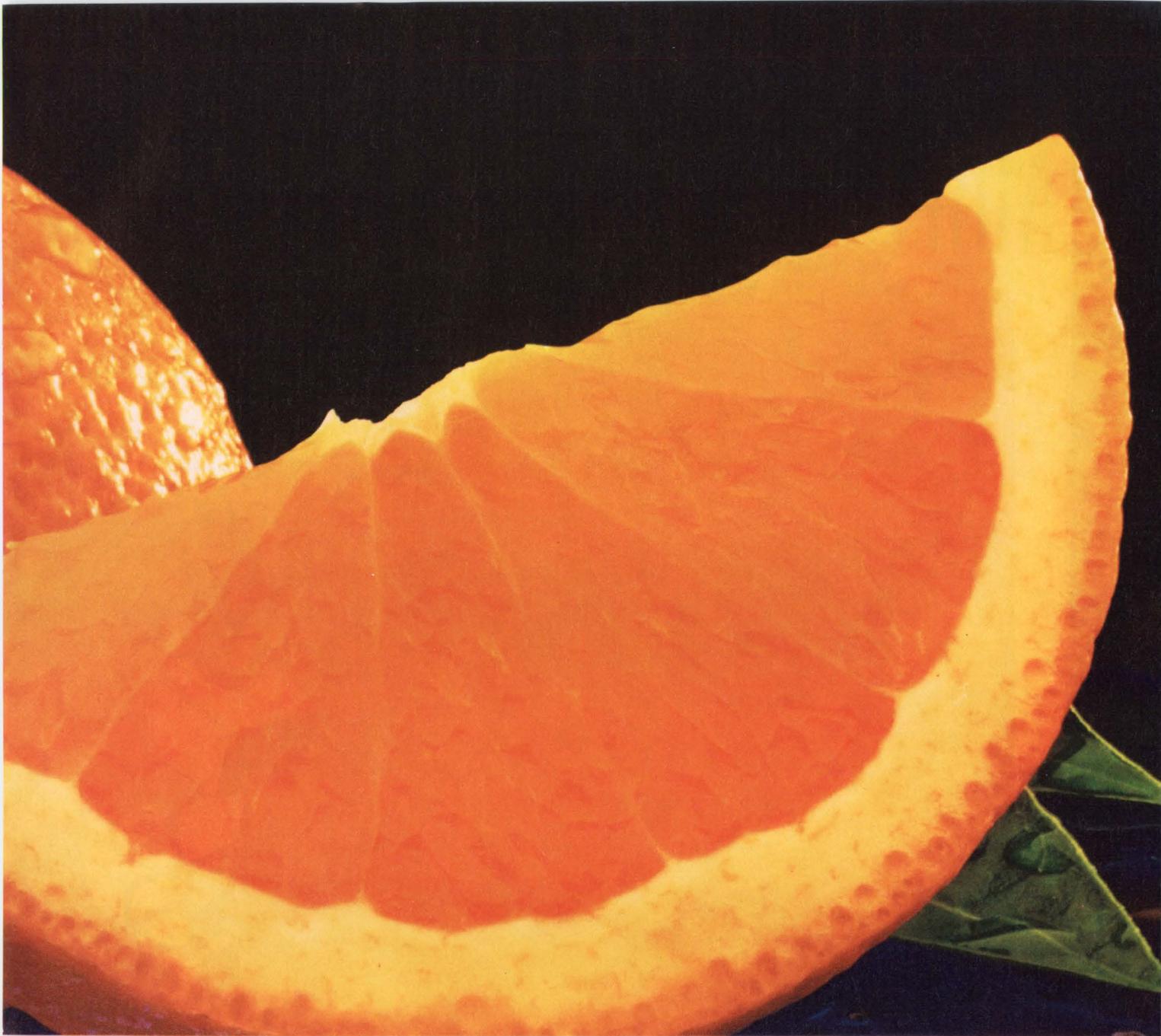


Jaguar 85/170 MB



Pancho 85 MB

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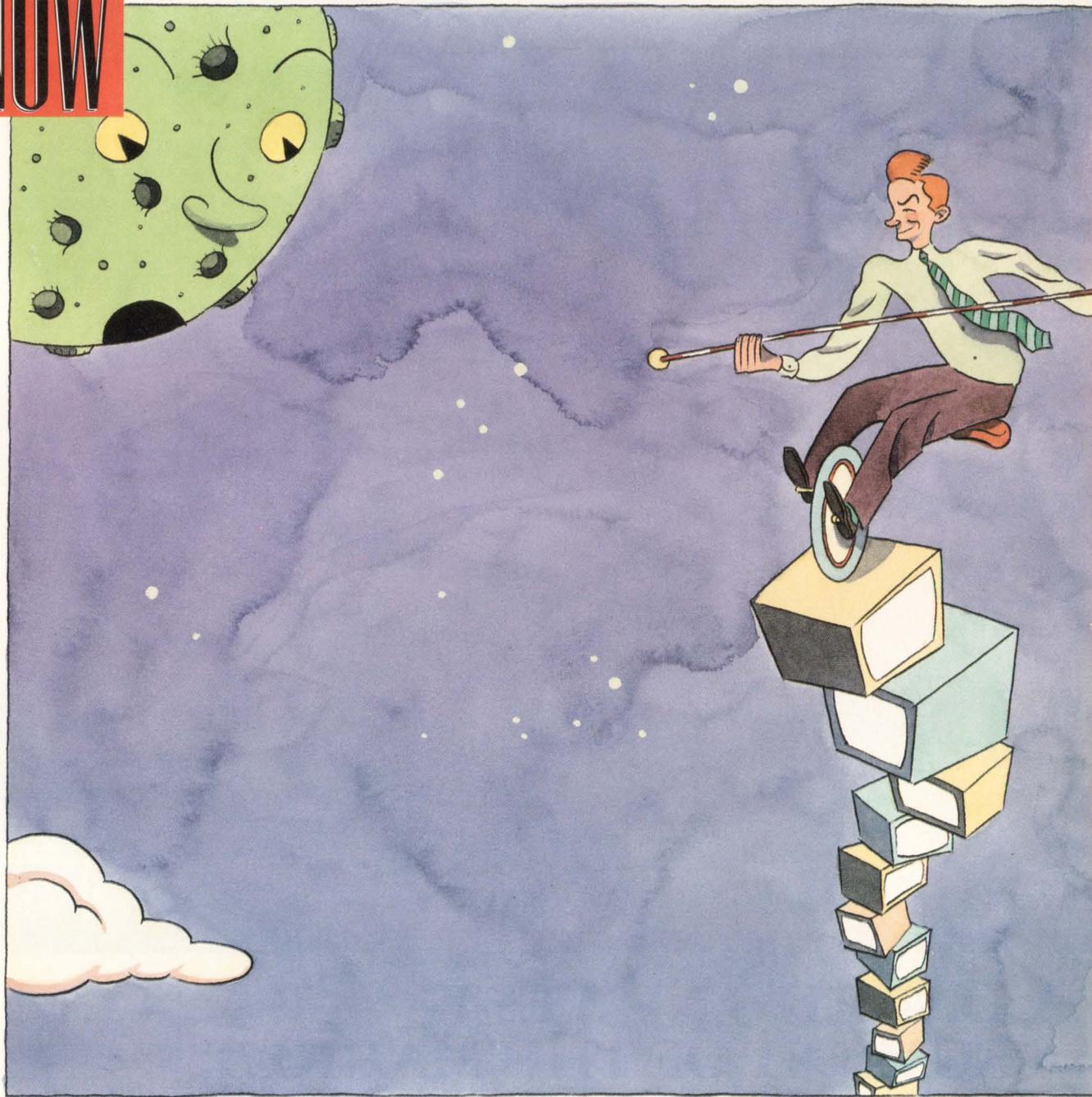
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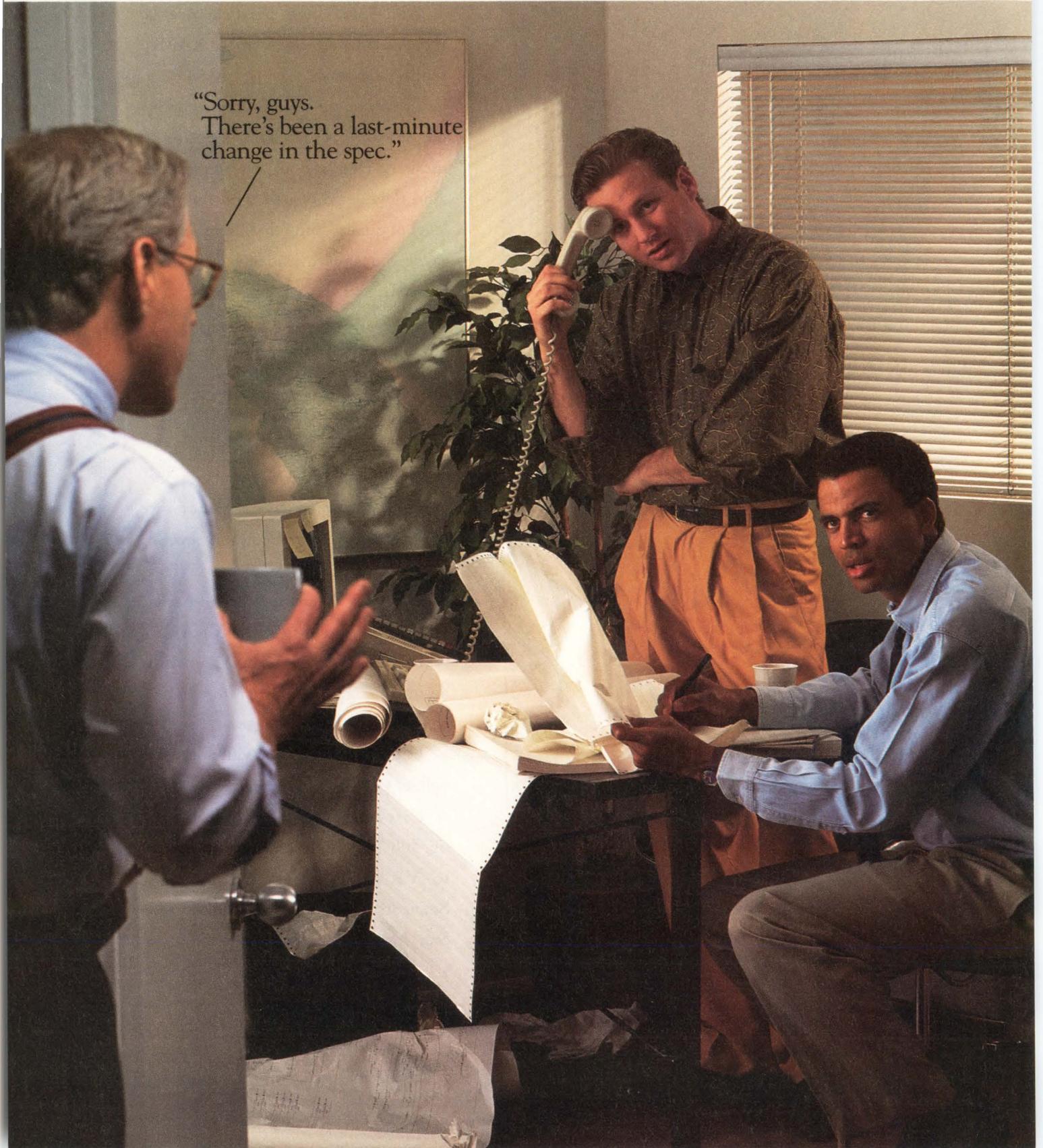
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XGA

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The new XGA standard has opened up an era of higher performance for PC graphics. And when IBM licensed their technology to INMOS, a division of SGS-THOMSON Microelectronics, as manufacturer and sole supplier of the IBM XGA chipset, they did it to ensure that the XGA parts got to the market quickly and reliably, setting the stage for XGA to become the next volume standard in PC graphics. Specifically designed for PCs, XGA is already available to support the MicroChannel Architecture bus, and an AT bus-compatible version is under way. The new XGA standard offers significant enhancements over VGA with:

- higher speed
- higher resolution (up to 1024 × 768)
- more colors (256 up to 64K) giving photo-realistic multimedia-style images
- optimized graphics interface for better windowing

- optimization for use with latest generation processors

Fully VGA compatible, XGA performance specs offer a package that is way ahead:

- 132 column text mode
- extended graphics function mode, including hardware sprite and coprocessor hardware drawing assist
- 90% faster than IBM VGA under DOS, 55% faster under OS/2
- 67% faster running Microsoft Windows applications

TWO CHIPS THAT SET THE STANDARD

The IBM compatible XGA chipset consists of two advanced VLSI chips, the INMOS IMS G190 XGA Serializer Palette DAC in a 144 pin CQFP and the INMOS IMS G200 XGA Display Controller in a 184 pin PQFP. A major advantage of the IMS G200 is its on-chip coprocessor which offloads tasks from the host processor and allows it to support:

United States Tel. + 1 602 867 6259 Fax. + 1 602 867 6290

Asia/Pacific Tel. + 65 482 1411 Fax. + 65 482 0240

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IBM ARCHITECTURE IN SILICON EXCLUSIVELY FROM SGS-THOMSON



- 1, 2, 4, and 8 bit pixel and bit block transfers
- line draw
- area fill
- logical and arithmetic pixel mixing
- map masking
- scissoring
- X, Y axes addressing

FULL SOFTWARE SUPPORT is offered for the IBM compatible XGA chipset with the following drivers available:

- DOS Application Interface (DOS AI)
- OS/2 Presentation Manager (OS/2 PM)
- Windows 3.0
- Double Byte character set

Plus a programmer's guide so you can develop your own BIOS software.

AVAILABLE NOW

Yes, the standard IBM MicroChannel Architecture-compatible XGA chipset is available right now. Just call or fax one of the SGS-THOMSON locations listed below and get details on delivery and price.

 **SGS-THOMSON**
MICROELECTRONICS

access to technology

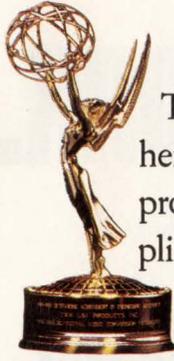
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HOLLYWOOD BUDGETS.





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The monolithic Video Encoder is here. Created by TRW, the film and production industry's leading supplier of high-performance ICs. And the only company ever to be awarded an Emmy for its video IC technology.

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TRW standards.

The TMC22090 boasts a 256x8x3 color lookup table, a

pixel mask register and compatibility with 171 and 176 RAMDACs. All

of which means transparent interface with existing device drivers.

Better still, the high performance Hollywood has come to rely on is provided by 4:4:4 digital encoding, oversampled 10-bit outputs,

and built-in test signals. The TMC22090 even gives you a JTAG interface for low cost production testing. So for everything from simply providing an affordable video output for computer display boards, to developing complex desktop video workstations, you can design in confidence. With the video encoder from the leader in video ICs: TRW.

And you can count on TRW to keep you at the forefront of multimedia, too. This Video Encoder, after all, is just our debut. We've got some great sequels in development.

For data sheets, applications and other information on TRW's TMC22090 Video Encoder, as well as to be first in line for coming attractions, call or write today:

TRW LSI Products Inc.,
P.O. Box 2472, La Jolla, CA 92038
(619) 457-1000, FAX (619) 455-6314
(800) TRW-LSIP (800) 879-5747



TRW LSI Products Inc.



Overlay graphics and titles onto video by selecting a transparent color for the Video Encoder chroma key

STANDARDS SET. STANDARDS TO BE MET.

Oh no. Please, not now. Not with manufacturing release next week.

THE PROTOTYPE DOESN'T WORK.

Six ASICs, fifteen PLDs and the whole thing's gone south. Maybe I should go south too. Yeah, hop a bus. Head for Mexico.

THE PROTOTYPE DOESN'T WORK.

Software? Could be. Hardware? Might be. So where do I start? At the beginning, of course. And just where is that, smart guy?

THE PROTOTYPE DOESN'T WORK.

And my performance review comes up next month. Maybe they'll just forget about all this, right? Yeah. Sure.

THE PROTOTYPE DOESN'T WORK.

Wait. What about that glitch in the handshake on the first pass? Couldn't reproduce it. Maybe it just reproduced itself.

THE PROTOTYPE DOESN'T WORK.



These are just a few of the reasons Tek makes a complete line of scopes, logic analyzers and signal sources. Instrumentation that can quickly get to the core of your prototype's problems. Whether they're digital, analog or software. Because even when your prototype doesn't work, Tek does. **TALK TO TEK/1-800-426-2200**

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NEWS BREAKS

EDITED BY SUSAN ROSE

SECOND ANNUAL INNOVATION AWARDS PRESENTED AT WESCON



From left to right: Roy Forsberg, EDN Publisher; Paul Gulick and Arlie Conner, In Focus Systems; John Whitmarsh, EDN News Edition Editor.

On November 19 at a banquet and reception at Wescon/91, the EDN staff presented the second annual Innovation and Innovator of the Year awards. The team of Paul Gulick and Arlie Conner from In Focus Systems were named Innovators of the Year. The team developed a triple super-twisted nematic (TSTN) LCD that furnishes brighter pictures than other LCDs. EDN presented a check for \$10,000 in their names to donate to the university of their choice.

Innovation winners were selected in seven product categories. The ISD10xx analog storage ICs from Information Storage Devices (San Jose, CA) won for ICs and semiconductors. The HP54600A 100-MHz

digital storage oscilloscope from Hewlett-Packard (Colorado Springs, CO) won for test and measurement. For CAE/CAD, the winner was the Falcon Framework for Concurrent design from Mentor Graphics (Wilsonville, OR). In Focus won again in computers and peripherals with the color LCD technology. The Isocon Interconnection System from Rogers Corp (Tempe, AZ) won for components, hardware, and interconnect. IRMX for Windows from Intel Corp (Hillsboro, OR) won for software. And, last but not least, the Genesis high-power-density battery from Gates Energy Products Inc (Gainesville, FL) won for power sources. For complete product descriptions, see the November 21, 1991, edition of EDN. All winners were selected by votes from EDN readers.—Susan Rose

SINGLE CHIP EMBEDS MS-DOS SYSTEMS

NEC Electronics Inc's DOS engine is a single chip that encompasses an entire IBM PC/XT, except for external memory. Aimed at embedded systems, this chip lets designers build a DOS-compatible system with a minimum number of chips. The DOS engine includes a clock generator, a DMA controller (8273A compatible), an interrupt controller (8259A compatible), a counter/timer (8254 compatible), a speaker interface, a memory controller, an expanded-memory system (EMS) controller, and a programmable PC/XT or PS/2 keyboard and mouse interface. Designed around the NEC V20/30, the DOS Engine is based on an 0.8 Ω m static process. Future versions will include an ASIC core that you can tailor to your needs. The core will have as many as 20,000 gates for customer-specific circuits that link to an internal 8-bit IBM PC/XT bus. The engine can access as much as 16 Mbytes of virtual memory through its EMS hardware.

The engine operates at 3 to 5V. Running at 8 MHz and 3V, it consumes 5 mA and operates with a minimum instruction-execution time of 250 nsec. Initially, there are two versions of the chip: the V41 μ PD70270, based on the V20HL with an 8-bit external bus; and the V51 μ PD70280, based on the V30HL with a 16-bit external bus. Both chips are available in a 160-pin plastic quad flatpack (PQFP) with 10-, 12-, and 16-MHz speed grades. The ASIC version comes in a 208-pin PQFP. From \$20 (10,000). NEC Electronics Inc, Mountain View, CA, (415) 960-6000.—Ray Weiss

NEWS BREAKS

PROCESS YIELDS FAST AMPS, PIN DRIVERS, AND ASICs

Harris Semiconductor today announced a series of high-speed linear products developed using the company's new complementary bipolar, silicon-on-insulator process. UHF-1 yields npn and pnp transistors with switching speeds greater than 8 and 4 GHz, respectively, and betas of 100 and 60, respectively. The process implements dielectric isolation with trench-isolation and bonded-wafer techniques. The combination of bonded wafers and trenches provides complete isolation between transistors, which results in reduced parasitic capacitance, resistance to latchup, and reduced leakage current at high temperatures. The process's values of beta, breakdown, and early voltage don't compromise the transistors' dc performance to achieve high speed. Size is also a crucial factor. The new process yields faster but smaller devices than were possible with the company's older process—a fact which should let the company offer performance increases without similar cost increases.

The first products built using this high-speed process include op amps, a closed-loop buffer, a pin-driver IC, and ASICs. The HFA1100 family of op amps (\$9.95 (100)) features an 850-MHz unity-gain bandwidth, 2500V/ μ sec slew rates, 11-nsec settling times to 0.1% accuracy, and 0.04-dB gain flatness to 50 MHz. The HFA1110 closed-loop buffer (\$9.95 (100)) has a 700-MHz bandwidth, and you can configure the buffer for voltage gains of ± 1 or 2 without external components. The buffer's 60 mA of output current makes it appropriate for use as a cable driver and distribution amplifier. The HFA5250 500-MHz pin driver (\$48 (1000)) guarantees an output impedance of 50 Ω with a maximum variance of $\pm 2\Omega$. Finally, the company has tied the process parameters into its Fastrack ASIC Design System, offering tile arrays and device-level designs. Designers can optimize the HTA3000 tile array or HDI3000 devices for either high speed or low-power consumption. The tile array consists of 10 device tiles, the elements of which can be op amps, current-feedback amps, comparators, and references. The HDI3000 library includes four npn and pnp transistor types. Typical NRE for the tile and device-level designs is \$97,000 and \$131,000, respectively. Harris Semiconductor, Melbourne, FL, (407) 724-3704, FAX (407) 724-3937.—Anne Watson Swager

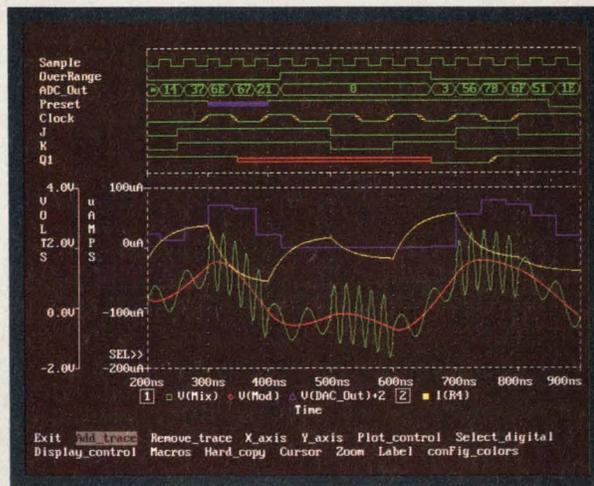
SHAMIR TOUTS BUSINESS OPPORTUNITIES IN ISRAEL

At a dinner for American industrialists in Boston in November, Israeli Prime Minister Yitzhak Shamir encouraged US high-tech companies to come to Israel. The dinner was part of a recent effort to raise interest for increased American investments in Israel. Ambassador Zalman Shoval said that the climate in Israel especially favors high-tech development: Many of the new Russian immigrants are engineers who want to stay in Israel. The country also has favorable trade relations with the US and Europe, Shoval said. Already Digital Equipment Corp, Intel, Motorola, and National Semiconductor have major facilities in Israel. For more information on the business opportunities in Israel, contact the nearest Israeli Consulate.—Susan Rose

ADD FOUR SERIAL PORTS TO YOUR WINDOWS 3.0-BASED PC

The Plus 8 multiport serial board from Star Gate lets you plug more than two serial devices into your Windows-based PC. The board contains hardware drivers that provide full-duplex asynchronous communication for Windows 3.0 in each of its three operating modes—real, standard, and enhanced. As a result, there is no need for your PC to load additional device drivers in order to accommodate a Windows environment. The board plugs into your PC's expansion chassis and uses two 8051 μ Ps. The RS-232C version costs \$570, and the RS-422 model costs \$670. Star Gate, Solon, OH, (800) 782-7428, (216) 349-1860, FAX (216) 349-2056.—JD Mosley

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Extensive Libraries

In addition to PSpice's libraries with over 3,500 analog components, Digital Simulation libraries offer over 1,500 TTL and CMOS components. Optional power supply pins are available on all digital components allowing your circuit's components to run from different power supplies and CMOS device thresholds to change with the power supply voltages.

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NEWS BREAKS

SMALL POWER SUPPLIES TARGET PORTABLE PCs

Two new families of switching power supplies from Tamura serve applications ranging from portable data-acquisition equipment to notebook and portable PCs. The company's new products include 1-in.-high, 50W units designed to mount inside a chassis. The FVS and FVM series products include single and triple output models that are smaller than a home-video cassette. The products range in price from \$90 to \$110, based on configuration and quantity ordered. Meanwhile, the company offers the SWA family products that target external power-supply applications. You can choose from 15, 20, and 30W units that plug directly into wall sockets or 40 and 60W table-top supplies. The external units range in price from \$40 to \$120. All of the new supplies can handle universal ac inputs that range from 85 to more than 200V. Tamura Corp, Carson, CA, (310) 638-1790, FAX (310) 638-9956.—Maury Wright

DSP CHIP SUITS PARALLEL-PROCESSING APPLICATIONS

The TMS320C40 DSP chip from Texas Instruments provides the processing power necessary for embedded parallel-processing tasks such as computer imaging and vision, 3-D graphics, neural networks, robotics, and speech recognition. The chip has six communication ports, two memory buses, and a 6-channel DMA coprocessor. Operating specs include 275 million operations/sec and 320-Mbyte/sec throughput. Both the manufacturer and third-party vendors offer parallel-processing development tools for the chip. Samples are available now for \$560. Texas Instruments, Dallas, TX, (800) 336-5236, ext 700, (214) 995-6111, ext 700.—JD Mosley

DATA-COMPRESSION IC HANDLES 3000 SIMULTANEOUS TASKS

Data-compression ICs currently let you effectively double the capacities of tape and disk drives, but the model 9705 compression chip from Stac Electronics expands that coverage to networks by incorporating support for as many as 1500 simultaneous, full-duplex data streams (3000 tasks). Because of network overhead, the chip provides a typical compression ratio of 4:1 for network data packets. Consequently, you can effectively quadruple a network's available capacity through data compression.

The IC employs the same compression/decompression algorithm as its single-tasking predecessor, the model 9704, and is pin- and software-compatible with the older device. At its maximum clock rate of 50 MHz, the new device compresses 2.5 Mbytes of data/sec and decompresses at 6 Mbytes/sec. For low-power applications, you can also put the chip into a sleep mode that reduces current consumption to 300 μ A. Samples of the IC are available; production quantities will be available in the first quarter of 1992. The chip costs \$24 (50,000). Stac Electronics, Carlsbad, CA, (619) 431-7474.—Steven H Leibson

X-TERMINAL SOFTWARE SERVES MS-DOS AND WINDOWS

AGE introduced two new software products that let PCs act as X servers in an X-Window application. Software for DOS supports video adapters ranging from monochrome to super VGA to 8514/A. The product include a hot key feature that lets you swap between X-server-DOS and Microsoft-Windows sessions. The product works with MS-DOS 5.0 and costs \$395—or \$465 when bundled with TCP/IP (transmission control protocol/internet protocol) networking software. Software for Windows, meanwhile, lets you use Microsoft Windows as a local window manager, and still provides the X-server capability. You can cut and paste between Microsoft Windows and X-Window applications. The software can work with any graphics hardware that comes with a Microsoft Windows driver. The Windows software costs \$495. AGE, San Diego, CA, (619) 455-8600, FAX (619) 597-6030.—Maury Wright



PROFILES IN PARTNERING

Raytheon and Dale®

PRODUCTS: Metal film and wirewound resistors.

OBJECTIVE: Develop efficient systems for supplying and procuring MIL-style components.

UNITS INVOLVED: Raytheon and Dale Electronics, Inc.

For more than two decades, Raytheon and Dale® have developed a strong manufacturer/vendor relationship focused on close communication and a common goal to continually improve quality.

Today, Dale works closely with other Vishay companies (including Angstrom and Ultronix) in supplying established reliability resistors used in the *Patriot*, *Sparrow* and other programs of the Raytheon Missile Division. Military specifications involved include: MIL-R-39005, MIL-R-39007, MIL-R-39009, MIL-R-39017,

MIL-R-55182, MIL-R-55342 and MIL-R-83401.

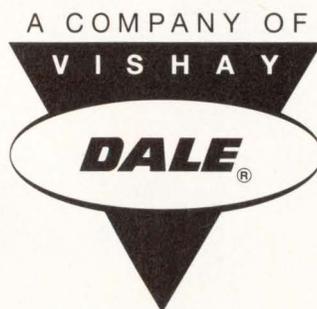
In helping Raytheon meet the exacting requirements of these programs, Dale, in 1984, became the first OEM vendor to Raytheon to install an on-line computer terminal, allowing direct-order capability with several Dale plants.

Since then, this system has been tailored to allow Raytheon purchasing locations to obtain a wide range of information on orders to Dale including everything from price, to production status, to a shipping date.

"In essence," a Dale spokesperson commented, "Raytheon can access anything we can in relation to any or all of their orders. More recently, Dale helped Raytheon pioneer their first system for electronic data interchange (EDI)."

Quality, also, has played a big part in the relationship. With a history of tens of millions of parts shipped to Raytheon, Dale has maintained exceptionally high quality levels. This is why Raytheon has chosen Dale for several quality and service awards over the last few years.

For more information on how Dale's commitment to effective partnering can benefit your operation, please contact Joe Matejka, Vice President, Quality Assurance, Dale Electronics, Inc., 1122 23rd Street, Columbus, Nebraska 68601-3647. Phone 402-563-6511. Fax 402-563-6418.



FILTERS



dc to 3GHz from \$11.45

lowpass, highpass, bandpass

- less than 1dB insertion loss • greater than 40dB stopband rejection • surface-mount • BNC, Type N, SMA available
- 5-section, 30dB/octave rolloff • VSWR less than 1.7 (typ) • rugged hermetically-sealed pin models • constant phase
- meets MIL-STD-202 tests • over 100 off-the-shelf models • immediate delivery

low pass, Plug-in, dc to 1200MHz

Model No.	Passband MHz loss < 1dB	Stopband, MHz loss > 20dB	loss > 40dB	Model No.	Passband MHz loss < 1dB	Stopband, MHz loss > 20dB	loss > 40dB
PLP-5	DC-5	8-10	10-200	PLP-250	DC-225	320-400	400-1200
PLP-10.7	DC-11	19-24	24-200	PLP-300	DC-270	410-550	550-1200
PLP-21.4	DC-22	32-41	41-200	PLP-450	DC-400	580-750	750-1800
PLP-30	DC-32	47-61	61-200	PLP-550	DC-520	750-920	920-2000
PLP-50	DC-48	70-90	90-200	PLP-600	DC-680	840-1120	1120-2000
PLP-70	DC-60	90-117	117-300	PLP-750	DC-700	1000-1300	1300-2000
PLP-90	DC-81	121-137	167-400	PLP-800	DC-720	1080-1400	1400-2000
PLP-100	DC-98	146-189	189-400	PLP-850	DC-760	1100-1400	1400-2000
PLP-150	DC-140	210-300	300-600	PLP-1000	DC-900	1340-1750	1750-2000
PLP-200	DC-190	290-390	390-800	PLP-1200	DC-1000	1620-2100	2100-2500

Price, (1-9 qty), all models: plug-in \$14.95, BNC \$32.95, SMA \$34.95, Type N \$35.95

Surface-mount, dc to 570MHz

SCLF-21.4	DC-22	32-41	41-200	SCLF-190	DC-190	290-390	390-800
SCLF-30	DC-30	47-61	61-200	SCLF-380	DC-380	580-750	750-1800
SCLF-45	DC-45	70-90	90-200	SCLF-420	DC-420	750-920	920-2000
SCLF-135	DC-135	210-300	300-600				

Price, (1-9 qty), all models: \$11.45

Flat Time Delay, dc to 1870MHz

Model No.	Passband MHz loss < 1.2dB	Stopband MHz loss > 10dB	loss > 20dB	VSWR	Freq. Range, DC thru	0.6fco X	Group Delay Variations, ns	fco X	2fco X	2.67fco X
PBLP-39	DC-23	78-117	117	1.3:1	2.3:1	0.7	4.0	5.0		
PBLP-117	DC-65	234-312	312	1.3:1	2.4:1	0.35	1.4	1.9		
PBLP-156	DC-94	312-416	416	0.3:1	1.1:1	0.3	1.1	1.5		
PBLP-200	DC-120	400-534	534	1.6:1	1.9:1	0.4	1.3	1.6		
PBLP-300	DC-180	600-801	801	1.25:1	2.2:1	0.2	0.6	0.8		
PBLP-467	DC-280	934-1246	1246	1.25:1	2.2:1	0.15	0.4	0.55		
▲BLP-933	DC-560	1866-2490	2490	1.3:1	2.2:1	0.09	0.2	0.28		
▲BLP-1870	DC-850	3740-6000	5000	1.45:1	2.9:1	0.05	0.1	0.15		

Price, (1-9 qty), all models: plug-in \$19.95, BNC \$36.95, SMA \$38.95, Type N \$39.95

NOTE: ▲-933 and -1870 only with connectors, at additional \$2 above other connector models.

high pass, Plug-in, 27.5 to 2200MHz

Model No.	Stopband MHz loss < 40dB	loss < 20dB	Passband MHz loss < 1dB	VSWR Pass-band Typ.	Model No.	Stopband MHz loss < 40dB	loss < 20dB	Passband MHz loss < 1dB	VSWR Pass-band Typ.
PHP-25	DC-13	13-19	27.5-200	1.8:1	PHP-200	DC-210	210-290	395-1600	1.7:1
PHP-50	DC-20	20-26	41-200	1.5:1	PHP-500	DC-280	280-365	500-1600	1.8:1
PHP-100	DC-40	40-55	90-400	1.8:1	PHP-600	DC-350	350-440	600-1600	2.0:1
PHP-150	DC-70	70-95	133-600	1.8:1	PHP-700	DC-400	400-520	700-1800	1.6:1
PHP-175	DC-70	70-105	160-800	1.5:1	PHP-800	DC-445	445-570	780-2000	2.1:1
PHP-200	DC-90	90-116	185-800	1.6:1	PHP-900	DC-520	520-660	910-2100	1.8:1
PHP-250	DC-100	100-150	225-1200	1.3:1	PHP-1000	DC-550	550-720	1000-2200	1.9:1
PHP-300	DC-145	145-170	290-1200	1.7:1					

Price, (1-9 qty), all models: plug-in \$14.95, BNC \$36.95, SMA \$38.95, Type N \$39.95

bandpass, Elliptic Response, 10.7 to 70MHz

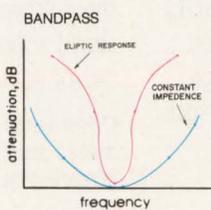
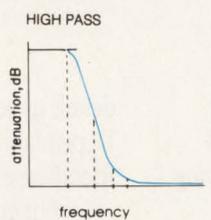
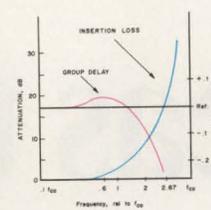
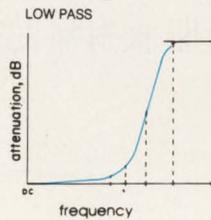
Model No.	Center Freq. (MHz)	Passband i.L. 1.5 dB Max. (MHz)	3 dB Bandwidth Typ. (MHz)	Stopbands i.L. > 20dB at (MHz)	i.L. > 35dB at (MHz)
PBP-10.7	10.7	9.6-11.5	8.9-12.7	7.5 & 15	0.6 & 50-1000
PBP-21.4	21.4	19.2-23.6	17.9-25.3	15.5 & 29	3.0 & 80-1000
PBP-30	30.0	27.0-33.0	25-35	22 & 40	3.2 & 99-1000
PBP-60	60.0	55.0-67.0	49.5-70.5	44 & 79	4.6 & 190-1000
PBP-70	70.0	63.0-77.0	68.0-82.0	51 & 94	6.0 & 193-1000

Price, (1-9 qty), all models: plug-in \$18.95, BNC \$40.95, SMA \$42.95, Type N \$43.95

Constant Impedance, 21.4 to 70MHz

Model No.	Center Freq. MHz	Passband MHz loss < 1dB	Stopband loss > 20dB at MHz	VSWR 1.3:1 Total Band MHz
PIF-21.4	21.4	18-25	1.3 & 150	DC-220
PIF-30	30	25-35	1.9 & 210	DC-330
PIF-40	42	35-49	2.6 & 300	DC-400
PIF-50	50	41-58	3.1 & 350	DC-440
PIF-60	60	50-70	3.8 & 400	DC-500
PIF-70	70	58-82	4.4 & 490	DC-550

Price, (1-9 qty), all models: plug-in \$14.95, BNC \$36.95, SMA \$38.95, Type N \$39.95



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setting higher standards

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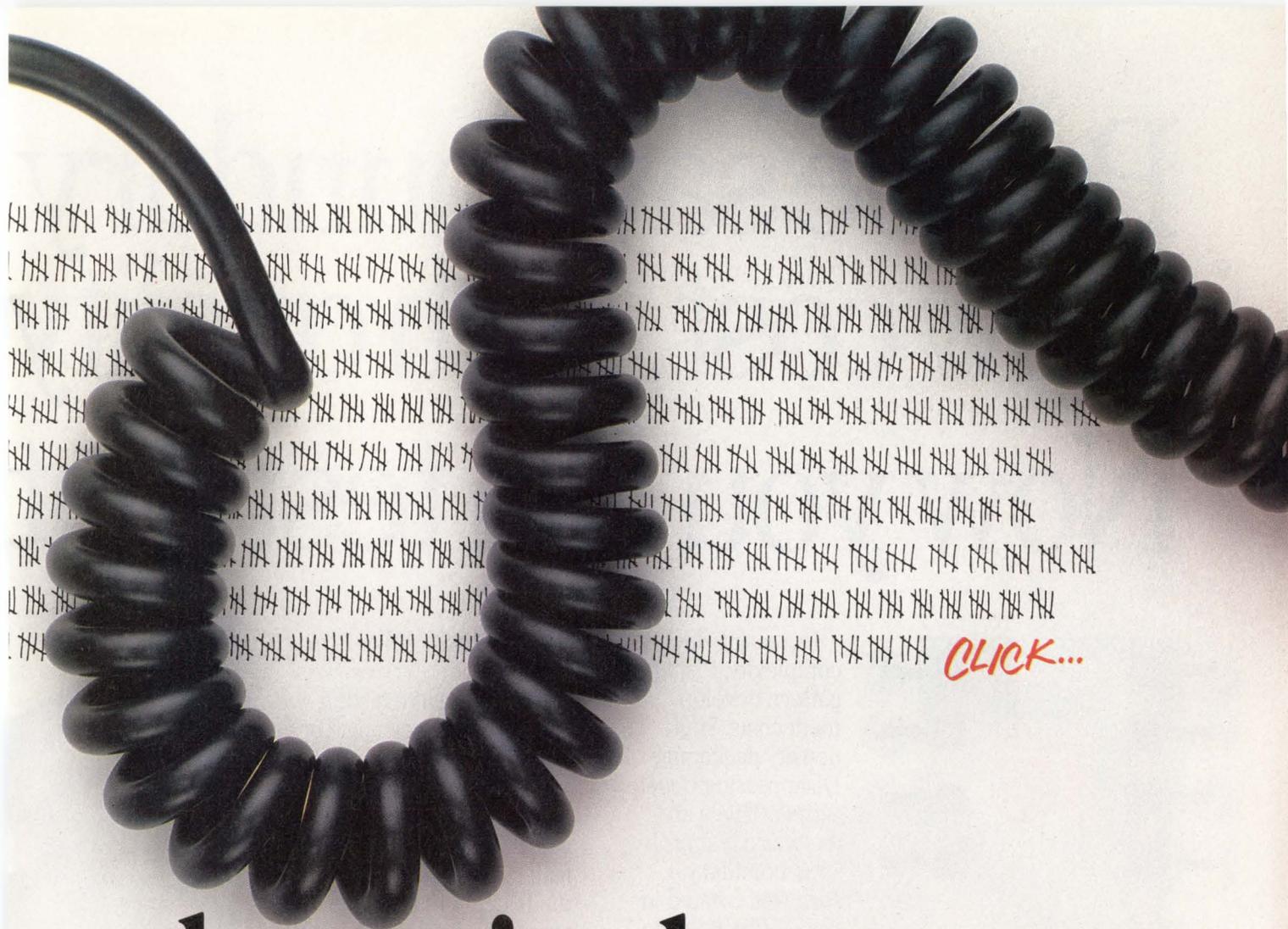
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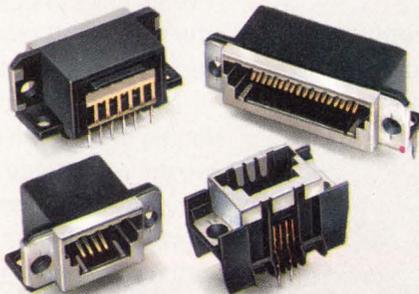


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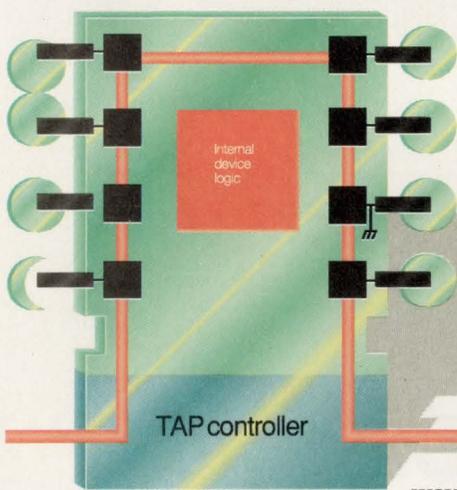


*Receptacle options:
top and side entry, and shunted side
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For technical information and literature on SDL connectors, call 1-800-522-6752. AMP Incorporated, Harrisburg, PA 17105-3608.

AMP Interconnecting ideas

People say boundary in low cost, high quality Now you can test that



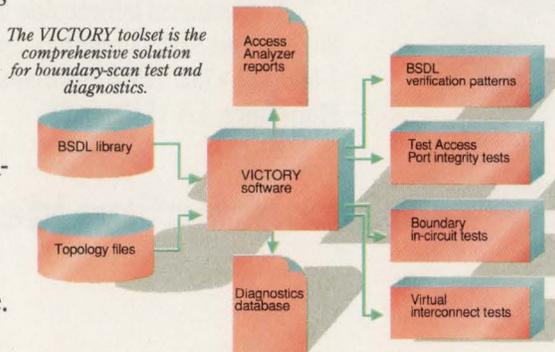
Find common manufacturing faults without test pattern libraries or physical test access with boundary-scan design and VICTORY software.

Increasing device complexity. Rising pattern development costs. High density packaging. Disappearing nodal access. These are the board test problems boundary scan was created to solve. Which is fine in theory. Only problem is there hasn't been any way to put boundary scan to the test. Until now.

VICTORY – the first software to automate boundary-scan testing.

Introducing VICTORY™ from Teradyne: the only software toolset ready to help you turn boundary-scan theory into a practical advantage. From the moment your first boundary-scan device is designed in, VICTORY starts

to simplify the testing of complex digital boards. And the more boundary-scan parts you have, the more time and money you save.



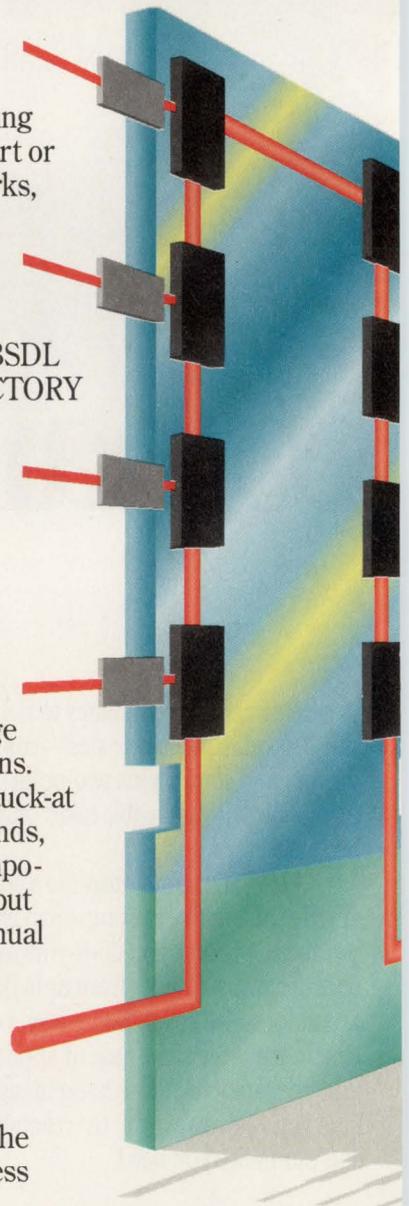
The VICTORY toolset is the comprehensive solution for boundary-scan test and diagnostics.

Delivers high fault-coverage.

Whether you're testing one boundary-scan part or boundary-scan networks, VICTORY software automatically gives you 100% pin-level fault coverage. Using the IEEE 1149.1 and BSDL standards, it takes VICTORY only a minute or two to generate test patterns. It would take a programmer days, even weeks to deliver the same fault coverage for conventional designs.

Now you can find stuck-at faults, broken wire bonds, wrong or missing components—even open input pins—all without manual diagnostic probing. VICTORY's fault diagnostics clearly spell out both fault type and fault location. And that's just the manufacturing process

Concurrent engineering takes on new meaning when you use VICTORY's Access Analyzer to optimize board layout for testability and cost-efficiency.

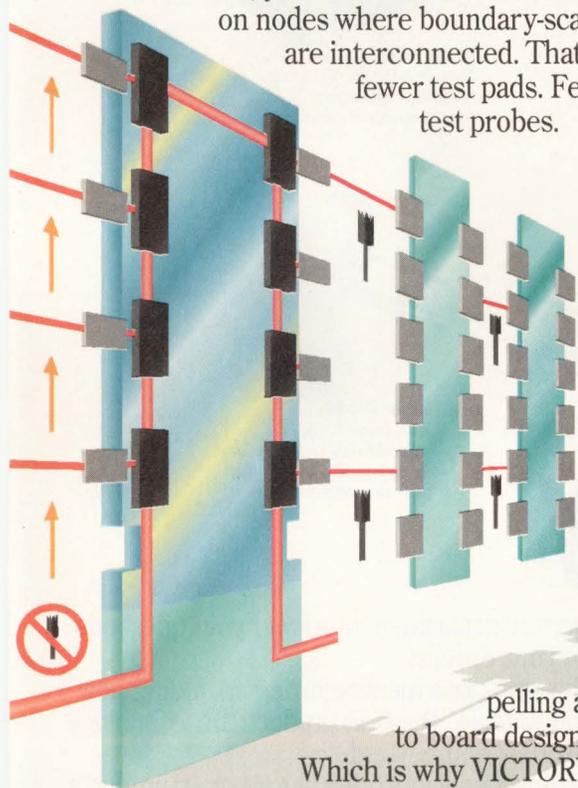


scan is a breakthrough board testing theory.

feedback you need to eliminate defects where it's most cost-effective—at the source.

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With boundary-scan design and VICTORY software, you won't need bed-of-nails access on nodes where boundary-scan parts are interconnected. That means fewer test pads. Fewer test probes.

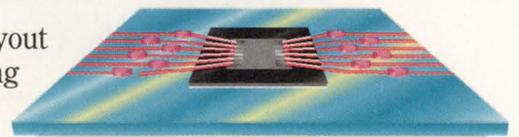


fewer test pads. Fewer test probes.

That's a compelling advantage to board designers.

Which is why VICTORY's Access Analyzer was developed. With this concurrent engineering tool, designers get testability information early in the design process. They can easily see where test points are required for visibility and where they can be dropped, for opti-

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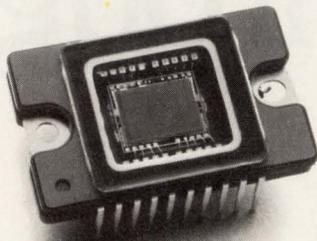


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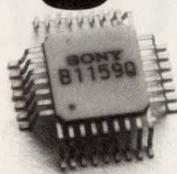
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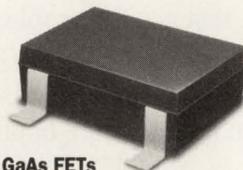
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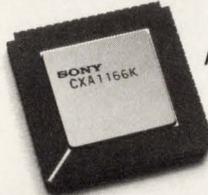
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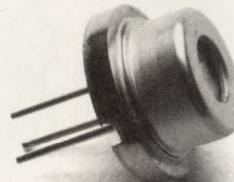
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SIGNALS & NOISE

Missing information

In the article on FPGA design methods (EDN, August 5, 1991, pg 122), EDN didn't include Synoptics as a manufacturer of image-processing boards. The company offers boards for the IBM PC/AT and VMEbus based on the ADSP2100 and a proprietary image processor. The boards offer recursive filtering and slow- or variable-scan frame-grabber modes for RS-170 or CCIR formats. Prices range from \$1300 to \$34,000.

Synoptics

Paragon Towers
233 Needham St
Newton, MA 02164
Phone (617) 527-4461
FAX (617) 527-4084.

EDN's article on DSP coprocessor boards in the September 16, 1991, issue, pg 108, also omitted a vendor: Mercury Computer Systems
600 Suffolk St
Lowell, MA 01854
Phone (508) 458-3100
FAX (508) 458-9580.

Mercury's MC family uses the i860 RISC μ P. The article noted that although the i860 is not technically a DSP μ P, several vendors have found it to be a very powerful DSP engine. EDN called attention to one such firm's products and indicated that you could expect to see i860-based DSP boards from other companies. Although any i860-based board can perform DSP operations, only a few vendors of such boards emphasize the DSP capabilities.

Engineers are treated like second-class citizens

According to a recent American Association of Engineering Societies (AAES) report, engineers' salaries are not keeping pace with inflation. (Mine hasn't for about 15 years.) And the Congressional debacle known as 1706 has reduced engineers to Professionals, Third Class, making it virtually impossible for them to work as independent contractors or consultants.

Engineers more than 40 years old now often cannot even get jobs in engineering. They have to leave engineering for law, or more likely, as common laborers. Yet our educators and government bureaucrats keep singing the refrain, "Shortage of engineers."

We are now second-class citizens in almost all areas of electronics because engineering leadership has been reduced to a form of rote labor. Our auto-industry products and major appliances are being made overseas, as well as most of our electronics.

Elimination of the exemption from requiring engineering activities to be headed by qualified licensed professional engineers can help, if it isn't already too late! A measure of the severity of the situation can be drawn from the fact that whereas new law graduates start as clerks with salaries of \$70,000 or more a year, young engineering graduates can't do better than about \$30,000 a year if they can even find a job. And many job openings list salaries in the low \$20,000s.

How long will there be a market for our professional journals and specialty trade journals, let alone college engineering courses, if this continues? Isn't it time that a balance be restored that can prevent further erosion of our engineering infrastructure?

Keats A Pullen, Jr
American Association of
Concerned Engineers Inc
Kingsville, MD

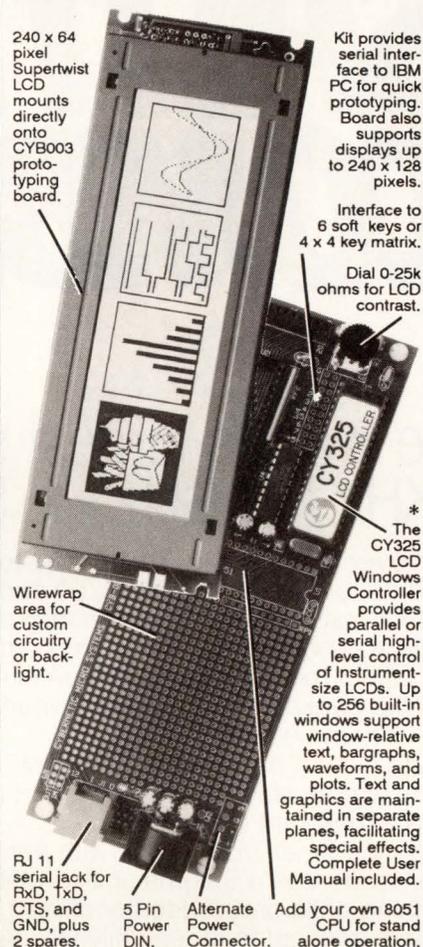
NEXT WEEK IN EDN

In the January 9, 1992, EDN News Edition, look for

- a Product Watch on emulators vs logic analyzers
- a Career Opportunities article on medical electronics
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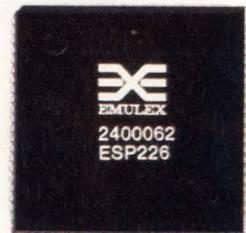
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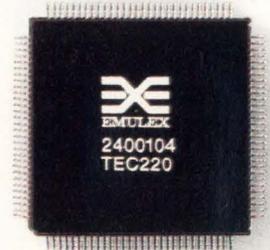
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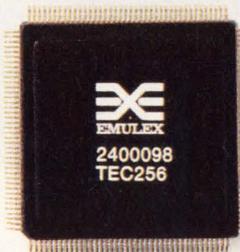
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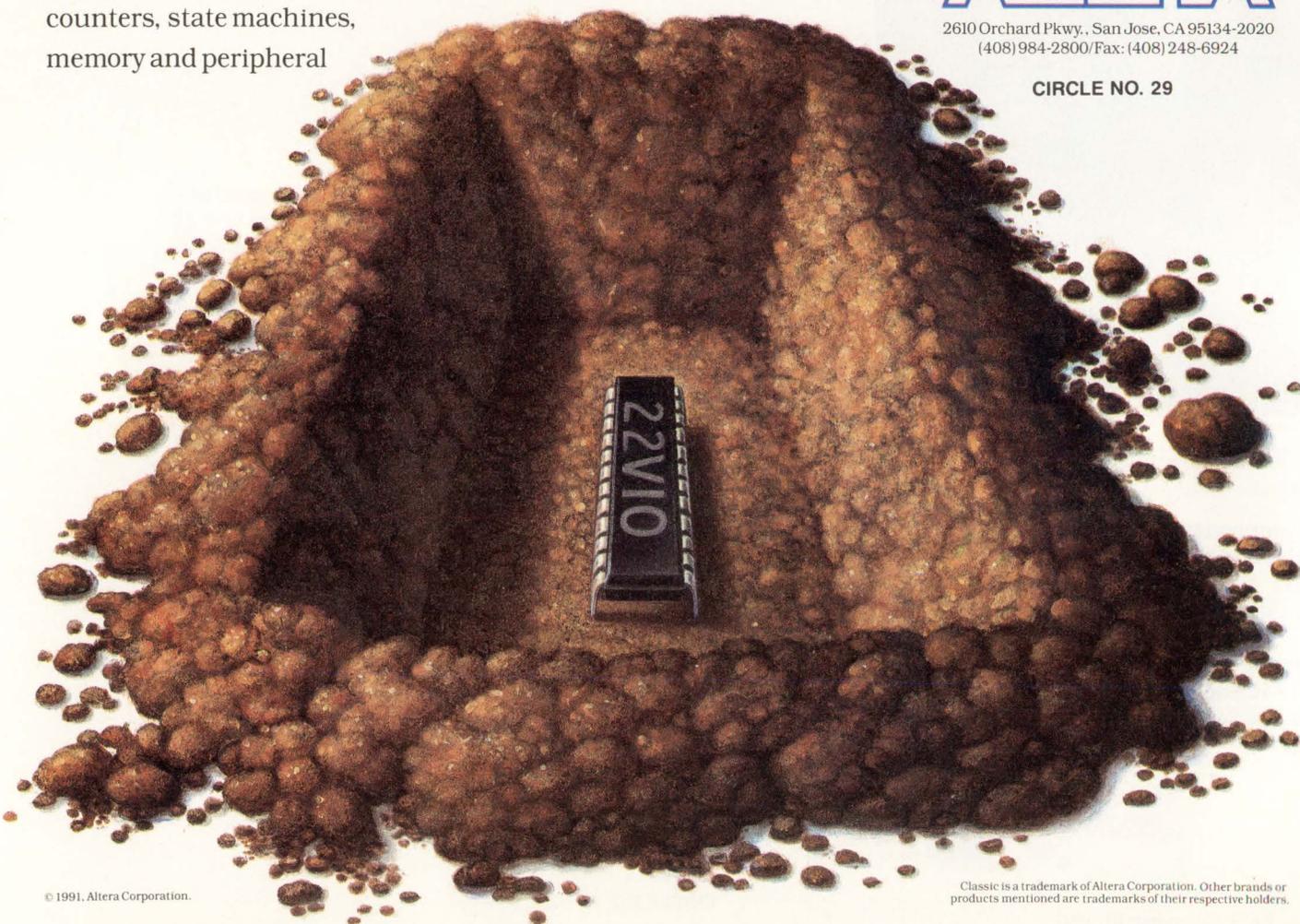
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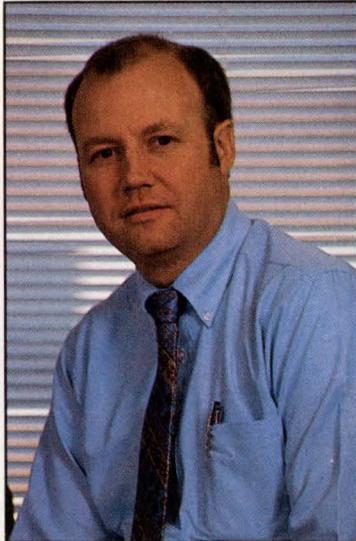
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CIRCLE NO. 29



EDITORIAL

Coming soon in EDN



Anyone looking at the electronics industry will see the momentum. And, they will realize that momentum usually relies on evolution. That momentum, and subsequent evolution, is extending to EDN. Starting with our January 20, 1992 issue, you'll see some of the ways in which EDN is evolving to help you better meet your changing needs for information.

A lot of thought and deliberation have gone into our changes and enhancements. In all cases, the new things you'll see arise from communication with our readers. We've looked at the comments on every reader-service card and we've talked with readers in focus groups. We've also run readers' needs surveys to gauge interest in specific types of articles, types of information, and organization, among other things. We know what you want and what you need.

There weren't any great surprises; readers like what we're doing to help them do their jobs better. Nevertheless, you can always improve a product and that's what we've done. For example, you'll see a new cover style. Many of you scanners or skimmers want more information about articles put on the cover. Thus, you'll find article titles and page numbers on the cover in a consistent place every issue.

You'll also find our table of contents is easier to use because we're color coding similar articles. The consistent colored labels will identify article types on the cover and throughout each issue. For example, a red or pink bar denotes new products.

We've also added some new sections to EDN. Many of our Special Reports will include an "Editor's Analysis" box that gives engineers and managers distilled information about cost, design, and management issues. Because the electronics business is so closely tied to microprocessors and microcontrollers, we're dedicating special "Processor Update" pages to introductions of μ Ps, μ Cs, and related hardware and software tools. Our editors often get their hands on products and will now bench test them. You'll read their findings and critiques in the new "Hands On!" section. Typically, we'll look at computer boards, instruments, design aids, books, catalogs, and other products that we can give a quick review.

Well, there is still more to come, but I'll save that for my next editorial. In the meantime, all of us at EDN wish you and your family a happy holiday season.



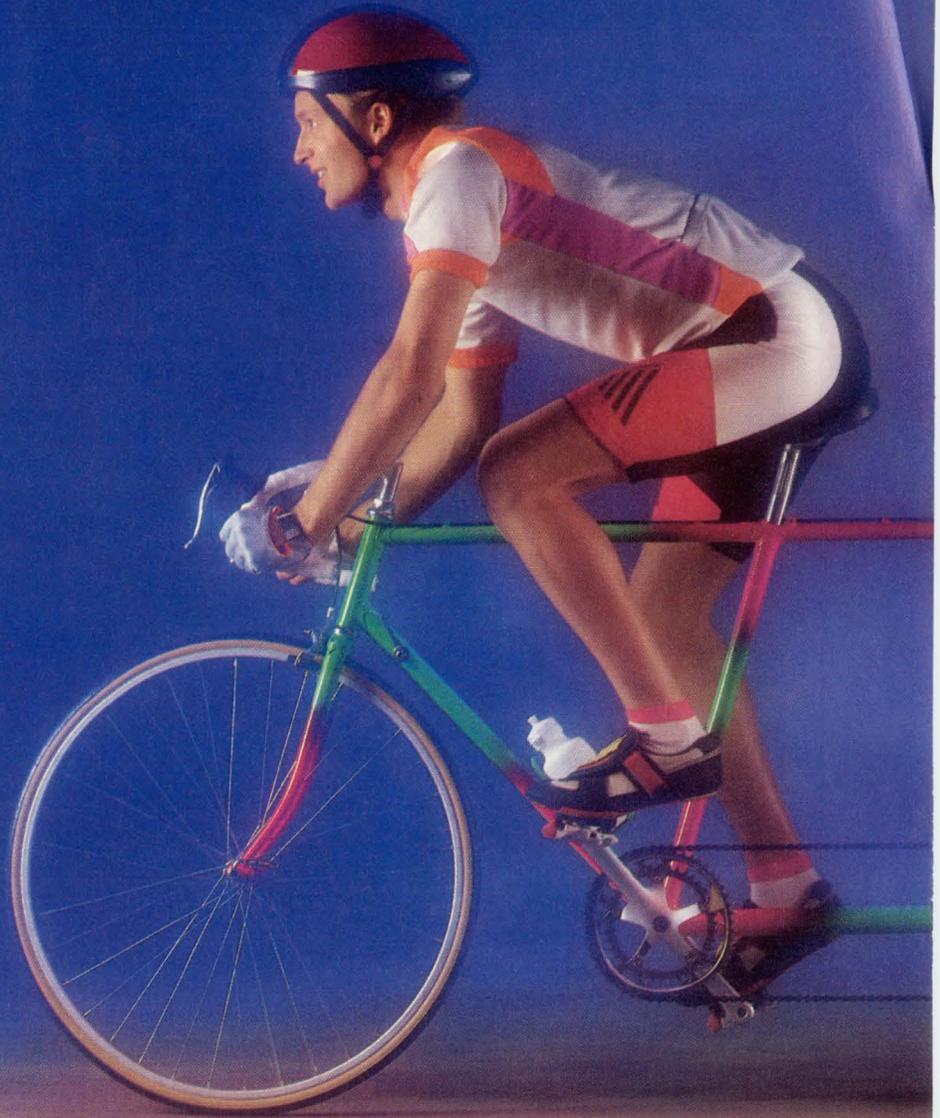
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1987, 1981 (2), 1978 (2),
1977, 1976, 1975

American Society of
Business Press Editors Award
1991, 1990, 1988, 1983, 1981

A handwritten signature in black ink that reads "Jon Titus". The signature is fluid and cursive, with a long horizontal stroke extending from the end.

Jon Titus
Editor

Send me your comments via FAX at (617) 558-4470, or on the EDN Bulletin Board System at (617) 558-4241 300/1200/2400, 8, N, 1.



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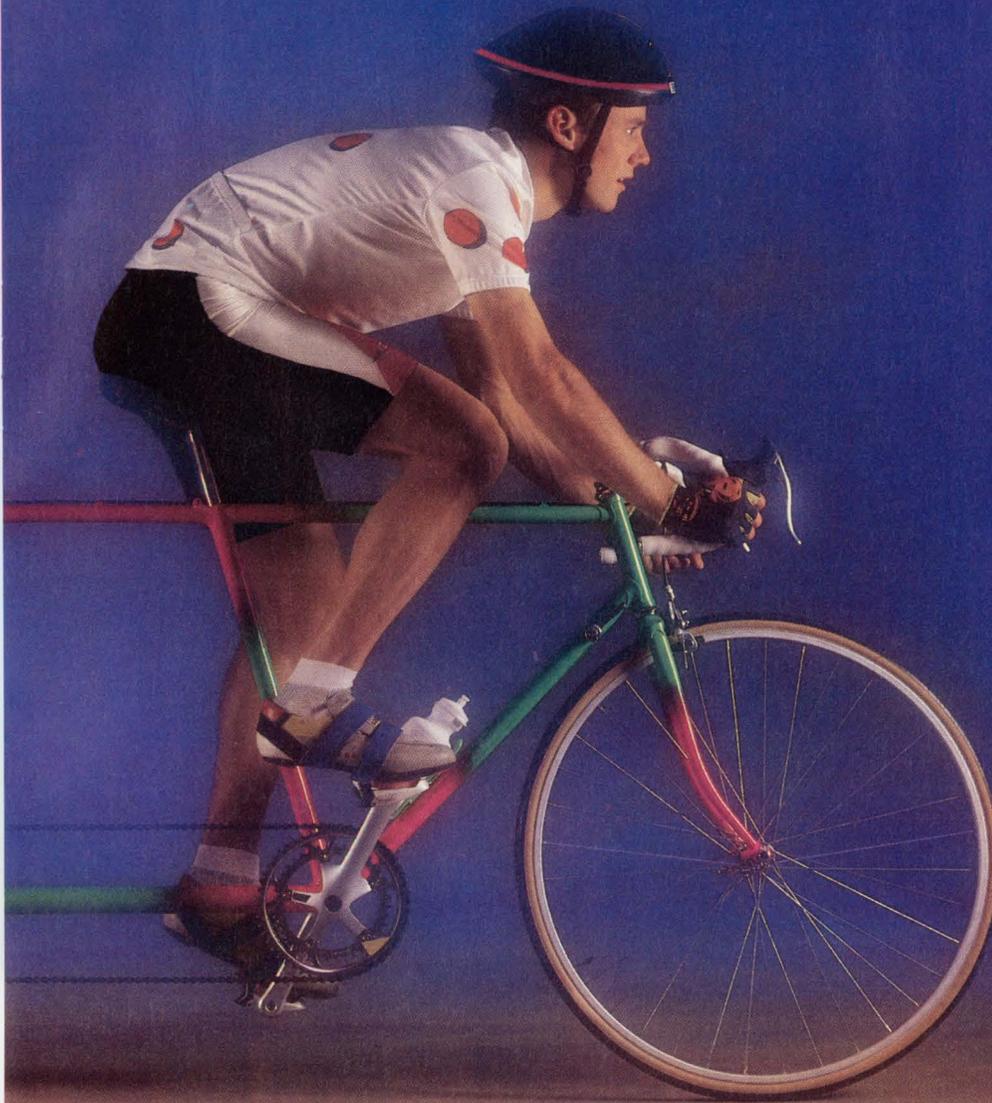


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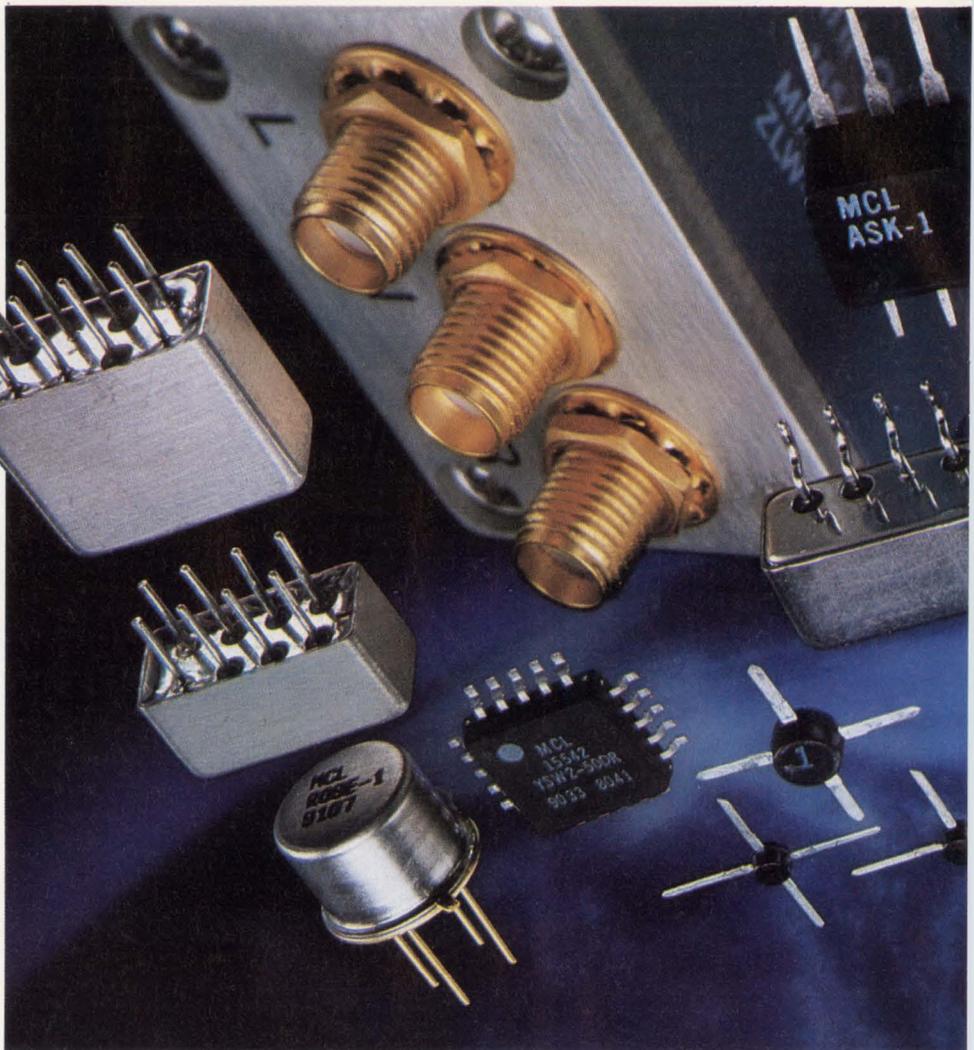
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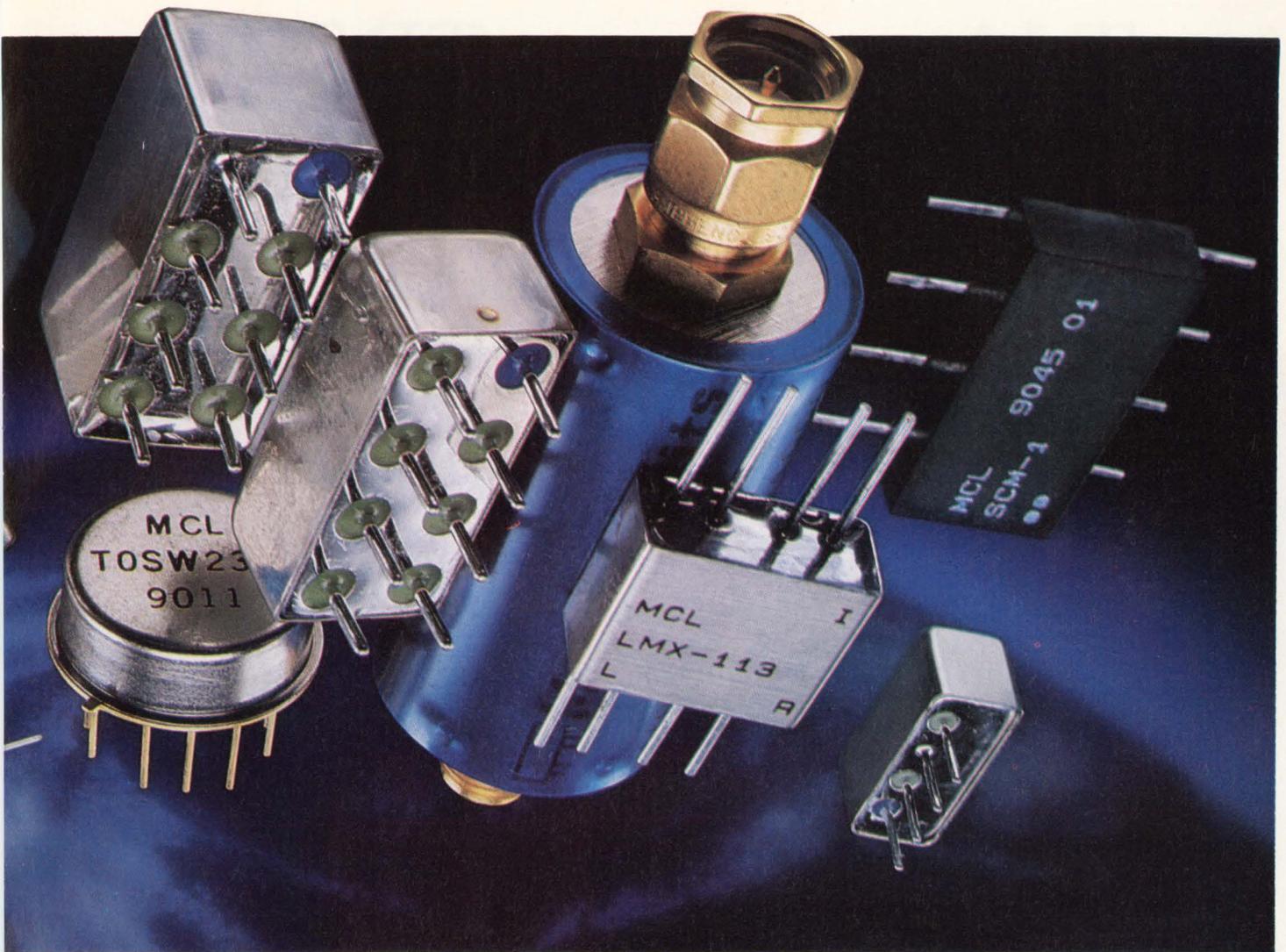
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CIRCLE NO. 8

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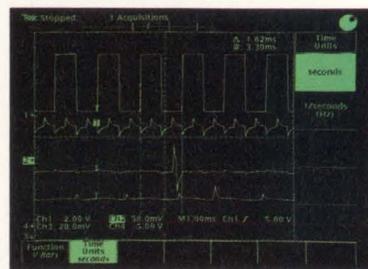
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Test and Measurement

Wideband monolithic op amp satisfies difficult HDTV video specifications

Designing and manufacturing a monolithic op amp that has a gain-bandwidth product greater than 100-MHz may no longer be the challenge that it once was to IC manufacturers. However, combining wide bandwidth with gain flatness, low noise, low distortion, low phase error and the ability to supply 100-mA of output current—all at a cost-effective price—is quite another matter.

The AD811 current-feedback op amp from Analog Devices is optimized for wide bandwidth and gain flatness when operating from a $\pm 15V$ supply. This device also solves the myriad problems presented by the demands of high-definition television (HDTV), medical imaging, and other video applications.

For example, compared with a bandwidth of 3.58 MHz for NTSC and 4.43 MHz for PAL standards, HDTV requires a gain flatness of 0.1 dB over a bandwidth of 30 MHz. At a gain of two, the AD811 meets this requirement handily while providing a minimum 3-dB bandwidth of 120 MHz. Moreover, differential gain and phase—key specifications for preventing color shifts and image distortion—are 0.01% and 0.01°, respectively. Another significant feature of the op amp is its ability to drive two back-terminated 75 Ω cables, an important consideration when using the amplifier as a line driver in video routers or distribution amplifiers.

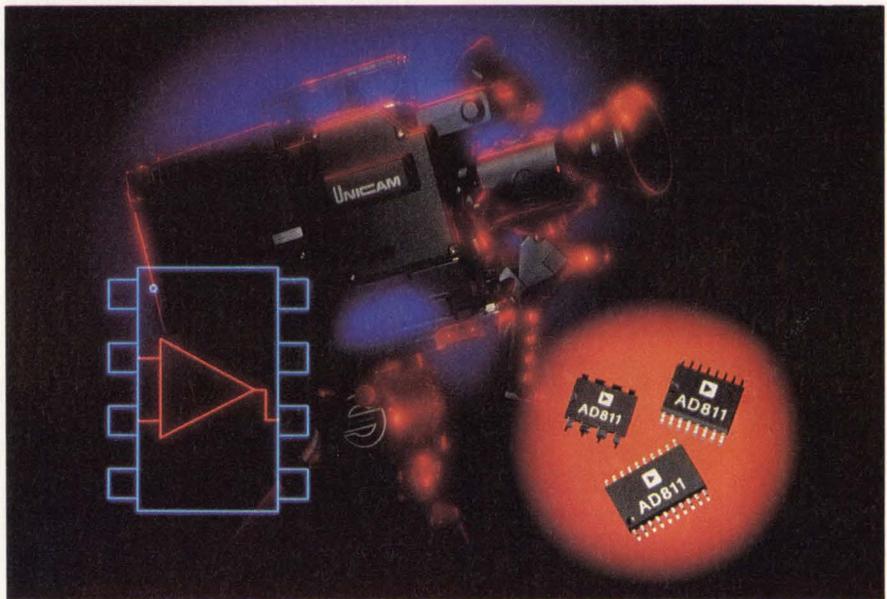
The AD811 is suited for medical-imaging applications, which require low noise and distortion. At 10 kHz, the op amp has a typical noise of

1.9-nV/ $\sqrt{\text{Hz}}$. At 10 MHz, THD is -74 dBc, and third-order intercepts occur at 43 dBm.

The op amp also suits high-speed pulse applications, such as infrared imaging and digital oscilloscopes, where transient response is critical. The device has a typical slew rate of 2500V/ μsec ; settling times are 25

other manufacturers that can equal the device's performance for a *single* specification, none combine the total performance capabilities of this op amp. Also, competing devices that exhibit similar performance can't match this op amp's cost.

The device is available in indus-



Designed for high-performance video applications, the AD811 op amp features a wide bandwidth, low noise and distortion, flat gain, and minimum phase error.

nsec to 0.1% for a 2V step and 65 nsec to 0.01% for a 10V step.

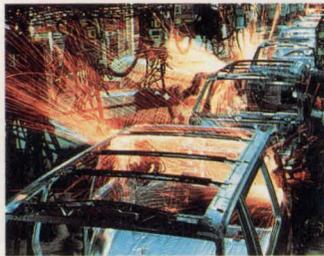
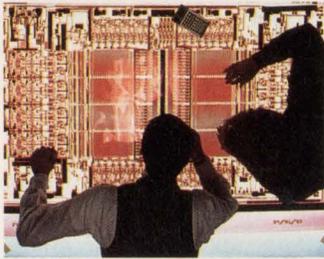
You can use the op amp as a buffer for ADCs and DACs or as a stand-alone gain stage: With a $\pm 15V$ supply, it has bandwidth of 140 MHz at unity gain and 100 MHz at a gain of ten. Even with a $\pm 5V$ supply, the op amp has a bandwidth of 80 MHz at unity gain and 70 MHz at a gain of ten. Full-power bandwidth (defined as a 10V p-p voltage swing) is 32 MHz.

Although there are devices from

trial (-40 to +85°C) and military (-55 to +125°C) temperature grades. Packages include 8-pin DIPs, 8-pin ceramic DIPs, 16- and 20-pin SOICs, and 20-pin LCCs. An industrial-grade device in an 8-pin plastic DIP costs \$3.35 (100) and \$2.85 (1000).—*Dave Pryce*

Analog Devices, 804 Woburn St, Wilmington, MA 01887. Phone (617) 937-2507.

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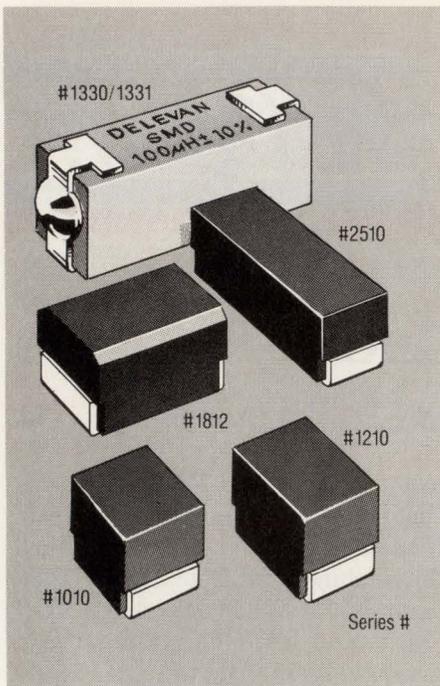
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EDN EDITORS' CHOICE

memory mix. The more registers there are, the higher the density should be. A built-in clock-distribution network minimizes skew, holding it to 1.3 nsec/clock.

The manufacturer is also fielding a programmer/tester for its arrays. The device ties into the arrays via a standard JTAG (Joint Test Action Group) port, taking four I/O pins running at 20 MHz. In addition, it provides parts pretests: a simple, 2-minute programming test and a production test. A JTAG boundary scan can test the programmed part. A developmental tool set back-ends standard CAE tools. It allows engineers to interactively hand-place and route, as well as automatically place and route. The tool set handles engineering change orders, and it allows users to freeze or thaw portions of the design for rework. The set provides a delay calculator and a pin and package editor.

The FPGAs use 3.5V internal logic, mainly to support 10V programming. As a side effect, the arrays consume less power than standard 5V parts. In addition, the transition to 3.3+ voltages for future systems will be easy, eliminating the present level translators at the I/O buffers.

The company uses a 0.75- μm , 2-level metal CMOS process for the arrays. The programmable interconnection is a metal-to-polysilicon antifuse with a native R_{OFF} of 1 G Ω and a programmed R_{ON} of 100 Ω . Each connection has low capacitance, measuring 0.65 fF per antifuse.

Each chip has five power and ground planes that have four decoupling capacitors. The devices come in ceramic PGAs (pin grid arrays), ceramic quad flatpacks, and plastic quad flatpacks. The CP20420 4245-gate FPGA will be available next month in a 155-pin ceramic PGA for \$277.70 (100). The programmer/tester sells for \$4000.—*Ray Weiss*
Crosspoint Solutions Inc., 5000 Old Ironsides Ave, Santa Clara, CA 95054. Phone (408) 988-1584. FAX (408) 980-9594.

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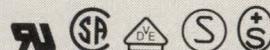
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8051 family gets second wind; new versions extend life of classic μ C

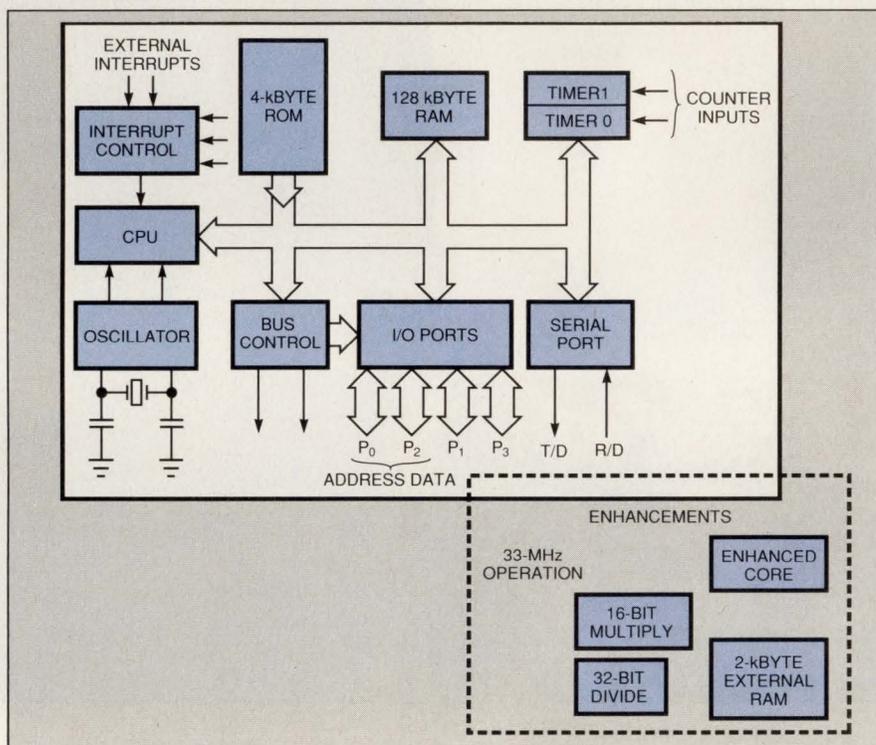
Old 8-bit microcontrollers don't quietly fade away, they just get more peripherals. And so the venerable 8051 family is quietly expanding as Intel and 8051 licensees continue to pour in additional capabilities.

Today's 8-bit 8051 carries a lot more muscle than did the early versions introduced in the late 1970s. The 8051's on-chip memory was initially limited to 128 bytes of RAM and 8 kbytes of ROM. Vendors have pushed beyond those limits to include as much as 2 kbytes of on-chip RAM and 32 kbytes of on-chip EPROM. Peripheral muscle has also been added to the microcontroller: as many as nine 8-bit I/O ports, multiple timers and counter arrays, and even a beefed-up math peripheral with a 32-bit divide and 16-bit multiply.

Processor speeds are up, too. Matra and Phillips Components (Sunnyvale, CA) have pushed clock rates to 30 and 33 MHz, respectively, from the original 12 MHz. Other efforts to speed up the 8051 family are focusing on the core's 12-clock-stage instruction cycle. Oki Semiconductor's reworked 8051, the nX 65 K series, executes instructions in four clock cycles, compared with the original 8051's 12 cycles.

New 8051 versions include

- Oki Semiconductor's one-time-programmable version of its nX 65K series. The architecture of this series is a superset of the 8051 architecture. The series has a fast core and 4, 8, or 16 kbytes of ROM and 128, 256, or 384 bytes of RAM. Prices start at \$6.51 (5000). Oki Semiconductor Inc, 785 N Mary Ave, Sunnyvale, CA 94086; (408) 702-1900. **Circle No. 734**



The 8051 is alive and well. The 8-bit microcontroller unit is gaining capability through new peripherals, faster implementations, and higher clock rates.

- Siemens's SAB/80C517A/83C517A-5. This 8051 version has an additional 2 kbytes of external RAM and as much as 32 kbytes of ROM. Its clock rate is as fast as 18 MHz. The device also has seven I/O ports, a 10-bit ADC (8 channels), six counters, eight 16-bit data pointers, a 16-bit-multiply and 32-bit-divide unit, and a 21-channel PWM. Prices start at \$15 (1000). Siemens Integrated Circuit Div, 2191 Laurelwood Rd, Santa Clara, CA 95054; (408) 980-4500. **Circle No. 735**

- Signetics's 83C524/87C58. This 512-byte-RAM version has as much as 32 kbytes of ROM or EPROM and runs as fast as 16 MHz. The chip includes two serial ports, three

timer/counters, and the company's I²C (Inter Integrated Circuit Bus) serial interface. Prices start at \$7.50 (10,000). Signetics Co, 811 E Arques Ave, Santa Clara, CA 94088; (408) 991-2000. **Circle No. 736**

- Matra's high-speed 8051s. Based on a fully static design, the 80C52, 80C32, and 80C154 now come in 25- and 30-MHz versions. The 80C154 also comes in 16- and 32-kbyte-ROM versions. The chips have three counter/timers, a full-duplex serial port, and 256 bytes of RAM. The 80C31 Ω -30 costs \$6 (10,000). Matra Design Semiconductor, 2895 Northwestern Pkwy, Santa Clara, CA 95051; (408) 986-9000; FAX (408) 748-1038. **Circle No. 737**

And over the last year, several vendors made some significant extensions to the 8051. Intel introduced its 87C58/80C58, which has as much as 32 kbytes of EPROM, and the 87C51FX, which has a set of programmable counter functions. And Signetics pushed out more microcontroller units with its chip-level serial bus, the I²C. This bus is part of Digital Equipment Corp's proposed Access Bus for low-speed desktop peripherals. It may become a standard.

Vendors continue to modify and extend the 8051 because of the device's popularity. Many engineers like the 8051 because of its many versions and the wide range of on-chip peripherals available. "With the 8051, if I need more power or different peripherals I can just go to another chip," says Jim Manley, director of electronic design at Span Instruments Inc (Costa Mesa, CA). Many take advantage of this prolific processor family to move to a higher-level language like C from assembly language. They pay for the additional overhead by moving to a more powerful chip.

The 8051 microcontroller has a rather baroque architecture. On one hand, it provides a complete set of processing operations including complex addressing and bit operations. The architecture provides memory-mapped I/O control.

On the other hand, Intel designers made some design compromises that complicate programming the device. For example, the 8051 has a complex addressing scheme that includes indexed, direct, and indirect addressing. But some addressing capabilities apply to only some

areas, thus segregating entities that share the same address space (special-function registers share the same space as external RAM, for example). Also, bit operations are confined to an addressing set of 128 bits in local RAM.

On the positive side, the 8051 has direct bit addressing, four register sets in RAM, and a pseudo-Harvard architecture with as much as 64 kbytes each for program and data memory. On the down side, off-chip memory accesses take an additional instruction cycle, making off-chip access expensive. Competing microcontroller units, such as the Motorola 68HC11, take the same time for on- and off-chip accesses. Also, the 8051 has one 16-bit pointer, which makes off-chip addressing difficult. However, Siemens has added a set of eight pointer registers to its 80C517A.

Many engineers find the 8051 easy to learn and program, but they find its peripherals complex. Intel, for example, has gone beyond the original two counter/timers by adding more counters, a programmable counter array, and an up/down counter. Similarly, other vendors have added their own versions of advanced counter peripherals.

Designing in 8051s can be easy. Dallas Semiconductor Corp (Dallas, TX) offers an 8051 superchip, the DS5000. The device is a hybrid: Inside is an 8051 CPU, 8 or 32 kbytes of RAM, and a battery backup—in other words, a complete system.

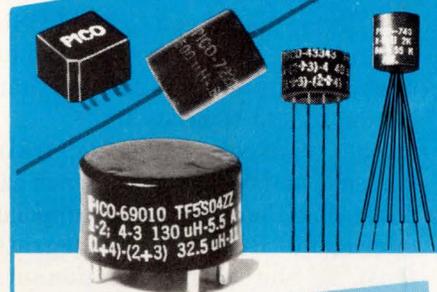
—Ray Weiss

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Transceiver IC handles both T1 CSU and ISDN primary-rate interfaces

The LXT310 transceiver integrates most of the elements of a T1-rate telephone channel-service unit (CSU) with ISDN primary-rate interface compatibility into one IC. The device allows you to build CSU capability into other customer premise equipment rather than having to add separate units.

The transceiver has separate transmit and receive ports, each capable of either bipolar or unipolar operation. Both ports integrate most of the active components needed for connection to the telephone network, requiring only isolation transformers and impedance-matching resistors to complete the interface. The device complies with relevant industry standards, including ANSI T1.403 and 408, FCC part 68, and AT&T Pub 62411.

The transmit port can drive signals through twisted-pair cable as long as 6000 feet. To handle shorter cables without needing tuned output circuits, the port offers selectable frequency-dependent line build-outs. You can select 7.5, 15, 22.5, or 0 dB of attenuation.

The receive port has a programmable receive equalizer. To increase noise margin in shorter loops, you can limit the maximum equalizer gain to 26 dB; otherwise, you can allow the gain to range to 36 dB. Using a status I/O pin, the receive channel reports on the line insertion loss as indicated by the equalizer gain setting.

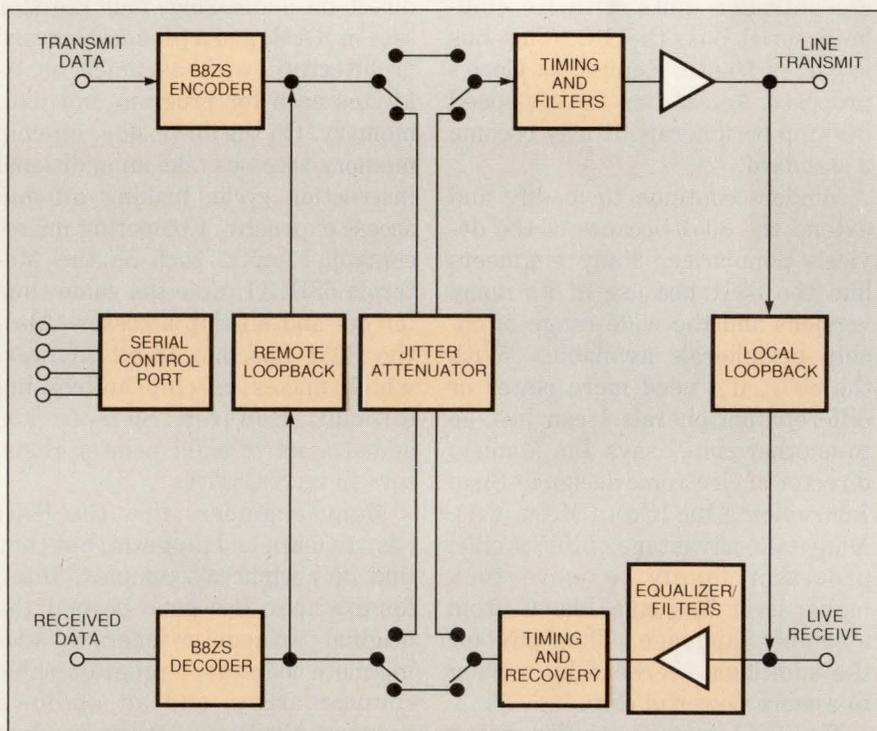
The transmit and receive channels both have selectable B8ZS encoder/decoders. In addition, the channels share a low-frequency (3-Hz) jitter-attenuator circuit. You can select which channel uses the attenuator. The attenuator stores incoming data in a FIFO register,

then reclocks the data. The output clock adjusts by intervals as small as $\frac{1}{8}$ of the clock period.

The transceiver offers several diagnostic features. For example, you can set the transmit section to produce a continuous stream of 1s at the transmit clock frequency to test the cable. You also have a choice of two loopback tests. The local

or software methods for controlling the device. The hardware method uses hardwired control pins and coded signals on data pins to select the various operating conditions. If you prefer software control, the device offers a serial communications port for exchanging commands and status information.

The LXT310 operates from a 5V



Packing most of a channel service unit (CSU) into one IC, the LXT310 allows you to embed CSU capability into other types of equipment.

loopback test routes the transmit output lines to the receive input lines, allowing you to test the entire on-chip data path. The remote loopback test routes the recovered receive data to the transmitter section so that the device acts as a repeater. You can activate the remote loopback test either at the chip or through the telephone network.

You have a choice of hardware

supply and typically consumes 300 mW. It comes in a 28-pin PLCC (plastic leaded chip carrier) and ceramic and plastic 28-pin DIPs. Prices are \$30 to \$33, respectively (1000). —Richard A Quinnell

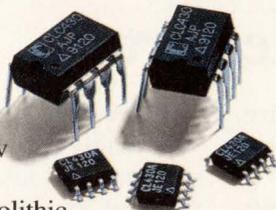
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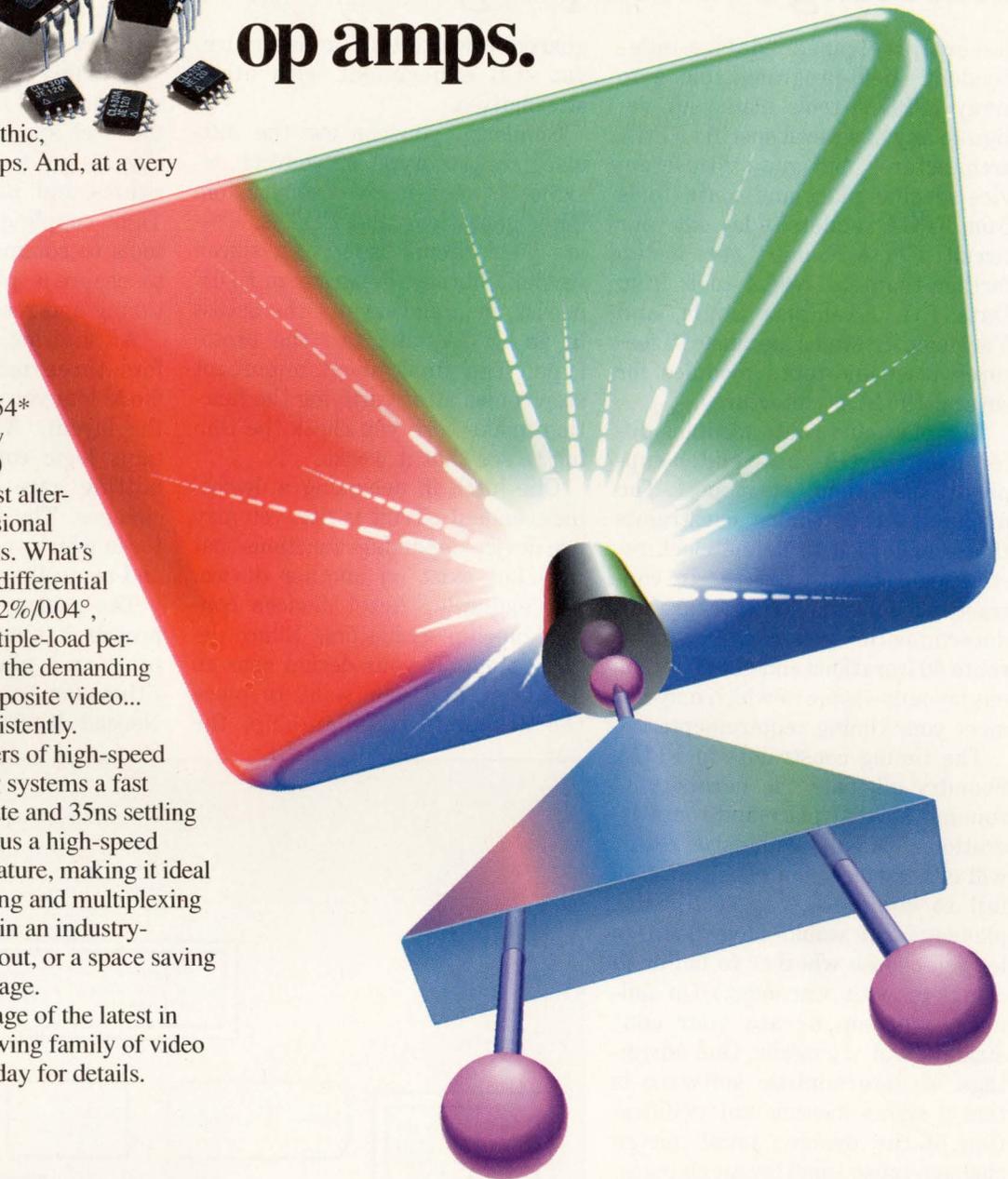
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Software package lets you postpone selecting of field-programmable parts

Recently released "device-independent" field-programmable gate array (FPGA) tools map your design to any of several specific FPGA architectures, but you still use device-specific place-and-route tools from FPGA vendors to lay out your circuit. FPGA Foundry goes a step further than the recent tools from Data I/O, Exemplar Logic, and Viewlogic Systems because it features place-and-route modules for several FPGA architectures.

The place-and-route modules differ from FPGA-chip-vendor-supplied tools in one key respect: The modules accept timing constraints that enable you to define clock restrictions or path delays. In contrast, vendor-supplied tools are not deterministic; you can place and route 50 iterations and get 50 different layouts—some of which may not meet your timing requirements.

The timing constraints in FPGA Foundry alleviate the necessity of running several place-and-route iterations; the deterministic result will either meet your constraints or fail to complete. (A better implementation would have been to let you choose whether to fail or to complete with warnings.) On failures, you can derate your constraints and try again. One advantage of deterministic software is that it allows incremental modification of the design; small design changes cause small layout changes.

The software provides device-independence by converting your design into low-level-logic intermediate data structures. Although your data is converted, the software still maintains whatever device-specific information you provide as part of the structure. As a result, you can design to a particular FPGA using macrocells and logic

geared toward that architecture, yet still experiment with other alternatives.

Similarly, you can use the software to prototype or convert designs between masked semicustom implementations and FPGAs. Create your circuit using your silicon vendor's library, generate an EDIF netlist, map and lay out the netlist in an FPGA, and test the prototype. The final, most important step comes after verifying the function; make sure you check the timing to see that it works.

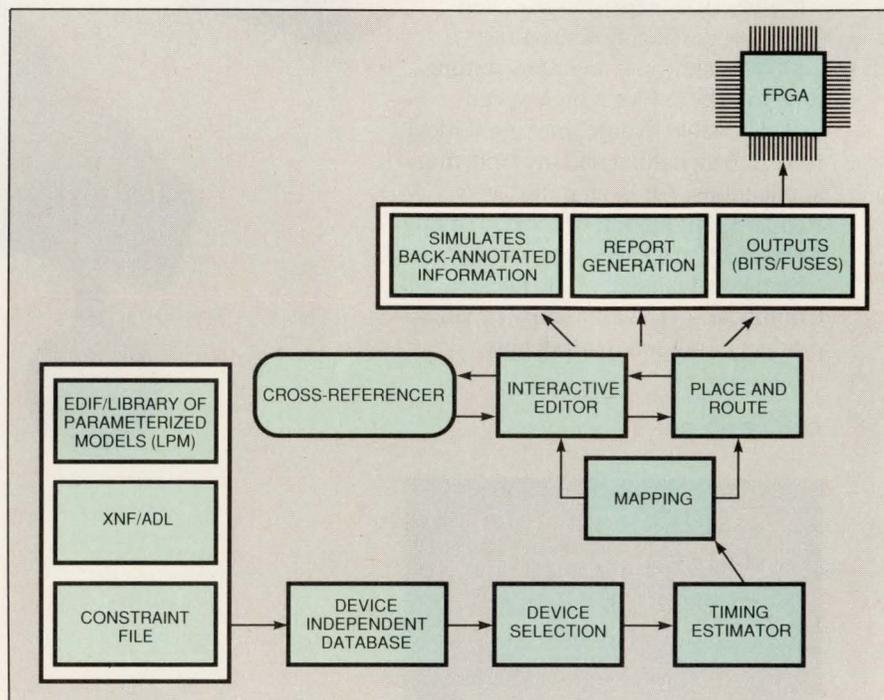
One hitch in designing a device-independent circuit is that you may use device-dependent functions that may not exist on another device. For example, Actel devices contain on-chip oscillators, Xilinx devices don't. If your design uses an oscillator and you want to place the design in a Xilinx chip, the

software won't lay out the circuit.

A timing estimator is part of the software tool kit. This module uses the clock speed and levels of hierarchy to guide the mapping algorithms and place-and-route tools. Tight coupling enables all of these tools to communicate during a run to ensure a placement that meets timing and resource constraints.

An interactive graphic editor offers three modes. The read-only mode lets you view and interrogate the layout. A second mode maintains logic consistency while permitting gate and implementation changes. The third mode is an editor in which you can manually place-and-route the entire design.

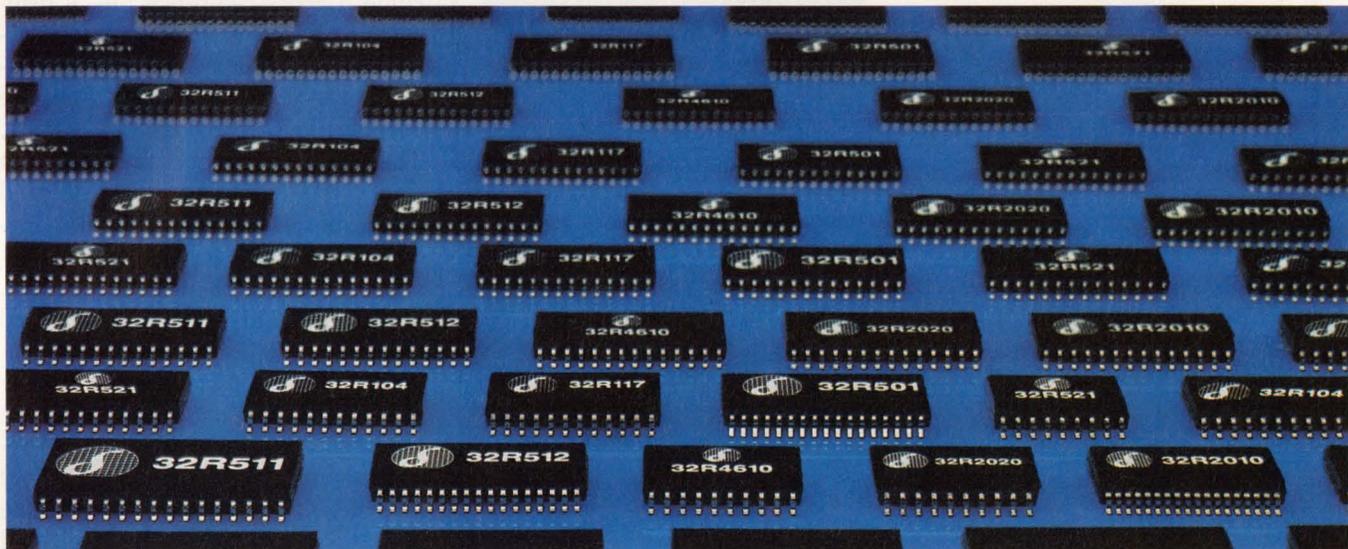
The package uses a modular approach that currently includes mapping and place-and-route algorithms for Actel and Xilinx FPGAs. Neocad developed these algorithms



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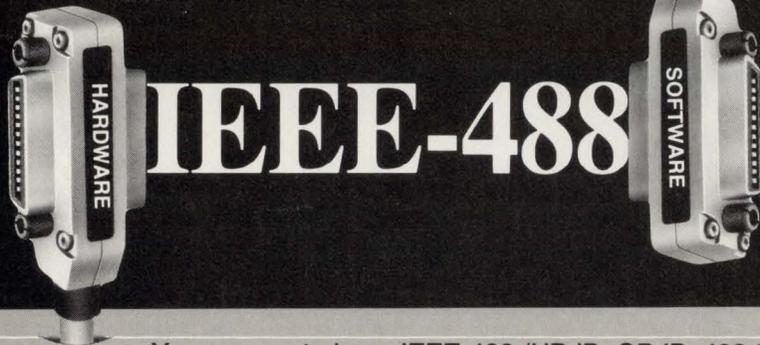
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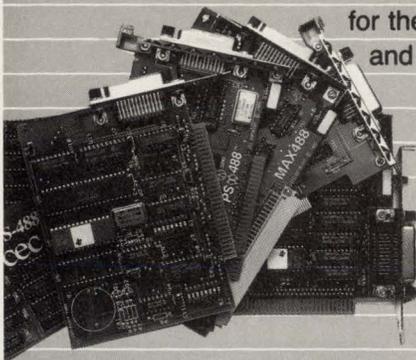
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without assistance from either company.

Support for devices from other FPGA vendors is under consideration. When available, these algorithms will be delivered as optional modules costing roughly \$5000 to \$7500 on the PC.

The software currently accepts design data in several formats. EDIF 2 0 0 and LPM (Library of Parameterized Models) standard formats as well as Xilinx- and Actel-specific formats are presently supported. Hooks written into the code will let the tool accept data from CAE- and ASIC-vendor libraries.

Outputs from the software include a cross-reference file, a utilization report, a file containing actual timing delays for back annotation into your simulator, and the output file to program the FPGA. The cross-reference file lets you find buried, replaced, or deleted nodes between schematic and layout. The report generator provides feedback on path and net delays, logic block and I/O utilization, and remaining FPGA resources.

The company is also separately offering its Xilinx place-and-route module. This module does not provide device independence—it only lays out Xilinx FPGAs. The module piggybacks off the Xilinx front-end tools. This software uses the Xilinx intermediate format and, therefore, doesn't support timing. Its cost starts at about \$8000.

Written in C++, the software runs under Windows on DOS workstations and on Unix-based workstations running X-Window and Motif. The company claims the software will be available in January, starting at \$18,000.

—**Michael C Markowitz**

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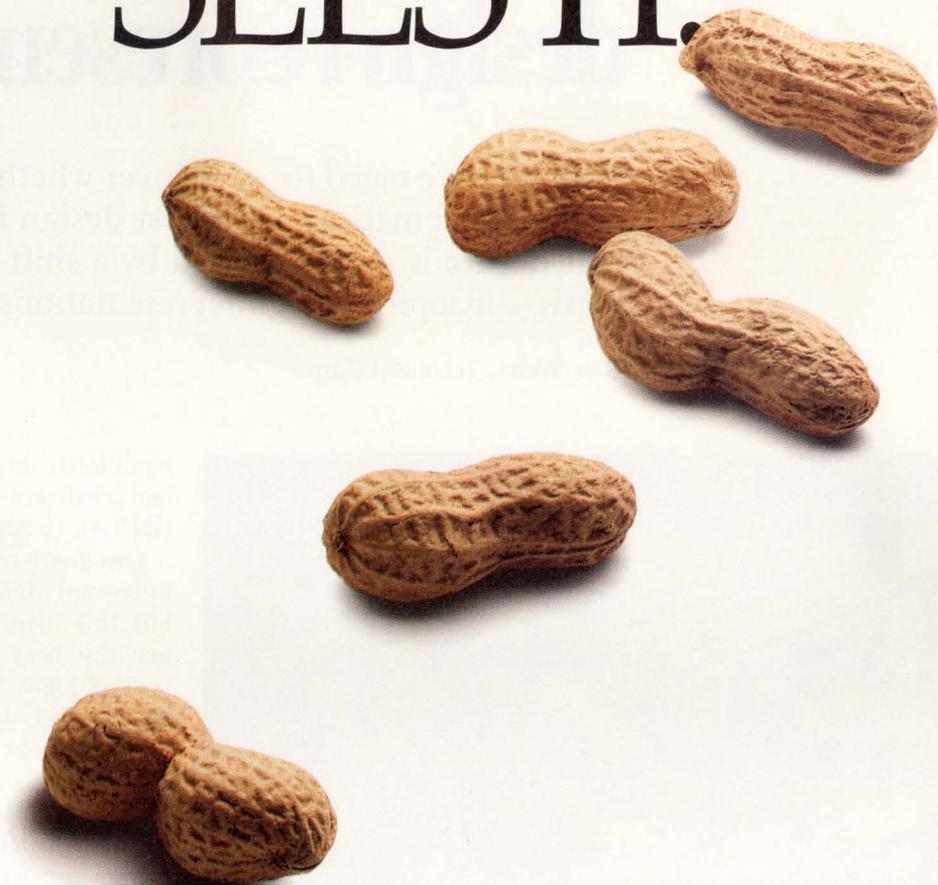
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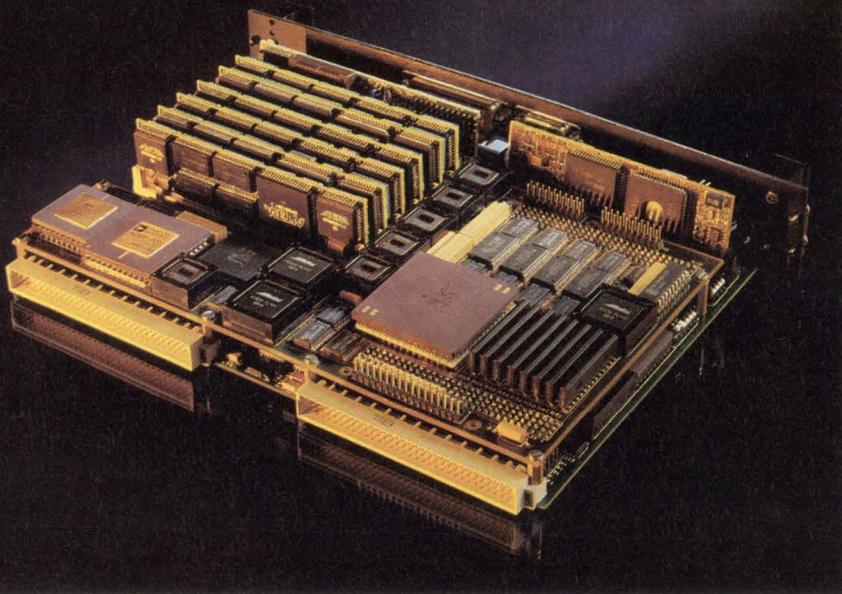


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Schematics battle equations for design representation

Debates have raged for years over whether equations or logic schematics are the best design form. Today, that debate is overshadowed by a shift toward synthesis—mapping design representations into silicon.

Ray Weiss, Technical Editor



Holding the equivalent of 20 modules, the Dacube Maxvideo 20 high-speed video processor uses only a single card. Typical of high-end designs, the pipelined processor uses a range of logic: ASICs for density and speed; EPLDs and FPGAs for integration; and PLDs for fast glue logic.

IN THE “GOOD OLD DAYS,” engineers had total control over their designs. Schematics, with gate-level design, ruled. If you drew it, you had it; a gate on a schematic was a gate on the board. Not so today—the designer-to-board connection is not as close, and schematics must compete with

equations, as well as truth tables and hardware description languages (HDLs), to represent designs.

Designers no longer have just one universal design representation, but this diversity means they can use the best mechanism for each type of logic. “We use what works. We do PAL [programmable array logic] devices in equations,” says Bob Donaldson, chief engineer at Annapolis Microsystems (Annapolis, MD), “and we use mainly schematics for FPGAs [field-programmable gate arrays]—they let us get close to the configurable-logic-block cell structure for efficient design.” However, opinions of what is best for each type of logic keep shifting.

But more is going on than just a simple competition between schematic-level and equational design methodologies. Engineers are turning to sophisticated tools to optimize and map their designs into silicon. Even with a gate-level schematic, tools may translate and optimize that design into an unrecognizable gate-level implementation.

Design methodologies and tools

are tied closely to the underlying implementation logic. Logic schematics, for example, meshed well with traditional 5400/7400 TTL SSI and MSI ICs. Over the last 30 years, three major logic waves have impacted engineers' design methods and representation (see **box**, "Logic waves").

The shift to equations

Programmable logic is responsible for a large-scale shift in design methodologies from logic schematics to equation-based design. During most of the 1970s and 1980s, programmable logic was largely ignored by mainstream CAE. Today, the majority of board-level designers work with programmable logic.

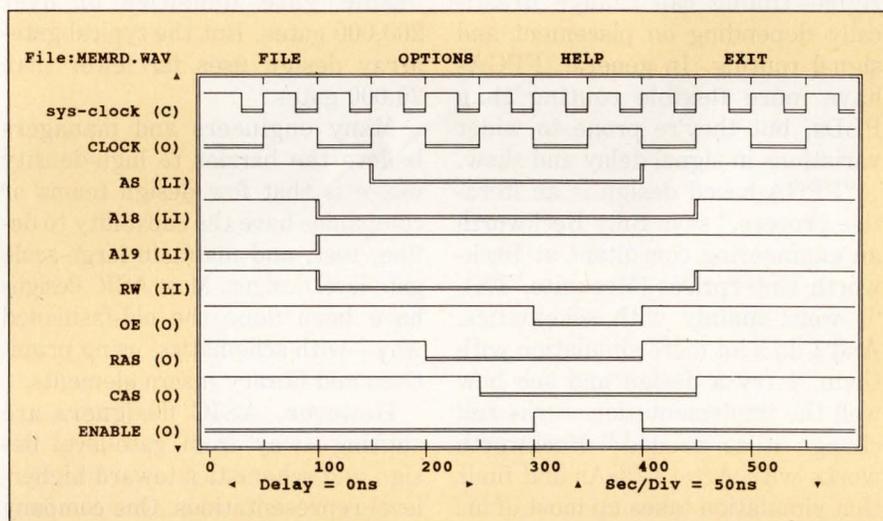
However, because of its early isolation, programmable logic developed its own brand of representations, including fuse maps and various equational forms. Hardware languages, such as Palasm, Cupl, Abel, and AHDL, evolved during this time for programmable as well as standard logic.

PLDs had fixed logic forms that lent themselves well to easy equational representations. PLAs had a sum-of-products form, with an AND array feeding into a selectable OR array. PAL devices simplified this structure by linking the AND array into a fixed OR array, linking each output to a fixed OR, and having a set number of AND-gate inputs. These PLA and PAL-device structures made it easy for designers to write simple AND/OR equations that mapped directly into the programmable silicon. Not only that, if a design needed changing, designers could simply reprogram a new part, or, with EPLDs, erase the old design and replace it.

PLAs and PAL devices now basically own the board-level design world. "This is the age of PAL-device design," says Trevor Marshall, president of Yarc Systems Inc

(Newbury Park, CA). In achieving dominance, PLDs led design into the world of equations: Most PLD designs are done in equations or a PLD language.

EPLDs and FPGAs have emerged to deal with logic problems beyond the PLD's grasp. They are large-scale programmable devices with higher pin counts and gate counts than PLDs. Typically, they are built around one or two core logic



cells. These cells typically take on the form of one or more flip-flops with some output control (enable, complement), front-ended by a simple logic-input set.

These larger programmable devices are having a major effect on design methodologies. Many designers are turning back to logic schematics to work with EPLDs and FPGAs. According to Stan Kopeck, Altera's director of strategic marketing, "over 70% of the EPLD designs are now done with schematics." For one thing, by using schematics you can build a design that approximates the underlying cell structure. For another, schematics lend themselves well to using the vendor-supplied macro cells for larger functional components.

The basic difference between EPLDs (erasable PLDs) and

You don't have to use logic schematics or equations to represent logic. Minc's PLDesigner software lets you use waveforms to represent PLDs. The circuit shown enables a microprocessor to read data from dynamic memory. Inputs appear as (LI) and outputs appear as (O).

FPGAs (field-programmable gate arrays) is that EPLDs use a hierarchical logic structure and fixed routing to combine cells, whereas FPGAs tend to follow the gate-array model, embedding a set of cells in a flat routing structure.

Designing for EPLDs and FPGAs is much more complicated than writing a set of equations for a simpler PLD. Placement and routing become critical for many designs—timing can change drastically depending on placement and signal routing. In general, FPGAs have more flexible routing than PLDs, but they're prone to wider variations in signal delay and skew.

"FPGA-based design is an iterative process," says Billy Beckworth an engineering consultant at Beckworth Enterprises (Mesquite, TX). "I work mainly with schematics. And I do a lot more simulation with them. I try a design and see how well the implementation works and change it as needed." Beckworth works with Actel FPGAs and finds that simulation takes up most of his design cycle.

With EPLDs and FPGAs, designers must map their logic into a collection of cells. This method is somewhat similar to designing with MSI-type logic, but mapping EPLDs and FPGAs into cells only lets designers use one or two MSI functions. However, some EPLD and FPGA cells allow designers to use elements in a cell for different macros or designs. In a Quicklogic (Santa Clara, CA) FPGA, for example, each cell can be treated as three separate elements for design.

Many EPLD and FPGA designers use vendor-supplied macros as design elements. The macros are optimized MSI components made up of cells. These macros serve as logic blocks and lend themselves well to schematic-based design.

ASICs have led large-scale design. But ASIC design levels have

"Programmable logic is the TTL of the 90s... My advice is to just dive in and start using it."—J Stewart Dunn

been growing slowly. Vendor capabilities have far outstripped mainstream usage. Vendors can deliver usable gate densities of over 200,000 gates. But the typical gate-array design uses far fewer than 20,000 gates.

Many engineers and managers believe the barrier to high-density usage is that few design teams or companies have the capability to define, test, and maintain large-scale gate-level designs. Most ASIC designs have been done the old-fashioned way—with schematics, using primitives and library macro elements.

However, ASIC designers are shifting away from gate-level design and schematics toward higher-level representations. One company shifting its ASIC-design methods is Teradyne Semiconductor Test Division (Agoura Hills, CA), which builds high-performance VLSI testers having hundreds of ASIC chips. "We're going to VHDL and logic synthesis," says Ben Brown, hardware engineering manager. "We used gate-level design at up to 200 MHz for our J971 tester. We averaged about a man year per ASIC on it. As chip densities go up, we need to up our productivity. HDL-based design offers a way up. There are some things I have some problems with, such as verification at the language level. But we've talked to a lot of users and feel it will work for us."

Almost all the major computer and workstation vendors are working with an HDL and logic synthesis. For example, IBM has designed its mainframes for years using this

combination. Similarly, Sun Microsystems uses an HDL for its workstation designs.

HDLs, such as Verilog and VHDL, enable engineers to describe their designs at a behavioral or register-transfer level and to verify the designs through simulation rather than breadboarding. However, until recently the HDL-based design had to be hand translated down to a gate-level design.

Some logic-synthesis tools can overcome that problem. These tools translate the HDL-based design into a silicon implementation. Synthesis tools from Synopsys, Mentor Graphics, Racal Redac, Exemplar, and Viewlogic optimize implementations to meet user-defined speed or area constraints. One of the major benefits to synthesis is a level of independence from the underlying silicon. Engineers can move their designs to different ASIC families, different vendors, or even different silicon technologies.

This new combination of HDLs and synthesis is a major force in the ASIC-design shift from schematic logic to equational forms. Many engineers predict that within five years the bulk of ASIC design for glue and control logic will be in an equational form.

However, all is not perfect yet. Synthesis is still at the logic-chunk level—designers must partition their designs into synthesizable chunks by trial and error. Also, synthesis comes up short in critical areas such as clock distribution and high-speed buffering with latches.

Bucking the trend

Over the last decade, equations have steadily advanced into the schematic world. A key factor has been the engineering shift to equation-based PLD design. Now, however, that invasion shows signs of losing momentum as engineers shift back to schematic based design for the

Logic waves

Design representations (schematics and equations) closely connect to their underlying logic. So as engineers have moved from logic family to logic family, the design representations they've used have also shifted. The last 30 years have seen three major waves in mainstream logic design:

- 5400/7400 SSI/MSI (TTL forms)
- programmable, packaged logic (PLDs: PLAs and PAL devices)
- large-scale logic (EPLDs, FPGAs, and ASICs).

In the first wave, the logic-design community reached an unparalleled degree of commonality and standards. Designers expressed most logic in standard SSI (small-scale integration) and MSI (medium-scale integration) forms. Engineers could go to any company and be comfortable with their design representations (everybody used the same design templates to draw their logic).

The second logic wave started in the 1970s with the emergence of programmable logic. When traditional schematic forms proved cumbersome, designers shifted to equational representations, which fit the sum-of-products structure of programmable logic. Engineers used simplified hardware languages, such as Abel, Cupl, and Palasm, as well as other forms, such as truth tables and even schematics, to design devices.

The third logic wave has paralleled the first two waves, slowly picking up momentum over time. This third wave, large-scale chip design, includes both

ASICs and emerging large programmable logic: EPLDs (erasable programmable logic devices) and FPGAs (field-programmable gate arrays). Larger designs built on more flexible logic components reflect these devices' greater complexity. Most third-wave design activity is at the schematic logic level; however, ASIC designers, particularly those tackling large designs, are turning to equational forms, using hardware description languages such as VHDL and Verilog.

You can view these three design waves and their underlying silicon as a silicon continuum, ranging from 5400/7400 TTL to gate arrays and standard cells. **Fig A** shows this continuum as one axis, with design mapping as the other axis. At the far extremes—SSI/MSI discretes and high-speed ASICs—most design is at the gate level and has a one-to-one mapping to the raw logic primitives.

However, as design moves from the earlier 5400/7400 components to more modern chips, engineers increasingly rely on design tools to optimize and map their logic into the target circuitry. PLA, PAL-device, and GAL (generic array logic) designers use optimizers and hardware languages. EPLD and FPGA designers rely on optimizers as well as place-and-route tools to map logic to the underlying FPGA cells. And ASIC designers are increasingly turning to synthesis (a software-based logical mapping) and HDLs.

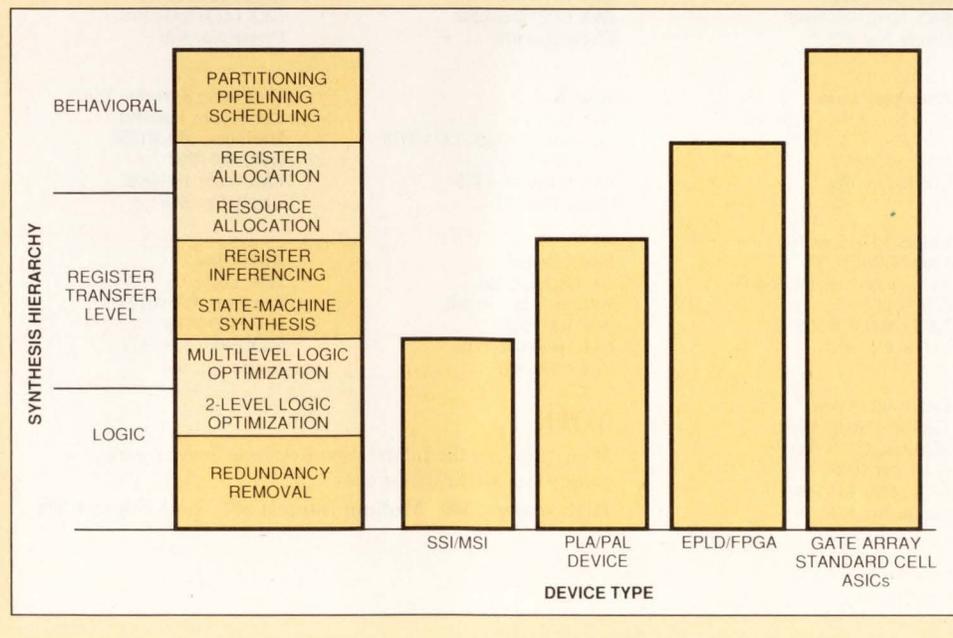


Fig A—Levels of logic synthesis and optimization are related to the underlying logic families. Larger and more complex chips lead to more logic optimization and synthesis. Behavioral synthesis is just starting to be viable.

higher-density EPLDs and FPGAs.

EPLD and FPGA vendors provide a path for engineers to stay with schematic-level design using libraries of vendor-supplied macros. Engineers can cobble together their designs using macro building blocks; and they can do so using schematics.

"I use schematic entry for FPGAs," says Highgate's Steve Wasson. "We build our own equivalents to the vendor's macros for efficiency. And we lay out a design in schematics and then tweak it to get high density and efficient routing. Schematics let us see what is happening and serve as a final design medium. We put constraints on the design, such as which pin aligns to what signal. With careful work we can get 75 to 85% gate usage."

"We use equations for PAL de-

"PAL devices are a tremendous bargain: they're fast and inexpensive. They're easy to use—just write the equations out."
—Trevor Marshall

vices, and generally schematics for the larger PLDs," says J. Stewart Dunn, vice president of R&D at Databcube (Peabody, MA). "With PAL devices, it was easy to see if a design would fit into a part. With the larger programmable parts, some designs won't fit. And we either redo the design or do hand fitting and routing. In general, equations are much faster—you can change a design in a few hours and have a

new part—whereas changing a schematic can take two days. However, for larger PLDs, schematics are the best way now to do design and map into the hardware."

Designers don't have to stay with schematics, they can choose from HDL alternatives. For example, Altera developed its own hardware language, AHDL. The language is basically an extension of the Abel-like languages, which feature simple logic equational forms. AHDL, however, supports hardware modules (subdesigns)—designs can be made up of multiple logic modules. Also, Data I/O's Abel now supports a number of EPLDs and FPGAs as well.

The verdict isn't in yet on which design representation is preferable for EPLDs and FPGAs. New tools are emerging that open FPGA de-

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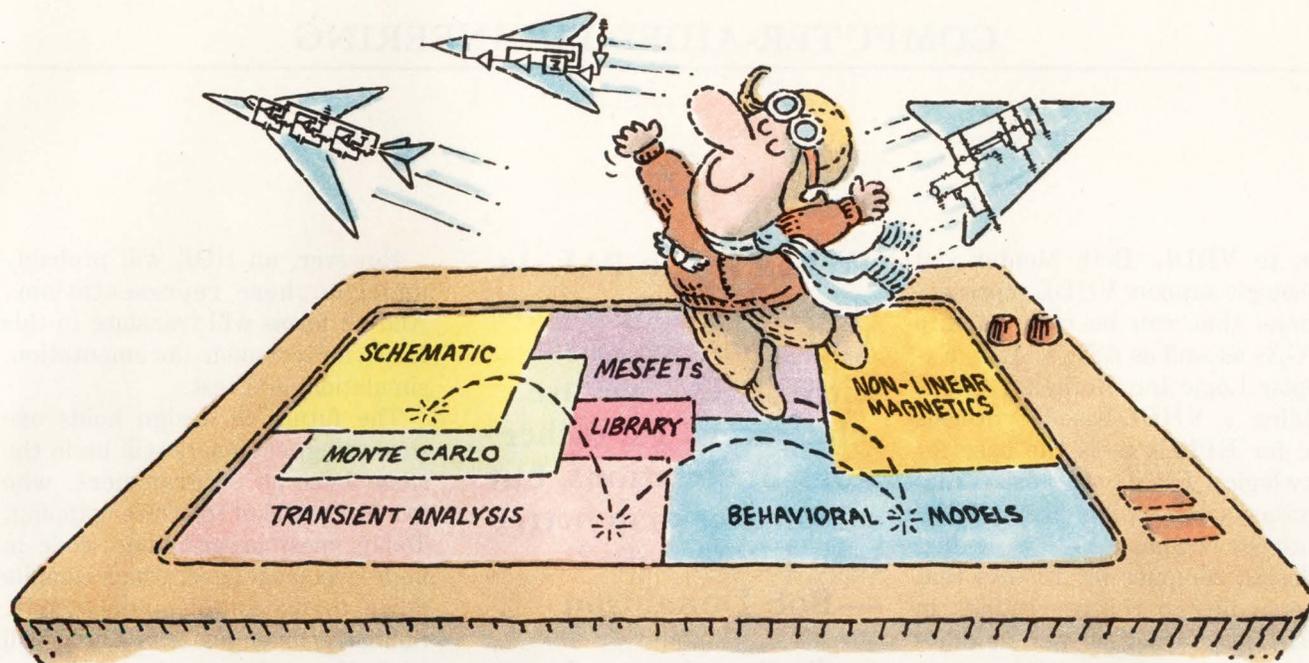
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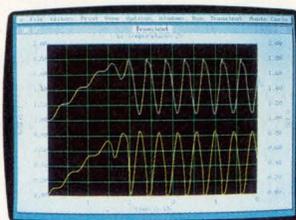
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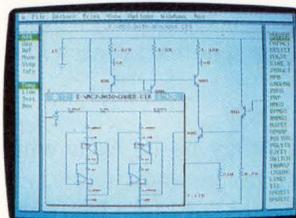
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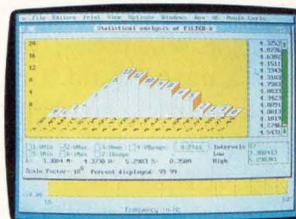
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sign to VHDL. Both Mentor and Viewlogic support VHDL representations that can be mapped into FPGAs as well as ASICs. Also, Exemplar Logic Inc (Berkeley, CA) is fielding a VHDL-based synthesis tool for EPLDs (it is the base for Viewlogic's EPLD synthesis). And Synopsys, the pioneering ASIC synthesis company, is now fielding a design compiler for FPGAs that accepts design representations in VHDL or Verilog as well as state tables, equations, or netlists.

Schematics reborn

Schematic capture is becoming more than just an entry tool for logic gates and MSI (medium-scale integration) parts. Instead, schematics are becoming the front end for management of top-down designs. They provide a graphical, hierarchical mechanism to climb down the design tree from a top-level block diagram to detailed logic diagrams and openings to code.

Thus, schematics can serve as the access mechanism for VHDL code as well as for other representations, including truth tables, state-machine diagrams or equations, and waveforms. For example, Mentor Graphics' Design Assistant allows engineers to describe their designs at a block level, with blocks then opening up into VHDL code. Users can define a block, and the system will create a VHDL code stub ready for coding. The schematic interface shows linkage between modules in addition to providing a top-down view.

OrCAD fields a development environment, ESP, that integrates schematic capture, PLD design tools, a simulator, and board-layout packages. You can access PLDs specified in the schematic via the other tools and examine or simulate the underlying source code. Addi-

**“When we do PAL devices, we use equations. And when we work with FPGAs, we use schematics. I'd rather work in equations, but schematics map better into FPGA cells.”
—Bob Donaldson**

tionally, the system transforms traditional logic (using special primitives) into PLD equations. The schematic serves as the overall controlling element.

Xilinx's Blox, a new schematic-based FPGA design tool, further encourages using schematics in engineering. Blox enables engineers to work with large parameterized modules. These modules or blocks are chunks of standard logic functions, such as adders, buses, and registers, whose width can be automatically adjusted. You only have to change one parameter on any one of the interconnected blocks to have the design automatically scale to a new size. Blox is an FPGA equivalent to the silicon compiler module generators. It accepts design input from the major schematic entry systems.

No winners

There may be no clear winner in the battle between equations and schematics at all. Instead of a wholesale adoption of hardware description languages or a retreat back to logic schematics, we may end up in a mixed world. Graphics and functional blocks may represent logic subsystems and functions. And those blocks may be in different representational forms, such as truth tables, equations, logic gates, or HDL descriptions for complex control logic.

However, an HDL will probably underlie these representations. And all forms will translate to this HDL for common documentation, simulation, and test.

The future of design holds one sure thing: engineers will be in the same boat as programmers, who live in a world of software mapping. Today, most programmers code in high-level languages, which compile down to executable object code. Similarly, an engineer's designs will pass through a tool-translation layer, which will map them to silicon. Thus, engineers, like programmers, will be increasingly dependent on their tools.

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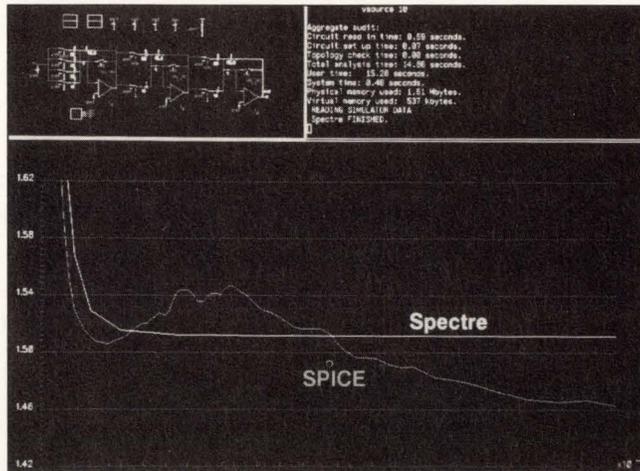
ZYCAD

Spice-compatible simulator improves convergence, capacity, and capability

Spectre from Cadence Design Systems is a circuit simulator that is written in C and uses modified Spice-based algorithms to improve convergence. Because the simulator is written in the C language, it uses a computer's memory more efficiently than Fortran-based Spice does. The simulator also uses data structures whose efficiency lets you simulate large circuits in half the memory other versions of Spice require.

Three features let the circuit simulator simulate faster than Spice. First, the simulator uses a more efficient sparse-matrix algorithm to calculate voltages and currents. And because the software uses a node-based algorithm rather than a device-based one, the simulator performs fewer calculations. Finally, the simulator uses automatic time-step control to minimize calculations when circuit voltages and currents are stable.

The simulator accepts both C-



language user-compiled models and standard Spice models. Among the models included are the Gummel and Poon BJT (bipolar junction transistor) model, five MOSFET models (MOS1, MOS2, MOS3, BSIM1, and BSIM2), a GaAs MESFET model, and standard diode models.

The simulator runs on most work-

stations and is integrated in the vendor's Analog Artist design framework. The software costs \$30,000 for a single-user license.

Cadence Design Systems Inc,
555 River Oaks Pkwy, San Jose,
CA 95134. Phone (408) 943-1234.
FAX (408) 943-0513.

Circle No. 684

CAE tools ease mixed-signal design for digital designers

MSDS is a suite of software tools that automates and simplifies mixed-signal ASIC designs. The Analog Model Builder uses your performance requirements as inputs to a compiler that adjusts model parameters for 17 analog functions such as filters, DACs, ADCs, comparators, references, and regulators. The software creates a simulatable behavioral model and schematic symbol for cells in the MSDS library and produces specifications for custom cells.

The Design Critiquer compares

your design against a set of rules that highlight potential design flaws. Another component of the tool suite is the Parameterized Analog Building Block Generators. The generators use files created by the model builders to generate silicon-level implementations of the functions you need.

Multiplexer cells modeled and characterized for accurate simulation are coupled to each of the analog building blocks. The simulator automatically inserts these blocks into your design, but you have the

option of removing any of the multiplexer cells.

The tool suite also includes Mentor Graphics's schematic-capture software and the Saber/Cadat mixed-signal simulation software. All of the pieces of the tool kit are integrated under an X-Window-compliant graphical user interface. The software is available now; prices start at \$75,000.

Gould AMI, 2300 Buckskin Rd,
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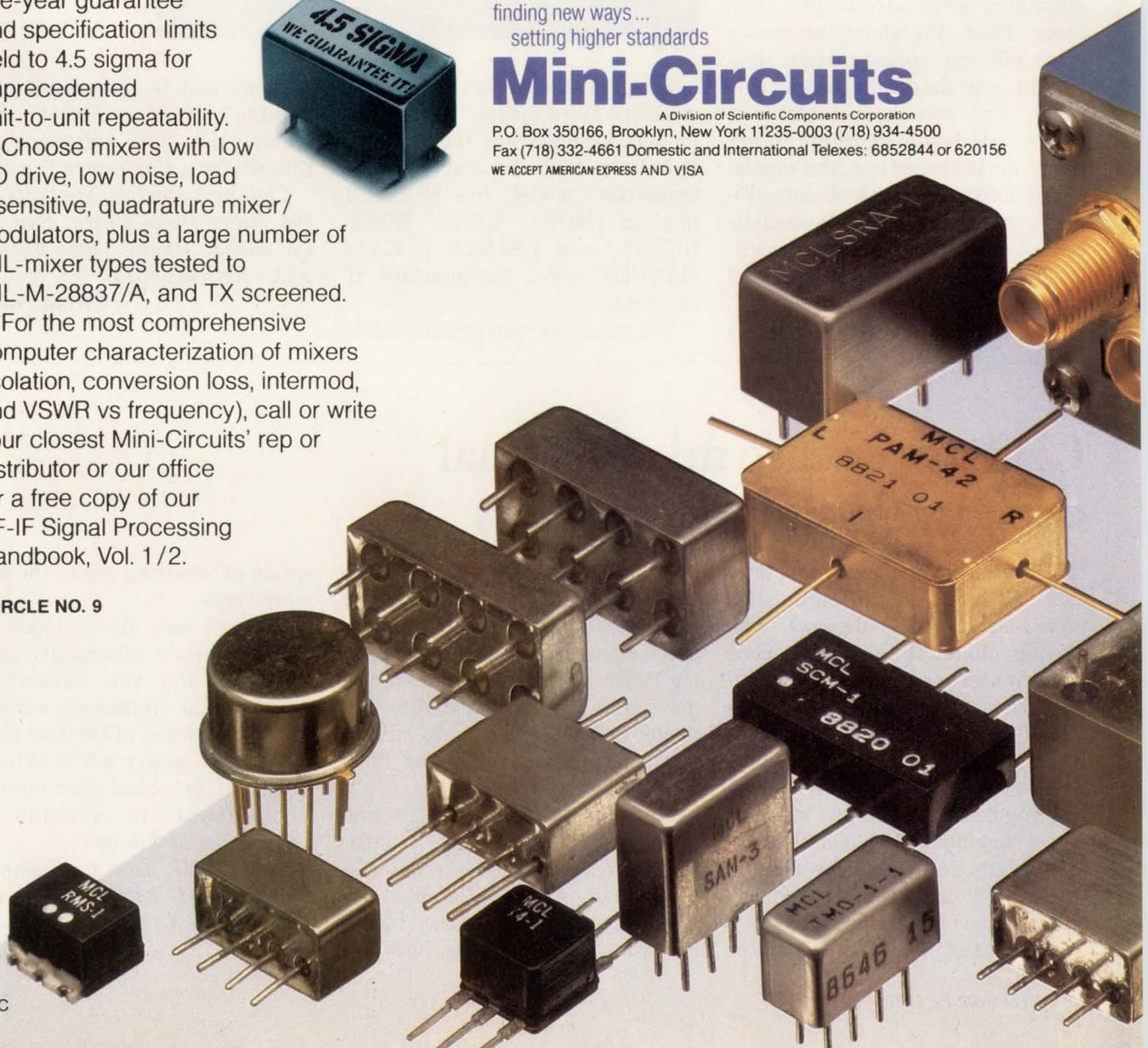
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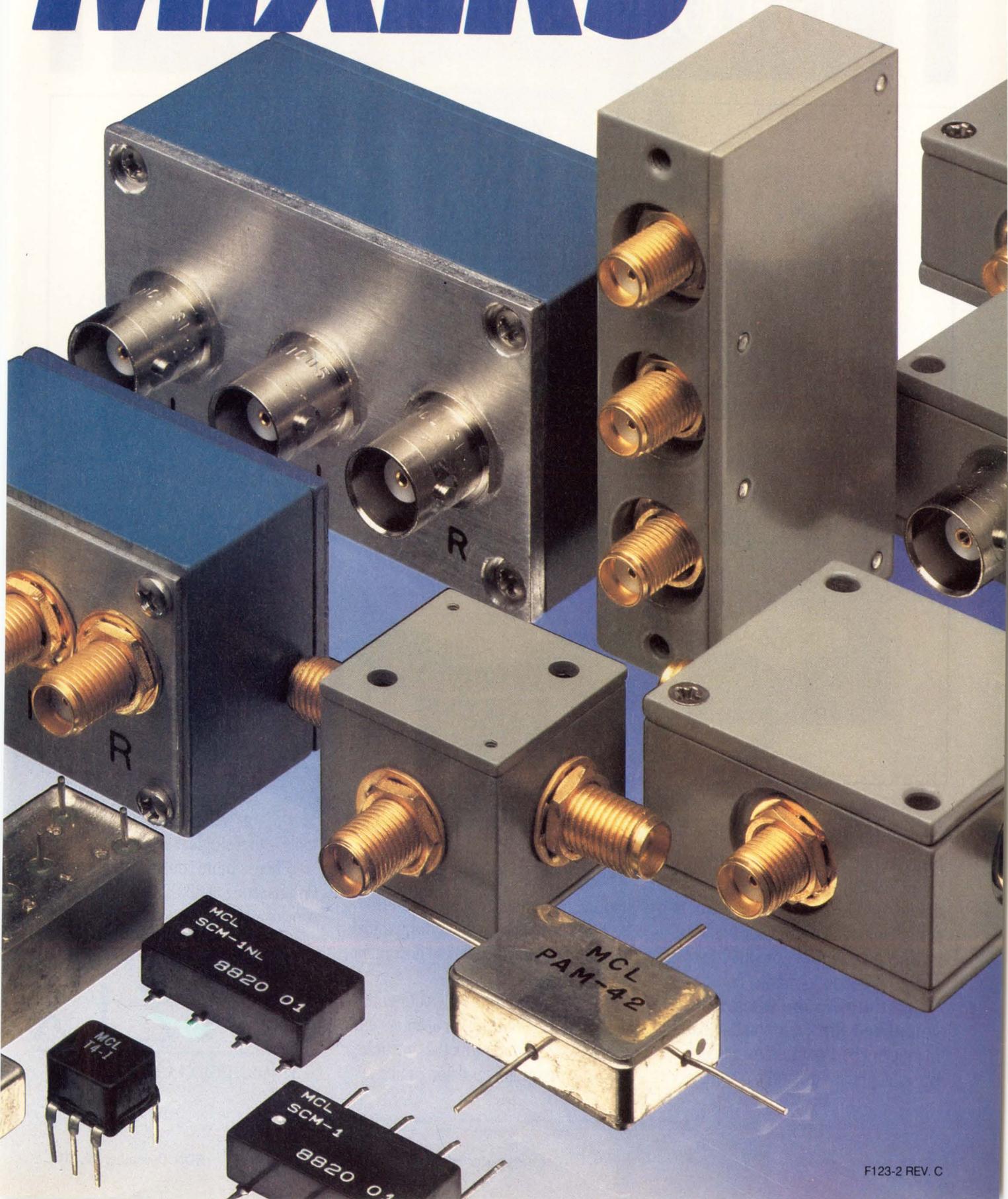
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Computer-Aided Engineering

VHDL Spreadsheet

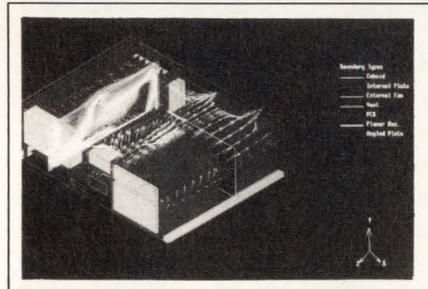
Hum uses a spreadsheet paradigm that maps a descriptive matrix into behavioral VHDL (VHSIC Hardware Description Language). Pop-up menus prompt you for the proper input needed to control object and state columns. The software creates data-conversion functions and assigns signals and variables. After developing your models, the software compiles your tabular design into an intermediate format, which you can compile into VHDL. SPARC or VAX X-Window version, \$12,000. An IBM PC version, which sacrifices the multiwindowing capability useful for displaying multiple tables and internally created waveform graphs, \$3500.

Lewis Systems Inc, 1915 Peters Rd, Suite 113, Irving, TX 75061. Phone (214) 438-2177.

Circle No. 410

Thermal-Analysis Program

Flowtherm is a thermal-analysis CAD program for studying 3-D airflow and heat-transfer in electronic systems. The program accepts data on your hardware design and considers the effects of air viscosity,

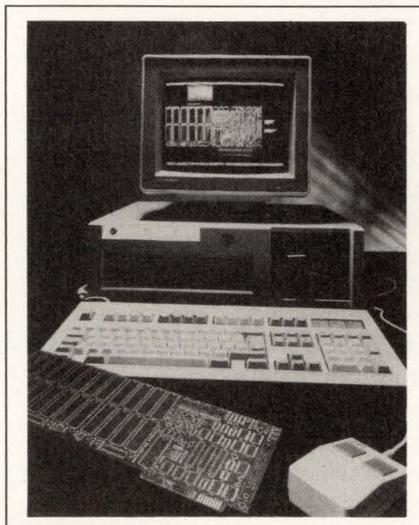


turbulence, and buoyancy force. The program outputs a picture of the hardware, showing fluid velocities and temperature profiles in all areas of your design. You can apply the program to only a section of pc board or to a complete rack of equipment. The program analyzes natural, forced, or mixed-convection designs and considers steady-state and transient effects. Ver-

sions for 386-PC and SPARC-2 workstation, £12,000 and £30,000, respectively. One month trial and two days of tuition, £1100.

Flowmerics Ltd, Kingsgate Business Centre, 12-50 Kingsgate Rd, Kingston-upon-Thames, Surrey KT2 5AA, UK. Phone (81) 547-3373. FAX (81) 547-2682.

Circle No. 411



PC-Board CAD Program

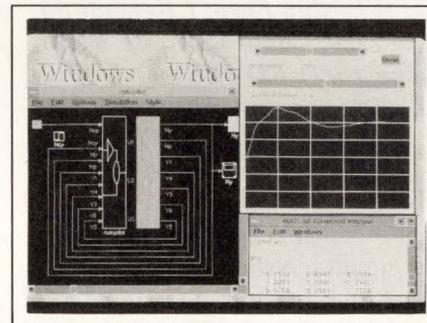
Boardmaker-2 is a pc-board CAD program for PCs that accepts netlist inputs, and outputs artwork data in HPLG, or DMPL penplotting language. The program handles through-hole and surface-mount components for as many as ten layers of circuit and silk screen. You can enter a netlist manually, or via a netlist translator, for Mentor, Protel, Racal-Redac, Schema, Tango, and Vutrax formats. The program includes a top-down modification facility for installing modifications to existing designs. Schematic changes automatically modify layout and netlist files and provide automatic time and date stamping. Component renumbering follows through to silk-screen mask, and an update file automatically back-annotates the schematic. A post-script driver lets you import layout files to text processing software, enabling you to generate artwork

master drawings on a laser printer or at a typesetting bureau. £295.

Tsien UK Ltd, Cambridge Research Laboratories, 181A Huntingdon Rd, Cambridge CB3 0DJ, UK. Phone (223) 277777. FAX (223) 277747. Circle No. 412

System Simulation Software

Simulab is a simulation and analysis tool for nonlinear dynamic systems. In addition to nonlinear systems, the software also simulates the behavior of linear, continuous, discrete-time, multirate, single-input-single-output, and multivariable input/multivariable output systems. The software models sets of linear and nonlinear differential or difference equations that you can provide as either block-diagram models or in equation form. The software assists in creating block diagrams, and it accepts C, Fortran, or the vendor's own format for the equations. Among the blocks included with the simulator are linear and nonlinear blocks, source and sink blocks, and connection blocks. The tool set allows hierarchical model-

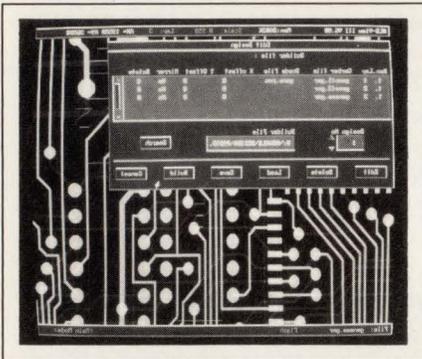


ing. Analysis tools allow you to solve differential equations, evaluate linear models and determine a system's equilibrium point. The software runs on Apple and IBM PCs and workstations from Apollo, HP, Sun, and DEC. Windows 3.0-based PC version, \$3995.

The Mathworks Inc, Cochituate Pl, 24 Prime Park Way, Natick, MA 01760. Phone (508) 653-1415. FAX (508) 653-2997.

Circle No. 413

Computer-Aided Engineering



PC-Board Software

ALS-View III Version 6 is a multi-layer pc-board software tool for viewing and editing pc-board layouts. The software, which runs on personal computers with 2 Mbytes of RAM, offers a Motif-like user interface. The software allows viewing and editing of as many as 128 layers; you can edit by window or layer. Resolution of the layers is to one mil. The software generates printer outputs for Postscript and Dot Matrix printers. You can use the software to generate drill files; it also merges multiple Gerber files on a single film. Software, \$795; Gerber design-rule-checker option, \$495.

ALS Design Corp, 1 Kendall Sq, Suite 2200, Cambridge, MA 02139. Phone (617) 621-7101. FAX (617) 577-1209. Circle No. 414

Fault Simulator

Unlike concurrent fault simulators that simultaneously simulate a good circuit and its evil twin, Adas Fault Simulator uses a differential algorithm that simulates a good circuit and a faulty circuit sequentially. The differential fault simulator only records and tracks the difference between the good and faulty circuits at latches and flip-flops. As a result, the simulator has lower memory requirements than concurrent fault simulators. The algorithm in the difference fault simulator includes dynamic fault grouping to simulate multiple faulted circuits simultaneously. Intelligent fault in-

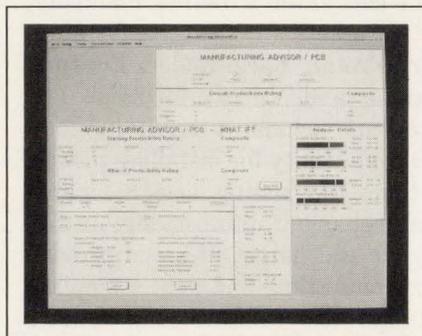
jection speeds runtimes and reduces the risk of eventless simulation. The software runs on SPARCstations. From \$25,000.

Adas Software Inc, 3333 Bowers Ave, Suite 295, Santa Clara, CA 95054. Phone (408) 988-3846. FAX (408) 988-2483. Circle No. 415

Simulation Comparison Program

VCAP is a simulation data comparison-and-analysis program. The software allows you to normalize data to adjust for differences in format, timing, and display modes. The normalization routines include state mapping, timing translation between print-on-change data and cycle data, and data separation on bidirectional pins. The software's analysis routines include reports on output-pin delays and transitions, input-pin timing, and a resource file that checks tester compatibility. You specify which data pins to compare, the allowable timing tolerance, times to mask the comparison, and four comparison algorithms. The software runs on Sun and HP/Apollo workstations. Single user, \$3995; server node configuration, \$7995.

Source III Inc, 3958 Cambridge Rd, Suite 247, Cameron Park, CA 95682. Phone (916) 676-9329. Circle No. 416

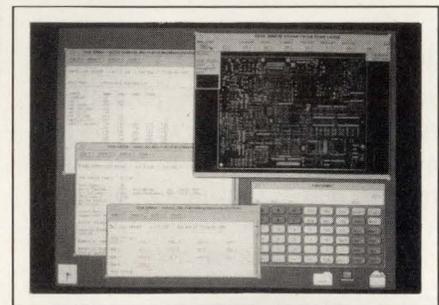


Manufacturability Tool

The Manufacturing Advisor/PCB tool provides information on product cost, quality, and delivery for the analysis of pc-board design al-

ternatives. Built upon the vendor's Falcon Framework, the software evaluates parts lists, board-area consumption, and other considerations that might impact product manufacture. The software monitors and identifies unusual labor requirements, special manufacturing processes, lack of standards compliance, and other issues that lead to high-risk assembly. The software includes a component library containing 800 package styles. Currently available on HP/Apollo workstations, the company plans to run it on Sun and HP Series 700 workstations early in 1992. Software, \$16,900 option to Idea Station and Board Station. Additional parts library, \$1500.

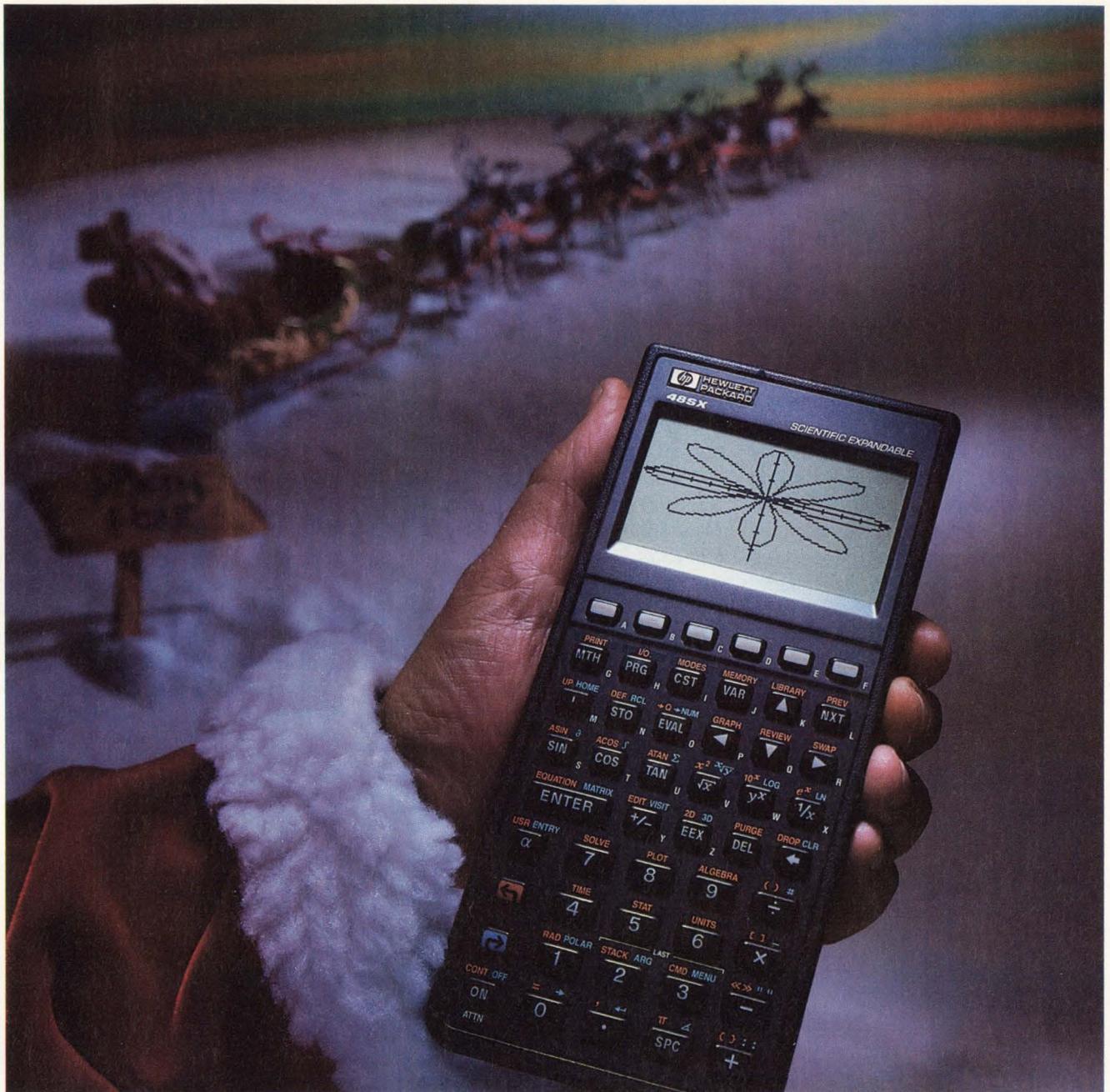
Mentor Graphics Corp, 8005 SW Boeckman Rd, Wilsonville, OR 97070. Phone (800) 547-3000; (503) 685-7000. Circle No. 417



PC-Board Software

PADS-2000/UX is a design tool for pc-board design. The software includes a push-and-shove autorouter. The design tool offers automatic component placement and rotation of pads and components in 1/10° increments. A 1-μm database provides high resolution and a capability of spacing traces and components closely. The software also features an automatic copper-fill facility. Available on SPARC-stations under OpenLook/X Window. \$19,995.

CAD Software Inc, 119 Russell St, Suite 6, Littleton, MA 01469. Phone (508) 486-9521. FAX (508) 486-8217. Circle No. 418



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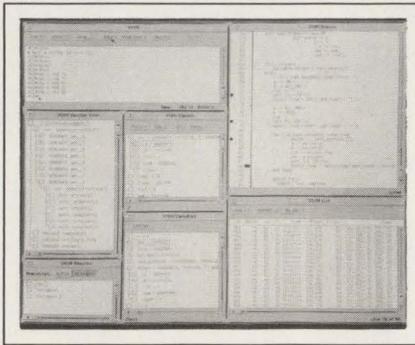


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Computer-Aided Engineering

VHDL Tools

The V-System/SPARC VHDL (VHSIC Hardware Description Language) development and simulation suite works on SPARCstations running Sun OS and Open Windows. The system, which handles designs of 100,000 lines of code, includes a VHDL compiler, an interactive VHDL simulator, and a source-level debugger. The system provides six windows that allow you to view and interrogate the design, display variables and signals, control the simulator, display processes, and list the simulation output. The debugger provides features such as breakpoints, reading and setting signal and variable values, and single-stepping through the source. The software supports the IEEE 1076 standard. The vendor claims initial compilation benchmark results of 15,000 lines per minute and simulation rates of 10,000 RTL statements



per second on a Sun IPC. Single-user license, which requires a 15% annual maintenance fee, \$4995.

Model Technology Inc, 15455 NW Greenbrier Pkwy, Suite 210, Beaverton, OR 97006. Phone (503) 690-6838. Circle No. 419

Spice Enhancement

The Profile front-end tool works with the Analog Workbench II Spice-based simulation tool. The front-end tool enables both graphi-

cal and textual entry of structural- and behavioral-level circuit descriptions. You can build circuit models from block diagrams that include such components as PLLs, differentiators, oscillators, and gain blocks. Although this software also accepts standard Spice netlists, it also permits behavioral-level models containing differential equations, Laplace transforms, and basic arithmetic. The software allows distributed processing of multiple tasks across a network; such tasks don't include simple dc and transient analysis but include statistical and parametric simulation. The software incorporates modeling extensions to Spice to enable such effects as hysteresis, memory, and conditional branching. The models also let you eliminate discontinuities in nonlinear models using piecewise-linear functions. An option to the company's \$12,000 Analog Workbench II simulation and analy-

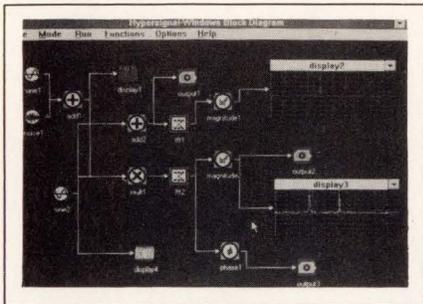
How well does Texas Instruments support



Computer-Aided Engineering

sis tools, Profile runs on Sun, DEC, and IBM workstations. \$15,000.

Valid, 2820 Orchard Pkwy, San Jose, CA 95134. Phone (408) 432-9400. Circle No. 420



DSP Simulation Software

Hypersignal-Windows Block Diagram software allows you to design and sequence process blocks for DSP applications. Among the functions included with the software are blocks for FFTs, FIR and IIR filters, linear predictive coding, IFFT

(inverse FFT), and difference equations. In addition to these blocks, you can create your own. Each block is of the input, output, process, or display type. After stringing each of the blocks together, you can apply a stimulus and simulate the response. You can measure the response using display blocks at your choice of probe points. The software runs on personal computers under Windows. From \$1995.

Hyperception Inc, 9550 Skillman, LB 125, Dallas, TX 75243. Phone (214) 343-8525. Circle No. 421

PC-Board Design Tool

Eagle is a modular PC-based circuit-board design tool that includes a schematics editor, an autorouter, and a layout editor. The tool databases are shared, thereby calling components into the layout editor as you use them in creating your

schematic. Alternatively, you can use a utility to convert netlists generated by several other schematic packages into the proper layout database. The software, which runs on PCs, uses expanded memory for large designs. An Electric Rules Checker evaluates the design for shorts, overlapping signals, and continuity. A Design Rules Checker compares trace spacing, wires not in a 45° raster, off-grid objects, and minimum and maximum sizes against user-defined criteria. The autorouter routes two signal layers and unlimited supply layers. Schematic editor, \$899; layout editor, \$399; autorouter, \$699; total system, \$1199.

American Small Business Computers Inc, 327 S Mill, Pryor, OK 74361. Phone (918) 825-4844. Circle No. 422

Cadsoft Computer GmbH, Rosenweg 42, W-8261 Pleiskirchen, Germany. Phone 8635-810. FAX 8635-920. Circle No. 423

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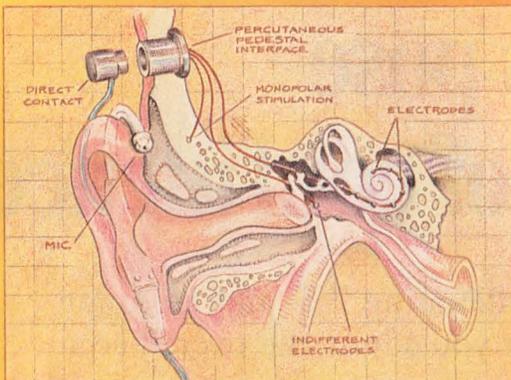


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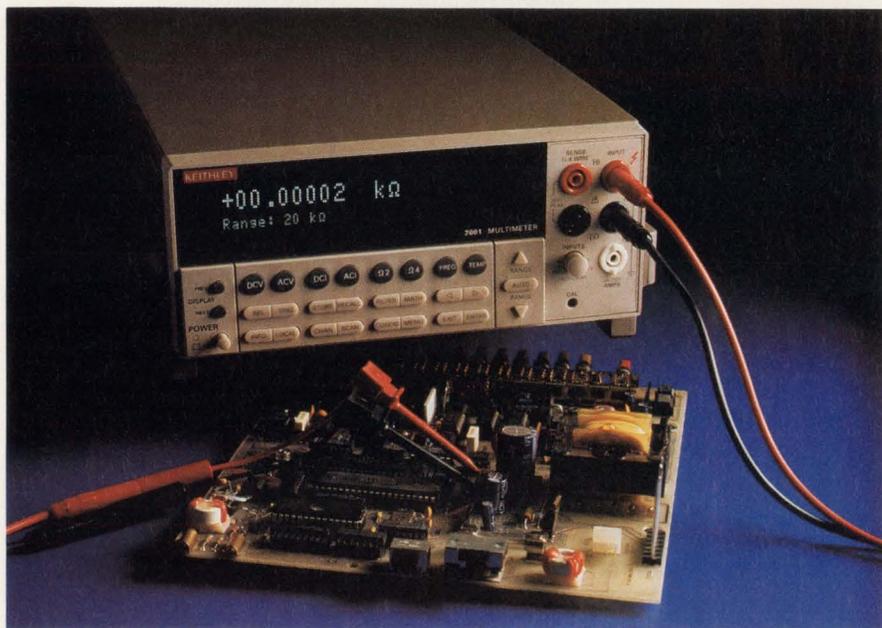
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Where quality starts with fundamentals

DMM calibration shortcuts pose question of confidence

Simpler methods of calibrating 7.5- and 8.5-digit digital multimeters let you adjust the overall accuracy of an instrument using as few as two external standards—or no standards at all. The methods are innovative but depart from principles the calibration community has cast in stone.

Brian Kerridge, Technical Editor



The requirement for only 2 and 20V dc and 20-k Ω and 1-M Ω standard sources to calibrate Keithley's model 2001 exemplifies the trend toward easier user calibration.

THE TREND TO SIMPLER methods of maintaining the accuracy of instruments stems from a natural desire to reduce the inconvenience and expense of calibration. Examples of easier ways to calibrate instruments appear on several high-end DMMs.

These instruments have many functions and ranges that require regular calibration, and traditionally the cost of ownership is high. Two new methods, "artifact" and "self calibration," imply you can enjoy substantial cuts in these support costs.

But take care. You might delight in the prospect of lower support costs and more convenience, but calibration diehards frown upon using these methods alone. They argue that traditional methods already represent a minimum procedure for achieving satisfactory calibration. Their argument maintains that the new methods break the all-important traceability chain and are incompatible with established company audit procedures and MIL-STD-45662A (Ref 1).

Artifact calibration is similar to the normal procedure for calibrating an instrument, during which you use external standards to check and adjust key points of a DMM's performance. The difference with artifact calibration is that the num-

ber of key points you need to check reduces from about 80 to just 2. Consequently, a calibration laboratory needs only two prime standards (the artifacts), instead of a full-compass calibrator, to perform a complete calibration. In practice, the artifacts needed are a 10V dc standard source and one or two resistance standards.

The other new method of calibrating, self calibration, requires no external equipment at all. DMMs with this facility use standard sources housed within the instrument. At any time you can initiate a self-calibration routine from the instrument's front panel, and a 10-minute cycle of internal adjustments resets the accuracy on all the unit's functions and ranges. Of course, the DMM's internal standards require calibrating at some time, otherwise there would be a complete loss of traceability. Vendors present self calibration primarily as a means of enhancing a DMM's accuracy and not as a replacement for conventional calibration—an acknowledgment that this method has traceability deficiencies.

Convenience vs confidence

It's easy to see why both artifact and self calibration offend calibration diehards. The trend among DMM vendors is to reduce most of the cross referencing carried out between external standards and instruments during calibration. DMMs, particularly high-end models, generally find application in critical measurement situations. For example, high-end DMMs are often deployed in ATE systems to provide traceable accuracy for the whole system. Elsewhere, you will find high-end DMMs heading up a company's in-house system for auditing the accuracy of many other instruments in the plant. In applications such as these, it's natural to imagine the need for more, rather

than fewer, checks in a calibration procedure.

There is no doubt that the easier methods of adjusting accuracy work effectively and are convenient. There's also no doubt that reconciling these methods with traditional procedures is awkward. The most obvious weakness of the new methods is that they leave you with very



little indication that the instrument has in fact been adjusted. It's this lack of hard records that causes doubts over the traceability of the techniques. If you follow the shortcut methods with a full calibration check, then traceability worries disappear. But you'll need a full set of calibration sources for that check, which devalues the convenience of the new techniques.

In the short term, it's unlikely that calibration methods such as artifact and self calibration will ease your calibration costs. In the long term, as the virtue of using the techniques alone becomes evident, you may find it acceptable to extend the regular interval for a full calibration. In the end, your confidence will be the deciding factor.

Laurie Cronin, principal officer

A self-calibrating DMM requires no external standards and offers the easiest way to improve instrument accuracy. For Datron's model 1281, self calibration provides approximately a 2:1 improvement in both overall long-term accuracy and the effective temperature coefficient over the 13 to 33°C ambient range.

and specialist in dc and low-frequency metrology with the National Physical Laboratory at Teddington, UK, offers advice to reconcile opposing views of artifact and self calibration. He says if you calibrate an instrument using any new technique, you should still check the instrument's performance on all its functions and ranges via a full conventional calibration. You should adopt this procedure each time you calibrate the instrument over the first few calibration intervals. As you build up confidence in artifact and self calibration, you can consider extending the interval between full calibrations.

As an example, you could choose to carry out artifact calibration every 12 months and conduct a full calibration at 24-month intervals.

Simpler methods for adjusting the accuracy of DMMs offer the possibility of extending the period between full calibrations.

Cronin emphasizes that extending the calibration interval is not a recommendation and should be done only when there is evidence to support the change. In his experience, users that have artifact- or self-calibration DMMs have all chosen to check performance fully each time they calibrate the instrument. Cronin suggests that as an overall policy you should treat each instrument on its merits, irrespective of the technique used for adjusting its accuracy.

Table 1 shows which calibration methods today's 7.5- and 8.5-digit DMMs employ. Artifact calibration appears only on Hewlett-Packard's 3458A and Keithley's 2001. HP's model 3458A needs two standard sources—10V dc and 10 k Ω . For Keithley's model 2001, you need 2 and 20V dc sources and 20-k Ω and 1-M Ω resistance standards. For both instruments you also need a low-thermal shorting link.

The 3458A also includes a means of self calibration, which the company calls auto calibration, or Acal. Self calibration, or Selfcal, is also a feature of Datron's model 1271 and 1281 DMMs. Datron's models also provide a means of conventional calibration against a full set of external standards for those who are not believers in calibration short-

Common DMM and calibration terms

Absolute accuracy—an accuracy figure that includes all sources of measurement uncertainty. Some standards laboratories calculate this figure as the arithmetic sum of all uncertainty elements. Other laboratories calculate it as the square root of the sum of the squares of the uncertainty contributions to a declared confidence level.

Accuracy relative to calibration standards—an accuracy figure that includes only the uncertainty elements contained within an instrument and excludes the uncertainty of the calibration source.

Artifact calibration—a calibration method that uses a minimum number of standard calibration sources. The sources for a DMM typically include a 10V dc standard and a standard resistance.

Calibration—comparing an instrument of unknown accuracy to a standard of known accuracy, the purpose being to record or adjust the difference.

Calibration interval—the period of time over which an instrument maintains its specification without adjustment or verification. Typical calibration intervals for DMMs are 90 days and 12 months.

Calibration uncertainty—the arithmetic or statistical total of all uncertainty contributions for a calibration standard.

Full scale—the maximum number of counts on a scale; for example, 19,999,999.

Full range—the number of counts at the cardinal point on a scale; for example, 10,000,000.

Linearity error—the maximum deviation from a straight line between zero and full scale.

Low-thermal short—a link used as a zero reference for short circuiting an instrument's input terminals and producing a minimal thermal EMF.

National standard—a standard maintained at a National Standards Laboratory, such as the National Institute of Standards and Technology in Washington, DC.

Reference standard—the best, or prime, standard of a hierarchy of standards in a calibration laboratory.

Traceability—an unbroken chain of calibration records going back to a national standard.

Transfer standard—a standard having no absolute accuracy but having sufficient stability and resolution to allow comparison of two similar devices.

Working standard—a standard used for general calibration. Working standards are regularly compared to a reference standard.

Acknowledgment

Thanks go to Peter Crisp, head of standards at Datron Instruments, for helping with this glossary.

Table 1—Representative 7.5 and 8.5-digit digital multimeters

Manufacturer	Model	Digits	Calibration method			Price
			Conventional	Artifact	Self	
Datron Instruments	1281	8.5	✓		✓	\$10,560
	1271	8.5	✓		✓	\$5880
John Fluke Manufacturing Co Inc	8505A	7.5	✓			\$4250
	8506A	7.5	✓			\$8450
Hewlett-Packard Co	HP 3458A	8.5		✓	✓	\$6700
Keithley Instruments	2001	7.5		✓		\$2695
Philips Test and Measurement	2530	7.5	✓			DM8200
Prema Präzisionselektronik	6047	7.5	✓			DM9980
	6048	8.5	✓			DM13,750
	8047 AT	7.5	✓			DM17,560
Schlumberger Technologies	7081	8.5	✓			\$9337
	7071	7.5	✓			\$7825

cuts. To add confusion, though, Datron uses the term auto calibration, or Autocal, to describe the company's conventional method of calibrating the DMMs.

All other high-end-DMM vendors stick rigidly to tradition with their models and provide only a conventional way of calibrating.

Eighty points need adjustment

Table 2 summarizes the merits of the three calibration methods you will find on high-end DMMs. Note that for the majority of DMMs, including even some 4.5-digit hand-held units, accuracy control relies solely on correction parameters stored digitally in nonvolatile RAM inside the DMM. It's partly the function of calibration to adjust these parameters to make the instrument produce accurate readings.

Normally, there is a correction parameter for every function and range combination on a DMM. Some ranges require more than one parameter. For example, the dc function has parameters for zero and both polarities of input, and the ac function has parameters for the low- and high-frequency ends of the band. In total, there could be 80 correction parameters.

In a conventional calibration procedure, you connect 80 inputs in turn to the DMM. At each setting, you initiate a trigger to update a corresponding parameter in the DMM's calibration memory. This method clearly provides a high degree of confidence that you've calibrated most aspects of the DMM's performance. The drawback is the extensive range of standard sources required to effect the calibration—a single-instrument calibrator to do this job costs approximately \$35,000.

Although most DMMs provide a front-panel key to initiate the trigger, usually vendors and calibration laboratories calibrate DMMs remotely using an IEEE-488 system

controller and a programmable calibrator. Even so, such an automatic routine could take two hours to calibrate a high-end DMM fully.

Although artifact calibration requires only two or three external standards, the 80 or so accuracy-correction parameters in the instrument still need updating during the process. Clearly, something smart needs to happen inside the instrument to translate two dc and resistance inputs to signals capable of adjusting the overall accuracy of the unit. The overall accuracy adjustment points appear not only on all the dc and resistance ranges of the unit but also on all current and ac voltage ranges.

On Keithley's 2001 DMM, you use 2 and 20V dc sources and 20-k Ω and 1-M Ω resistances to calibrate ranges for those inputs directly. To calibrate other dc and resistance ranges, the DMM internally switches its internal gain-defining components to scale up or down from the same standard inputs. When you calibrate the resistance function, you in fact calibrate the currents the unit sources when operating in its normal mode as a resistance meter. The DMM uses these same currents to calibrate its operating current-function ranges.

For ac ranges, the 2001 DMM uses the dc source to calibrate the low-frequency end of the band while

Table 2—Comparison of DMM calibration methods

Characteristics	Calibration method		
	Conventional	Artifact	Self
Traceability	Full	Partial ¹	None
Calibration equipment	Full-function calibrator	10V dc and resistance standards	None
Calibration cost	\$400 to \$1000 ²	\$350	\$0
Calibration interval	12 months ³	12 months ³	1 or 30 days, depending on model ⁴

- Notes: 1. Full traceability if you check all functions and ranges after artifact calibration.
 2. Depends if you require calibration to MIL-STD-45662A.
 3. Depends on your company's in-house procedures, but 12 months is typical.
 4. Self calibration must be carried within calibration interval to guarantee specification.

in a dc-coupled mode. For the high-frequency end, the DMM requires no source at all. The DMM's internal reference voltage generates a step input to each ac range in turn. On each range the DMM stores two samples of the transient response of the input circuits. The magnitude of the samples, in turn, determines the setting of a flatness-compensation amplifier in the ac-measurement signal path.

But there are factors that influence accuracy that artifact calibration doesn't compensate for. These factors include linearity of the main ADC, ac/dc difference in the ac-detection circuit, and self heating on high-voltage and high-current inputs. John Banaska, 2001 project manager at Keithley, explains that you can look at these factors as characterization factors for an individual DMM. He says characterization factors are stable over the life of the product and any change has minimal effect on overall accuracy.

Keithley cancels the effects of these characterization factors at the manufacture stage using an in-house calibration routine. This once-in-a-lifetime routine should need repeating only if the instrument receives a major repair. Banaska says routine user calibration compensates for drifts in the DMM's reference and gain-defining components and that these drifts are the predominant reasons for accuracy drift in a DMM.

In answer to the suggestion that artifact calibration is weak on traceability, Banaska explains that you can output all the accuracy parameters stored in the 2001 DMM. These figures provide a basis for maintaining full records of the stability of the instrument.

A tradeoff of artifact calibration is your loss of flexibility to adjust one area of the instrument's performance or to improve on the pub-

Artifact calibration lets you adjust the accuracy of a digital multimeter using one voltage and one resistance standard.

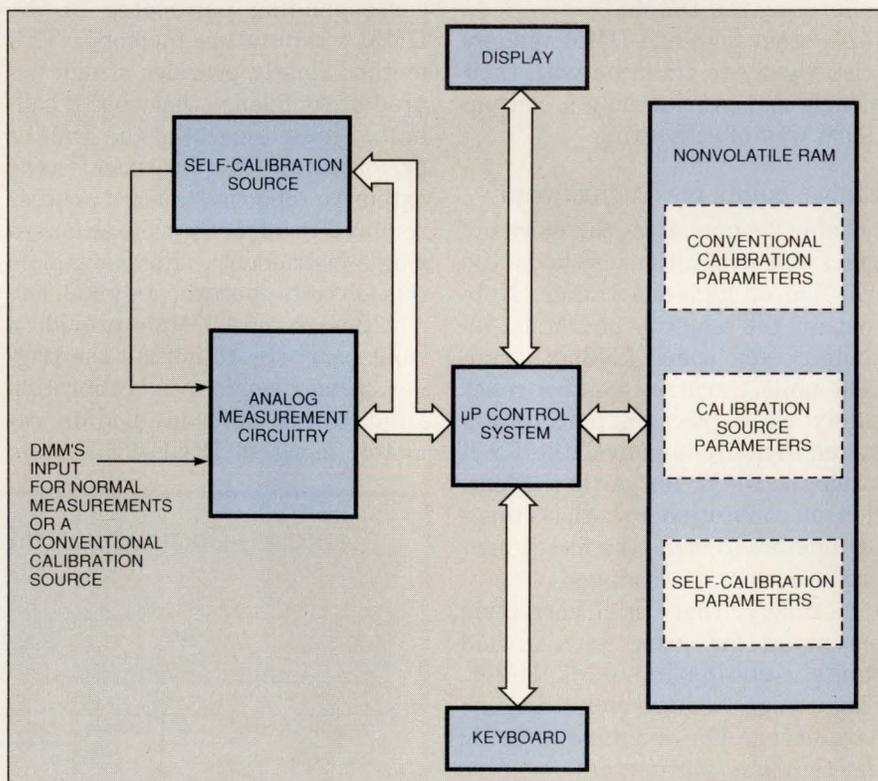
lished specifications of the product. Conventional calibration lets you optimize one specific range and always make the instrument read nominal value. Artifact calibration gives you no way to do this fine tuning. When the artifact-calibration routine is over, all readings will be within published limits, but not necessarily reset to the center point of the accuracy spread.

Datron's 1271 and 1281 DMMs

embody a limited set of calibration sources to let you improve the accuracy of the unit without any external standards. These models also let you perform a conventional external calibration; during that process, the calibration of the internal sources takes place transparently.

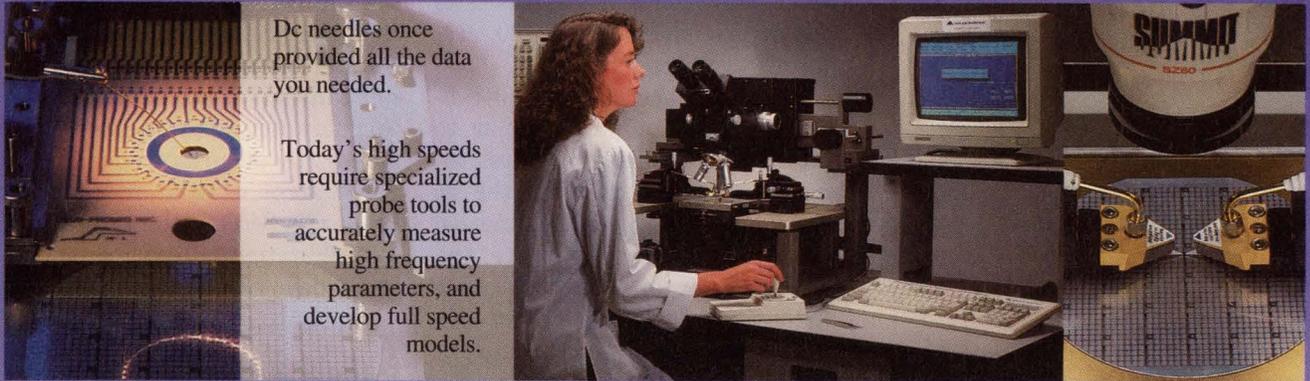
Fig 1 shows the salient features of the arrangement. In Datron's instruments, three separate blocks of nonvolatile RAM store different sets of accuracy parameters. The first block sets the accuracy of the DMM following a conventional external calibration. The second block stores parameters relating to the internal calibration sources. The third block sets the DMM's accuracy each time you conduct an internal calibration.

The internal dc voltage sources



Datron's self-calibrating DMMs hold accuracy-correction parameters in three blocks of nonvolatile RAM. The first block sets the accuracy of the DMM following a conventional external calibration. The second block contains parameters relative to the accuracy of internal calibration sources. The third block sets the DMM's accuracy following an internal calibration. In normal operation, the DMM can measure inputs using parameters in blocks one or three.

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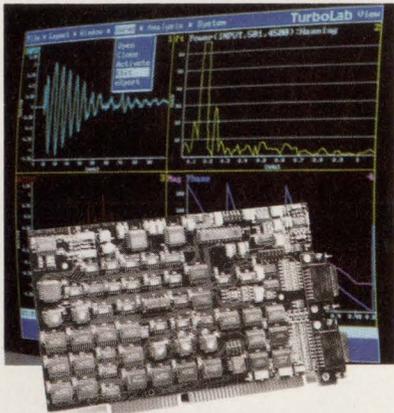
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are ± 100 mV, ± 1 V, and ± 10 V. The two resistance sources are 1 and 100 k Ω . A critical feature of the dc sources is their use of a transformer multiplier's fixed turns ratio to determine the 10:1 and 100:1 ratio of the voltages.

The internal process of self calibration follows a path similar to that of artifact calibration. First, internal dc sources calibrate the dc and ac functions; next, the internal resistance sources calibrate the drive current on the resistance function; and last, these drive currents calibrate the DMM's current function.

The real benefit of self calibration is the cancellation of drift effects in gain-defining components of the DMM's measurement circuits. These drifts occur when you operate the DMM at varying ambient temperatures or as the values of the components change with time. Self calibration does not cancel the effect of drift in the DMM's main internal reference.

Not all models make use of self calibration in the same way. On Datron's 1281 model, you use self calibration as a means of enhancing the specified accuracy when you decide you need enhanced accuracy. On other models, you must operate self calibration at regular intervals to guarantee that the instrument meets its accuracy specification. For Datron's 1271 and Hewlett-Packard's 3458A, these mandatory self-calibration intervals are 30 days and 1 day, respectively. **EDN**

Reference

1. Department of Defense MIL-STD-45662A, Calibration Systems Requirements, 1988.

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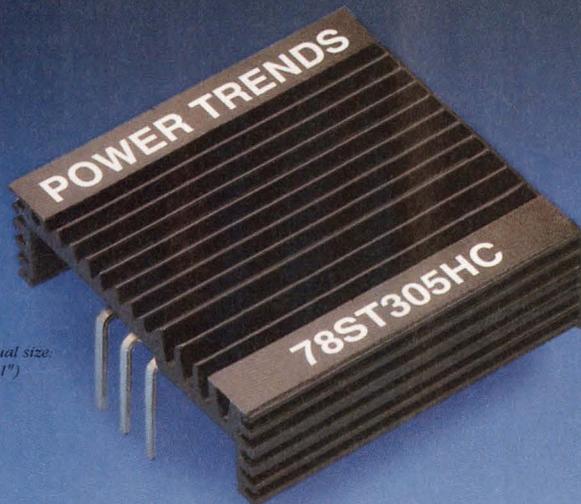
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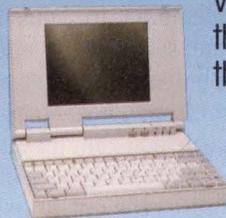
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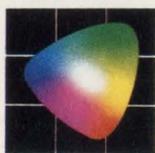


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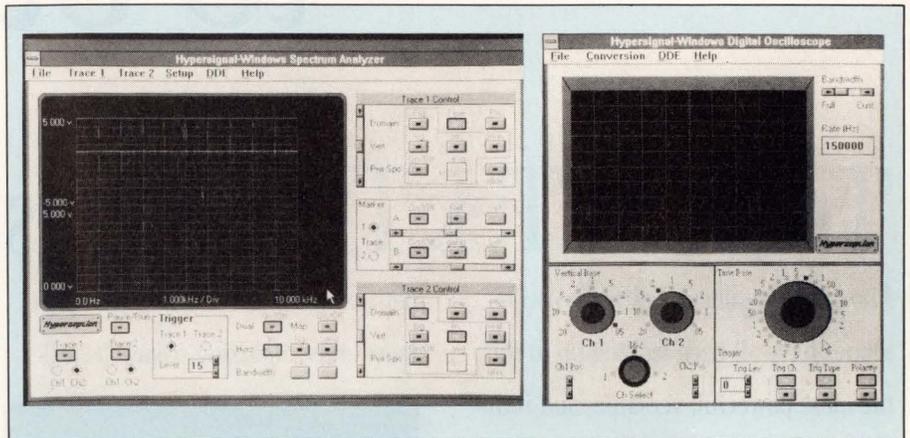
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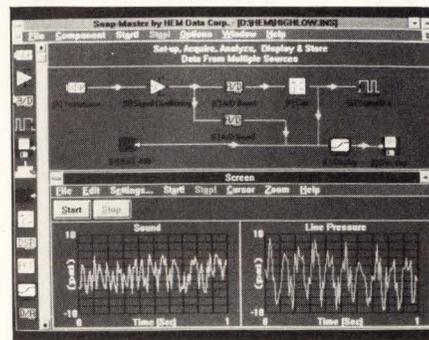
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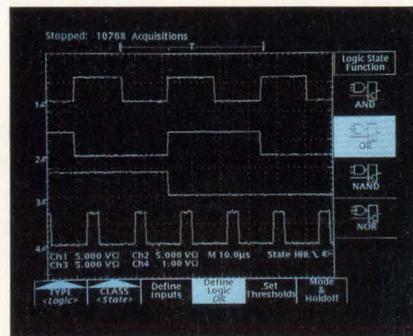
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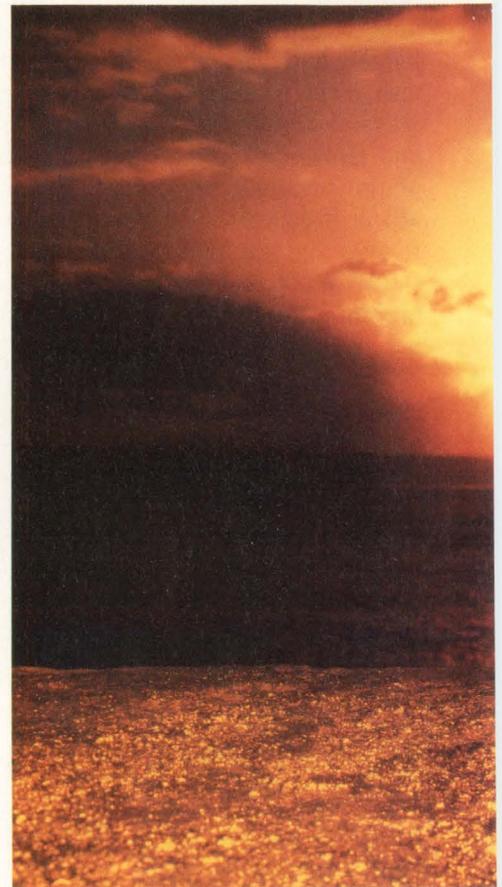
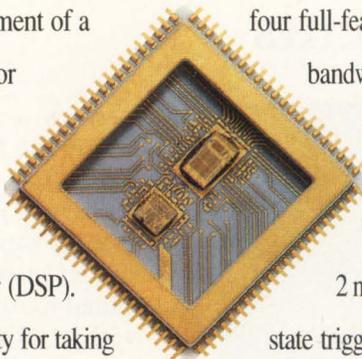
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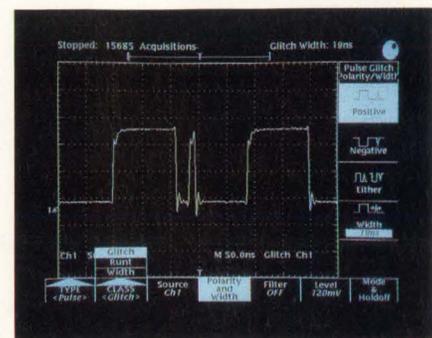
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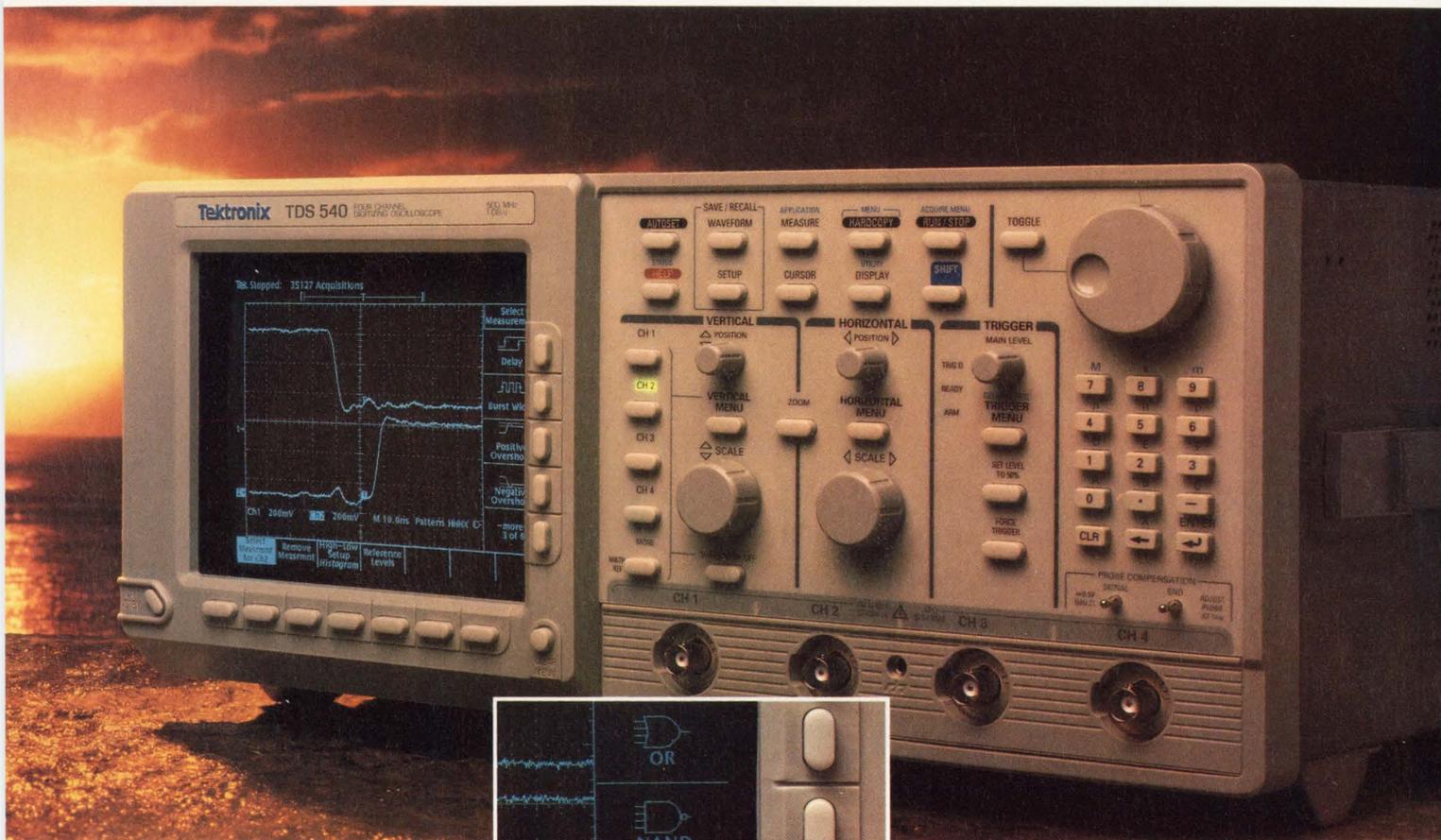
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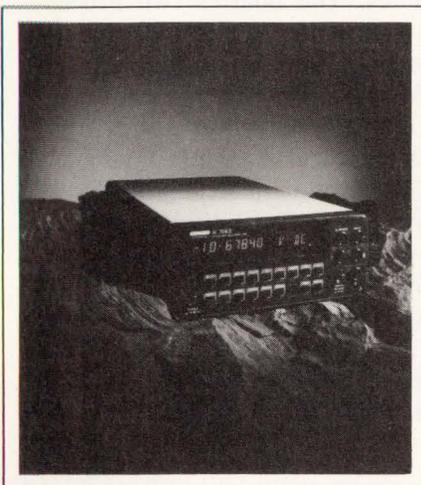
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KEITHLEY INSTRUMENTS

Instruments



6.5-Digit Digital Multimeter

The SI 7063 is a 6.5-digit DMM for measuring dc and ac voltage in the range 100 nV to 1050V, and dc and ac current in the range 1 nA to 2A. The meter also measures resistance from 100 $\mu\Omega$ to 999 M Ω ; it measures temperature using a platinum-resistance thermometer, or J, K, R, T type thermocouple sensors. The meter has counter and timer functions to let you measure 1 Hz to 1 MHz, and 1 μ sec to 1 sec for analog signals; and measure to 20 MHz and to 100 nsec for TTL signals. IEEE-488 interface programming includes an on-line help facility to provide correct syntax commands. £1810.

Schlumberger Technologies, ATE Systems Div, Victoria Rd, Farnborough GU14 7PW, UK. Phone (252) 544433. FAX (252) 543854. Circle No. 370

Handheld Oscilloscopes

The models 93, 95, and 97 Scopemeters combine a 50-MHz, 25-Msample/sec, dual-channel storage oscilloscope and an autoranging digital multimeter. The model 97 also includes a signal generator and component tester. The units have an RS-232C interface for calibration. The scopes capture glitches as narrow as 40 nsec and can store eight waveforms and 10 front-panel setups. Metering capabilities in-

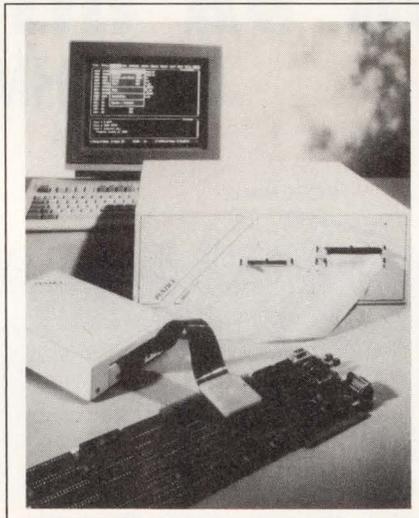
clude simultaneous display of minimum and maximum readings, relative and percent-relative, readings, and dB readings. The units have soft keys and weigh 4 lbs. Batteries power the units. Model 93, \$1195; model 95, \$1495; model 97, \$1795.

John Fluke Mfg Co Inc, Box 9090, Everett, WA 98206. Phone (206) 347-6100. FAX (201) 356-6100. TLX 185102. Circle No. 371

68302 μ P Emulator

The Mime-700 in-circuit emulator works with the 68302 microcontroller (μ C). You can connect the emulator to the Integrated Services Digital Network as a terminal controller, multiplexer, or concentrator. The 68302 personality module (pod), tracks the μ C's pipelined execution to halt when the emulated μ C actually executes an instruction, not when the μ C first fetches the instruction.

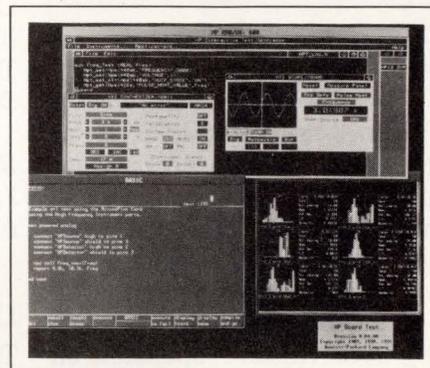
The emulator has 256 kbytes (2 Mbytes max) of emulator memory that you can allocate in 512-byte blocks. The emulator's trace and



trap circuitry features 64k discrete breakpoints as well as 64k breakpoints for 512-byte blocks of memory. The circuitry also has four 80-bit word recognizers, each with its own pass counter. The unit has an 8-ksample \times 128-bit trace memory, as well as a digital-waveform gen-

erator, a frequency meter, and a digital voltmeter. Emulator with 68302 pod, \$14,159.

Pentica Systems Inc, 1 Kendall Square, Bldg 200, Cambridge, MA 02139. Phone (617) 577-1101. FAX (617) 494-9262. Circle No. 372



VXI Chassis

The HP 307X VXI board tester combines a VXIbus chassis with the manufacturer's existing board tester. You can mount the VXIbus chassis externally or on the tester's test-head. The VXIbus chassis provides connections to VXIbus and IEEE-488 instruments. The chassis accepts C-sized VXIbus cards. \$221,500.

Hewlett-Packard Co, 19310 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 752-0900.

Circle No. 373

Low-Noise Synthesizer

The PTS 310 broadband signal source covers 0.1 to 310 MHz with a 1-Hz resolution (0.1 Hz optional). Spurious suppression specifies 60 or 65 dB. The instrument offers switching times of 20 μ sec or 1 μ sec to 20 μ sec, depending on band selected. Frequency switching is phase continuous. You have a choice of BCD or IEEE-488 interfaces. PTS 310, approximately \$6000. Delivery, six weeks ARO.

Programmed Test Sources Inc, Box 517, Littleton, MA 01460. Phone (508) 486-3008. FAX (508) 486-4495. Circle No. 374

Instruments



Logic Analyzers

The TA4000 series of logic analyzers includes models with 32, 48, or 80 channels. Asynchronous sampling is at 100 MHz max across all channels or at 400 MHz max across 8 or 16 channels. Memory depth at 100- and 400-MHz sampling is 2k and 8k words, respectively. Its 5-nsec glitch capture operates on eight channels without loss of memory depth.

Synchronous sampling is at 50 MHz max across all channels and

includes an 8-level branching-trigger facility that steps as much as 20 nsec. Optional disassemblers cover a range of 8-, 16-, and 32-bit μ Ps. In addition to internal non-volatile memory, you can store 512 kbytes of data on a front-panel plug-in memory card. Included as standard are interfaces for IEEE-488, Centronics, RS-232C, and composite video. TA4000-32, £2495; TA4000-48, £2995; TA4000-80, £3995.

Thurlby-Thandar Ltd, Glebe Rd, Huntingdon, Cambs PE18 7DX, UK. Phone (480) 412451. FAX (480) 450409. Circle No. 375

DSP Board

The MacDSP MB/A digital-signal-processing pc board for Macintosh computers runs at 30 Mflops. The board includes a DSP32C DSP μ P, a 68000 μ P, and data-acquisition

modules. The board's two processors run under Apple's A/Rose out of onboard memory. The onboard RAM maps directly into the Mac's Nubus memory space. Board, \$3495; expanded-memory version, \$4995; data-acquisition daughter boards, \$595; C compiler, \$1500; array-processor library, \$495; signal-analysis package, \$495.

Spectral Innovations Inc, 4633 Old Ironsides Dr, Suite 401, Santa Clara, CA 95054. Phone (408) 727-1314. FAX (408) 727-1423.

Circle No. 376

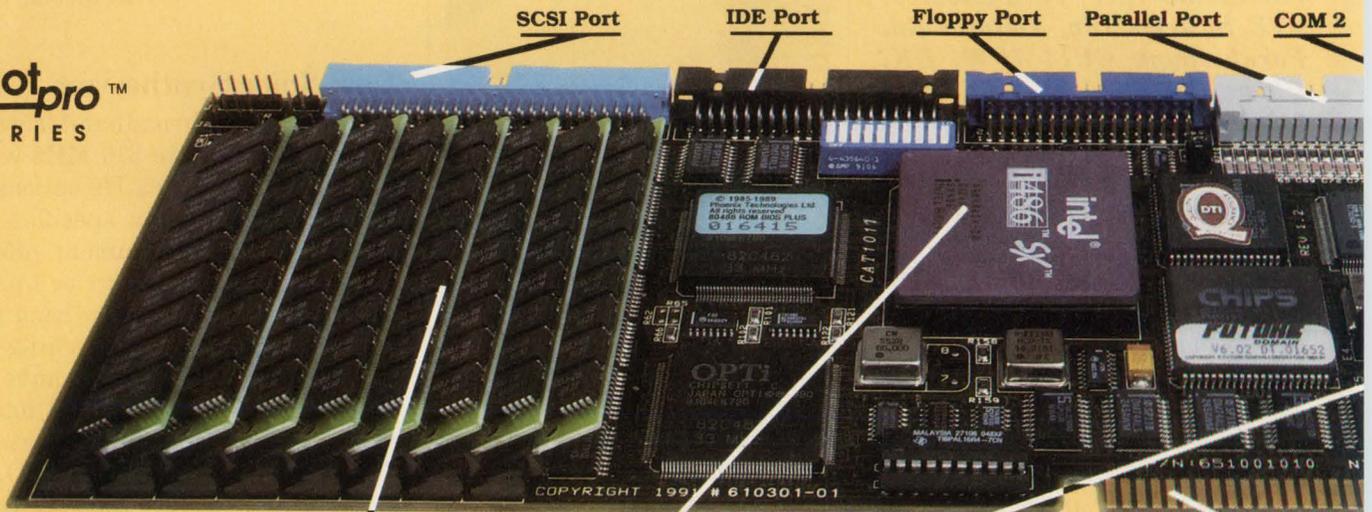
Gang Programmer

The Multitrk-4000 gang programmer programs as many as 32 devices at once using four 8-device plug-ins. It can also impress sequential serial numbers on as many as 32 devices simultaneously. Plug-ins are available for DIPs, plastic

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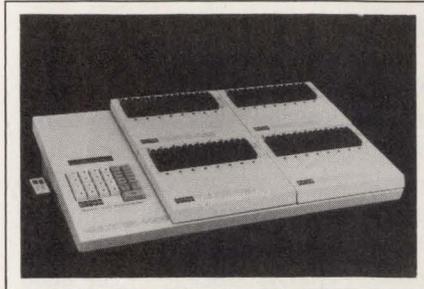
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Instruments

leaded chip carriers, and pin-grid arrays. You can program copies of a single ROM or sets of ROMs for 8-, 16-, and 32-bit-wide designs. The unit handles certain microcontrollers and CMOS PLDs. Other features include a keypad, an LCD, RS-232C and parallel interfaces, and a 3½-in. disk drive. The on-



board memory has 256 kbytes, expandable to 16 Mbytes. \$4995. Delivery, four to six weeks ARO.

Bytek, 543 NW 77th St, Boca Raton, FL 33487. Phone (407) 994-3520. Circle No. 377

Wooden And Nylon Probers

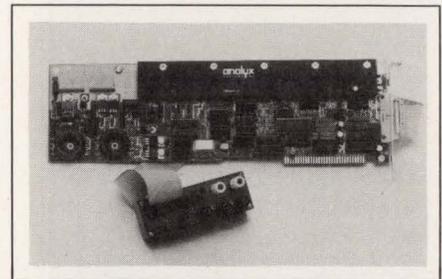
This line of wood and nylon probers is safe for use around ESD-sensitive components. The hygroscopic properties of these probing tools mean that they will readily take up and retain static-dissipating moisture from the atmosphere or skin. The probers will not mar or nick component leads. The birchwood spudgers will not melt when holding wires near soldering irons. \$0.22 to \$1.56.

Desco Industries Inc, 761 Penarth Ave, Walnut, CA 91789. Phone (714) 598-2753.

Circle No. 378

PC-Programmable Power Supply

The model ATEPS-1606 triple-output, programmable power supply plugs into a PC's backplane. It features a single 0 to 6V, 0 to 2A output, and two independent bipolar

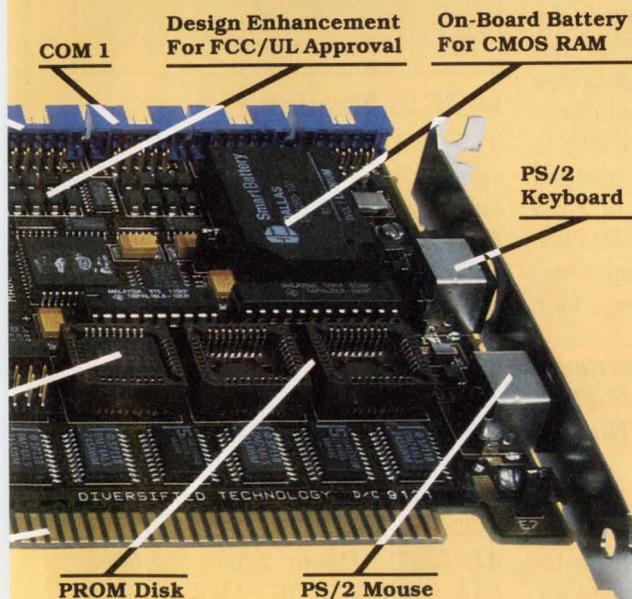


lar outputs. The bipolar outputs range from -15.75V to +15.75V at 0 to 200 mA each. Outputs of 0 to 28V and 0 to 125 mA are alternately available. You can vary all outputs in real time and monitor the supply's outputs via an onboard 12-bit A/D converter. You control and monitor the outputs using onboard control registers. The board comes with software. Model ATEPS-16, \$995.

Analyx Systems Inc, Box 14644, Fremont, CA 94539. Phone (415) 656-8017. FAX (415) 657-0927.

Circle No. 379

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	1011 Integrated	1001 CPU Only	1010 Integrated	1000 CPU Only
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25 or 33MHz - Shipping Now			✓	✓
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8K Internal CACHE	✓	✓	✓	✓
Internal Math Coprocessor			✓	✓
Noise Reduction Circuitry For FCC Class B	✓	✓	✓	✓
PS/2 Mouse Support	✓	✓	✓	✓
/AT-PS/2 Keyboard Support	✓	✓	✓	✓
On-Board Battery Real-Time Clock	✓	✓	✓	✓
Parallel Printer Port	✓	✓	✓	
2 Serial Ports	✓	✓	✓	
Future Domain SCSI	✓		✓	
IDE Interface	✓		✓	
Floppy Interface	✓		✓	
Up to 512Kb User PROM Disk	✓		✓	
Double-Sided Surface Mount Technology	✓	✓	✓	✓
Manufactured In-House (USA)	✓	✓	✓	✓
Landmark V1.14 Speed at 20MHz	90.1	90.1		
Landmark V1.14 Speed at 25MHz			114.1	114.1
Landmark V1.14 Speed at 33MHz			150.7	150.7

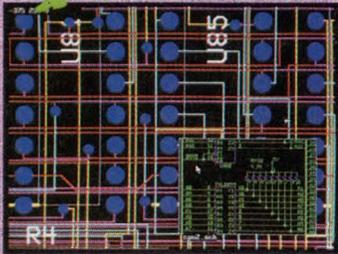
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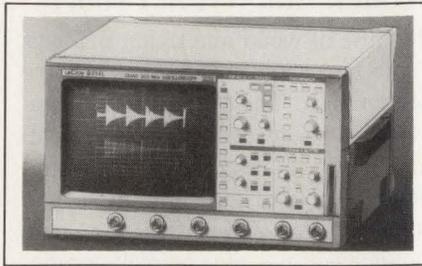
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Instruments



300-MHz Digital Oscilloscopes

The 2-channel model 9310L and the 4-channel model 9314L digital oscilloscopes have 300-MHz analog bandwidth, independent 100-Msample/sec digitizers on all inputs, and 1-Msample/channel memories. You can segment the sample memories for storing multiple events. Trigger events include pass/fail testing, glitches, and windows. The scopes perform signal-processing functions including FFTs. The scopes use credit-card-sized memories for off-line storage. Model 9310L, \$9900; model 9314L, \$14,900. Delivery, six weeks ARO.

LeCroy Corp, 700 Chestnut Ridge Rd, Chestnut Ridge, NY 10977. Phone (800) 553-2769; (914) 425-2000. Circle No. 380

3-GHz Oscilloscope Plug-ins

The model 11A81 3-GHz plug-in for the company's models 11403A and CSA 404 digitizing scopes has a rise time of ≤ 130 psec. The plug-in's external-trigger input's bandwidth is 2 GHz. Input sensitivity ranges from 10 mV/div to 1V/div in 1-2-5 sequence. Offset range is ± 50 divisions. The unit is programmable. Model 11A81, \$5495. Delivery, four to six weeks ARO.

Tektronix, Box 19638, Portland, OR 97219. Phone (800) 426-2200; (503) 627-7111. Circle No. 381

VXIbus Test System

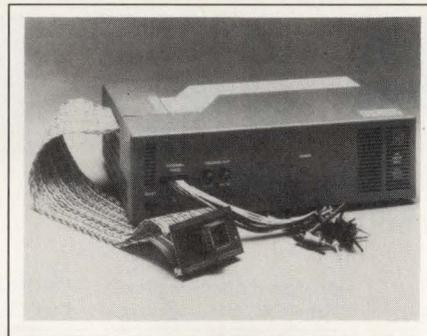
Modular test system 3538 has a C-size, 13-slot cardframe, controller and slot-0 modules, a signal proces-

sor, a configurable switch, a memory module, and a development card. Software support includes an object-oriented operating system, Pascal, system-device drivers, and generic device-driver development software. Three versions of controller and slot 0 modules offer interfacing via IEEE-488, Ethernet, or both.

The multitasking DSP module handles signal-analysis and waveform-generation tasks with 32-bit floating-point accuracy. The switch module lets you connect 12 6-MHz signals in a variety of multiplex or matrix configurations. The memory module expands storage of the 3538 system from a 4-Mbyte, 70-nsec memory to 128 Mbytes. Test system, from \$23,150.

Brüel & Kjaer, DK-2850, Naerum, Denmark. Phone 4280-0500. FAX 4280-1405.

Circle No. 382



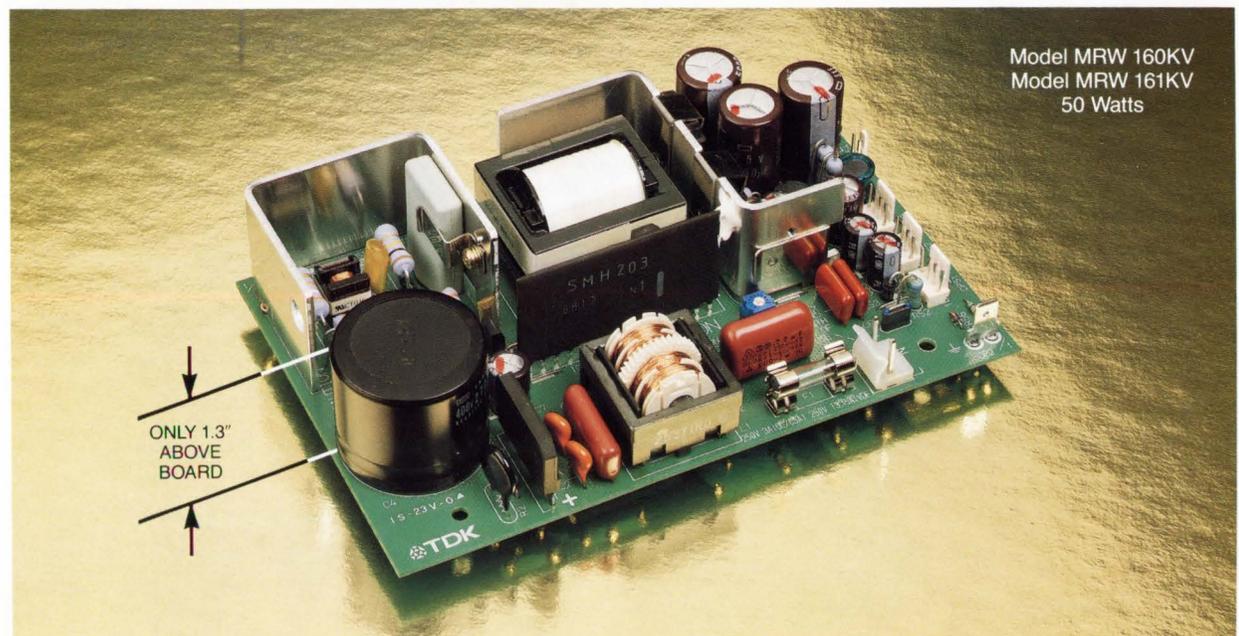
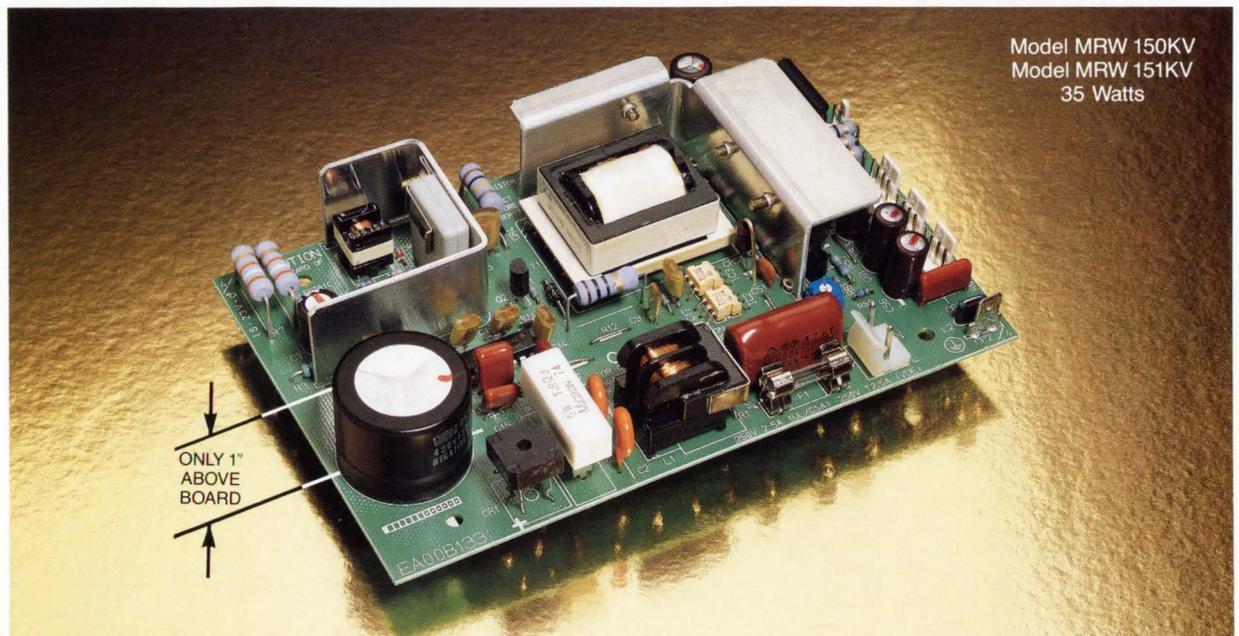
68HC16 Emulator

The HMI-200 in-circuit emulator supports the 68HC16 DSP μ P. The emulator runs in real time. It has four complex hardware breakpoints and two 4-ksample \times 104-bit trace buffers. The unit comes with 256 kbytes of emulation memory. Emulator and software, \$16,000; software-performance-analysis unit, \$2500; software for Sun or Apollo workstations, \$1000.

Huntsville Microsystems Inc, 3322 S Memorial Pkwy, Huntsville, AL 35801. Phone (205) 881-6005. FAX (205) 882-6701. TWX 510-600-8258. Circle No. 383

KEPCO TRIPLE OUTPUT, LOW PROFILE, OEM a-c TO d-c SWITCHING MODULES

SERIES MRW/35 AND 50 WATTS



FEATURES:

- **115/230V a-c operation without user intervention:** Special flyback circuit accepts any input voltage from 90V to 264V a-c.
- **Power-OK logic (TTL compatible) signal** may be used as *power fail* signal. Logic "1" is given when +5 output is above 4.5V.
- **Current trade-off:** Current may be increased from one of the outputs at the expense of the others, within the limits defined by Figure 1.
- **Adjustable voltage:** Internal trimmer accessible through the case allows manual adjustment of the voltage setting.
- **Overvoltage protection for principal output** shuts down all outputs if output voltage is forced beyond the set limit.
- **Holding time:** Output is sustained by internally stored energy for 30 milliseconds typically, 20 milliseconds minimum.
- **Built-in EMI filter** attenuates conducted noise below the requirements of FCC 20780 for Class B computing devices.
- **Safety:** All models recognized by UL, certified by CSA, and approved by TÜV Rheinland to meet VDE 0806/IEC 380.

MRW INPUT CHARACTERISTICS

SPECIFICATION	MRW 150KV MRW 151KV	MRW 160KV MRW 161KV	CONDITION
Voltage range	90 to 264V a-c; 130 to 370V d-c		
Brownout voltage	85V a-c; 120V d-c		Maximum load
Current	1.0A	1.3A	Typ load, 115V a-c
	0.5A	0.8A	Typ load, 230V a-c
Fuse value	2.5A	3A	
Initial, turn-on surge, first 1/2-cycle.	50A max		115V a-c, typical load 25°C cold start
Frequency	50/60Hz nominal; range 47-440Hz ⁽¹⁾		Single Phase
EMI	Meets the conducted noise standard of FCC 20780, Class B and VDE 0871, Class B		
Leakage current	0.5mA		115V a-c (UL method) 25°C
	0.75mA		230V a-c (VDE method) 25°C
Startup time	400msec (typ)	500msec (typ)	Std. ⁽²⁾
Holdup time	20ms		Std. ⁽²⁾
Circuit type	Flyback		
Switching frequency	~100KHz	80KHz typ	Operating

(1) At 440Hz the leakage current exceeds the UL/VDE safety specification limit.

(2) Std conditions = nominal input, typical load, 25°C



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TUV APPROVED



MRW OUTPUT CHARACTERISTICS

SPECIFICATION	MRW 150KV/MRW 151KV			MRW 160KV/MRW 161KV			CONDITION
	OUTPUT #1	OUTPUT #2	OUTPUT #3	OUTPUT #1	OUTPUT #2	OUTPUT #3	
Source effect	1% max	1% max	1% max	2% max	2% max	1% max	90-132V a-c or 180-264V a-c
Load effect	3% max	5% max	1% max	4% max	2% max	1% max	Minimum load to rated load
Temperature effect	2% max	2% max	1% max	2% max	2% max	1% max	Nominal input, rated load, 0-50°C
Combined effect (source, load, & temperature)	+4%-2% max	+4%-6% max	±6% max	±4% max	+6%-4% max	±6% max	Initial setting 5.00V ± 20 mV
Time effect (drift)	0.5% max						0.5-8.5 hr; nom input, rated load, 25°C
Cross effect	Output #1	—	4.0% max	0.5% max	—	4.0% max	Load change from minimum to typical, nominal input 25°C
	Output #2	1.5% max	—	0.5% max	1.5% max	—	
	Output #3	0.5% max	0.5% max	—	0.5% max	0.5% max	
Recovery characteristics:	<4.0%						Step load change from 50% to 100% of rated load. Nominal input, 25°C
Recovery (within ± 1%)	<2msec						



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MRW MODEL TABLE

SPECIFICATION	OUTPUT VOLTAGE		OVP SETTING	OUTPUT CURRENT	CURRENT LIMIT	OUTPUT POWER				RIPPLE		NOISE (SPIKE)	EFFICIENCY
	Units	Volts	Volts	Amps		Watts				SOURCE	SWITCHING	mV	Percent
Condition	Factory set ⁽¹⁾	Adjustment range ⁽³⁾	Nominal input, 25°C	50°C (See Fig. 1)	Nominal input	40°C	50°C	60°C	71°C	Nominal input, typ load p-p max		d-c 1b 20MHz p-p max	Nom input, rated load typ
MRW 150KV (35 WATTS)													
Output #1	+ 5	4.75-5.25	5.8-6.9 ⁽²⁾	1.0-2.2 (typ) (4.0 max)	Total maximum output power no more than 38.5 Watts	35.0	35.0	24.5	14.0	30	50	150	70%
Output #2	+ 12	—	—	0.6-1.8 (typ) (2.5 max)						30	50	290	
Output #3	- 12	—	—	0-0.1 (typ) 0.3 (max)						10	20	290	
MRW 151KV (35 WATTS)													
Output #1	+ 5	4.75-5.25	5.8-6.9 ⁽²⁾	1.0-2.2 (typ) (4.0 max)	Total maximum output power no more than 38.5 Watts	35.0	35.0	24.5	14.0	30	50	150	70%
Output #2	+ 15	—	—	0.6-1.4 (typ) (2.0 max)						30	50	290	
Output #3	- 15	—	—	0-0.1 (typ) 0.3 (max)						10	20	290	
MRW 160KV (50 WATTS)													
Output #1	+ 5	4.75-5.25	5.8-6.9 ⁽²⁾	1.0-5.0 (typ) (6.0 max)	Total maximum output power no more than 60 Watts	50	50	35	20	30	50	150	72%
Output #2	+ 12	—	—	0.6-2.0 (typ) (2.5 max)						30	50	290	
Output #3	- 12	—	—	0-0.1 (typ) 0.5 (max)						10	20	290	
MRW 161KV (50 WATTS)													
Output #1	+ 5	4.75-5.25	5.8-6.9 ⁽²⁾	1.0-5.0 (typ) (6.0 max)	Total maximum output power no more than 60 Watts	50	50	35	20	30	50	150	73%
Output #2	+ 15	—	—	0.5-1.5 (typ) (2.0 max)						30	50	350	
Output #3	- 15	—	—	0-0.1 (typ) 0.4 (max)						10	20	350	

(1) Nominal input, typical load, 25°C

(2) All outputs are shut down when OVP is activated

(3) Output #2 follows the adjustment of Output #1

KEPCO TRIPLE OUTPUT, LOW PROFILE, OEM a-c TO d-c SWITCHING MODULES SERIES MRW

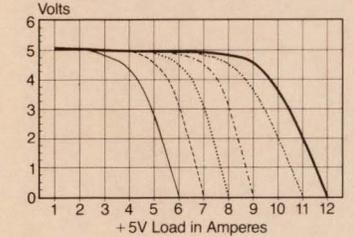
A new series of multi-output PC card switchers featuring a low profile (component height) on the popular 100x160mm footprint. The MRW 150KV and MRW 151KV produce 35W. MRW 160KV and MRW 161KV are rated for 50W continuous duty. All are triple output designs in which output #3 (the "—" rail) is stabilized by a 3-terminal regulator.

MRW GENERAL SPECIFICATIONS

SPECIFICATION	RATING/DESCRIPTION	CONDITION	
Temperature	0-71°C (see model table)	Operating	
	- 40 to 85°C	Storage	
Humidity	95% RH	Non-condensing; operating & storage	
Shock	20g, 3 axes (11msec ± 5msec pulse duration)	Non-operating 3 shocks each axis	
Vibration	5-10Hz: 10mm amplitude	Non-operating 1 hour each axis	
	10-55Hz: 2g, 3 axes		
Isolation	Output to ground	500V d-c, 100MΩ	25°C, 65% RH
Withstand voltage	Input to output	3.75KV a-c for 1 minute	25°C, 65% RH Y capacitor removed
	Input to ground	2KV a-c for 1 minute	25°C, 65% RH
Safety	UL 478 recognized, CSA C22.2 certified. VDE 0806/IEC 380 approved by TÜV Rheinland		
Type of construction	PC card		
Enclosure	Optional metal		
Cooling	Convection		

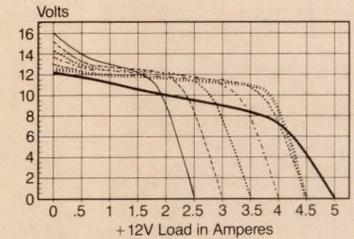
A feature of MRW is the ability to draw nearly full power from either of the two "+" rails. The curves reproduced to the right illustrate how the current from one output can be balanced against the other to power your application. Note the effect of the secondary voltage dropping when the primary output's load is reduced below its minimum value (the stabilization of the secondary output is degraded).

MRW 150KV
Plot of +5V as a Function of +12V Load



— +12V = 0A - - - +12V = 1.0A - - - +12V = 2.0A
- - - +12V = 5A - - - +12V = 1.5A - - - +12V = 2.5A

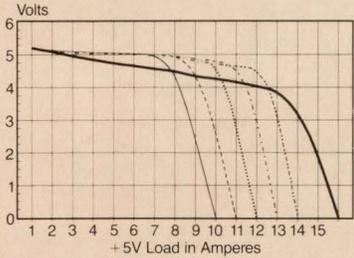
MRW 150KV
Plot of +12V as a Function of 5V Load



— 5V = 0A - - - 5V = 1A - - - 5V = 3A - - - 5V = 5A
- - - 5V = .5A - - - 5V = 2A - - - 5V = 4A

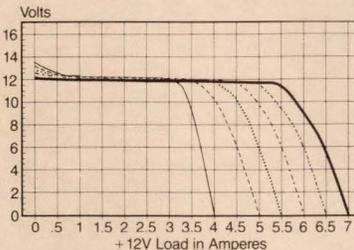
MRW 151KV curves are similar

MRW 160KV
Plot of +5V as a Function of +12V Load



— +12V = 0A - - - +12V = 1.0A - - - +12V = 2.0A
- - - +12V = .5A - - - +12V = 1.5A - - - +12V = 2.5A

MRW 160KV
Plot of +12V as a Function of 5V Load



— 5V = .5A - - - 5V = 2A - - - 5V = 4A
- - - 5V = 1A - - - 5V = 3A - - - 5V = 5A

MRW 161KV curves are similar

KEPCO TRIPLE OUTPUT, LOW PROFILE, OEM a-c TO d-c SWITCHING MODULES SERIES MRW

FIG. 1
OUTPUT RATINGS (MRW 150KV)
MAX POWER: 38.5W

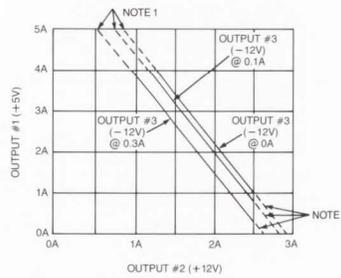


FIG. 1
OUTPUT RATINGS (MRW 151KV)
MAX POWER: 38.5W

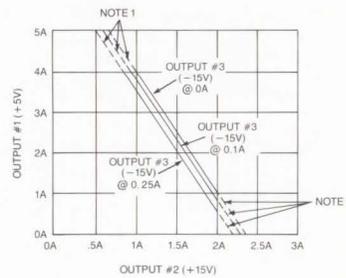


FIG. 1
OUTPUT RATINGS (MRW 160KV)
MAX POWER: 60W

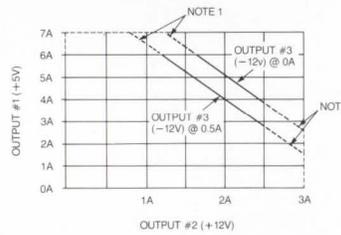
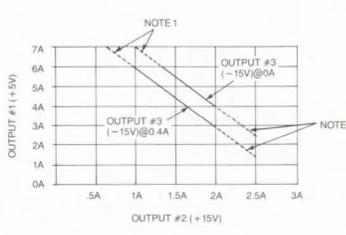


FIG. 1
OUTPUT RATINGS (MRW 161KV)
MAX POWER: 60W



NOTE 1:
Forced air 20 CFM
at 1 atmosphere

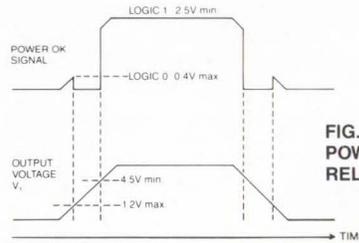


FIG. 2
POWER OK SIGNAL
RELATED TO OUTPUT

DIMENSIONS

MRW 150KV:
inches — 1.14 x 3.94 x 6.3
mm — 29 x 100 x 160

MRW 151KV:
inches — 1.14 x 3.94 x 6.3
mm — 29 x 100 x 160

MRW 160KV:
inches — 1.5 x 3.94 x 6.3
mm — 38 x 100 x 160

MRW 161KV:
inches — 1.5 x 3.94 x 6.3
mm — 38 x 100 x 160

NET WEIGHT

MRW 150KV: 12.35 oz, 350 gm
MRW 151KV: 12.35 oz, 350 gm
MRW 160KV: 17.65 oz, 500 gm
MRW 161KV: 17.65 oz, 500 gm

OPTIONAL STEEL ENCLOSURES:

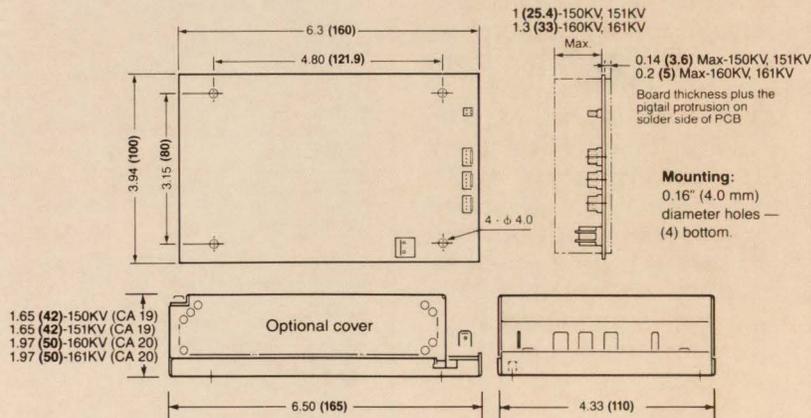
For MRW 150KV: CA 19
For MRW 151KV: CA 19
For MRW 160KV: CA 20
For MRW 161KV: CA 20

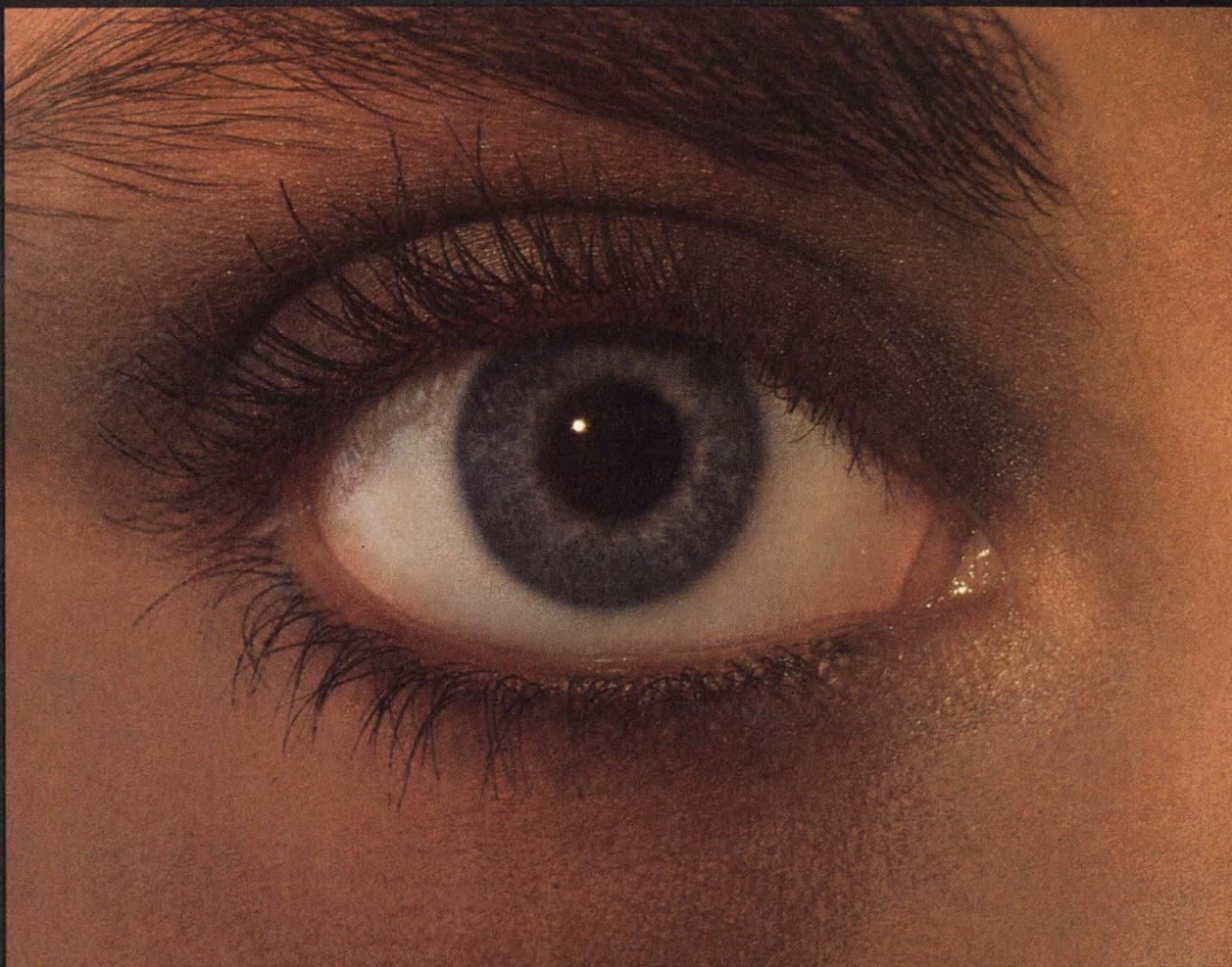
INPUT-OUTPUT CABLE KITS:

For MRW 150KV — 219-0184
For MRW 151KV — 219-0184
For MRW 160KV — 219-0184
For MRW 161KV — 219-0184

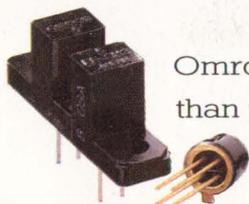
OUTLINE DIMENSIONAL DRAWINGS

Dimensions in light face type are in inches, dimensions in bold face type are in millimeters.





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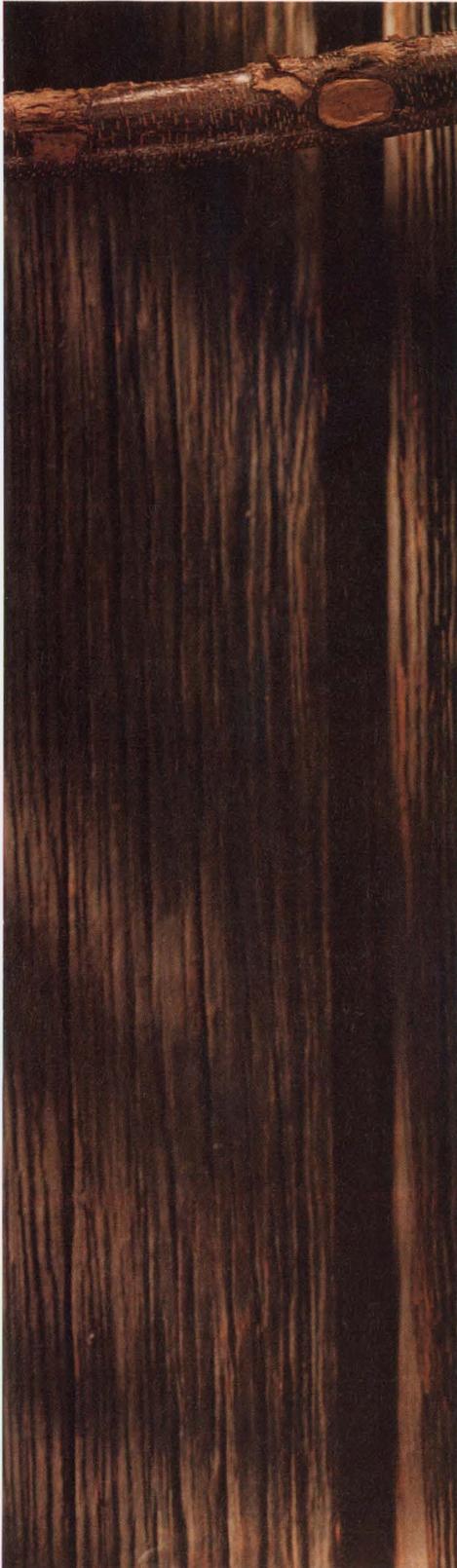
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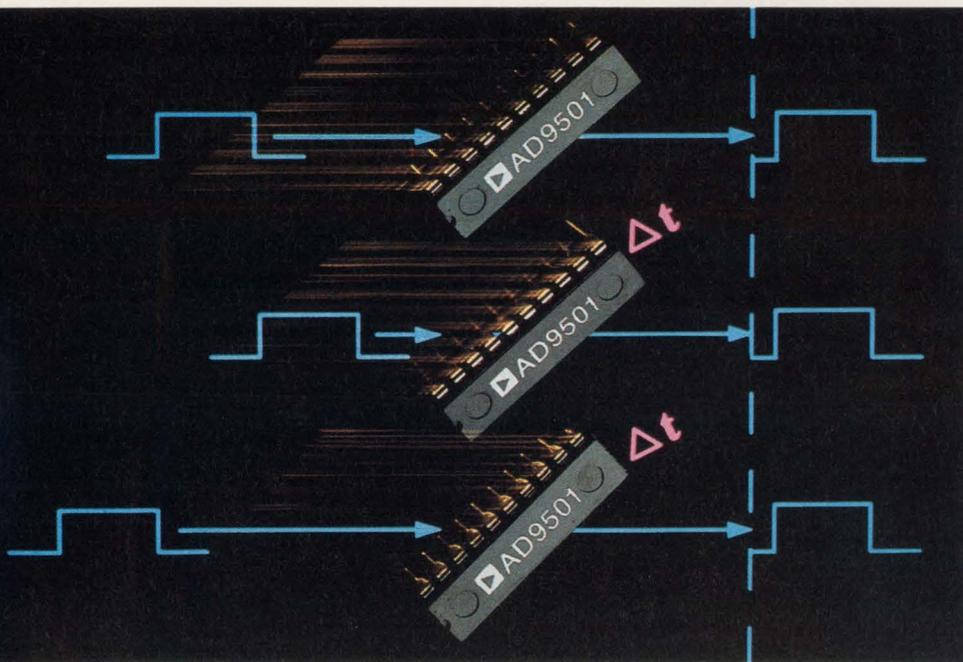



**TEXAS
INSTRUMENTS**

Delay lines take on timing tasks

As system designs get more complex and operating speeds get faster, timing must be extremely precise. Programmable delay lines let designers adjust circuit timing and maximize the performance of today's high-speed systems.

Tom Ormond, Senior Technical Editor



Designed for ATE and radar applications, Analog Devices' AD9501 TTL-compatible delay generator provides digitally programmable pulse time adjustments ranging from 2.5 nsec to 10 μ sec.

PROGRAMMABLE DELAY lines allow designers to readily introduce timing corrections in today's systems. These devices employ control inputs to generate a variable delay between input and output signal transitions. The variable delay lets OEMs stock a single part for a variety of applications requiring delay lines. For one, you can use the variable delay in

upgradable PCs to resolve speed mismatches between the upgraded CPU and the system clock.

Most programmable-delay-line applications fall into two categories—de-skewing and timing generation. In the first case, the lines cancel or compensate for the variations generated by system components. Typical de-skew applications would be found in clock-distribution systems, high-speed buses, instrumentation, and test equipment—especially automatic test equipment (ATE). In timing-generation applications, the delay line is used to initiate events at specified times. Typical applications would involve test equipment and other instrumentation.

Programmable delay lines typically employ one of two circuit approaches: selected path or analog variable. In analog-variable delay lines, the designs employ a constant signal path but rely on a variable control level to develop a given propagation delay. The ramp-and-generator design is a popular analog-variable approach because it is flexible and linear. In this design, an input signal transition causes a ramp voltage to start from an initial

level. The ramp and control voltage levels serve as the inputs of a comparator that switches at a time determined by the value established at the control inputs.

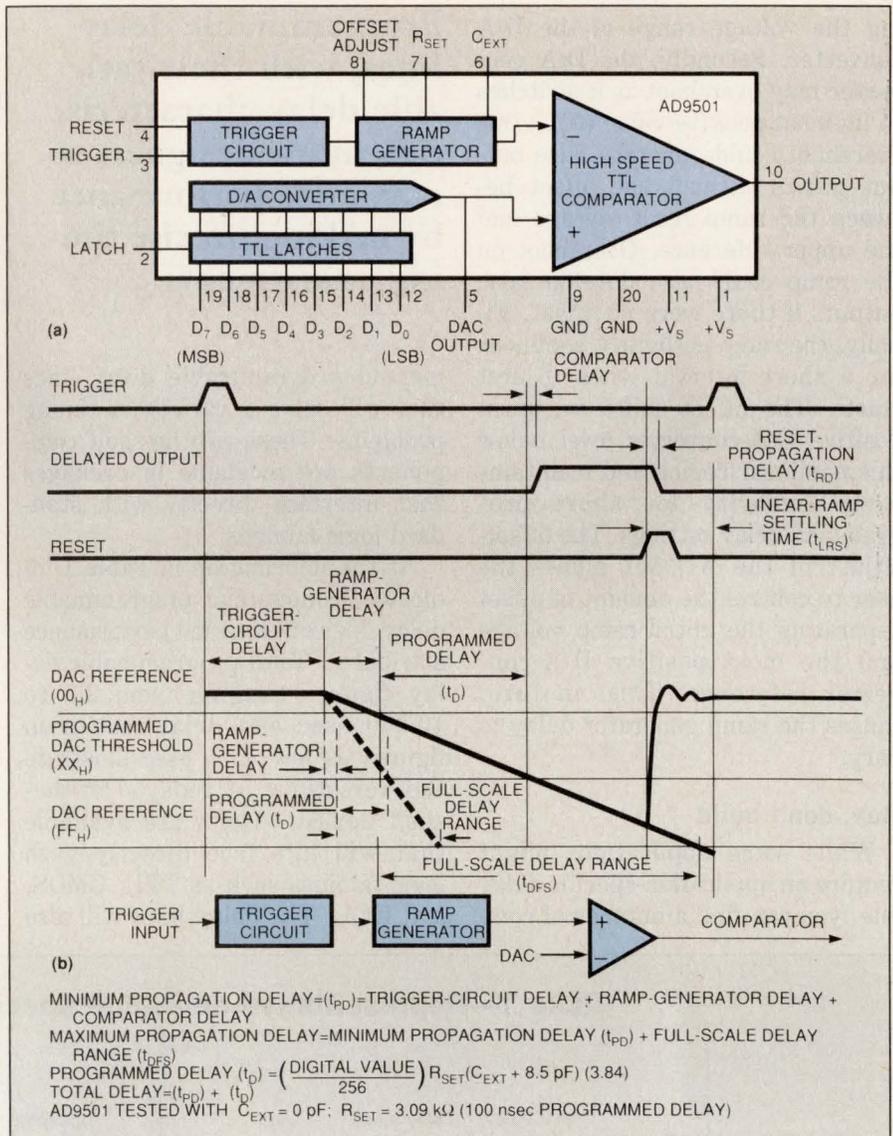
Selected-path devices use digital gates to select one of several fixed-delay paths between the input and the output. Selected-path devices can consist of different elements, including transmission lines, digital gates, and RC delays. All these elements may be configured either in series or in parallel.

While implementations vary from manufacturer to manufacturer, most off-the-shelf programmable delay lines rely on similar operating theory. Hence, examining a single delay line—Analog Devices' AD9501—will give some insight into the internal workings of delay lines in general.

The inside story

As the block diagram in Fig 1a illustrates, the AD9501 consists of three main subcircuits—a linear ramp generator, an 8-bit D/A converter, and a voltage comparator. The rising edge of the input trigger pulse initiates the delay cycle by enabling the ramp generator. The voltage comparator monitors the ramp generator output and switches the delayed output High when the ramp voltage crosses the threshold set by the D/A-converter output voltage. Users program the threshold of the D/A-converter output voltage using digital inputs D_0 through D_7 .

The internal timing diagram of the AD9501 (Fig 1b) provides a detailed illustration of how the delay is established. Minimum delay value t_{PD} equals the sum of trigger-circuit delay, ramp-generator delay, and comparator delay. The trigger-circuit delay and the comparator delay are fixed; ramp-generator delay varies as a function of the rate of change of the linear ramp and, to a lesser degree, the



value of the offset voltage. Maximum delay is the sum of minimum delay (t_{PD}) and full-scale program delay (t_{DFS}). Ramp-generator delay is a measure of the time required for the ramp to slew from its reset voltage to the most positive D/A-converter reference voltage (00_H). The difference in these two voltages is nominally 18 mV with offset-adjust open or 34 mV with offset-adjust grounded.

These two voltage levels require an offset between them for three reasons. An offset allows the ramp to reset and settle without reenter-

Fig 1—To provide a programmable delay, the AD9501 employs three main subcircuits—a ramp generator, a D/A converter, and a voltage comparator (a). The internal timing diagram (b) illustrates how the unit establishes the required delay.

ing the voltage range of the D/A converter. Secondly, the D/A converter may overshoot as it switches to its most positive value (00_H); this overshoot could generate false output pulses without the offset between the ramp reset voltage and the upper reference. Overshoot on the ramp could also develop false outputs if there were no offset. Finally, the ramp is slightly nonlinear for a short interval when it first starts. The offset shifts the most positive D/A-converter level below this nonlinear region and maintains ramp linearity for short programmed delay settings. The offset-adjust of the AD9501 allows the user to control the amount of offset separating the initial ramp voltage and the most positive D/A-converter reference. This, in turn, causes the ramp generator delay to vary.

Buy, don't build

While some applications might require an application-specific delay line, you can find a number of com-

Programmable delay lines, with their variable delay characteristics, allow designers to maximize performance by making precise timing adjustments.

mercial programmable delay lines that will solve a variety of timing problems. These off-the-shelf components are available in packages that interface directly with standard logic families.

As the information in **Table 1** indicates, commercial programmable delay lines offer varied performance attributes. Total programmable delay figures ranging from 2.5 to 10,000 nsec and delay-resolution figures as low as 5 psec illustrate the versatility of today's off-the-shelf devices. Units are available that will interface directly with logic families such as TTL, CMOS, and ECL. The delay lines will also

operate at trigger rates as high as 800 MHz. Off-the-shelf delay lines are available for both commercial and military applications.

While the figures in the **table** illustrate delay-line capability, they don't tell the whole story; today's off-the-shelf units offer other advantages. When you look at pc-board real estate considerations, you'll find plenty of packaging options—14-, 16-, and 20-pin DIP, 28-pin PLCC (plastic leaded chip carrier), 32-pin quad flatpack, and gull-wing, surface-mount units. All TTL-compatible units operate from one 5V supply, so there's no problem with unique power-supply requirements to consider. The TTL-compatible delay lines also have good driving capabilities—from 10 to 20 gates.

Technitrol and Analog Devices offer products screened to MIL-STD-883, and the PLD-ACT devices from Engineered Components have a standby mode power drain of only 5 nW. Brooktree even makes it easy to familiarize yourself

Table 1—Representative delay-line specifications

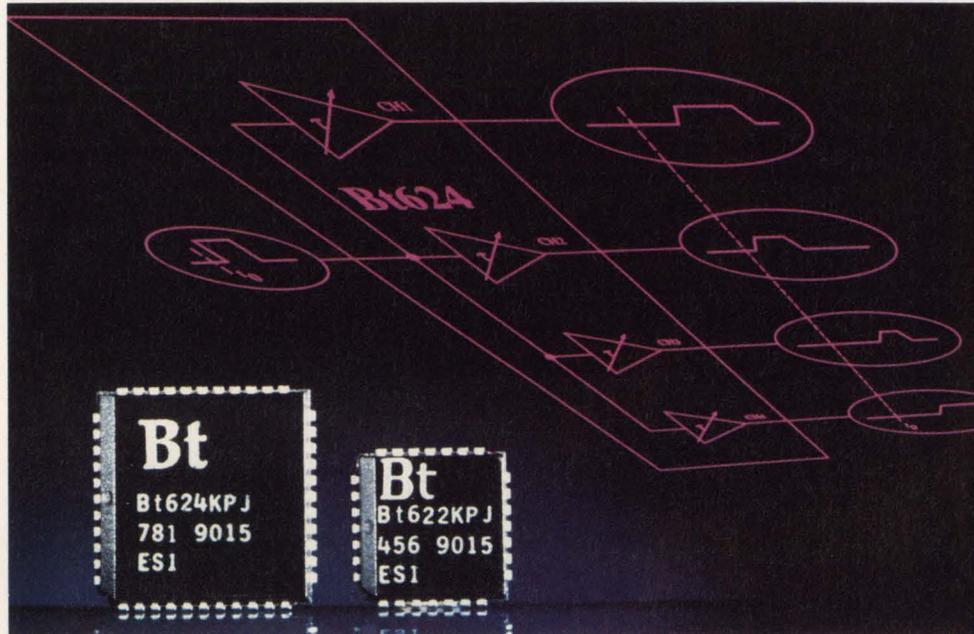
Manufacturer	Model	Total delay (nsec)	Delay steps (psec)	Logic output	Trigger rate (MHz)	Operating range	Package	Circuit type (AV=analog variable, SP=selected path)	Price
Analog Devices	AD9501	2.5 to 10,000	10	TTL, CMOS	50	0 to 70, -55 to +125°C	20-pin DIP, plastic leaded chip carrier	AV	From \$8.60 (100)
Brooktree	BI630	25 to 400	NS	TTL	50	-55 to +125°C	14-pin DIP	AV	\$11.10 (100)
Dallas Semiconductor	DS1020	74 to 522	250 to 1000	CMOS	0.020	0 to 70°C	16-pin DIP	AV	\$13 (1000)
Elmec Technology	PDL 6	3.1 to 31	50 to 500	ECL	80	-10 to +60°C	12-pin single in-line package	SP	\$63 (1000)
Engineered Components	PDL-ACT	15 to 358	1000 to 50,000	TTL	To 80	-40 to +85°C	16-pin DIP	SP	\$15 (100)
Motorola	MC10E/100E195	2.58	20	ECL	1000	0 to 85°C	28-lead plastic leaded chip carrier	SP	\$38.07
Newport	60A	14 to 91	1000 to 12,000	TTL	NS	0 to 70°C	16-pin DIP	NS	£3.8
Sony	CBX1159QY	1.4 to 22	5	ECL	800	-55 to +125°C	32-pin quad flatpack	SP	\$25 to \$40 (100)
Technitrol	GCTR PC	13 to 111	1000 to 15,000	TTL, CMOS	0.100 to 1	-55 to +125°C	16-pin gull-wing surface mount	AV	\$49 (100)

NS=Not specified.

with standard delay products. They offer a demonstration board that lets you test and evaluate the performance of their BT630 programmable delay lines. The board includes circuitry that can generate a TTL input signal that has user-selectable period and pulse width. The board also includes DIP switches to set the delay range and potentiometers for making fine delay-time adjustments.

Maximizing flexibility

The PDL-ACT devices from Engineered Components have been designed to allow for final delay adjustment during installation or after the lines have been installed in a circuit. These delay lines incorporate all required drive and pick-off circuitry and are self-contained in a 16-pin DIP. Compatible with TTL, advanced CMOS, and FAST (Fairchild Advanced Schottky TTL) logic families, the delay lines feature a hybrid design that includes compensation for propagation de-



Featuring delay ranges of 10, 20, or 30 nsec, Brooktree's continuously adjustable delay lines are available in dual (Bt622) and quad (Bt624) versions.

lays and incorporates internal termination at the output—no additional external components are required to obtain the required delay.

The delay lines are programmed

by inputting a logic 1 or 0 at each of the three programming pins. Because only dc levels are involved, you can program the lines using remote switches or you can perma-

For more information . . .

The following companies form a representative list of manufacturers that offer programmable delay lines; they supplied information used to prepare this article. For more information on the products discussed in the article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the manufacturers directly, please let them know you saw their products in EDN.

Analogue Devices Inc
Box 9106
Norwood, MA 02062
(617) 329-4700
FAX (617) 326-8703
Circle No. 650

Brooktree Corp
9950 Barnes Canyon Rd
San Diego, CA 92121
(619) 452-7580
FAX (619) 452-7294
Circle No. 651

Dallas Semiconductor
4401 S Beltwood Pkwy
Dallas, TX 75244
(214) 450-0400
Circle No. 652

Elmec Technology of America Inc
1255 Corporate Center Dr
Suite 406
Monterey Park, CA 91754
(213) 265-1861
FAX (213) 265-1908
Thomas Miracle
Circle No. 653

Engineered Components Co
Box 8121
San Luis Obispo, CA 93403
(805) 544-3800
FAX (805) 544-8091
Bo Wilkes
Circle No. 654

Motorola Inc
Semiconductor Products Sector
2100 E Elliot Rd
Tempe, AZ 85284
(602) 897-3615
FAX (602) 897-4193
Circle No. 655

Newport Components Ltd
Tanners Dr
Blakelands North
Milton Keynes MK14 5NA, UK
(908) 615232
TLX 825621
Peter Osborn
Circle No. 656

RF Technology Inc
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South Norwalk, CT 06854
(203) 866-4283
FAX (203) 853-3513
Chris Kallay
Circle No. 657

Sony Corp of America
10833 Valley View St
Cypress, CA 90630
(714) 229-4331
FAX (714) 229-4333
Circle No. 658

Technitrol
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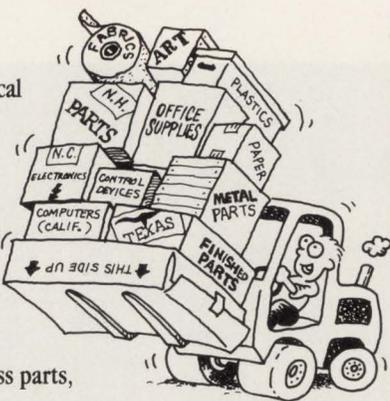
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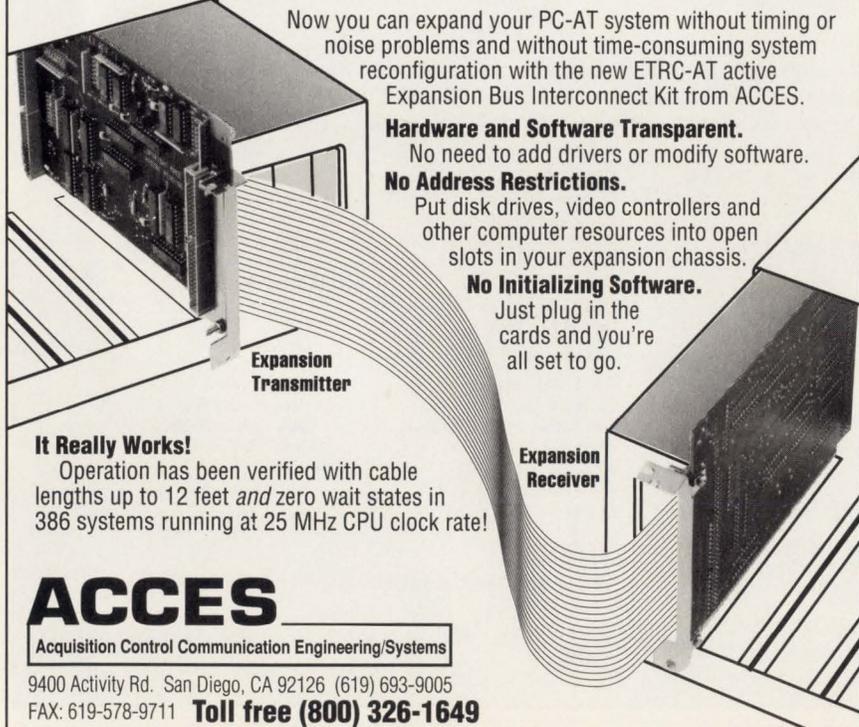
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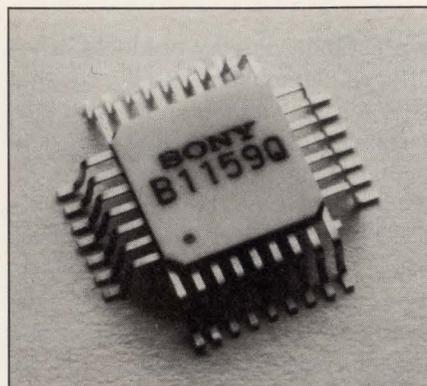
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CIRCLE NO. 50

COMPONENTS



With an 800-MHz max operating frequency, Sony's ECL-compatible delay lines are designed for high-speed bus, test-equipment, and clock-distribution applications.

nently terminate the programming pins. You can also automatically program the PLD-ACT devices using computer-generated data—multiplexer setup time is typically 3 nsec.

Looking down the road

Today's off-the-shelf programmable delay lines offer high performance. However, looking down the road, designers want more. They want more on-board functionality, higher resolutions, and faster programmability. This is particularly true in mixed-signal and VLSI ATE, where programmable-delay networks play an important role in minimizing overall test times without sacrificing precision. Multichannel event-triggered applications require more functionality and easier interfacing to μ P/control circuitry.

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THE SERIES 6600/6700 THERMOSTATS

Now you can ensure the highest level of thermal protection for your P.C. board without compromising its design. Specify an Airpax Series 6600 or 6700 miniature bimetallic snap-action thermostat.

The 6600 provides precise sensing of ambient temperatures in applications where the control of high temperatures is crucial. The 6700 gives you accurate thermal surface sensing when mounted on heat sinks in applications such as

Small things come in good packages.

The 6700 conforms to Y220/TO220 international product package standards, so you can automatically insert and solder the thermostats onto your board with high-speed automated equipment. The nickel-plated copper mounting bracket assures accurate thermal conductivity for heat-sink applications.

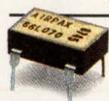
Excellent repeatability from 40°C to 110°C.

Series 6600/6700 thermostats provide fast, positive response with 1-amp switching capability at 48 Vdc over their operating range of 40°C to 110°C (104°F to 230°F) for a minimum of 30,000 operations. The operating temperature is pre-set at the factory. Both the 6600 and 6700 meet UL and CSA standards.

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power supplies. Both the 6600 and 6700 are ideal for today's crowded P.C. boards, where reliable thermal protection is essential. And space is at a premium.

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The 6600 is VDE approved; the 6700 is VDE pending.

A little information goes a long way.

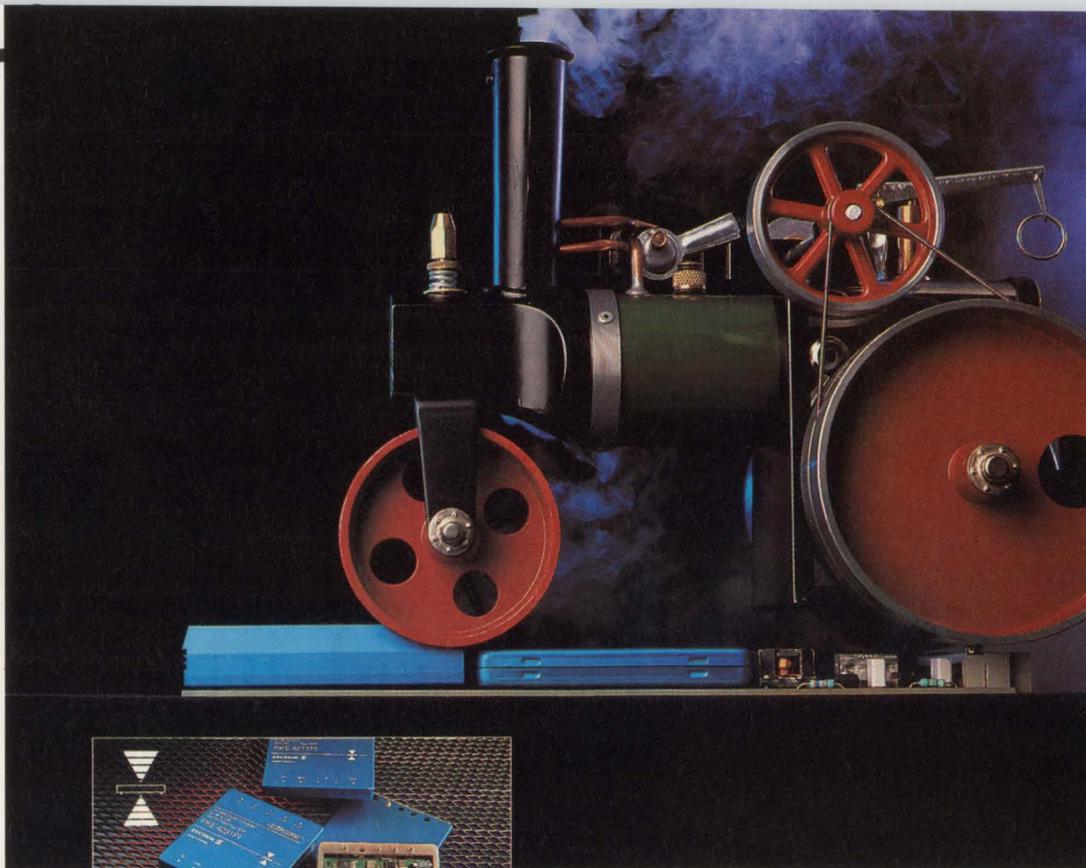
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The new PKE is a 25-30 W DC/DC converter squeezed into a slim package little more than half the height of its predecessor, the internationally acclaimed PKA converter. The PKE is only 10.7 mm (0.42") high and has the same 3"x3" industry-standard footprint and pin out.

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Perhaps most surprisingly, performance is in no way compromised by the size reduction. In fact, the PKE is even better than the PKA. A wide input voltage of 38 to 72 VDC is complemented by 1500 VDC isolation, 80-85% typical efficiency and two million hours MTBF at +45 °C ambient.

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Hong Kong:	Ericsson Components , East Asia, Wanchai, Tel: +852-5-75 66 40 Fax: +852-834 53 69
Italy:	Ericsson Components Europe , Milano, Tel: +39-2-33 20 06 35 Fax: +39-2-33 20 06 41
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Sweden:	Ericsson Components AB , Stockholm, Tel: +46-8-757 43 84 Fax: +46-8-757 44 21
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Telephone _____

Fax _____

CIRCLE NO. 34

ERICSSON 

Components

Sealed toggle switch meets severe-environment demands

If your control panel needs a toggle switch that can withstand the rigors of road graders, farm vehicles, or industrial processing equipment, the NT Series from Micro Switch is worth a look. Switches in the series have lever-to-bushing and cover-to-case seals made from a molded elastomer, as well as terminal inserts that are molded into the high-impact thermoplastic case.

This complete sealing of the switching chamber enables the toggle switches to comply with the UL 508, paragraph 13.3 hose-down test. You can use these switches in control panels that are subjected to periodic splashes or wash downs, such as the panels common to food and beverage equipment. The switches can also withstand exposure to heavy accumulations of moisture, such as that experienced by vehicles left outdoors overnight.

Options include 1-, 2-, or 4-pole



circuitry; screw, quick-connect, or solder terminals; and momentary or maintained action. The switches are available in 5, 10, and 15A ratings. The toggle levers are 0.68-in. long and have a nonglare nickel finish. In addition to the bat-handle toggle lever, the company can furnish pull-to-unlock and logic-level versions.

NT Series switches have an operating range of -40 to $+71^{\circ}\text{C}$ and are UL recognized and CSA certified. List prices range from \$11.59 to \$26.44.

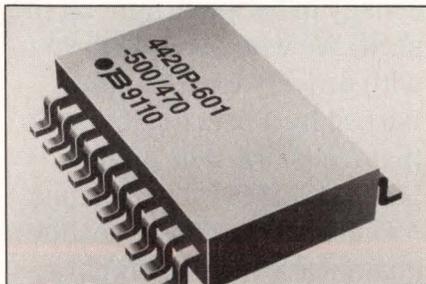
Micro Switch, 11 W Spring St, Freeport, IL 61032. Phone (815) 235-6600.

Circle No. 688

Surface-mount RC networks satisfy EMI/RFI filter applications

Advances in digital IC technology are creating stringent demands for the reduction of electromagnetic interference (EMI) and radio-frequency interference (RFI) in electronic equipment. EMI/RFI filters are used in personal computers, data terminals, test equipment, and process controllers to suppress high frequencies. Bourns's 601 Series EMI/RFI lowpass filters are smaller and less expensive than inductive-type filters. The filters come in surface-mount packages and use a resistor-capacitor (RC) network.

Featuring a T-configuration of 16



series resistors and 8 parallel capacitors, the filters can handle filtering for as many as eight lines. The filters are available with resistor values of 10 to 100 Ω and capacitor values of 50 to 200 pF. Using 25 Ω resistors, a filter's typical 3-dB

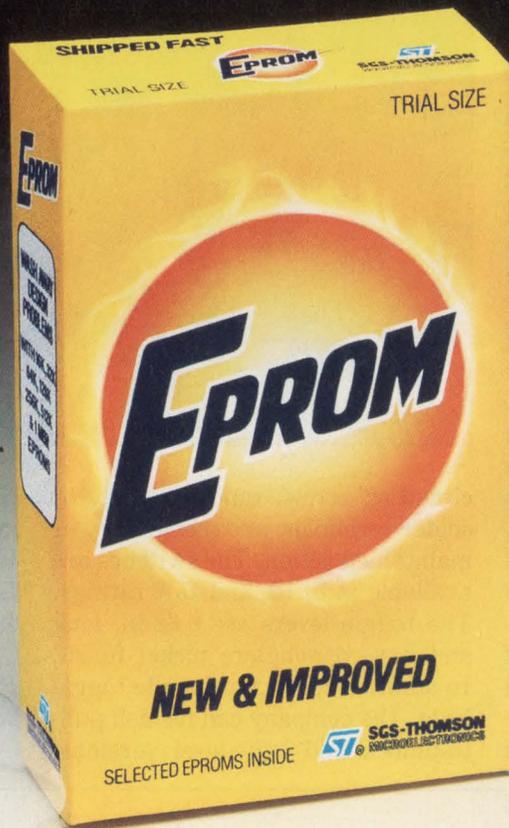
attenuation point ranges from 20 to 64 MHz, depending on the capacitor value.

The tolerance for component values is $\pm 10\%$ for resistors and $\pm 30\%$ for capacitors. The operating temperature range is 10 to 85 $^{\circ}\text{C}$. In addition to 18- and 20-pin surface-mount packages, the filters are available in 18- and 20-pin plastic DIPs. Prices for the 601 series EMI/RFI filters begin at \$2.15 (10,000).

Bourns Networks Inc, 1400 N 1000 W, Logan, UT 84321. Phone (801) 750-7200.

Circle No. 689

How to wash away memory problems.



The tide is turning. More and more people are washing their hands of ordinary memories and looking to SGS-THOMSON for EPROMs and EEPROMs.

One big reason: our new King Size 4 Megabit device. It's specially formulated with high-performance ingredients to make your designs come out sparkling: CMOS low power, plus an 80ns super-fast access speed, ultra-short programming time and more.

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and 2 Meg devices, plus every density in between, right off the shelf. We won't soft-soap you with delivery excuses either. Backed by a list of distributors that reads like Who's Who, SGS-THOMSON ships on time.

Our serial EEPROMs feature guaranteed one million Erase/Write cycles and are available in I²C and MICROWIRE® bus versions.

No wonder we're now one of the world's top EPROM suppliers.

And we'll continue to sparkle in the memory business.

Full-feature serial EPROMs in 4K and 8K sizes are ready to hit the shelves. And our 16 Meg EPROM is in the works!

Let SGS-THOMSON's quality, selection and service wash away your memory problems once and for all.

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MICROELECTRONICS

SGS-THOMSON Microelectronics
1000 E. Bell Rd., Phoenix, AZ 85022 (602) 867-6259

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Whether You
Go By The
Book



Or Write
Your Own
Ending...



The NEW Piher Opens Up Unlimited Specifying And Design Options

The New Piher is now backed by the resources of The Meggitt Group. Powered by a nationwide sales and distribution network. Poised to offer you unmatched resistive component options and value.

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Choose from a complete, quality line of carbon and cermet trimmer potentiometers in a wide range of specifications. All are competitively priced and readily available

from one of the nation's most extensive inventories.

And all Piher components (as evidenced by our prestigious Ford Q-1 award) meet the highest standards for quality and reliability.

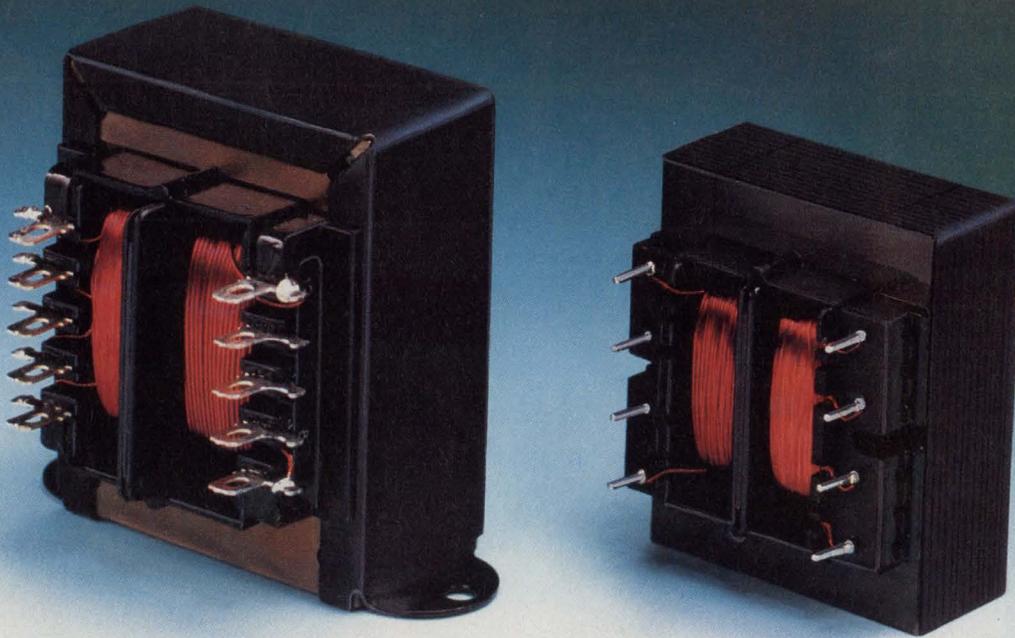
Find out more about the New Piher. For a Free 108-page Product Catalog, call 1-800-323-6693, or write Piher, 903 Feehanville Drive, Mt. Prospect, IL 60056.

In Illinois call 708-390-6680.
FAX: 708-390-9866.



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NEW TRANSFORMERS FOR CLASS 2 APPLICATIONS.

DUAL BOBBIN DESIGNS FEATURE 4000 VRMS PRIMARY AND SECONDARY ISOLATION.

* INHERENTLY LIMITED
 ** NON-INHERENTLY LIMITED
 MAXIMUM FUSE VALUE SPECIFIED
 ALL PRIMARIES ARE 115/230 VOLT 50/60 HZ

PART NO.	SECONDARY RMS RATING	FUSE REQ.	PRICE
CL2-25-12	12V @ 2.10A	2.5A**	14.50
CL2-25-24	24V @ 1.05A	N/A*	14.50
CL2-40-12	12V @ 3.33A	4.0A**	18.50
CL2-40-24	24V @ 1.66A	2.0A**	18.50
CL2-80-24	24V @ 3.33A	4.0**	25.25

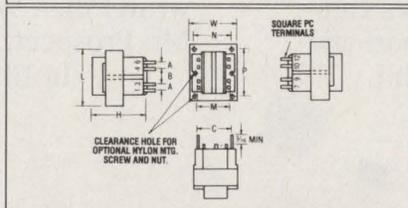
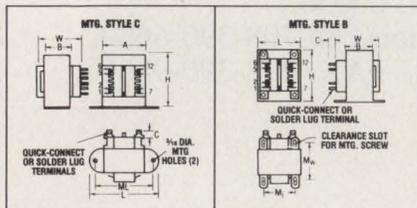
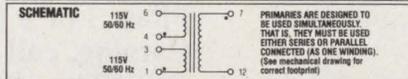
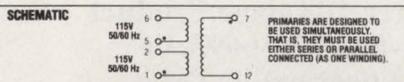
PART NO.	SECONDARY RMS RATING	FUSE REQ.	PRICE
CL2-2.5-12	12V @ .20A	N/A*	9.00
CL2-2.5-24	24V @ .10A	N/A*	9.00
CL2-5.0-12	12V @ .42A	N/A*	9.75
CL2-5.0-24	24V @ .20A	N/A*	9.75
CL2-10-12	12V @ .83A	N/A*	10.90
CL2-10-24	24V @ .42A	N/A*	10.90
CL2-20-12	12V @ 1.66A	N/A*	13.25
CL2-20-24	24V @ .833A	N/A*	13.25
CL2-30-12	12V @ 2.50A	3.0A**	15.25
CL2-30-24	24V @ 1.25A	N/A*	15.25
CL2-50-12	12V @ 4.20A	5.0A**	18.65
CL2-50-24	24V @ 2.10A	2.5A**	18.65

Signal "The American Original" introduces a new family of transformers for 2.5 to 80 VA applications that require low power and a high degree of isolation. These new "Class 2" transformers feature the same dual high-temperature bobbin construction and insulating shroud originally developed for the company's very successful International Series. Available in both PC and chassis mount versions, they offer a choice of inherently limited or non-inherently limited designs and feature 4000 VRMS primary and secondary isolation.

Signal's insulation system results in very high isolation between the primary and the secondary windings, and between either winding and the core. The dual bobbin design reduces capacitance and eliminates the need for an electrostatic shield. The Class 2 dual bobbin series satisfies UL 1585 requirements and CSA safety and performance standards.

Signal transformers are available through Signal's PRONTO 24-Hour Off-the-Shelf shipment program. For additional technical data, contact Signal Transformer, 500 Bayview Avenue, Inwood, N.Y. 11696.

BUY DIRECT
 (516) 239-5777
 Fax: (516) 239-7208



DIMENSIONS						Pin			Mtg. Screw			
VA	L	W	H	A	B	Dimensions	M	N	P	Size	Quantity	Lbs.
2.5	1 1/8	1 1/8	1 1/8	200	250	1.000	0.025SQ	1 1/8	-	#4	2	0.25
5.0	1 1/8	1 1/8	1 1/8	200	400	1.000	0.025SQ	1 1/8	-	#4	2	0.37
10.0	1 1/8	1 1/8	1 1/8	200	400	1.140	0.038SQ	1 1/8	-	#4	2	0.53
20.0	2 1/4	1 1/8	1 1/8	400	400	1.460	0.038SQ	1 1/2	-	#4	2	0.90
30.0	2 1/8	2 1/8	1 1/8	550	275	1.680	0.045SQ	-	1 1/4	#6	4	1.15
50.0	3	2 1/2	1 1/8	600	300	1.900	0.045SQ	-	2	#6	4	1.70

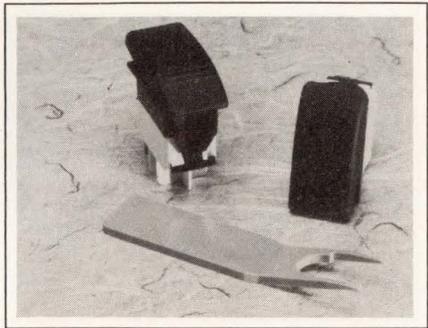
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The American Original.™

THE PRONTO™ PLEDGE

Because we are America's largest stocking manufacturer of power magnetics (over 1000 part numbers), we promise to ship a minimum of 24 pieces in 24 hours.

Components



Power Switch With Environmental Shielding

Designed to meet the needs of the marine, trucking, automotive and food-processing industries, the V series switch provides complete protection against dust and prolonged immersion in water under pressure. The short-throw, rocker-actuated panel switch is available with a rocker made from a hard, thermoplastic surface or a soft, rubberized surface. The rockers are easily removable using an actuator removal tool, allowing separate stocking of base assemblies and actuators. Illumination options include neon, incandescent, or LED lamps. The switch has a 15A/125V rating. \$2.80 (1000). Delivery, six weeks ARO.

Carlingswitch Inc, 60 Johnson Ave, Plainville, CT 06062. Phone (203) 793-9266. FAX (203) 793-2239. Circle No. 390

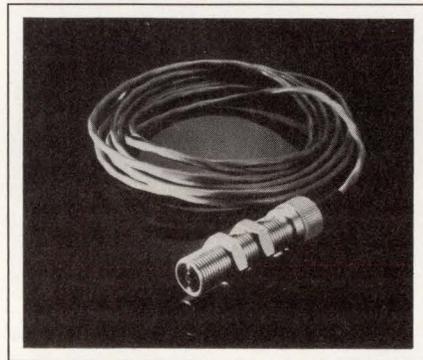
Picosecond Delay Lines

The PE-23451 to PE-23460 series delay lines help control clock skew and allow users to fine-tune critical clock-distribution circuits. The series comes in delay values from 100 to 1000 psec, in 100-psec increments. The delay lines have an impedance of 50 Ω and a maximum dc resistance of 0.5 or 1 Ω , depending on part number. The devices meet UL 94V-0 flammability ratings. \$2.44 (1000).

Pulse Engineering, 7250 Convoy Ct, San Diego, CA 92111. Phone (619) 268-2400. FAX (619) 268-2515. Circle No. 391

Magnetic Speed Sensor

Model 70084-1000-077 magnetic speed sensor features a 10-ft cable assembly, allowing for easier positioning of a tachometer or process controller used in conjunction with the sensor. The sensor features a stainless-steel body and pole piece and measures 2.75 \times 0.74 in. The output voltage is 190V p-p with an external 100-k Ω load. The operating temperature range is -40 to +107 $^{\circ}$ C. Applications include variable and constant-speed motor or turbine controls, fans, and compres-



sors. In unit quantities, sensor/cable assembly, \$35.

Airpax, Cheshire Industrial Park, Cheshire, CT 06410. Phone (800) 982-0030; (203) 271-6000. Circle No. 392

Noise-Suppression Capacitor

Constructed with a series-wound polyester dielectric rated at 250V ac, the RBEX series of noise-suppression capacitors are available with standard values between 0.01 and 1 μ F. The capacitors can handle transient spikes of 2.5 kV and have a rated dielectric withstanding voltage of 1075V dc for 2 sec. Depending on the capacitance value, the maximum pulse-rise-time rating is between 100 and 200V/ μ sec. The capacitors meet the requirements of UL-1414, CSA C22.2, and VDE 0565-1 (approvals are pending) for line-to-line capacitors. The capacitors have a flame-retardant case and epoxy fill that meets the requirements of UL-94V-0, and they

can operate between -55 and +100 $^{\circ}$ C. From \$0.50 to \$3 (100).

Aerovox Inc, Electronic Products Group, 742 Belleville Ave, New Bedford, MA 02745. Phone (508) 999-1000. Circle No. 393

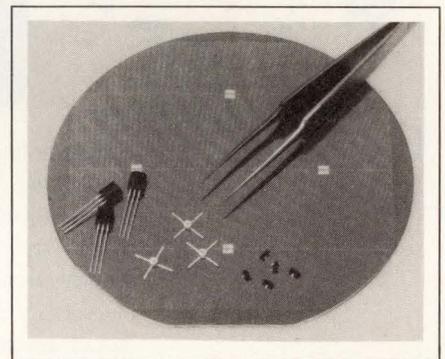
Low-Profile Crystal

The CP21B range of low-profile crystals suits surface-mount applications. You can choose a frequency in the 16- to 110-MHz range to a tolerance of \pm 10 ppm. Temperature coefficient is \pm 5 ppm over the temperature range -10 to +50 $^{\circ}$ C. The leadless package size is 7.5 \times 5.1 \times 1.3 mm. Sample quantities, \pounds 4.30.

NDK Europe Ltd, Tolworth Tower, Ewell Rd, Surbiton KT6 7EL, UK. Phone (81) 390-8344. FAX (81) 390-6926. Circle No. 394

Microwave Transistor

Designed for VHF and UHF applications, the silicon bipolar B12V105 microwave transistor features a typical f_T of 10 GHz at a collector



current of 10 mA. At that current, the transistor has a gain of 18.1 dB at 1 GHz and 12.6 dB at 2 GHz. At 5 mA, the gain is 16 dB at 1 GHz. At a collector current of 2 mA, the noise figure is typically 1.6 dB at 1 GHz and 2 dB at 2 GHz. Package options include TO-92, SOT-23, SOT-143, 85-mil Micro-X, and hermetic 70-mil stripline. From \$0.99 (1000).

Bipolarics Inc, 5437 Scotts Valley Dr, Scotts Valley, CA 95006. Phone (408) 438-0806. Circle No. 395

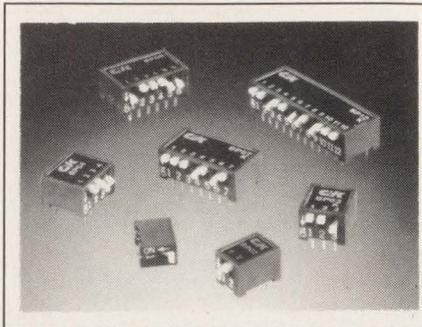
Components

10Base-T Filter And Common-Mode Choke

The 1661 filter and isolator and the 1662 common-mode choke meet requirements of IEEE-802.3 10Base-T network systems. The filter and isolator provide 17-MHz lowpass filtering with 2-kV isolation in both transmit and receive lines. The

common-mode choke attenuates common-mode noise signals by 20 dB, without differential loss. The 1661 and 1662, in 16- and 8-pin DIPs, respectively, £3.88 and £1.86 (100).

Newport Components Ltd, Tanners Dr, Blakelands North, Milton Keynes MK14 5NA, UK. Phone (908) 615232. Circle No. 396



Side-Actuated DIP Switch

The BP series of side-actuated DIP switches consists of 10 spst models having 1 through 8, 10, or 12 positions. Wiping contacts provide reliable switching, and high-temperature materials meet UL 94V-0 requirements. The contacts are rated at 100 mA (max) and have a resistance of <math><50\text{ m}\Omega</math>. All terminals are tin plated and epoxy sealed. Models are also available with gold-plated contacts. 8-position switch, \$1.08 (1000).

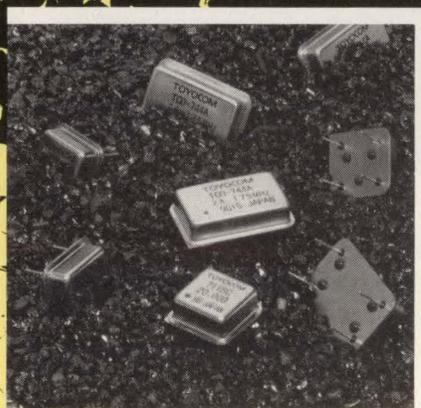
C&K Components Inc, 15 Riverdale Ave, Newton, MA 02158. Phone (617) 964-6400. FAX (617) 527-3062. Circle No. 397

Solid-State Relays

The LH1500 family of solid-state relays features 21 devices that represent the most common relay forms. Included are Form A, Form B, Form A/B,C and dual versions of Form A and B. The relays use a GaAs LED for actuation control and a monolithic silicon chip comprising a photodiode array, control circuitry, and a DMOS output switch. Some of the relays employ current-limiting circuitry, enabling them to pass FCC voltage-surge requirements. The Form A/B relays have a break-before-make action that provides a true Form-C function in a solid-state relay. From \$1.25 to \$4.75 (1000).

AT&T Microelectronics, Dept 52AL040420, 555 Union Blvd, Allentown, PA 18103. Phone (800) 372-2447, ext 810. In Canada, (800) 553-2448, ext 810. Circle No. 398

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TIMING IS EVERYTHING

CIRCLE NO. 44



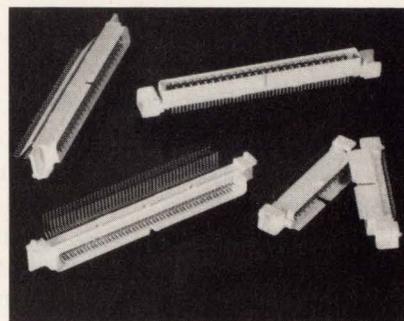
BNC Cable Assemblies

- Impedance matched
- High strength molded terminations

Meritec's BNC impedance matched cable assemblies are available in a var-

ety of configurations, including cable end plug, cable end jack, front panel mount jack, front panel mount jack with isolated ground and rear panel mount jack. The connectors are terminated to subminiature coax cable and feature standard BNC and cable impedances of 50 and 75 ohms. High strength molded terminations make the assemblies ideal for critical applications requiring high reliability. The assemblies may be terminated with Meritec's SSI™, SSC™, SPI™ or PCB Solderable interconnects on the opposite end.

Mark No. 40 on Inquiry Card



.050" Pitch Hermaphroditic Connectors eliminate the need for separate male and female parts

- Feature .050" centers
- 50 Ω impedance matched

Meritec introduces a new concept in board-to-board interconnects—CP50™ Hermaphroditic Connectors. Each mating half is identical in configuration, eliminating the need for separate male and female parts. Close pitch .050" centers minimize board space requirements. The 50 Ω, impedance matched connectors feature precision, high strength molded terminations for reliability in critical applications and are designed to meet IR or vapor phase reflow requirements. Contact tails come in SMT and through hole configurations, straight and right angle.

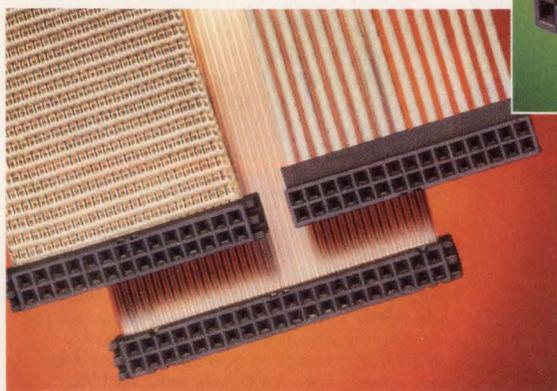
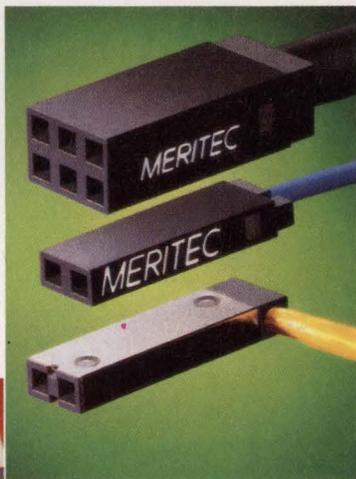
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High-Performance Interconnects That Terminate High Cost.

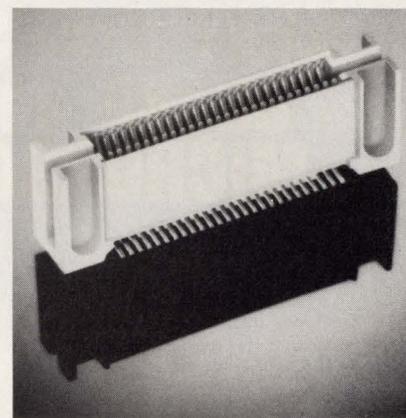
Meritec has terminated the high cost of high performance interconnects for fast logic applications. We produce a full line of cable assemblies for applications in the 3ns to sub nanosecond range—engineered to match your requirements for controlled impedance and propagation rate while minimizing crosstalk. We deliver assemblies of unparalleled quality. On time. At a very reasonable price.

Our complete line includes Single Signal Interconnects (SSI™), Shielded Performance Interconnects (SPI™) and Multi Signal Interconnects (MSI™), terminated to a diversity of controlled impedance cables, including coax, twin coax, FEP, PTFE and our Filatex™ textile cable.

Call Meritec today at 216-354-3148 for more information and a free copy of our capabilities brochure.



1359 West Jackson Street
P.O. Box 8003
Painesville, Ohio 44077
216-354-3148
FAX: 216-354-0509



Card Edge Connectors with .050" centers are available in SMT and through hole configurations

Meritec's CP50™ Card-Edge Connectors are designed with .050" centers to minimize board space requirements. The 50 Ω, impedance matched connectors are ideal for high density board-to-board applications. The connectors are designed to meet IR or vapor phase reflow requirements. Through hole and SMT contact tail configurations are available. Precision, high strength molded terminations provide reliability in critical applications.

Mark No. 40 on Inquiry Card

CIRCLE NO. 40

Components

Accurate Power Resistors

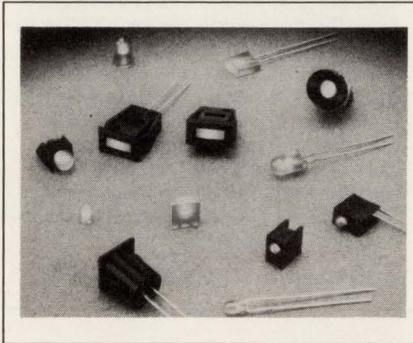
The PAC-series wirewound resistors have 1% accuracy and power ratings of 2 to 6W. Resistance values range from 0.22 Ω to 12 k Ω in E24 steps. Temperature coefficient is <100 ppm/ $^{\circ}$ C, and long-term stability is <0.5%. The size of the 2W version is 13 \times 5.5 mm, and the 6W version is 25 \times 7.5 mm. 1 k Ω , 2W resistor, gld 35 (100).

Philips Components, Box 218, Bldg BAF-153, 5600 MD Eindhoven, The Netherlands. Phone (40) 722091. FAX (40) 724825.

Circle No. 399

Amber LEDs

Emitting a wavelength of 605 nm, these LEDs exhibit a true amber color. In the color spectrum, the amber hue falls between that of pure yellow at 580 nm and standard orange at 630 nm. Because of its



“emotionally neutral” color, an amber LED is commonly used in automotive instrument-panel lighting. Previously, designers who wanted a near-amber hue had to use yellow LEDs that were off-color to the high side, or orange LEDs off-color to the low side. The LEDs are available in T-1, T-1 $\frac{3}{4}$ and 2 \times 5-mm shapes. The devices can handle a steady peak-current of 30 mA, and a pulsed current (10- μ sec duty cycle) of 155 mA. Light efficiency is 2 lm/W and quantum efficiency is

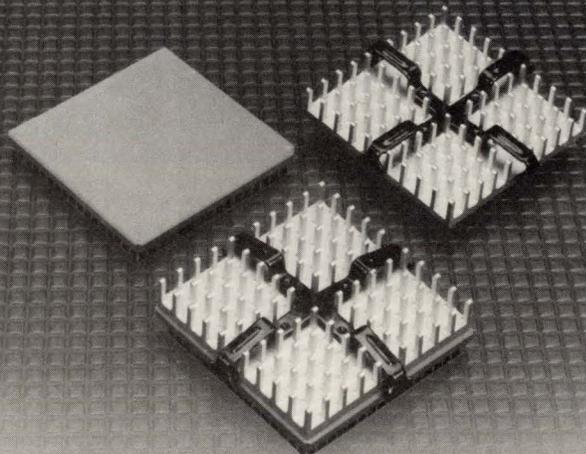
0.6%. Depending on quantity and package style, \$0.15 to \$0.50. Delivery, stock to eight weeks ARO.

Lumex Opto/Components Inc, 292 E Hellen Rd, Palatine, IL 60067. Phone (708) 359-2790. FAX (708) 359-8904. Circle No. 400

Subminiature Pin-Plunger Optical Switch

Offering longer service life and higher reliability than traditional mechanical switch designs, the EE-SA105 optical switch operates without a contact mechanism. The subminiature, pin-plunger switch uses an infrared LED and phototransistor combination to activate the device, eliminating the contact bounce and wear associated with electro-mechanical switches. The EE-SA105 activates with a 15-gram (max) operating force and has a 0.059-in. (max) pretravel and a

HEAT SINKS for INTEL 80486 and i860XR MICROPROCESSORS



EG&G WAKEFIELD ENGINEERING
60 AUDUBON ROAD, WAKEFIELD, MA 01880
TEL: (617) 245-5900 • FAX: (617) 246-0874

Designed for use with the Intel 80486DX and 80486SX microprocessors and the Intel i860XR RISC processor, packaged in 168-pin ceramic PGAs, the EG&G Wakefield 669 Series Heat Sink/Clip Assembly offers a cost-effective heat dissipation solution for today's high-speed microprocessors. This assembly provides the highest clamping force available with a nylon-coated stainless steel clip, for the most efficient interface heat transfer and to meet system shock and drop test requirements.

Our omnidirectional heat sink offers optimized heat dissipation and ease of application; the symmetrical clip is suitable for high volume installation with the EG&G Wakefield 162-IT installation tool.

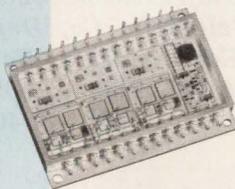
Heat dissipation with the 669 Series Heat Sink/Clip Assembly is optimized for PC, workstation, and server applications with low airflows (e.g., 50-200LFM). Pressure drop is minimized in multiple-processor applications.

Intel, 80486, i860XR, and 80386 are trademarks of Intel Corporation.

Call our Application Engineering Department today at (617) 245-5900 for information about the EG&G Wakefield Engineering 669 Series (patent pending) and other heat sinks for the Intel 80386 and 80486 microprocessor family. Also ask for information about the EG&G Wakefield DELTEM™ family of heat sinks for cooling high-speed cache RAM used with 50 MHz microprocessors.

POWER SOLUTIONS

Smart Power 3-Phase Bridge

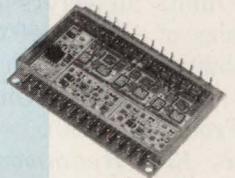


PWR-82331

The PWR-82331 is a 200V, 30A 3-phase motor drive hybrid. Contained within the PWR-82331 are six power MOSFETs and associated flyback diodes, which comprise the output stage. Each phase has separate high- and low-side gate drives to control the output stage, and protection circuitry that prevents simultaneous turn-on of upper and lower output FETs in the same phase. The internal drive and protection circuitry can operate on 5V or 15V logic levels and has Schmitt triggered inputs for noise immunity. The internal dc-dc converter provides constant high-side gate drive and power to the internal logic.

Circle #99 For Sales Contact, Circle #100 For Literature

Smart Power High Voltage 3-Phase Bridge

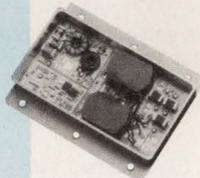


PWR-82333

The PWR-82333 is a 270V, 30A, 3-phase motor drive with a maximum voltage rating of 500Vdc. Designed for high-power motor applications, the PWR-82333 can deliver 10kW of power to the load. The PWR-82333 uses an IGBT output stage with flyback diodes, high- and low-side gate drives, and protection circuitry for in-line firing. The internal dc-dc converter supplies continuous power to the high-side drives for continuous operation even in stall conditions. Packaged in a 2.1" x 3.0" chassis mount package with a thermal resistance from junction-to-case of 0.85°C/W.

Circle #101 For Sales Contact, Circle #102 For Literature

60 Watt, Triple Output DC-DC Converter



PWR-82400

The PWR-82400 is a triple output 60W dc-dc converter. Designed using a forward converter topology, the PWR-82400 has a power density of 19.4 watts per cubic inch. Available as a ±15V or ±12V output at 1.3A and 1.7A respectively, both versions have a +5V output at 4Amps. The input voltage range is 16-40Vdc and operates under emergency power conditions in accordance with MIL-STD-704. Full power output is available up to +100°C case temperature with linear derating to 10 watts at +125°C.

Circle #103 For Sales Contact, Circle #104 For Literature

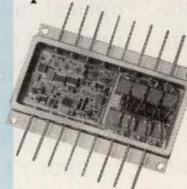
Solid-State Power Controllers



SSP-21110

The SSP-21110 series of 28 Volt dc, Solid-State Power Controllers (SSPCs) replace electromagnetic circuit breakers and solid-state relays rated from 2 thru 25 amp. They provide status outputs and permit logic input control so they may be remotely located near the load. Solid-state electronics offers instant trip (fault) and a true I²T trip protection for the wire and loads.

The SSP-21116 Series of 270 Volt dc, (SSPCs) replace electromagnetic circuit breakers and solid-state relays rated from 5 thru 15 amp. They provide status outputs and permit logic input control so they may be remotely located near the load. Solid-state electronics offers fault (under 25 μs) and a true I²T trip protection for the wire and loads. They also provide an output leakage clamp for system safety.



SSP-21116

Power MOSFET switches are used for their low "on" resistance, low voltage drop, high "off" impedance and low power dissipation. Built with power MOSFETs and custom monolithics and using thick-film hybrid technology, they offer small size, low power, and high reliability. There is isolation designed-in between the load power and the 5 volt control logic input and the status outputs.

A standard series of currents are available, however, optional current ratings, status outputs, and packages are available.

The SSP-21110 and SSP-21116 series will operate over the full military temperature range.

Circle #105 For Sales Contact, Circle #106 For Literature



Application Notes on SSPCs



Solid-State Power Controllers (SSPCs) are becoming the choice for the next generation military and industrial systems! Why! "SSPCs combine power switching and wire protection, with a computer control input and status feedback. These devices take digital input as control and return digital status, allowing computer control and monitoring of electrical power." DDC's application note AN/P-1, covers applications of SSPCs in the next generation power distribution systems and highlights SSPC advantages over conventional circuit breakers.

Circle #107 For Sales Contact, Circle #108 For Literature



Contact Bob Fryer, at (516)567-5600 ext. 390, for information on the above products.



Contact Steve Friedman, at (516)567-5600 ext. 381, for information on the above products.

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Components

0.035-in. (min) overtravel. The LED accommodates 50 mA of forward current and has a light-intensity degradation of only 7.5% over 500 hours of continuous operation at a forward current of 20 mA. \$0.99 (5000).

Omron Electronics Inc, 1 E Commerce Dr, Schaumburg, IL 60173. Phone (708) 843-7900. FAX (708) 843-7787. Circle No. 401

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μF. Tolerance is 0 to 100%, and capacitance stability is ±30 ppm for NPO types and ±15% for X7R types. Approximately \$2 (1000).

Spectrum Control Inc, 2185 W 8th St, Erie, PA 16505. Phone (814) 455-0966. Circle No. 402

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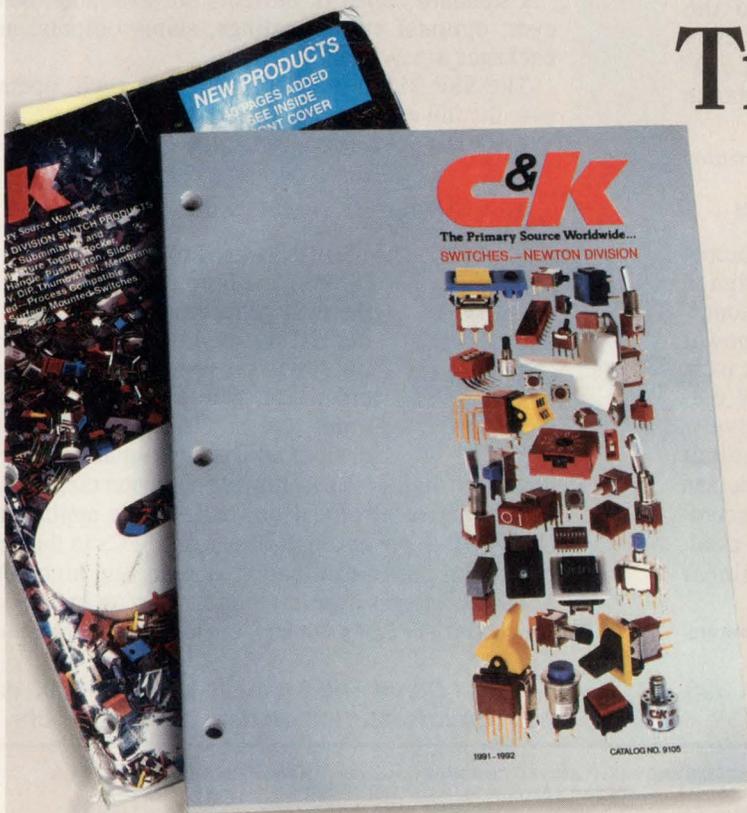
ing accessories are available. \$149.

Edmund Scientific Co, Dept 11B1, N900 Edscorp Bldg, Barrington, NJ 08007. Phone (609) 573-6250. Circle No. 403

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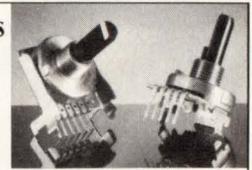
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BIG IDEA

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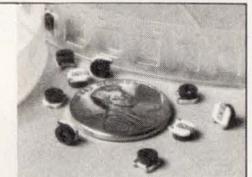
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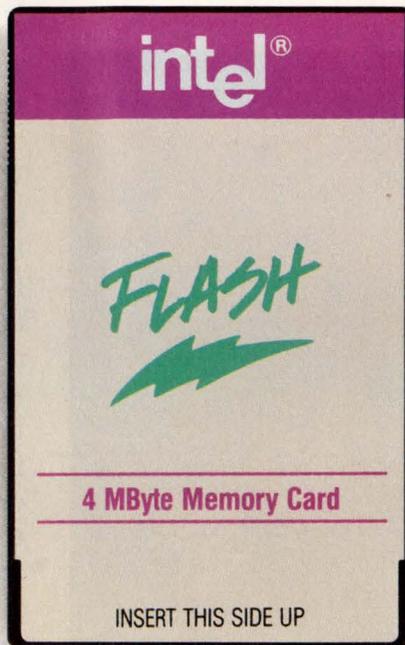
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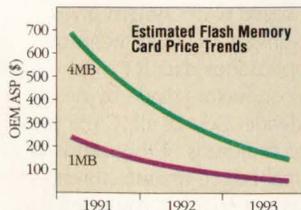
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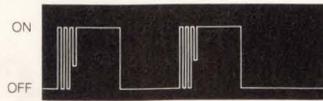
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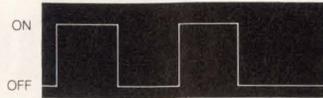
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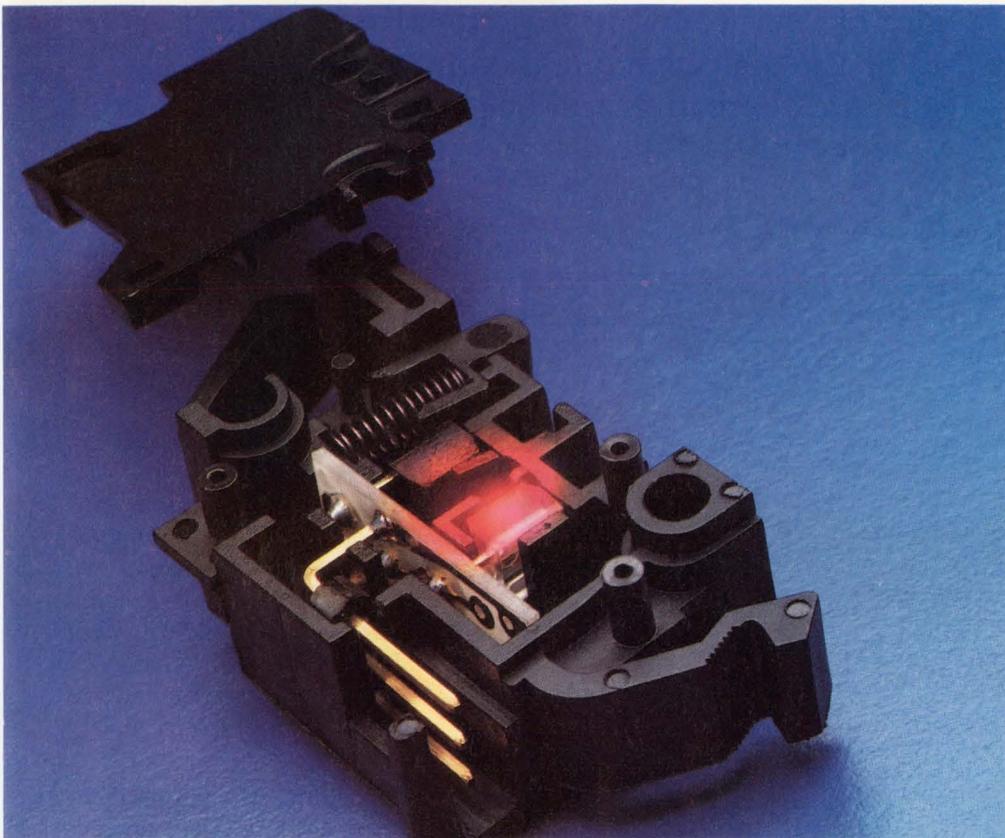
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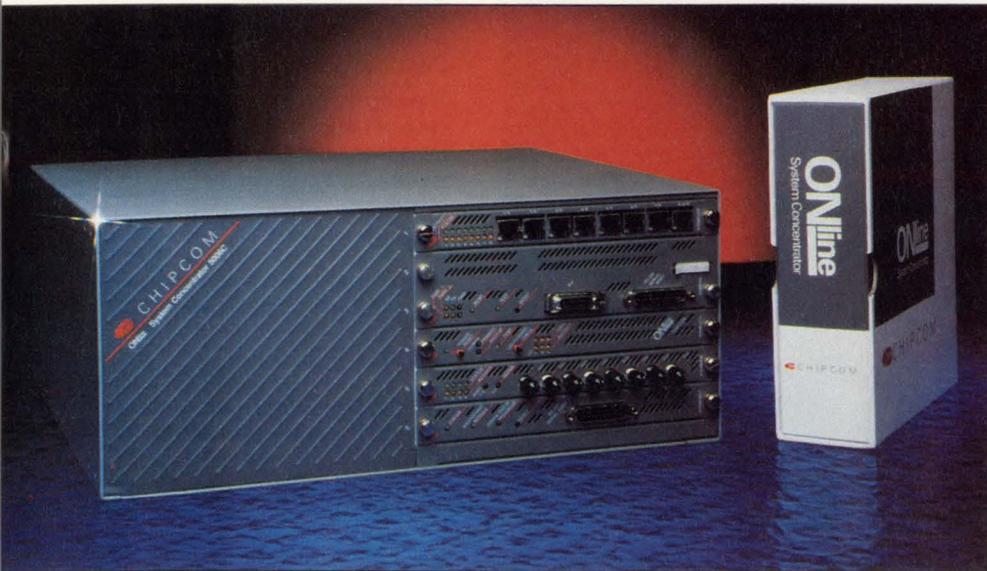
Circle #126 for Future Need

10/87

Arm yourself with LAN know-how

Setting up a local-area network is complicated—especially if you've never done it before. A clear idea of what you want to accomplish as well as a basic understanding of your hardware and software alternatives will help you deal with vendors and consultants.

Dan Strassberg, Technical Editor



A wiring hub might sound like a trivial item consisting of nothing more than terminal blocks and wire. But wiring hubs (also called concentrators) are places where you can best monitor LAN activity. This μ P-based unit from Chipcom (Southborough, MA) is for small 10Base-T Ethernet LANs. It performs network-management functions. \$2295 (\$2795 with redundant, fault-tolerant power supply.)

FOR A LONG MOMENT, the phone line was silent. When the consultant spoke, his tone was one of disbelief tinged with exasperation: "You're going to do what in eight pages?" he demanded. "I'm going to write a primer for engineers who have no LAN experience and whose managers want them to set up a local-area network in an engineering department or a manufacturing-test area," I replied, my manner reflecting

more humility than it had earlier. "I'm hoping to get these people to the point where they can ask questions of LAN hardware and software vendors without embarrassing themselves," I continued. There was another pregnant pause. "It's clear that you don't understand how enormous this field is," the consultant retorted. "I don't think you can do what you want to do; I'm not sure anyone can. For certain, what you've described would take a LAN expert, and you aren't one." "I know," I said, "but I'm certainly going to try."

At this point, the consultant seemed to change the subject abruptly; he asked if I ever get to New York City. I happened to be going the following week. He recommended that I stop at the McGraw-Hill Bookstore at 1221 Avenue of the Americas in Manhattan. Several other people gave me similar advice, asserting that the store's collection of technical books is unequalled elsewhere. When I arrived at 1221 and descended into the basement store, I asked where I could find LAN books. The salesperson directed me to a section of

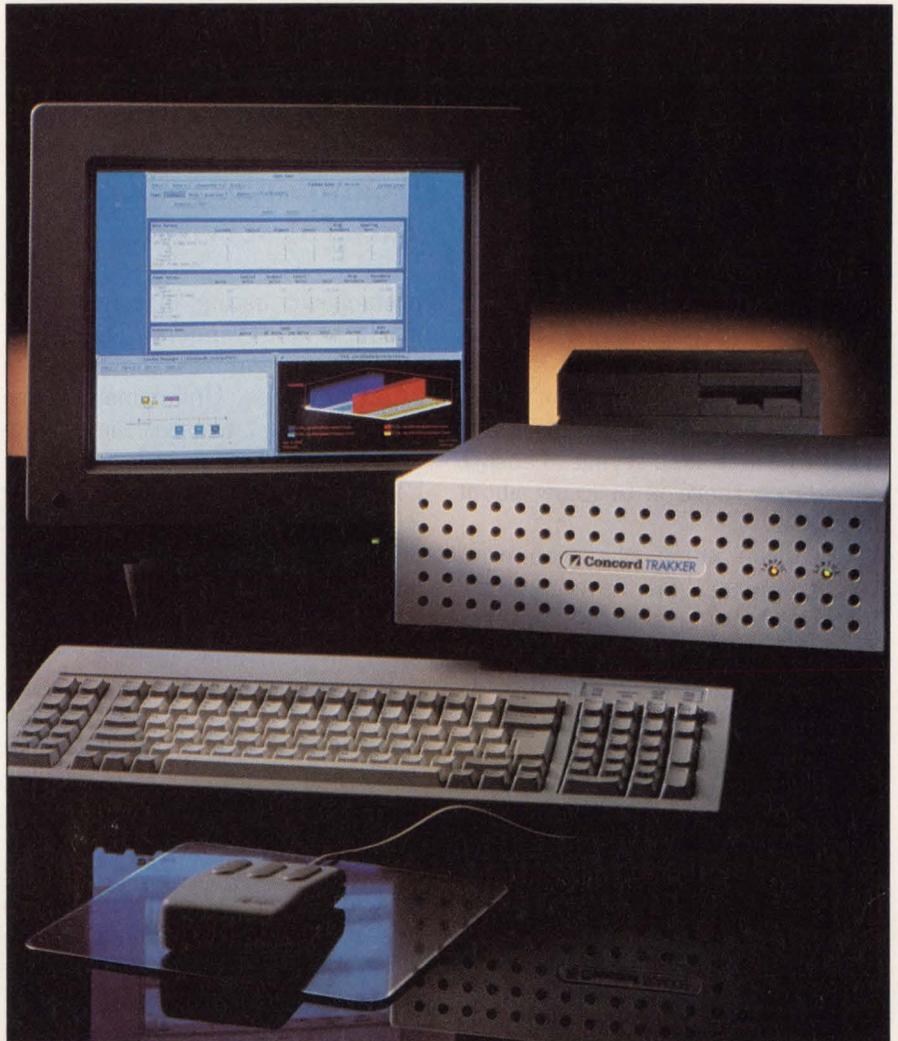
shelving at least four feet wide by eight feet high, filled from top to bottom and side to side with books on networking and LANs. Even after the warnings I had received, I gulped; I wasn't prepared for so much material.

I began to think that perhaps one of the most important things my tutorial could do would be to provide a reading list. The box "LANs: Read all about 'em" names the books I picked up at the bookstore and elsewhere, as well as a few magazine articles. Obviously, it includes only a small fraction of the LAN and networking materials available. However, some of the materials are particularly useful.

To paraphrase Sophie Tucker, a good LAN consultant, these days, is hard to find. The networking field is so vast and continues to evolve so rapidly that most consultants have experience with only a fraction of the available products. Indeed, many consultants are familiar with only a few *types* of products. Moreover, because of its complexity and rapid rate of change, the networking field is rife with mythology and strongly held opinions that, too often, result from an incomplete understanding. Unfortunately, the consulting fraternity is not totally innocent of disseminating misinformation.

Still, the situation is not all bad. If you have no networking experience, the person you need to guide you is someone with *relevant* experience—somebody who knows products and techniques likely to work for you, who understands where the pitfalls lie and how to avoid them. A consultant need not have experience with a wide variety of networking products and technologies. The important thing is that your consultant be familiar with networking requirements similar to your own.

Nearly all modern texts on net-



working begin with a diagram of the so-called 7-layer cake—the International Standards Organization's open-systems-interconnection model (the ISO/OSI model). In an attempt to guide you through the black forest of connectivity, the OSI model organizes network hardware and software into seven conceptual "layers." The ability to categorize an item as performing functions associated with one or more layers can be useful, because if you know where the product belongs, you will be less likely to compare it with another product whose function is not really equivalent.

Instead of digesting this cake, you may be better off first deter-

Continuous, real-time monitoring of network activity—including activity on very large and interlinked networks—is the function of Concord Communications Inc's (Marlboro, MA) Trakker System. The console costs \$18,000; segment monitors cost \$5200 each.

mining why you want to have a LAN. LAN projects are important enough to justify a considerable amount of study before you commit to a course of action. Understanding both your immediate and longer-term goals can save you from selecting a seemingly cost-effective approach that you will outgrow rapidly. And careful examination can lead you to products that are less costly than those you had thought necessary. Although you don't want to choose too quickly, you also don't want to waste time trying to absorb *everything* there is to know about networks.

Once you know what you want to accomplish, you have to avoid jumping to conclusions about the products you must have and being swayed by every input you receive. Keep an open mind while talking to vendors, but remember that claims that seem too good to be true usually are just that. The best immunization against seductive sales pitches is to inoculate yourself with information. If you become confused by conflicting claims as you evaluate products, take time for additional study.

F J Derfler, Jr's *PC Magazine Guide to Connectivity* (see **box**) organizes the process of determining your needs and selecting the classes of products most likely to meet them. Bound into the book is a decision tree (flow chart) that asks questions about the types of data you expect to share, how you propose to use the data, and the physical arrangement of the people and equipment you want to connect. Each time the tree leads you to a class of hardware or software, it highlights strong and weak points typical of products in the class. Considering the complexity of the issues it deals with, the simplicity of the diagram is reassuring.

Another strong point of the book is its extensive, though hardly com-

A consultant need not have experience with a wide variety of networking products and technologies to perform a useful service.

prehensive, listing of connectivity products and vendors. This 51-pg appendix organizes the products into categories. Unfortunately, the section doesn't present the categories in any obvious order, and the book's index fails to mention the categories. Individual companies and products do appear in the index, however.

Glossaries untangle technobabble

In addition to a directory of connectivity products and services, an item that you'll quickly realize you need is a glossary of networking terms. Several of the source materials in the **box** contain glossaries, but a full-fledged dictionary wouldn't hurt. LANs are closely related to telecommunications, and the network field has picked up the telephone industry's penchant for technobabble. Many networking acronyms have other acronyms nested within them. Often, the second acronym is built on yet a third one. (An example is 10Base-T—which stands for 10-MHz, baseband-signaling, twisted-pair technology—a network-wiring scheme that forms a part of IEEE standard 802.3. IEEE-802.3 governs a network architecture that began life as Ethernet and is still commonly known by that name. The standard is just one in a family, collectively called IEEE-802.x, whose members cover a variety of LAN technologies.)

Networking glossaries worthy of the name are longer than this article; one that I found useful is in Derfler's guide. Actually, much of his book is equally useful. Chances

are, before you're done you'll want to acquire additional texts, but if you have no LAN experience and you can afford only one book on networking, this guide should be it.

While fortifying yourself with some healthy LAN reading, you may find yourself mulling over some of the considerations that follow.

One common reason for wanting a network is to be able to share expensive hardware that no one computer user uses very heavily. A good example of an item you might want to share is a laser printer. If four or five people in a work group each use a printer for an average of a few minutes a day, together they won't use the printer more than an hour a day. If the cost of connecting the computers of all of the work-group members to a single printer is significantly less than the cost of buying four or five printers, the company saves money. The likelihood of any work-group member having to wait very long for a printout is small. If sharing a printer or some other piece of lightly used equipment (a modem, for example) is all you need to do, you can buy hardware (switchboxes) that will do the job. You might not think of several computers connected to one printer via a switchbox as a network, but such a setup is the most elementary form of a computer network.

A switchbox need not have a rotary or pushbutton switch on its front. If you had to walk over and set the switchbox to receive data from your PC every time you wanted to print, you would be losing a major advantage of printer sharing. Some switchboxes automatically connect to the PC of a user requesting printer services. Other users who try to use the printer at the same time receive a "busy" indication. To avoid this annoyance, some switchboxes incorporate a memory buffer. Then all us-

ers can send data to the switchbox at the same time, and the switchbox will buffer the incoming data and queue it up for printing.

Reaping real benefits

Printer-sharing hardware can give you a few networking benefits—most notably equipment-cost savings and perhaps some associated office-space savings. However, to achieve the major benefits of networking (file sharing is the first one that comes to mind), you must choose a more ambitious arrangement; in other words, a *real* network.

For small networks, an approach that has considerable appeal is “peer-to-peer” resource sharing. The majority of networks—including

Unix-based networks—don’t provide peer-to-peer capabilities. Most networks (that is, those without peer-to-peer resource sharing) designate the computers either as “clients” or “servers.” A client is usually a PC or workstation at which an individual work-group member works. A server is a computer whose resources (printers, mass-storage devices, data files, certain program files) are available to all of the work-group members. Servers are often more powerful than the work-group members’ computers. Without peer-to-peer resource sharing, the computer resources of an individual work-group member are available only to that member.

With peer-to-peer resource sharing, all of the networked computers perform both client and server functions. The situation sounds ideal until you consider the drawbacks. A significant drawback of MS-DOS-based peer-to-peer networks is the amount of memory the networking software uses. With DOS’s ability to directly address only 640 kbytes, the amount of memory available for running client applications can be so limited that the individual PCs become all but useless. Using extended or expanded memory for portions of the network software and portions of client applications can alleviate these memory problems. Nevertheless, you don’t need a great deal of imagination to envision soft-

LANs: Read all about ’em

If you know little or nothing about LANs and you have to set up a network, you have two choices: do a lot of reading or hire a good consultant and rely on his or her expertise. But to blindly accept a consultant’s recommendations is to court disaster, so what you really need is to do a lot of reading, or hire a good consultant *and* do a lot of reading. The following are some useful books and magazine articles. The main text of this article discusses a few of the references in greater detail.

1. Apple Computer Inc, *Apple Multivendor Network Solutions Guide*, Cupertino, CA, 1990, 274 pgs. (Includes product directory).
2. Cohen, A M, *A Guide to Networking*, Boyd & Fraser Publishing Co, Boston, MA, 1991, 101 pgs.
3. Comer, D E, *Internetworking with TCP/IP, Second Edition; Volume I: Principals, Protocols, and Architectures*, Prentice-Hall Inc, Englewood Cliffs, NJ, 1991, 547 pgs.
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ware-compatibility issues rearing their heads at nearly every turn.

Another approach sometimes used in small networks is to make only one computer both a client and a server. With PCs based on 80386 and i486 CPUs, you can create additional "virtual" 8086-based machines. Virtual machines behave as if they consist of dedicated hardware, whereas in fact, a virtual machine borrows all of its hardware resources from another computer. If you create a virtual machine, it can act as a client while the real machine performs as the server. The two machines can coexist happily—until a client application crashes. Even then, the server will continue working, blissfully unaware of the misfortune that has befallen its virtual-machine client. But to get the client application running again, you must reboot the virtual machine. Whether you like it or not, doing so means bringing down the real machine—in this case, the server. The effects on all of the other clients are potentially disastrous.

Such problems often dictate dedicating a computer as a server. Most networks have dedicated servers. Probably the most important attribute of a server is a fast hard-disk drive with greater capacity than you can imagine ever needing. Though an effective technique on client computers, using a disk cache to improve the access time of a hard disk may not prove very helpful on a server. A group of clients can ask a server to access many widely dispersed files in rapid succession. Caches determine what information they should store by analyzing which files the CPU has recently accessed. In a server, the likelihood is lower than in a client computer that a disk cache will contain information the CPU needs. Therefore, you should be sure the server's hard drive has fast access even without

To guide you through the black forest of connectivity, the ISO/OSI model organizes network hardware and software into seven conceptual "layers."

improvements achieved through disk caching.

You might think that other factors—for example the speed at which messages travel around a network—would have a profound effect on the speed with which clients can access information. To be sure, network speed is affected by many factors. However, several authors report that tests show that with today's technology, no factor is as important as the server's hard-disk access speed. So when selecting a server, pick one with the fastest, highest capacity hard disk you can afford.

Many other considerations

Despite the importance of disk access speed, no discussion of LANs should neglect transmission media, physical topologies, logical topologies, and media-access protocols. When you start to deal with these topics, you begin to appreciate just how large and complex a field networking is.

The routes that the LAN signals travel within a building (the network's physical topology) don't necessarily bear any relationship to the way the computers that make up the LAN perceive the connection scheme (the network's logical topology). Physically, a network can be a daisy chain (a bus) or a star. Logically, the network can be a star, a ring, or a bus. But a network that is physically a star can, for example, behave as if it were a ring. Moreover, all other permutations of

physical and logical topologies are possible. In general, a physical star will be more reliable than a daisy chain, but the reliability has a price. Despite being easier to install, the physical star costs more than the daisy chain—it uses more cable and requires wiring-hub hardware at its center.

Examples of LAN architectures are Ethernet, Appletalk, Token Ring, and Arcnet (in which ARC is short for attached-resource computing). Although some network architectures are associated with particular physical topologies, when you choose an architecture, you often still have a choice of physical topology. On the other hand, choosing an architecture determines a network's logical topology.

Similarly, some architectures tie you to a particular transmission medium, whereas others permit choosing among media. Examples of media are fiber-optic cable, coaxial cable, shielded twisted-pair cable, and unshielded twisted-pair cable. None of these descriptions is adequately detailed, however, because each medium has characteristics that depend strongly on its physical properties. Therefore, a specification for coaxial cable might call for type RG-58/AU.

Actually, the situation is a bit more complicated than the previous paragraph implies. For example, the term Ethernet is often changed or modified to tell you something about the medium. "Thick-wire" Ethernet refers to the original Ethernet implementation, which used thick, semi-rigid coaxial cable (a medium known in the trade as "frozen, yellow garden hose"). "Thin-wire" Ethernet (sometimes called "Cheapernet") uses much thinner, flexible coaxial cable. The thinner medium is not only less expensive than the thick cable, it is easier to work with. However, using it reduces the maximum permissible

length of the LAN cabling and necessitates placing the network's nodes (the points where you connect computers) closer together. The term 10Base-T Ethernet describes an implementation that uses unshielded twisted-pair cable—similar to that used for telephone wiring. Such cable is less expensive and easier to work with than the thin coax, but using it places still greater restrictions on wiring length.

Mixing and matching technologies

Sometimes, a network-architecture specification will let you combine networks having different architectures. For example, through a protocol named Ethertalk, Apple Computer has extended its Appletalk standard to let Appletalk networks take advantage of many attributes of the IEEE-802.3 Ethernet standard. Originally, Appletalk used an unshielded, twisted-pair wiring scheme now called Localtalk. Localtalk, which is still being installed, is an economical medium well suited to small networks. It is limited in speed, however, having a data rate (signaling rate) of 230 kbits/sec. Ethernet, now including twisted-pair implementations, supports a data rate of 10 Mbits/sec. Ethertalk also allows Appletalk networks to incorporate many more nodes than does Localtalk.

You should not confuse running Appletalk over Ethernet with the interconnection of networks. One of the hottest subjects in networking at the moment is "internetworking"—tying networks together; for example, connecting a network in a design department to one in a test-engineering department. Internetworking schemes use hardware systems called bridges, routers, and gateways.

A common misconception about LANs is that using fiber-optic cable will greatly increase a network's

speed. Certainly, optical cable can handle much greater signal bandwidths than copper cable can. Nevertheless, in LANs as they exist today, the bandwidth of high-quality coaxial cable isn't what limits data rates. At present, LANs can achieve the same data rates with carefully chosen coax as with optical cable. Therefore other considerations should determine which medium you select. Paramount among these is cost—both the initial cost of the hardware and the installation cost. Other factors include the cable's diameter and flexibility (which affect its ease of installation), the maximum allowable cable length,

LANs use radio-frequency (RF) or infrared signals as the transmission medium. Several RF schemes use spread-spectrum techniques in which the signals are disbursed over a wide frequency spectrum to improve both data security and the rejection of interference. Proponents of wireless LANs insist that the networks address two major costs of copper-wire (coaxial or twisted-pair) and fiber-optic-cable LANs: the cost of the cable and the cost of installing it. Although that claim is true, wireless-LAN hardware costs sufficiently more than cabled-LAN hardware to make informed consultants suggest that



Proprietary networks can benefit specific applications that industry-standard networks often can't. Omron Electronics Inc.'s (Schaumburg, IL) Sysmac Net is a high-speed, fiber-optic token-ring LAN for industrial applications that require high noise immunity. The vendor claims that its plastic-fiber cable is easier to work with than glass-fiber cable. Systems cost approximately \$4000/node.

the network's required degree of immunity to electrical interference (including lightning), the need for keeping the network secure from electronic eavesdropping, and the difficulty of adding nodes to an existing cable run.

A technology that is just emerging is the wireless LAN. Wireless

you need some reason besides cost for choosing a wireless LAN. One such reason is that with some wireless LANs, you can walk around your office using a notebook PC, all the while remaining connected to the network—the computer equivalent of using a cordless telephone.

A LAN architecture implies a

method of controlling nodes' access to the transmission medium. By definition, networking involves sharing the medium. With sharing comes the likelihood that several nodes will try to talk at once so that nobody can hear. There are several radically different access-control schemes (protocols). The three most important are carrier-sense, multiple-access with collision detection (CSMA/CD), used by Ethernet and defined by IEEE-802.3; token passing, used on IBM token-ring networks and defined by IEEE-802.5; and the scheme, apparently known only as the Arcnet scheme, used by

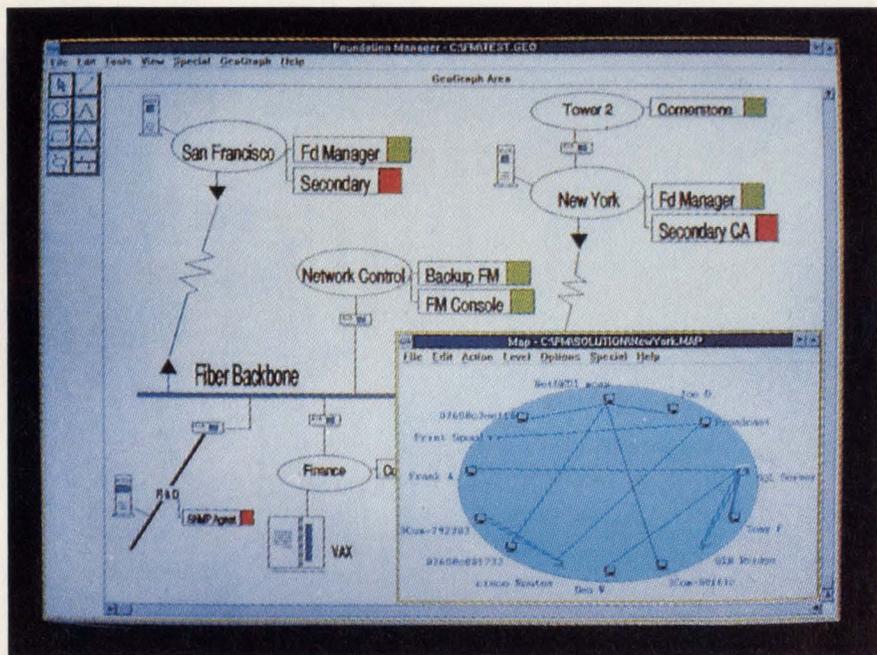
You have to walk a fine line between jumping to conclusions about the products you must have and being swayed by every input you receive.

mit at the same time, they will sense the "collision" and stop. Before trying again, each node will wait for a brief interval whose duration is randomly selected. The node whose random delay happens to be

The Arcnet protocol is in many ways less sophisticated than the other two. Each Arcnet adapter has a set of switches that you must program with a node number from 1 to 255. (Token-ring and Ethernet adapters require no such address-switch programming.) The lowest numbered node becomes the network controller. It polls all of the nodes for messages. A node that has no message remains silent. Nodes that have messages are granted use of the network for a limited time. Adding a node (for example by applying power to a computer that had been shut down), initiates a reconfiguration process that takes at most 65 msec. Thanks to the address switches, Arcnet adapters are relatively simple—a real advantage, but the scheme imposes a burden on the network manager. When network problems arise, he or she must know which address corresponds to which node. Woe betide the manager who loses (or fails to maintain) a record of the numbers assigned to an Arcnet LAN's nodes.

Although the topologies and protocols may be similar, typical applications of networks in electronic engineering departments are not entirely representative of LAN applications in business. There is probably more similarity between the uses of LANs on college campuses and in electronic-engineering departments in industry than there is with typical LAN applications in manufacturing, commerce, and finance. Design-engineering departments and universities have a significant lead over most nontechnical users in storing and manipulating graphical information. Despite the growing popularity of graphical user interfaces, computers outside engineering departments and universities still deal overwhelmingly with text.

The emphasis on graphics in engi-



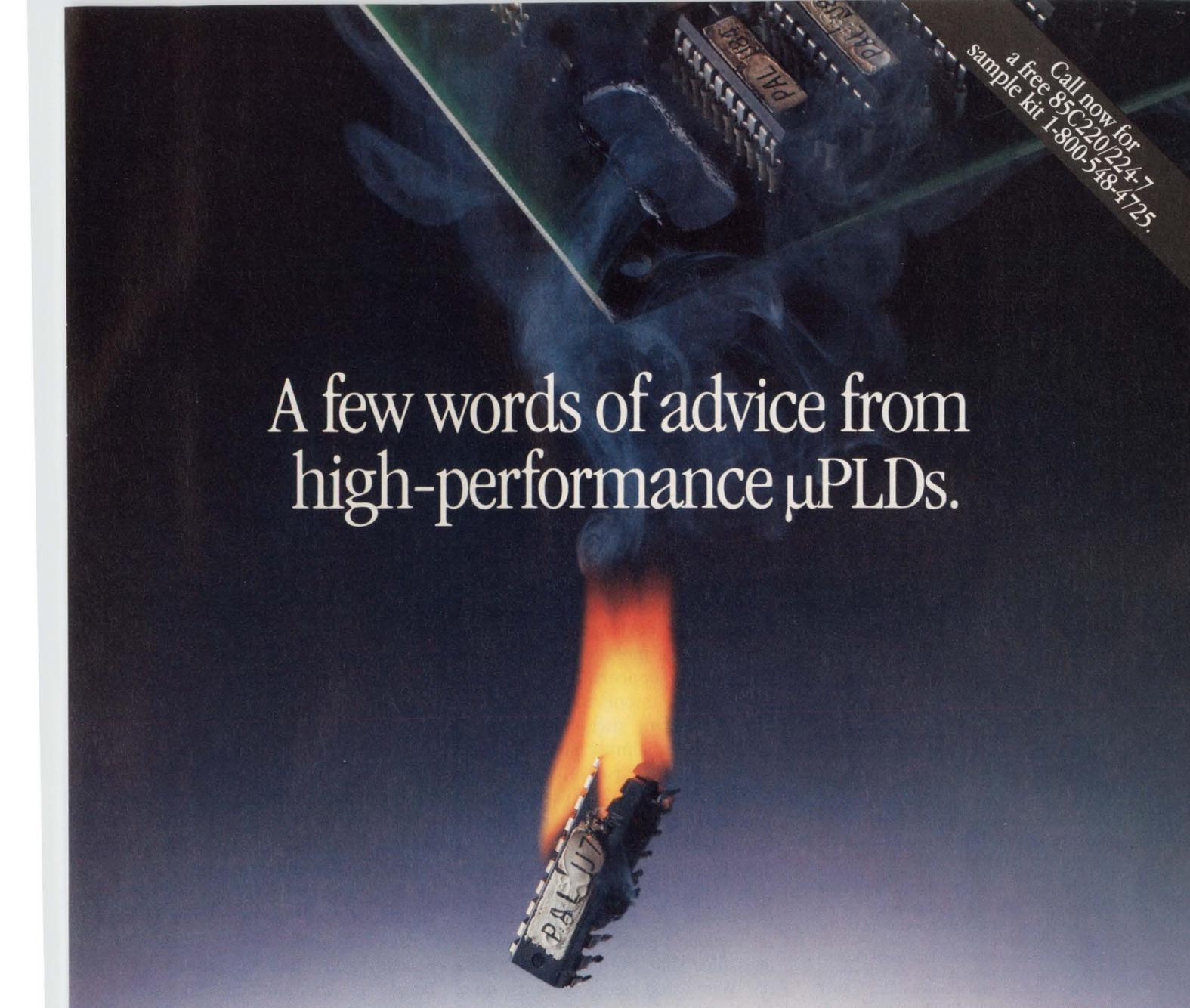
Managing a large network can be a full-time activity. As you might expect, you need specialized software tools for the job. Protools (Beaverton, OR) provides several network-management packages, including Foundation Manager for enterprise-wide networks (\$8995) and Cornerstone Agent (\$1295) for local nets. Among their functions, the packages assist you in visualizing network activity.

(you guessed it) Arcnet. Arcnet is a widely supported de facto industry standard. At present, there is no IEEE standard governing Arcnet.

Under CSMA/CD, a node that wants to transmit listens for network activity to stop. Then it transmits. If several nodes try to trans-

mit at the same time, they will sense the "collision" and stop. Before trying again, each node will wait for a brief interval whose duration is randomly selected. The node whose random delay happens to be

the shortest will be the first of the colliding nodes to gain access. Once a node gains access, it must fall silent after a specified interval. In token passing, a special message (a token) circulates among the nodes. The node that has the token gets access to the network—if it needs access—for a limited period.

A hand in a blue nitrile glove holds a PAL chip that is on fire. The fire is bright orange and yellow, with a thick trail of smoke rising from the chip. In the background, other PAL chips are visible on a green printed circuit board. The overall scene is set against a dark, smoky background.

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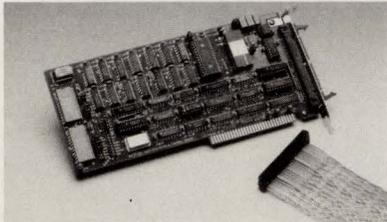
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COMPUTERS AND PERIPHERALS

neering means that your LAN requirements, though almost certainly not unique, probably aren't run-of-the-mill. Confucius understated the real facts when he said that a picture is worth a thousand words. Without the use of data compression, high-resolution images (especially color images) require megabytes to store and transmit. A screen filled with text encoded in ASCII (American-Standard Code for Information Interchange) represents a mere two kilobytes. The high data content of images can tax networks designed for text.

Despite the differences between engineering LAN applications and many others, most of the areas that customarily concern LAN specialists are also important in engineering LANs. One such area is shared databases or simply shared access to files. A major reason for wanting a LAN is to free yourself from at least part of the nightmare of keeping track of multiple versions of data files. Consider this very simple case: Fred and Joe have a 2-man office—an office without a network. At various times, each of them creates files that the other one works on. When Joe needs to work on a file that Fred created, he asks Fred to copy it from his hard drive onto a floppy disk. Joe then loads the file onto his hard drive. Now there are three copies of the file. If Fred and Joe each work on their own copies, they will soon find it difficult, if not impossible, to figure out whose copy is the "correct" one.

With a LAN, only one copy of the file need exist—on the server's hard drive. There are still complex issues involved when both Fred and Joe attempt to update the file simultaneously. However, network operating system-software and application-software packages designed to run on networks incorporate mechanisms for dealing with prob-

lems of this type. By installing a LAN, Fred and Joe can, in effect, delegate their file-revision-control problem to the authors of the software they use. When they select particular packages, they are opting for certain ways of making the tradeoffs. Chances are, though, that they won't have to give the tradeoffs another thought.

There are many reasons for the huge popularity of networking; you can almost guarantee that your list of reasons for setting up a departmental, facility-wide, or company-wide network aren't unique. Moreover, once you have a network, you will discover ways to benefit from it that you hadn't thought of originally. That networks drastically and permanently alter the way people do their jobs is no exaggeration. The effects of adopting networking are nearly as profound as those of adopting computers. Because of this great potential and great effect on people, you should take setting up a network very seriously; doing your homework will pay big dividends. If reading this article is the first research you've done on LANs, you have not really even scratched the surface. The references listed in the box will take you much further. **EDN**

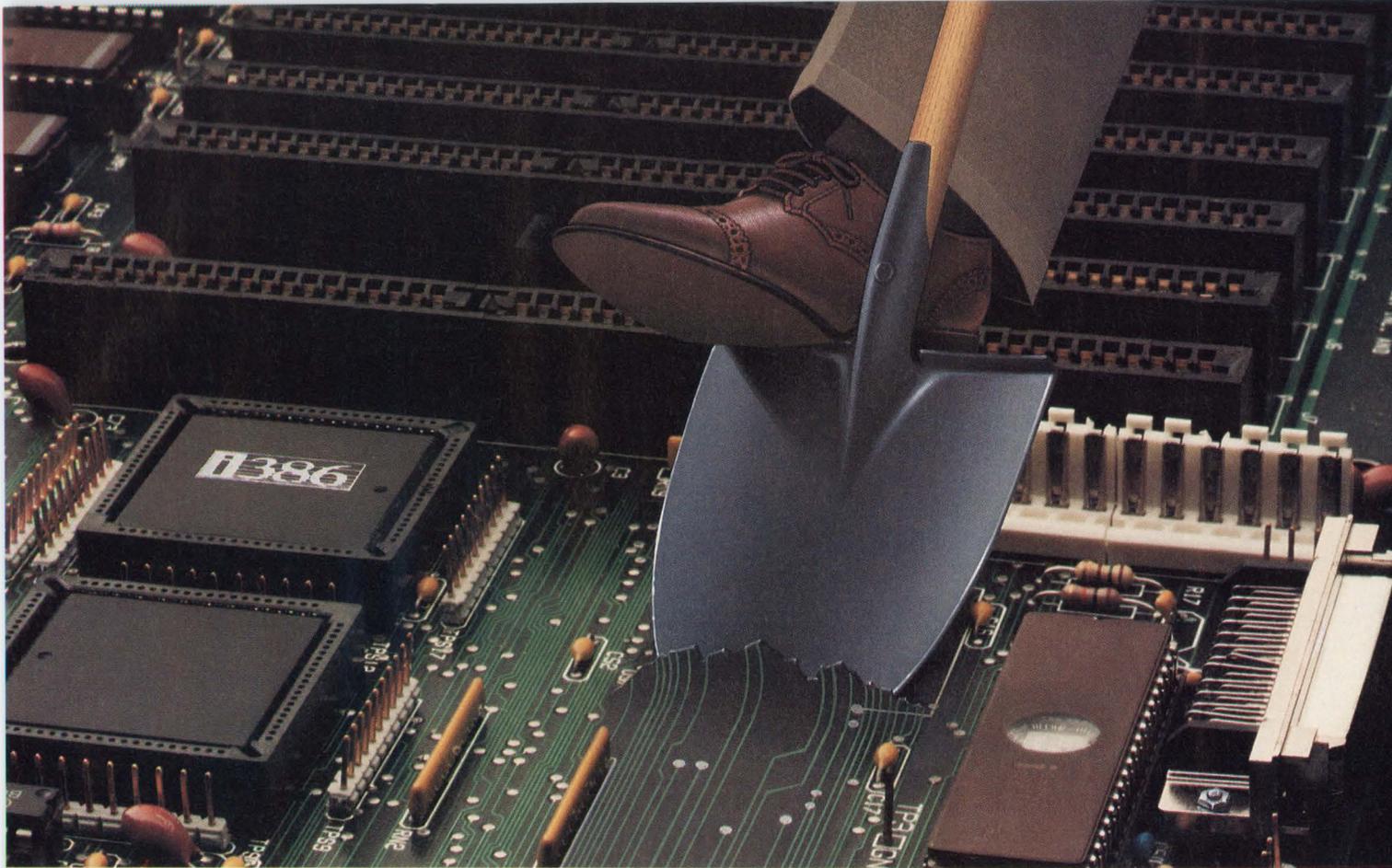
Acknowledgments

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Joseph Biagiotti and Leonard Pienta III of Compu-tame Inc, Box 1826, Wakefield, MA 01880 familiarized me with their personal experiences in setting up a LAN in a small company.

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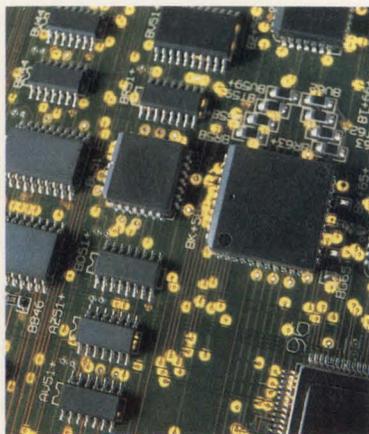


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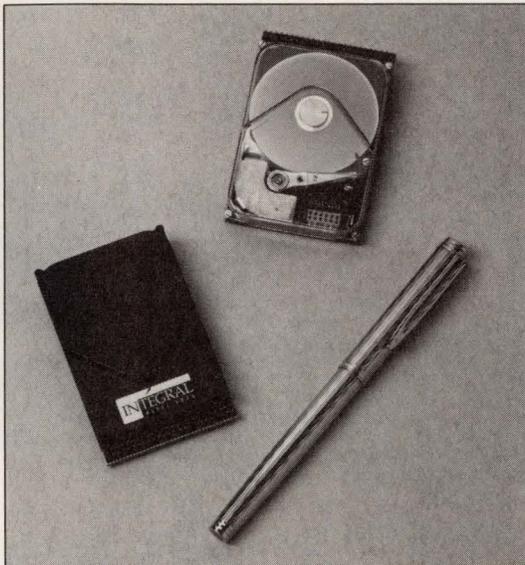
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While in the idle mode, the drive keeps the platter spinning in case another data-transfer request appears. If no requests are made during the 5-sec idle time, the drive drops into its 35-mW standby mode.



After another 5 sec of inactivity, the drive goes into its 15-mW sleep mode.

The controller circuitry includes a 32-kbyte data buffer and an IDE (integrated device electronics) disk interface that transfers data in bursts at 4 Mbytes/sec. The aver-

age seek time is 20 msec. The disk drive costs \$485.

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Viewsonic, 12130 Mora Dr, Santa Fe Springs, CA 90670. Phone (800) 888-8583; (213) 946-0711. FAX (213) 946-1618.

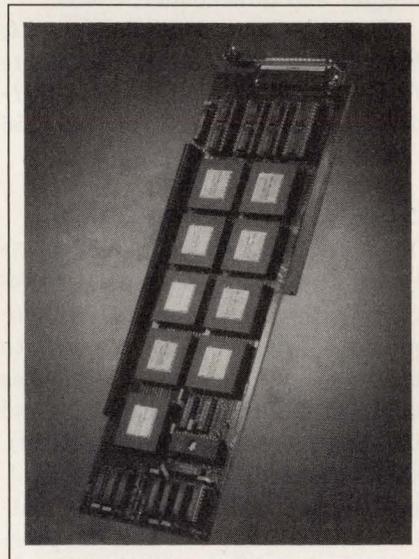
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Configurable-Hardware Computer

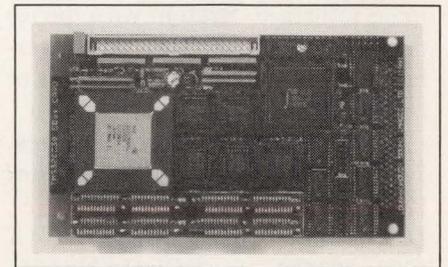
The CHS2 × 4 custom computer operates by configuring hardware to a computational task. A 16-bit ISA-bus plug-in card houses the computer, and data flows via the PC bus or a rear-panel I/O connector. The board contains a 2 × 4 array of the company's CAL1024 32 × 32 cell and CMOS field-programmable gate array (FPGA). Using on-chip static RAM (SRAM), you can program each cell of the FPGA to behave as any function of two Boolean variables, or as a D-type latch with a 100-MHz toggle rate. You can pro-

gram one 32 × 32 array in 70 μ sec. The computer also contains 2 Mbytes of SRAM for local data storage in pipelined computations. A suite of software tools includes a symbolic editor for design work, an assembler and loader for array programming, and a C library for support functions, including dynamic reconfiguration. Depending on configuration, board and software, from \$5000 to \$10,000.

Algotronix, Kings Bldgs-TTC, Mayfield Rd, Edinburgh EH9 3JL, UK. Phone (31) 668-1550. FAX (31) 662-4678. Circle No. 353

Sbus DSP Board

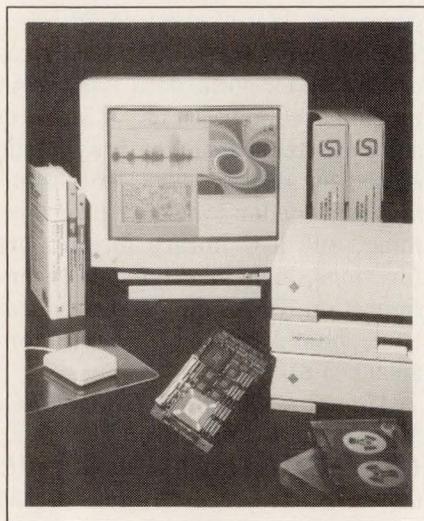
The Sbus board is a DSP development board for the Sbus in Sun SPARCstations. The board uses TI's 33-MHz TMS320C30 DSP chip and 128k × 32 bits of zero-wait-state RAM. You can expand the RAM to 512k × 32 bits. You can also add a daughter card, which has dual 16-bit ADCs and DACs. Daughter cards containing either a 200-kHz I/O module or a delta-sigma I/O module are also available. The board contains the company's 16-bit DSP-Link expansion bus for high-speed communication with other Sbus boards. Operating as an Sbus slave, the board has a 2k × 32-bit dual-port static RAM for communicating with the SPARCstation. \$4595. Board with TI's assembler



and linker, TI's C compiler, and SPOX operating system, \$9595.

Spectrum Signal Processing Inc, Suite 301, 3700 Gilmore Way, Burnaby, BC V5G 4M1, Canada. Phone (604) 438-7266. FAX (604) 438-3046. Circle No. 354

Computers and Peripherals



DSP System For Sbus Workstations

The SDSP/C30D DSP system on a card suits Sbus-compatible workstations. The system hardware consists of a Texas Instruments 33-MHz TMS320C30 processor, 2k × 32-bit-word dual-port static RAM (SRAM), and 128k × 32-bit-word zero-wait-state SRAM (expandable to 512k). The base card accepts plug-in analog-signal I/O daughter boards, and the combination fits an Sbus single-slot space. Options exist for either a proprietary 16-bit parallel I/O port or a SCSI port. Software support includes an interface library of control functions and a device driver. Other software tools include a debug monitor, C compiler, and Spectron Microsystems Spox applications programming interface. System with device driver, debug monitor, and interface library, £2695; analog daughter board, £600.

Loughborough Sound Images, The Technology Centre, Epinal Way, Loughborough LE11 0QE, UK. Phone (509) 231843. FAX (509) 262433. Circle No. 355

STD-32 DSP Board

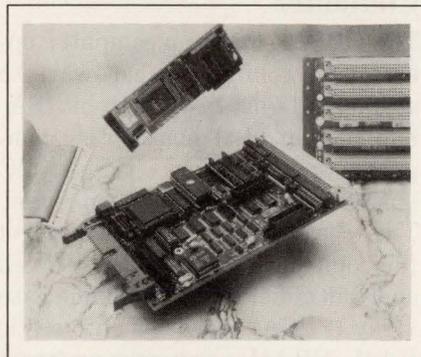
The ZT 89CT30 DSP board conforms to the STD-32 specification. The board contains a 27-MHz 56001 DSP chip, which executes 24-bit in-

teger arithmetic. The board also contains two synchronous serial channels, a 24-bit Opto-22 interface, a watchdog timer, 2 kbytes of EEPROM; and a configurable DIP switch that lets the board control a variety of I/O operations. As an I/O controller, the board communicates with the STD system's master via dual-port I/O registers and a priority interrupt controller. Motorola's C compiler and simulator are available for program development. An optional debugger and downloader is also available. The all-CMOS design operates from -40 to +85°C. \$1050. Development kit, which includes the board, 12k × 24 bits of RAM, and the debugger and downloader, \$1450.

Ziatech Corp, 3433 Roberto Ct, San Luis Obispo, CA 93401. Phone (805) 541-0488. FAX (805) 541-5088. Circle No. 356

STEBus Processor Board

The SCIM88 STEbus processor board combines a 16-MHz 80188 CPU with a user-defined 1-Mbyte memory array. You can populate the memory array with 0.5 Mbytes of EPROM or flash EPROM and 0.5 Mbytes of static RAM (SRAM). Of the SRAM, 16 kbytes are dual-ported, and 256 kbytes can be battery-backed. You can link the processor board to the company's range of remote signal-conditioning mod-



ules via a front-panel ribbon connector. You can expand the function of the processor board with plug-in options, which include a VGA

graphics controller, PC-communications ports, analog and digital I/O, and a prototyping module. Software options include DR-DOS and Sourceview, which is a source-level remote debugger for developing DOS-compatible target programs. SCIM88 without memory, £300.

Arcom Control Systems, Units 8-10 Clifton Rd, Cambridge CB1 4WH, UK. Phone (223) 411200. FAX (223) 410457. Circle No. 357

Sbus Graphics Board

The GXTRA 1280 single-slot graphics card works with the Sbus in Sun SPARCstations. It drives 1280 × 1024-pixel displays and has a Sun-4 keyboard and mouse port. The board contains an 8-bit color frame buffer, and it runs on Sun's Open Windows 2.0 software. Windows executes partially on the board and partially on the host CPU. You can install multiple Sbus boards to service additional users on a single SPARCstation. The board uses a proprietary gate array, which accelerates low-level graphics primitives such as drawing 2-D vectors, solid fills, and characters. \$2250.

Tech-Source Inc, 442 S North Lake Blvd, Suite 1008, Altamonte Springs, FL 32701. Phone (407) 830-8301. FAX (407) 339-2554. Circle No. 358

PCXI Computers

The PX1010 and PX1012 are 19-in. rack-mount and 17-in. desktop industrial computers, respectively. The computers conform to the PC Extended for Industry standard (PCXI) for modular industrial PCs. They feature passive back-planes, PCXI-specified cooling systems, and EMI/RFI metal-shielded modules. The cooling system consists of two 72-cfm positive pressure fans that have washable polyurethane foam filters. The modules accept PC-instrumentation function cards from any manufacturer, and you can

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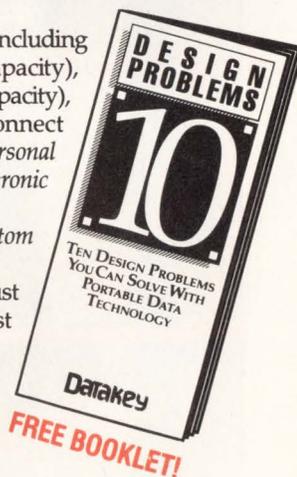
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Computers and Peripherals

order custom connectors. The modules also feature front-panel access. The backplane has 12 16-bit ISA bus slots and an additional slot for a power-supply module. A base system comes with a 200W switching power supply. \$1595.

Rapid Systems, 433 N 34th St, Seattle, WA 98103. Phone (206) 547-8311. FAX (206) 548-0322.

Circle No. 359

VMEbus Single-Board Computer

The MVME167 single-board computer for the VMEbus uses a 25-MHz 68040 μ P and from 4 to 32 Mbytes of dynamic RAM. It has a VME D64-compatible interface, letting the board transfer data at 40 Mbytes/sec. All CMOS electronics keep the power consumption at 15 to 18W typ. The 6U board uses ASICs and VLSI controllers that

are optimized for Unix and real-time applications. Additional features include a 32-bit Ethernet controller; a 2-way parallel port; four sockets for as much as 2M bytes of ROM, EPROM, or EEPROM; a 7-level interrupt handler; a 4-level arbiter; four serial I/O ports; 128 kbytes of static RAM; and 8 kbytes of nonvolatile RAM. The board supports VMEexec real-time development software. \$3995.

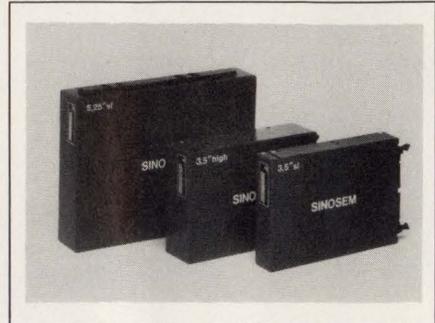
Motorola Inc, Computer Group, 2900 S Diablo Way, Tempe, AZ 85282. Phone (800) 624-8999, ext 230; (602) 438-3576.

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40-Mbyte capacity. Typical data retention time is five years. You can expand memory size in 1-Mbyte steps for the 10-Mbyte model, and in 2-Mbyte steps for other models. Minimum data-transfer rate is 4



Mbytes/sec. The 40-Mbyte version is 160 \times 41.5 \times 48 mm. 10-Mbyte version, DM 4870; 20-Mbyte version, DM 7914.

Atron Electronic, Am Zeigelstaedel 14, W-8015 Markt Swaben, Germany. Phone (81) 21-5071. FAX (81) 21-40333. Circle No. 361

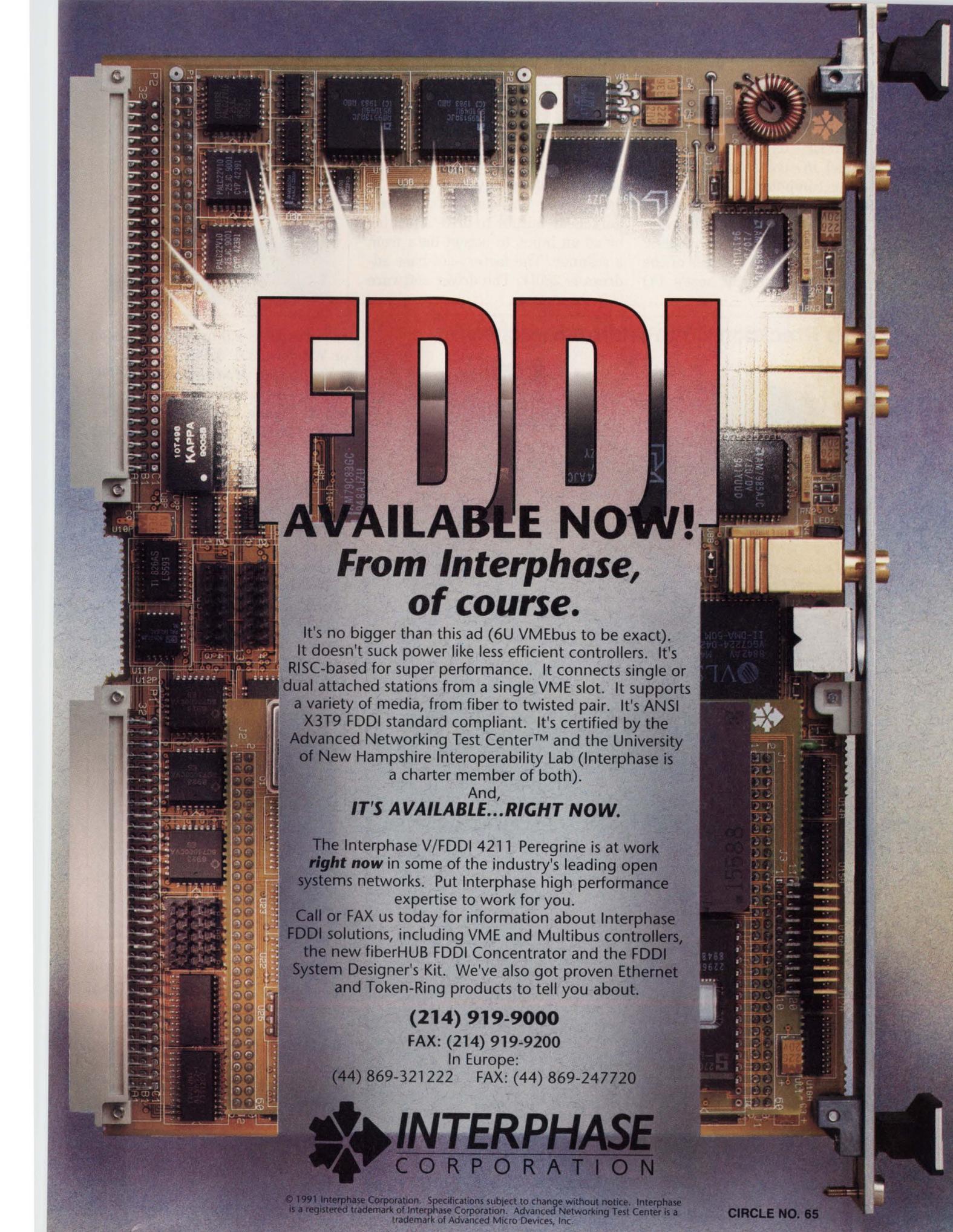


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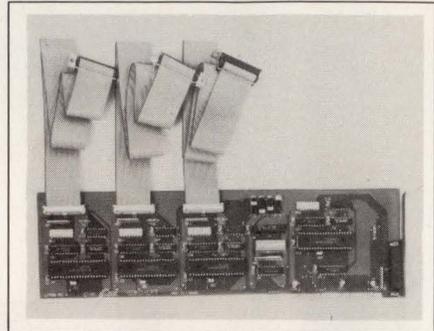
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Computers and Peripherals

Parallel-Port Expander

The Quad LPT expands the number of parallel I/O ports on an ISA- or EISA-bus computer. The expansion board adds four additional ports to the one or two ports generally available in DOS-compatible computers. You can set the base address of the board anywhere in the host's I/O

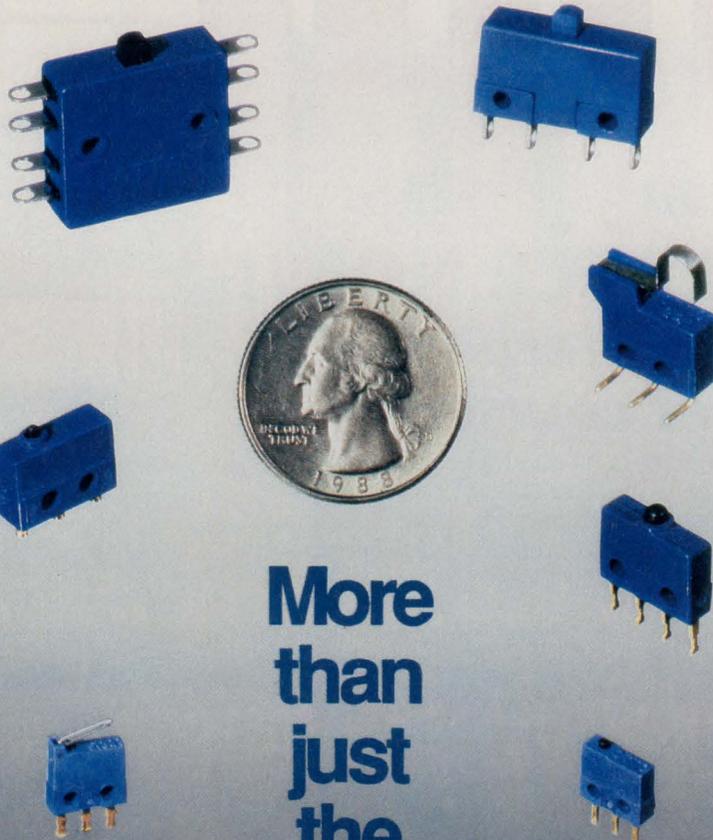
space using a DIP switch. The host sequentially accesses each port starting with Port 0 at the selected base address, followed by Port 1, Port 2, and Port 3. You can configure any port as an output to drive a printer or as an input to accept data from a scanner. The factory-set base address is 280H. The driver software



requires DOS 2.0 or higher version or Windows 3.0. \$295.

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The Microdyn II is a voice I/O system that provides voice recognition of 1000 isolated words or phrases. The system provides unlimited text-to-speech synthesis. The system consists of an external module that plugs into the serial port of an MS-DOS- or OS/2-compatible computer, a headset and microphone, software, and documentation. Because the module plugs into a standard RS-232C port, the system does



not occupy an expansion slot. The system requires 5 kbytes of RAM and runs with any monitor. To train the system, you establish a range of voice patterns for a spoken command, which the computer stores as voice macros. \$1995.

Voice Dynamics Corp, 17835 Skypark Circle, Suite C, Irvine, CA 92714. Phone (714) 252-1211.

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Quick Charge Battery Charger

One half of the LTC1155 Dual MOSFET Driver controls the charging of the battery pack. The 9V, 2A current limited wall unit is switched directly into the battery pack through an extremely low resistance MOSFET switch, Q2. The gate drive output, Pin 2, generates about 13V of gate drive to fully enhance Q1 and Q2. The voltage drop across Q2 is only 0.17V at 2A and, therefore, can be surface mounted to save board space.

An inexpensive thermistor, RT1, measures the battery temperature and latches the LTC1155 OFF when the temperature rises to 40°C by pulling low on pin 1, the Drain Sense Input. The window comparator also ensures that battery packs which are very cold (<10°C) are not quick charged.

Q1 drives an indicator lamp during quick charge to let the computer operator know that the battery pack is being charged properly. When the battery temperature rises to 40°C, the LTC1155 latches OFF and the battery charge current flowing through R9 drops to 150mA.

Extremely Low Voltage Drop Regulator

A four-cell Ni-Cad battery pack produces about 6V when fully charged. This voltage will drop to about 4.5V when the batteries are nearly discharged. The second half of the LTC1155 provides gate voltage drive, pin 7, for an extremely low voltage drop MOSFET regulator. The LT1431 controls the gate of Q4 and provides a regulated 5V output when the battery is above 5V. When the battery voltage drops below 5V, Q4 acts as a low resistance switch between the battery and the regulator output.

A second power MOSFET, Q3, connected between the 9V supply and the regulator output "bypasses" the main regulator when the 9V supply is connected. This means that the computer power is taken directly from the AC line while the charger wall unit is connected. The LT1431 provides regulation for both Q3 and Q4 and maintains a constant 5V at the regulator output. The diode string made up of diodes D2-D4 ensure that Q3 conducts all

the regulator current when the wall unit is plugged in by separating the two gate voltages by about 2V.

R14 acts as a current sense for the regulator. The regulator latches OFF at 3A when the voltage drop between the second Drain Sense Input, pin 8, and the supply, pin 6, rises above 100mV. R10 and C3 provide a short delay. The μ P can restart the regulator by turning the second input, pin 5, OFF and then back ON.

The regulator is switched OFF by the μ P when the battery voltage drops below 4.6V. The standby current for the 5V, 2A regulator is less than 10 μ A. The regulator is switched ON again when the battery voltage rises during charging.

Very Low Power Dissipation

The power dissipation in the notebook computer is very low. The current limited wall unit dissipates the bulk of the power created by quick charging the battery pack. Q2 dissipates less than 0.5W. R9 dissipates about 0.7W. Q4 dissipates about 2W for a very short period of time when the batteries are fully charged and dissipates less than 0.5W as soon as the battery voltage drops to 5V. The three integrated circuits shown are micropower and dissipate virtually no power.

Cost Effective and Efficient Power System

The circuit shown in Figure 1 consumes very little board space. The LTC1155 is available in a 8-pin SO package and the three power MOSFETs can also be housed in SO packaging. Q4 must be heatsinked properly for the short period of time that the battery voltage is above 5.5V. (Consult the MOSFET manufacturer data sheet for SO heatsink recommendations).

The LTC1155 allows the use of inexpensive N-channel MOSFET switches to directly connect power from a 4-cell Ni-Cad battery pack to the charger and the load. This technique is very cost effective and is also very efficient. Nearly all the battery power is delivered directly to the load to ensure maximum operating time from the batteries.

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DESIGN IDEAS

EDITED BY CHARLES H SMALL & ANNE WATSON SWAGER

Circuit adjusts duty cycle, not frequency

Yongping Xia

Dept of Electrical and Computer Engineering,
West Virginia University, Morgantown, WV

The output of Fig 1's circuit has an adjustable duty cycle that, once set, is constant for inputs that range in frequency from 30 Hz to 1 kHz. The leading edge of the input signal generates a 3- μ sec pulse at point A. This pulse closes IC_{3A} and causes the voltage on C₄ to equal the output of IC_{2B}. The 3- μ sec pulse also generates a narrower 1.5- μ sec pulse at point B through C₂, R₂, IC_{1C}. This pulse discharges the integrator after its peak output is stored in the hold capacitor C₄. The integrator is composed of IC_{2B}, R₃, and C₃ and has the following ramping rate:

$$\text{Rate} = 5V / (R_3 \times C_3) = 0.106V/\text{msec.}$$

Thus, if the input frequency is 100 Hz, the peak output of the integrator will be 1.06V.

IC_{2C} buffers and R₄ divides C₄'s peak signal after

which it serves as a reference for voltage comparator IC_{2A}. The other comparator input is the output of the integrator at point C. When the signal at point C is lower than the reference, IC_{2A}'s output will be negative. Otherwise, its output will be positive. Since point C is a linear ramp signal and the reference is the peak of that signal, IC_{2A}'s output duty cycle will only depend on the divide ratio of R₄. Thus, you can adjust the duty cycle by adjusting R₄. The errors of R₃ and C₃ will not alter the output duty cycle.

The output of IC_{2A} is between $\pm 3.5V$. IC_{1D}, D₁, and R₅ convert this output to a standard TTL signal. With no input signal present, the integrator will reach the highest voltage and the output will stay at zero. Changing the frequency range of the circuit requires changing the values of the hold capacitor and components that make up the integrator and pulse generators.

EDN BBS /DL_SIG #1056

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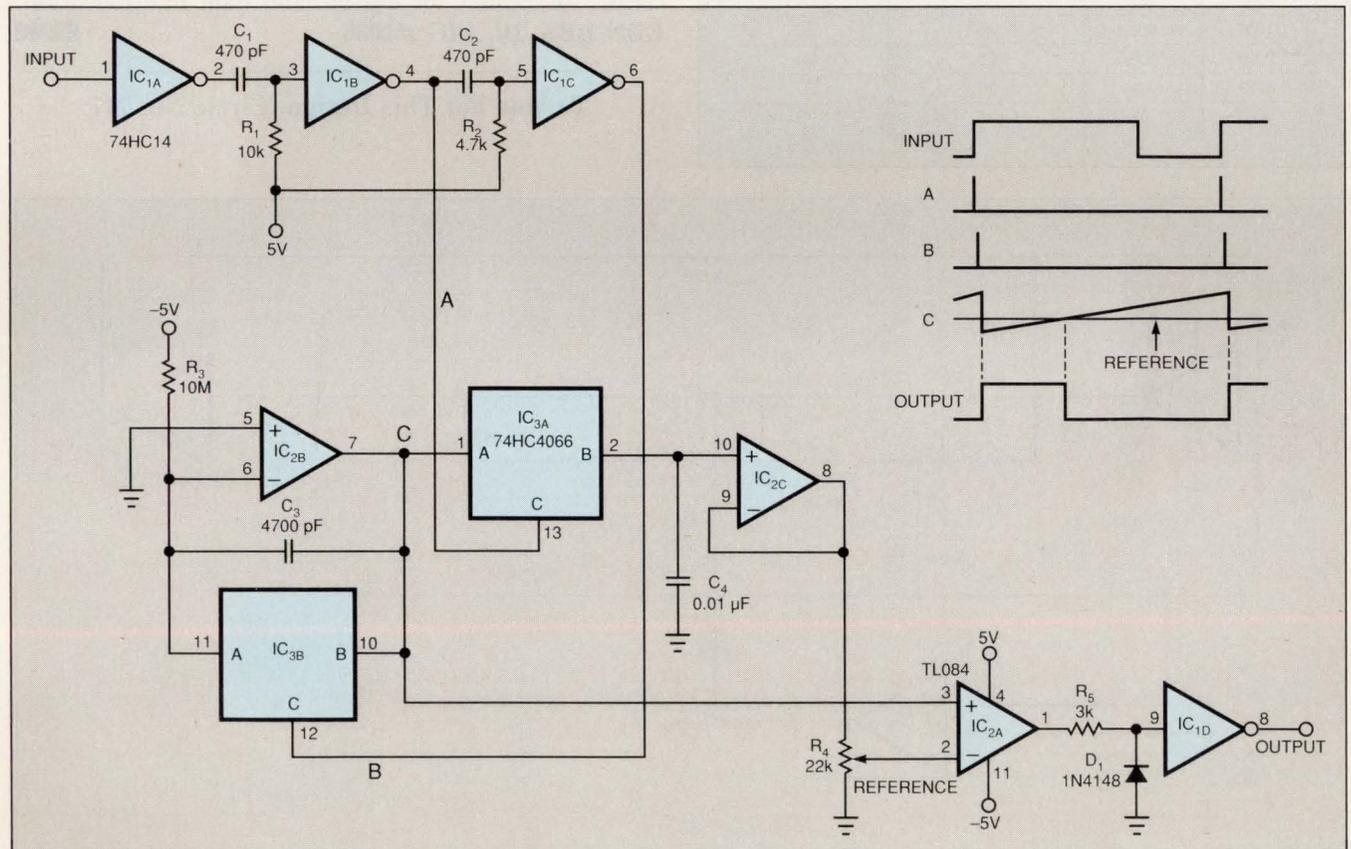


Fig 1—Once you adjust and set R₄, the output duty cycle of this circuit remains constant over a 30 Hz to 1 kHz range.

Filter quashes 60-Hz interference

Adolfo A Garcia
Analog Devices, Santa Clara, CA

The circuit in **Fig 1** filters 60-Hz interference from low-frequency, low-level signals. The filter exhibits 40-dB rejection ($Q=0.75$) and draws 95 μA max from a single-sided 5V supply.

Resistors R_1 , R_2 , and R_3 and capacitors C_1 , C_2 , and C_3 form a classic twin-T section, and IC_1 and IC_2 provide local and global feedback. The frequency selectivity (Q) and the rejection performance of this active filter are very sensitive to the relative matching of the capacitors and resistors in the twin-T section. **Table 1** shows rejection and Q as a function of the value of R_Q .

R_4 , R_5 , C_4 , and IC_3 form a very-low-impedance refer-

ence source to bias IC_1 and the twin-T section to half the supply voltage.

To configure the filter to operate at 60 Hz, choose a Q that will provide enough rejection without excessive loss of desired low-frequency signals that may be close to the filter's notch frequency. The value of R_Q is

$$R_Q = (4Q - 2)R_7.$$

The gain of the output amplifier is simply that of a conventional noninverting amplifier:

$$A = 1 + (R_Q/R_7) = 4Q - 1,$$

and the overall gain of the band-reject filter below and above the notch frequency is

$$V_{\text{OUT}}/V_{\text{IN}} = 2A/(1 + A).$$

If you need additional rejection, cascade filter sections. Keep in mind that you might have to modify the circuit to account for out-of-band gain multiplication. **EDN BBS /DL_SIG #1036**

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Table 1— R_Q rejection at 60 Hz, and the filter's voltage gain as a function of the filter Q

Filter Q	R_Q (k Ω)	Rejection (dB)	$V_{\text{OUT}}/V_{\text{IN}}$
0.75	1.0	40	1.33
1.00	2.0	35	1.50
1.25	3.0	30	1.60
2.50	8.0	25	1.80
5.00	18	20	1.90
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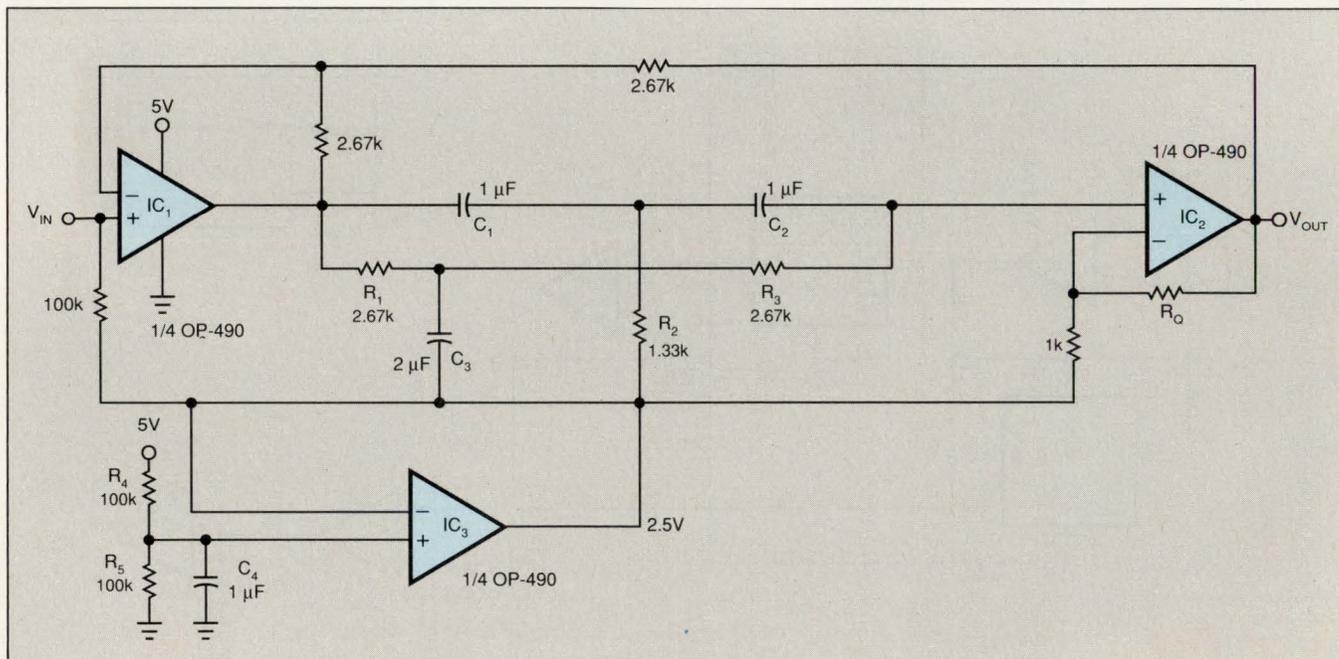


Fig 1—This notch filter suppresses 60-Hz interference in low-frequency signals.

You asked for a connector family that's ideal for both high-density signal and power applications.

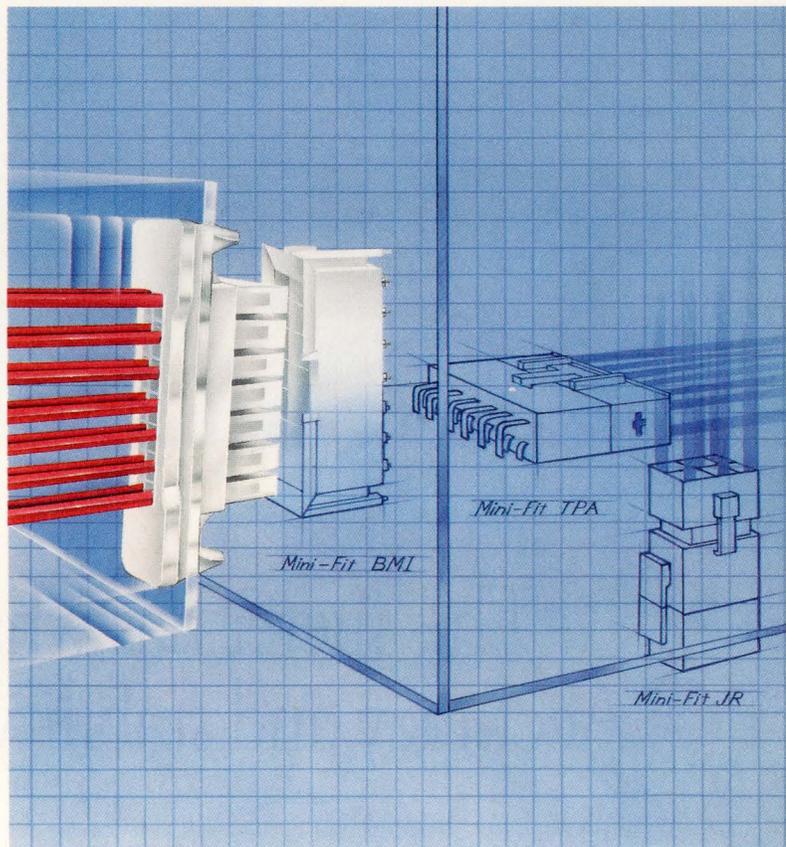
We were listening.

Change your circuit size. Change the configuration. There's no re-qualification of connectors when you work with the Mini-Fit family, including Mini-Fit, Jr.[™] and Mini-Fit, TPA[™] connectors.

That can mean substantial savings in time and work, especially since the Mini-Fit family offers such a wide range of connection options for power, (up to 9 amperes/circuit), and signal applications, (10 milliohm contact resistance).

And now the new Mini-Fit, BMI connector makes assembly more efficient and fool-proof than ever. Blind Mating Interconnects are designed for fast, positive alignment in blind-mating situations requiring wire-to-board, panel-to-board, and board-to-board connections. They can even eliminate harnesses in many applications.

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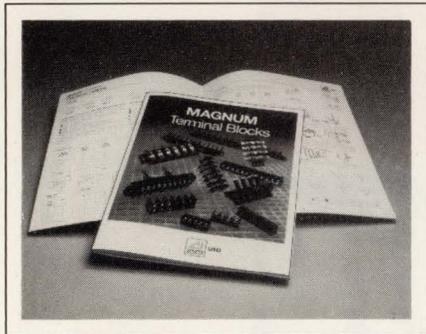
Take a look at the *fresh, innovative, and dynamic* graphic and editorial enhancement of EDN in the January 20th Magazine Edition.

EDN Magazine
Edition
News
Edition

EMC/EMI Materials Design Manual

The 24-pg Materials Design Manual contains information on properties of materials used to prevent electromagnetic interference, as well as design tips, formulae, and product applications. In particular, the manual discusses the new EC Directive on EMC, 89/336/EEC, a standard that takes effect in January of 1992. This directive affects European Community business standards as well as businesses that deal internationally and plan to conduct business within the EEC after the first of the year.

Nutwood Publicity Ltd, Marketing Consultants to RFI Shielding Ltd, Boyton End Farmhouse, Baythorne End, Halstead, Essex CO9 4AW, UK. Circle No. 435

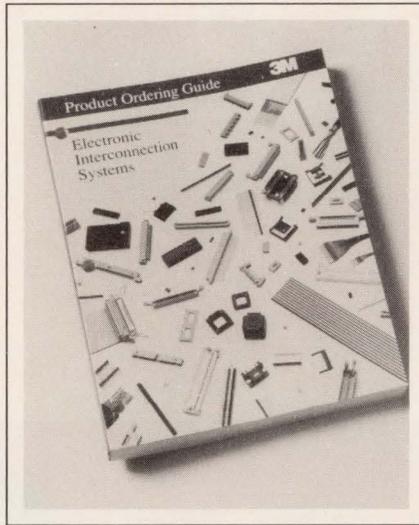


Offering Of Terminal Blocks

This 44-pg catalog covers a line of terminal blocks that include Magnum terminal blocks. It provides specifications and illustrations. The publication features the Magnum single-row terminal blocks, providing a selection of termination styles, such as pc boards, and right-angle, wrapped-wire, quick-connect, and solder turrets. Other products include double-row terminal blocks, edge-board connectors, stud-type junction blocks, and Mag-Master electronic/field wiring interfaces. The catalog lists six series types.

USD Products, 7300 W Wilson Ave, Chicago, IL 60656.

Circle No. 436



Plethora Of Connectors And Related Products

This 576-pg catalog, Electronic Interconnection Systems, is a product-ordering guide to connectors and related products. It describes connectors for IC sockets; board-mount and wire-mount sockets; Mix stacking; headers; plugs; DIN standard; pc boards; DIPs; card edge; D-sub; and D-ribbon. Related products include breadboard systems, cable, and assembly equipment. The publication features cross-reference charts for locating the products you want. Three indexes are classified by grid spacing, part number, and product type. Physical, electrical, and environmental specifications are given for each product.

3M, Electronic Products Div Catalog, Box 3064, Cedar Rapids, IA 52406. Circle No. 437

Publication Features Adjustable Speed Controls

The 8-pg brochure, Type ABL, presents operating and application information for the Type ABL low-voltage, adjustable speed controls for brushless dc motors. It discusses the three chassis-level PWM models: analog voltage, 8-bit parallel digital, or variable frequency. The publication describes other features, such as dynamic braking, plug-

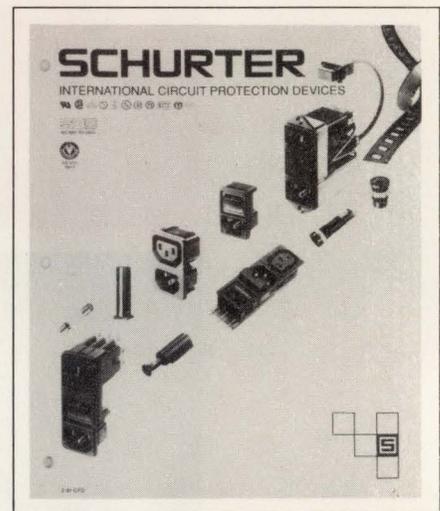
reversible direction control, adjustable acceleration rates, and current limiting. Specifications for the ABL-compatible 34B brushless dc motors and gearmotors as well as optional ABL accessories are included.

Bodine Electric Co, 2500 W Bradley Pl, Chicago, IL 60618.

Circle No. 438

Catalog Of Components

This 100-pg catalog provides an expansive listing of fuses, fuse holders, ac connectors and plugs, Nema 5-15R outlets, power-entry modules, and voltage selectors. It describes components for ac power-entry products having 1 to 20A IEC 320 inlets and outlets. Also featured are plugs for cold or hot



connections, snap-in and chassis-mount filtered power-entry modules, and the Felcom series of modular power-entry modules for custom configurations. It discusses newly introduced products, such as medical-grade fuse holders with captive fuse carriers, filtered and unfiltered power-entry modules, and 250V microfuses with pc-board leads built to IEC standards with UL recognition.

Schurter Inc, Electronic Components, Box 750158, Petaluma, CA 94975. Circle No. 439



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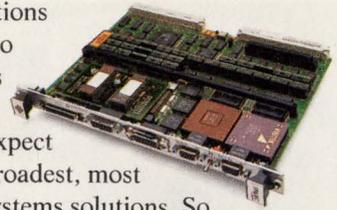
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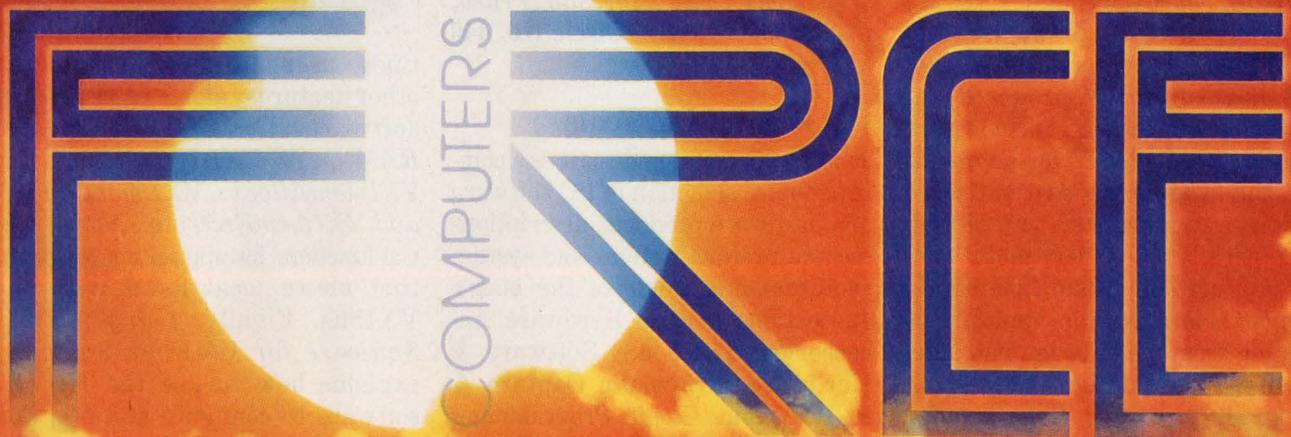
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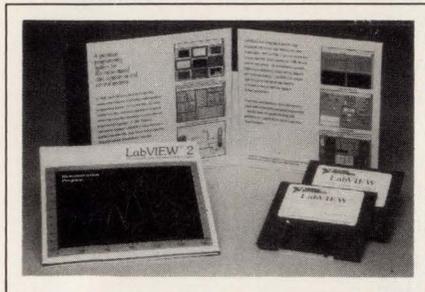
OUR NEW PARTNERSHIP IS AS HOT AS IT GETS.

CIRCLE NO. 37



Instrumentation-Software Demo Package

This demonstration package for a Macintosh computer with at least 2 Mbytes of RAM, 2 Mbytes of hard-disk space, and a 13-in. moni-



tor provides a "guided tour" of the Labview 2 instrumentation software package. It explains how the software works, shows how to build a virtual instrument (VI), and looks at a completed VI and its components.

National Instruments Corp., 6504 Bridge Point Pkwy, Austin, TX 78730. Circle No. 444

Catalog Documents Add-On Products For CAD/CAM

The 1991 Third Party Catalog features the vendor's software. It discusses approximately 200 hardware and software products that complement or extend the uses of the Personal Designer CAD package and the Personal Machinist CAM package. More than 80 third parties—including hardware and software vendors, CAD/CAM users, and CAD/CAM resellers—developed and now offer the products described in the catalog. Included are *Application Software* for augmenting the company's two software packages in areas such as solid design, parametrics, sheet-metal folding and unfolding, and kinematics; *Symbol Libraries* for applications ranging from mold design and steel detailing to tool design and welding; *Data Management Software* for tracking, revision control, and controlling access to engineering documents; *Translators* for exchanging the software packages' databases

with Chrysler, Ford, GM, and other databases; *Networking Products*, which links more than one of the two software-package systems; *Macros and Utilities* for time saving and convenience in areas such as text editing, plot spooling, and redefining keyboard and menu layouts; *Training Manuals and Teaching Aids* to augment the standard documentation and tutorials; and *PC Hardware*, which provides graphics boards, plotters, digitizers, and other peripherals.

Computervision, 100 Crosby Dr, Bedford, MA 01730. Circle No. 445

Newsletter Cites Spice Options

You can read about undocumented Spice options and the development of the first Spice-based fuse model in this issue of the company's newsletter. One example cited is Source Stepping, a Spice option that enhances Spice dc-convergence properties. An application note traces the development of Spice models for slow-blow, normal, and fast-acting electrical fuses. Other features include a special upgrade of the Spice model generator, Spicemod 1.4; a Spice model library for RF frequency-range transistors; op-amp model libraries; and training seminars for Spice.

Intusoft, Box 710, San Pedro, CA 90733. Circle No. 446

Catalog Of PC Tools

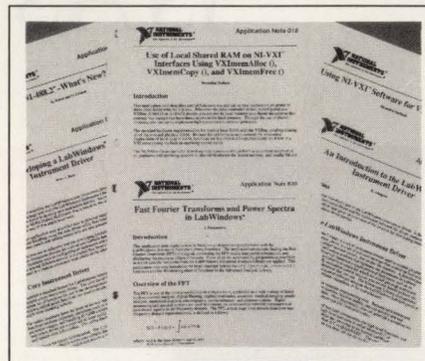
This 160-pg catalog describes a comprehensive selection of PC software and hardware products; descriptions include product options and system requirements. Some of the book's 12 sections include Hardware Accessories, IEEE-488 Software & Hardware, Schematic Capture & PCB Layout, Logic Programming & Simulation, Analysis & Design Programs, CAD, Programming Tools & Utilities, and Text Processing. The Product Index helps you

find your selections. Discounts for related products are specified in the "Acom-Packs," which are found throughout the catalog.

Acom Technologies Inc, 2330 Old Middlefield Way #10, Mountain View, CA 94043. Circle No. 447

App Notes Cover FFTs, LabWindows, And VXI Systems

The first of these six application notes, titled *An Introduction to the LabWindows Instrument Driver*, describes the components of an instrument driver and the interaction between the driver components. *Developing a LabWindows Instrument Driver* explains how to use the core driver utility functions to perform error handling. *Fast Fourier Transforms and Power Spectra in LabWindows* examines the building of a signal-processing application, using the Labwindows Advanced Analysis Library. *NI-488.2—What's New?* discusses the functions, rou-



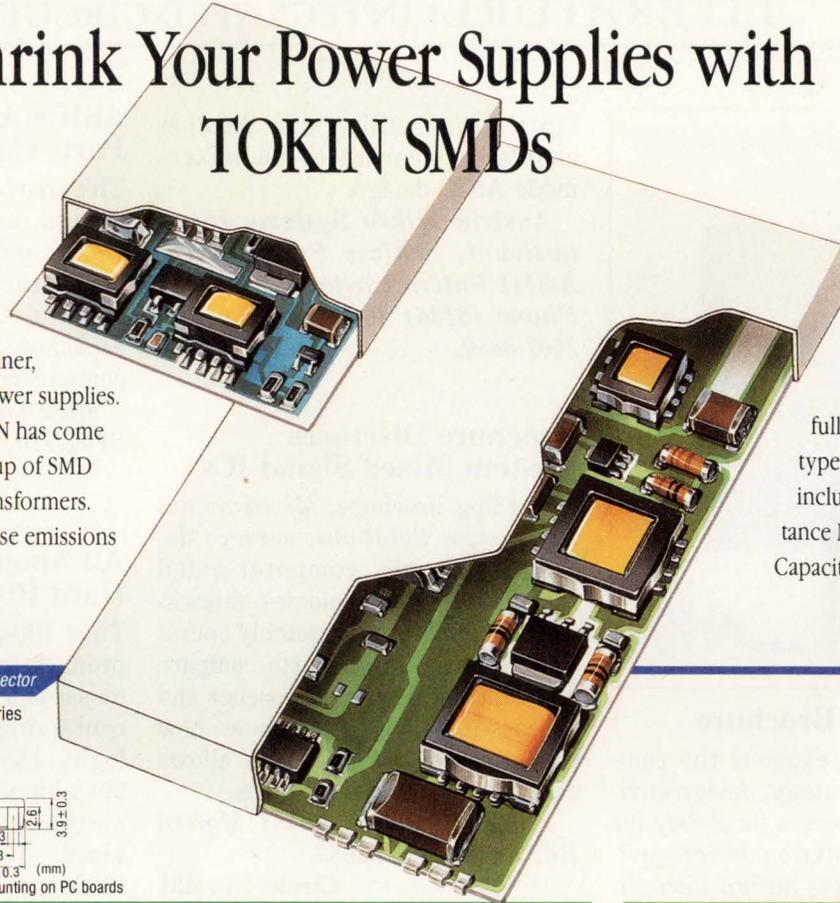
tines, user-interface options, and other features added to the driver software. *Use of Local Shared RAM on NI-VXI Interfaces, Using VXImemAlloc(), VXImemCopy(), and VXImemFree()*, examines special functions for application programs that share local RAM with the VXIbus. Finally, *Using NI-VXI Software for VMEbus Systems*, explains how to use the NI-VXI software to configure and program a VMEbus system.

National Instruments, 6504 Bridge Point Pkwy, Austin, TX 78730. Circle No. 448

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Products above are sold only in the U.S.

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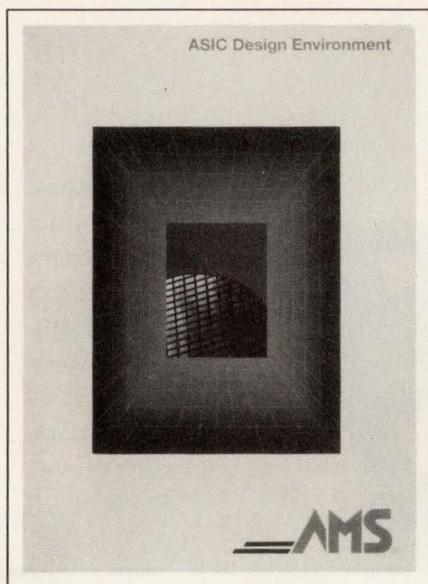
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ASIC Design Brochure

This publication explains the company's design strategy, design environment, and process flexibility for ASICs. The chapter on design environment overviews design tools, li-

braries, and utility kits. Another chapter concentrates on mixed-mode ASIC design.

Austria Mikro Systeme International, Schloss Premstätten, A-8141 Unterpremstätten, Austria. Phone (3136) 36660. FAX (3136) 2501-3650. Circle No. 430

Brochure Discusses Custom Mixed-Signal ICs

The 12-pg brochure, *Mixed Signal IC Custom Solutions*, surveys design approach, computer-aided tools, process technologies, fabrication capability, and assembly operation. Easy-to-read charts compare and contrast design approaches and processes. A flow chart shows how the step-by-step approach allows satisfactory custom solutions.

Silicon Systems, 14351 Myford Rd, Tustin, CA 92680.

Circle No. 431

ASICs And Standard Parts Cataloged

This short-form catalog explains the design services for producing CMOS and BiCMOS ASICs. It details a range of standard parts, including ADCs, DACs, switched-capacitor filters, and a variety of communications ICs.

Micronas Inc, Kamreerintie 2, SF-02770, Espoo, Finland.

Circle No. 432

All About Radiation Hard Products

This 700-pg publication contains product information about silicon-on-sapphire ICs. It describes RAMs containing as many as 64k bits, logic, 1553 databus components, 29xx bit slice, and MIL-STD 1750A microprocessors and peripheral devices. Also included are ASICs having as many as 30,000 gates.

GEC Plessey Semiconductors, Cheney Manor, Swindon, Wiltshire SN2 2QW, UK. Circle No. 433

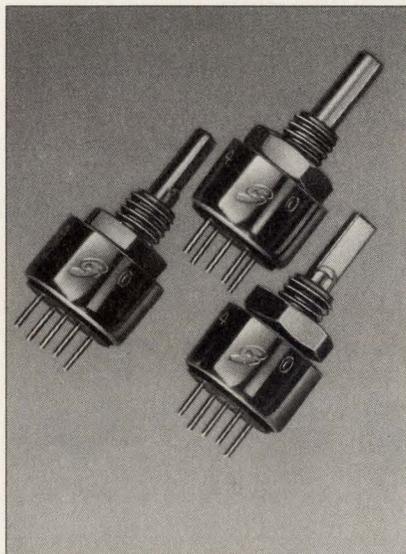
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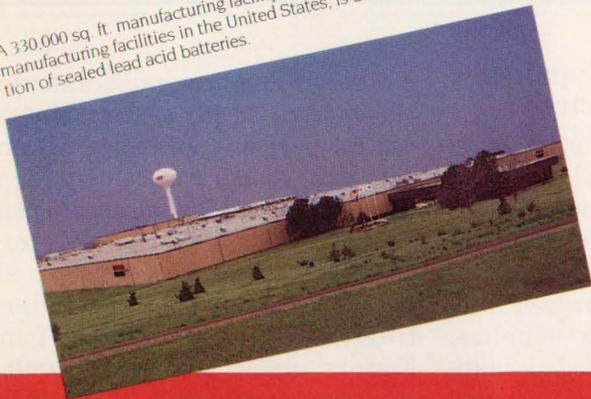
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Four Publications Present IC Products

The sixth edition of *ASIC & Custom Products Short Form Catalog* provides single-page descriptions of devices from the frequency-synthesis, forward-error-correction (FEC), and coding and demodulation product families. The book also outlines the custom design service. *The DDS Handbook* offers 216 pages of data sheets and application notes on direct-digital-synthesis products, from ASICs through board- and chassis-level products. *The Spread Spectrum Handbook* is a 189-pg compilation of data sheets and application products. *The Forward Error Correction Handbook* covers FEC encoding and decoding in its 56 pages of data sheets.

Stanford Telecom, ASIC & Custom Products Div, 2421 Mission College Blvd, Santa Clara, CA 95056. Circle No. 434

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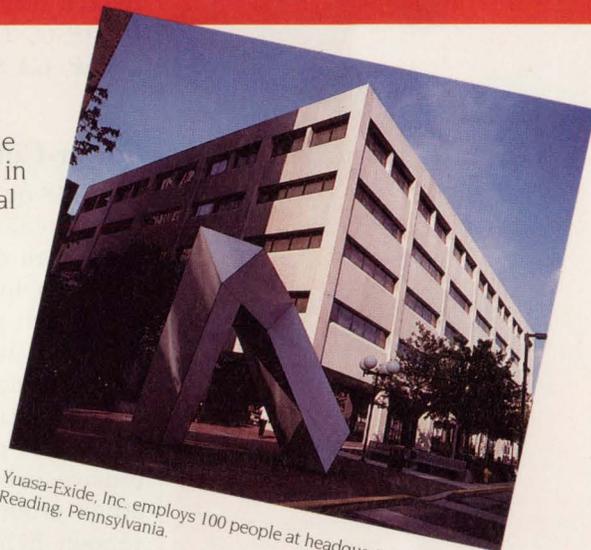
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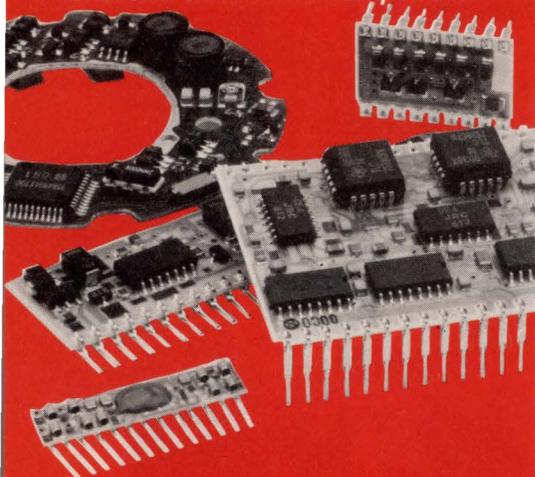
Yuasa-Exide, Inc. employs 100 people at headquarters in Reading, Pennsylvania.

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Power supply needs?...contact Xentek, Inc. (a subsidiary of Taiyo Yuden) at (1-619) 727-0940 or ask your Taiyo Yuden representative.

CIRCLE NO. 96

LITERATURE: POWER SOURCES

Listing Of Power Supplies And DC/DC Converters

This 16-pg catalog offers a quick glance at the company's products for high-voltage power supplies and dc/dc converters. Proportional PC modules, miniature low-power converters, low-noise PC modules, precision photomultiplier supplies, miniature-rugged, regulated multiple-output, and precision-regulated CRT supplies, as well as custom high-voltage supplies are a few of the products covered in this catalog. For each section, a product photo accompanies specifications and related technology or information.

EMCO, 11126 Ridge Rd, Sutter Creek, CA 95685. Circle No. 440

Power-Conversion Catalog

This 148-pg power-conversion catalog provides specifications, data sheets, an ordering guide, and applications for more than 170 power-conversion products. The range of products includes 57 wide-range-input, dc/dc converter modules in industry-standard 2x2-in., 2x1-in., and 24-pin double DIPs. An extensive overview of the vendor's other products includes data-conversion hybrids, IBM PC/AT and VMEbus board-level products, and panel-mount instruments. A glossary of Power-Supply Terms and a section on Modern Power Supply Principles and Practices details some recent innovations in power-converter design as well as in standard design practices.

Datel Inc, 11 Cabot Blvd, Mansfield, MA 02048. Circle No. 441

Switch-Mode Rectifier Series

This 23-pg short-form catalog presents electrical specifications, operating characteristics, and design benefits of the Twinpack switch-mode rectifier systems. It outlines the advantages of each component and offers charts and product photos. Describing Twinpack modular

power systems, the publication includes the PS/19; system status/control panels; low-voltage disconnect panels; miniload centers; digital-equalize panels; fuse-alarm panels; fuse panels; circuit-breaker panels; battery-disconnect panels; positive or negative-bus bars; battery trays; relay racks; ringing generators; dc/dc converters; dc/ac static converters; and a μ P monitor.

Power Conversion Products Inc, Box 380, Crystal Lake, IL 60014. Circle No. 442



Power-Protection Devices

This 46-pg catalog presents power-protection devices for PCs, microcomputers, minicomputers, LANs, workstations, PBXes, and other sensitive equipment. The table of contents lists section titles such as New Technology, How to Solve Power Problems, Choosing the Level of Protection That's Right for You, How to Buy a UPS, The Ferrups Line, Fortress, PLC, Spike-free, Interface Kits, Extended Runtime Options, Installation Options, and Service Plans. Photos and question-and-answer sections complement the product specifications, listings, and technology updates. The catalog's tables supply competitor's prices and comparative product information such as option prices and compatibility requirements.

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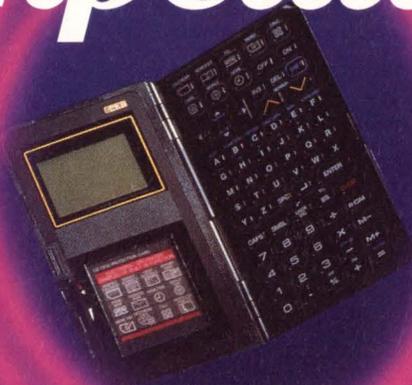
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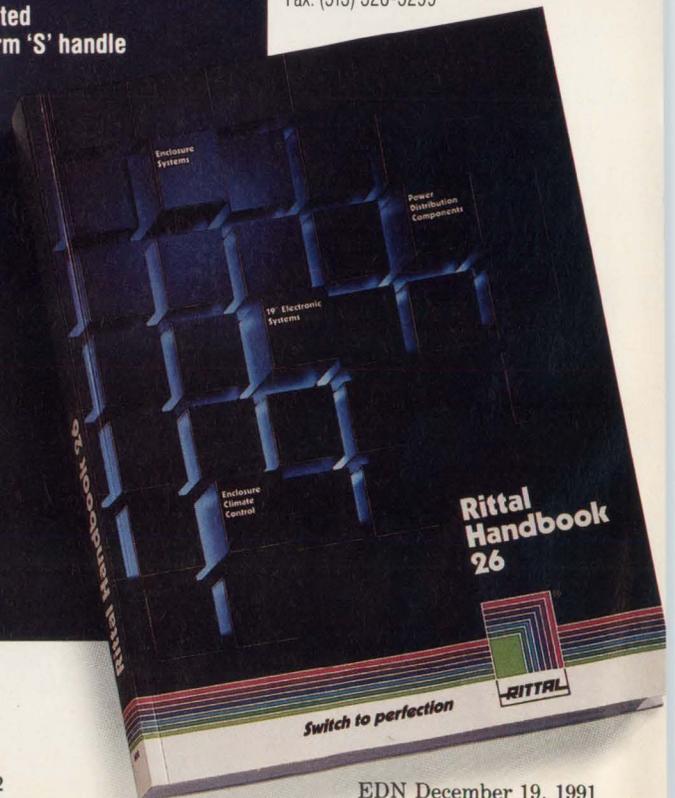
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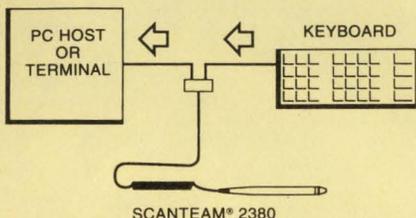


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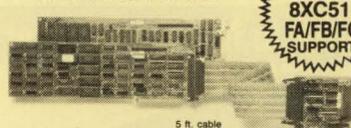
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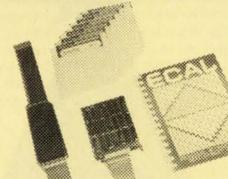
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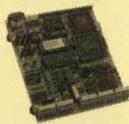
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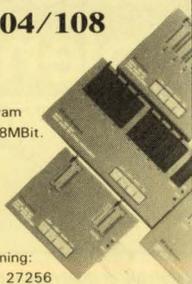
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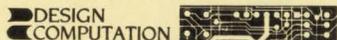
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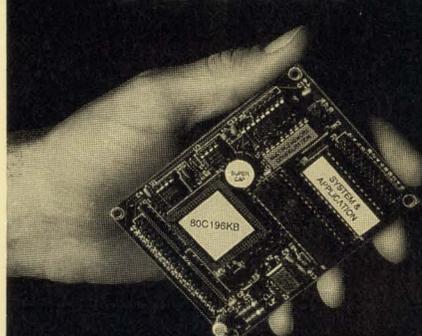
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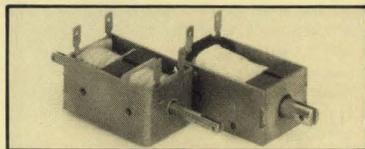
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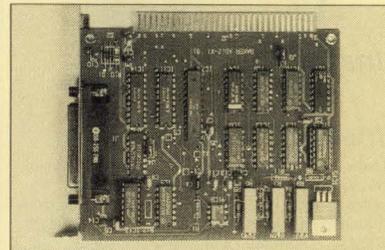


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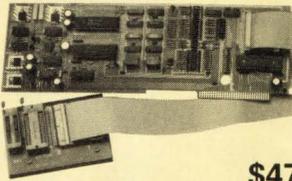
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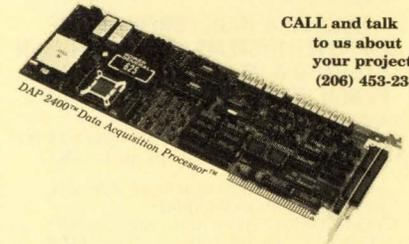
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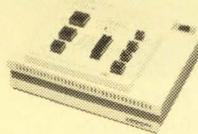
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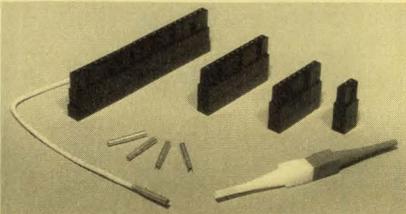


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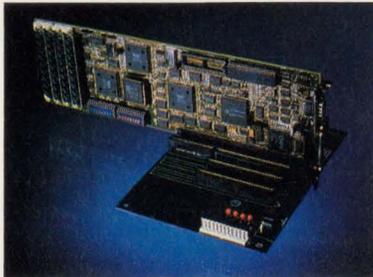
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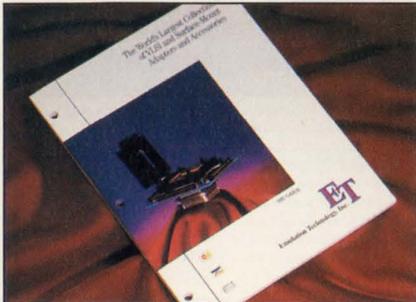
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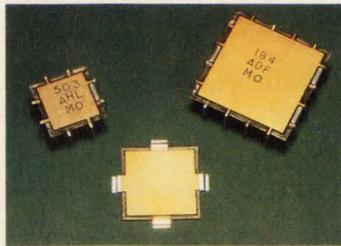


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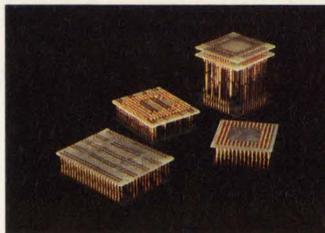
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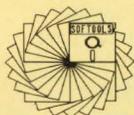
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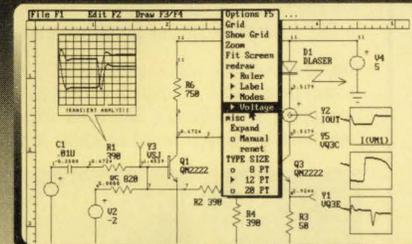


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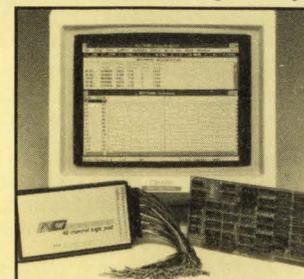
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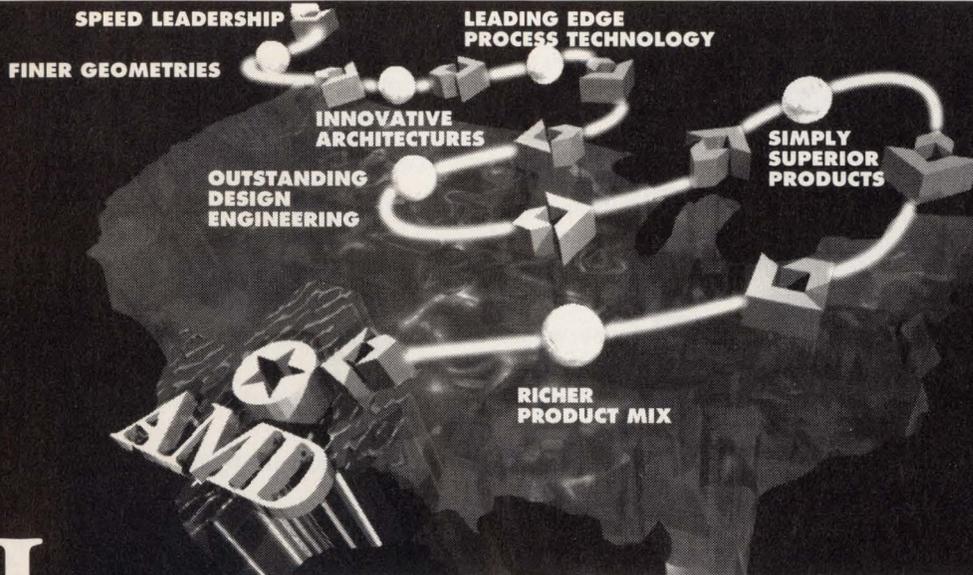
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News Edition	Jan. 9	Dec. 24, '91	Test & Measurement • Medical Electronics • Diversity Special Series
Magazine Edition	Jan. 20	Dec. 26, '91	Microcomputer Boards & Software—Part I • ICs & Semiconductors • Hardware & Interconnect • Technical Article Database Index • Buscon Show Coverage
News Edition	Jan. 23	Jan. 9, '92	Embedded Processors & Controllers • Buscon Hot Products • Automotive Electronics Regional Profile: N. Carolina, S. Carolina, Georgia
Magazine Edition	Feb. 3	Jan. 9, '92	Digital ICs • Microcomputer Boards & Software—Part II High-Speed Digital Circuits Software/CAE
News Edition	Feb. 6	Jan. 23, '92	STATE OF ENGINEERING Special Supplement Computers & Peripherals Communications Technology Annual Salary Survey
Magazine Edition	Feb. 17	Jan. 23	EDN's 35th Anniversary Issue • ASICs • ICs & Semiconductors • Test & Measurement • Manufacturing Issues
News Edition	Feb. 20	Feb. 6	ICs & Semiconductors • ISSCC Hot Products • Computers & Peripherals • Regional Profile: Colorado, Utah, Idaho
Magazine Edition	Mar. 2	Feb. 6	COMMUNICATIONS SPECIAL ISSUE • Test & Measurement • Local-area Networks • Microprocessors Memory Technology
News Edition	Mar. 5	Feb. 20	Memory Technology • CPU Boards • Computers & Peripherals • Diversity Special Series
Magazine Edition	Mar. 16	Feb. 20	COMPUTER & PERIPHERAL SPECIAL ISSUE • Multimedia Components • Memory Technology • Computer Peripherals • International Technology Update—Japan
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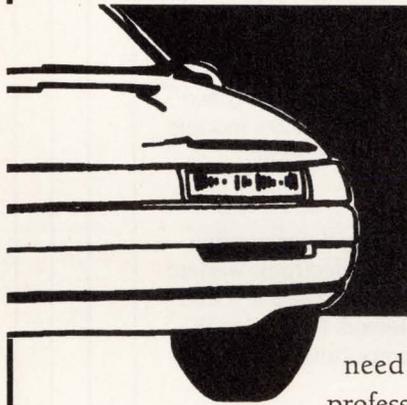
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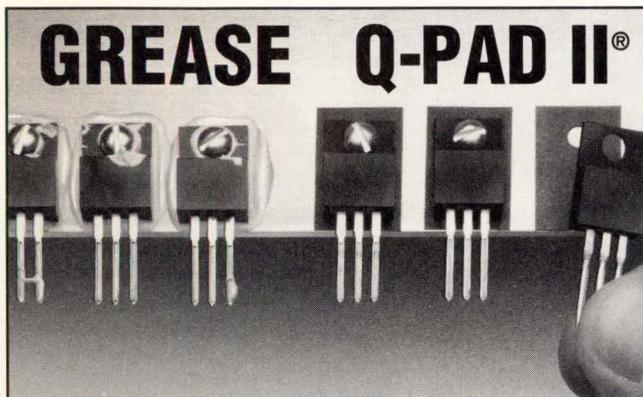
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ADC—analog-to-digital converter
Arcnet—attached-resource computing network. The first local-area network, developed by Datapoint Corp.
ASCII—American Standard Code for Information Interchange
ASIC—application-specific integrated circuit
ATE—automatic test equipment
CAE—computer-aided engineering
CCD—charge-coupled device
CLB—configurable logic block
CMOS—complementary metal-oxide semiconductor
CPU—central processing unit
CSMA/CD—carrier-sense multiple access with collision detection
D/A—digital to analog
DIP—dual in-line package
DMM—digital multimeter
DoD—Department of Defense
ECL—emitter-coupled logic
EMF—electromotive force
EPLD—erasable programmable logic device
EPROM—erasable programmable read-only memory
FAST—Fairchild Advanced Schottky TTL
FDDI—fiber-distributed data interface
FPGA—field-programmable gate array
GAL—generic array logic
HDL—hardware description language
IEEE—Institute of Electrical and Electronics Engineers
IEEE-802.3—Standard governing networks using a logical bus architecture and a CSMA/CD media-access protocol. This architecture is more commonly called Ethernet.
IEEE-802.5—Standard governing the token-ring network architecture originated by IBM Corp.

IEEE-802.x—Family of network-architecture standards; also the IEEE subcommittees responsible for those standards.
I/O—input-output
ISO—International Standards Organization
LAN—local-area network
LCA—logic cell array
MAP—Manufacturing-Automation Protocol. A network protocol developed by General Motors Corp to interconnect computers and programmable factory equipment.
MS-DOS—Microsoft disk operating system
MSI—medium-scale integration
OEM—original equipment manufacturer
OSI—open-systems-interconnection
PAL—Programmable Array Logic, trademark of Advanced Micro Devices
PC—personal computer
PLA—programmable logic array
PLCC—plastic leaded chip carrier
PLD—programmable logic device
PROM—programmable read-only memory
RAM—random-access memory
RC—resistance-capacitance
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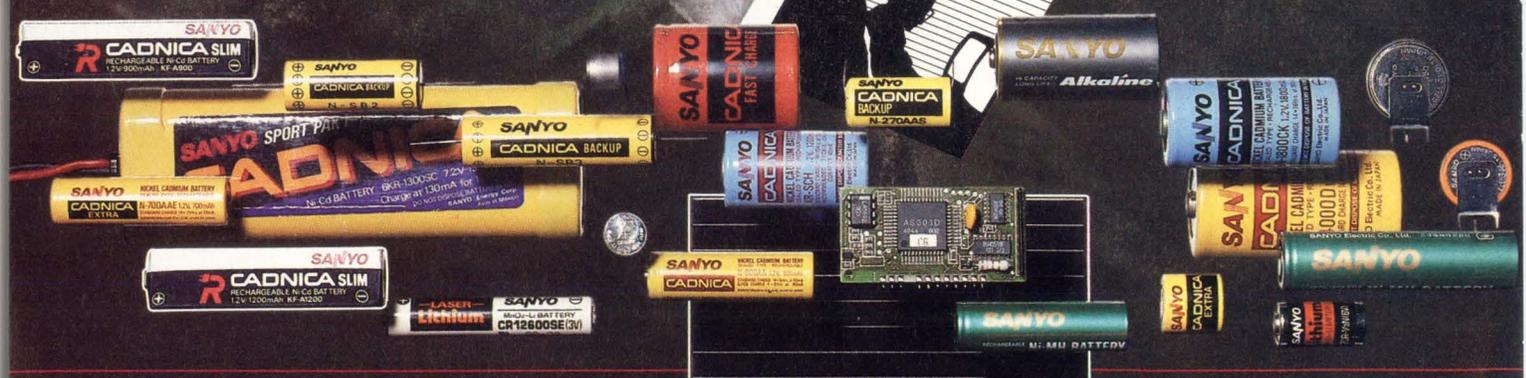
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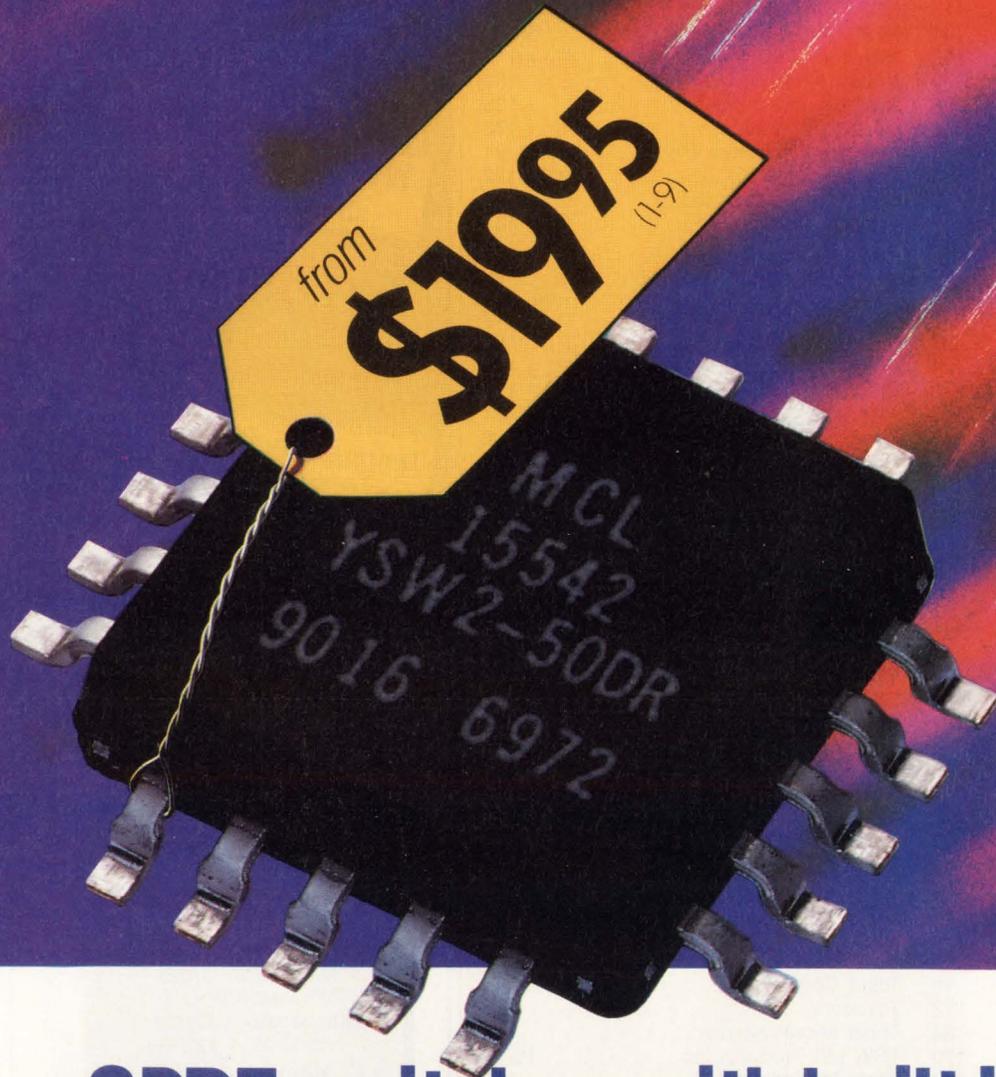
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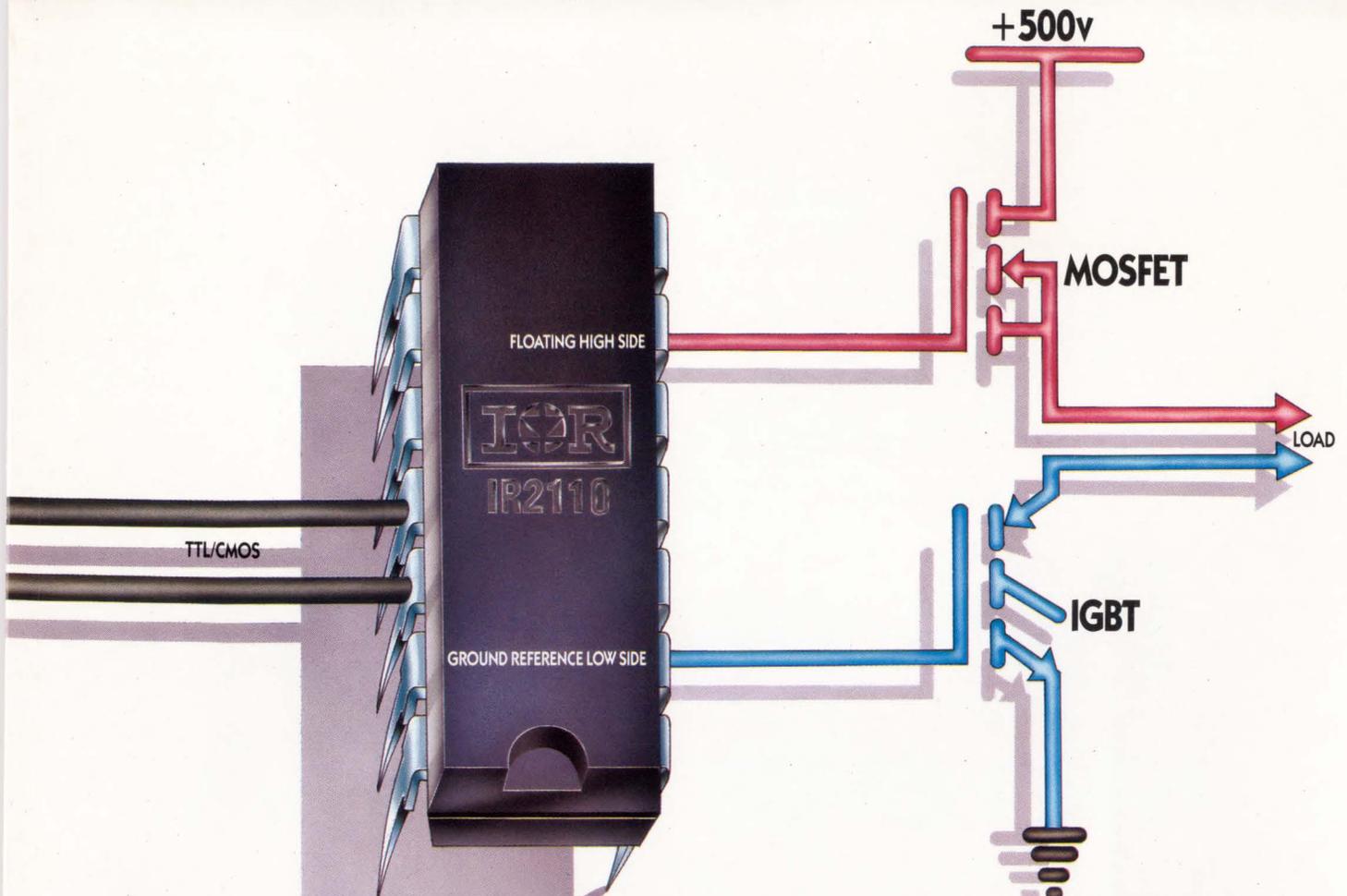
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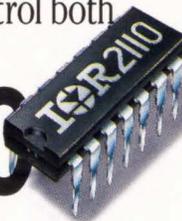
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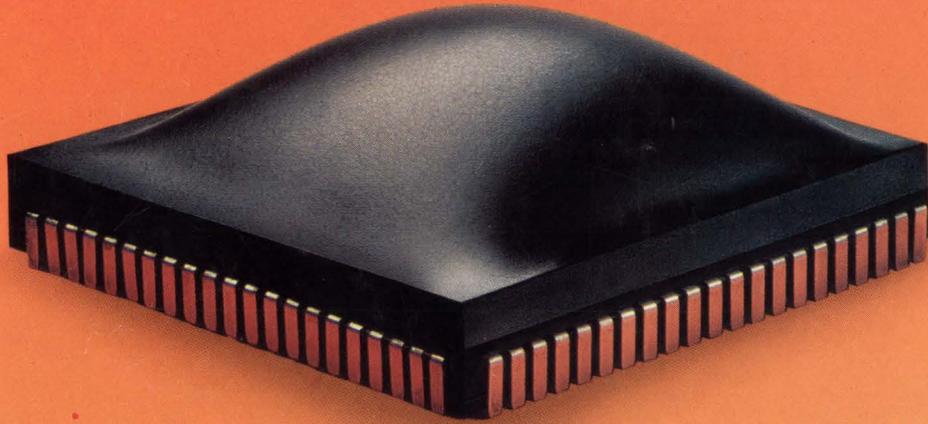
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