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COMPUTER DESIGN®

SEPTEMBER 15, 1988

THE FIRST MAGAZINE OF SYSTEM DESIGN, DEVELOPMENT AND INTEGRATION

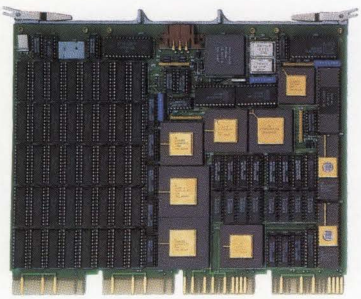
Designers' Buying Guide to Peripheral Controller Boards

In search of the high-performance controller

New analysis techniques pave the way for analog simulation

High-resolution monitors fulfill demands of CAD/CAM

The Graphics Engine That Meets Government Standards As Well As Your Own.



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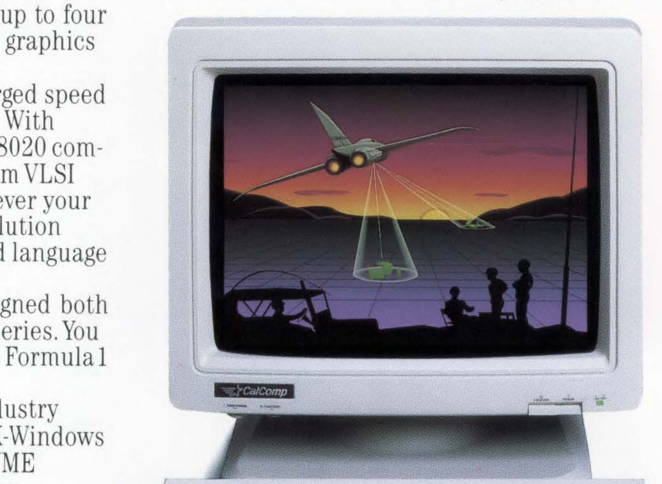

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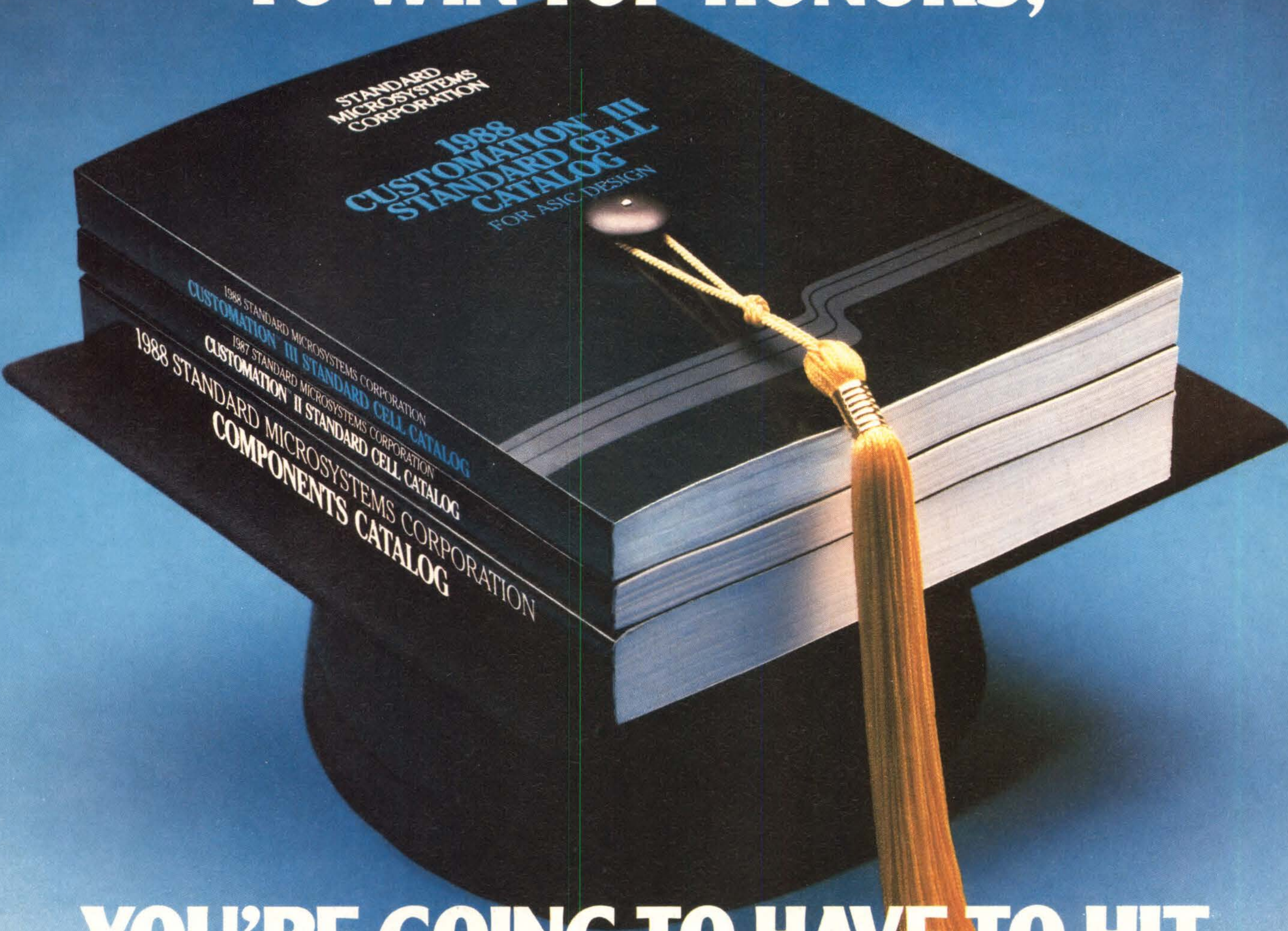

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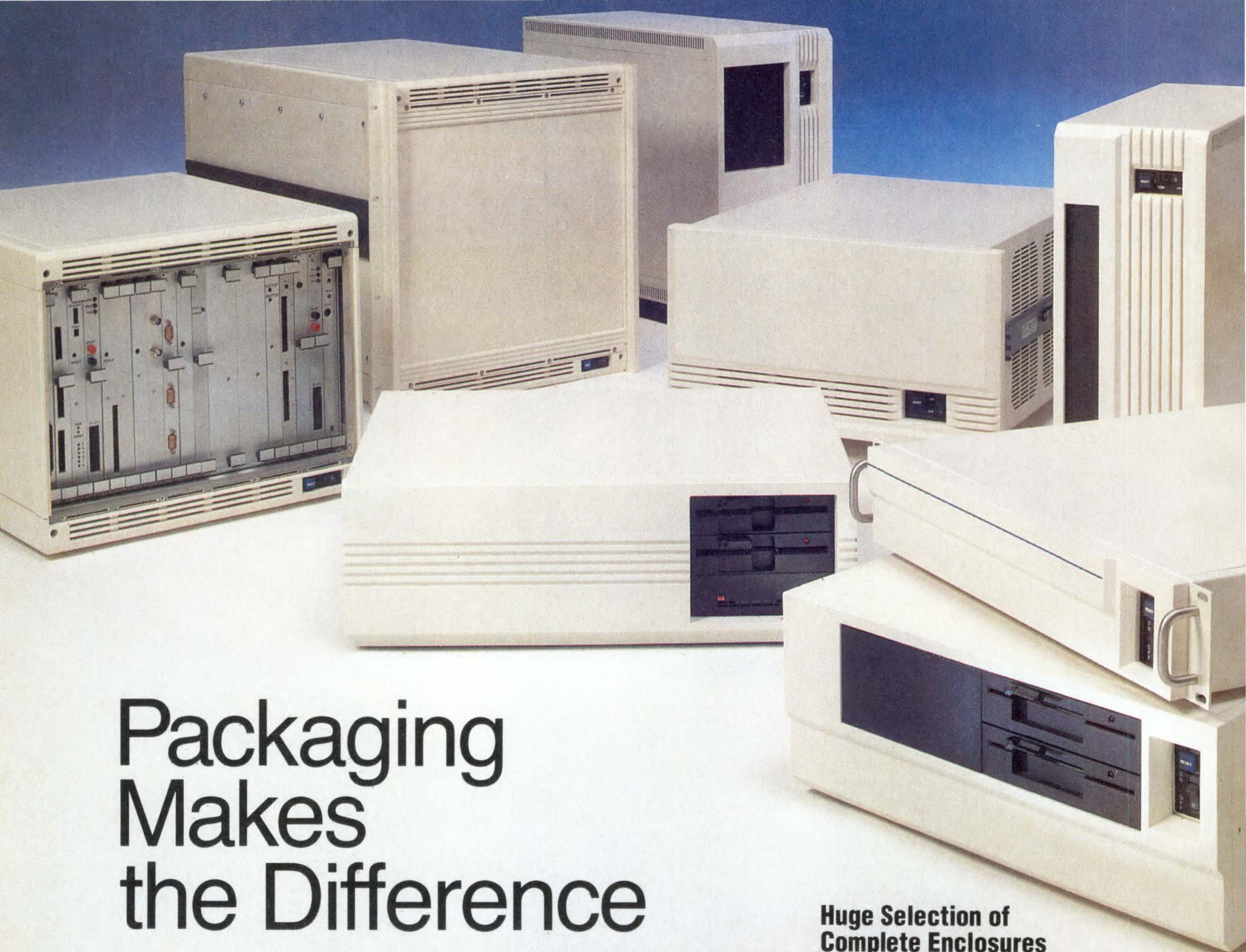

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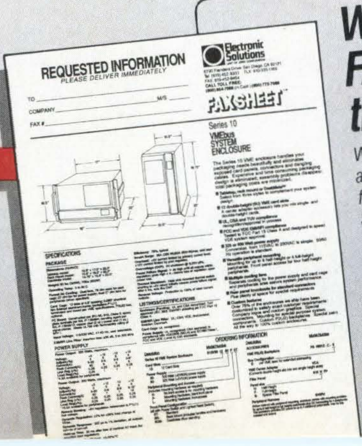

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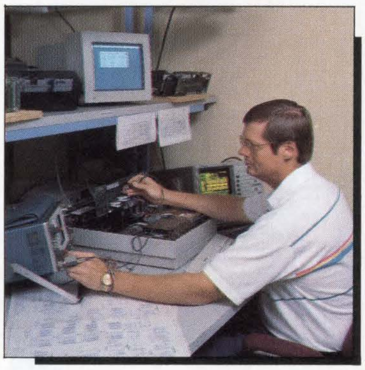
CIRCLE NO. 3

Vol. 27, No. 17

COMPUTER DESIGN®

SEPTEMBER 15, 1988

THE FIRST MAGAZINE OF SYSTEM DESIGN, DEVELOPMENT AND INTEGRATION



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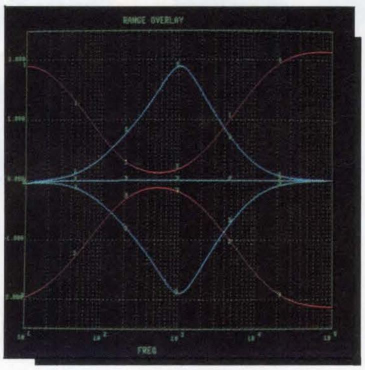
■ TECHNOLOGY UPDATES



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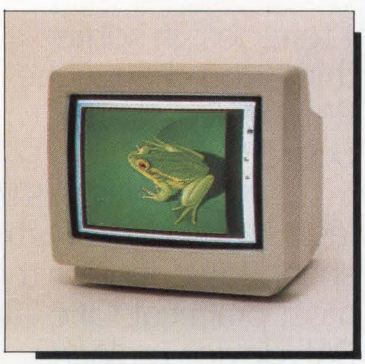
■ TECHNOLOGY AND DESIGN FEATURES



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■ NEW PRODUCT HIGHLIGHTS

■ DEPARTMENTS/COLUMNS

How the fa

Our new 7.5ns PAL® device is fast enough to prove that standard logic shouldn't set the standard anymore.

It's also fast enough to finally let today's new microprocessors run at the speeds for which they were designed—breathtaking.

Raising your standard.

How fast would you like your standard logic?

How about faster than any TTL logic around? Even FAST™ or AS? You've got it with the 7.5ns PAL device.

And the fact that you can configure it yourself means you can get exactly what you want.

If you want to redesign something, you change the PAL device. Not the board.

Not only is this the fastest way to get high speed logic, it's also the most practical. One 7.5ns PAL device replaces two to six standard TTL devices.

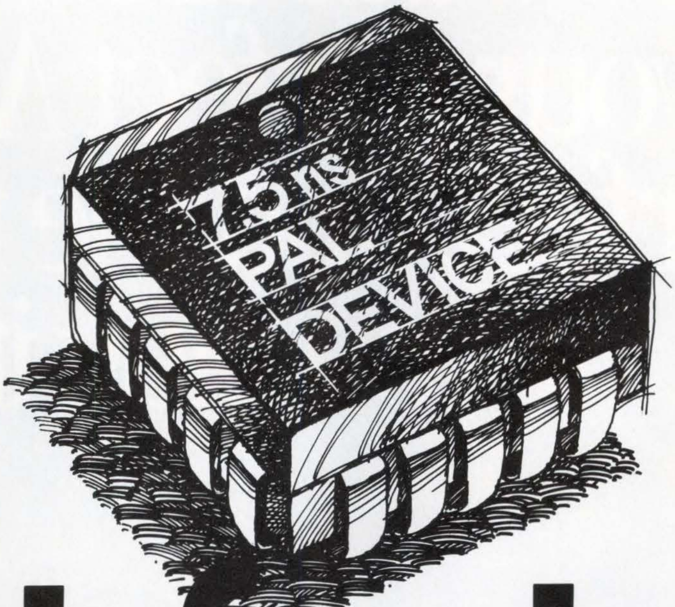
Which cuts down on board size.

And cuts down chances for a device failure.

7.5ns PAL Device vs. FAST & AS

SSI/MSI		FAST	AS	7.5ns PAL Device
Combinatorial				
74138 Decoder	tPD	8.0	10.0	7.5
74151 Mux	tPD	11.0	15.0	7.5
Register/Latch				
74374 Octal Register	tCO	10.0	9.0	6.5
74373	tPD	8.0	6.0	7.5
Octal Latch	tLEO	13.0	11.5	7.5
Counters				
74161	tS	5.5	8.0	7.0
Four bit Ctr	tCO	11.0	13.5	6.5
74269/869	tS	2.5	5.0	7.0
Eight bit Ctr	tCO	10.0	11.0	6.5

st get faster.



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CIRCLE NO. 4


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CIRCLE NO. 5 CAREER INFORMATION
CIRCLE NO. 6 PRODUCT INFORMATION

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The vertical-recording cha-cha plays on

It's on again, off again as far as the shipment of real products incorporating vertical-recording technology. In vertical recording, the magnetic domains are perpendicular to the surface of the media and can thus be spaced much more closely together than in traditional longitudinal recording used in present magnetic disks and tape.

Censtor (San Jose, CA) has developed vertical-recording heads and media for Winchester drives, and products using the technology had been expected to appear this summer. Likewise, Toshiba, which introduced a 3½-in. floppy drive with vertical recording based on a barium-ferrite media, suddenly balked at a scheduled announcement of product shipment. In both cases, however, the problems appear to be hassles with initial customers rather than problems with the technologies.—*Tom Williams*

DEC challenges AT&T with open-system Ultrix

This month's DECworld '88 will provide a platform to demonstrate Ultrix-32 Version 3, an enhanced native-mode Unix-based operating system. This marks the first major operating system introduction to be made by Digital Equipment Corp (Maynard, MA) since the formation of the Open System Foundation (OSF), a consortium of major computer manufacturers organized to challenge the AT&T/Sun domination of Unix as an industry operating system standard.

DEC's sponsorship of the OSF was a first move toward supporting open operating environments. Ultrix-32 V3.0 lets applications be run on computers from many different vendors—including those from IBM, DEC's major rival. The move to an open operating system came about because customers expressed a need to protect their technological investments but wanted software portability, according to Donald McInnis, vice-president of DEC's Engineering Systems Group.

In addition to meeting OSF Application Environment Specification Level 0, Ultrix-32 V3.0 offers full compliance with the IEEE 1003.1 Portable Operating System for Computer Environments (Posix), the National Bureau of Standards interim Posix FIPS, and the Common Application Environment. It also meets the System V interface Definition Release II, Vol 1, and has added Berkeley Distribution 4.3 enhancements.—*Sydney Shapiro*

Flat-panel displays inch toward full-VGA goal

The biggest barrier today to the wide acceptance of laptop computers is the quality of the display. Current LCD flat-panel displays may sport 600×300 dots, but the actual screen resolution has reached only about 320×200 displayable pixels—the quality of IBM's low-level Color Graphics Adapter (CGA) standard—in monochrome. When these displays are backlit, they provide passable viewability, but not the black-and-white paperlike quality desired by users.

Now, however, practically all Japanese manufacturers are readying displays using neutralized twisted nematic (NTN) LCD technology that, when backlit, can provide crisp, printlike black-on-white contrast as well as up to 16 levels of gray scale. What's more, the new displays offer a screen display resolution of 640×480 pixels, compatible with IBM's Video Graphics Array (VGA) standard, which was introduced with the Personal System/2 family. Still missing is color, but that will have to wait for the perfection of active matrix displays.

Active matrix displays have transistors at each pixel location to turn that pixel on or off. When such transistor/pixel locations are arranged in sets of three and backlit by a matching pattern of red, green and blue areas, color images can be produced. Color active matrix displays are available in small formats. Ovonic Imaging (Troy, MI) produced prototypes of a VGA resolution monochrome active matrix display in a 6-×8-in. format, but has not yet begun producing in volume.
—*Tom Williams*

New bus equips AT for multiprocessing

"The next technology to make its way from mainframes to the desktop will be multiprocessing," claims George White, president of Corollary (Irvine, CA). The company has come up with a scheme to facilitate that transition. Corollary has developed a new architecture, code-named ATtack, that lets sophisticated multiprocessing take place on an IBM PC AT platform without sacrificing compatibility with the bus.

The ATtack system is built around a 32-bit data channel and a multiprocessing kernel. Called the C-bus, the data channel lets up to six 80386-based CPU boards intercommunicate at up to 64 Mbytes/s. The multiprocessing kernel, which is derived from, and is binary-compatible with, Xenix, distributes workloads among the different processors. The company is currently pursuing cooperative ventures with leading PC-compatible vendors to bring the architecture to market.—*David Lieberman*

Agreement links CASE to development system

One of the weak points of computer-aided software engineering (CASE) is its lack of integration with microprocessor development systems. A recent agreement between Interactive Development Environments (San Francisco, CA) and Interact (New York, NY) may help bridge the gap by tying IDE's CASE tools to Interact's development system.

Under the agreement, IDE's Software through Pictures product will become part of the Interact System Design Environment. Software through Pictures includes tools for structured analysis, structured design and documentation. The System Design Environment provides cross compilers, assemblers, linkers, simulation tools and debugging tools. The integrated system will be marketed by LSI Logic (Milpitas, CA), one of Interact's major backers.—*Richard Goering*

(continued on page 10)

Intel boosts 386 chip performance to 25 MHz

Intel (Santa Clara CA) hopes to break away from the IBM Personal System/2 competition by raising the speed and integration levels of its Micro Channel peripheral chips. Slated for sampling in the fourth quarter with production early next year, the next generation of the 82310 series can handle processing speeds up to 25 MHz. To ease migration for users of older 16- and 20-MHz families, Intel will offer a daughter board housing most of the new functions. A similar migration path is planned for the next generation of 33-MHz products, allowing an engineer to retain at least a portion of the previous generation's design. *—Mike Donlin*

Large-scale computers move up to GaAs

IBM will move beyond ECL to gallium-arsenide logic in its next decade's mainframes, according to a report just issued by the International Technology Group (Los Altos, CA). The company's coming architecture, according to the report, will also incorporate reduced-instruction-set computer technology, some form of parallel processing, and a distributed I/O bus structure that uses high-speed peer-to-peer fiber-optics communications. GaAs processing will hit the streets well before IBM's next-generation offering, however, with the GaAs-based Cray 3 supercomputer from Cray Research (Minneapolis, MN) expected to be formally announced sometime next year and with Digital Equipment Corp (Maynard, MA) reportedly also developing a high-speed GaAs-based memory subsystem. *—David Lieberman*

Logic synthesis addresses ASIC testability issues

Although logic-synthesis tools can generate gate-level logic from high-level descriptions, most don't help with testability. A new product, the Logic Synthesizer from VLSI Technology (San Jose, CA), automatically produces high fault-coverage test vectors for the gate-level logic it generates. This capability can greatly reduce test development time and remove engineers even further from the details of gate-level logic.

The Logic Synthesizer is an enhanced version of VLSI Technology's State Machine Compiler, which generates logic from a state machine language. It can produce an optimized layout for a programmable logic array within an ASIC, or a net list that's implemented in a gate array or standard-cell device. *—Richard Goering*

Not-so-fast PS/2 data-acquisition boards meet today's needs

Being faster may not always buy you much. Reacting to customer requests for low-level data acquisition that will match the limited available power of IBM Personal System/2 models now in use for scientific and engineering applications, Data Translation (Marlborough, MA) has introduced two such boards for PS/2 Models 50, 60 and 80.

The lack of the OS/2 operating system for the PS/2 prevents PS/2 models from using their full potential, according to Bernadette Morrissey, product marketing specialist. These initial introductions from Data Translation, although slower than the comparable boards introduced recently by National Instruments (Austin, TX), for example, are adequate for current applications, Morrissey claims.

To overcome real-estate limitations inherent in the small PS/2 board size, Data Translation designed two custom ICs, one to control on-board data transfers and one to serve as an interface to the PS/2's Micro Channel bus. In addition to saving space and thereby making room for additional board features, these chips also reduce power consumption. Data Translation will introduce image-processing boards for the PS/2 in November, according to Morrissey.*—Sydney Shapiro*

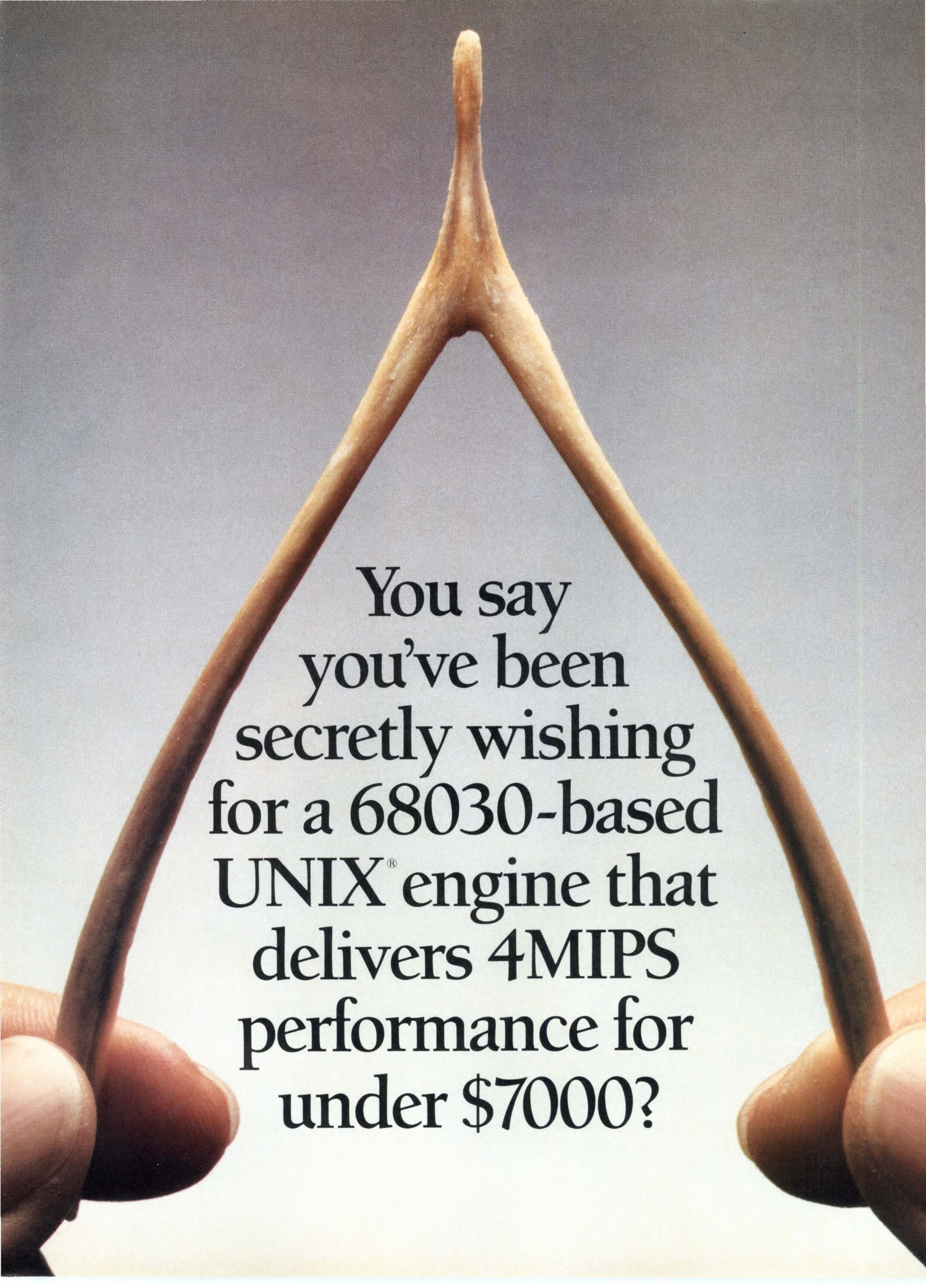
New file system transparently manages scalable I/O

As Intel Scientific Computers (Beaverton, OR) sees it, the prime claim to fame of the hypercube architecture for parallel computing is its inherent scalability. Computing power can be increased simply by adding nodes to the system. This month, the company will introduce a set of new facilities that adds scalable I/O to the equation in its iPSC/2 parallel machine. While a number of other vendors of parallel computers are enhancing their I/O subsystems by replacing a central disk drive resource with banks of small drives—typically with one drive per computing node—Intel's approach is somewhat different.

The company's Concurrent File System makes a mass-storage matrix look like a conventional large disk drive to the user, yet there's no need to queue and coordinate I/O requests. File management is, however, completely transparent to the programmer, who need not concern himself with what data is stored on which drive.*—Mike Donlin*

Mini-cartridge drives track 3½-in. Winchester evolution

As 3½-in. Winchesters move well beyond the 100-Mbyte barrier, tape drive manufacturers offering comparable backup potential are striving to follow suit. Look for tape drive vendor 3M (St Paul, MN) to debut its first 100-plus-Mbyte ¼-in. tape drive in a 3½-in. format this month. The drive records 128 Mbytes on a single extended-length DC2000HD cartridge using a modified extension of the industry-standard QIC-100 data format. On the new unit, 3M has pushed data rates to 98.5 kbytes/s, roughly double the rates of its existing QIC-100 drives. Burst rates reach 750 kbytes/s.*—John Mayer*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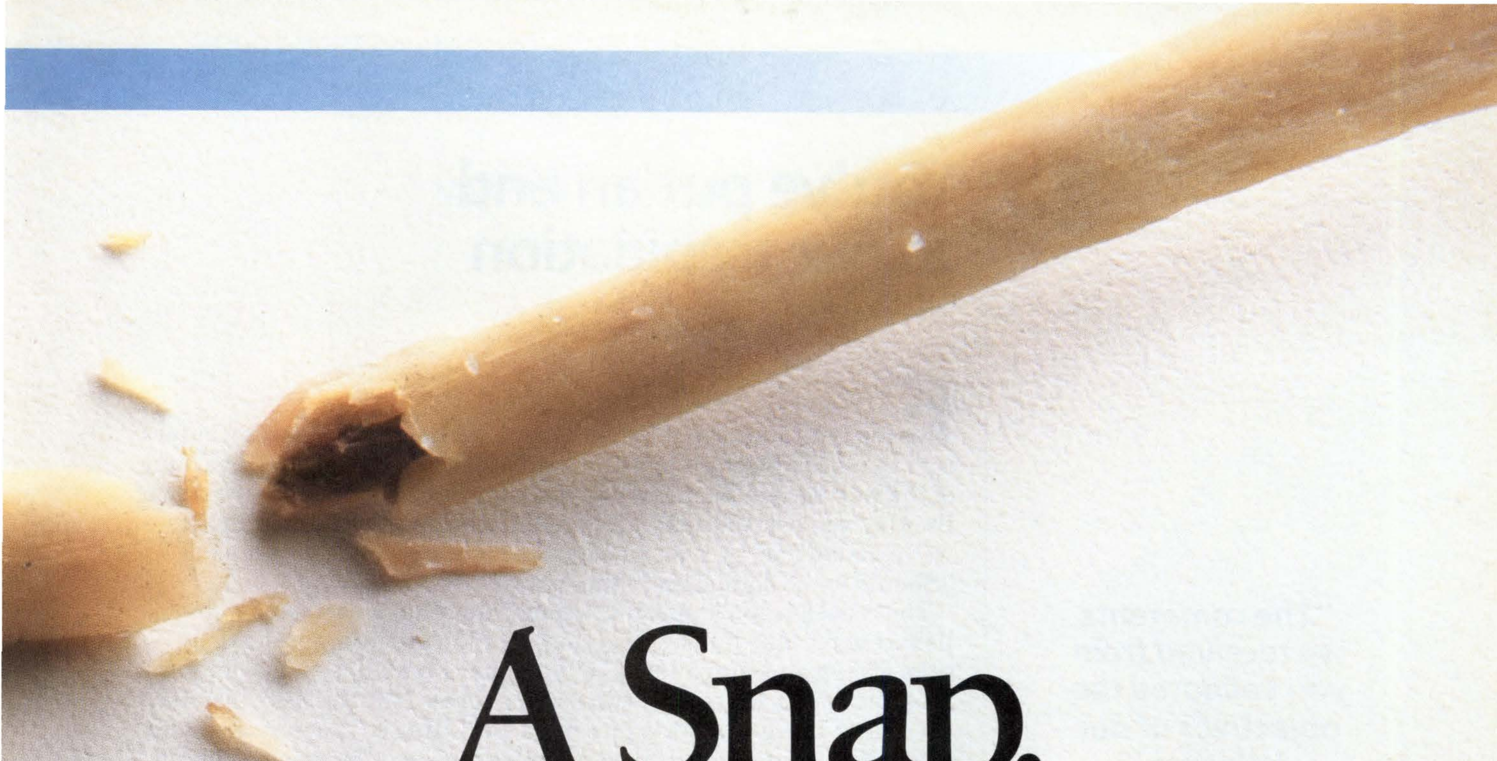

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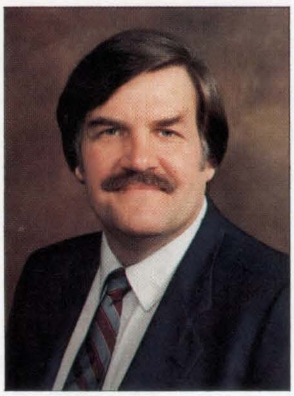
"The comments we received from you validated the objectives of our redesign."



John C. Miklosz
Associate Publisher/ Editor-in-Chief

Every editor (and publisher as well, perhaps even more so) enters into the redesign of a magazine with great trepidation and a variant of the well-known phenomenon of cognitive dissonance. Every step of the way, you ask yourself, "Will readers be upset with the changes we've made?" or, "Are we making the right changes?" or even, "Should we be doing this in the first place?"

The redesign of a magazine is something that editors and publishers don't take lightly. And they shouldn't redesign just for the sake of change—the changes that are made have to be made for good reasons. For us, there were two driving forces. The first was to make *Computer Design*'s appearance more appealing so that readers were more likely to pick it up (looks, feelings and emotions play a big role here, although most technical people don't like to admit it). Once those readers did pick up a copy, we wanted to make the information inside easier to access.

This issue is the fourth of our "new" *Computer Design*, and the comments we've received from many, many readers have banished any trepidation we may have had. A systems engineer from Detroit, for example, said, "I love it, especially the new cover and table of contents." The president of a computer company in Minneapolis said, "Love the graphic concept representations on the front cover." From a neighbor in Dedham, Massachusetts, we heard, "We do like the new, more readable layout. The contents page is much improved. But most important (for the technical area we work in), the information is uniformly clear and concise."

"I found it much better organized and easier to find articles specific to my interests," said one reader who didn't identify himself or herself, while another reader from College Station, Texas, said, "I want to read it again. The new design does make a difference in being able to quickly get the information needed from each issue. Terrific." Another anonymous reader commented, "The new look is clean, informative and easy to read. Good balance of flashy and traditional." Right on.

Not only did the comments we received from you validate the objectives of our redesign, but your input also highlighted some of the problems we were struggling with. For example, one reader noted, "You need to demarcate the columns and products better in the New Product Highlights section." We're acting on that, and you'll see the changes in the next issue.

There's really no way for us to express our thanks to all of the readers who took the time to write in their comments. Except to say, "Thanks," and offer to buy you a beer if you're ever in the Boston area. Or the next time you see us at a show or conference—Electro, Wescon, Buscon or DAC, for example—stop by and say hello. We'll buy you a beer then.

John Miklosz

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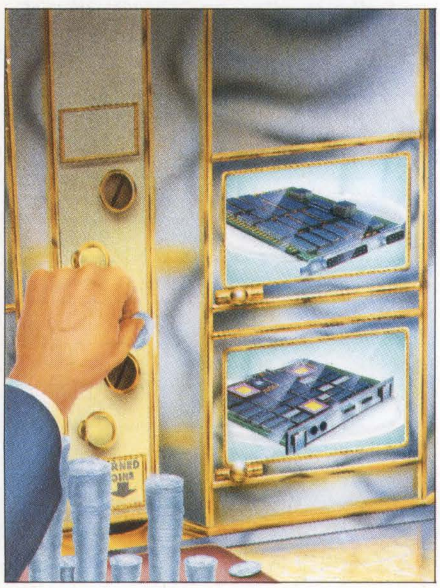
This issue's cover. . .



One of the hardest editorial concepts to illustrate is a buying guide or directory. Every idea under the sun has been used at one time or another, with conveyer belts, storage racks and cornucopias probably ranking as the most widely used and worn-out solutions that editors turn to in desperation.

By now, everyone who received the Sept. 1 issue of *Computer Design*, and the Buscon/East Preview that accompanied it, knows that Buscon/East is being held in New York next month—Oct. 4-6, to be exact. Maybe there was a hook here, we thought, and indeed there was. At one time, every visitor to New York made a point of stopping by one of several Horn & Hardart Automats scattered around the city. The Automats may have been the quintessential fast-food establishments serving New Yorkers a variety of foods—sandwiches, salads, soups and desserts—all displayed behind little windows and yours immediately for the right number of quarters. (And *long* ago, the right number of nickels). The variety of peripheral controller boards being served up today is far more impressive. But then, you need a lot more quarters.

Cover design by Sergio Roffo

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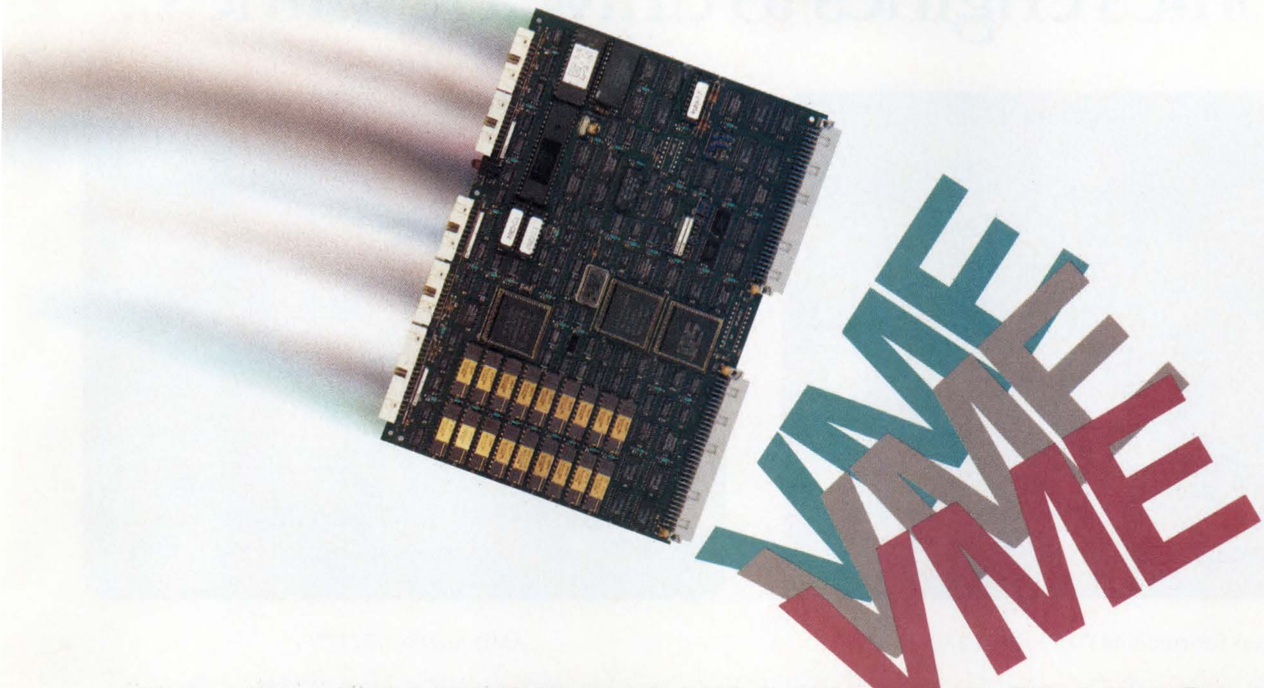

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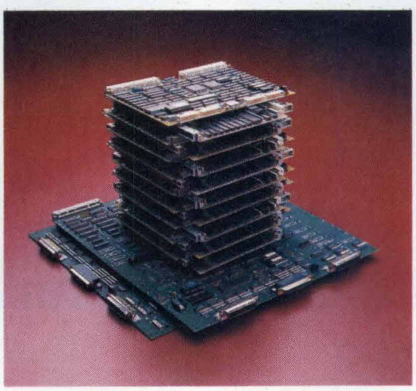

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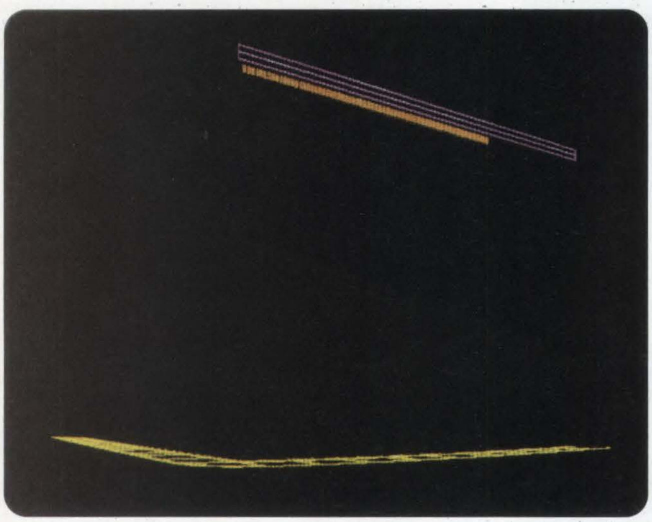

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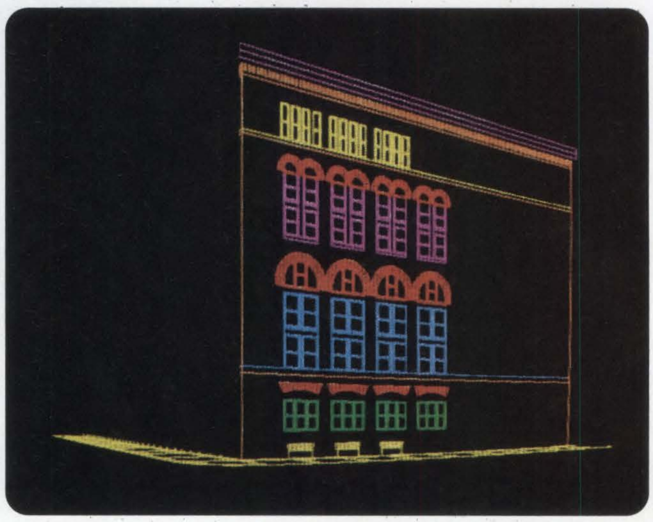

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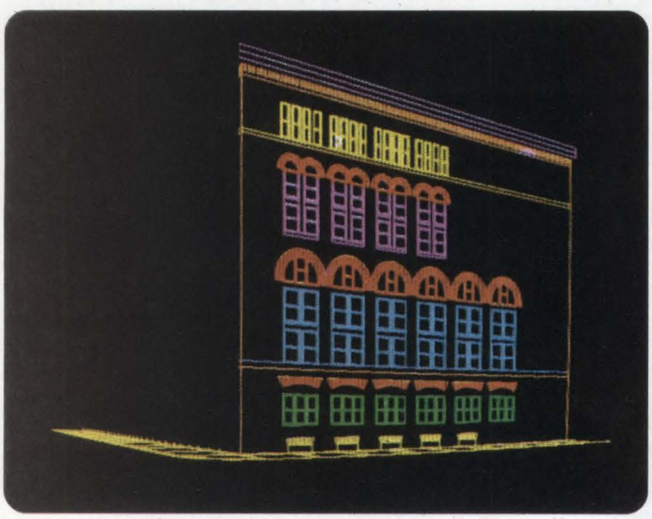

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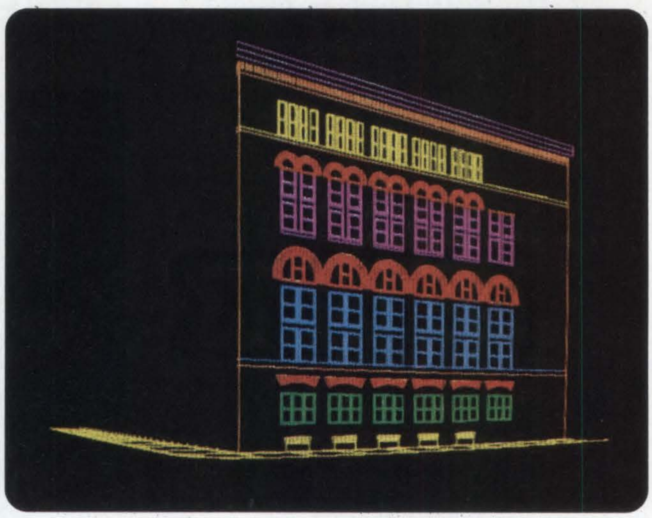

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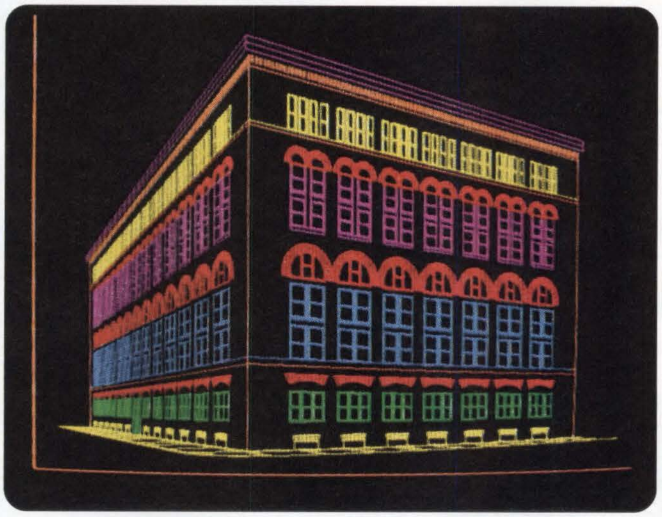

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COMPUTERS AND SUBSYSTEMS

NuBus picks up steam as first chips and cards emerge

Warren Andrews, Contributing Editor

While the fate of NuBus in the industrial market is still undetermined, there's a growing undercurrent of activity that could bring NuBus from a slow simmer to a boil at almost any moment. The first of the NuBus interface chips has just been introduced by Texas Instruments (Dallas, TX), with more to follow from VTC (Bloomington, MN) and others. And NuGroup, the recently formed trade association of NuBus vendors, is rapidly picking up members.

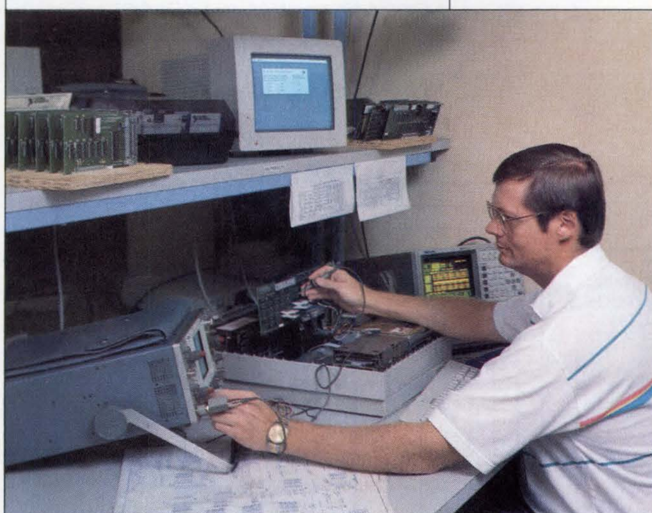
A technical committee within NuGroup is looking at a number of proposed additions to the specifications that, if implemented, should broaden the appeal and application of the bus. At the same time, members of the IEEE PC-Standards Committee have recommended NuBus as the route to ride for 32-bit personal computers. Finally, NuGroup members are gently applying pressure on Apple Computer (Cupertino, CA) by extolling the potential of the industrial open-bus marketplace.

Though the 32-bit NuBus was first conceived back in 1979—when there were scarcely 16-bit microprocessors, not to mention 32-bit devices—the way it handles addressing, arbitration and interrupt signaling places the NuBus in the ranks of such "advanced" buses as Multibus II and FutureBus. In addition, the NuBus interface is relatively clean and simple, compared with that of some of the other popular 32-bit buses, particularly VMEbus and Multibus II.

But despite the growing momentum, there are still a number of obstacles to overcome before NuBus can stand alone as a viable competitor in the 32-bit, open-bus market—either as an industrial bus or as the 32-bit PC standard. Except for those used in Apple's Macintosh II, there are few NuBus backplanes or CPU cards at hand. Some fundamental differences between the Intel 80XXX and Motorola 68XXX architectures (primarily byte ordering) will also make it difficult to swap Apple NuBus cards into PC-based NuBus machines (if they materialize).

■ Interface chips crucial

"It's vital that a bus architecture be supported with the appropriate interface chips," says Bill Nowlin, vice-president of engineering at National Instruments (Austin, TX) and head of NuGroup's technical committee. He cites how the Micro Channel had designers pulling out their hair trying to squeeze the required functions on the small board before interface chips became available.



Bus architectures like the NuBus must be supported with the appropriate interface chips, according to Bill Nowlin, vice-president of National Instruments and head of NuGroup's technical committee. Such chips are now starting to appear, with recent introductions from Texas Instruments and VTC.

With the introduction of its NuBus chip set, TI becomes the first IC vendor to support the bus. The set includes two types of chips: a 32-bit CMOS interface controller (the ACT-2440) and a 16-bit BiCMOS address/data transceiver chip (the BCT2420). A typical implementation calls for one interface controller and a pair of transceiver chips. According to TI, the chips replace as many as 45 of the discrete parts now needed for the NuBus interface function.

The chip set contains all the logic required for a master, slave and master/slave interface conforming with the IEEE P1196 spec. The interface controller handles signaling protocols and provides a simple connection to the NuBus backplane. The interface controller contains a master state machine, which performs arbitration and bus locking and unlocking. It also provides status bits for cycle control. In addition, the chip contains a slave state machine to monitor the NuBus status and notify the circuitry of the local board when it's being addressed.

TI's transceiver chip is fabricated in the company's BiCMOS process, which maintains the 24-mA drive required for NuBus while holding standby current to a minimum. It comprises bus transceiver circuits, D-type flip-flops, latches and control circuitry arranged for multiplexed transmission of address and data information across the NuBus. It includes an on-chip comparator to detect a NuBus transfer cycle requesting the local board. While designed to operate with TI's NuBus controller chip, the transceiver operates equally well with other ASIC- or PAL-based controllers.

"The availability of a standard interface solution for the NuBus backplane not only gives designers more room on the board, but dramatically reduces board design cycles," says Brian Kelly, strategic marketing manager for advanced bus interfaces at TI. Freed from the task of designing interface circuitry, designers have more time to focus on the specific board application and can get a product to market faster.

COMPUTERS AND SUBSYSTEMS

■ A second silicon effort

So far, the only other company with NuBus interface chips is VTC, which has completed design of a NuBus interface controller chip for one of its customers, reports product manager Jeff Hutton. He says the controller is similar in function to the one that's offered by TI. VTC will retain rights to the design and is deciding whether to bring the chip out as a standard product, according to Hutton. The first version is designed in VTC's VL2000 ECL standard-cell process. The bipolar process was required because the customer had specific military conformance and speed requirements.

When the chip was designed, says Hutton, VTC also designed a CMOS cell version of the product for the company's VL5000 cell library. But, says Hutton, there are no immediate plans to bring out the cell in a packaged version.

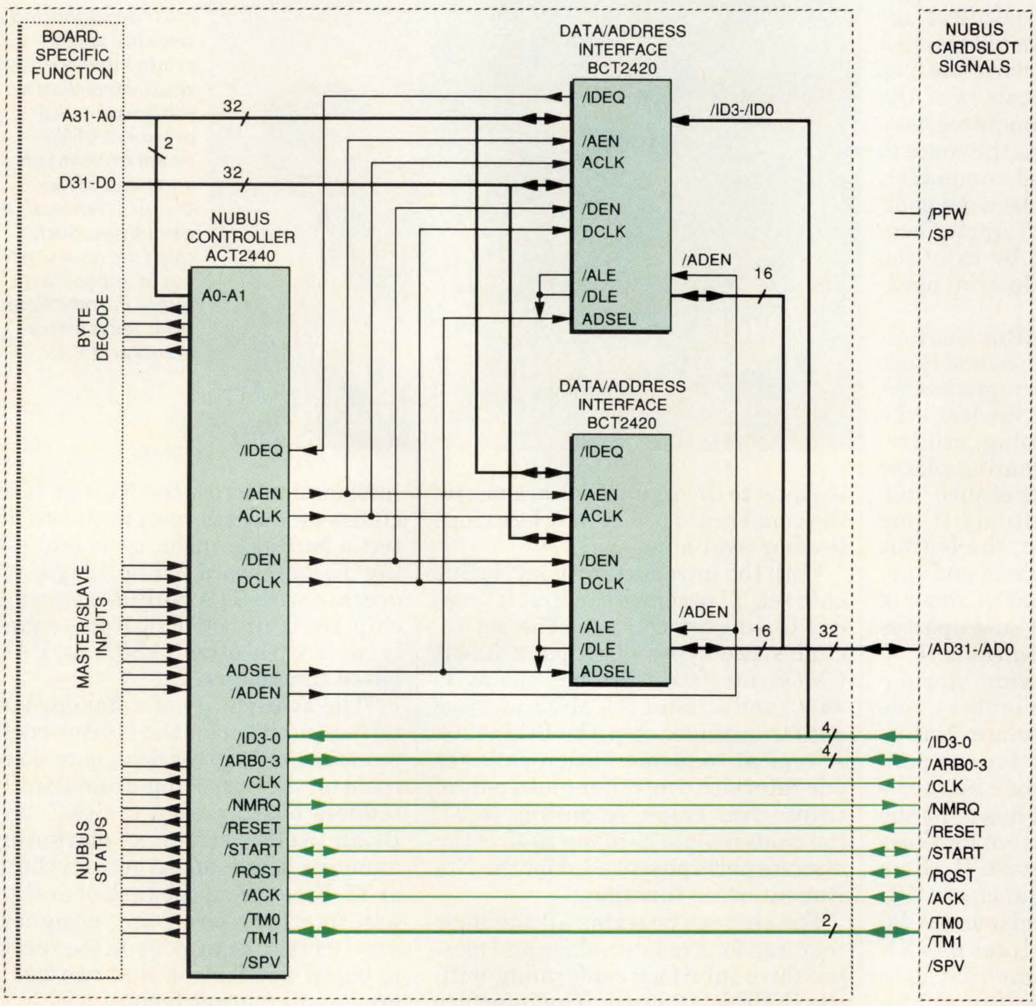
According to Hutton, the VTC-designed chip—as well as the TI chip set—are first efforts at providing some kind of NuBus silicon. Hutton believes that the bus interface will undergo a number of iterations before manufacturers settle on exactly what it is that they want. These and other issues, he hopes, will be ironed out by the technical committee in coming months. Looking at the bus's shortcomings today, Hutton sees little possibility that the interface function will remain the same for very long.

■ DMA controller possible

To permit the design of more sophisticated applications, TI added more status and control lines to the ACT-2440 than the IEEE P1196 specification calls for. Such functions may loom more significant as the NuGroup technical committee begins to define additions and modifications to the specification. These include enhancements such as defining multiprocessor communication—either memory-based, or message passing using block-mode transfers. Another proposal is the definition of backplane DMA transfers so that a DMA controller would be able to exist on the backplane.

In the present Apple NuBus configuration, there's no DMA controller.

A TYPICAL ACT 2440 NUBUS INTERFACE



In the Texas Instruments implementation of the NuBus interface, the controller chip directly interfaces with all the control signals on the NuBus backplane. Address and data lines are handled by the transceiver chips. Each transceiver has three 16-bit I/O ports and an on-chip comparator for backplane and slot identification.

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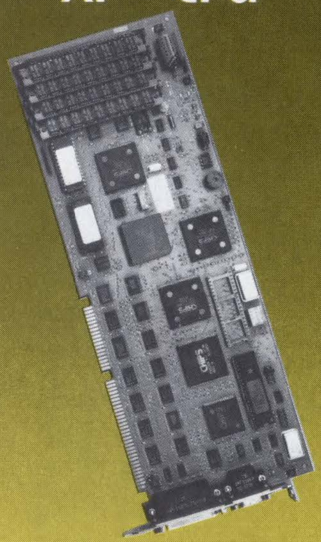

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CIRCLE NO. 14

To use DMA, an add-in board must be a master: it must take control of the bus and implement its own DMA transfer. This requires the add-in card to have its own DMA controller circuitry and adds to the complexity of the bus interface. At this point, NuBus slave cards have no DMA capability. To work around that, vendors have had to include buffer memory on add-in cards. A DMA controller on the backplane would eliminate the problem.

The NuGroup committee is also looking at defining event cycles in regard to multiprocessing communications. "These are generally software issues that deal with expanding the scope of NuBus to more and larger applications," says Nowlin.

CPU cards appear

Despite all the smoke, there's been little fire behind NuBus as anything other than an Apple platform. To date, just about all of the NuBus cards available, or under development, are enhancements to the Mac II. Some key events that will force a change, says Nowlin, will be the introduction of stand-alone CPU cards and perhaps passive backplanes. The first such stand-alone card made its debut at MacWorld last month in the form of an Apple format card and backplane from Second Wave (Austin, TX). The card sports a 68000 family processor.

Other CPU cards, though not necessarily stand-alone system cards, have also recently emerged, including two RISC-based cards. One, from Tektronix (Beaverton, OR), uses the Motorola 88000. The coprocessor board boasts a 17-VAX-Mips rating, almost 10 times that of the Mac itself. It gets its performance from a 20-MHz MC88100 CPU and three MC-88200 CMMUs (partitioning two caches for code, one for data) and has 8 Mbytes of dynamic RAM.

The other coprocessor board, from YARC Systems (Thousand Oaks, CA), packs a 25-MHz Am29000. The board is expected to reach or top the performance of the Tektronix 88000-based card. Running C, benchmark tests indicate that the YARC board can deliver up to 30,000 Dhrystones. In addition, the company claims that up to four coprocessor boards can be dropped into the Mac II NuBus slots for a potential combined performance of 68 Mips.

A redefined format?

Though originally defined as a triple-high, triple-connector Eurocard form-factor, Apple redefined NuBus to fit a PC-sized format, where most of the interest now lies, according to Nowlin. However, he adds, the technical committee would be willing to entertain proposals to redefine the bus to a double-high Eurocard. "Right now, though, there's no indication that anyone's interested," he says. Others peripherally involved with NuBus believe the PC format card will become a commodity item. Until NuBus settles on an industrial card format (preferably 6U Eurocard), they say most industrial card makers won't participate in the NuBus market.

For the short term, many applications will have to wait until NuBus reaches some kind of critical mass.

■ ■ ■

The bulk of applications for NuBus have revolved around the Apple Mac II platform as used in anything from desktop publishing to instrumentation and workstation front ends. Obviously the deal penned earlier this year between Apple and Digital Equipment Corp (Maynard, MA) has loosed many DEC front-end applications for Apple machines—so much so, in fact, that the DEC sales force has been authorized to sell Apple machines.

However, says Nowlin, "We're starting to see an increasing number of people looking at stand-alone NuBus systems for more industrial and test-and-measurement applications." For the short term, though, many applications will have to wait until NuBus reaches some kind of critical mass. How soon it can develop a strong following of vendors offering a variety of cards will determine when—and if—NuBus will join the mainstream of open-architecture buses□

Credit card-sized XT mother board introduces DOS to embedded systems

Tom Williams, Western Managing Editor

Numerous factory-floor control systems, medical instruments and clusters of electronic instrumentation are controlled and monitored by an IBM PC or compatible. Even real-time control systems that use dedicated microcontrollers to monitor critical processes need a user interface, which is often provided by a PC attached to the system. Such systems also require an increasing amount of flexibility for programming at the functional level to retrieve and analyze data that's been acquired by a real-time system or to set parameters for process monitoring. But PCs are bulky, aren't protected against harsh environments and represent a cost factor the system designer would like to reduce.

The Wildcard 88, recently introduced by Intel (Santa Clara, CA), lets OEM system designers embed DOS functionality into all kinds of equipment, from consumer products to medical and industrial instrumentation. The Wildcard incorporates all of the core logic found on a 48-in.^{2} IBM PC XT mother board onto a circuit board measuring 8 in.^{2} All connections for I/O, memory, power and control interface are brought out to a 68-pin card edge connector that plugs into a standard high-density single in-line module (SIM) connector.

The board space was reduced through a chip-on-board technique in which the IC die was wire-bonded directly onto the circuit board and then covered with a layer of epoxy. This technique was accomplished by using an 80C88 CMOS microprocessor and an application-specific IC designed to incorporate memory refresh, interrupt, timer/counter and clock functions. Clock speed is 7.15 MHz, but is software-switchable to the XT standard 4.77-MHz frequency.

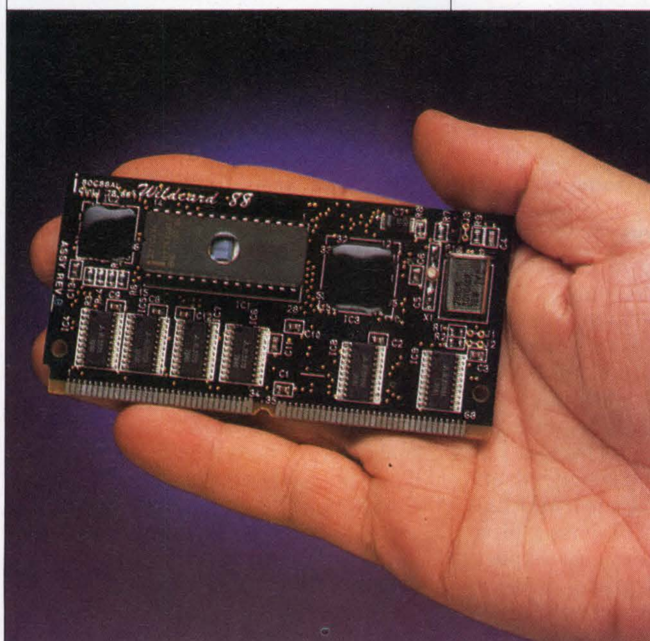
Various approaches use DOS

Although there's plenty of space on the back of the board, Intel hasn't incorporated any system memory on the card. There simply was no incentive for the company to include memory, according to product manager Dirk Smits, since Intel no longer makes memories. Memory can be added via SIM memory modules to the system being designed.

The Wildcard carries a socket for a ROM BIOS that's supplied by Phoenix Software (Norwood, MA) and Award Software (Los Gatos, CA). Since the card is 100 percent XT-compatible, designers will take different approaches to incorporating DOS in their systems. The easiest way, of course, is to include a floppy drive and boot DOS, just like in a desktop PC. That solution, however, is undesirable in portable equipment.

Instead, ROM or battery-backed RAM cartridges can be used, as well as credit card-sized memory cards such as the Star Card from ITT Cannon (Santa Ana, CA) and the Melcard from Mitsubishi (Tokyo, Japan). The latter two options are available in EPROM, ROM and RAM configurations, letting designers mix and match memory and embedded software. These memory cards also have the added advantage of being about the same form factor as the Wildcard. In addition, there's a ROM version of DOS, DR-DOS, available from Digital Research (Monterey, CA)

Smits is careful to point out that the embedded PC functionality isn't intended for real-time control, but is more of a monitor. It lets users interact with the system in terms of familiar DOS functions or some specialized user interface, such as graphics instrument symbols. It also allows programming of system functions, which may include real-time control. In addition, DOS compatibility allows incorporation of off-the-shelf applications, such as spreadsheets, for data analysis in specialized equipment. A lot of software development can also be done off-line on a normal desktop XT or compatible and moved directly to the target equipment.



At only 2 × 4 in., the Wildcard 88 holds all the core logic of an IBM PC XT mother board, letting OEMs incorporate DOS functionality into a wide range of intelligent systems. A CMOS 80C88 processor and an integrated peripheral controller chip are mounted directly on the board and encased in epoxy.

Intel supplies a prototyping board with connections for a power supply, a keyboard, several SIM connectors and three XT card slots. Presumably, a system designer could prototype his system, develop software and then make the decision whether to use off-the-shelf cards, such as I/O boards or display controllers, or to fold the desired functionality into a more compact special circuit board for the final design. □

COMPUTERS AND SUBSYSTEMS

Advanced peripheral interface finally arrives in VMEbus controller

David Lieberman, Senior Editor

In development since 1980, the Intelligent Peripherals Interface (IPI) was finally completed in 1986, a year that also brought a host of new product preannouncements. It's only now, though, with this month's introduction of the V/IPI 4260 Cougar IPI-2 controller for the VMEbus from Interphase (Dallas, TX) that the new interface has become accessible via an off-the-shelf controller board for one of the popular industry-standard buses.

Why such a delay? "The market stalled dead in its tracks because available IPI disk drives were no faster than SMD drives," explains Dal Allan, president of ENDL Consulting (Saratoga, CA) and a principal player in the development of IPI. The first-generation IPI-2 drives from Control Data (St. Paul, MN), Fujitsu America's Storage Products Division (San Jose, CA) and NEC Information Systems (Boxborough, MA) looked, with their 2.4- to 3-Mbyte/s data-transfer rates, like "warmed-over SMD drives," according to one observer, and they gave designers little incentive to make a change.

There's a clear, conservative engineering rationale for the SMD-like transfer rate of early IPI drives, however. They let designers gain experience with the new interface—its command and response structure, for example—without having to simultaneously deal with a heightened data rate. "You want to treat a new interface very cautiously," says Michael Gamerl, product line manager for IPI-2 products at Fujitsu. "The more new variables you crank into a new product, the greater the headache."

It's only recently that IPI drives have been shipped in any appreciable volume, and demand for data rates above 3 Mbytes/s still isn't great, according to Ralph Funk, director of disk marketing at NEC Information Systems. As David Ujita, marketing manager for the Computer Division of Hitachi America (San Bruno, CA), sees it, IPI lacks any significant market growth because its performance capabilities aren't required. "Few systems can operate with a 10-Mbyte/s storage subsystem," he says.

The performance edge

Why bother with IPI, then, at this point in time? "It's a clear upgrade path that positions you for future growth," says Ernest Godsey, Interphase director of product marketing. "The drive manufacturers have said in no uncertain terms that they're going to blow right past 10 Mbytes/s."

NEC has already achieved a 4.5-Mbyte/s rate, soon to be designed into its IPI drives, by pushing disk bit density out to 32,000 bits/in.; and Control Data has doubled its rate to 6 Mbytes/s by allowing two read/write heads on its drives to read or write simultaneously. "Now that drive vendors are finally cracking the 3-Mbyte barrier," says Allan, "there's a good rationale for moving to a new generation of controllers." With a few firmware timing changes, the Cougar will be available to accommodate the coming IPI drives.

Even at 2.4 or 3 Mbytes/s, IPI be-

The IPI hierarchy

The Intelligent Peripherals Interface (IPI) is a multileveled interface consisting of IPI-1, the physical interface shared by IPI-2 and IPI-3; IPI-2, a device-level, or "system-specific," interface; and IPI-3, a host-level, or "system-generic," interface. While IPI-2 and IPI-3 can, but don't have to, coexist, most of the IPI market activity of the past two years has involved IPI subsystems that package multiple large drives with an IPI-3 interface that hides the device-level interface—IPI-2 or SMD—from the host system, typically a mainframe or minicomputer.

Although IPI is most applicable for large disk drives, Jim Patton, manager of product marketing for Micropolis (Chatsworth, CA), reports that there's "strong sentiment in isolated places" for an IPI-2 interface on 5¼-in. drives. The amount of electronics required to implement an IPI-2 interface exceeds practicality for a small drive, however, and the arrays of small disk drives the company has begun selling are better managed by an intelligent buffered interface such as IPI-3. "We can provide an IPI-2 interface if the customer insists on it," says Patton, "and that customer is usually a systems house, which typically believes that it can build its own controller better than anybody else."

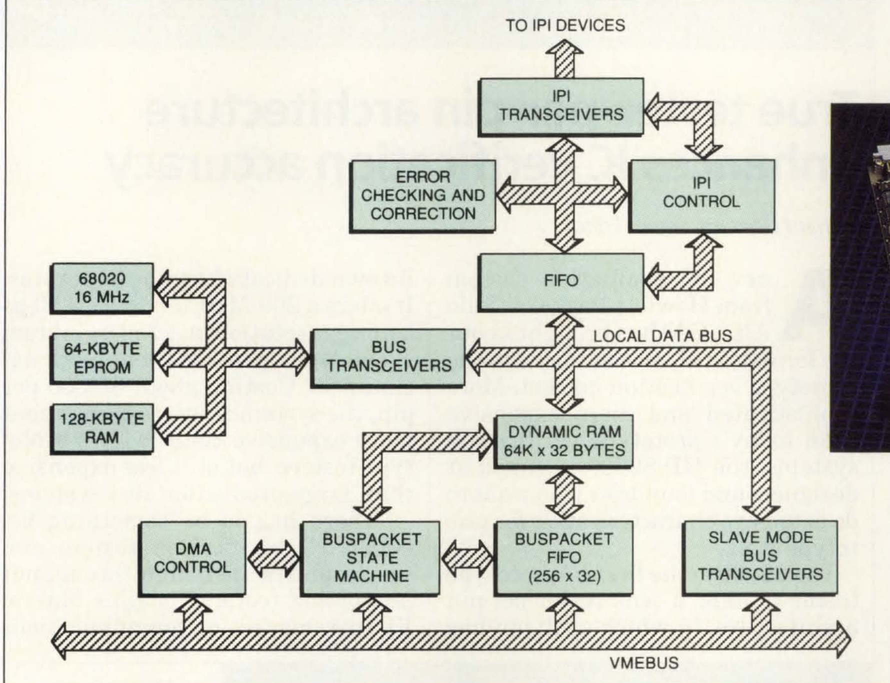
Just as early IPI-2 drives haven't pushed the capabilities of that interface, most of the early IPI-3 implementations have also taken a one-step-at-a-time approach. While the intelligence inherent in IPI-3 can decouple the host from disk-related operations, most vendors have not taken advantage of this. "While one approach to IPI-3 is very rich and scales the interface to the kind of performance that customers demand," says Dal Allan, president of ENDL Consulting (Saratoga, CA), "the more common approach scales the interface to the characteristics of the existing operating system." That is, large computer manufacturers are first putting IPI hardware out on the customer's floor and will eventually make the software architecture changes the interface allows.

Like the small computer system interface (SCSI), IPI is defined as a general-purpose peripheral interface with the Winchester disk drive as its initial peripheral target. The IPI-2/IPI-3 combination lets some very large and diverse peripheral subsystems be configured—with, for example, as many as eight controllers managing as many as 16 peripherals, for a 128-peripheral system. In the long run, according to Ernest Godsey, director of product marketing at Interphase (Dallas, TX), this capability plus the ability to mix IPI-2 and IPI-3 devices on a single cable will offer unprecedented system configuration opportunities in the future. "Once there's a greater variety of IPI peripherals and controllers available, we'll start seeing people getting very creative in how they organize their total system architectures," he says.

gan its functional life at the outer reaches of SMD performance. Initially defined with a maximum data-transfer rate of 1.8 Mbytes/s, the serial SMD interface has been pushed as far as 3 Mbytes/s over the years by means of ECL driver and receiver technology. Yet, the 24-MHz clock frequency of the most advanced SMD interfaces is something of a strain on the reliable transmission of data.

"You have to be very careful with high-performance SMD as far as grounding is concerned," says Gene Velaski, field-support engineer at Control Data. "While shielded I/O cables used to be a good idea, with today's faster clock frequencies, they're an absolute necessity."

THE COUGAR IPI-2 CONTROLLER



Interphase's Cougar IPI-2 controller for the VMEbus uses the company's familiar Buspacket Interface and intelligent software interface, but with an expanded 256- or 512-kbyte dynamic RAM caching buffer and a 32-bit internal data path that boosts burst-transfer rate capability across the VMEbus to 36 Mbytes/s.

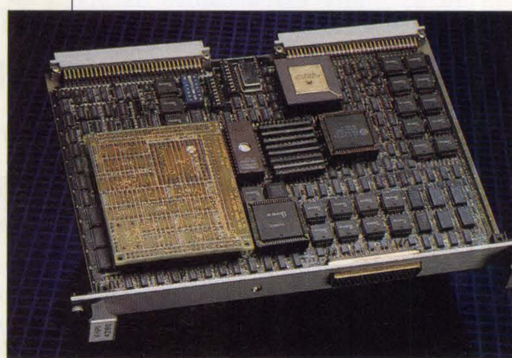
More than sheer speed

As a double-byte-wide parallel interface, IPI can achieve the same data rates as serial SMD with a far lower clock frequency and, hence, less potential electromagnetic and radio-frequency interface difficulties and greater margin for error. It can also reliably accommodate far higher transfer rates: up to 10 Mbytes/s as initially defined. The benefits of IPI over SMD, however, extend beyond sheer speed. "I'm afraid that by looking at just the speed differential, the industry is being myopic," claims Gamerl. "IPI has far more to recommend it than just faster transfers."

IPI, for instance, uses a single 50-conductor cabling scheme compared to SMD's separate 60-conductor and 20-conductor cabling for control functions and data transfers, respectively. SMD also requires a separate data cable for each disk drive in a subsystem, while IPI lets 16 drives be daisy-chained on one cable. Thus, while state-of-the-art SMD controllers typically manage four drives, the Interphase IPI controller manages eight. "Using a single cable is very cost-effective," says Gamerl, "and you don't have the packaging problems of stacking cables side by side and blocking air flow that you have with SMD."

"To manage eight SMD drives, we'd need nine cable connectors on the controller board," says Interface's Godsey, "while IPI needs only one. When you're talking about a board as small as a VME card, you can't afford to fill up half the card with connectors."

An IPI link can also reach to about 164 ft, compared to about 50 ft for SMD, giving IPI more configuration flexibility. "Everybody thought file servers would be small devices placed close to a computer," says Gamerl. "But, for example, with the vast amounts of CAD data they're being called on to store, they've gotten pretty big, noisy and hot, and you want to locate them remotely in a closet. IPI's 164 feet gives you a lot more opportunity to find that closet."



IPI also has the smarts that SMD lacks. "Lack of status information is a long-standing complaint about SMD," says Gamerl. "SMD gives you 5 bits that say 'fault,' and you have to take the drive off-line and test it if you want to know what went wrong." IPI, in contrast, provides "all the status information you'd ever want to use," he adds. It also provides an abundance of configuration information, while SMD only reports a "ready" condition.

IPI also specifies methods of defect handling so that a drive's defect map can be loaded into RAM without the time-consuming manual entry procedures necessary with other interfaces. In addition, it incorporates a rotational position-sensing capability to inform a controller of head location. And since data is converted from serial to parallel format before it crosses the interface, features such as error checking and correction can

COMPUTERS AND SUBSYSTEMS

also be implemented in the drive. One noteworthy IPI feature—defect swallowing—lets the drive "leap over" known media flaws, rather than waste disk space and access time by assigning an alternate track.

■ One-Mbyte/s-per-pin rate

Despite limited market activity, IPI hasn't stood still since 1986 in terms of technical specs. As Allan reports, IPI committees have pushed the transfer rate out to 25 Mbytes/s with existing TTL drivers and receivers and to 50 Mbytes/s with ECL. "We've also defined a new 100-pin option to double these rates to 50 and 100 Mbytes/s and defined the ability to add as many extra cables as you want," he says. "So if you want a 1-Gbyte/s transfer rate, you need 10 cables. Basically, what enhanced IPI can get you is 1 Mbyte/s per pin."

The extension of IPI to ever higher data rates, however, will eliminate part of its reliability advantage over SMD. "As we pass 10 Mbytes/s," says Interface's Godsey, "the signal rate of the cable comes right back up again, so reliability will be a short-lived advantage. If you're running 24 MHz on a cable, you're running 24 MHz on a cable. I don't care if it's 16 bits wide or single wide or whatever; the physics are the same."

In the future, SMD reportedly will also be stretched even further, to 32 or 36 MHz or at least to 4 Mbytes/s, according to Control Data's Velaski. But, Allan cautions, "That's going to be a tough squeeze. The rise and fall times on current drivers and receivers are pretty tight already, and we're really squeezed for margin at 3 Mbytes/s. Taking it any further is a risk factor: in a worst-case analysis, it simply won't work."

NEC's Funk agrees. "There may be clever ways to make a 4-Mbyte/s SMD work, but if this involves continuing to decrease cable lengths, it doesn't sound like a good idea," he says. "In general, we wouldn't want to support that because enough major systems people are implementing IPI-2-compatible controllers."

Hitachi's Ujita expects to see a lot of IPI action within about three years. "It's the up-and-coming interface," he says, "still relatively young and untouched, but with great potential. It's somewhat analogous to erasable optical disk drives, with an early burst of activity, but without the performance edge to replace an alternative technology."

Funk expects IPI activity to accelerate within the next few years as accelerating I/O requirements outstrip the practical capabilities of SMD. "As the faster drives and then the controllers come out, there will be an avalanche effect caused by the transfer rate issue and the need for higher I/O throughput," says Funk. "But even if the rest of the year's orders for new computers were for IPI-2 drives, in terms of total drives shipped, it will still be three to five years before IPI represents a high percentage of drives shipped. Most new contracts within the last year have been for SMD and will have a shipment life of four to five years. It takes a long time for shipment volume percentages to cross over." □

DESIGN AND DEVELOPMENT TOOLS

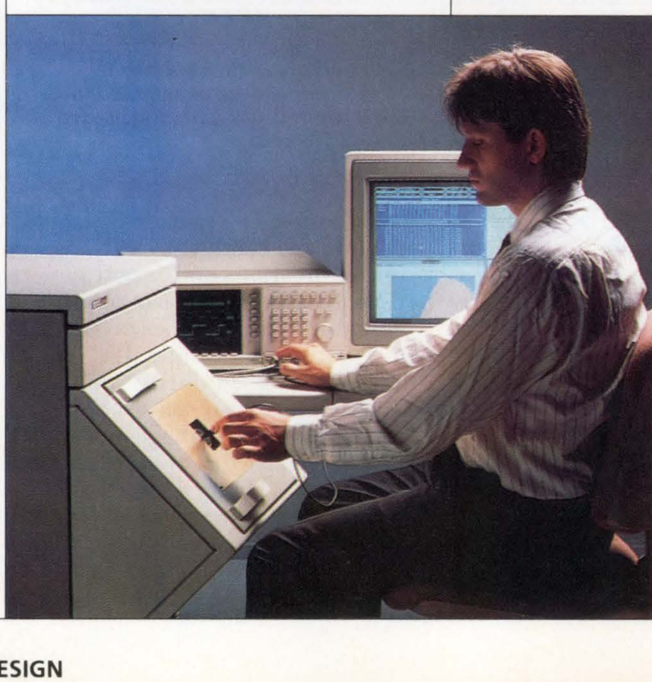
True tester-per-pin architecture enhances IC verification accuracy

Richard Goering, Senior Editor

A new IC evaluation system from Hewlett-Packard (Palo Alto, CA) has brought about the formation of another niche in the prototype-verification market. More sophisticated and more expensive than today's prototype verification systems, the HP 82000 is aimed at designers and foundries who want to do extensive characterization for prototype ICs.

The 82000 is the first IC prototype tester to offer a true tester-per-pin architecture, in which each pin has its own dedicated timing generator. It offers a 200-MHz test rate, a 50-ps timing resolution, a ±250-ps system skew and up to 384 bidirectional channels. Costing about $3,000 per pin, the system is two to three times more expensive than today's prototype testers, but still less expensive than large production test systems.

"There has to be something between IC verification testers and very sophisticated, high-throughput production testers," claims Martin Kellner, marketing communications



The first IC prototype tester to offer a true tester-per-pin architecture, the HP 82000 from Hewlett-Packard has been developed for designers with extensive characterization needs. Priced at around $3,000 per pin, the system features a 200-MHz test rate and a ±250-ps system skew specification.

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CIRCLE NO. 15

manager for HP's Boblingen Instruments Division (Boblingen, W Germany). "Users want to characterize devices as well as verify them. They want to define the limits of their device, vary parameters and get immediate results."

The introduction of the 82000 follows a great deal of speculation about HP's plans in the prototype-verification market. The system represents a more integrated solution than HP's 81810S, which is basically an instrument cluster that includes a data generator, a data analyzer and a dc parametric unit. And the 82000 portends a much stronger thrust by HP into the prototype test market.

■ 1,000 timing generators

IC prototype testers from such manufacturers as Integrated Measurement Systems (Beaverton, OR) and Hilevel Technology (Irvine, CA) offer a shared-resource, or "per-pin," architecture, in which a limited number of timing generators can be assigned to individual pins. These testers also let voltage drive levels, data formats, masking, inhibiting and tristating be assigned to individual pins. But the 82000 is the only prototype tester offering a dedicated timing generator behind every pin.

The 82000 actually supplies four edge generators for every pin, providing a leading and trailing edge for both drivers and comparators. "That gives us 1,024 timing generators in a 256-pin system," says Matthias Stahl, product manager for IC test at the Boblingen Instrument Division. "And the same is true for voltage levels—you can individually define high and low voltage for both drivers and comparators."

Because each pin has its own timing generator, the user can calibrate every channel independently, thus providing better accuracy than that offered by a shared-resource architecture. And information from the logic-simulation environment can be transferred to the tester on a true signal-to-pin basis. "We don't run into the problem of having 50 different timing requirements from the simulator but only 12 timing generators in the tester," says Stahl.

> ***"There has to be something between IC verification testers and very sophisticated, high-throughput production testers."***
>
> *—Martin Kellner, Hewlett-Packard*

HP now provides interfaces to the System Hilo simulator from Genrad (Concord, MA), which is also sold by HP, as well as to simulators from Mentor Graphics (Beaverton, OR) and Daisy Systems (Mountain View, CA). In addition to transferring the data, 82000 software can automatically generate a complete test program with timing, formatting and parametric data.

■ Compromises at 200-MHz rate

The 200-MHz test rate offered by the 82000 is almost double that of any competing prototype test system, but some compromises are involved. The 200-MHz rate is either multiplexed, which halves the channel count, or it offers a reduced selection of timing formats and doesn't allow tristate capabilities. A 100-MHz rate is available with no limitations.

While ac and dc parametric capabilities of the 82000 are comparable to other prototype-verification systems, the system's 50-ps timing resolution offers a new level of accuracy. And its $\pm$250-ps skew specification compares favorably with the $\pm$1-ns skew specifications available on many prototype-verification systems.

The capabilities of the 82000 make it a good candidate for low-volume production test, and HP will address that area as well. For the average application-specific IC designer, it's probably overkill—but for designers pushing the limits of technology, it could open new horizons for verification and characterization. □

Compiler provides logic synthesis from hardware description languages

Richard Goering, Senior Editor

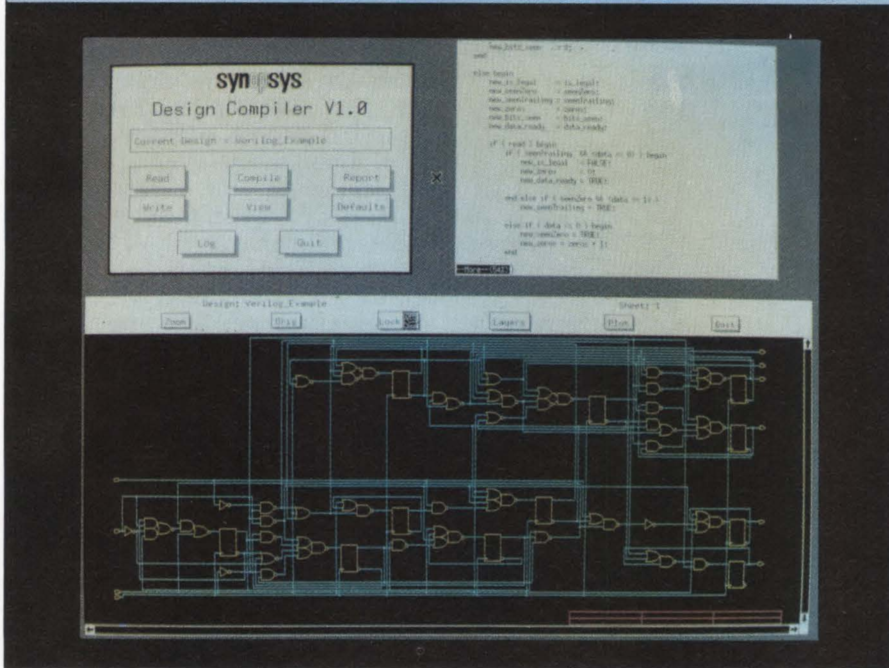
Hardware description languages are great for specifying system-level behavior, but sooner or later the design must be broken down to the gate level. This painstaking process can be dramatically shortened with the HDL Compiler from Synopsys (Mountain View, CA), a new program that allows logic synthesis directly from hardware description languages.

The HDL Compiler now supports the Verilog hardware description language from Gateway Design Automation (Westford, MA) and will support other languages in the future. This compiler acts as a translator for the Design Compiler, a logic-synthesis program introduced by Synopsys in June. Available on Apollo and Sun workstations, the Design Compiler automatically generates gate-level net lists and schematics. It then optimizes net lists for area and timing, and maps logic into specific application-specific IC cell libraries.

Verilog offers design descriptions and simulation from the abstract architectural to the gate level. Synopsys' HDL Compiler can accept Verilog descriptions at the register-transfer level, which lets engineers behaviorally describe blocks such as counters, decoders and registers. "Designers are comfortable working at the register-transfer level," says Aart de Geus, vice-president for research and development at Synopsys. "It's a nice step away from gate-level implementations, yet you still have enough control over the architecture so you can assure high quality."

■ Substantial productivity gains

Because it's much easier to work at the register-transfer level than at the gate level, the HDL Compiler promises enormous productivity gains. It



The HDL Compiler from Synopsys provides logic synthesis from the Verilog hardware description language. An optimized, gate-level net list can be automatically generated from a register-transfer-level description in Verilog.

lets designers quickly explore alternative architectures and evaluate their impact on die size and timing. In addition, the use of a hardware description language creates an implicit documentation methodology.

In a real-world example, Synopsys synthesized a 3,000-line Verilog description developed by Sun Microsystems (Mountain View, CA) for a 25,000-gate array. The design was optimized for area in one-half hour of CPU time, and the result was 17 percent smaller than the original circuit. Timing optimization is a much more difficult problem, however—it took 10 hours of CPU time, and the results were comparable to those of Sun's designers.

Synopsys ran into a few problems that delayed the synthesis process. Because the behavioral model wasn't up to date with the net list, the test vectors didn't match the simulation results at first. An asynchronous clocking scheme also required extra work. Even so, Synopsys programmers completed in days a process that took Sun several months. "This tool will be much more effective in the hands of the original designer," says de Geus.

The Synopsys HDL Compiler takes the full register-transfer-level description from Verilog and factors out simulation-specific constructs. Both sequential and combinational logic can be synthesized. The user provides a separate file that specifies, and gives relative weightings to, area and timing constraints.

Future support for VHDL

Synopsys chose Verilog because the language is now popular for designing ASICs, and it has a simulation capability. In the future, however, support for the VHSIC Hardware Description Language (VHDL) will become important. While Verilog is a proprietary language, VHDL is on its way to becoming an industry standard. Since VHDL is an extremely rich language, it may be necessary to identify a subset for synthesis.

In order to develop synthesis from VHDL, Synopsys competitor Silc Technologies (Burlington, MA) recently signed a technology agreement with Vantage Analysis Systems (Fremont, CA), a new company that sells a VHDL simulator. The two companies will provide an interface that will let users describe designs in VHDL and generate gate-level logic with Silc's Silcsyn product.

Both VHDL and Verilog permit high-level behavioral descriptions, and synthesis will someday be possible at such levels. De Geus speculates that high-level behavioral synthesis will be aimed at specific types of architectures, such as digital signal processing or filters. Meanwhile, register-transfer-level synthesis is an intermediate step that can boost productivity, yet still let engineers control the structural implementation of designs. □

Synopsys' HDL Compiler can accept Verilog descriptions at the register-transfer level, a level at which designers are comfortable working, according to Aart de Geus, vice-president for research and development at Synopsys. "It's a nice step away from gate-level implementations, yet you still have enough control over the architecture so you can assure high quality."

INTEGRATED CIRCUITS

Designers debate advantages of EDACs in small systems

Ron Wilson, Senior Editor

Error detection and correction circuits (EDACs) for dynamic RAMs are a common feature in mainframe computer memory architectures. Now, larger microcomputer memory systems and new EDAC parts are conspiring to move the technique of memory error detection into the world of deskside and desktop machines. Some designers, however, still question the cost and speed implications of EDACs in small systems.

In smaller systems, memory error detection usually consists of a parity-checking circuit, which simply interrupts the CPU when a byte containing a parity error is read. This feature first became an established fixture in personal computers with the introduction of the IBM PC. "Once IBM does it, everybody has to. So all PC chip sets have parity generation and detection," says Sikander Naqvi, marketing manager at Chips and Technologies (Milpitas, CA).

But PC-sized systems generally don't use more sophisticated, multibit error detection and correction techniques. "The probability of failure is very low in systems with only 2 or 4 Mbytes of memory," explains Naqvi. "In addition, correction isn't generally a big issue in single-user systems. If there's a bit error, the system stops, and the user just starts it up again. There isn't any demand for absolutely failure-free operation."

■ EDAC improves the odds

Most observers agree that EDAC is overkill for PCs. But the two factors cited by Naqvi—memory size and the cost of a failure—work together to make full correction more attractive in medium-scale systems. Department-level computers, for example, which are now often implemented with microprocessors, can have large physical memories and a great number of simultaneous users. "There's a fundamental fear of rebooting," claims Chris DeMonico, strategic marketing manager for VLSI logic products at Texas Instruments (Dallas, TX). "The reliability of DRAMs has actually improved a great deal. But the number of DRAMs in a memory has increased. More important, when a multiuser system goes down, it can be devastating to a department. So when you multiply the probability by the number of chips and the cost of failure, it can work out to be worthwhile to use EDAC hardware to improve the odds."

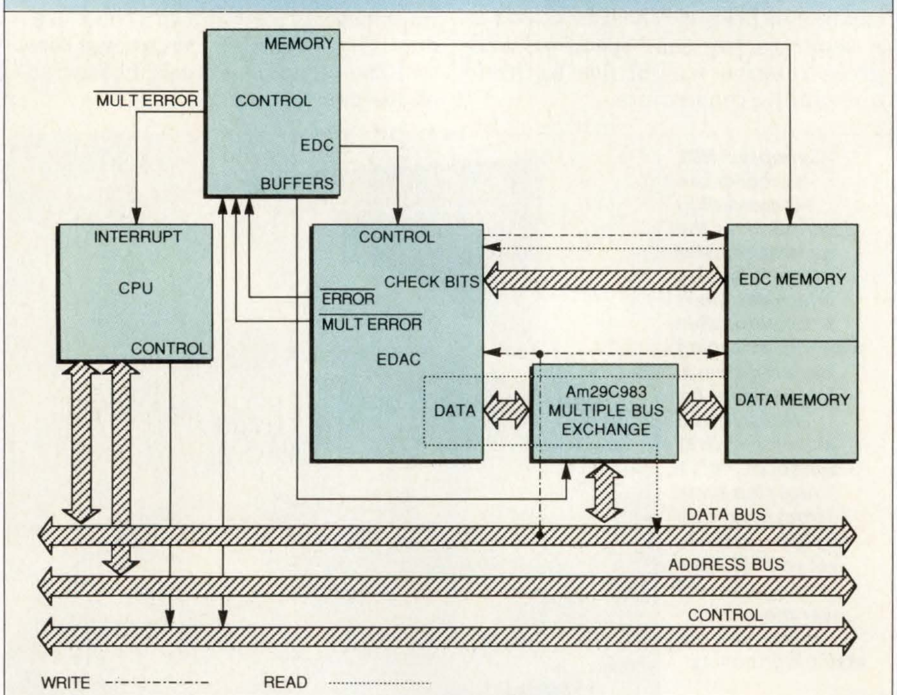
EDACs better the odds by correcting the errors that can spontaneously occur in DRAMs. "Noise, supply glitches, even alpha particles can cause a DRAM cell to spontaneously transition from 1 to 0," explains DeMonico. The EDAC helps with this problem via a two-step process. When a word is written into memory, the EDAC generates from the word a pattern of check bits: 7 bits for a 32-bit word, or 8 bits for a 64-bit word. When the word is read out of memory, the EDAC again generates the check bits, and compares the pattern originally stored with the word against the pattern just generated.

If the two check-bit patterns don't match, the EDAC has detected an error, which it can signal to the CPU. But the hardware can go even further. The EDAC can determine from the two patterns which data bit is in error, and then correct the bit.

■ Flow-through vs. scrubbing

Naturally, there's a price for the service EDACs provide. The error-detection process takes a finite amount of time, and the correction takes an additional 2 or 3 ns. Detection time is a point of competition in the industry, with Advanced Micro Devices (Sunnyvale, CA) claiming to have the fastest 32-bit part—the 29C660—checking in at 16 ns from data in to error detection. Even though AMD's part is claimed to be from 20 to 36 percent faster than its competitors, the 16-ns delay still isn't negligible, and at times forces designers to adopt a less-than-optimal correction strategy.

FLOW-THROUGH EDAC CONFIGURATION



Advanced Micro Devices uses its 29C660 error detection and correction circuit (EDAC) in a flow-through configuration. In such an arrangement, the EDAC can correct any single-bit memory error before it reaches the CPU, but at the expense of slower memory access time.

Ideally, designers would place the EDAC in the memory data path, so that the data from every read cycle flowed through the chip. That way, no single-bit error could ever hang the system up. But with CPU clock frequencies passing 20 MHz, there just isn't time for the data to flow through the EDAC.

An alternative used by many designers is scrubbing. Instead of placing the EDAC in the data path, where data must pass through it on every cycle, designers place it in the refresh path. Memory words are read, checked and then corrected during refresh cycles if necessary. In this way, the entire memory is scrubbed clean of any incorrect bits, but without introducing delay in the memory cycle time.

The technique isn't failure-proof, since an error can theoretically occur in the time between when the word was last scrubbed and when the CPU reads it. But the probability of such an error is minute. Most EDACs, including AMD's new part and TI's industry-standard 74ALS632, can be used for scrubbing as well as for flow-through operation.

A new workstation feature?

The appearance of new competition in 32-bit EDACs suggests that vendors are expecting market growth for the parts. In fact, EDAC capability is becoming a hot issue for workstation and high-end PC designers.

Such a trend might seem justified by the increasing size of workstation memories. But even vendors with hardware to support the capability seem skeptical. Naqvi, whose high-end PC chip sets provide hooks for the TI EDAC part, suggests that the expense of the chip and the extra memory probably isn't justified for systems with memory sizes around 4 Mbytes. "As memory reliability continues to improve, that threshold could move up to 16 Mbytes," he says.

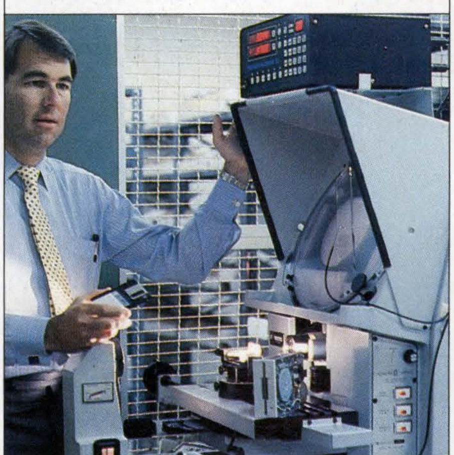
Other observers are also restrained in their enthusiasm, suggesting that the parts have become a marketing fad as much as a prudent architectural alternative. But new parts will create new marketing programs. And the appearance of EDAC hooks in PC chip sets could give high-end 32-bit PC vendors yet another tenuous ploy with which to differentiate themselves. After all, it can be hard to argue against insurance. □

Floppy drive uses optical servo to reach 20-Mbyte capacity

Tom Williams, Western Managing Editor

Optical servo tracks 4 microns wide engraved by a laser into standard high-density 3½-in. floppy media are the key to a new data storage technology. A special head carriage assembly and optical servo tracking mechanism combine to serve up a whopping 20 Mbytes of formatted storage on a 3½-in. floppy diskette. That's what Insite Peripherals (Santa Clara, CA) claims it has achieved with its new "floptical" technology, which is a marriage of standard floppy magnetic recording to optical servo technology for high, Winchester-class track density—1,250 tracks/in., to be exact.

The optical servo tracks separate magnetic recording tracks that are themselves only 40 microns wide. The magnetic tracks contain all sector formatting information and all stored data. The optical tracks are used for servo only. In addition to having vastly increased density, optical servo tracks have the advantage of being indelible—they can't be erased accidentally, according to James Adkisson, Insite president. And they don't rely on totally defect-free media to function. "You can map out bad sectors or data tracks, but you can't map out servo," he says.



The optical servo tracks engraved into Insite Peripheral's floptical drive not only have increased density, but are also indelible and don't rely on totally defect-free media to function, according to James Adkisson, Insite president. "You can map out bad sectors or data tracks, but you can't map out servo," he says.

Most of the mechanical parts of the drive are standard 3½-in. floppy drive parts, such as the stepper and spindle motors, and the frame. Insite has, however, designed a special board for the drive electronics to support the optical servo and has included a small computer system interface controller board with the drive. The parts that are of special design include the read/write head, the LED and photodetector arrangement, and a special voice-coil assembly for fine positioning of the heads.

The head carriage assembly is positioned with a stepper motor, much the same as with a normal floppy drive. But the stepper is used only for gross positioning. Mounted on the carriage assembly is a small voice-coil actuator that moves the head to the tight adjustments required by the drive's high track density. The infrared LED shines through a hole in the read/write head, and the reflected light travels back through a plastic lens to the photodetector.

The optical positioning system, Adkisson notes, must handle three tasks: performing power-up alignment to compensate for mechanical and thermal variations in diskette media; seeking across tracks; and following tracks to keep the heads exactly positioned over the tracks of the

Real time trace of the activity in VMEbus systems

The Single Board VMEbus Tracer

- *Provides all the functions of a Logic State Analyzer, with complex triggering and store qualifiers.*
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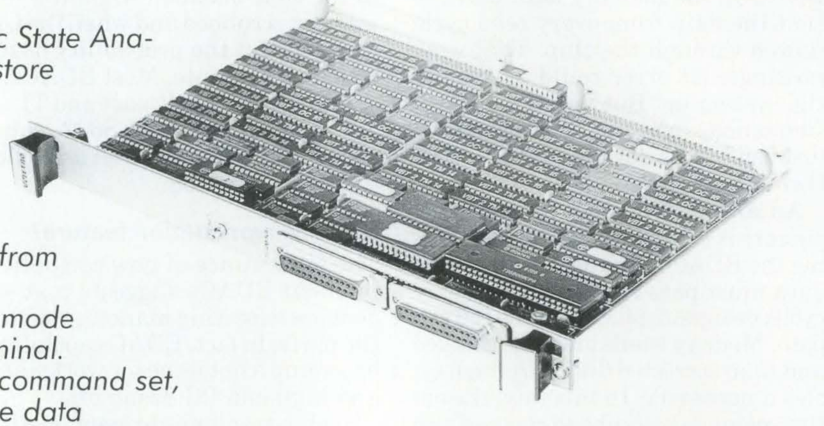
- *Two serial ports and a transparent mode eliminates need for a separate terminal.*
- *Extremely user friendly and simple command set, aided by powerful help menu. Trace data presented in a decoded, human readable form.*



Logic State analysis

- 2 K Trace of 96 VMEbus signals.
- Bus Master Level stored with each sample.
- Powerful Triggers and Store qualifiers, including Bus Master Level.
- Time Tag showing relative or accumulated time.
- Powerful search in Trace memory.

```
   V M E b u s   T r a c e ,  group 1 of 3     Sampling mode : SYNC

        !  TIME     BUS  ADDRESS    DATA    R/W SIZE  STAT   IRQ*  IACK* AM EX
        !  rel.   LEVEL                                    7654321 OC IO
   -----!--------------------------------------------------------------------
==> TRIG !  00.0       0   00202EDC  xxxx4028  R  WORD   OK   1111111  1 1 3D 1
       1 !  3.22 us    0   00202EDA  xxxxFFF1  W  WORD   OK   1111111  1 1 3D 1
       2 !  0.49 us    0   00202EDC  xxxx402C  W  WORD   OK   1111111  1 1 3D 1
       3 !  4.71 us    2   402FFFFC  00200CE8  W  LONG   OK   1111111  1 1 3D 0
       4 !  256  us    2   40300000  FFF140DC  W  LONG   BERR 1111111  1 1 3D 0
       5 !  4.52 us    0   00202ECC  00202EFA  W  LONG   OK   1111111  1 1 3D 1
       6 !  1.79 us    0   00202EC8  FFF06916  W  LONG   OK   1111111  1 1 3D 1
       7 !  0.49 us    0   00202EC4  00200CE8  W  LONG   OK   1111111  1 1 3D 1
       8 !  0.49 us    0   00202EC0  0015000C  W  LONG   OK   1111111  1 1 3D 0
       9 !  0.79 us    3   126543E7  xxxxxx01  R  LBYTE  OK   1111111  1 1 3D 0
      10 !  0.68 us    3   126543E8  00200Cxx  R  UNAL3  OK   1111111  1 1 3D 1
      11 !  3.41 us    1   00200CF0  FFFB0040  R  LONG   OK   1111111  1 1 3D 1
      12 !  18.4 us    1   00200D0F  xxxxxx00  R  LBYTE  OK   1111111  1 1 3D 1
      13 !  21.2 us    1   00202ED8  xxxx02xx  W  UBYTE  OK   1111111  1 1 3D 0
      14 !  2.41 us    1   00202EBC  00000124  R  LONG   OK   1111111  1 1 3D 0
      15 !  0.68 us    1   00202EC0  0015000C  R  LONG   OK   1111111  1 1 3D 1

Time abs/rel:T     Group:1,2,3    Jump:J    Search:S    Print:ctrl-P    Quit:Q
```

Performance analysis

- Address distribution of eight user defined ranges.
- Bus Level distribution.
- Total VMEbus utilization.
- Bus Level utilization.

```
                      V M E b u s   D i s t r i b u t i o n

Total # of samples :   20480

Address ranges          0%  10%  20%  30%  40%  50%  60%  70%  80%  90% 100%

00000000-1FFFFFFF  12% ******
20000000-3FFFFFFF   4% **
40000000-5FFFFFFF  12% ******
60000000-7FFFFFFF   9% ****
80000000-9FFFFFFF  21% **********
A0000000-BFFFFFFF  10% *****
C0000000-DFFFFFFF   9% ****
E0000000-FFFFFFFF  20% **********

     Bus levels         0%  10%  20%  30%  40%  50%  60%  70%  80%  90% 100%

          3        36% ******************
          2        20% **********
          1        26% *************
          0        16% ********

Run: R                         Print: ctrl-P                         Quit: Q
```

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rotating diskette. To solve these problems, Insite invented a photodetector in which four square elements are positioned diagonally to the direction of the servo tracks. The diagonal of one element equals the nominal distance between servo tracks. Thus, when a track is centered over one element, it's not over the element next to it. So the greatest difference in current output between the two elements occurs when a track is directly over one of them. In an ideal alignment, the difference between the two other elements' output signals will be equal but opposite in phase.

A self-aligning drive

The position error signal (PES) derived from processing these different signals is used to correct the head position. But because real media is subject to temperature and manufacturing variations, the optical servo tracks may not be exactly spaced. Their spacing can vary up to a whole magnetic track width (40 microns).

To allow media to be interchangeable and to compensate for variations in both drive and diskette dimensions, the floptical drive incorporates a self-aligning feature. On power-up, the drive electronics senses the variations and, through an alignment algorithm, generates digital values loaded into multiplying digital-to-analog converters to generate a final PES, which compensates for the deviation from the normal track spacing.

In addition to having variations in track spacing, the floppy media and the tracks engraved on it can be distorted out-of-round, and the servo mechanism must be able to follow any such track distortion. This distortion appears to be a major factor limiting the floptical drive's data-transfer rate. The greater the distortion, the greater the servo mechanism's ability to respond must be—and the wider its bandwidth must be. So for a given degree of distortion, spinning the diskette faster will also require a wider bandwidth.

The floptical drive spins at 720 rpm—faster than a normal floppy, but well below the 3,600-rpm rate of most Winchester drives. Since the media is magnetically the same as high-density floppies, it records at a flux density of 16,500 flux changes/in., but the higher rotational speed gives the drive a data-transfer rate of 1.6 Mbits/s, better than twice that of floppies. This is done using run-length-limited encoding, which yields an effective 24,000 bits/in.

The company's 20-Mbyte I325 is the first of a family of drives that with the advent of barium-ferrite vertical recording will eventually reach capacities of 100 Mbytes, according to Adkisson. Barium-ferrite vertical recording takes advantage of a tight lattice structure in the media to concentrate magnetic domains in sharply defined regions. It's now appearing at 4- and 6-Mbyte capacities in normal 3½-in. floppy drives, and will not only raise the capacity of the floptical drive, but will also improve the data-transfer rate. The 33,000-flux-changes/in. density available from barium ferrite will double the data rate to 3.2 Mbits/s.

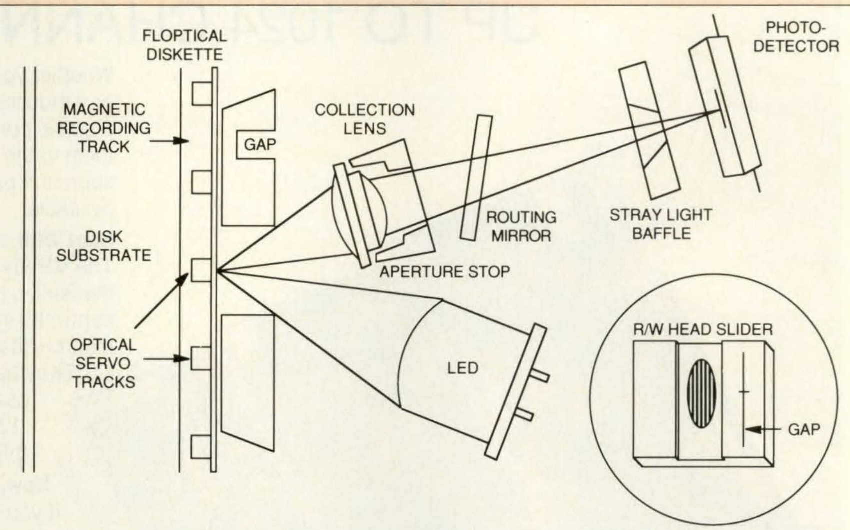
Floptical applications

Given the characteristics that set it apart from normal floppies as well as from Winchesters and tape, where does the floptical drive fit in the system environment? Adkisson sees several possibilities. One is software distribution. For example, today's Unix for the Macintosh II is distributed on 70 3½-in. floppy diskettes. A higher capacity media could greatly reduce the burden of distributing huge software systems. Another distribution problem is increasingly found in data bases and graphics, where the bulk of data is also overpowering the capacity of normal media.

Insite also intends to aim the floptical at Winchester backup as well as at archiving and security, where media removability can be an advantage. Another application will be in laptop systems, where the floptical can offer removability and reduced power consumption (the spindle turns only when the drive is accessed), even though the floptical's data rates are slower than those of Winchesters. Another advantage will no doubt be in price. The initial price of the drive (in OEM quantities) is expected to be $250, with diskettes around $8.

"In the end, we're going to have to license our technology to a lot of people because we're trying to establish a standard," Adkisson says. In addition, Insite has sourced key components outside of Japan in an attempt to give floptical technology a good foothold in the United States. If successful, it could let U.S. industry regain a strong position in the floppy drive arena, which was long ago ceded to Japan. □

THE FLOPTICAL SERVO SYSTEM



In Insite's floptical servo system, an infrared LED shines through a hole in the read/write head to reflect an image of the servo tracks through an aspherical collection lens onto a quad-element photodetector.

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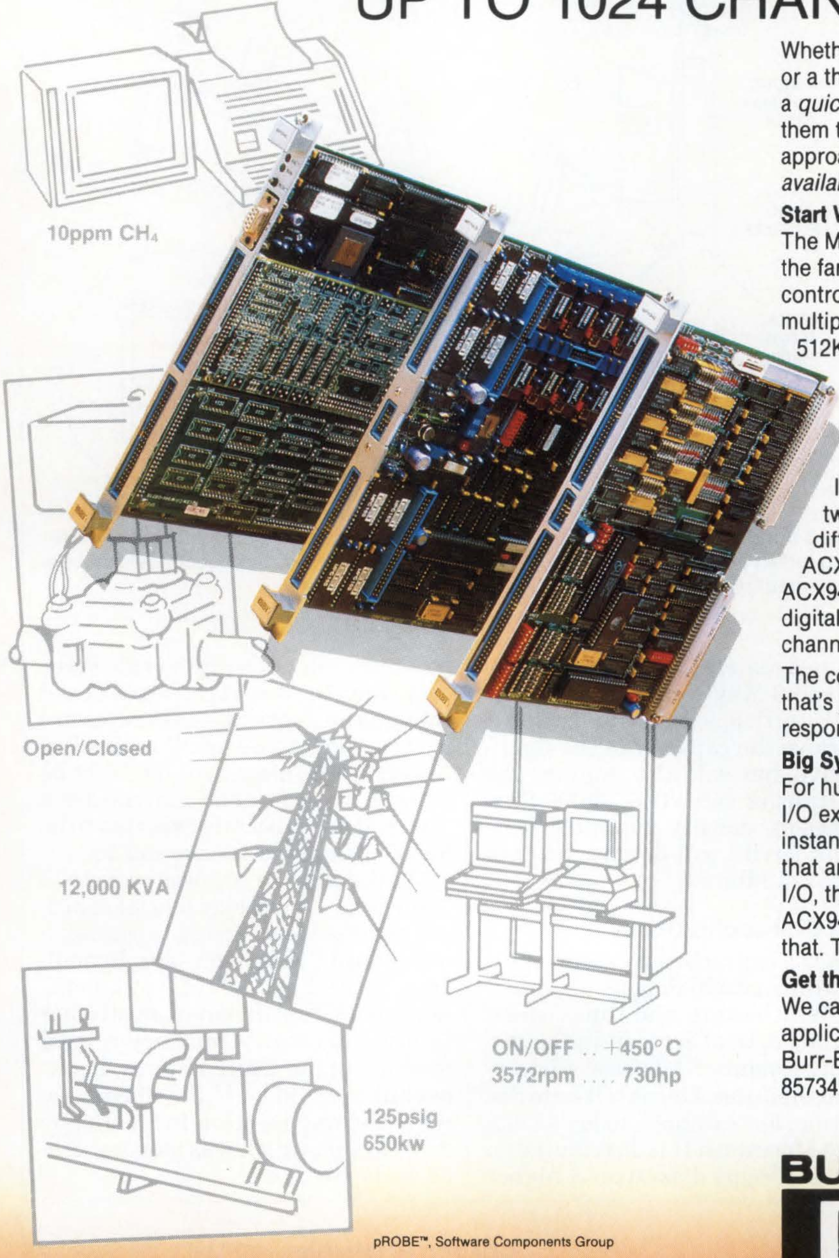

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For hundreds of channels, you can slave up to 10 of our I/O expansion boards to the MPV940. The MPV941A, for instance, offers 128 analog inputs. The MPV941B matches that and adds another eight analog outputs. For digital I/O, the MPV942 provides 32 programmable channels. Its ACX942 daughterboard adds another 32 input lines to that. The result? Maximum density, minimum cost!

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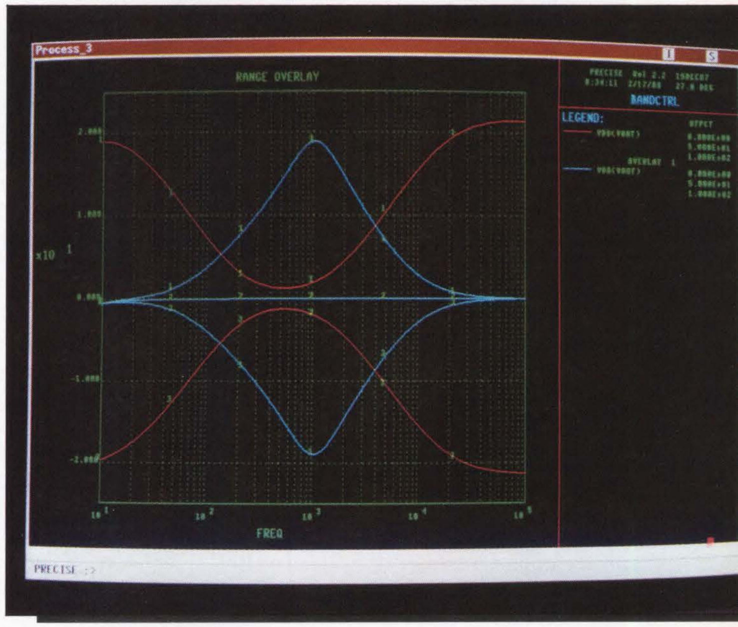
CIRCLE NO. 16

New analysis techniques pave the way for analog simulation

The path to design productivity is wide open for designers who utilize new Spice-based systems, statistical- and stress-analysis programs, and behavioral modeling.

Bill Harding
Contributing Editor



Most analog simulators plot values in a single domain, such as time or frequency. Mixed domain analysis lets the designer view two or more domains in one plot. This Precise simulator plot of gain dB vs. frequency for a tone control circuit shows mixed-domain analysis, which varies frequency and varies the base, mid-range and treble potentiometers from boost to cut.

Analog design may well be the last bastion of the bench-level electronics engineer. Many analog engineers still scratch something out on paper, calculate a few values, build a breadboard and do testing with familiar lab tools. Analog simulators, however, and the CAE tools that surround them, should go a long way toward expanding design automation in the pure analog world.

Analog CAE has outgrown the mere computerized simulation of familiar lab instruments that characterized its early offerings. Faster engineering workstations let simulators handle larger designs and extract information that wasn't practical a few years ago. Statistical-analysis programs predict manufacturing yields based on component distribution probability. Stress-analysis programs predict system reliability based on the power dissipation of each component. Behavioral analog simulation expands simulation capacity, links analog and digital for mixed-mode simulation, works with transistor-level simulators for multilevel simulation, and allows modeling of nonelectrical functions such as mechanical actions and chemical reactions for total system simulation.

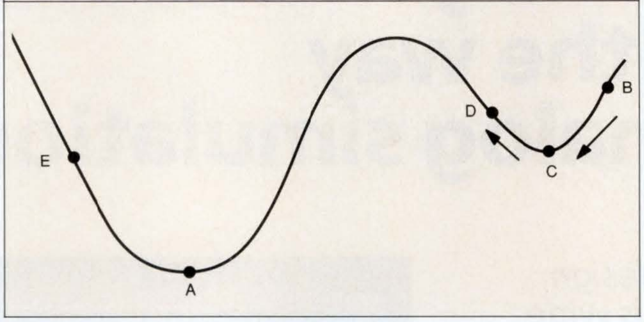
Endless stream of breadboards

In analog design, just as in digital design, the purpose of a simulator is to delay the point at which a breadboard must be constructed, while still providing much of the information that a breadboard would provide. Simulators won't replace breadboards any time soon; they'll only postpone the point in the design process at which a breadboard must be constructed, according to Paul Giordano, product marketing manager at Valid Logic Systems (San Jose, CA). "There are just too many analog functions that simply can't be simulated right now," explains Giordano.

An analog simulator, as part of a total analog design environment, can provide a never-ending stream of simulated breadboards, which can be tested with simulated lab instruments. At the heart of most analog design systems are transistor-level simulators such as Spice, which was developed at the

Irregular curves cause convergence problems in Spice. Spice may be looking for point A, but may be starting at point B. Spice will converge toward point C, but subsequent guesses will cause it to diverge toward point D. It won't reach point A unless it gets a new starting point, such as E.

THE SPICE CONVERGENCE PROBLEM



University of California at Berkeley. Spice solves the same equations that an engineer learned in college, and arrives at the same values that an engineer could develop given enough time, paper and patience. But Spice isn't a perfect solution.

The trouble with Spice

Most vendors who deliver Spice-based simulators have enhanced them to eliminate many of Spice's limitations. One of Spice's key deficiencies is that it's inherently slow due to the compute-intensive nature of its functions, with compute times increasing proportionately as the square of the number of nodes in the design. A small increase in design size, therefore, can significantly increase simulation time.

Convergence is another major problem. Spice guesses at a solution to a waveform problem and then solves equations to see if the guess is correct. This procedure is similar to guessing the square root of a number, then multiplying the guess by itself and comparing the result to the original number. If the result is too high, the next guess is smaller; if the result is too low, the next guess is larger. By repeated guesses, the result converges on the true square root, to whatever precision is needed.

While a simple square root problem will always converge on the correct answer to a very high level of precision, this isn't always the case with irregular waveforms. Sometimes the convergence algorithm gets stuck in a segment of the curve where subsequent guesses diverge from the correct value rather than converge.

Many Spice-based simulators include improved algorithms to either help make an initial guess in another part of the curve, or to provide diagnostics that let designers make necessary changes to the simulation inputs. Some expert systems being developed promise to effectively eliminate convergence problems altogether.

Speed is a different matter. If analog designs would remain constant in size, newer and faster computers could eventually solve the speed problem. But analog designs are getting bigger, and simulation times seem to be increasing at a faster rate than the speed of workstations. Faster computers alone aren't likely to solve the simulation speed problem.

Statistical analysis predicts yields

An analog simulator may also be used to develop and display other information that's either very difficult or impossible to develop with typical lab tools. Analog simulators can perform statistical analysis to predict manufacturing yields, and

Spice-based simulators: an overview

Several companies offer Spice-based simulators, either with their own proprietary CAE systems, or for integration into other vendors' systems. Analog Design Tools (Sunnyvale, CA) offers Spice Plus, based on Berkeley Spice3, in its Analog Workbench product. Spice Plus incorporates the new Berkeley MOS4 model, also known as the Berkeley Short-channel IGFET Model (BSIM), as well as a new op amp, current- and voltage-controlled switches, and gallium-arsenide FET models.

Daisy Systems (Mountain View, CA) offers DSpice, a mature Spice-based analog simulator that's part of its Virtual Lab analog design environment. A unique feature of DSpice is its functional-block modeling capability. Functional blocks are ideal transfer functions that model generic operations such as adders, differential amplifiers, dividers and operational amplifiers. They simulate much faster than detailed transistor-level models, but don't provide the same level of accuracy. Daisy's functional-block models can be used to simulate designs in a top-down design approach, in much the same manner as behavioral simulation. They can also be used in multilevel simulations where some functions are modeled by functional blocks and others by detailed device models from Daisy's 1,500-part analog device library.

The Precise simulator from Electrical Engineering Software (Santa Clara, CA) is a simulator designed to be integrated into analog CAE systems from other vendors, such as Valid Logic Systems' Advantage analog CAE system. Unlike the majority of Spice-based simulators, which support analysis in only one domain at a time, Precise supports mixed-domain analysis, letting users analyze two domains (including temperature, parametric, statistical, frequency and time) in one analysis.

Meta-Software (Campbell, CA) offers HSpice and RadSpice. HSpice is geared toward simulating ICs at the circuit level and is a powerful tool for printed circuit board design. It provides better convergence than Spice through improved algorithms and models, and has diagnostics that give the user various options for achieving convergence in difficult circuits. RadSpice is essentially the same as HSpice, with an added capability to calculate the effects of radiation on a design.

MSpice from Mentor Graphics (Beaverton, OR) is a technology-independent simulator based on Spice-2G.6. MSpice Plus provides higher capacity simulations than MSpice, particularly for entire analog systems. Both simulators use the same analog library and can be upgraded with a Monte Carlo statistical-analysis package.

Microsim (Irvine, CA) bases its PSpice simulator on Spice2G.6, but completely rewrote it into the C language in order to be able to provide future enhancements in C. PSpice 3.07, released in May, includes the Berkeley BSIM MOS transistor model, plus an analog library of about 275 components. PSpice is one of the few (if not the only) Spice-based simulators available on the Apple Macintosh II. It's also available on IBM PC, VAX and Sun workstations.

stress analysis to predict reliability. Statistical analysis recognizes that components used in a design normally have a range of acceptable values, typically varying anywhere between 1 and 20 percent from the stated value. When a breadboard is built and tested, one possible combination of values is observed. Similarly, initial simulations use the exact values shown on the schematic. But the question is whether the design will continue to work satisfactorily with other possible combinations.

Monte Carlo analysis, the statistical-analysis method most commonly used, helps answer this question. When instructed to perform Monte Carlo analysis, the CAE system randomly selects values for all components (or for specified components) within their acceptable operating ranges, and then simulates the design with each set of values and records the results. The designer can display the results either in tabular form or, on some systems, in a graph showing the output distribution. Several systems even generate bar charts that easily pinpoint out-of-bounds results.

If the results of the analysis show that too many outputs fall outside acceptable boundaries as component values change, then manufacturing yields may be too low. The designer can then have the system analyze which components have the greatest effect on the output. Frequently, only one or two components have the greatest effect, and tightening up the tolerances (by replacing a 10 percent resistor with a 1 percent resistor, for example) may produce acceptable yields. The designer can make the appropriate changes and rerun the simulator to test the results.

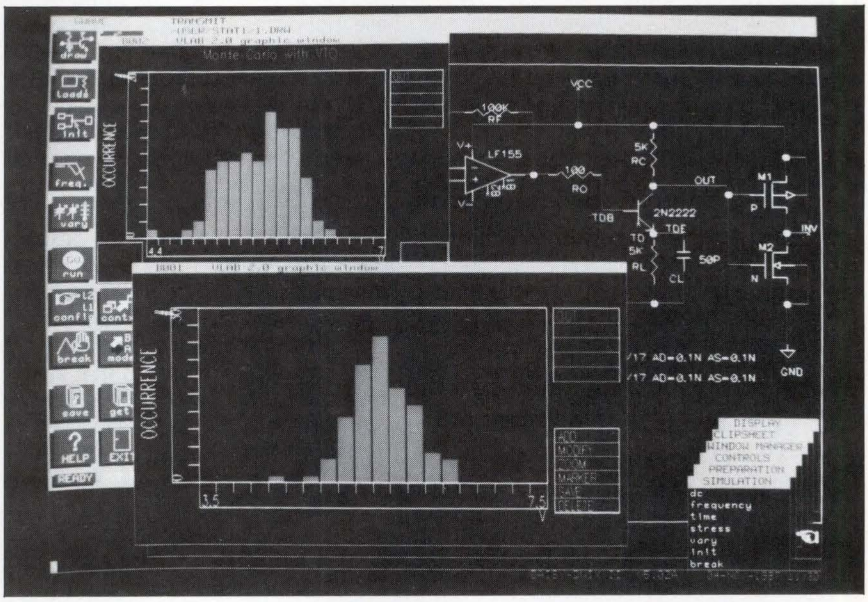
Stress analysis checks reliability

In the same manner, the analog simulator can be used to determine potential system reliability by performing stress tests on the design and comparing the load applied to each component with acceptable ranges. The results can be displayed in the form of a table or a graph to alert the designer to problem areas.

There are two kinds of stress tests: one checks for instantaneous load and the other for average load. The instantaneous load test alerts the designer if the part exceeds its acceptable ratings, even for an instant. This is usually the first stress test run, since there can be no average current overloads if there are no instantaneous overloads. If there are instantaneous overloads, the designer can check for average overloads and make any necessary design changes, armed with complete information.

Departures from Spice

While Spice is the benchmark against which all transistor-level simulators are measured, other methods can be used for transistor-level simulation under certain circumstances. The Adept (Automatic Dynamic Electrical Partitioning of Transistors) simulator from Silicon Compiler Systems (San Jose, CA) takes an event-queue approach, while the Andi (Analog Digital) simulator from Silvar-Lisco (Menlo Park, CA) is a modified switch-level simulator. Both simulators are used primarily in mixed-mode analog and digital simulations.



Monte Carlo analysis can be used to predict manufacturing yields by determining the possible spread of outputs based on various combinations of part values. Information is frequently displayed using bar charts, as shown in this display from the Virtual Lab analog design environment from Daisy Systems.

Instead of using time as the independent variable, such as is done in Spice, Adept uses voltage. Rather than evaluating every node at specific time steps, it evaluates only nodes that are changing voltage. Since this number is almost always smaller than the total number of nodes, simulation is significantly faster.

Adept's major advantage over Spice is that simulation times using Adept grow at a slower rate than the number of transistors in the circuit, while Spice simulation times grow as the square of the number of transistors. An increase in design size that would double simulation times using Spice would thus result in only a small increase with Adept.

Silvar-Lisco's Andi is a special-purpose analog simulator that's somewhere between a switch-level simulator and a Spice simulator in its simulation accuracy. Since switch-level simulators treat transistors as on/off switches rather than as linear devices, they're not suitable for those applications where transistors operate in their linear range, but are faster in applications that use transistors as switches. Andi includes the ability to handle more analog functions than does a switch-level simulator, but is less accurate and performs fewer analysis functions than Spice. But Andi is approximately 20 times faster than Spice, so the speed can make up for the lack of detailed analysis in applications where linear simulation isn't required.

Link with behavioral simulation

As designs increase in performance and reliability, they grow in size. Larger designs mean there are more components and interconnects to simulate, which in turn taxes the capacity and speed capabilities of analog simulators. CAE vendors have taken several routes to address the need for larger and faster simulations. One popular approach is analog behavioral simulation, which lets a large block of circuitry be modeled

Analog simulation moves toward optimization and expert systems

Expert-system concepts, faster algorithms, optimization and customized user interfaces will combine to create a productive design environment for analog applications in the 1990s. Higher circuit densities and increased circuit functionality will continue to affect analog design, as well as its digital counterpart. The shrinking sizes of printed circuit boards and ICs will let designers include more functionality in each new system. And expert-system software techniques coupled with nonlinear optimization will offer relief from mounting pressures on designers to increase both density and functionality.

Analog engineers need design software that will minimize breadboarding and increase yields to improve overall design productivity. This software must be both reliable and accurate. Yet the actual gain in productivity will occur not from the software itself, but from the application of new techniques that let engineers maximize their use of the software-tools, in much the same way as a hammer is most effective in the hands of a skilled carpenter.

■ Analysis takes on new meaning

Spice has long been the mainstay of analog simulation. New software techniques in optimization and expert systems promise to build on the solid analysis foundation provided by Spice. In addition, these techniques give engineers the flexibility to build knowledge into their systems to improve both the overall capabilities and the usefulness of software.

The ability of a software package to make decisions and provide next-step information without burdening the user is the basis for providing better information faster. The keys to an expert-system environment are the ability of its engineers to define their own set of rules, or knowledge base, coupled with an inference engine in the system that applies these rules as needed. These two elements let engineers grow with the software by supplying new rules, and let them view both the application and the results of applying these rules.

A tight interaction between analysis results and the knowledge base further speeds up the design process. Rule-based systems can review the results of a current analog analysis, make a judgment based on rules established and embedded by the design engineer or the supplier, and take one or more additional steps based on those judgments. The time saved by these independent steps is enormous.

The interface software surrounding an expert system must be visual and easy to understand, and designers should be able to customize it. The ability to customize the design environment gives engineers various ways to create commands and pictures that are easily recognizable. Finally, the ability to display results in a meaningful fashion is essential to improve productivity.

Expert-system software techniques coupled with nonlinear optimization will offer designers relief from mounting pressures to increase both density and functionality.

■ ■ ■

Expert rule-based systems also provide a mechanism to transfer valuable innovations and ideas from one person to another or from one group to another. Not unlike the relationship between a senior and junior engineer, expert software can train novices on the advantages of one approach over another. The link with the basic analysis capabilities, Spice or a derivative, forms the grounds for analyzing the impact of new design ideas, technologies and methodologies.

■ Nonlinear optimization

Optimization promises to add speed to the analog design process. Recent applications of sequential quadratic programming and gradient algorithms arrived at solutions to nonlinear relationships in much less time. Of course, analog design is replete with nonlinearities. Software programs with the ability to optimize nonlinear equations will streamline the entire design process. Computer-generated sensitivities provide the direction, and the optimization algorithms provide the next guess. Design engineers supply the design specifications and tolerances.

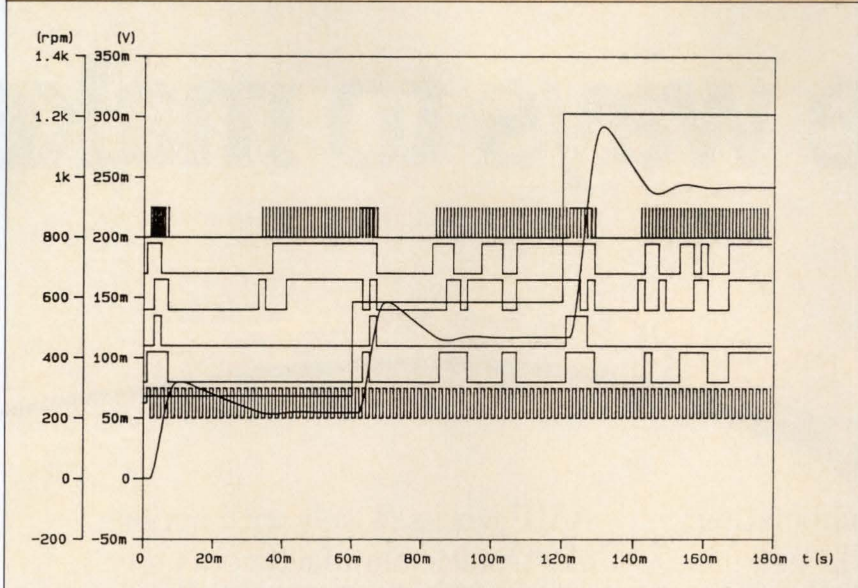
The optimization software determines the changes in circuit value necessary to reach the design objective. This software is doing more than analyzing a topology—it actually changes element values and model values to reach a target. The targets are the expected performance of the design stated in terms, such as maximum gain, minimum propagation delay, corner frequency, 3-dB point and a host of other possible design-objective descriptions.

The link between rule-based and optimization algorithms provides a powerful mechanism for the design and synthesis of analog circuits. Rules can add and change topology based on the results of analysis and optimization. Reaching the maximum gain objective, for example, may best be handled by adding another amplification stage. Rules set up to control fabrication or element counts can determine if a stage should be added. Rules in the knowledge base applied after optimization can add appropriate circuitry to the topology and quickly move to the design objective.

Rule-based systems can form the basis for top-down design strategies in the analog design environment. Just as all high-level languages eventually are translated into machine code for execution on a computer, rule-based systems can form the basis for determining exactly how analog circuitry will integrate into the overall system design. Even engineers with little analog experience will be able to successfully integrate analog functions into their designs.

Kevin M. Walsh, BSEE, vice-president, Electrical Engineering Software

DIGITAL AND ANALOG WAVEFORMS FROM SABER/CADAT



The Saber/Cadat mixed-mode simulator (a merger of Analogy's Saber analog simulator and HHB Systems' Cadat digital simulator) provides the means for mixing analog and digital in the same simulation and for simulating mechanical as well as electronic functions. This printout displays both digital and analog waveforms for a motor speed controller, with an analog output waveform overlaying the digital control signals to show how the digital signals generate the analog signal.

with a hardware-modeling language that defines the block's functions rather than the individual components within the block.

Behavioral simulation can be used in a top-down approach to examine a system's overall performance before creating detailed designs, says Andre Vladimirescu, director of simulation technology at Analog Design Tools. The whole system can be simulated at the behavioral level, with each function represented by a behavioral model. For more detailed analysis, behavioral models are replaced by transistor-level models that can be simulated using a transistor-level simulator. Transistor-level simulation also helps refine behavioral block definitions for subsequent system-level designs.

As a final test, designs can be simulated using a combination of behavioral simulation and transistor-level simulation. In this case, higher level blocks that have been expanded and simulated at the transistor level are modeled at the behavioral level again, and the interconnects between blocks are modeled at the transistor level. This approach provides fast system-level simulation, since the blocks, which typically make up the bulk of the design, are known to function correctly. Only the circuitry that connects one block to another, therefore, must be modeled in detail.

An advantage of behavioral simulation is its ability to model more than just electronic functions. Mechanical functions such as valve controls, flow sensors and lever positions, as well as chemical reactions, can be modeled with the same behavioral-modeling language used to model analog electronic functions. Since analog circuits frequently provide the controlling element in systems involving mechanical or chemical reactions, this is a particularly important capability.

The future of analog CAE

The next few months and years should see the introduction of even more powerful analog-simulation capabilities. Two areas that offer particular promise in the near future are circuit optimizers and expert systems.

An optimizer helps an engineer determine the exact component values needed to make a design perform according to specifications. An engineer may develop a design for an amplifier, for example, and provide some starting values for the components, as well as some output specifications. The optimizer routine will then vary the values of the components in the design until they meet the output specifications.

Expert systems take up where optimization leaves off. An expert system is typically a rule-based design tool that's based on the knowledge and experience of expert analog designers. Where optimization changes values within a design in order to achieve the required output, an expert system may question the design itself.

Expert systems let engineering teams develop and specify rules to be followed for all designs. These systems may address such problems as Spice convergence, or the relaxation of Spice parameters to speed up simulation during design phases where high levels of detail aren't needed. They may prompt a designer with possible design changes to help find solutions to complex problems.

Such advances in analog simulation may well signal the end of an era. How much longer will analog designers consent to sit at lab benches and measure wire-wrapped breadboards with their limited oscilloscopes when they could be gathering more complete information, much faster, with an analog simulator? □

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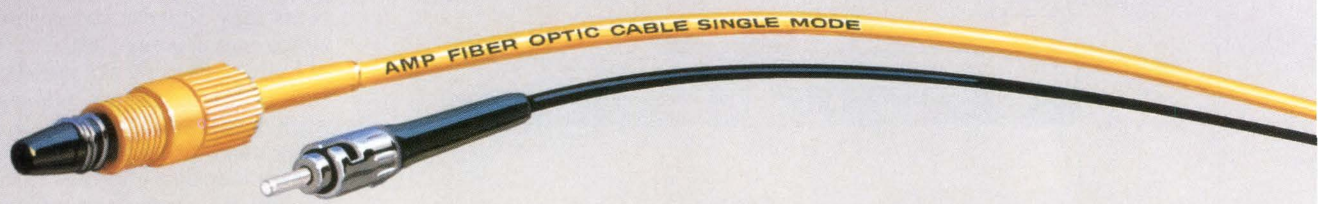

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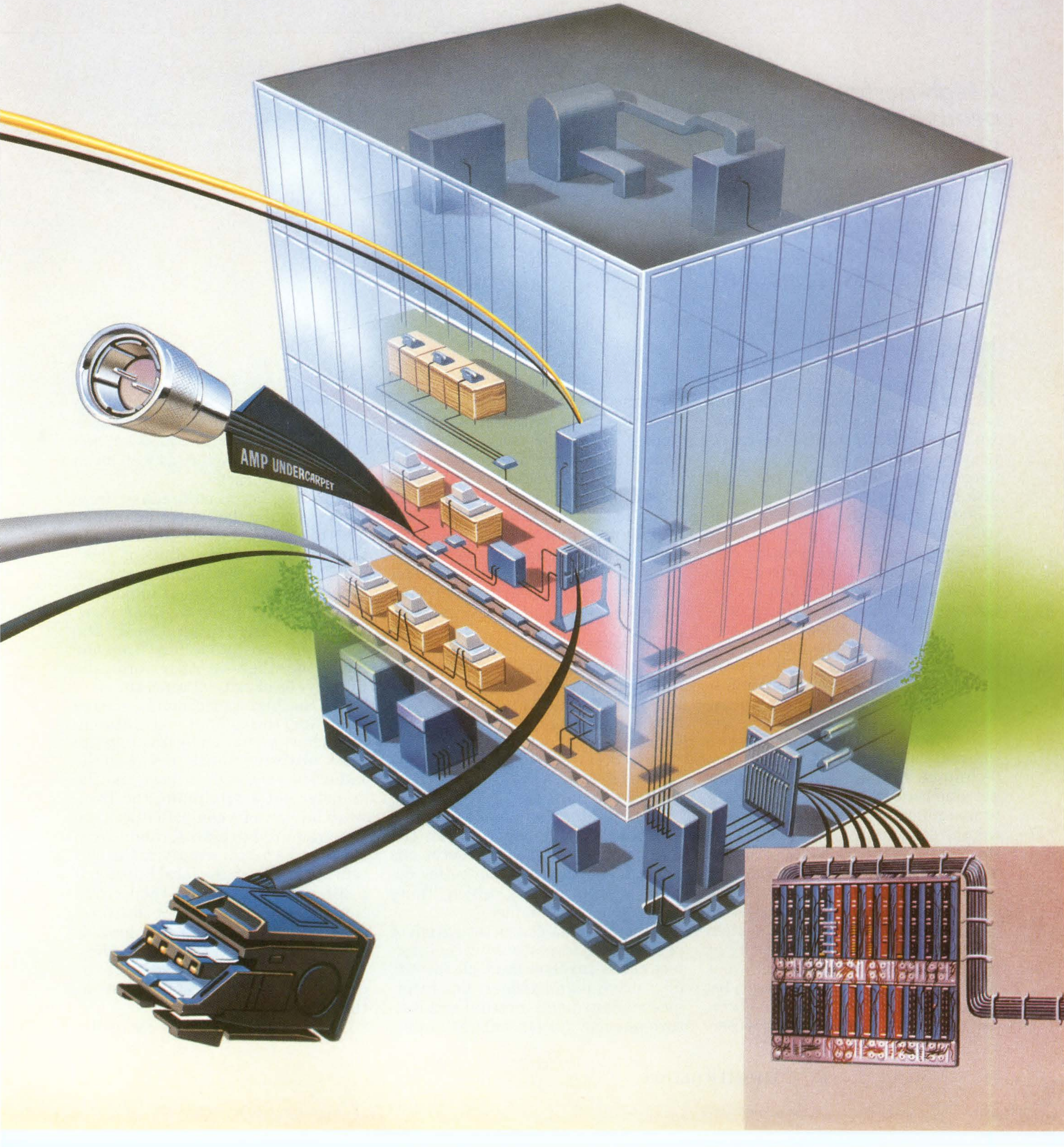


In search of the high-performance controller

David Lieberman, Senior Editor

A high-performance CPU needs high-performance peripheral and I/O controllers to balance its power. But how do you measure a controller's true performance and make the best selection?

High performance. How many times have you heard that claim? And what is the technical reality beneath the marketing verbiage, say, for a high-performance Winchester disk drive controller?

The mission of the Winchester controller in a system is to quickly and efficiently deliver data between disk drives (mechanical, magnetic devices that store data serially) and system CPUs (electronic devices that handle their data in parallel form). The controller's success can be measured in burst transfer rates and overall throughput, but these are ultimately determinable only by operating the completed system with the controller in residence. Since this is an impractical controller evaluation technique for those in a rush to market, and because any full-fledged system simulation is equally impractical, the designer usually tries to measure controller performance with commercial or home-brewed benchmarks.

But such benchmarks seldom give a true picture of storage subsystem performance in its eventual system environment. By looking closely at the architectures of many different controllers and the philosophies behind those architectures, however, designers can identify the key performance areas to hone in on when benchmarking controllers for a particular application. In the abstract, a controller will perform to the extent that it can mask the characteristics of the disk and system from each other and dissociate their operations, and then overlap and optimize those operations, decoupling the two for the good of the system. The controller vendors' particular art in achieving these goals lies in the details.

First-order considerations

Differentiating between low-, medium- and high-performance controllers is a two-level process, the first level addressing the traditional performance breakdown by drive class. "Users don't expect much from ST-506 and so don't want to pay much for the drive or controller," says William Moren, product manager at Ciprico (Plymouth, MN). "SMD is just the reverse. But pricing considerations place restrictions on controller designs within a class, which limits subsystem performance."

A second-level characterization of performance levels—within an interface class—involves multiple factors: disk drive management, bus interface management, internal architecture and the system software interface. The ultimate performance equation for any controller board depends on the level of optimization applied to each of these factors as well as on how they interact.

Consider, if you will, a disk drive controller as a data pipeline, analogous to an oil pipeline from Alaska to Oregon. From some points of view, the flow rate at the beginning or end of the pipeline is the most important consideration. From another viewpoint, the time required to fill the pipe or for the data to flow from one end to the other—in other words, the latency—is of critical concern.

"To us, high performance means maximum throughput," says Moren, "which is calculated by dividing the block size being transferred by all the latencies required to perform the transfer. At a minimum, the firmware latency of a controller plus the time required to transfer data from the board's local memory to the system bus make up the total latency. If a disk access is required, then a rotational latency is added. At the worst case, a seek time is also added. It should be apparent that the application and how the system accesses the disk can also dramatically affect actual sustained rates."

Clearly, the disk drive controller

doesn't operate in a vacuum, and the particulars of a system architecture introduce a number of complexities to the pipeline analogy. On the peripheral end, for example, high-performance controllers typically manage multiple data sources (drives) with multiple read/write heads, only one of which can provide data at any one point in time. And on the system end, the controller is only one of many data sources (boards) that must share the system's data bus.

The differences among particular applications further complicate the analogy—and the controller selection decision. The controller that excels at performing long transfers may be deficient for short transfers, for example, or vice versa, and the board that reads disk data with great speed may operate less than optimally when called on to perform alternating reads and writes, or vice versa. While some controllers may perform admirably in single-user, single-disk systems, they may fail miserably to serve the needs of multiuser or multidisk systems. And so on.

Managing the disk drive

One of the more simplistic methods of differentiating controller performance is to look at the data-transfer

INTERFACE PERFORMANCE			
Interface	Data Rate (Mbytes/s)	Data Format	Controller Cost
ST-506	0.625	Serial encoded	$100 to $500
ESDI	1.875	Serial NRZ	$350 to $850
SCSI	4	8-bit parallel	$350 to $850
SMD	2.4	Serial NRZ	$1,000 to $3,500
IPI-2	10	16-bit parallel	N/A

The first-order decision about a mass-storage subsystem involves a choice among interface classes. The interface's basic specs can be misleading, however. With SCSI (small computer system interface), for example—the only system-level interface in the group—normal latencies plus additional protocol processing means that throughput will be in the kbyte-per-second, not Mbyte-per-second, range. And, of course, no 10-Mbyte/s IPI-2 disk drives currently exist.

rate to and from the disk drive that the controller can sustain, which depends on its driver/receiver technology, serializer/deserializer implementation, buffer architecture, and so forth. Sustained transfer rates for a controller are inevitably limited by drive rates of one track per revolution. Any controller has this limitation, but not every controller can reach it.

Beyond data-transfer rate, controllers also differ in how quickly they can begin reading or writing data after a disk drive head reaches the correct track and settles and, in some cases, the disk revolves to the correct sector. They also differ in the degree to which they can keep up with the data stream without having to skip sectors (the interleave factor). Most of today's high-performance controllers support 1:1 interleaving—that is, they can read and write consecutive sectors—and many provide zero-latency reads and writes.

"For a controller to be considered high-performance, it must be able to operate the highest-performance drives in its class with a 1:1 interleave," says Ernest Godsey, director of product marketing at Interphase (Dallas, TX). "For large block reads, it should be capable of continuously sustaining the native data rate of the attached drives."

"Any good high-performance controller," adds Chappell Cory, senior vice-president for marketing operations at Xylogics (Burlington, MA), "should be able to perform a continuous transfer of, say, five or 10 tracks of a cylinder or the whole cylinder, switching heads without losing disk revolutions."

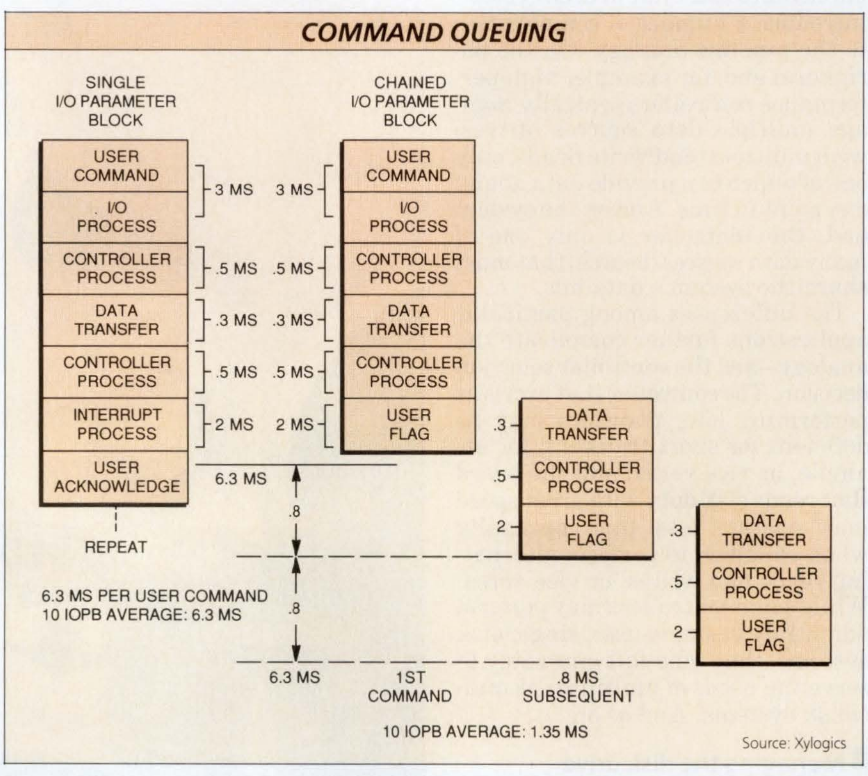
A zero-latency read capability lets a drive start reading and transferring data as soon as a head settles, rather than having to wait until the disk revolution brings the proper sector into place. Zero-latency writes, which let the head start writing as soon as it lands, is the less common function of the two and, according to Cory, generates real performance gains only when at least half of the data track is going to be written. Being able to accept the second half of a track before the first half requires that there's a certain degree of intelligence on the controller and a certain amount of buffer memory, as with most drive-optimization techniques. This and other optimization techniques are intended to minimize, and/or make the most of, the required disk operations—the slowest operations within a system.

The mechanical nature of a disk drive makes it the greatest potential contributor to overall data access latency. Intelligent management of disk accesses can, therefore, substantially cut down on overall time required to access data. When a controller writes data to a drive, for example, its placement on the various sectors and tracks of various data surfaces can be manipulated so that subsequent reads of the data require less mechanical motion. Placing sequential parts of a file on a single cylinder, for example, can obviate head repositioning.

Overlapped seek common

Among today's more common optimization techniques are overlapped seeks. Overlapped seeks let a controller effect a seek on one drive, then on a second drive, reconnecting to the first drive when its seek is complete and it's prepared to transfer data. Here, as elsewhere, the high-performance controller makes very good use of the unavoidable latency involved in one operation to go off and perform another.

"Overlapped seeks overlap nonproductive seek times of disks," Inter-



By queuing commands on-board, an intelligent controller can minimize time-consuming host interrupts and let commands be manipulated to minimize overhead. Here, chained I/O parameter blocks (IOPBs) reduce the 10-IOPB average overhead from 6.3 to 1.35 ms.

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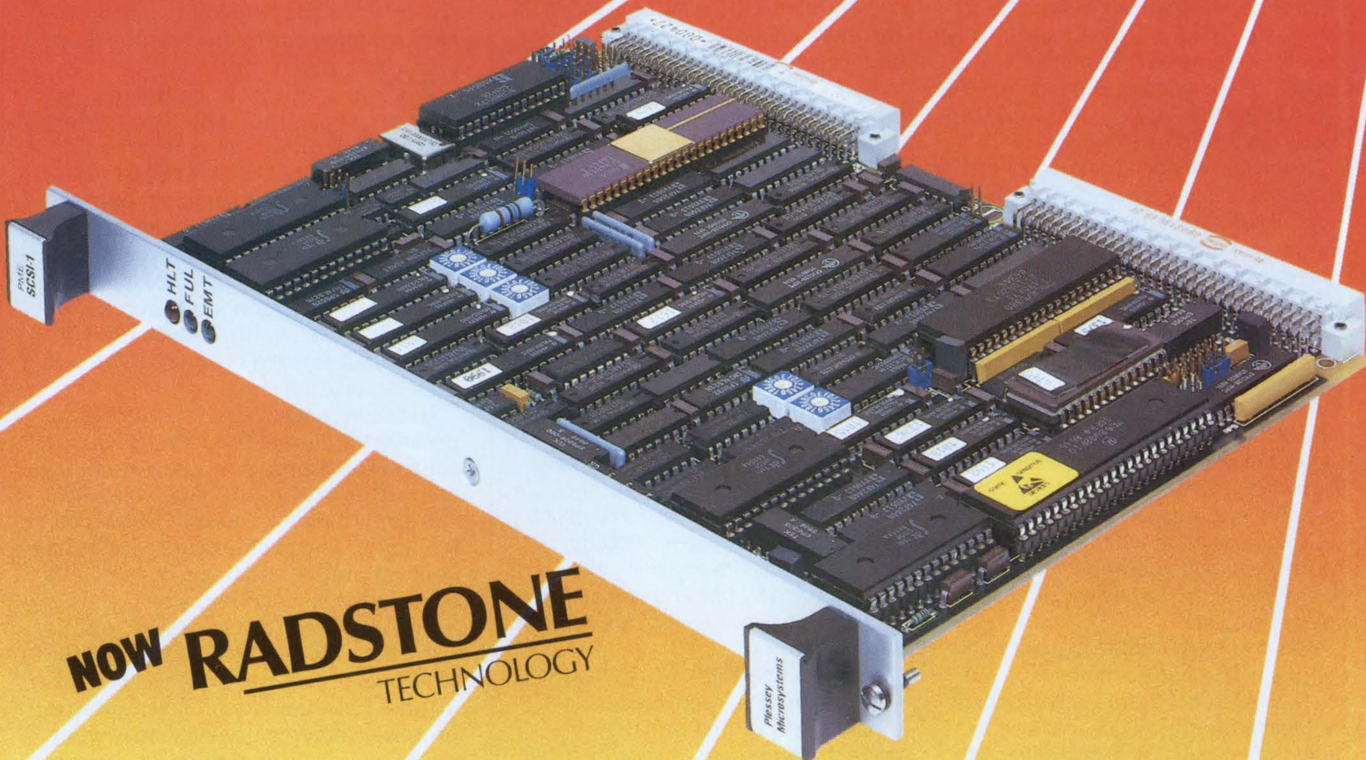

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CIRCLE NO. 18

The controller selection dilemma

In an ideal world, a company would have its core system completed and its customers' applications programs up and running before attempting to select a disk drive controller. But, of course, this is seldom the case. "Some very large companies may have three to four years to develop a new computer and an I/O system for it," says Chappell Cory, senior vice-president for marketing operations at Xylogics (Burlington, MA), "but in the fast-moving OEM world, nobody can afford that kind of time."

In the real world, I/O and peripheral controller selection doesn't lie in the critical path of system development and it's often a rushed, haphazard, low-priority affair. Cory describes the typical development flow chart of a certain customer: "The bus is selected, then the CPU and memory boards are designed, then someone works on the card cage, and a bunch of software guys work on the operating system. By the time a crude lab model has been developed (which is probably seven to eight months late), marketing has been busy pricing and selling the thing, everybody's rearing to go, and then somebody cries out, 'Hey, we've got to get a disk controller.'"

What follows is tremendous pressure to pick a drive and controller; iron out the wrinkles; get the driver working; develop the format utilities, and device- and system-level diagnostics; integrate the subsystem; and get the computer into production. "There's a very tiny time window for I/O performance evaluation, which hardly ever gets the attention it deserves," Cory says.

Without the real-world applications the system will be called on to run, the designer reverts to benchmarks to evaluate controller performance. He may use a commercially available benchmark, which may or may not be very applicable, or he may develop his own benchmark, which may or may not be based on a true picture of the expected uses of the system—depending on the time available to develop it.

"Many people benchmark in totally fictitious environments with no bus loading at all," says Ernest Godsey, director of product marketing at Interphase (Dallas, TX), "and the evaluations are often very rushed because of the business pressures to get a product to market." Ciprico (Plymouth, MN) reports similar experiences. "Benchmarks are undoubtedly one of the most misused ways of evaluating controllers," says William Moren, Ciprico product manager. "They are typically very simplistic—measuring how long it takes to read and write a lot of data, and the controller that takes the least amount of time wins. This doesn't mimic real life very well, but real-life simulations aren't easy to write, which certainly is one reason why simple benchmarks are used so frequently."

Cory finds a diversity of benchmarking sophistication among customers. But on the whole, he says, "The benchmarks used to ultimately select the controller of choice are abysmally inadequate, inaccurate and unmeaningful, yet major bus decisions are made around them."

Moren suggests that, whatever the benchmark being used, evaluations should be performed with the controller manufacturers' assistance in getting the controllers operating at peak efficiency for the particular application at hand. "High-performance controllers require fairly extensive device drivers that can be modified or configured to make proper use of controller options," he says. "Using a quick and dirty driver for testing may not paint a picture representative of a controller's capability. And getting the controller house to help in the evaluation also gives the customer a chance to see their support structure in action."

phase's Godsey explains. "The controller may still end up waiting while the disks seek. At least, however, there will be more than one seeking at a time."

Scatter/gather read/writes have also become fairly common, optimizing the data pipeline by letting a disk or system memory accept a data transfer even though a contiguous block may not be available to place it in (scatter) or to reassemble the data on the other end (gather). Scatter/gather capability minimizes the command overhead of these operations, managing multiple fragments of memory in response to a single command from the host.

Format skewing (also called spiral reads/writes) is a less common feature. Format skewing equips the controller to automatically cross head and track boundaries when absorbing the contents of a long lookahead read.

Offloading the microprocessor

To isolate peripheral from system performance, most controllers use some sort of supervisory microprocessor or microcontroller and the local memory to buffer data and decouple peripheral data rates from those of the system. But beyond this, high-performance controllers and others part company.

With a traditional buffering approach, typical of the low-performance controller, for any given request the data is transferred from the source (either system or disk) entirely into the buffer and is then transferred to the destination. "This results in poor performance," says Moren, "because it requires a disk access for each request, and the most the controller can service is one request per disk revolution."

In these controllers, the managing processor is involved in all disk I/O control functions, contains a small local buffer and most likely includes the direct memory access (DMA) control logic. The problem here is that a general-purpose microprocessor can't sustain high-speed transfers, and its buffer can't tolerate long, continuous transfers. "The controller is unable to support multiple overlapped operations," claims Cory, "because the processor is typically very busy managing one disk operation at a time, nor can it simultaneously communicate with the host CPU. So while this represents an inexpensive solution that, at first, looks elegant and simple, it's totally incapable of achieving high performance."

A part of the high-performance controller's answer to microprocessor overload is to offload time-critical disk- and bus-related tasks from the microprocessor to dedicated custom silicon or proprietary discrete circuitry. It also incorporates additional on-board memory to implement a sizable buffer memory. An offshoot of using specialized parts is that the unburdened microprocessor is freed to handle a number of high-level functions that would be impossible for the type of controller whose microprocessor manages the data path.

Command management

The traditional buffering approach tends to go hand in hand with a tradi-

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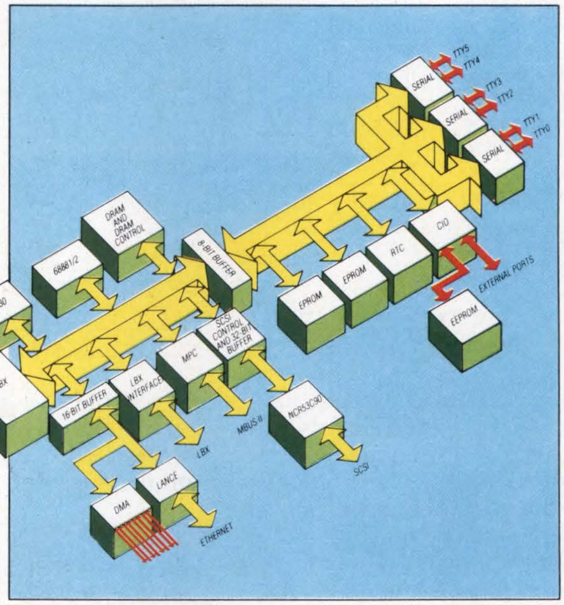

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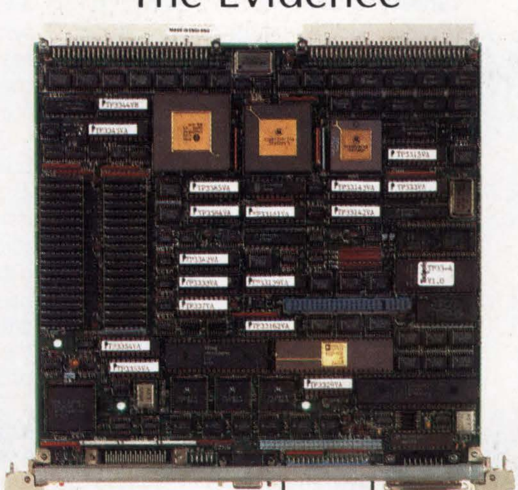

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CIRCLE NO. 19

Once queued, a string of commands can be scanned and restructured to help minimize overhead. Grouping seek commands with the same (or nearly the same) cylinder, head and sector parameters, for instance, minimizes lost disk revolutions, intertrack head positioning and head switching from seek to seek. Here, optimizing the command order cuts disk overhead in about half.

COMMAND OPTIMIZATION

Data Location		Sequential Order	Seek Time (ms)	Optimized Order	Seek Time (ms)
Block 1 Track 0	Head 0	1	18	1	18
Block 30 Track 20	Head 2	2	25	4	25
Block 41 Track 308	Head 0	3	45	8	45
Block 20 Track 70	Head 4	4	45	6	30
Block 32 Track 20	Head 2	5	30	5	2
Block 30 Track 0	Head 4	6	25	2	8
Block 4 Track 309	Head 1	7	45	9	16
Block 5 Track 0	Head 4	8	16	3	0
Block 21 Track 70	Head 3	9	45	7	2
Total Seek Time			294		146

Source: Xylogics

tional approach to command management. Here, the device driver in the operating system queues the command stream, sets up an I/O parameter block (IOPB) and, as Moren puts it, "gooses" the controller (typically by writing to a register on the board) to let it know there's a command waiting to be performed. At this point, the controller reads the IOPB, performs the command and interrupts the system when it's complete, at which point the driver can issue another command. "This approach is somewhat archaic, since the controller has little opportunity to do any command optimization," comments Moren. It also requires interrupt processing on a per-command basis, injecting overhead into each operation.

High-performance controllers commonly perform their own command queuing by means of an on-board command buffer and a mechanism that lets the device driver pass commands to the controller board as they become available from the operating system, "regardless of controller activity or the status of previously issued commands," Moren explains.

There are two benefits of placing the queuing function on the controller: the driver is simplified because it's relieved of much of the queuing function and, by queuing all pending commands, the controller can execute multiple sequential functions without recurrent host involvement and can apply optimization techniques that reduce latencies and improve throughput. According to Godsey, almost any command-queuing scheme will achieve some base level of performance improvement "because the queuing will overlap command-issuing times, command-parsing times and command-complete interrupt-service times with other controller activities."

The minimum optimization that command queuing allows is the implementation of overlapped seeks on however many drives the controller manages. Intelligently managed, however, the command queue can be scanned and the commands sorted and reordered or even combined (or "chained") to minimize the amount of head switching, disk revolutions or intertrack movement required between sequential operations.

The difference between a medium- and high-performance controller within an interface class is, perhaps, most apparent in the types of command optimization it performs—that is, what it does with multiple commands once they're resident in local memory. While overlapped seek capability is fairly common across the performance spectrum, intelligent command sorting with such optimizations as command combining and

The benefit of burst transfers

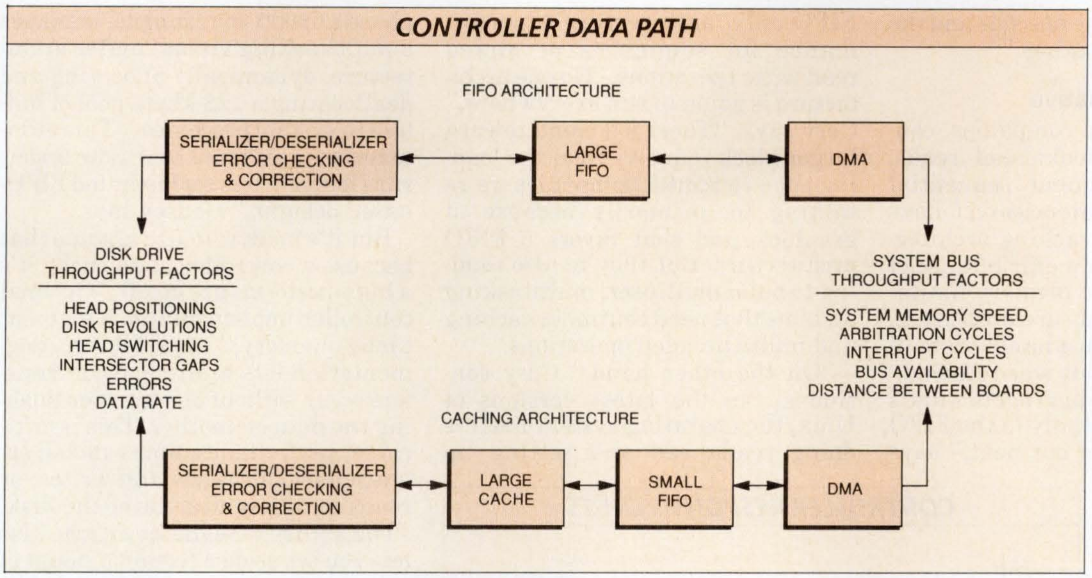
No controller issue has created more controversy, and confusion, than burst transfer rate. "A popular misconception we run into frequently is the effect burst rates have on subsystem throughput," says William Moren, product manager at Ciprico (Plymouth, MN). "High burst rates simply do not dramatically increase disk throughput."

It seems that items such as seek and rotational latency times, disk transfer rates, firmware overhead and optimization techniques all have a more dramatic effect on throughput than do burst transfer rates, which really indicate the amount of overhead a board interjects in each system bus transfer cycle. "About 200 ns or less of overhead is characteristic of VMEbus controllers in the 30-Mbyte/s range," says Moren.

But a controller's burst rate has a big impact on overall system performance. As Ernest Godsey, director of product marketing at Interphase (Dallas, TX), sees it, if controller A has double the burst rate of controller B, then A will transfer the same amount of data in half the time, making that much more bandwidth available for other system operations and for a controller to perform other tasks. But Chappell Cory, senior vice-president for marketing operations at Xylogics (Burlington, MA), adds a qualifier. "That's true only if the system has infinitely fast memory. The real performance key is in controller overhead, since memory cycle times are much longer than burst rates."

Godsey, however, views a controller's burst transfer rate across the system bus as a more important consideration than its latencies. "A controller's ultimate throughput, or the maximum aggregate data rate it can sustain over the long haul, is essentially limited by the data rate of the disk drive." Thus, Godsey says, the real frontier for controller optimization lies at the bus interface.

"While it's usually a fairly straightforward task to add resources to a system, bus bandwidth isn't an expandable resource," he says. "It's crucial that a controller makes effective use of the bus to maintain overall system performance, particularly as disk data rates go up, as systems attempt to do more and more, and as many systems move to multiprocessing architectures with a substantial amount of interprocessor communications. It's important to design the system so that system requirements, bus data rate, the controller and memory are all matched. Anything else is classic suboptimization."



Each step in the data path between disk and system introduces latencies and overhead. The key to performance is the decoupling of the disk from the system to overlap operations. A high-performance controller, whether FIFO or RAM-based, will interface with the disk and bus at the peak rate they'll allow and will offer sustained performance equaling the disk drive rate.

elevator seeks is relatively rare. With elevator seeks, a track close to where the head lies will be read before a second, more distant track that may have been requested first.

Architectural differences

The current-generation high-performance controllers from Ciprico, Interphase and Xylogics illustrate some of the common and diverse elements in today's high-performance controllers. Perhaps the most obvious difference between the three is that while both Ciprico and Interphase use 16-bit microprocessors (the Intel 80186 and Motorola 68000, respectively) and run data through a two-stage process involving a large cache memory and a small bus-interface first-in, first-out buffer, Xylogics uses only a large bus-interface FIFO buffer and, since there's no cache memory to manage, makes do with an 8-bit microcontroller, the Intel 8031. As a rule, caching introduces a great deal of complexity into a controller; however, it also offers much greater opportunities for performance enhancement.

"Our processor spends most of its time setting up some very fast custom hardware," says Corey, "and since we're not doing sophisticated caching algorithms and don't need constant microprocessor intervention to figure out what data is where, whether it's old or new, spoiled or good, we can avoid a lot of internal controller overhead."

All three companies' controllers (and all others with any claim to being high-performance devices) buffer at least one full track of data, and all three pull in subsequent blocks of information (performing lookahead seeks or "prereading") so that, should following requests be for sequential data (as they often are in Unix), the request can be met without reaccessing the disk drive. The buffers at all three companies' bus interfaces are treated as FIFOs, which have a "virtual buffer" capability—a virtual size much greater than their actual size. "Because they can be filled at one end while simultaneously being emptied on the other,"

> ***"Any high-performance controller should continuously transfer a cylinder without losing disk revolutions."***
>
> *—Chappell Cory, Xylogics*

explains Cory, "their capacity is not an absolute value and is, in fact, infinite when the disk and bus rates are equivalent. Ping-pong and staged buffers don't share this ability and will overrun much sooner than a FIFO buffer."

The three companies also all packetize data in their FIFOs and use proprietary DMA schemes to blast packets across the bus: Xylogics at a peak rate of about 18 Mbytes/s, Ciprico and Interphase at about 30 Mbytes/s—assuming that system memory is fast enough or cleverly designed enough to support such rates. Like disk data-transfer rates, however, the bus burst transfer rate of a disk drive controller gives only a partial picture of its overall performance. Advocates of the throughput school of controller selection say that sustained and aggregate rates must also be taken into account.

Xylogics claims superior performance for its FIFO architecture for long sequential reads and writes by virtue of an internal transfer rate that exceeds the sum of its disk transfer rate and bus interface rate. According to Cory, having a large FIFO that can be filled as quickly as it's being emptied means that continuous peak transfer rates can be sustained as long as required.

In the caching architectures, the internal and bus interface data rates aren't coupled in that way and, according to Cory, the latency that's involved in filling a FIFO at a lower rate compromises the aggregate performance.

Moren responds: "When I'm comparing automobiles for speed, I look at miles per hour, not revolutions per minute. Beyond a certain point, you get performance from the way data is managed by firmware, not from hardware architecture."

As Godsey sees it, the internal latencies of a controller are far less important than its burst transfer rate across the bus. "Obviously, the controller internals can't be slow in comparison to bus speed, but at some point they become insignificant because they're overlapped by other operations on the bus. What the controller does when it's off the bus is of little import in the overall scheme of things as long as it's fast in interfacing to the disk on the one side and the system bus on the other."

The cache alternative

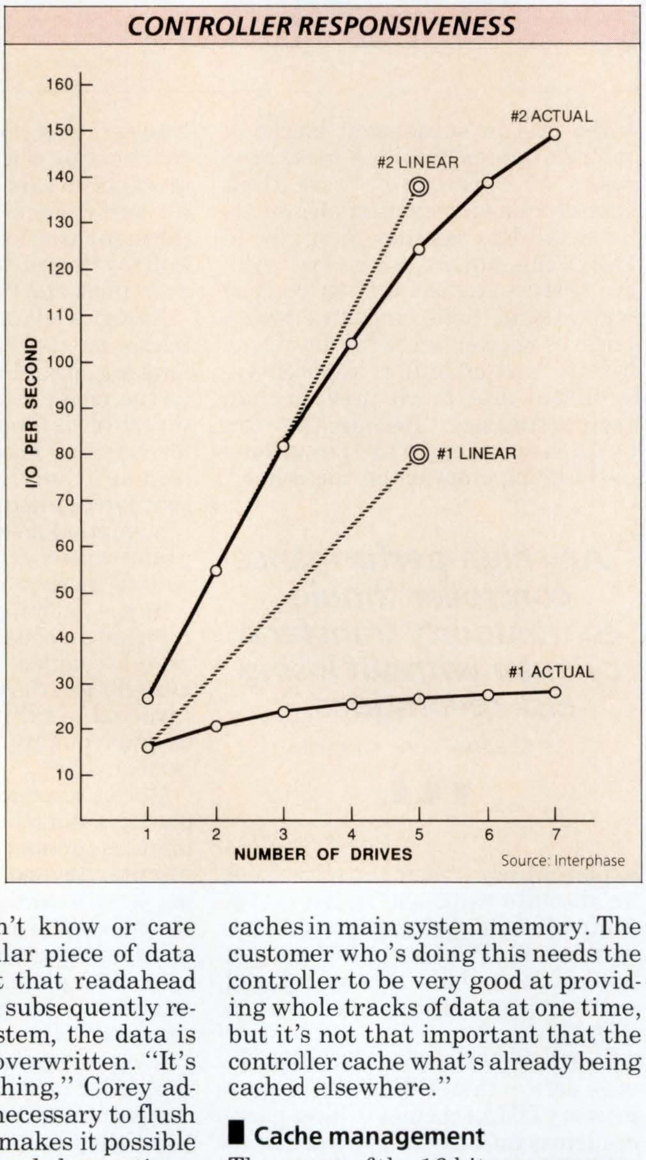
Although all three companies' controllers perform lookahead reads, pulling in subsequent sequential data to avoid disk latencies on following requests, the caching architectures make far more efficient use of the capability. The primary limitation of the FIFO-only architecture is, of course, that it must handle data in the order in which it was received.

"We know in the aggregate what's stacked up sequentially in the FIFO and what's coming out next," says Cory, "but we don't know or care where any particular piece of data is." If it turns out that readahead data is not, in fact, subsequently requested by the system, the data is simply flushed or overwritten. "It's only with true caching," Corey admits, "that it's unnecessary to flush the data, and that makes it possible to support multithreaded operations, for example, with each user or process having its own data cache."

The necessity to flush unneeded data, Moren points out, limits the FIFO-only architecture's performance for sequences of mixed read/write operations. "No one architecture is going to win everywhere," Cory says. "There's a trend toward larger block requests from the leading-edge computer companies we're talking to, primarily because of graphics, and that favors a FIFO architecture. But they're also tending to build multiuser, multitasking systems that need controller caching and multithreaded operations.

"On the other hand," Cory continues, "in the latest versions of Unix, the operating system itself is doing readahead and setting up caches in main system memory. The customer who's doing this needs the controller to be very good at providing whole tracks of data at one time, but it's not that important that the controller cache what's already being cached elsewhere."

Two SCSI (small computer system interface) host adapters fared very differently in a simulated data base application, performing random reads on from one to seven disk drives. With controller 1, adding an extra drive gains little performance in terms of overall I/O operations/s. By means of intelligent command management and multiple work queues, controller 2 permits near-linear improvements.



Cache management

The power of the 16-bit processors on caching controllers such as those from Ciprico and Interphase is applied, in part, to sophisticated cache-management techniques. Interphase's 68000, for example, manages a multitasking virtual buffer architecture, dynamically allocating and deallocating a 128-kbyte pool of buffers to system processes. "This eliminates read overruns and write underruns found in less sophisticated FIFO-based designs," Godsey says.

But it's inadvisable to assume that because a controller has a cache it's a high-performance board. "Optimal controller implementations segment cache memory," says Moren. Segmentation lets multiple data transfers occur without one transfer flushing the data of another. This is critical for performance under mixed operations—both reads and writes, or reads to different areas of the disk. "The ability to segment a cache also lets you set aside a certain amount of memory for a process," Moren adds, "and then satisfy its data requests without going out to disk."

What does a low-performance cache look like? "The cache implementation on some controllers will flush cache data whenever it receives a command that isn't a read that can be satisfied from the cache," says Moren. "Thus, its performance is good for sequential reads, but performance for mixed reads and/or mixed reads and writes is degraded. Instead of flushing cache data, a high-performance controller will allocate additional cache space for each new operation, preserving the previously cached data, so if the host resumes reading sequentially from the original disk location, that data is still in the cache, saving a disk access."

How does an automatic cache flush affect system performance? "Imagine a simple copy operation," Moren suggests. "The host reads data from a file and writes it to a second, reads more from the first file and writes it to the second, and so on. A controller that flushes the first file's data from its cache on every write to the second file will have to access the disk for each operation, and the advantage of having a cache is lost."

Who needs high performance?

Moren, Corey and Godsey all agree on where the real need for high performance lies today: in minisupercomputers and minimainframes, network file servers, file servers for graphics workstations, multiuser Unix systems, high-performance workstations and sophisticated imaging systems. "It seems like everybody wants high performance these

The MC88000 RISC Multibus II Single Board Computer

The TP880M from Tadpole

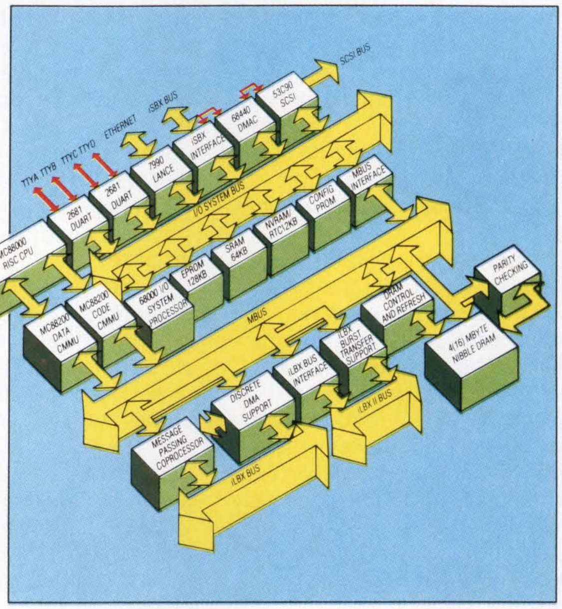
•The Philosophy•

The TP880M design brings together the outstanding performance of the Motorola MC88000 RISC processor set, the power of the full MultibusII/iLBX II interfaces, an MC68000/68440 I/O subsystem with SCSI and Ethernet, and the specially designed Tadpole 88000 RISC optimising C Compiler. The result is an outstanding product that offers users the very best of current SBC technology.

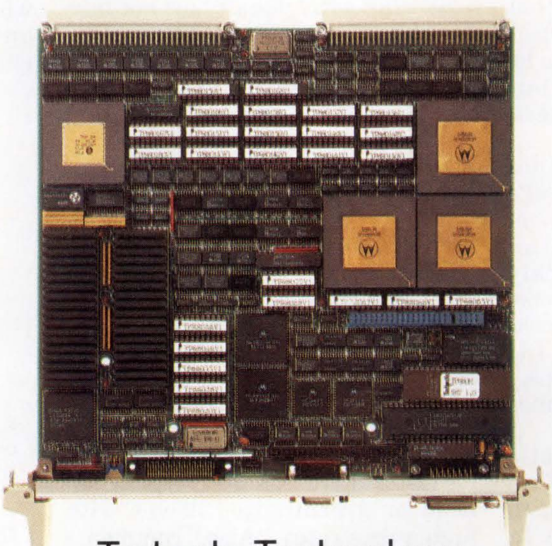
•The Specification•

- MC88100 RISC processor (20-33MHz)
- 16Kb MC88200 cache/MMU instruction cache
- 16Kb MC88200 cache/MMU data cache
- 4-16Mb Nibble mode parity-protected DRAM
- iPSB interface implemented using the Intel Message Passing Coprocessor (MPC)
- iLBX interface and iSBX connector
- I/O Subsystem MC68000/68440 CPU/DMA provides SCSI 4 RS232 ports
- Up to 128Kb EPROM
- 64Kb SRAM and optional ETHERNET networking
- TP-IX V.3.1*
- TP-CDS/88K advanced C development environment
- T-Mon 88K Monitor with extensive SCSI support

•The Design•



•The Evidence•



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the driving force in 32-bit design

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CIRCLE NO. 20

The trouble with Unix

One major hindrance to high-performance data access lies beyond the realm of the disk drive controller. "The Unix file system is not, by its nature, performance-oriented," says William Moren, product manager for Ciprico (Plymouth, MN). Chappell Cory, senior vice-president for marketing operations at Xylogics (Burlington, MA), agrees. "Much of what a controller is doing," says Cory, "is compensating for the weaknesses of Unix, not running in harmony with it."

What's wrong with Unix and its "small" requests? Except for physical transfer rates, according to Moren, all latencies in a disk access are constant, regardless of request size. Thus, the smaller the request, the worse the throughput. For a small request—say, 512 bytes, 1 kbyte or 8 kbytes—these constant latencies are a larger percentage of the total time required to satisfy a request. For larger requests—say, above 128 kbytes—the constant latencies are a much smaller percentage.

Comparing the throughput of a 1-kbyte and 128-kbyte transfer at a limiting disk rate of 3 Mbytes/s and a fixed overhead of 4 ms, the 1-kbyte transfer has a throughput of about 230 kbytes/s; the 128-kbyte transfer, about 2,680 kbytes/s. "Without a doubt," says Moren, "one of the best things a systems builder can do to improve disk throughput, without changes in disk/controller technology, is to request disk data in large pieces. However, this is much easier said than done—imagine the overhaul required for Unix, for instance."

The concept of moving the Unix file system to the disk controller itself is appealing and has been done within closed computer systems. The open architecture bus world, however, is another situation entirely. "The question," says Cory, "is how to create a generic file system interface to the operating system kernel so that all customers will accept it. It seems as though the more intelligence you own, the more objections people have to your version of intelligence."

days," says Moren, "but systems that can get by without it are single-user workstations on a network with a local disk for convenience, and a fair number of systems used in process-control applications."

The need for high performance lies in systems that handle large amounts of data for each application, far more than main memory will allow. Here, the inability to quickly swap data in and out to disk can become the key system bottleneck. "When you're using a 32-bit CPU such as the 68020 with lots of Mips," says Cory, "the I/O channel becomes the performance key."

The need for high performance also lies in sophisticated imaging applications, especially those attempting to display realistic images in motion. In medical imaging, for example, "a quick high-performance controller will let a full, clear CAT scan image be displayed in real time without degradation," says Cory. "In contrast, a slow peripheral controller may only let half of the same image be produced in the same time, perhaps negatively affecting the speed and accuracy of a diagnosis."

So what's the penalty for not having high performance? Response time. User dissatisfaction. "From a philosophical perspective," explains Moren, "if I/O performance can't track improvements in CPU performance, total system performance will hit a wall."

■ What next?

What will be the routes to higher performance in days to come? The advent of better buffer managers and DMA parts, faster RAM, and an increased use of surface-mount parts to increase the functional density of controllers. There will also be head, media and read-chain improvements for faster drives, as well as parallel-head or synchronized drives with higher data rates. "Also," comments Cory, "controllers capable of writing on two or more disks simultaneously will offer another order of improvement."

According to Godsey, "Device-level interfaces such as IPI-2 that allow parallel data streams off a disk drive will certainly contribute to higher performance in the near term." Moren, meanwhile, sees short-term improvements from "more efficient firmware, higher-speed processors and optimized code."

In the long term, Moren hopes to see changes in the way system software manages I/O operations. "The Unix file and I/O systems could use an overhaul, for example, to get away from asking for disk data in small pieces at a time. It could also do a better job of letting the I/O system queue and optimize its requests. One idea many of us have toyed around with is moving the file system to the controller. In this scenario, the operating system would ask for a file by name, with the details of how the file is retrieved left to the controller. As you can well imagine, however, this will take a lot of cooperation between controller houses, system software people and system designers."

What do these and other controller vendors have up their sleeves? New strategies to boost performance. Xylogics, for example, has a new architecture in the offing, and Ciprico has a pair of new application-specific ICs in its laboratories. "This tends to be a leapfrog business," claims Cory. "One of us comes out with something new that beats the others on one front or another; then one of the others does the same. Meanwhile, we all modify what we've done based on what we learn from customer input, and then we apply it to the next generation." □

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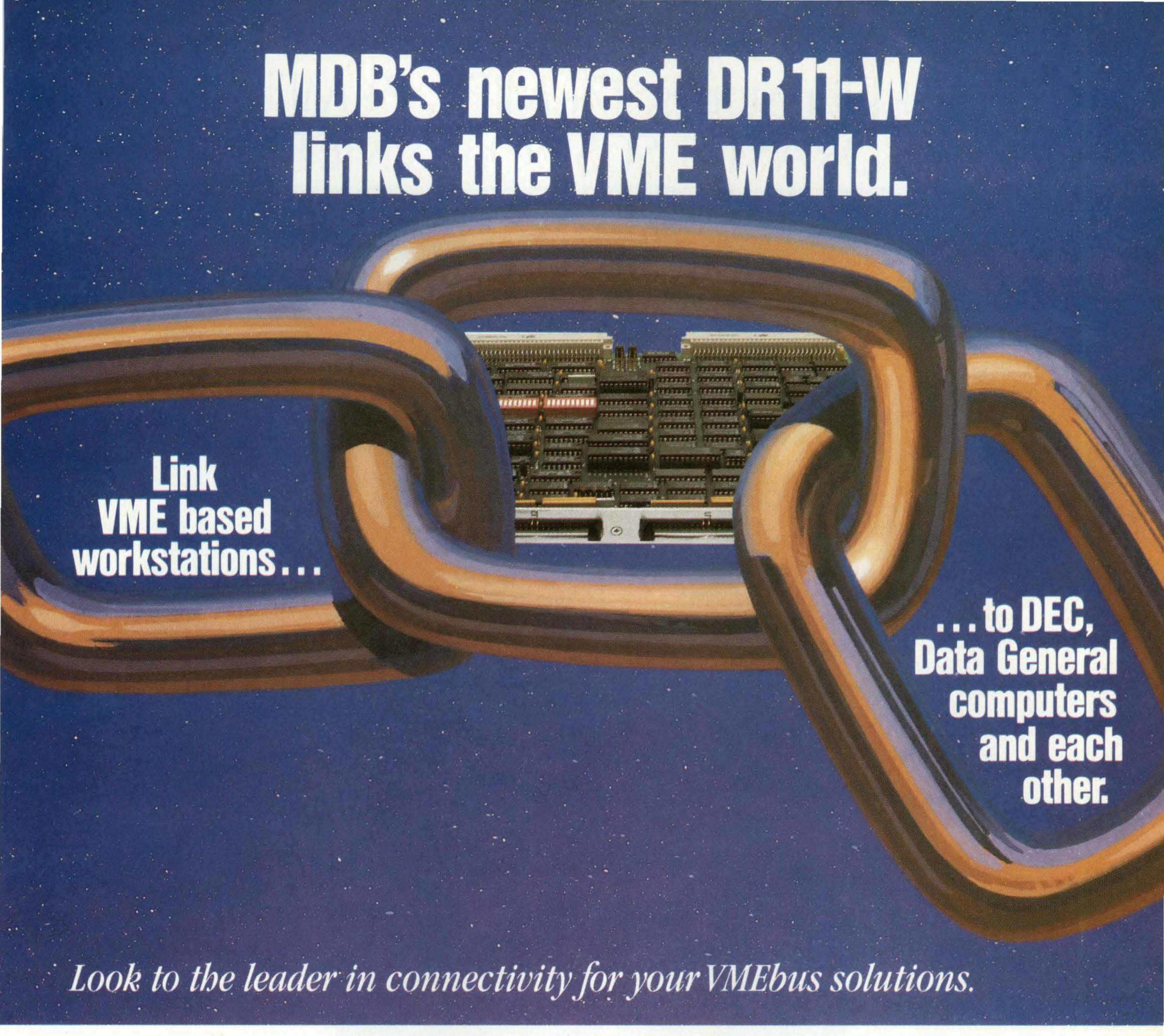

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CIRCLE NO. 21

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The TP880V from Tadpole

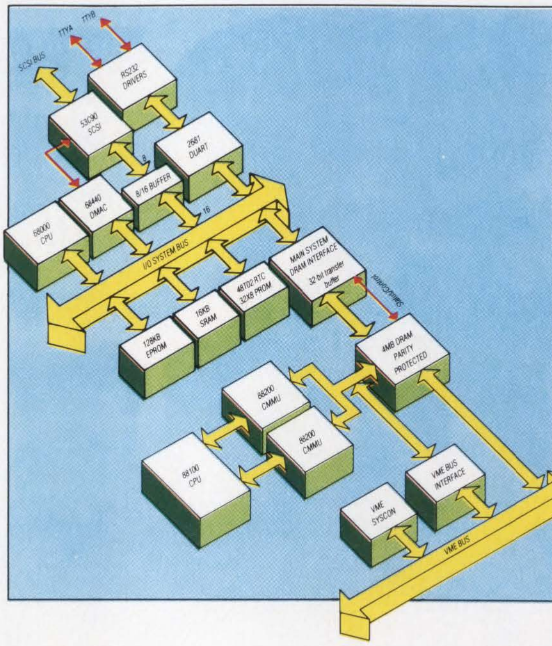
•The Philosophy•

The TP880V is a high performance Single Board Computer for VME based systems. Designed round the Motorola 88000 RISC architecture, the TP880V offers 17MIP, 6MFlop performance at 20MHz and provides a very high level of integration of processing and I/O features on a single card. Tadpole's 88K C Compiler was specially developed to take full advantage of the 88000 RISC architecture.

•The Specification•

- MC88100 RISC processor (20-33MHz)
- 16Kb MC88200 cache/MMU instruction cache
- 16Kb MC88200 cache/MMU data cache
- 4-16Mb Nibble mode parity-protected DRAM
- I/O Subsystem MC68000/ 68440 CPU/DMA
- 53C90 high performance sync/asynchronous SCSI
- 2 RS232 Ports • 128Kb-1Mb EPROM
- Extensive diagnostics capabilities
- Full VME Interface Rev C.1 IEEE 1014
- DTB Master-DTB Slave Syscon interrupter/handler
- 64Kb SRAM battery-backed RTC
- TP-CDS/88K advanced C development environment
- T-Mon 88K Monitor with extensive SCSI support
- TP-IX*

•The Design•



• The Evidence•

Tadpole Technology

the driving force in 32-bit design

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T A D P O L E

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CIRCLE NO. 22

Designers' Buying Guide

Editor's note: *When this Buying Guide was being planned, we were hoping to include details on the most widely used I/O and peripheral boards in all of the popular buses—namely, disk and tape controllers, SCSI adapters, communications controllers and memory boards. Unfortunately, we underestimated the number of boards available and could not do justice to all of them in a single Buying Guide. We've therefore limited this particular Buying Guide to Winchester controllers and SCSI adapters. So that you're not shortchanged, we'll cover the other boards in an upcoming issue of* Computer Design.

Model	Bus	CPU	CPU clock speed (MHz)	SCSI chip(s)	Bus transfers (bits)	Address decoding (bits)	Max bus transfer rate (Mbytes/s)	Memory type and amount (bytes)	Buffer/cache details (bytes)	SCSI target	SCSI initiator	Synch. transfers/ speed (Mbytes/s)
Aeroflex Laboratories 35 S Service Rd, Plainview, NY 11803 (516) 694-6700												**Circle 306**
25	VMEbus	—	—	NCR 5380	8, 16	20	1.5	—	64k SRAM	•	•	no
Applied Control Concepts 6589 N Sidney Pl, Glendal WI 53209 (414) 351-2550												**Circle 315**
AVME-1686	VMEbus	—	—	NCR 5385/5386	16	24	3	256k DRAM	16k to 256k	•	•	yes, 3
Arcom Control Systems Unit 8, Clifton Rd, Cambridge, UK CB1 4WH **Val-Tech (U.S. Distributor)** PO Box 9086, Newark, DE 19714 (302) 738-0500												**Circle 316**
SCSI	STE	none	—	NCR 5380	8	12	—	—	—	•	•	—
Aviv 26 Cummings Pk, Woburn, MA 01801 (617) 933-1165												**Circle 318**
TFC 319	VMEbus	—	—	—	—	16, 24, 32	30	—	—	•	•	yes, 5
Central Data 1602 Newton Dr, Champaign, IL 61821 (800) 482-0315												**Circle 323**
CD22/ 45000512	Multibus II	80186	12.5	WD33C93	8, 16, 32	32	40	128k EPROM, 64k SRAM	512k DRAM	•	•	4
CD22/ 45002048	Multibus II	80186	12.5	WD33C93	8, 16, 32	32	40	128k EPROM, 64k SRAM	2,048 DRAM	•	•	4
Ciprico 2955 Xenium Ln, Plymouth, MN 55441 (612) 559-2034												**Circle 326**
Rimfire 1500	Multibus I	80186	10	WD33C-93A, WD33C92	8, 16	24	5	16k SRAM, 64k EPROM	1k FIFO buffer	•	•	5
Rimfire 2500	Multibus II	80186	10	WD33C92	8, 16, 24, 32	12 (intercon. space)	32	64k SRAM, 64k EPROM	256k cache	•	•	5
Rimfire 3510	VMEbus	80186	10	WD33C-93A, WD33C92	8, 16, 32	16, 24, 32	30	64k SRAM, 64k EPROM	45k FIFO	•	•	5
Compcontrol 15466 Los Gatos Blvd, Suite 109-365, Los Gatos, CA 95032 (408) 356-3817												**Circle 329**
CC74/174	VMEbus	—	—	NCR 5385/ 5386	8, 16	16, 24	—	—	—	•	•	—
CC97	VMEbus	68000	16	WD33C93	8, 16	24	—	2M DRAM, 256k EPROM	2M DRAM, 256k EPROM	•	•	—
Computer Dynamics 107 S Main St, Greer, SC 29651 (803) 877-8700												**Circle 330**
SCSI floppy	STD	all	12	5380	8	16	1	0	0	•	•	no
Dilog 1555 S Sinclair St, Anaheim, CA 92806 (714) 937-5700												**Circle 346**
SQ703	Q-Bus	—	—	NCR 8372	—	16, 18, 22	1.5	64k RAM	FIFO buffer	•	•	—

Asynch. transfers/ Speed (Mbytes/s)	Single-ended operation	Differential operation	Disconnect/reconnect	Floppy interface	Tape interface	Operating system drivers	Real-time executive	Board size (Q-Bus, Unibus)	Message-passing coprocessor (Multibus II)	Form factor (VMEbus)	Comments	OEM price
1.5	•	•	•	SCSI	no	Sun Unix	none	—	—	6U	mil-spec conduction cooled	—
1.5+	•		•	SCSI	no	none	none	VME, 9U	no	VME	—	$800
—				—	—	—	—	3U	—	—	communicates with up to 7 devices	$265.47
2	•	•	•	SCSI	—	Unix	—	—	—	6U	—	—
1.5	•		•	WD37C65	no	RMX, Unix	prop.	Multibus II, 6U	yes	6U	—	$1,895
1.5	•		•	WD37C65	no	RMX, Unix	prop.	Multibus II, 6U	yes	6U	—	$3,125
2	•	•	•	ANSI 3½ in. and 5¼ in.	SCSI	Unix V.3, iRMX 286, iRMX 86	yes	—	—	—	circular command queue, pass-through software interface	$875
2	•	•	•	ANSI 3½ in. and 5¼ in.	SCSI	Unix V.3, iRMX 286	yes	—	yes	—	same as above	$1,975
2	•	•	•	ANSI 3½ in. and 5¼ in.	SCSI	Unix V, 4.2 BSD, Sun-OS, OS-9, VRTX, VersaDOS	yes	—	—	6U	same as above	$880
1.5	•	•	•	SCSI	SCSI	OS-9, Unix	—	VME	—	6U	4 channel DMA controller	$1,165
1.5	•		•	SCSI	SCSI	OS-9	OS-9	VME	—	6U	same as above	$2,720
1.5	•		•	Shugart or SCSI	SCSI	MS-DOS	MX	STD Bus	—	—	standard floppy interface plus SCSI	—
1.5	•		•	no	SCSI	none	none	dual	no	—	DEC TU driver compat.	—

Model	Bus	CPU	CPU clock speed (MHz)	SCSI chip(s)	Bus transfers (bits)	Address decoding (bits)	Max bus transfer rate (Mbytes/s)	Memory type and amount (bytes)	Buffer/cache details (bytes)	SCSI target	SCSI initiator	Synch. transfers/ speed (Mbytes/s)
Dilog 1555 S Sinclair St, Anaheim, CA 92806 (714) 937-5700												**Circle 346**
SQ706	Q-Bus	—	—	NCR 8372	—	16, 18, 22	1.5	64k RAM	FIFO buffer	•	•	—
SQ716	QBus	—	—	NCR 8372	—	16, 18, 22	3	64k RAM	FIFO buffer	•	•	3
DSP Design LTD Unit 1, Apollo Studios, Charlton Kings Rd, London, NW5 2SB 44-1 482-1773 **Val-Tech (U.S. Distributor)** PO Box 9086, Newark, DE 19714 (302) 738-0500												**Circle 339**
SF840	STE	none	—	5380	8	20	5	—	—	•	•	—
Dual Systems 3906 Trust Way, Hayward, CA 94545 (415) 785-8890												**Circle 348**
VUSC	VMEbus	68000	10	NCR 5830	8, 16	32	4 (burst)	512k DRAM, 64k PROM	—	•	•	no
Emulex 3545 Harbor Blvd, Costa Mesa, CA 92626 (714) 662-5600												**Circle 350**
VH01	VMEbus	68000	12	Emulex ESP	16, 32	16, 24	—	64 × 16-bit dual ported FIFO	—		•	4.8
UC04	Q-Bus	LSI II, μPDP II, μVAX I, II	—	NCR	0 to 4 bytes	22	—	—	20k data buffer		•	—
UC14	Unibus	PDP11/ 04-11/70, VAX-II	—	NCR	0 to 128 kwords	18	—	—	20k data buffer		•	—
Force Computers 3165 Winchester Blvd, Campbell, CA 95008 (408) 370-6300												**Circle 353**
ISCSI-I	VMEbus	68010	10	NCR 5386S	8/16	A24	4	128k EPROM, 128k SRAM	128k SRAM	•	•	no
Gespac 50 W Hoover Ave, Suite 2, Mesa, AZ 85202 (602) 962-5559												**Circle 359**
GESCSI-1	G-96	68010	12.5	Fujitsu	—	24	20	256k RAM, 64k ROM	—	•	•	4.8
GW Three 7623 Fullerton Rd, Springfield, VA 22153 (703) 451-2043												**Circle 355**
SSB-4	STD	none	—	NCR 5380	8	16	1.5	none	—	•	•	no
Integrated Solutions 1140 Ringwood Ct, San Jose, CA 95131 (408) 943-1902												**Circle 366**
VMEbus-SCSI/U	VMEbus	Z8000	—	—	—	24	1.5	16k RAM	16k			no
VMEbus-SCSI	VMEbus	Z8002	—	NCR	8	24	1.5	—	—			no
Interphase 2925 Merrell Rd, Dallas, TX 75229 (214) 350-9000												**Circle 368**
V/SCSI 4210	VMEbus	68000	12.5	Fujitsu	16, 32	16, 24, 32	30	—	128k RAM virtual buffer	•	•	5
Introl 2675 Patton Rd, St Paul, MN 55113 (612) 631-7600												**Circle 369**
Introl 300	VMEbus	68000	10	Fujitsu 87030	32, 16	16, 24, 32	—	16k EPROM, 16k SRAM	2k FIFO	•	•	4

Asynch. transfers/ speed (Mbytes/s)	Single-ended operation	Differential operation	Disconnect/reconnect	Floppy interface	Tape interface	Operating system drivers	Real-time executive	Board size (Q-Bus, Unibus)	Message-passing coprocessor (Multibus II)	Form factor (VMEbus)	Comments	OEM price
1.5	•		•	SCSI	no	none	none	dual	no	—	DEC DU driver compat.	—
1.5		•	•	SCSI	no	none	none	dual	no	—	same as above	—
—	•		•	4 floppies	no	CP/M +, Z-system	—	3U	no	3U	—	$400
1.5	•			SA450	SCSI	Unix 5.2, pSOS 68k	pSOS, 68k	—	—	6U	ST506 interface, SA450 interface	$1,014
3 Mb/s	•	•	•	SA450	no	Unix	none	no	no	6U	optical support	$926 to $972
2 Mb/s	•		•	none	Cipher 540, QIC-36	Unix	none	dual Q-Bus	—	—	internal self-test, optical support	$1,224 to $1,564
2 Mb/s	•		•	none	Cipher 540, QUC-36, QIC-44	Unix	none	quad Unibus	—	—	optical support, firmware resident diagnostics	$1,496 to $2,006
1.5	•		•	SA450	—	yes	yes	6.3×9.2	—	6U	floppy interface (SA450)	$1,690
1.2				SCSI	SCSI	yes	yes	VME, 3U	yes	3U	—	$1,101
1.5	•			SCSI	SCSI	PDOS	PDOS	STD	no	STD	battery backed; clock/calendar	$195
1.5			•	—	—	4.3 BSD	no	—	—	6U	—	—
1.5			•	—	—	4.3 BSD	no	—	—	6U	—	—
1.5	•	•	•	none	SCSI	Unix 4.2 BSD, Unix 4.3 BSD	—	—	no	6U	dual independent SCSI ports	—
1.5	•	•	•	SCSI	SCSI	Unix, Sun, OS-9	—	VME, 6U	—	6U	—	—

Model	Bus	CPU	CPU clock speed (MHz)	SCSI chip(s)	Bus transfers (bits)	Address decoding (bits)	Max bus transfer rate (Mbytes/s)	Memory type and amount (bytes)	Buffer/cache details (bytes)	SCSI target	SCSI initiator	Synch. transfers/ speed (Mbytes/s)
IO 2430 N Huachuca Dr, Tucson, AZ 85745 (800) 426-2876												**Circle 363**
IOVME402	VMEbus	—	—	none	8	24	0.18	none	—		•	no
IOVME403	VMEbus	—	—	NCR 5380	16	24	0.6	none	—	•	•	no
IOVME303	VMEbus	none	—	WD33C93	16, 32	16, 32	4.0	2k NV	1k	•	•	yes
Ironics 798 Cascadilla St, Ithaca, NY 14850 (607) 277-4060												**Circle 370**
IV-3273	VMEbus	none	—	NCR 5380	8, 16, 32	32	6	none	—	•	•	—
IV-1602	VMEbus	68010	10, 12.5	NCR 5380	16	24	4	1M DRAM	—	•	•	no
Matrix 1203 New Hope Rd, Raleigh, NC 27610 (919) 833-2000												**Circle 376**
SASI	STD	6809	8	discrete logic	8	16	2	—	—			—
Megadata 35 Orville Dr, Bohemia, NY 11716 (516) 589-6800												**Circle 378**
M80780	Multibus	—	—	NCR 53C90	16	24	10	—	—	•	•	4
Micro Industries 691 Greencrest Dr, Westerville, OH 43081 (614) 895-0404												**Circle 381**
mSMP-E346	SMP	none	—	none	8	24	—	—	—	•	•	no
mAMS-M340-A1	AMS	80186	8	NCR 5380	8, 16	24	1.5	1M DRAM, 64k EPROM	—	•	•	no
Micro-Link 14602 N U.S. Hwy 31, Carmel, IN 46032 (800) 428-6155												**Circle 384**
VME620	VMEbus	—	—	WD33C93	8	16, 24	2	512k DRAM opt	512k DRAM	•	•	yes, 2.0
STD603	STD	—	—	P10	8	8	1	none	—			no
Micro/Sys 1011 Grand Central Ave, Glendale, CA 91201 (818) 244-4600												**Circle 385**
SB8740	STD	—	—	—	8	8	1	none	—			—
Microproject 4551 Glencoe Ave, Suite 225, Marina Del Rey, CA 90292 (213) 306-8000												**Circle 390**
2501-7718-5	VMEbus	68020	12.5, 16	SCN2641	16, 32	24, 32	26.7	256k EPROM, 2k NOVRAM	128k SRAM	•	•	4
2501-7518-7	VMEbus	none	—	prop.	16, 32	24, 32	26.7	—	—	•	•	4
Mini Computer Technology 696 E Trimble Rd, San Jose, CA 95131 (408) 435-1616												**Circle 391**
MCT6008	VMEbus	68000	24	Fuji MB87030	8	16	20	256k PROM	256k SRAM, 2 to 128k buffers	•	•	4

Asynch. transfers/ speed (Mbytes/s)	Single-ended operation	Differential operation	Disconnect/reconnect	Floppy interface	Tape interface	Operating system drivers	Real-time executive	Board size (Q-Bus, Unibus)	Message-passing coprocessor (Multibus II)	Form factor (VMEbus)	Comments	OEM price
0.18	•			SCSI	9 track	PDOS, Forth	none	—	—	6U	2 serial ports async, 16-bit counter/timer	$708
0.60	•		•	SCSI	9 track	PDOS, Forth	none	—	—	6U	2 sync/async serial ports	$876
4 Mb	•		•	yes	no	PDOS, Forth	none	—	—	6U	VME system controller, calendar/clock	$900
—				SCSI	SCSI	Unix V.2	pSOS	VME, 6U	no	6U	—	$915
—				SCSI	SCSI	Unix V.2	pSOS	VME, 6U	—	6U	SBC w/SCSI	$1,530
—				no	yes	OS-9 and flex	none	STD	no	—	—	$297
1.5	•	•	•	yes	SCSI	Unix V.2	—	—	—	—	—	—
1.5	•			SCSI	no	none	none	—	no	3U	—	$325
1.5	•			1797 FDC	no	none	none	—	no	6U	2 RS232 serial ports, 3 counter/timers	$2,545
1.5	•		•	SCSI	no	PDOS	PDOS	—	—	3U	DMA (opt) activity/ error lights	$348.50
1	•			SCSI	no	CP/M, PDOS	PDOS	—	—	—	DMA interface	$143.50
—	•			SASI/SCSI	no	CP/M	none	STD Bus (4.5 × 6.9)	no	—	drive independent transfers & prog.	$140
1.5	•	•	•	—	SCSI	Unix, Sun-OS, OS-9	—	VME	no	6U	dynamic bus throttling	—
1.5	•		•	—	SCSI	same as above	—	VME	no	6U	—	—
1.5	•	•	•	SCSI	SCSI	Unix	none	VME	—	6U, 6U	—	$1,390

Model	Bus	CPU	CPU clock speed (MHz)	SCSI chip(s)	Bus transfers (bits)	Address decoding (bits)	Max bus transfer rate (Mbytes/s)	Memory type and amount (bytes)	Buffer/cache details (bytes)	SCSI target	SCSI initiator	Synch. transfers/ speed (Mbytes/s)
Mizar 1419 Dunn Dr, Carrollton, TX 75006 (800) 635-0200												**Circle 393**
MZ 75811	VMEbus	—	—	WD33C-92/3	32	24	—	—	—	•	•	4
MZ 8500	VMEbus	—	—	PALs	16	16	—	—	—	•	•	4
Motorola, Microcomputer Div. 2900 S Diablo Way, DW283, Tempe, AZ 85282 (602) 438-3518												**Circle 397**
MVME 327A	VMEbus	68010	10	WD33C93	8	16	16 VMEbus	256k EPROM, 128k SRAM	1k FIFO	•	•	4
Moya 9001 Oso Ave, Unit C, Chatsworth, CA 91311 (818) 700-1200												**Circle 398**
135	STD	STD	9.216	NCR 53C80	8	19	2.3	—	—	•	•	no
NCR, SCSI Technology Group 3718 N Rock Rd, Wichita, KS 67226 (316) 636-8510												**Circle 399**
ADP-32	Multibus I	—	—	NCR 5380	8, 16	8, 16	1.3 async	8k PROM, 128 RAM	—	•	•	—
ADP-33	VMEbus	—	—	NCR 53C90	16, 32	16, 24, 32	1.3 async, 4 sync	1k×16 RAM	—	•	•	up to 5
Omnibyte 245 W Roosevelt Rd, W Chicago, IL 60185 (800) 638-5022												**Circle 404**
OB68K/ VSBC1	VMEbus	68000/10	12.5	AMD5380	—	24	40	512k DRAM	512k DRAM/none	•	•	—
OB68K/VIO	VMEbus	none	—	AMD5380	—	24	40	none	none/none	•	•	—
OB68K/ VSBC20	VMEbus	68020	12.5, 16, 20, 25	AMD5380	—	16, 24, 32	40	1M DRAM	1M DRAM/ none	•	•	—
OB68K/ MSBC30	Multibus	68030	16, 20, 25, 33	AMD5380	—	16, 24, 32	20	2M DRAM	2M DRAM/ none	•	•	—
Pep Modular Computers 600 N Bell Ave, Pittsburgh, PA 15106 (412) 279-6661 Am klosterwald 4, D-8950 kaufloeuren, Germany 08341/81001												**Circle 408**
VSCSI	VMEbus	—	—	53C90	8	16, 24	4	—	2×1k FIFO	•	•	4
Performance Technologies 435 W Commercial St, East Rochester, NY 14445 (716) 586-6727												**Circle 409**
PT-VME 400	VMEbus	68010	10	NCR 5385E	16	24	1.2	512k DRAM	512k buffer	•	•	no
PT-VME 418	VMEbus	68020	12.5	WD33C-92/3	32	32	12.5	256k DRAM	256k buffer	•	•	4
PT-VME 420	VMEbus	68020	12.5	WD33C-92/3	32	32	12.5	2M DRAM	512k buffer	•	•	5
PT-VME 422	VMEbus	68020	12.5	WD33C-92/3	32	32	12.5	2M DRAM	2M buffer	•	•	5
Philips Electronic Instruments 85 McKee Dr, Mahwah, NJ 07430 (203) 592-3800 **Philips Industrial Automation** PO Box 218, 5600 MD Eindhoven, The Netherlands (31) 40 785509												**Circle 410**
PG3150	VMEbus	none	—	NCR 5385	8, 16	24	1.5	—	—	•	•	no

Asynch. transfers/ speed (Mbytes/s)	Single-ended operation	Differential operation	Disconnect/reconnect	Floppy interface	Tape interface	Operating system drivers	Real-time executive	Board size (Q-Bus, Unibus)	Message-passing coprocessor (Multibus II)	Form factor (VMEbus)	Comments	OEM price
1.5 Mb/s	•	•	•	SCSI	no	OS-9, VRTX, VxWorks	OS-9, VRTX, VxWorks	—	—	6U	—	$956
1.5 Mb/s	•		•	SCSI	no	OS-9, VRTX, VxWorks	OS-9, VRTX, VxWorks	—	—	3U	—	$295
115	•		•	yes	SCSI	system V/68, VersaDOS	none	—	—	6U	—	$1,995
1.1	•		•	SCSI	SCSI	CP/M, maxDOS	yes	STD	no	—	board mounted drive, clock/calendar	$220
1.3	•	•	•	—	—	samples avail. (C source)	—	Multibus	—	—	—	$275 to $301
up to 2	•		•	—	—	samples avail. (Unix)	—	VME, 6U	—	6U	—	$797
1	•		•	SCSI	SCSI	none	none	—	—	6U	up to 2 SCSI ports	$1,157
0.5	•		•	SCSI	SCSI	none	none	—	—	6U	up to 4 SCSI ports	$507
1	•		•	SCSI	SCSI	none	none	—	—	6U	—	$2,197
1	•		•	SCSI	SCSI	none	none	—	—	—	requires 2 slots	—
3	•		•	SCSI	SCSI	OS-9, PDOS	none	no	no	3U	low printer CMOS technology	—
1.5	•		•	yes, 350	no	Unix	yes	—	—	6U	supports target	$1,500
1.5	•		•	yes, 350	no	Unix/Sun	yes	—	—	6U	supports target	$1,350
2	•	•	•	yes, 350	no	Unix/Sun	yes	—	—	6U	same as above	$1,675
2	•	•	•	yes, 350	no	Unix/Sun	yes	—	—	6U	same as above, user-defined commands	$2,425
1.5	•		•	SCSI	SCSI	ERM, Uni-Five	—	—	—	6U	68450 DMA controller	$1,550 approx

Model	Bus	CPU	CPU clock speed (MHz)	SCSI chip(s)	Bus transfers (bits)	Address decoding (bits)	Max bus transfer rate (Mbytes/s)	Memory type and amount (bytes)	Buffer/cache details (bytes)	SCSI target	SCSI initiator	Synch. transfers/ speed (Mbytes/
Qualogy 2241 Lundy Ave, San Jose, CA 95131 (408) 434-5200												**Circle 412**
QLC-1100	Unibus	NEC U50	28.5	WD33C93	18	16	2.5	—	64k DRAM buffer		•	0.75
Radstone Technology One Blue Hill Plaza, Pearl River, NY 10965 (914) 735-4661												**Circle 414**
SCSI-1/1A	VMEbus	68008	8	5380	32	16, 24, 32	6	4k SRAM	2k FIFO		•	no
PMV-SCSI-1	VMEbus	68000	8	—	32	16, 24, 32	6	512k EPROM; 256k SRAM	2k FIFO; 8k dual port RAM		•	no
Sigma Information Systems 3407 E LaPalma Ave, Anaheim, CA 92806 (714) 630-6553												**Circle 419**
SA-HA-11	Q-Bus	μVAX, μPDP II	20	not avail.	16	22	0.8	—	2 data		•	—
SDC-RQD11-SCSI	Q-Bus	μVAX, μPDP II	20	not avail.	16	22	1.8	—	48k buffer		•	—
Sun Microsystems, OEM Board Products 2550 Garcia Ave, Mountain View, CA 94043 (415) 960-1300												**Circle 429**
3E340	VMEbus	—	—	NCR 5380	8, 16, 32	24, 32	6.4	—	64k SRAM data buffer		•	no
501-1236	VMEbus	—	—	NCR 5380	8, 16, 32	24	7	—	512k FIFO		•	no
Systek 1027 N Kellogg St, Kennewick, WA 99336 (509) 735-1200												**Circle 433**
6320-0	STD	none	—	NCR 5380	8	20	PD	—	32k SRAM	•	•	no
Tadpole Technology 1601 Trapelo Rd, Waltham, MA 02154 (617) 890-8898												**Circle 455**
TPISCV	VMEbus	68020	16	NCR 5386	32	24, 32	16	64k EPROM, 2M DRAM	DRAM cache buffer, copy-back look ahead	•	•	no
TPDSCM	Multibus II	68020	14	NCR 53C90 (2)	32	—	40	128k EPROM; 1M DRAM	DRAM cache buffer, copy-back, look ahead	•	•	4
VME 542 Valley Way, Milpitas, CA 95035 (408) 946-3833												**Circle 441**
V500	VMEbus	68008	6	NCR 5385E	8, 16	16, 24	1.5	8k PROM; 8k SRAM	—	•	•	no
V510	VMEbus	RTX 2000	20	WD33C93	8, 16, 32	16, 24, 32	16	64k EPROM; 64k SRAM	128k SRAM buffer	•	•	5

Asynch. transfers/ speed (Mbytes/s)	Single-ended operation	Differential operation	Disconnect/reconnect	Floppy interface	Tape interface	Operating system drivers	Real-time executive	Board size (Q-Bus, Unibus)	Message-passing coprocessor (Multibus II)	Form factor (VMEbus)	Comments	OEM price
1.5	•		•	no	TMSCP	TMSCP	—	quad	—	—	optical (WORM)	—
4	•		•	—	—	Unix, OS-9, VersaDOS	—	VME	—	6U	4 Mb/s SCSI transfer rate sustained	—
1.5	•	•	•	—	—	Unix, OS-9 VersaDOS, VRTX-32, ARTX	—	VME, 6U	—	6U	1.5 Mb/s sustained avail	—
—	•			SASI	SASI	none	VMS, RSX, RSTSE, RT11, TSX, Unix	dual	—	—	controls 7 devices	$271
—	•			SCSI	SCSI	not required	VMS, RSX, RSTSE, DSM, RT11, TSX, Unix	dual	—	—	controls 7 devices	$928
1.5	•		•	SCSI	SCSI	incl. in Sun-OS	no	—	no	6U	for use w/3E120 CPU; on-board Ethernet	$1,800
1.5	•		•	SCSI	SCSI	incl. in Sun-OS	no	—	no	9U	—	$1,200
1.5	•		•	SCSI	SCSI	MS-DOS	—	STD (4.5×6.5)	no	—	32 kb SRAM cache	$413
1.5	•		•	SCSI	SCSI	Unix Sys V	prop	VME	—	6U	—	—
3	•		•	SCSI	SCSI	Unix Sys V	prop	Multibus II	yes	—	full Intel transport firmware support	—
1.5	•		•	no	no	none	none	—	—	6U	memory to memory DMA	$842
1.5	•	•	•	no	no	Unix	RTX	—	—	6U	12 Mips CPU memory to memory DMA	$1,170

■ DESIGNERS' BUYING GUIDE/SCSI Host Adapters

Model	Bus	CPU	CPU clock speed (MHz)	SCSI chip(s)	Bus transfers (bits)	Address decoding (bits)	Max bus transfer rate (Mbytes/s)	Memory type and amount (bytes)	Buffer/cache details (bytes)	SCSI target	SCSI initiator	Synch. transfers/ speed (Mbytes/
VME Specialists 558 Brewster Ave, Redwood City, CA 94063 (415) 364-3328												**Circle 442**
VME620	VME 3U	—	—	NCR 8372	8	24	2	512k dual-ported RAM	512k dual-ported RAM	•	•	2
VME620 NR	VME 3U	—	—	NCR 8372	8	24	2	—	—	•	•	2
Winsystems PO Box 121361, Arlington, TX 76012 (817) 274-7553												**Circle 447**
MCM-SCSI	STD, CMOS STD	8088, 80186, 80286	8	L53C80	8	20	4	none	—	•	•	no
Xycom 750 N Maple Rd, Saline, MI 48176 (800) 367-7300												**Circle 449**
XVME-405	VMEbus	64180	6	NCR 5380	8	24	0.6	64k PROM	128k SRAM	•	•	no
Xylogics 53 Third Ave, Burlington, MA 01803 (617) 272-8140												**Circle 450**
720	VMEbus	8031	16	Fujitsu 87033	16, 32	32	16	256k PROM	8k FIFO RAM	•	•	5
Ziatech 3433 Roberto Ct, San Luis Obispo, CA 93401 (805) 773-5854												**Circle 453**
ZT 8850	STD	none	5, 8	discrete	8	8, 16	8	—	—		•	no

■ Winchester Controllers (VMEbus)

Model	Bus transfers (bits)	Address decoding (bits)	CPU	CPU clock speed (MHz)	DMA channels (no. and width)	Max bus transfer rate (Mbytes/s)	Operating system drivers	Real-time executive	No. of Winchester disk drives	Disk type/speed	Interleave factor	Zero latency read/wri
Aviv 26 Cummings Pk, Woburn, MA 01801 (617) 933-1165												**Circle 318**
DFC 317	8, 16, 32	16, 24, 32	—	24	—	30	Unix	—	4	SMD	1:1	—
DFC 304	16, 32	16, 24, 32	—	20	—	20	Unix	—	4	ESDI	1:1	—
Ciprico 2955 Xenium Ln, Plymouth, MN 55441 (612) 559-2034												**Circle 326**
Rimfire 3200	8, 16, 32	16, 24, 32	80186	10	2 16-bit	30	Unix V, BSD4.2, Sun OS, VRTX, OS-9	yes	2	SMD-E, 24 MHz	1:1	yes
Rimfire 3220	8, 16, 32	16, 24, 32	80186	10	2 16-bit	30	same as above	yes	4	SMD-E, 24 MHz	1:1	yes
Rimfire 3400	8, 16, 32	16, 24, 32	80186	8	2 16-bit	30	same as above	yes	2	ESDI, 20 MHz	1:1	yes
Dual Systems 3906 Trust Way, Hayward, CA 94545 (415) 785-8890												**Circle 348**
VUSC	8, 16	—	68000	10	0	—	Unix 5.2, P505 68k	—	8	ST506, 5 Mbits/s, SCSI, 1.5 Mbits/s	—	—

Asynch. transfers/ speed (Mbytes/s)	Single-ended operation	Differential operation	Disconnect/reconnect	Floppy interface	Tape interface	Operating system drivers	Real-time executive	Board size (Q-Bus, Unibus)	Message-passing coprocessor (Multibus II)	Form factor (VMEbus)	Comments	OEM price
2	•		•	SCSI	SCSI	OS-9	OS-9	VME, 3U	no	3U	single high, dual-ported RAM	$650
2	•		•	SCSI	SCSI	OS-9	OS-9	VME, 3U	no	3U	single high	$400
4	•		•	WD37C65 supports 3½ in., 5¼ in.	no	none	none	STD	no	STD	avail. in CMOS or NMOS/TTL	$375
0.6	•		•	SCSI	SCSI	OS-9, PDOS	OS-9, PDOS	—	—	3U, 6U	—	$720
1.5	•	•	•	via daughter card	SCSI	Unix, Sun-OS	prop	VME, 6U	no	6U	supports Dynathrottle	$1,375
1	•			yes	yes	STD DOS	none	—	—	—	DMA oper.	$274

Memory type and amount (bytes)	Buffer/cache details	Error detection details	Error correction details	Floppy interface	Overlapped seeks	Lookahead seeks	Command optimization	Scatter/gather commands	Form factor	Bus master/slave	Intrpt handler/gen levels	Block transfers	OEM price
512k	—	48-bit ECC	—	—	•			•	9U	no	—	yes	—
512k	—	48-bit ECC	—	—	•			•	6U	no	—	yes	—
64 kbyte SRAM, EPROM	512 kbyte	48-bit ECC	15-bit single burst	none	•	•	•	•	6U	yes	0/7	yes	$1,931
64 kbyte SRAM, EPROM	512 kbyte	48-bit ECC	15-bit single burst	none	•	•	•	•	9U	yes	0/7	yes	$2,305
64 kbyte SRAM, EPROM	512 kbyte	48-bit ECC	15-bit single burst	none	•	•	•	•	6U	yes	0/7	yes	$1,295
128 FIFO, 512k RAM, 64k ROM/ EPROM	—	—	—	2 SA450					6U	yes	0/7	—	$1,018

Model	Bus transfers (bits)	Address decoding (bits)	CPU	CPU clock speed (MHz)	DMA channels (no. and width)	Max bus transfer rate (Mbytes/s)	Operating system drivers	Real-time executive	No. of Winchester disk drives	Disk type/speed	Interleave factor	Zero latency read/wri
Dual Systems 3906 Trust Way, Hayward, CA 94545 (415) 785-8890												**Circle 348**
VESDI-32	8, 16	—	68000	10	0	—	Unix 5.2, P505 68k	—	4	15 Mbits/s	yes	yes
VSMD-32	8, 16	—	68000	10	0	—	Unix 5.2, P505 68k	—	—	—	yes	yes
Electronic Modular Systems 1325 Capital Pkwy, Carrollton, TX 75006 (214) 446-2900												**Circle 349**
HD-1	8, 16	16, 24	6809	10	4 16-bit	—	Unix	yes	4	ST506, 5 Mbits/s	4:1	no
Emulex 3545 Harbor Blvd, Costa Mesa, CA 92626 (714) 662-5600												**Circle 350**
VM21	8, 16, 32	16/24	68000	12.5	1 16-/ 32-bit	5	Unix	no	4	ESDI, 20 Mbits/s	1:1	yes
VM31	8, 16, 32	16/24	68000	12.5	1 16-/ 32-bit	5	Unix	no	4	SMD-E, 24 Mbits/s	1:1	yes
Force Computers 3165 Winchester Blvd, Campbell, CA 95008 (408) 370-6300												**Circle 353**
WFC-1	8, 16	24/16	WD	—	—	4	yes	yes	3	ST506, 5 Mbits/s	—	—
ISCSI-1	8, 16	24	68010	10	—	4	yes	yes	—	SCSI, 1.5 Mbits/s	—	—
Integrated Solutions 1140 Ringwood Ct, San Jose, CA 95131 (408) 943-1902												**Circle 366**
VME-SCSI/11	8, 16	24	Z8000	—	—	1.5	—	—	—	—	—	—
Interphase 2925 Merrell Rd, Dallas, TX 75229 (214) 350-9000												**Circle 368**
V/SMD 3200	8, 16, 32	16, 24, 32	68000	12.5	—	—	Unix 4.2 BSD, Unix 4.3 BSD	—	4	SMD, SMD-E, 24 Mbits/s	1:1	yes
V/SMD 4200	16, 32	16, 24, 32	68000	12.5	1 16-/ 32-bit	30	same as above	—	4	SMD, SMD-E, 24 Mbits/s	1:1	yes
V/ESDI 4201	16, 32	16, 24, 32	68000	10	—	30	same as above	—	4	ESDI, 24 Mbits/s	1:1	yes
Matrix 1203 New Hope Rd, Raleigh, NC 27610 (919) 833-2000												**Circle 376**
MS-HFD	16	24	68454	16	1 16-bit	5	yes	no	2	ST506, 5 Mbits/s	prog.	no
Micro Industries 691 Greencrest Dr, Westerville, OH 43081 (614) 895-0404												**Circle 381**
PG3101A	16	24	8X305	—	1 16-bit	—	none	no	2	ST506, SA1000, 5 Mbits/s	2:1	no
Microproject 4551 Glencoe Ave, Suite 225, Marina Del Rey, CA 90292 (213) 306-8000												**Circle 390**
2501-7718-5	16, 32	—	68020	12.5, 16.7	—	26.7	Unix, pSOS, OS-9, MTOS-UX, VRTX	no	7	SCSI	—	—
2501-7518-7	16, 32	—	none	—	—	26.7	same as above	—	7	SCSI	—	—

Memory type and amount (bytes)	Buffer/cache details	Error detection details	Error correction details	Floppy interface	Overlapped seeks	Lookahead seeks	Command optimization	Scatter/gather commands	Form factor	Bus master/slave	Intrpt handler/gen levels	Block transfers	OEM price
—	—	48-bit ECC	—	—					6U	yes	0/7	—	$1,194
—	—	48-bit ECC	—	—					6U	yes	0/7	—	$1,434
12k RAM	none	32-bit ECC	burst mode	no	•		•		6U	no	0/7	yes	$1,234
512k RAM	512-byte dual-ported, LRU, read-ahead/look around	48-bit ECC	11-bit burst	none	•	•	•	•	6U	yes	1/7	no	$1,204
512k RAM	same as above	48-bit ECC	11-bit burst	none	•	•	•	•	6U	yes	1/7	no	$1,426
—	—	—	—	SA460					6U	no	0/7	no	$1,000
12k EPROM, 128k SRAM	—	—	—	SA460					6U	yes	0/7	no	$1,690
16k RAM	16k	self test	—	—					6U	yes	—	—	—
—	—	48-bit ECC	—	—					6U	yes	—	—	—
—	128 kbyte	48-bit ECC	—	—	•	•	•	•	6U	yes	—	—	—
—	128 kbyte	48-bit ECC	—	—					6U	yes	—	—	—
none	128 byte	32-bit/ 40-bit ECC	prog.	4 5¼ in. or 4 3½ in.					3U	yes	0/7	yes	—
4k×24 ROM, 1k RAM	—	CRC, 32-bit ECC	single burst	2 SA400, 450; SA800, 850			•		6U	yes	0/7	yes	$1,160
256k EPROM, 2k NOVRAM	128 kbyte SRAM	—	—	SCSI	•	•	•	•	6U	yes	0/7	yes	—
—	—	—	—	SCSI					6U	yes	0/7	yes	—

Model	Bus transfers (bits)	Address decoding (bits)	CPU	CPU clock speed (MHz)	DMA channels (no. and width)	Max bus transfer rate (Mbytes/s)	Operating system drivers	Real-time executive	No. of Winchester disk drives	Disk type/speed	Interleave factor	Zero latency read/wri
Mizar 1419 Dunn Dr, Carrollton, TX 75006 (800) 635-0200												**Circle 393**
MZ 7400	16	24	68000	10	4 16-bit	—	VxWorks, VRTX, OS-9	yes	4	ST506, 5 Mbits/s	1:1	yes
Motorola, Microcomputer Div. 2900 S Diablo Way, DW283, Tempe, AZ 85282 (602) 438-3518												**Circle 397**
MVME 320B1	8, 16	24	8X305	—	1 16-bit	—	system V/68 VersaDOS	no	2	ST506, 5 Mbits/s	2:1	no
MVME 321	8, 16, 32	24, 32	68010	10	1 32-bit	8	system V/68 VersaDOS	no	2	ST506, 5 Mbits/s	1:1	yes
Nissho Electronics 17320 Red Hill Ave, Suite 200, Irvine, CA 92714 (714) 261-8811												**Circle 402**
N2306	16	—	68010	10	0	10	none	no	7	ESDI, 17 Mbits/s	1:1	no
Pep Modular Computers 600 N Bell Ave, Pittsburgh, PA 15106 (412) 279-6661 Am klosterwald 4, D-8950 kaufloeuren, Germany 08341/81001												**Circle 408**
VMSC	16	24	Z80	4	—	—	OS-9, PDOS	yes	2	ST506, 5 Mbits/s	prog.	no
Philips Electronic Instruments 85 McKee Dr, Mahwah, NJ 07430 (230) 592-3800 **Philips Industrial Automation** PO Box 218, 5600 MD Eindhoven, the Netherlands +31 40 785509												**Circle 410**
PG 3101	8, 16	16, 24	8X305	8	1 16-bit	1.5	Unix 5.2, ERM, DRM	—	2	ST506, 5 Mbits/s	prog.	—
Radstone Technology One Blue Hill Plaza, Pearl River, NY 10965 (914) 735-4661												**Circle 414**
WFC-1	8, 16	16, 24, 32	—	—	0	—	VersaDOS	no	3	ST506	prog.	no
Scientific Micro Systems 339 N Bernardo Ave, Mountain View, CA 94043 (415) 962-5458												**Circle 416**
SMS6009	16	24	68k	—	—	—	OS-9, Unix V	no	2	ST506/ESDI	1:1	no
Stollmann GmbH Max Brauer-Allee 79-81, D2000 Hamburg 50, W Germany 40-389-003-0												**Circle 426**
SDC 31	16 (m), 8 (s)	24	micro-controller	16	1 16-bit	2.5	Unix, VersaDOS, PDOS, OS-9	no	2	SMD, 40 Mbits/s	0	yes
SDC 32	16 (m), 8 (s)	24	micro-controller	16	1 16-bit	2.5	same as above	no	2	SMD, 40 Mbits/s	0	yes
SDC 33	16 (m), 8 (s)	24	micro-controller	16	1 16-bit	2.5	same as above	no	2	SMD, 40 Mbits/s	0	yes
SDC 34	16 (m), 8 (s)	24	micro-controller	16	1 16-bit	2.5	same as above	no	2	SMD, 40 Mbits/s	0	yes
SB-SDC 4032	8, 16, 32	24, 32	68020	16 (20)	1 (local), 1 (VME)	16	Unix V	no	2	SMD-E, 24 Mbits/s	0	yes
EXT-SDC 40	8, 16, 32	24, 32	68020	16 (20)	1 (local), 1 (VME)	16	Unix V	no	2	SMD-E, 24 Mbits/s	0	yes
Storage Concepts 1622 Deere Ave, Irvine, CA 92714 (714) 852-8511												**Circle 427**
VME plus-31	16, 32	32	2901 8031	12.9	2	40	Unix	yes	4	par. E-SMD, 12 Mbits/s	1:1	no

Memory type and amount (bytes)	Buffer/cache details	Error detection details	Error correction details	Floppy interface	Overlapped seeks	Lookahead seeks	Command optimization	Scatter/gather commands	Form factor	Bus master/slave	Intrpt handler/gen levels	Block transfers	OEM price
32k RAM, 32k ROM	ping-pong buffer	implied seeks	transparent	WD1772	•	•	•	•	6U	yes	7/7	yes	$1,279
1k RAM, 128k ROM	—	32-bit ECC	11-bit burst	2 SA400/800			•		6U	yes	0/—	no	$995
32k RAM, 128k ROM	—	32-bit ECC	11-bit burst	4 SA400		•	•		6U	yes	0/—	no	$1,695
128k EPROM, 10k SRAM	64 kbyte	32-bit ECC	single burst	none	•	•	•		6U	yes	0/7	yes	$1,950
16k DRAM, 16k ROM	128 byte FIFO	32-bit ECC	no	4 SA850					3U	no	0/7	no	—
—	0.5 kbyte	32-bit ECC, 16-bit CRC	to 11 bits burst	SA450, SA850					6U	yes	0/1	no	$1,600
2k SRAM	2 kbyte	32-bit ECC	single burst	SA450					6U	no	0/7	no	—
—	32 kbyte	64-bit ECC	—	2 SA465	•		•		—	no	—	yes	$1,150
64 FIFO PROM	64 byte FIFO	32-bit ECC	11-bit burst	no					6U	yes	0/6	no	—
64 FIFO PROM	64 byte FIFO	32-bit ECC	11-bit burst	no					6U	yes	0/6	no	—
64 FIFO PROM	64 byte FIFO	32-bit ECC	11-bit burst	no					6U	yes	0/6	no	—
64 FIFO PROM	64 byte FIFO	32-bit ECC	11-bit burst	no					6U	yes	0/6	no	—
512k RAM, 64M EPROM	Stollmann intelligent reading algorithm	48-bit ECC	15-bit burst	no	•	•	•	•	6U	yes	0/7	no	—
512k RAM, 64M EPROM	same as above	48-bit ECC	15-bit burst	no	•	•		•	6U	yes	0/7	no	—
8k RAM, 32k EPROM	512 kbyte	32-bit ECC	auto. ECC	—	•	•	•	•	6U	yes	7/7	yes	—

DESIGNERS' BUYING GUIDE/Winchester Controllers (VMEbus)

Model	Bus transfers (bits)	Address decoding (bits)	CPU	CPU clock speed (MHz)	DMA channels (no. and width)	Max bus transfer rate (Mbytes/s)	Operating system drivers	Real-time executive	No. of Winchester disk drives	Disk type/speed	Interleave factor	Zero latency read/write
Storage Concepts 1622 Deere Ave, Irvine, CA 92714 (714) 852-8511											**Circle 427**	
VME plus-51	8, 32	32	8186 (10)	10	—	40	Unix	yes	63	ESDI, up to 3 Mbits/s	1:1	no
Xycom 750 N Maple Rd, Saline, MI 48176 (800) 367-7300											**Circle 449**	
XVME-404	8, 16	24	Am9590	10	1 16-bit	—	OS-9, PDOS	yes	2	ESDI, ST506, 5 Mbits/s	prog.	yes
Xylogics 53 Third Ave, Burlington, MA 01803 (617) 272-8140											**Circle 450**	
753	16, 32	20	80C31	16	32-bit	18	Unix	yes	4	SMD	1:1	yes
754	16, 32	20	80C31	16	32-bit	18	Unix	yes	4	SMD	1:1	yes
714	16, 32	20	80C31	16	32-bit	18	Unix	yes	4	SMD	1:1	yes

Winchester Controllers

Model	Bus	Bus transfers (bits)	Address decoding (bits)	CPU	CPU clock speed	DMA channels (no. and width)	Max bus transfer rate (Mbytes/s)	Memory type and amount (bytes)	Buffer/cache details (bytes)
Aviv 26 Cummings Pk, Woburn, MA 01801 (617) 933-1165									**Circle 318**
DFC 817	Unibus	—	—	—	—	—	3	—	—
DFC 507	Multibus	—	16, 20, 24	—	—	—	2.4	—	8k FIFO buffer
DFC 904	Q-Bus	—	—	—	—	—	3	—	1M
DFC 804	Unibus	—	—	—	—	—	3	—	—
DFC 917	Q-Bus	—	—	—	—	—	3	—	1M
Ciprico 2955 Xenium Ln, Plymouth, MN 55441 (612) 559-2034									**Circle 326**
Rim Fire 1200	Multibus I	8, 16	24	80186	10	2 16-bit	2	32k EPROM	64k cache
Rim Fire 1400	Multibus I	8, 16	24	80186	8	2 16-bit	3.2	64k EPROM	128k cache
Rim Fire 2200	Multibus II	8, 16, 24,32	12	80186	10	2 16-bit	32	64k SRAM, 64k EPROM	512k cache
Computer Dynamics 107 S Main St, Greer, SC 29651 (803) 877-8700									**Circle 330**
WIN-35	STD	8	16	Z80, 8088/86	10	external	5	2k	2k sector buffer
WIN-8	STD	8	16	Z80, 8088/86	10	0	4.3	2k	2k sector buffer

Memory type and amount (bytes)	Buffer/cache details	Error detection details	Error correction details	Floppy interface	Overlapped seeks	Lookahead seeks	Command optimization	Scatter/gather commands	Form factor	Bus master/slave	Intrpt handler/gen levels	Block transfers	OEM price
—	2 Mbyte	48-bit ECC	11-bit burst	—	•	•	•	•	6U	yes	7/7	yes	—
64 kbyte SRAM	64k SRAM	32-bit ECC	double burst	SA450					3/ 6U	yes	0/7	no	$1,050
256k PROM, 16k SRAM	512 kbyte FIFO	48-bit ECC	auto. read retries	no	•	•	•	•	6U	yes	0/7	no	$2,230
256k PROM, 16k SRAM	512 kbyte FIFO	48-bit ECC	auto. read retries	no	•	•	•	•	6U	yes	0/7	no	$2,230
256k PROM, 16k SRAM	512 kbyte FIFO	48-bit ECC	auto. read retries	no	•	•	•	•	6U	yes	0/7	no	$2,095

No. of Winchester disk drives	Disk type/speed	Interleave factor	Zero latency read/writes	Error detection details	Error correction details	Overlapped seeks	Lookahead seeks	Command optimization	Scatter/gather commands	Operating system drivers	Real-time executive	Board size	OEM price
4	SMD	1:1	—	48-bit ECC	—	•	•	•		MSCP emulation	—	quad	—
4	SMD	1:1	—	32-bit ECC	—	•	•			Unix, RMX-86	—	6U	—
4	ESDI	1:1	—	48-bit ECC	—	•	•	•		MSCP emulation	—	quad	—
4	ESDI	1:1	—	48-bit ECC	—	•	•	•		MSCP emulation	—	quad	—
4	SMD	1:1	—	48-bit ECC	—	•	•	•		MSCP emulation	—	quad	—
4	SMD-E, 24 MHz	1:1	yes	48-bit ECC	14-bit single burst	•	•		•	iRMX 86/286, Sun OS, Unix V	yes	—	$1,605
2	ESDI, 16 MHz	1:1	yes	48-bit ECC	15-bit single burst	•	•	•	•	iRMX 86/286, Sun OS, Unix V, Xenix	yes	—	$1,295
4	SMD-E, 24 MHz	1:1	yes	48-bit ECC	15-bit single burst	•	•	•		iRMX 286, Unix V	yes	—	$2,475
4	ST506/ST412, 5 Mbits/s	1:3	no	CRC w/auto retry	—	•				CP/M, MS-DOS	—	STD	—
4	Shugart SA-1000 8 in.	1:3	no	CRC w/auto retry	—	•				CP/M, MS-DOS	—	STD	—

Model	Bus	Bus transfers (bits)	Address decoding (bits)	CPU	CPU clock speed	DMA channels (no. and width)	Max bus transfer rate (Mbytes/s)	Memory type and amount (bytes)	Buffer/cache details (bytes)
Cromemco 280 N Bernardo Ave, PO Box 7400, Mountain View, CA 94039 (415) 964-7400									**Circle 335**
ESDC	Multibus	8	24	Z80	4	8-bit	1	256k RAM	196k LRV cache
Dilog 1555 S Sinclair St, Anaheim, CA 92806 (714) 937-5700									**Circle 346**
MQ606	Q-Bus	7.5M	16, 18, 22	—	—	16-bit	1.0	8k RAM	FIFO buffer
MQ696	Q-Bus	20M	—	—	—	16-bit	2.5	16k RAM	FIFO buffer
DQ686	Q-Bus	15M	16, 18, 22	—	—	16-bit	1.75	16k RAM	FIFO buffer
DQ246	Q-Bus	30M	16, 18, 22	—	—	16-bit	3.75	32k RAM	FIFO buffer
DQ256	Q-Bus	30M	16, 18, 22	—	—	16-bit	3.75	32k RAM	FIFO buffer
Emulex 3545 Harbor Blvd, Costa Mesa, CA 92626 (714) 662-5600									**Circle 350**
QD21	Q-Bus	adapt.	16, 18, 22	LSI-11, μPDP-11, μVAX II	—	2 MB/s	—	26k	—
QD24	Q-Bus	adapt.	22	μVAX 3500, μVAX 3600	—	2 MB/s	—	57k	—
QD33	Q-Bus	adapt.	22	LSI-11, μPDP-11, μVAX II	—	3 MB/s	—	26k	—
QD34	Q-Bus	adapt.	16, 18, 22	μVAX 3500, μVAX 3600	—	3 MB/s	—	32k	—
UD23	Unibus	adapt.	16, 18	PDP-11, VAX Unibus	—	—	2	—	32k
UD33	Unibus	adapt.	16, 18	PDP-11, VAX Unibus	—	—	3	—	25k
Gespac 50 W Hoover Ave, Suite 2, Mesa, AZ 85202 (602) 962-5559									**Circle 359**
GESHDC-1A	G-64/ G-96	8	24	WD	20	yes	1.2	1	8k
Intel 3065 Bowers Ave, PO Box 58065, Santa Clara, CA 95052 (800) 548-4725									**Circle 367**
iSBC 214	Multibus	8, 16	24	80186	5	4 8-bit, 2 16-bit	2.5	32k ROM	32k data buffer
iSBC 221	Multibus	16	24	80186	10	2 8-bit, 3 16-bit	5	64k ROM	128k data buffer
iSBC 186 224A	Multibus II	32	32	80186	5	4 8-bit, 2 16-bit	32	64k ROM	128k data buffer
Interphase 2925 Merrell Rd, Dallas, TX 75229 (214) 350-9000									**Circle 368**
Storager II	Multibus	—	—	68000	10	—	—	—	16k
SMD 2190	Multibus	8, 16	8, 16	8085	12	24-bit	4	—	16k

No. of Winchester disk drives	Disk type/speed	Interleave factor	Zero latency read/writes	Error detection details	Error correction details	Overlapped seeks	Lookahead seeks	Command optimization	Scatter/gather commands	Operating system drivers	Real-time executive	Board size	OEM price
2	ESDI, 10 Mbits/s	1:1	yes	ECC poly 32-bit	11-bit single burst	•		•		Unix 4.3, Cromix	—	IEEE-696	—
2	ST506, 5 Mbits/s	1:1	no	32-bit	32-bit	•				no	no	dual	—
2	ESDI, 20 Mbits/s	1:1	no	32-bit	—	•	•	•		no	no	dual	—
4	ESDI, 15 Mbits/s	1:1	no	32-bit	32-bit	•	•	•		no	no	quad	—
4	SMD, 20 Mbits/s	1:1	no	32-bit	32-bit	•	•	•		no	no	quad	—
4	SMD, 24 Mbits/s	1:1	no	32-bit	32-bit	•	•	•		no	no	quad	—
2	ESDI, 10 Mbits/s	1:1	no	48-bit ECC, 16-bit CRC	11-bit single burst	•	•	•		Micro VMS V4.1, Ultrix-32m, V1.2	no	quad	$1,017
4	ESDI, 24 Mbits/s	1:1	no	48-bit ECC, 16-bit CRC	11-bit single burst	•	•	•		Micro VMS V4.1, Ultrix-32m, V1.2	no	quad	$1,187
2	SMD, SMD-E, 24 Mbits/s	1:1	no	48-bit ECC, 16-bit CRC	—	•	•	•		Micro VMS V4.1, Ultrix-32m, V1.2	no	dual	$1,496
4	SMD-E, 24 Mbits/s	1:1	no	48-bit ECC, 16-bit CRC	—	•	•	•		Micro VMS V4.1, Ultrix-32m, V1.2	no	quad	$1,666
4	ESDI, 15 Mbits/s	1:1	no	48-bit ECC, 16-bit CRC	11-bit single burst	•	•	•		VMS, RSTS/E, RX11-M, RT11 RX11M+	no	quad	$1,700
4	ESDI, 24 Mbits/s	1:1	no	48-bit ECC, 16-bit CRC	11-bit single burst	•	•	•		VMS, RSTS/E, RX11-M, RT11 RX11M+	no	hex	$2,380
2	ST506, 5 Mbits/s	1:1	yes	CRC	CRC					OS-9	OS-9, PDOS	3U	$293
2	ST506, 5 Mbits/s	1:1	yes	CRC	ECC (Winchester)	•				iRMX1, iRMX11, Unix	—	Multibus I	$1,090
2	ESDI, 10 Mbits/s ST506, 5 Mbits/s	1:1	yes	CRC	ECC (Winchester)	•				iRMX1, iRMX11, Unix	—	Multibus I	$1,421
4	ST506, 5 Mbits/s	1:1	yes	CRC	ECC (Winchester)	•			•	iRMX1, iRMX11, Unix	—	6U	$1,871
2	ESDI, ST506, ST412HP	1:1	yes	CRC	32-bit	•		•		Unix V, Unix III, RMX86	—	—	—
4	SMD, SMD-E, 24 Mbits/s	1:1	no	—	32-bit	•		•		Unix V, Unix 4.2 BSD, RMX86	—	—	—

Model	Bus	Bus transfers (bits)	Address decoding (bits)	CPU	CPU clock speed	DMA channels (no. and width)	Max bus transfer rate (Mbytes/s)	Memory type and amount (bytes)	Buffer/cache details (bytes)
Interphase 2925 Merrell Rd, Dallas, TX 75229 (214) 350-9000									**Circle 368**
SMD 2490	Multibus	8, 16	8, 16	8085	12	24-bit	4	–	64k
Matrix 1203 New Hope Rd, Raleigh, NC 27610 (919) 833-2000									**Circle 376**
FDC2	STD	8	16	6809	8	1 8-bit	64k	–	–
Megadata 35 Orville Dr, Bohemia, NY 11716 (516) 589-6800									**Circle 378**
M80780	Multibus	16	24	–	–	1 16-bit	10	–	–
Micro Technology 1620 Miraloma Ave, Placentia, CA 92670 (714) 632-7580									**Circle 383**
MDQ19	Q-Bus	16	22	80186	10	1 16-bit	3	128k EPROM	128k
MQDX4	Q-Bus	16	22	80186	10	1 16-bit	3	128k EPROM	128k
MQD13	Q-Bus	16	22	80186	10	1 16-bit	3	128k EPROM	128k
MQDX3	Q-Bus	16	22	80186	10	1 16-bit	3	128k EPROM	128k
Micro/Sys 1011 Grand Central Ave, Glendale, CA 91201 (818) 244-4600									**Circle 385**
SB8740	STD	8	8	–	–	1	1	–	–
Moya 9001 Oso Ave, Unit C, Chatsworth, CA 91311 (818) 700-1200									**Circle 398**
135	STD	8	19	STD	9.216	2 8-bit	2.3	50 non-volatile	–
Qualogy 2241 Lundy Ave, San Jose, CA 95131 (408) 434-5200									**Circle 412**
QE2	Q-Bus	–	–	VAX II, PDP-11	–	–	–	–	1M cache
MC-5217	Multibus	8, 16	20, 24	68000	10	–	–	–	–
MC-5217	Multibus	8, 16	20, 24	68000	10	–	–	–	–
MC-5317	Multibus	8, 16	20, 24	68000	10	–	10	–	–

No. of Winchester disk drives	Disk type/speed	Interleave factor	Zero latency read/writes	Error detection details	Error correction details	Overlapped seeks	Lookahead seeks	Command optimization	Scatter/gather commands	Operating system drivers	Real-time executive	Board size	OEM price
4	24	1:1	no	—	32-bit	•	•	•		Unix V, Unix 4.2 BSR, RMX86	—	—	—
—	—	—	—	—	—					OS-9 and flex	no	STD bus	$297
2, 4 (opt.)	ST506, 5 Mbits/s, ESDI 10/15 Mbits/s	1:1	no	CRC, CCITT	16-bit double burst					—	—	—	—
4	ESDI, 15 MHz	1:1	no	CRC	Reed-Solomon single, double burst	•	•	•	•	VMS, Unix, RT11, RSX11, RSX11MT, RSTS/E	—	dual	—
4	ESDI/ST506, 15 MHz	1:1	no	CRC	same as above	•	•	•	•	VMC, Unix, RT11, RSX11M/MT RSTXE	—	dual	—
4	ESDI, 15 MHz	1:1	no	CRC	same as above	•	•	•	•	VMS, Unix, RT11, RSX11M/MT, RSTS/E	—	dual	—
4	ESDI, 15 MHz	1:1	no	CRC	same as above	•	•	•	•	VMS, Unix, RT11, RSX11M/MT, RSTS/E	—	dual	—
1	5¼, 8 & 14 in.	—	—	—	—					—	no	(4.5 × 6.9)	$140
7	SCSI, 1.5 Mbits/s	1:1	no	ECC	drive dependent	•				CP/M, MAX-DOS	yes	STD	$220
4	ESDI, 10 Mbits/s	1:1	yes	Reed-Solomon	48-bit ECC polynominal	•	•	•		—	—	quad	—
2	ST506/SA 1000, 5 Mbits/s	1:1	—	CRC	32-bit ECC	•	•	•		—	—	1 slot iSBC 604/614	—
2	ST506/412, 5 Mbits/s	1:1	—	CRC	32-bit ECC	•		•		—	—	1 slot iSBC 604/614	—
2	ESDI, 10 Mbits/s	1:1	—	CRC	32-bit ECC	•	•	•		—	—	1 slot iSBC 604/614	—

Model	Bus	Bus transfers (bits)	Address decoding (bits)	CPU	CPU clock speed	DMA channels (no. and width)	Max bus transfer rate (Mbytes/s)	Memory type and amount (bytes)	Buffer/cache details (bytes)
Scientific Micro Systems 339 N Bernardo Ave, Mountain View, CA 94043 (415) 962-5458 **Circle 416**									
SMS8009	Multibus	16	24	286, 386	8	–	–	–	track cache
SMS 0108	Q-Bus	16	24	11/23, 11/73	–	–	–	–	track cache
SMS 0109	Q-Bus	16	–	11/23, 11/73	–	–	–	–	track cache
Sigma Information Systems 3407 E LaPalma Ave, Anaheim, CA 92806 (714) 630-6553 **Circle 419**									
SDC-RQD-11-SC	Q-Bus	16	22	μVAX, μPDP	20	–	1.8	512k EPROM	1M cache
SDC-RQD-11-EC	Q-Bus	16	22	μVAX, μPDP	20	–	1.8	512k EPROM	1M cache
SDC-RQD-11-C	Q-Bus	16	22	μVAX, μPDP	20	–	1.8	256k EPROM	full track buffer
SDC-RQD-11-SCSI	Q-Bus	16	22	μVAX, μPDP	20	–	1.8	–	48k buffer
Storage Concepts 1622 Deere Ave, Irvine, CA 92714 (714) 852-8511 **Circle 427**									
Concept 31-QB	Q-Bus	16	22	2901, 8031	12.0	1 16-bit	12.3	16k	512k
Systek 1027 N Kellogg St, Kennewick, WA 99336 (509) 735-1200 **Circle 433**									
6320	STD	8	24	–	–	1	4	32k RAM	32k RAM
Xylogics 53 Third Ave, Burlington, MA 01803 (617) 272-8140 **Circle 450**									
451	Multibus	16	24	8031	12	16-bit	3	128 PROM	8k FIFO
431	Multibus	16	24	8031	12	16-bit	3	128 PROM	8k FIFO
432	Multibus	16	24	8031	12	16-bit	3	128 PROM	8k FIFO

No. of Winchester disk drives	Disk type/speed	Interleave factor	Zero latency read/writes	Error detection details	Error correction details	Overlapped seeks	Lookahead seeks	Command optimization	Scatter/gather commands	Operating system drivers	Real-time executive	Board size	OEM price
2	ST506/ESDI	1:1	no	64-bit ECC	—	•		•		RMX 286	—	—	$850
2	ST506/ESDI	1:1	no	ECC	—	•		•		RT-11, RSX	—	quad	$900
1	optical	1:1	no	ECC	—	•		•		VMS	—	quad	$1,150
2	SMD-E, 25 Mbits/s	1:1	no	ECC	48-bit ECC with 11-bit span	•	•	•	•	not required	VMS, RSX11M, RSTSE, RT11, TSX, Unix, DSM	quad	$1,007
4	ESDI, 25 Mbits/s	1:1	no	ECC	same as above	•	•	•	•	not required	same as above	quad	$1,038
2	ST506, 10 Mbits/s	1:2, 1:3	no	ECC	Western Digital ECC	•	•	•	•	not required	same as above	dual	$537
7	SCSI, 10 Mbits/s	1:1	no	ECC	SCSI controlled	•	•	•	•	not required	same as above	dual	$928
4	parallel, SMD-E	1:1	no	ECC, CRC	32-bit double burst	•	•	•		MicroVMS	VMS	quad	—
4	SCSI, 8 Mbits/s	1:1	—	32-bit ECC	32-bit ESDI	•	•	•		MS-DOS	—	STD	$675
4	SMD, 2.4 Mbytes/s	1:1	no	CRC	32-bit ECC	•	•			Xenix, RMX-286	no	Multi-bus I	$1,930
2	ST506	1:1	no	CRC	48-bit ECC	•				Xenix, RMX-286	no	Multi-bus I	$1,595
4	ESDI	1:1	no	CRC	48-bit ECC	•				Xenix, RMX-286	no	Multi-bus !	$1,595

How To Size Up

A complete range of color monitor technologies and sizes for every application.

There's a lot to consider when sizing up a supplier of color graphic display monitors. Critical questions arise, such as manufacturing experience, technology innovation, proven reliability, product selection, and customer support.

That's why you should consider Mitsubishi.®

For years, Mitsubishi Electronics has led the industry in supplying color graphics monitors. Mitsubishi offers the widest range of monitor features, sizes and advanced technologies on the market today. Quality monitors to support your exact requirements—whether large screen, small screen, fixed-frequency or multiple-frequency performance.

A comprehensive line which includes 14″, 15″, 16″, 20″, 26″, 33″, and 37″ models, available in a variety of performance ranges. Whatever your application—CAD/CAM, image processing, presentation graphics, or desktop publishing—Mitsubishi has the right monitor, at the right cost.

Technology leadership.

When you size up technological advancements, Mitsubishi clearly leads the way. The leader in auto-tracking technology with more models and sizes, covering the broadest range of horizontal scan frequencies, than anyone else. The leader in dynamic beam focus (DBF) technology for sharper, clearer images to the edge of the screen. And the leader in microprocessor-enhanced, digital scan mode memory technology for optimum display size and clarity in *any* mode, text or graphic, or when switching between multiple modes.

OEM experience and commitment.

And when you size up Mitsubishi's continuing commitment to serving the OEM market, you'll find a company with the industry's broadest range of experience, service, applications assistance and resources to support you with high-quality monitors in volume.

To size up monitor technology, one name is all you have to know: Mitsubishi. Call or write Mitsubishi Electronics America, Inc., Computer Peripherals Division, 991 Knox Street, Torrance, CA 90502, (213) 217-5732.

The leader in auto-tracking technology.

Mitsubishi's auto-tracking monitors automatically track horizontal and vertical frequencies, eliminating manual frequency adjustments. From 14″ to 37″ display sizes, Mitsubishi offers you a total solution in auto-tracking convenience and versatility.

The leader in large screen technology.

Mitsubishi offers the two largest auto-tracking monitors in the industry today. Bright, vivid colors on our big 33″ or 37″ monitors result in greater impact and add a new dimension to the growing presentation graphics market.

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Monitor Technology.

Actual unretouched screen images.

Screen Size	Mitsubishi Model	Horizontal Scan Frequency (kHz)	Screen Size	Mitsubishi Model	Horizontal Scan Frequency (kHz)
14″	XC1409C	15.7	20″	C3920/21/22	15-24
14″	XC1410C/30C	22 or 15.75	20″	C6920/21/22	28–35
14″	XC1429C	31.5	20″	HA3905*	15.7 ~ 36
14″	AUM1381A*	15.7 ~ 36	20″	HL6905*†	30 ~ 64
14″	FA3415/25*	15.7 ~ 36	20″	HG6905□	40–67
14″	HF1400/50	15.5–20	20″	HJ6905*□	40 ~ 70
14″	HF2400/50	20–25	26″	C3510	15–18
14″	HF3400/50	30–35	26″	C6512	28–34
15″	FHF3500 (flat square)	30–35	33″	XC3310*	15 ~ 35
16″	C8652	47–52	37″	XC3710*	15 ~ 35
16″	FG6600	60–65			
16″	HL/FL6605*†	30 ~ 64			

*Auto-tracking †Microprocessor-enhanced programmable display settings □Available with DBF

Sales Offices:
Carrollton, TX (214) 241-5300
Minnetonka, MN (612) 938-7779
Mt. Prospect, IL (312) 298-9223
Norcross, GA (404) 368-4845
Piscataway, NJ (201) 981-1001
Sunnyvale, CA (408) 730-5900
Torrance, CA (213) 217-5732
Woburn, MA (617) 938-1220

The leader in microprocessor-enhanced technology.

Mitsubishi was the first on the market with auto-tracking microprocessor-enhanced monitors. Digital scan mode memory features a microprocessor in the monitor which can remember up to 20 combinations of settings for horizontal width, phase, centering and pincushion correction, as well as vertical height and centering.

The leader in dynamic beam focusing (DBF).

With advanced DBF technology, Mitsubishi offers OEMs distortion-free, high-resolution displays. DBF technology changes the beam shape from elliptical to circular as it strikes the corners and edges of the CRT, resulting in the highest picture quality possible over the entire screen.

Performance Peripherals.

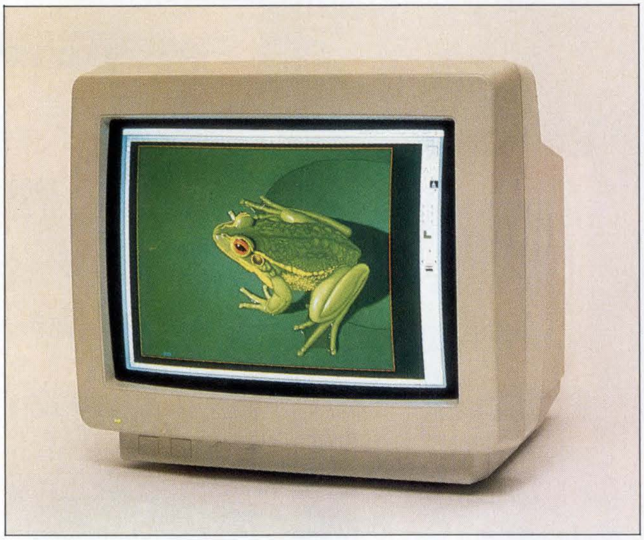
MITSUBISHI ELECTRONICS

CIRCLE NO. 23

DESIGN AND DEVELOPMENT TOOLS

High-resolution monitors fulfill demands of CAD/CAM and desktop publishing

John H. Mayer, Senior Associate Editor



One of the latest members of Mitsubishi's Diamond Scan family, the 20 L is the first 20-in. (19-in. viewable) monitor capable of autotracking from 30 to 64 kHz. A microprocessor-based digital scan memory mode automatically fine tunes up to 20 discrete combinations of horizontal and vertical display settings.

The rapidly declining costs and exponential performance improvements of desktop computer systems coupled with the growing availability of personal-computer-based CAD and desktop-publishing applications software have ignited a rising demand for higher performance, higher resolution graphics technology. Low-cost but fairly sophisticated PC CAD packages such as AutoCAD and VersaCAD, and popular desktop-publishing packages such as Ventura and Pagemaker, are bringing those functions in-house for a rising number of firms. With highly respected market researchers such as Dataquest (San Jose, CA) predicting that the market for high-resolution graphics systems will grow ten-fold over the next five years, monitor manufacturers are rushing to develop products with higher resolutions and larger display sizes.

As the accompanying table demonstrates, at least 22 companies already offer ultrahigh-resolution monitors capable of resolutions of 1,024× 1,024 pixels or better. Improved electron gun design inside the CRT, better convergence of the the electron beams as they scan the screen, higher contrast phosphors and glare-reducing faceplate materials are helping to improve the legibility of these displays with each succeeding product generation. In addition, ergonomic improvements such as tilt-and-swivel base-plates and front-panel controls designed to eliminate user discomfort are becoming virtually mandatory features.

Monitors for all frequencies

Multiscanning is finally coming of age in the ultrahigh-resolution color monitor arena. Monitors capable of automatically adjusting to ranges of horizontal and vertical synchronization frequencies have been available in the low end since NEC (Mountain View, CA) debuted its Multisync units in 1985. The ability of these monitors to adapt to the variety of PC cards available operating at various graphics standards, such as Color Graphics Adapter, Enhanced Graphics Adapter and Video Graphics Array (VGA), lets monitor vendors meet the wide range of performance requirements with a single unit.

Those same benefits haven't been available at the high-end professional graphics level, however. With little in the way of standards beyond VGA, monitor manufacturers have had to face a wide range of frequencies. Prohibitive manufacturing costs and difficulties relating to power-supply design have also hindered multiscanning monitors at higher resolutions. "As frequencies go up, it's more difficult to maintain a bright and accurate high-resolution display because scan rates are typically dependent on the high energy pulses of the monitor's power supply," says Roger Nielsen, president of Monitronix (Westerville, OH). "Without an independent high-voltage power supply, the video display inevitably suffers.

But monitor manufacturers are finally finding ways to overcome these obstacles. Within the last six months, Mitsubishi (Torrance, CA) extended the scope of its autotracking, or multiscanning, Diamond Scan family into the ultrahigh-resolution range by adding the 20 L, a 20-in. (19-in. viewable) monitor capable of supporting resolutions from 640×480 pixels (VGA) to 1,280×1,024 pixels. (A 16-in. unit was introduced in March.)

The 20 L features a microprocessor-controlled digital scan mode memory that automatically fine tunes the setting of a display's size and position, both horizontally and vertically. The microprocessor-based circuitry, supported by EEPROMs, stores up to 20 discrete combinations of settings. "We wanted a monitor that would handle all the recent controller cards and work through all the CAD/CAM controller cards," says Charles Root, marketing manager for the company's Peripherals Division. "There seem to be an infinite variation of frequencies, so it was necessary to give the user the ability to fine tune the vertical and horizontal frequencies, so that the quality of the image was comparable to an image from a fixed-frequency monitor."

Both the 16- and 20-in. units use 100-MHz video bandwidths with 30- to 64-kHz horizontal scanning frequencies and 50- to 90-Hz vertical scanning frequencies. Both have a

68030 - VME
The Real *Single* Board Computer

The TP32V from Tadpole

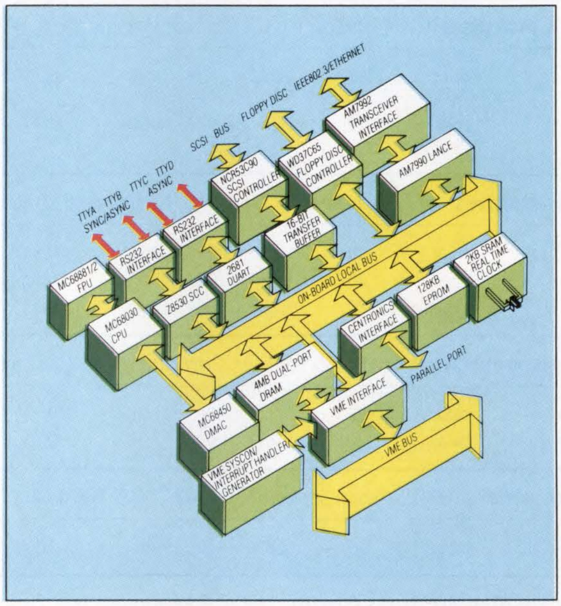
• The Philosophy •

Designed for optimum system performance from a single full IEE 1014 VME board, the TP32V needs no other cards, piggy-backs or mezzanines to deliver the full potential of the 16-33 MHz MC68030. To maximise overall throughput, all the on-board I/O facilities were designed to take advantage of hardware transfer buffers, DMA facilities and advanced DRAM arbitration techniques between competing resources.

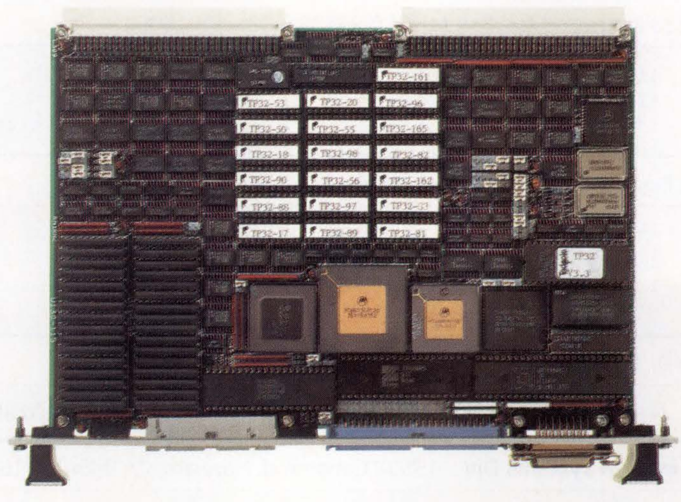
• The Specification •

- MC68030 16-33MHz
- MC68450 4-channel DMA controller
- 4Mb multi-ported nibble-mode DRAM
- AMD Lance IEEE 802.3 Ethernet with DMA
- Z8530 SCC giving two DMA-driven RS232 sync/asynchronous ports and two further RS232 asynchrous ports
- NCR 53C90 DMA-driven synchronous or asynchronous SCSI interface • Floppy disk controller
- Full VME Rev C.1 IEEE 1014 interface
- 64-512Kb EPROM • Battery-backed RTC/SRAM
- Full debug monitor • Optional MC68881/2 FPU
- TP-IX/68K version of UNIX V.3.1* • NFS, RFS, TCP/IP

• The Design •



• The Evidence •



Tadpole Technology

the driving force in 32-bit design

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T A D P O L E

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*VRTX is a trademark of Ready Systems *TP-IX V.3.1 is derived from UNIX V.3.1*

CIRCLE NO. 24

■ ULTRAHIGH-RESOLUTION MONITORS

Model	Monochrome or color	Size (in.)	Resolution (pixels)	Input signals	Dot pitch (mm)	Vertical scan rates (Hz)	Horizontal scan rates (kHz)	Bandwidth (MHz)	Price (OEM quantity)	Comments
Aydin, Controls Div 414 Commerce Dr, Fort Washington, PA 19034 (800) 366-8889										**Circle 100**
8815	color	13	1,024 × 1,024	RGB	0.31	40 to 70	25 to 38	40	$1,425 to $2,195	interlaced; metal cabinet or open chassis
8964/65	color	19	1,280 × 1,024	RGB	0.31	40 to 70	62 to 66	100	$1,675 to $3,350	noninterlaced
Barco Industries 472 Amherst St, Suite 16, Nashua, NH 03063 (603) 880-1430										**Circle 101**
calibrator	color	20	1,200 × 1,024	RGB	0.31	45 to 120	45 to 66	120	—	μP controlled
CDCT 6451	color	20	1,024 × 1,024	RGB	0.31	45 to 80	26 to 38	45	—	extremely color stable
CDCT 6551	color	20	1,280 × 1,024	RGB	0.31	45 to 120	45 to 75	120	—	same as above
Chugai Boyeki (America) 55 Mall Dr, Commack, NY 11725 (516) 864-9700										**Circle 102**
CPD-2030	color	20	1,024 × 768	RGB	0.31	60	48	80	—	nonglare CRT coating
CPD-2040	color	20	1,280 × 1,024	RGB	0.31	60	64	120	—	noninterlaced
Conographic 16802 Aston St, Irvine, CA 92714 (714) 474-1188										**Circle 103**
Conovision 2800	mono	19	2,880 × 720	all	103	78	29	100	—	eight shades of gray
Conrac Display Products Group 1724 S Mountain Ave, Duarte, CA 91010 (818) 303-0095										**Circle 104**
7351	color	19	1,280 × 1,024	RGB	0.31	47 to 63	62.5 to 67.5	110	$1,897	noninterlaced; cabinet, rack slide or chassis
7400	color	19	1,280 × 1,024	RGB	0.31	47 to 63	62.5 to 67.5	110	$2,500	same as above
Cornerstone Technology 1883 Ringwood Ave, San Jose, CA 95131 (408) 279-1600										**Circle 105**
Dualpage/PC	grayscale	19	1,600 × 1,280	ECL	—	67	89	200	—	two-page layout or DTP
Dualpage/Mac II	mono	19	1,600 × 1,280	ECL	—	67	89	200	—	two-page layout
Z21 IQ	grayscale	21	1,152 × 864	—	—	—	—	—	$3,495	Mac II compatible
Display Tek 1355 Holmes Rd, Elgin, IL 60123 (312) 931-2100										**Circle 106**
Lambda	mono	17/19	1,024 × 1,280	all	—	70	100	120	—	40,000-hr MTBF
Kappa	mono	19	2,000 × 2,000	ECL	—	70	to 150	200	—	same as above
Venus	color	16	1,024 × 1,024	analog RGB	0.26	60	to 64	100	—	utilizes Sony Trinitron CRT
E Machines 9305 SW Gemini Dr, Beaverton, OR 97005 (503) 646-6699										**Circle 107**
Z21 II	mono	21	1,152 × 864	—	—	—	—	—	$2,495	Mac II compatible
Hitachi America, Office Automation Systems Div 19530 Cabot Blvd, Hayward, CA 94545 (415) 785-9770										**Circle 108**
HM-4115	color	15	1,280 × 1,024	RGB	0.28	55 to 65	61 to 65	100	$990	noninterlaced
HM-4117	color	17	1,280 × 1,024	RGB	0.28	55 to 65	61 to 65	100	$1,290	noninterlaced
HM-4119	color	19	1,280 × 1,024	RGB	0.31	55 to 65	61 to 65	100	$1,990	noninterlaced
HM-5219	color	19	1,600 × 1,280	RGB	0.26	60 to 75	78 to 80/ 88 to 90	150	$3,090	noninterlaced
HM-4119 (HP)	color	19	1,280 × 1,024	RGB	0.31	60 to 75	60 to 65/ 72 to 78/ 84 to 90	150	$2,250	noninterlaced
HM-4120 (HP)	color	21	1,280 × 1,024	RGB	0.31	55 to 80	47 to 78	120	$2,350	noninterlaced

Key: * = retail price; ECL = emitter coupled logic; HGC = Hercules graphics card; MDA = monochrome display adapter; RGB = red-green-blue; RGB/analog = monitor that uses analog signals to carry RGB signals; VGA = Video Graphics Array

Model	Monochrome or color	Size (in.)	Resolution (pixels)	Input signals	Dot pitch (mm)	Vertical scan rates (Hz)	Horizontal scan rates (kHz)	Bandwidth (MHz)	Price (OEM quantity)	Comments
Hitachi America, Office Automation Systems Div 19530 Cabot Blvd, Hayward, CA 94545 (415) 785-9770 **Circle 108**										
HM-6219	color	19	2,048 × 2,048	RGB	0.21, 0.26	60	126	250	$38,000	noninterlaced
HM-4625	color	25	1,280 × 1,024	RGB	0.37	55 to 65	61 to 64	100	$18,800	noninterlaced
Micro Display Systems 1310 Vermillion St, PO Box 455, Hastings, MN 55033 (612) 437-2233 **Circle 109**										
1000 (Genius²)	mono	19	1,280 × 1,024	ECL	—	63	66	106.6	—	full dual page
420	mono	15	736 × 1,008	TTL	—	60	63	70	—	single page (66 lines)
Microvitec 1943 Providence Court, College Park, GA 30337 (404) 991-2246 **Circle 110**										
3019/SP	color	20	1,280 × 1,024, 1,024 × 768	RGB	0.31	30 to 100	48 to 64	50 to 100	$3,695	antiglare screen
Mitsubishi Electronics America 991 Knox St, Torrance, CA 90502 (213) 217-5732 **Circle 111**										
FL6605	color	16	1,280 × 1,024	analog	0.26	50 to 90	30 to 64	110	$2,145*	autotracking
HJ6905	color	20	1,280 × 1,024	RGB	0.31	50 to 80	40 to 70	110	$3,790*	autotracking, tilt-swivel base opt.
HL6905	color	20	1,280 × 1,024	analog	0.31	50 to 90	30 to 64	100	$3,650*	diamond scan, auto-tracking
Monitronix 929 Eastwind Dr, Suite 220, Westerville, OH 43081 (614) 891-3232 **Circle 112**										
MX-160	color	16	1,280 × 1,024; 1,024 × 768	RGB	0.26	60	63.4	100	$2,795*	—
MX-200	color	19	1,280 × 1,024	RGB	0.31	45 to 90	40 to 74	120	$4,695	—
MX-210	color	19	1,280 × 1,024	RGB	0.31	45 to 90	40 to 74	160	$3,695	—
MX-240	color	19	1,600 × 1,280	RGB	0.26	45 to 90	74 to 90	250	$6,995	—
Nanao USA 23510 Telo Ave, #5, Torrance, CA 90505 (213) 325-5202 **Circle 113**										
9070S	color	16	1,024 × 1,024	TTL, analog RGB	0.31	50 to 80	20 to 50	50	$1,699*	autoscan, front controls
9500	color	20	1,280 × 1,024	analog	0.31	55 to 75	31.5 to 78	120	$3,999*	autoscan, antireflection surface
NEC Home Electronics (USA) 1255 Michael Dr, Wood Dale, IL 60191 (312) 860-9500 **Circle 114**										
Mongraph System	mono	16	1,024 × 1,024	analog	—	70	76	100	$1,999*	noninterlaced, config. for PC XT, PC AT
Princeton Graphic Systems 601 Ewing St, Bldg A, Princeton, NJ 08540 (609) 683-1660 **Circle 115**										
LM-317	mono	17	1,664 × 1,200	TTL	—	60	74.6	160	$949*	paper-white phosphor; PC XT, PC AT, Mac II/SE compatible
LM-300	mono	15	1,200 × 1,664	TTL, ECL	—	60	74.3	160	$839*	first WYSIWIG monitor for PC XT, PC AT, Mac SE
LM-301	mono	15	1,200 × 1,664	TTL, ECL	—	60	74.6	160	$839*	two-page viewing
Sigma Designs 46501 Landing Pkwy, Fremont, CA 94538 (415) 770-0100 **Circle 116**										
LVS-PC-1901	mono	19	1,664 × 1,200	ECL	—	60	75	160	$2,495	HGC, MDA emulation
Colormax	color	19	1,152 × 870	RGB	0.31	70	63	100	$4,995	control panel
LVS-SE-1901	mono	19	1,664 × 1,200	TTL	—	60	75 MHz	160	$2,395	832- × 600-pixel resolution mode
LVS-M2-1901	mono	19	1,664 × 1,200	TTL	—	60	75 MHz	160	$2,495	same as above

ULTRAHIGH RESOLUTION MONITORS

Model	Monochrome or color	Size (in.)	Resolution (pixels)	Input signals	Dot pitch (mm)	Vertical scan rates (Hz)	Horizontal scan rates (kHz)	Bandwidth (MHz)	Price (OEM quantity)	Comments
Sony, Computer Peripherals Div 1 Sony Drive, Park Ridge, NJ 07656 (201) 930-7071										**Circle 117**
GDM-1601	color	16	—	—	0.26	—	64	—	$3,095	—
GDM-1602	color	16	—	RGB	0.26	—	64	—	$3,095	—
GDM-1953	color	19	1,280 × 1,024	RGB	0.31	59.9	64	100	$4,195	noninterlaced
Tektronix PO Box 14928, Portland, OR 97214 (800) 835-9433										**Circle 118**
GMA201	mono	19	2,048 × 1,536	analog, video, syncs	—	60	93	200	—	dynamic focus and astigmatism control
GMA202	mono	19	1,536 × 2,048	analog, video	—	60	126	200	—	same as above
GMA251	mono	19	2,048 × 1,536	digital, TTL	—	60	93	200	—	2,048- × 2,048-pixel frame buffer
Toshiba America 1101A Lake Cook Rd, Deerfield, IL 60015 (312) 945-1500										**Circle 174**
P20CU00	color	21	1,280 × 1,024; 1,024 × 768	RGB	0.31	47 to 73	31.5, 48, 64	100	—	autoscanning between VGA—48-64 kHz
P19CU00	color	20	1,280 × 1,024	RGB	0.31	50 to 70	64	100	—	compact, lightweight
U.S. Pixel 59 Fountain St, Framingham, MA 01701 (508) 875-6958										**Circle 122**
PX15	mono	15	1,600 × 1,200	TTL, ECL, linear	—	60 to 90	35 to 75	180	$495	antireflection faceplate
PX19	mono	19	1,600 × 1,200	TTL, ECL, linear	—	60 to 90	35 to 75	180	$595	antireflection faceplate
PX19CAB	mono	19	1,600 × 1,200	TTL, ECL, linear	—	60 to 90	35 to 75	180	$695	tilt and swivel, antireflection faceplate
Video Monitors (subsidiary of Dotronix) 3833 N White Ave, Eau Claire, WI 54703 (715) 834-7785										**Circle 121**
M2400	mono	5 to 25	1,280 × 1,024	analog, TTL, ECL	—	60 to 80	30 to 120	100	$500	custom designed
C6000	color	16 to 19	1,280 × 1,024	RGB	0.31	60 to 80	30 to 80	100	$2,000	custom designed

CRT dot pitch of 0.31 mm.

Monitronix plans to unveil its own multiscanning solution this fall. Called Easysync, the product is a low-cost upgrade kit that plugs into the backplane of existing Monitronix units and comes standard on new models. With the Easysync kit, Monitronix monitors will accommodate graphics cards with scan rates ranging from 40 to 74 kHz.

Flat and square monitors

The first flat and square monitor capable of multiscanning over ultrahigh-resolution frequencies was unveiled by Toshiba (Deerfield, IL) this summer at Siggraph. The 21-in. P20-CU00 scans a frequency range of 30 to 70 kHz, ensuring compatibility with IBM's Personal System/2, Apple's Macintosh and graphics boards for the older IBM PC line, while offering a maximum resolution of 1,280× 1,024 pixels. The CRT has a dot pitch of 0.31 mm and runs at a 100-MHz bandwidth.

Flat and square monitors offer a number of advantages. A flat surface eliminates much of the distortion caused by the curved faceplate of traditional CRT displays. It also reduces glare from overhead lighting by about 30 percent. The square CRT design supplies a larger viewing area and can improve resolution or sharpness of image in the corners by as much as 30 percent.

Fixed-frequency units, which are still the most popular form of monitors, often offer significant price advantages over multiscanning versions. The 19-in. GDM-1953 from Sony (Park Ridge, NJ) uses that company's Trinitron picture tube with a fine-pitch aperture grille to deliver a high-contrast image. The practically flat, square-cornered image display area offers a 1,280-× 1,024-pixel resolution over a display area of 13½ × 10 in. Toshiba recently added a fixed-frequency, 64-kHz, 19-in., 1,280-× 1,024-pixel monitor, the P19CU00, to its product line.

Demand for higher resolution

The rapid development of desktop-publishing software over the past few years has driven the demand for higher resolution monochrome and grayscale monitors. As vendors increased the precision of desktop-publishing packages and added capabilities to manipulate more complex images, monitor vendors responded with higher resolution products. Monochrome, or paper-white, units range in resolution up to 1,600×1,280 pixels. A full slate of vendors offer products in the 1,280-×1,024-pixel class.

Higher signal bandwidths and video scan rates have been the focus of most technological improvements. Cornerstone Technology (San Jose, CA) brings a 1,600-×1,280-pixel resolution to its new 19-in. Vista 1600 by using a 67-Hz refresh rate that requires a 89-kHz horizontal rate and a 200-MHz video data rate.

Unlike the color CAD/CAM arena where multiscanning is on the rise, higher resolution monochrome monitors typically come in a system package with the monitor supported by a specialized controller, cables and drivers. Many of the boards come with 16-bit bus connectors that demand an AT-style slot. Some, such as Cornerstone Technology's product line, operate in either an 8-bit or a 16-bit slot.

Improved page-display functions

The desktop-publishing arena is split by software application into two areas. At the lower end, the emergence of desktop-publishing features in what were formerly word-processing packages has spurred growth in single-page monitors. Popular single-page units such as the Genius from Micro Display Systems (Hastings, MN) offer significant cost advantages over two-page units. That unit, now available in a 19-in. version called the Genius^2, offers a 1,280-×1,024-pixel resolution and adds a PC-compatible interface board with a Texas Instruments 34010 coprocessor to speed operation.

Both the Genius^2 and its predecessor are portrait-mount monitors. As the photographic term implies, portrait-format monitors orient the display vertically. This approach mimics the $8\frac{1}{2}$-×11-in. sheet of paper on which the finished product will be published, giving users a fairly accurate prepublication picture.

Flat and square monitors such as Toshiba's 21-in. FS give the user a slightly larger viewing area and less corner distortion than do curved faceplate monitors. The 64-kHz, 1,280- × 1,024-pixel monitor is due out by year-end. A multiscanning version, ranging from a 1,024- × 768- to a 1,280- × 1,024-pixel resolution, will be available in early 1989.

Although less-expensive, portrait-mount displays are limited in that they can't display two pages at once. Highly sophisticated desktop-publishing packages such as Ventura offer fairly complex page-layout functions that are best utilized in a two-page display. A two-page display such as Cornerstone Technology's new 19-in. Dualpage, introduced at Comdex this spring, lets desktop publishers view two-sized pages side-by-side. The display system supports up to 16 levels of gray at a 1,600-×1,280-pixel resolution.

Hitachi (Hayward, CA) added a 20-in. monochrome monitor last February to its product line with the same applications in mind. The MM2136 features a universal power supply and a video analog amplifier to drive a wider range of grayscales than those offered by typical TTL monitors. The monitor offers a 1,280-× 1,024-pixel resolution. □

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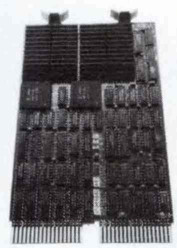

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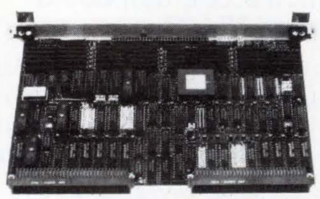

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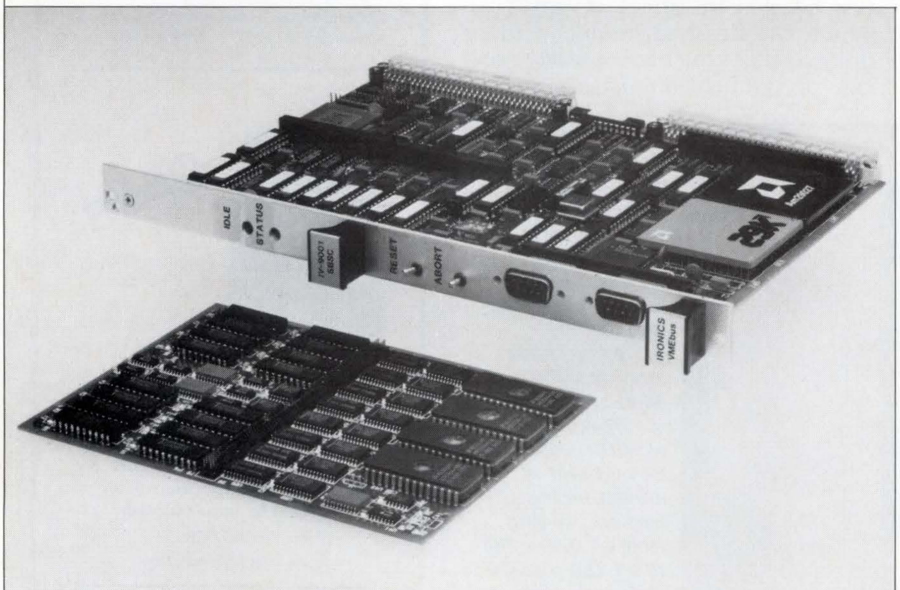
CIRCLE NO. 25

COMPUTERS AND SUBSYSTEMS

VMEbus single-board computer uses RISC chip for 17-Mips performance

Based on the Am29000 reduced-instruction-set microprocessor from Advanced Micro Devices, the IV-9001 is a VMEbus single-board computer that provides a sustained execution rate of over 17 Mips from 16 kbytes of cache as well as up to 16 Mbytes of dynamic RAM. The board uses a unique memory architecture that lets local buses achieve 200-Mbyte/s transfer rates through interleaved DRAM memory, same-page algorithms and a coherent cache design that avoids stale data in multiprocessor applications.

The base system consists of a 6U VMEbus board with the Am29000 25-MHz microprocessor, a 16-kbyte data cache, two single serial I/O ports, local board control, and the VMEbus interface and debug monitor in ROM. An optional Am29027 floating-point unit is also offered. The board features several daughterboard options developed for personalizing the architecture to the application, providing interfaces for additional RAM and I/O. DRAM daughter boards are available in 2-, 8- and 16-Mbyte versions. A family of I/O daughter boards is being developed that includes VSB and a variety of networking interfaces.

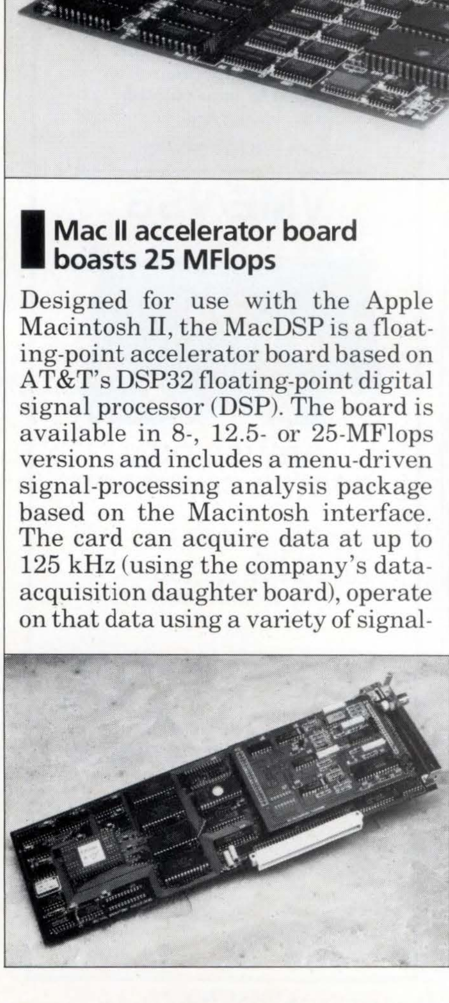


Local memory is dual-ported to both the VMEbus and the I/O daughter-board interface, with all shared or dual-ported accesses to the local memory sent through the cache. On a write cycle, the cache as well as the DRAM is updated, eliminating the need for a complex bus-watching algorithm for cache coherency. In quantities of 100, the price is $6,495.

Ironics
798 Cascadilla St
Ithaca, NY 14850
Circle number 146

Mac II accelerator board boasts 25 MFlops

Designed for use with the Apple Macintosh II, the MacDSP is a floating-point accelerator board based on AT&T's DSP32 floating-point digital signal processor (DSP). The board is available in 8-, 12.5- or 25-MFlops versions and includes a menu-driven signal-processing analysis package based on the Macintosh interface. The card can acquire data at up to 125 kHz (using the company's data-acquisition daughter board), operate on that data using a variety of signal-processing functions and display the data in real time.



A wide range of signal-processing functions are supported, including fast Fourier transforms, spectral averaging, Hilbert transforms, Hamming, Blackman and Kaiser windows, and differentiators. To select a function, users click on the appropriate icon. In response, the MacDSP immediately applies the function and displays the results in real time. Function parameters, such as a filter's cutoff or gain, can be altered and applied to incoming data, to data stored in main memory (up to 800 ksamples/s), or to data that's been captured on disk (up to 70 ksamples/s). Flexible viewing modes allow the display of data in terms of magnitude, phase, color spectrogram or waterfall formats. Prices for the accelerator card start at $2,249.

Spectral Innovations
292 Gibraltar Dr
Sunnyvale, CA 94089
Circle number 147

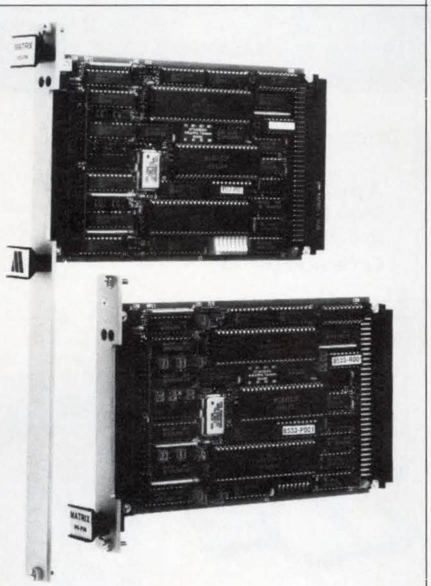
STEbus computer transfers data at 5 Mbytes/s

An MS-DOS compatible single-board computer based on STEbus architecture, the SV25 is built around an NEC 8086 code-compatible CMOS microcontroller. The board features a 1-Mbyte address field, 4 kbytes of I/O space and multimaster capability, with asynchronous, nonmultiplexed data transfer at rates up to 5 M-bytes/s. Also included on the board are two RS-232 serial ports, 24 buffered I/O lines capable of sinking or sourcing up to 48 mA, two 16-bit programmable counter/timers and a dual-channel direct memory access controller. The single-board computer can support up to 384 kbytes of local memory, permitting large target application programs to be run entirely on-board.

Val-Tech
24 McMillan Way
Newark, DE 19713
Circle number 148

Interface card offers 32 lines of byte-programmable I/O

A single-height VMEbus I/O interface card, the MS-PIM hosts 32 lines of byte-programmable I/O, in addition to eight handshake and 10 auxiliary lines. Each of the two 50-pin headers is a 16-bit channel composed of two 8-bit I/O ports. No additional hardware is needed to drive Opto-22 type inputs, since each output can drive up to 48 mA. Each channel is capable of supplying up to 350 mA of



5-V power at each header, eliminating the need for an external power supply. Interrupts may be generated from parallel I/O port activity, I/O handshaking, external header input, timers or I/O data match/mismatch. The price is $595.

Matrix
1203 New Hope Rd
Raleigh, NC 27610
Circle number 149

PC AT-compatible SBC expands to 4 Mbytes

A highly integrated IBM PC AT computer system on a single 13.25-×4.8-in. board, the CAT903 requires only a single slot in an AT passive backplane. The single-board computer has a 12-MHz CPU, a floppy and ST506 hard disk controller, two serial ports, a parallel port and sockets for up to 4 Mbytes of RAM. The onboard Enhanced Graphics Adapter (EGA) video subsection provides compatibility with standard EGA, Color Graphics Adapter, Hercules Graphics Adapter and Monochrome Display Adapter graphics display modes. Prices start at $850.

Diversified Technology
112 E State St
Ridgeland, MS 39158
Circle number 150

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CIRCLE NO. 26

DESIGN AND DEVELOPMENT TOOLS

16.7-MHz zero-wait-state emulation offered for 68000 microprocessor

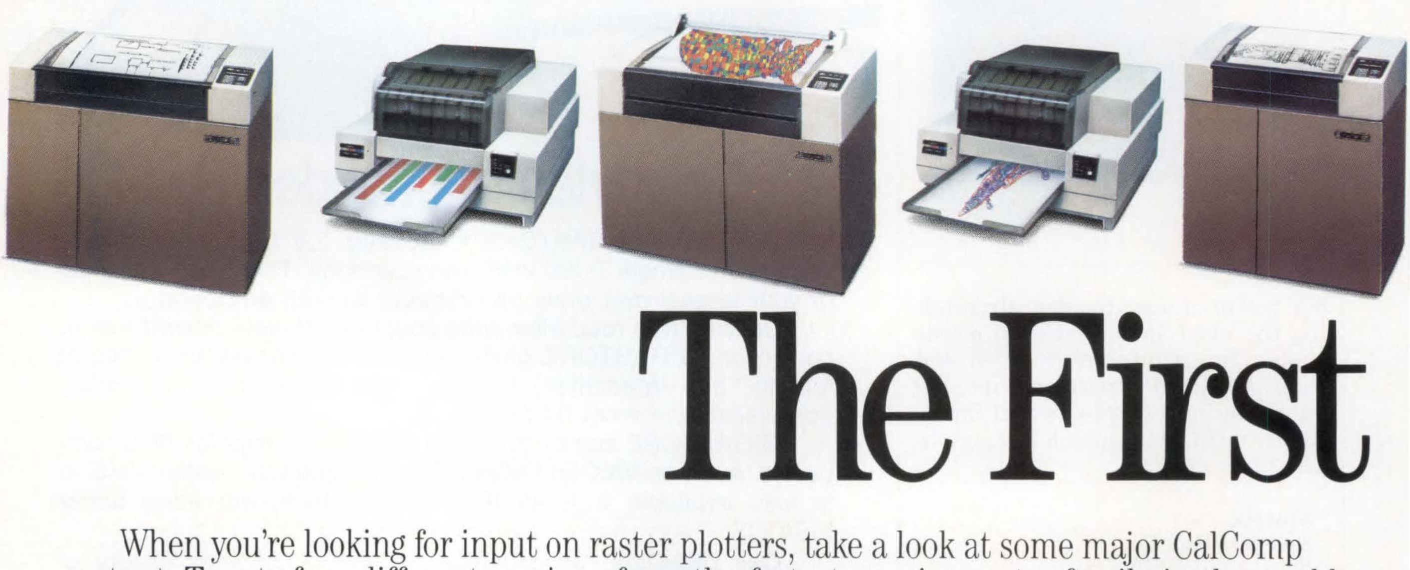
A 16.7-MHz probe module allows zero-wait-state emulation support for the Motorola 68000 microprocessor. Supporting both the dual in-line and plastic leaded chip carrier 68000 packages, the module connects to the manufacturer's ES 1800 emulator for operation with a variety of host computers, including Sun, Apollo, VAX, IBM PCs and compatibles.

The emulator utilizes an Advanced Event Monitor System that lets an engineer control emulation by breaking on any combination of address, data status, pass counter and logic state fields. An event or combination of events, defined by logic statements, can be used to break emulation, trace software sequences and count events or trigger outputs. A small computer systems interface option allows a faster data-rate transfer than the RS-232 interface.

In addition, the Validate family of software development tools provides full C source-level debugging. The probe module costs $4,095; emulator prices start at $11,000.

Applied Microsystems
5020 148th Ave NE
Redmond, WA 98073

Circle number 151



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DESIGN AND DEVELOPMENT TOOLS

ASIC design toolkit runs on Mentor/Apollo platforms

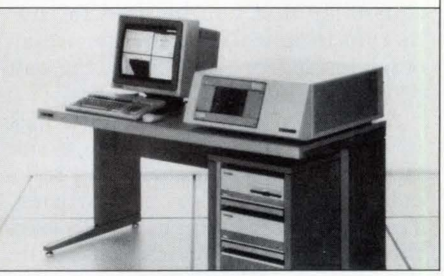
A toolkit for the design of application-specific ICs, the VLSI Design System operates with release 6.0 of Mentor Idea software running on Apollo hardware platforms. The toolkit is technology-independent and supports all phases of gate array design. Facilities for schematic capture and logic simulation are included, as well as back annotation of pin delays, static timing analysis and timing simulation. A key feature of the toolkit is support for advanced design-for-test techniques, including serial scan, boundary scan and VHSIC Phase 2 Test and Maintenance bus. The kit is available in two forms: Design Capture and Design Verification. Design Capture provides complete capture and "what if" analysis capability, and is priced at $2,500 per workstation node or $5,000 per site. At $7,500 per node or $15,000 per site, the Design Verification package includes complete workstation-based capture and simulation tools, in addition to the tools supplied with Design Capture.

Honeywell
1150 E Cheyenne Mountain Blvd
Colorado Springs, CO 80906
Circle number 152

IC evaluation system tackles turnaround time

Using tester-per-pin architecture, the HP82000 IC Evaluation System provides bidirectional timing and level capabilities to each pin without sharing resources. This capability lets a new device test be set up quickly because the user isn't restricted by limited system resources. In addition, it avoids the need for time-consuming pin-wiring. Device parameters for ac and dc such as propagation delay and leakage current can be measured by executing ready-to-use test routines. The user has a choice of result displays: three-dimensional Schmoo plots, high-resolution timing diagrams, state lists and error maps. Prices for the system start at $65,000.

Hewlett-Packard
19310 Pruneridge Ave
Cupertino, CA 95014
Circle number 153



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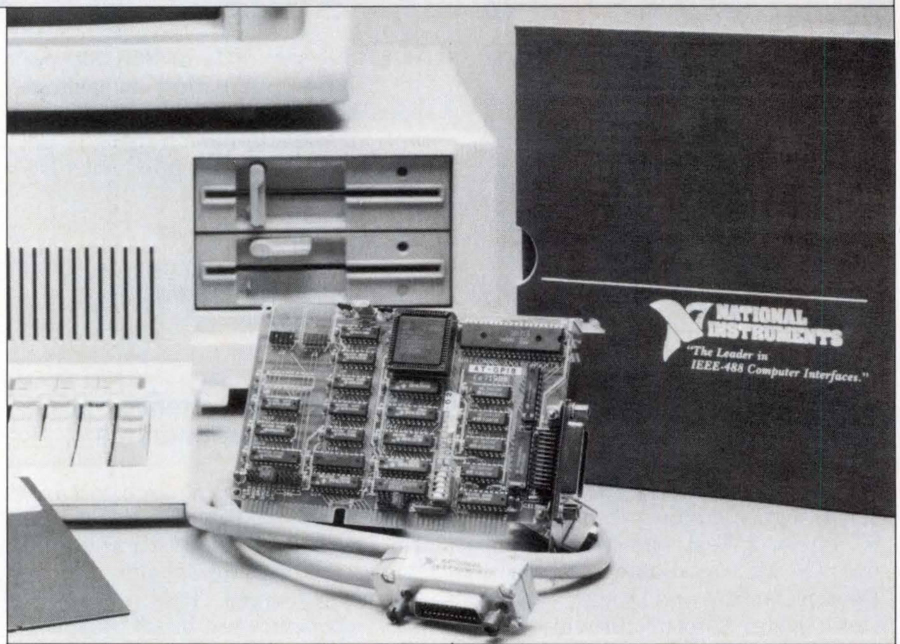
CIRCLE NO. 27

DATA ACQUISITION AND CONTROL

Controller implements IEEE-488 functions on IBM PC ATs



Developed specifically for 80386- and 80286-based personal computers with 16-bit plug-in slots, the AT-GPIB is a stand-alone, plug-in circuit card that provides IEEE-488 interface functions. Standard, double-shielded IEEE-488 cables can connect the device with up to 13 instruments (or more using the manufacturer's extender card). A computer configured with the hardware/software package becomes an IEEE-488 controller that can be used for numerous applications in the areas of lab testing, production testing and process monitoring and control.

An on-board NECμPD7210 GPIB interface controller implements the IEEE-488 functions including talker/listener/controller capabilities. The controller, which is accessed through a custom application-specific IC, contains 21 separate program registers. These registers configure, control and monitor all data flow, interface functions and transfer commands from other IEEE-488 devices.

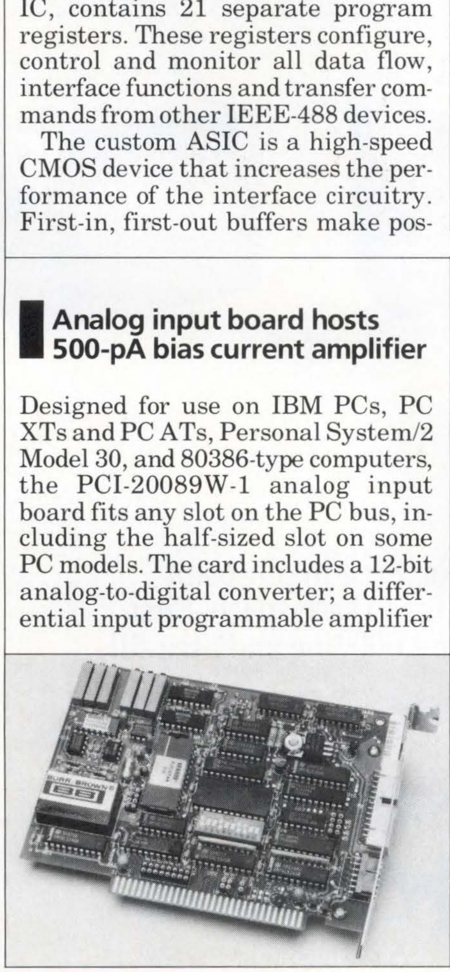
The custom ASIC is a high-speed CMOS device that increases the performance of the interface circuitry. First-in, first-out buffers make possible high-speed, burst-mode direct memory access (DMA) transfers, 1-Mbyte/s GPIB reads, 700-kbyte/s GPIB writes and 320-kbyte/s GPIB commands. The PC takes advantage of byte-to-word packing and unpacking circuitry in the ASIC to communicate with the IEEE-488 bus in full 16-bit mode, rather than 8-bit bytes, halving the data transfer overhead and PC I/O channel utilization time.

The device is capable of interrupting the PC microprocessor via one of 11 jumper-selectable input lines. Full AT bus 16-bit DMA transfers are supported. The controller card with software is priced at $495.

National Instruments
12109 Technology Blvd
Austin, TX 78727
Circle number 179

Analog input board hosts 500-pA bias current amplifier

Designed for use on IBM PCs, PC XTs and PC ATs, Personal System/2 Model 30, and 80386-type computers, the PCI-20089W-1 analog input board fits any slot on the PC bus, including the half-sized slot on some PC models. The card includes a 12-bit analog-to-digital converter; a differential input programmable amplifier with gains of 1, 10 and 100; a sample-and-hold amplifier; and a CMOS multiplexer that scans up to 16 single-ended or eight differential input signals. The board also has an internal timebase/rate generator and a general-purpose digital counter for measuring output rates of tachometers and other pulse-generating devices. Counter inputs can be at rates of up to 8 MHz. The price is $495.



Burr-Brown
1141 W Grant Rd
Tuscon, AZ 85705
Circle number 180

Mezzanine module boosts MAP controller performance

A MAP controller board, the MVME-372A is an enhanced version of the previously released MVME372 and consists of the MVME372 plus a plug-in mezzanine board. Implemented in surface-mount technology, the mezzanine board speeds up all EPROMs on the host controller and adds 256 kbytes of static RAM to the 640 kbytes of dynamic RAM resident on the main board. VLSI devices on the controller include the MC68824 Token Bus Controller and a 12.5-MHz MC68020 32-bit microprocessor. Generic 40-pin 802.4.G serial interfaces to the off-board modem allow connection to a broadband, carrierband or fiberoptic physical layer, while the Common Environment firmware provides communication with other processors and communications modules on the VMEbus.

Motorola Microcomputer Div
2900 S Diablo Way
Tempe, AZ 85282
Circle number 181

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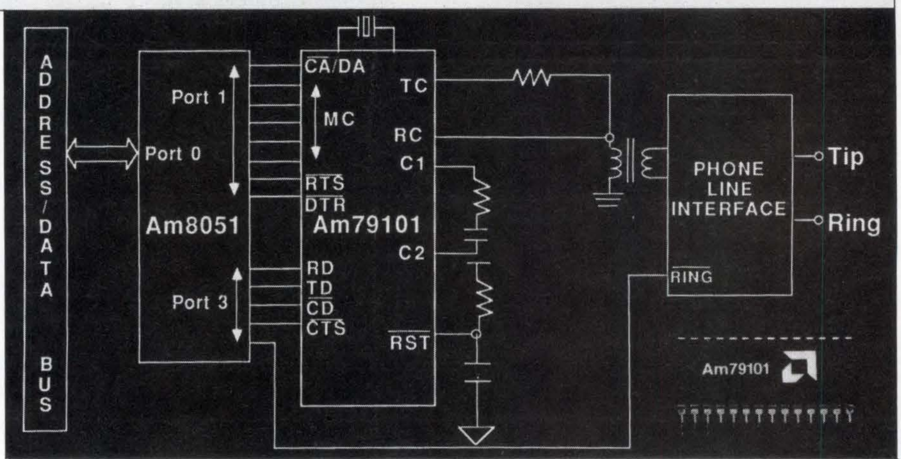
INTEGRATED CIRCUITS

Single-chip frequency shift keying modem needs no external dialer

Operating at 300 bits/s full duplex and 1,200 bits/s half duplex, the Am-79101 single-chip frequency shift keying modem features a dual-tone multifrequency generator that eliminates the need for an external dialer chip. It provides modulation, demodulation, filtering, analog-to-digital and digital-to-analog functions.

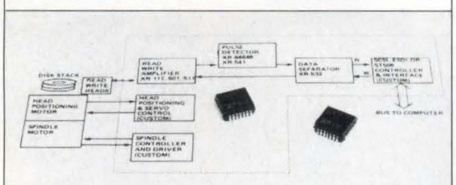
An intelligent autodial, auto-answer modem can be easily implemented using the Am79101 under the control of a host microprocessor. Connection to the switched network requires a simplified data-access arrangement circuit. Fully compatible with CCITT V.21, V.23 and Bell 103 and 202 modem standards, the modem chip features digital signal processing architecture. The device is available in 28-pin plastic leaded chip carrier and 28-pin plastic and ceramic dual in-line packages.



Advanced Micro Devices
901 Thompson Pl
Sunnyvale, CA 94088
Circle number 154

Pulse detector boasts 1-ns/2.5-MHz pairing

An addition to the manufacturer's hard disk component line, the XR-541 pulse detector IC offers pulse-pairing accuracies of better than 1 ns at 2.5 MHz. The device is compatible with both modified frequency modulation and run-length-limited clock encoding techniques. When used with the manufacturer's existing



line of read/write amplifiers, it provides the complete analog channel for low- to high-density Winchester disk drives. Fabricated using a high-speed bipolar process with mixed linear and digital functions, the chip uses ECL logic, which minimizes performance-degrading current transients. The device is available in a 28-pin plastic leaded chip carrier. In lots of 1,000, the pulse detector is priced at $5.85.

Exar
2222 Qume Dr
San Jose, CA 95161
Circle number 155

RISC processor speeds to 60 MHz

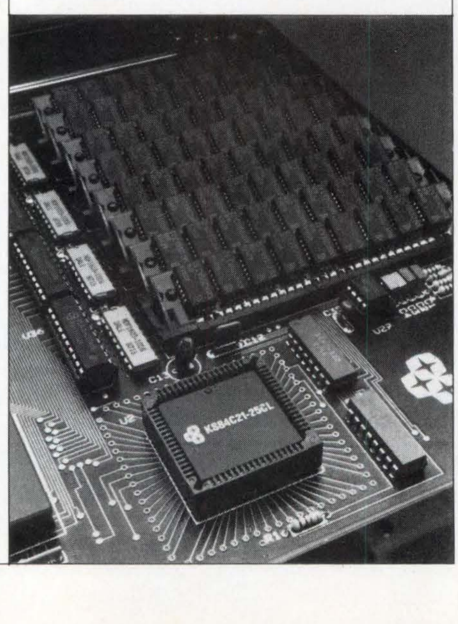
A 32-bit reduced instruction set microprocessor, the MD-484 has been clocked at almost 60 MHz and produces an output every 17 ns. The gallium-arsenide device consists of 21,606 transistors using enhancement mode junction field-effect transistor technology with 17 general-purpose registers and a full 32-bit arithmetic logic unit. In addition, the microprocessor provides a barrel shifter for specialized computer operations. The chip, when combined with recently developed high-speed memory chips and large gate array circuits, provides the military with a very high speed, rad-hardened computer that meets Strategic Defense Initiative processing requirements.

McDonnell Douglas
5031 Bolsa Ave
Huntington Beach, CA 92647
Circle number 156

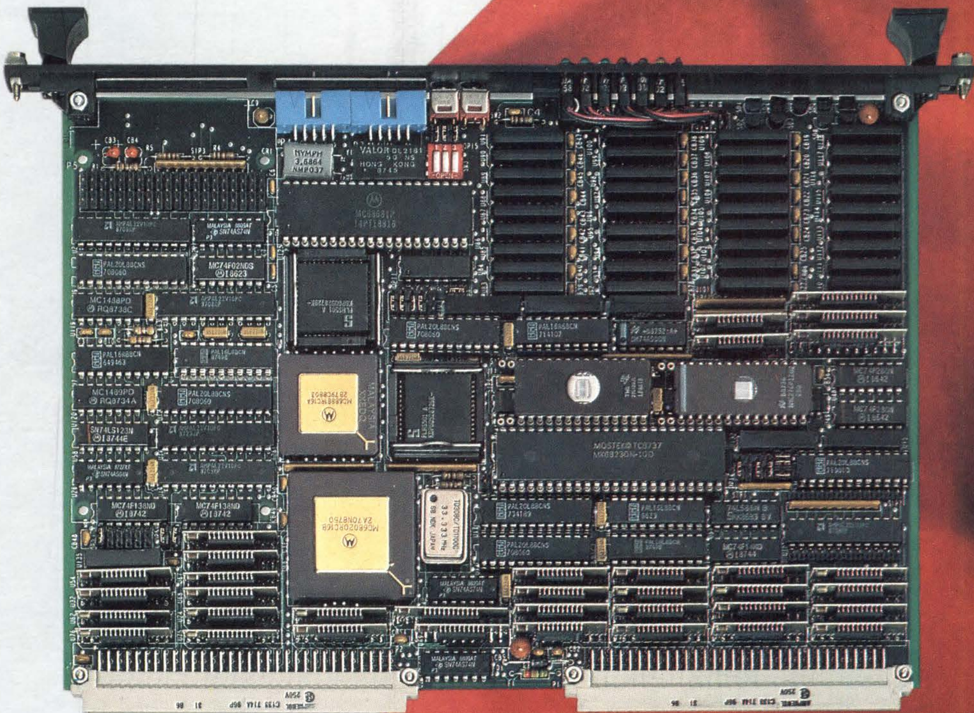
Controllers squeeze 80-ns performance from DRAMs

Two high-performance dynamic RAM controllers for 256-kbit, 1-Mbit and 4-Mbit DRAMs accelerate array speed by 30 percent and simplify the interface between controller and microprocessor. The KS84C21 supports 256-kbit and 1-Mbit DRAMs, while the KS84C22 supports these devices as well as 4-Mbit DRAMs. Both controllers can make 120-ns DRAMs appear to a system as if they were 80-ns DRAMs. Available in externally programmable or mask-programmable versions, the controllers have a drive capability of 500 pF, sufficient to drive arrays of at least 88 DRAMs under worst-case conditions. The price is $22.80 in 1,000-piece quantities.

Samsung
3725 N First St
San Jose, CA 95134
Circle number 157



Our 68020 VME SBC Gives You Flexible I/O



OB68K/VSBC20™ with OMNIMODULES™

Our OB68K/VSBC20 with its OMNIMODULE™ modular I/O, adjusts to meet your I/O needs. You can add 2 more serial ports or 20 more lines of parallel I/O. GPIB or SCSI can also be added. Our prototyping module even allows you to implement custom I/O. And with an OMNIMODULE on board, the OB68K/VSBC20 still uses only one slot.

Additional features include:

- 16 MHz 68020 (other speeds optional).
- 1-4 MB of dual access DRAM with parity (0-wait-state up to 20 MHz).
- (2) asynch RS232C serial ports.
- 16-bit parallel port.
- 68881/2 Co-Processor (optional).
- (2) 32-pin ROM sockets.
- 4 level VME arbiter (optional).
- Mailbox interrupt.
- Supports unaligned transfers (UAT).
- IEEE 1014 (Rev. C.1) compatible.
- 2 year limited warranty.

Today your choice of OMNIMODULE's include:

- Kluge prototyping module.
- (2) asynch RS232C serial ports.
- (2) synch/asynch RS232C serial ports.
- (2) asynch RS422 serial ports.
- (20) lines of parallel I/O.
- SCSI controller.
- GPIB interface.
- And more to come!

To learn more about our OB68K/VSBC20 or OMNIMODULE modular I/O, contact our Marketing Manager, Peter Czuchra at 1-800-638-5022 or (312) 231-6880 in Illinois.

OMNIBYTE™

OMNIBYTE CORPORATION
245 W. Roosevelt Road
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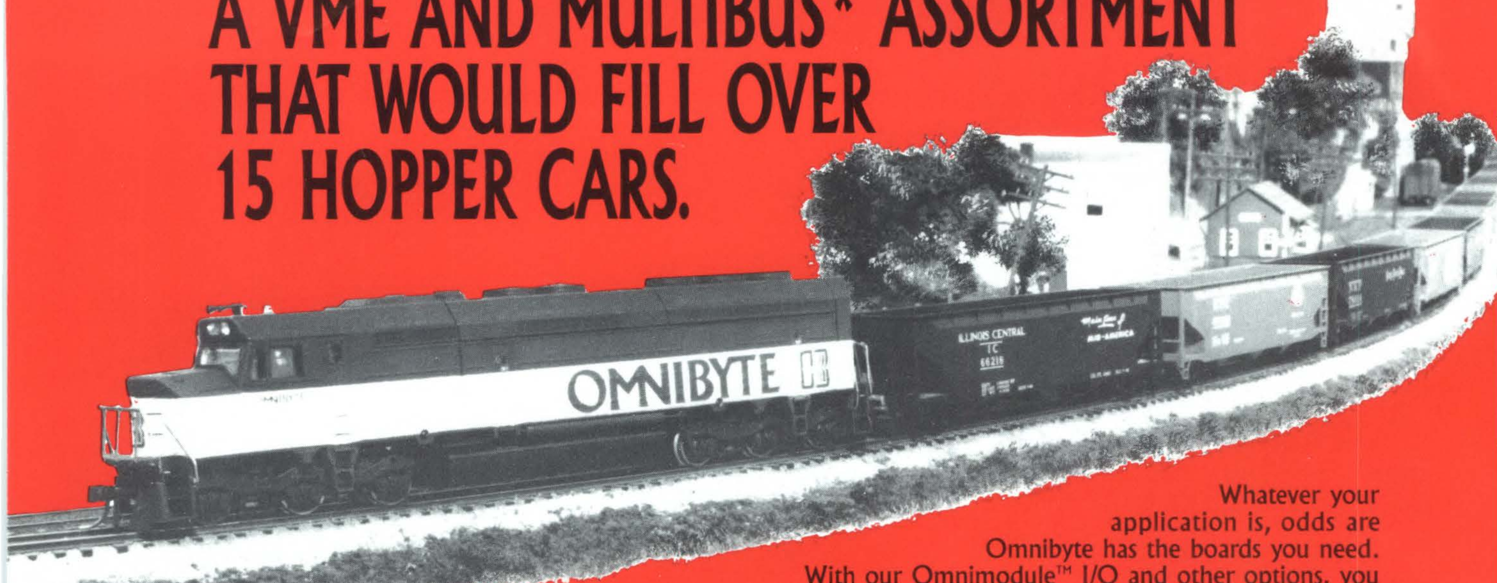
1-800-638-5022

A Look At Today. . . A Vision Of Tomorrow.

CIRCLE NO 120

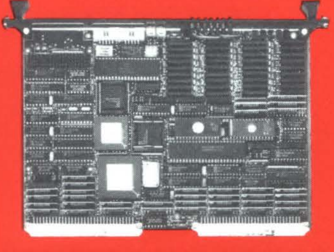
A VME AND MULTIBUS* ASSORTMENT THAT WOULD FILL OVER 15 HOPPER CARS.



Whatever your application is, odds are Omnibyte has the boards you need. With our Omnimodule™ I/O and other options, you can select from over 84,000 different single board computers and I/O configurations. If you ordered one of each, we'd need over 15 hopper cars to ship them. And they come with a 2 year limited warranty. Here are a few of the thousands of outstanding boards we offer.

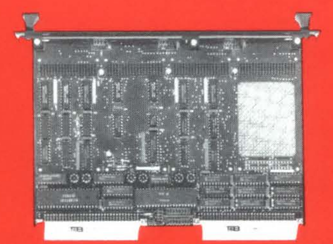
If you don't see the board you need in this ad or would like more information, call our Marketing Manager, Pete Czuchra today. He'll put you on the right track to finding the boards that fit your needs.

OB68K/VSBC20™ VME SINGLE BOARD COMPUTER



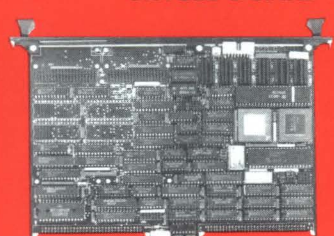
- 68020 12.5 – 33MHz CPU
- 1-4 MB of dual-access, zero-wait-state DRAM with parity
- 68881/2 (optional)
- (2) 32-pin ROM sockets
- (2) RS232C serial ports
- (2) 8-bit parallel ports
- (1) OMNIMODULE socket for a wide variety of I/O (ie. 2 serial ports, 20 parallel lines)
- 4 level bus arbiter (optional)

THE OB68K/VIO™ VME UNIVERSAL I/O BOARD



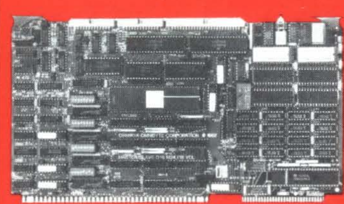
- (4) Omnimodule I/O sockets for a wide variety of I/O (ie. 8 serial ports, 80 parallel lines)
- One (1) interrupt per Omnimodule, two (2) optional

OB68K/VSBC1™ VME SINGLE BOARD COMPUTER



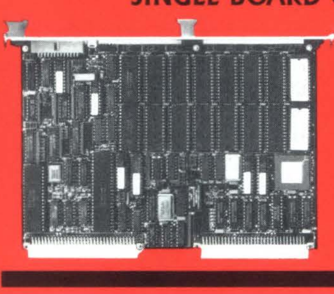
- 68000/10 12.5-16MHz CPU
- 512KB of dual-access, zero-wait-state DRAM with parity
- (4) 28-pin ROM sockets
- (3) 16-bit counter/timers
- (2) Omnimodule™ I/O sockets for a wide variety of I/O (ie. 4 serial ports, 40 parallel lines)
- DMA controller (optional)
- VME bus interrupter (optional)
- Optional 4 level bus arbiter

OB68K1A™ MULTIBUS SINGLE BOARD COMPUTER



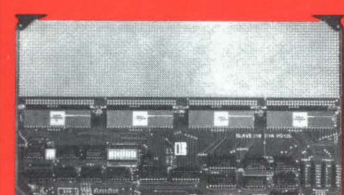
- 10MHz 68000 CPU
- 128K/512K of zero-wait-state dual ported RAM
- Up to 192K bytes of EPROM
- (2) RS-232C serial ports
- (2) 16-bit parallel ports
- A triple 16-bit timer/counter
- (7) Prioritized-vectored interrupts

OB68K/VME1™ VME SINGLE BOARD COMPUTER



- 12.5MHz 68000 CPU
- (8) pairs of 28-pin sockets for RAM and ROM (up to 448K RAM or 896K ROM)
- (2) RS-232C serial ports
- (2) 8-bit parallel I/O ports
- System controller

OB68K230™ MULTIBUS PARALLEL I/O BOARD



- 96 bits of software definable parallel I/O
- (4) 68230 PI/T chips
- (4) 24-bit timers
- 35 sq. in. of prototyping area

OMNIBYTE™

OMNIBYTE CORP.
245 W. Roosevelt Road
West Chicago, IL 60185
1-800-638-5022
In IL (312) 231-6880

Photo shot at Midwest Railroad Modelers, Batavia, IL. *Multibus and ISBX are trademarks of Intel Corp.

CIRCLE NO 119

SOFTWARE

Simulator software package features C source-level debugger

A personal computer-hosted software package, the Simcase microcontroller simulator has a C source-level debugger. Designed to work with the manufacturer's microcontroller C cross compilers, the package speeds up development by allowing software prototyping without any target hardware. The kit consists of several integrated parts: the simulator engine, the C and Assembler source debugger, the performance-analysis tool, and the input stimulus generator.

The simulator engine, the core of the product, simulates the complete microcontroller on the PC, including the instruction set, the interrupt handling system and all I/O ports. Users are given the option of symbolic and source debugging on the C and/or Assembly level by the source debugger, which includes all of the traditional debugging tools such as trace, code and data examinations, step, and breakpoints.

Execution times of every block and line of code are given by the performance-analysis tool, which helps the user identify performance bottlenecks in the microcontroller design. With the input stimulus generator, the user can simulate real-time I/O-intensive applications by creating input stimulus files that are mapped to any I/O port. This tool can also simulate and test out worst-case scenarios, including hardware tolerances, right on the PC.

A window-based program, the simulator kit includes a special 43-line Enhanced Graphics Array mode, a slow-motion mode that continually updates hardware and debug information, and a fast-motion mode that updates screens only when there's a program interrupt or a breakpoint. The package supports all Intel 8051 proliferation chips and will operate on any IBM PC XT, PC AT or compatible with 640 kbytes of RAM using MS-DOS 2.1 or higher.

Archimedes Software
2159 Union St
San Francisco, CA 94123
Circle number 123

Software runs CodeView in less than 8 kbytes

An add-on to Microsoft's CodeView debugger, MagicCV reduces the conventional memory requirements of CodeView from 200 kbytes to less than 8 kbytes. The software requires an 80386 personal computer such as the IBM Personal System/2 Model 80 or equivalent, and uses the virtual machine capabilities of the 80386 to run CodeView and program symbols in separate virtual machine extended memory. This gives the users more than 500 kbytes of conventional memory for target programs, device drivers and resident programs. The price is $199.

Nu-Mega Technologies
PO Box 7607
Nashua, NH 03060
Circle number 124

Operating system provides real-time Ada tasking

Targeted to a Force CPU-386A single-board computer, the DACS-80× 86 is an Ada compiler system that doesn't need a third-party kernel or executive to handle time-critical task management. A pure Ada real-time operating system is provided by the port, which has met the validation requirements of the Department of Defense (DOD). By eliminating the need for a separate third-party task scheduler, the port cuts system development time, simplifies the integration of application software and eases compliance with DOD specifications mandating Ada-compiled software. Prices range from $10,000 to $40,000, depending on the host.

DDC-I
PO Box 37767
Phoenix, AZ 85069
Circle number 125

Object module librarian reduces link time

Boasting speeds that are ten times faster than Microsoft's librarian, Optlib is an object module librarian that provides a complete cross reference for the programmer, while reducing link time. Directory control directives let users set the maximum number of collisions and the maximum directory size. All necessary librarian functions are supported, including adding modules or libraries, deleting and extracting modules, and public symbol listing for each module. Further reporting capabilities include an index and a symbol map. The software is fully compatible with Microsoft format object modules and is priced at $49.

SLR Systems
1622 N Main St
Butker, PA 16001
Circle number 175

Software performs like Unix for PC XTs/ATs

An operating system comparable to Unix for IBM PC XTs, PC ATs and compatibles, Minix includes more than 50,000 lines of C source code and 75 utilities. The software is functionally similar to the Bourne shell used in Unix, supports hard and floppy disks, and features over 100 library procedures. Full multiprogramming is offered by the operating system as well as an Emacs-style full-screen editor with the C compiler source available separately. The software and reference manual is priced at $110.

Simon & Schuster
Prentice Hall Building
Englewood Cliffs, NJ 07632
Circle number 127

Library provides windows for PCs with C compilers

A windowing package for PCs and compatibles, Aewindos software works with most popular C compilers (Turbo C, Microsoft, Quick C, Lattice and Power C). A snapshot program copies any portion of a screen into a window and incorporates it into a library while a window editor lets programmers paint windows for storage.

Aesoft
2570 Woodstock Pl
Boulder, CO 80303
Circle number 176

SOFTWARE

Software bridges development from Unix host to OS-9 targets

Unibridge is a software package that lets system developers link a Unix host system, using Ethernet and the TCP/IP protocol, to real-time target systems that run the OS-9 operating system. The package uses communications library routines to implement the "socket" interface that's part of the Berkeley BSD 4.2 version of Unix, speeding applications movement through Unibridge.

With the help of Telnet communications software, utilities provided with the package allow remote log-in to other systems for transfer of files. Cross compilers for 68000 or 68020 chips are then used to produce executable code modules for target systems that run OS-9. A source-level debugger is provided that runs on target computers equipped with OS-9, which can call on the Unix host for source-code file information.

Assembly-level debuggers are also available that access OS-9 kernel system calls without affecting on-going applications. A special system state debugger is included that takes control of registers and stops the target computer to look at processes. Once the applications code has been downloaded and debugged, target systems can operate on a stand-alone basis. The Ethernet link to the host can be maintained, however, so that the target systems can continue to function in tandem with the host.

Microware
1900 NW 114 St
Des Moines, IA 50322
Circle number 158

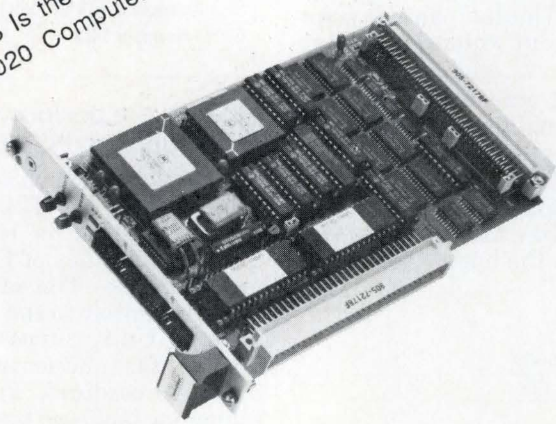
Software package features real-time VMEbus integration

A software package for VMEbus real-time multiprocessing system integration, EASI-RT lets a programmer implement an entire application by changing parameters in a configuration file. Hardware bugs or mistakes in physical configuration of the system can be found by running the sample application and configuration file immediately after setup to test system operation. Applications requiring off-the-shelf real-time kernel or user-written real-time executives are also supported. The configuration file specifies which standard real-time components to include or not include in the application. The software runs only on the manufacturer's Performer 32 VMEbus Unix systems and costs $995.

Ironics
798 Cascadilla St
Ithaca, NY 14850
Circle number 159

Think Small.

Our SBC-3 Is the Fastest Selling 3U-MC68020 Computer Board!



Yes, think small. And simple. And cost-effective. Single-high VMEbus computer modules offer no-nonsense solutions to your industrial control requirements while mounting in either single-high or double-high VME chassis.

VME Specialists brings the industry a broad single-high VMEbus product line. Select from among four single-high single board computers, hosting Motorola 68000/68010/ and 68020 processors. Breadth to support your diverse requirements, from our very low cost SBC1, to our 68020 based SBC3 with location monitor, OEM expansion connector, floating-point co-processor, real-time clock, ROR requestor, dual-port RAM and twin serial ports. And the same software can run on all members of the family.

Look to VME Specialists for processor support functions, development assistance, and operating software.

DRAM Memory modules of 1 through 16 Mbytes

SCSI Our VME620 with DMA and 512 Kbytes of dual port cache

Serial I/O The VME490 multiprotocol serial I/O co-processor

Video VME360 High-resolution color graphics with palette

Development made easy Consider our VME1100 development system

Not to mention software Like OS9™ and REGULUS™ real-time OS

We're VME Specialists. The solution was never easier.

VME specialists
558 Brewster Ave.
Redwood City, CA 94063
415 364-3328
Fax 415 369-5982

CIRCLE NO. 29

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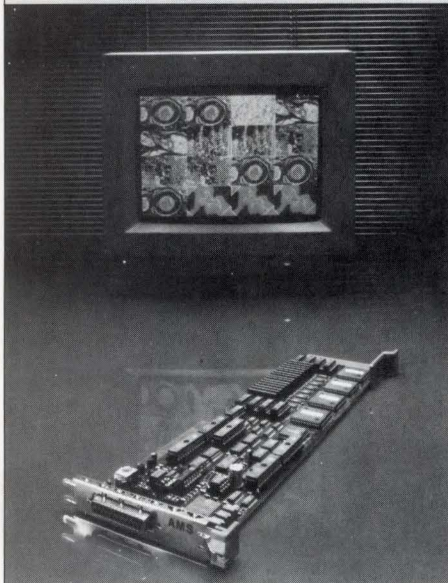
CIRCLE NO. 28

GRAPHICS AND IMAGING



PS/2 frame store houses 2 Mbytes of image memory

An IBM Personal System/2-compatible frame store, the Photon Card has 2 Mbytes of memory that can be configured as five 720×560 8-bit image stores. Rapid transfers to the host computer are accomplished using the on-board direct memory access controller. The board also features the Hitachi ARCTC graphics controller for generation of overlays, cursors and text. An output look-up table lets pseudocolor displays be generated with a choice of 256 colors from a palette of 16 million. Graphics overlay is also featured on real-time monochrome or color video signals.

Analytical Measuring Systems
London Rd, Pampisford,
Cambridge, Cambs, CB2 4EF, England
Circle number 129

Library develops 3-D graphics quickly on PCs

Software developers can write large device-independent three-dimensional graphics applications on a personal computer equipped with an Nth 3-D Engine display controller. Hoops, a high-level, object-oriented graphics library, runs in an on-board T800 Inmos transputer without impacting DOS memory limits. Software applications may be transferred to a PC using the hardware/software package without recompilation or a new device driver. The relinking process is handled through C and/or Fortran bindings on the PC that pass commands to the graphics engine where the software calls are handled. Polygon transparency and vector antialiasing are also featured.

Nth Graphics
1807-C W Braker Ln
Austin, TX 78758
Circle number 177

PC graphics board supports 640- × 400-pixel resolution

The SuperSpectrum graphics add-on card for IBM PCs, PC XTs, PC ATs and compatibles provides a full spectrum of features from IBM Monochrome Display Adapter, Color Graphics Adapter, Plantronic Plus and Hercules graphics. Implemented with the manufacturer's proprietary application-specific IC chips, the board is compatible with color or monochrome monitors and comes with a parallel port and installation software. The card supports speeds of up to 25 kHz, offers 16 shades of gray when run on a monochrome monitor, can display 132 columns of text, and achieves 640-×400-pixel resolution.

Genoa Systems
75 E Trimble Rd
San Jose, CA 95131
Circle number 131

Software boosts graphics card performance

An updated level of software support for the manufacturer's Ultra Graphics Adapter 1104 PC graphics card, Microcode 4.3 doubles the performance in Autocad's display list redraw. For many applications, such as objects that lie entirely within a clipping region, up to a 46-times performance increase can be achieved. A 31-times performance increase is noticed for filled circles, while for objects that are transformed—such as vectors and polygons—the performance is increased 4.5 times. The microcode also provides a dual-head system configured with an Enhanced Graphics Adapter (EGA) primary display adapter, letting users run high-resolution or standard EGA applications without having to reload the system.

Metheus
5510 NW Elam Young Pkwy
Hillsboro, OR 97214
Circle number 132

Transputers used for parallel processing

A single Eurocard frame grabber, the TFG-Module uses transputers for parallel processing in image-processing applications. The video interface supports all input signals according to the International Radio Consultative Committee or RS170A at up to a 768-×512-pixel resolution with 256 levels of gray scale. Synchronization may be either internal or external (pixel-synchronous), and several of the devices may be cascaded for RGB input. The processor section contains a T800/T414 transputer with 1 Mbyte of memory sporting 10 Mips/1.5 MFlops and can access 0.5 Mbytes of video RAM without additional wait states. The bus-free module may be combined with an adapter for use with a standard personal computer and operates either as a stand-alone or in cooperation with other processors. The same application applies to VMEbus, Q-Bus and Nubus.

Parsytec
Juelicher Strasse 338
D-5100 Aachen, W Germany
Circle number 133

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PAL and PALASM are registered trademarks of Monolithic Memories Inc.

GEOMETRY ENGINE is a trademark of Silicon Graphics Inc.

386, 386SX, 376, Intel386, iRMK, iRMX, and ICE are trademarks of Intel.

MAJOR SYSTEM COMPONENTS

5-V input, ±15-V ouput dc-dc converter guarantees 1-mV output noise

The PWR1546A 5-V input, ±15-V output dc/dc converter has a guaranteed maximum output noise of 1 mV peak-to-peak over a dc to 10-MHz bandwidth. No external parts are required to obtain this performance.

Designed to power sensitive circuits such as high-precision data converters, high-gain amplifiers, precision test equipment or any other low-noise application, the unit is isolated and capable of withstanding up to 750 Vdc continuously from its input to its output. The device measures 2×2×0.4 in. and can be

mounted on a printed circuit board with ½-in. board spacing. Linear regulators are used on each output of the converter.

Due to strict enforcement of design rules, stress ratios are kept small enough to yield a mean time between failures of over 890,000 hr at +25 °C (calculated per MIL-HDBK-217 Rev E, circuit-stress analysis method, ground benign). This is equivalent to over 100 years. In 100-piece quantities, the device is priced at $42.

Burr-Brown
PO Box 11400
Tuscon, AZ 85734
Circle number 160

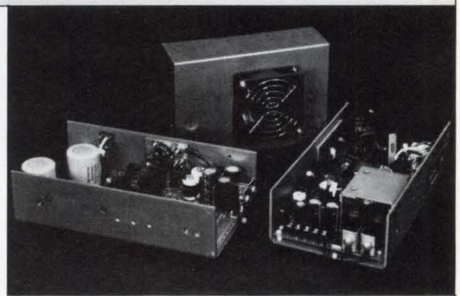
Switcher achieves 4-W/in.³ power density

Using a high-reliability 100-kHz field-effect-transmitter forward converter and optimal packaging, the MD225 triple-output switching power supply features a power density of 4 W/in.³. The unit measures 4×8×1¾ in. and delivers 225 W of fully regulated power. The calculated mean time between failures of the product is in excess of 100,000 hr per MIL HDBK-217E at 40 °C.

Modular Devices
4115 Spencer St
Torrance, CA 90503
Circle number 161

Family of dc-dc converters offers up to 350 W

A family of dc-dc converters provides up to 350 W from 48-Vdc input. Two versions are being offered: a 250-W dc single-output series and a 350-W multiple-output series. With a main output of 50 A of 5-V power, the units feature two fully regulated, high-efficiency, post-regulated mag-amp outputs and one low-power, three-ter-



minal regulated output. The +12-V line has a peak current rating of 12 A, letting it power up to four disk drives. Units can be expanded to include isolation diodes and modified current sharing for redundancy. Optional remote inhibit and dc power fail is available. In quantities of 100, prices range from $296 to $415.

Todd Products
50 Emjay Blvd
Brentwood, NY 11717
Circle number 162

Build Electronic Products That Don't Fail From Surge & ESD.

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KeyTek Instrument Corporation
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Wilmington, MA 01887
Phone (617) 658-0880
TELEX 951389 FAX (617) 657-4803

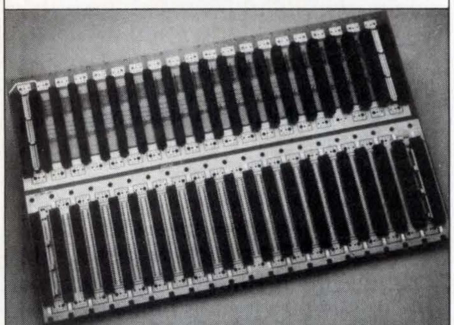
*USA price list

CIRCLE NO. 30

MAJOR SYSTEM COMPONENTS

Monolithic backplane uses six-layer construction

Designed to meet Revision C.1 of the VMEbus specifications, the J1/J2 Monolithic Backplane uses six-layer construction to control impedance, crosstalk and noise. One-piece construction ensures a more stable ground reference for 32-bit implementation and eliminates the potential for ground loops, while two full power plane layers and two full ground plane layers maximize the power distribution system. Initial



size offerings include 5-, 10-, 15- and 21-slot models, with power terminals that are available in three different styles: power cubes, press-fit posts and snap-on lugs.

Augat
33 Perry Ave
Attleboro, MA 02703
Circle number 163

Backplanes comply with IEEE-896.1-1987 standard

Featuring multilayer construction, the Futurebus 10- and 21-slot backplanes provide constant characteristic impedance from microstrip signal lines and effective shielding. High-reliability 96-pin DIN 41612 connectors are assembled on the IEEE-896.1-1987 compatible backplanes, along with ¼-in. power connectors. Off-board termination is incorporated, with rear-pluggable terminator modules available separately. Prices start at $525.

Bicc-Vero Electronics
1000 Sherman Ave
Hamden, CT 06514
Circle number 164

COMPUTER DESIGN

THE FIRST MAGAZINE OF SYSTEM DESIGN, DEVELOPMENT AND INTEGRATION

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Publisher, David L. Allen
Associate Publisher, John C. Miklosz
Marketing Services Manager, Mary M. Gregory
Sales Promotion and Research Manager, Judy Leger
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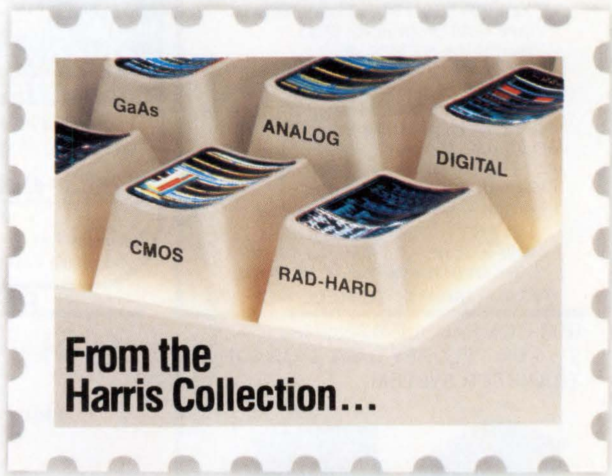

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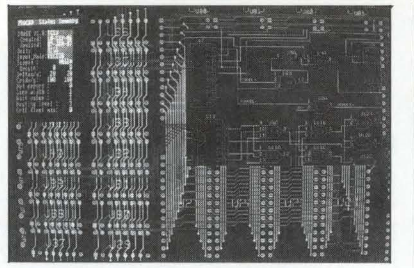

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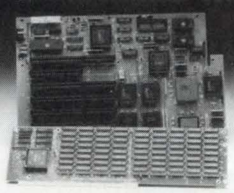

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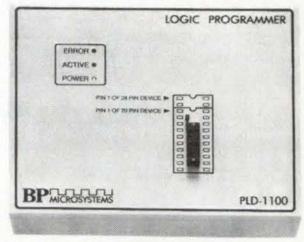

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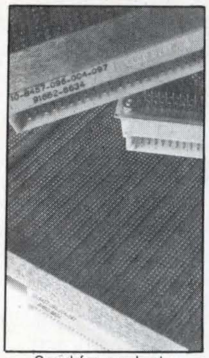

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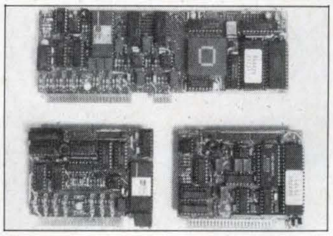

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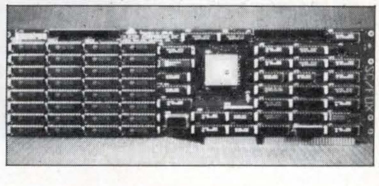

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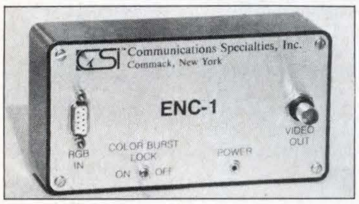

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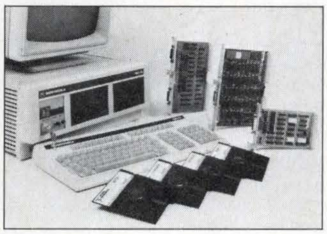

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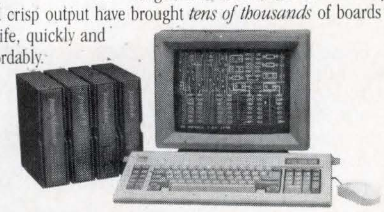

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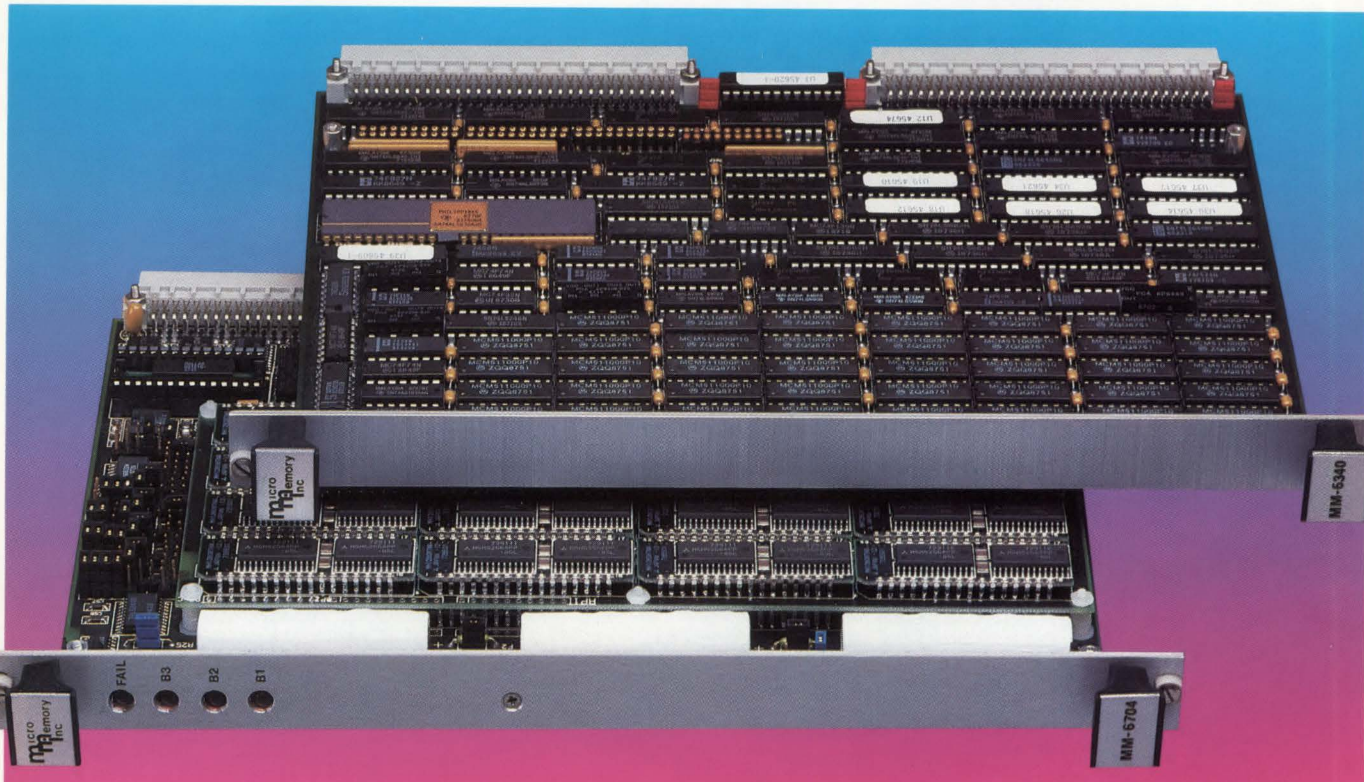

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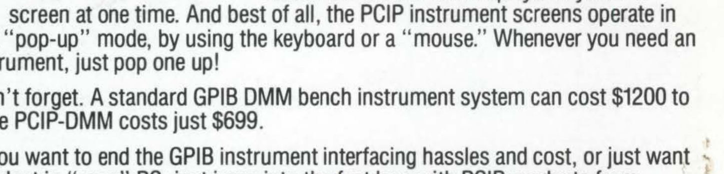

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