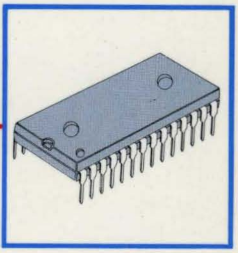
SAMSUNG

Data Book

MPR

(Microprocessor Peripheral)

1989



SAMSUNG
DATA BOOK LIST

I. Semiconductor Product Guide

II. Transistor Data Book

Vol. 1: Small Signal TR

Vol. 2: Bipolar Power TR

Vol. 3: TR Pellet

III. Linear IC Data Book

Vol. 1: Audio/Video

Vol. 2: Telecom/Industrial

Vol. 3: Data Converter IC

IV. MOS Product Data Book

V. High Performance CMOS Logic Data Book

VI. MOS Memory Data Book

VII. SFET Data Book

VIII. MPR Data Book

IX. CPL Data Book

X. Dot Matrix Data Book

MICROPROCESSOR PERIPHERAL

Data Book

CONTENTS

Chapter 1: Product Guide

Overview 13

Samsung's Total System Solution 14

Alpha Numeric Index 15

Cross Reference Guide 16

Chapter 2: Quality/Reliability 17

Chapter 3: Data Sheets

KS53C80 41

KS68C45S 68

KS82C37A 89

KS82C50A 111

KS82C52 136

KS82C54 152

KS82C55A 167

KS82C59A 185

KS82C84A 211

KS82C88 220

KS82C284 229

KS82C288 240

KS82C289 260

KS84C21/C22 280

KS84C31/C32 309

KS85C30 348

Chapter 4: Sales Offices 377

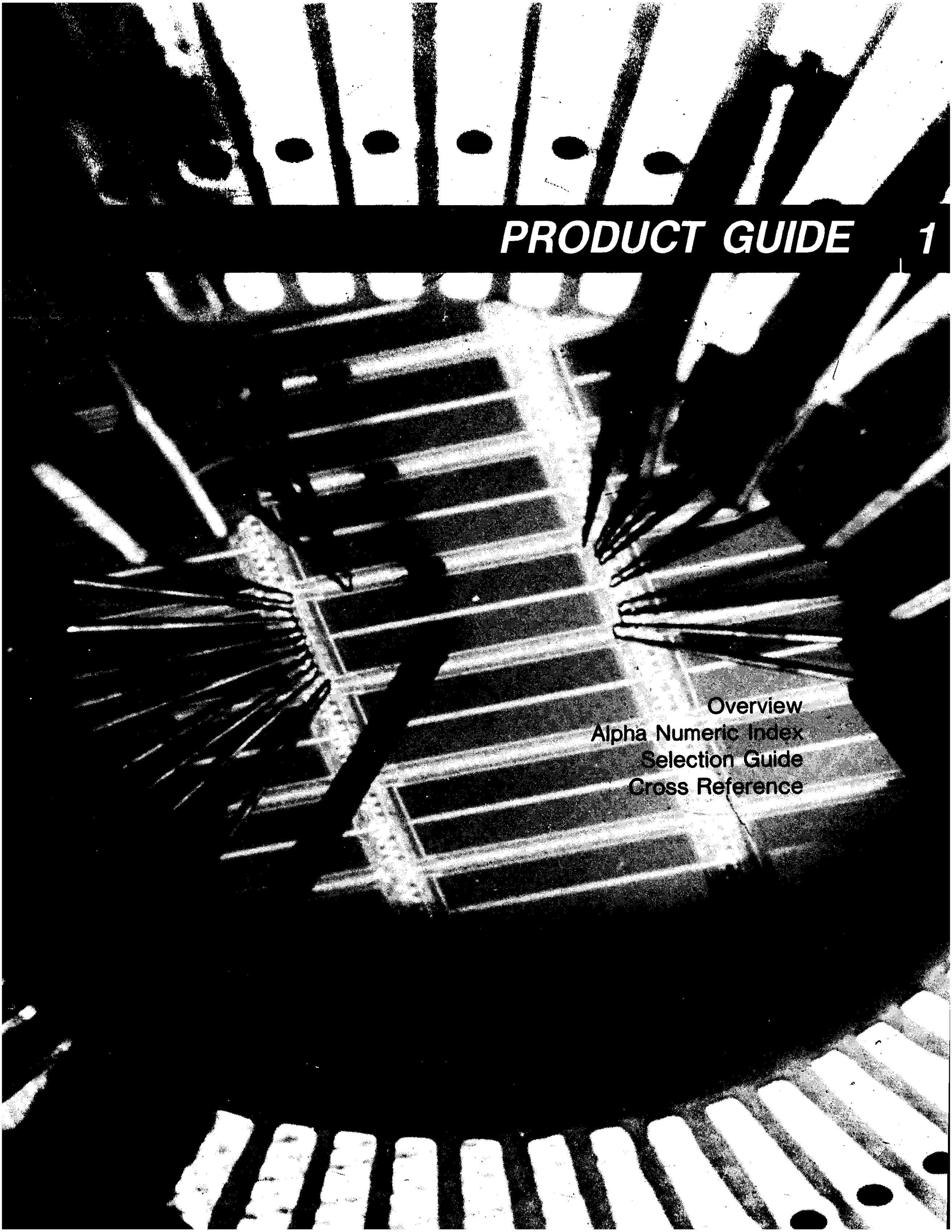
1

2

3

4

PRODUCT GUIDE 1



Overview
Alpha Numeric Index
Selection Guide
Cross Reference

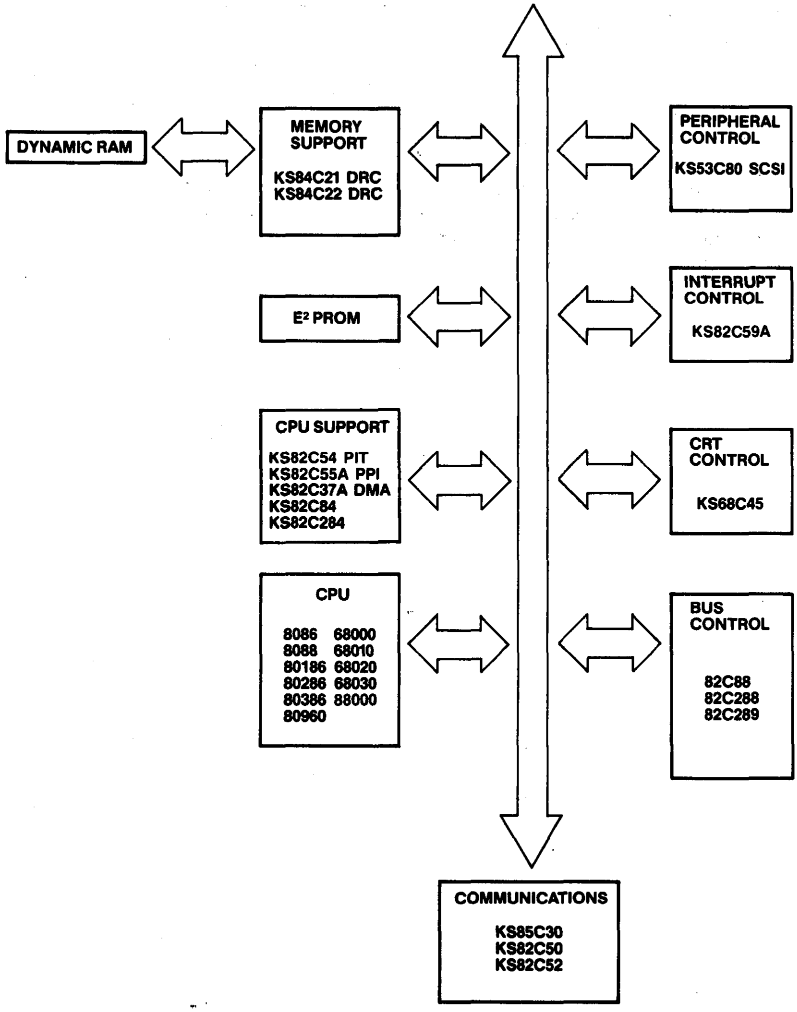
OVERVIEW

Samsung microprocessor peripherals provide a complete solution to increasing complex and performance-oriented applications environment. Standard functions in high performance CMOS technology reduce designers time-to-market by shortening design, testing and debug activities.

At Samsungs world class manufacturing facilities in Korea and San Jose, product reliability and failure rates are carefully monitored. This emphasis on manufacturing products of the highest quality and reliability translates into higher system reliability, reduced down time and reduced repair costs.

Our advanced CMOS technology, CSP II, provides performance levels to match today's high speed microprocessors. CSP II features dual-layer metal, singler-layer poly, and features sizes down to 2μ drawn. This 13 mask process results in cost-effective manufacturing to produce high performance CMOS building blocks at competitive prices. Figure 1 summarizes microprocessor support from Samsung peripheral products.

SAMSUNG'S TOTAL SYSTEM SOLUTION



ALPHA NUMERIC INDEX

DEVICE	FUNCTION	PAGE
KS82C37A	DMA Controller	89
KS82C52	Serial Controller Interface	136
KS82C50A	Asynchronous Communications Controller	111
KS82C54	Interval Timer	152
KS82C55A	Programmable Peripheral Interface	167
KS82C59A	Interrupt Controller	185
KS82C84A	Clock Generator	211
KS82C88	Bus Controller	220
KS53C80	SCSI Bus Controller	41
KS84C21/22	1M/4M DRAM Controller (Mask Programmable)	280
KS84C31/32	Enhanced Dynamic RAM Controllers	309
KS85C30	Serial Communication Controller	348
KS82C284	80286 Clock Generator	229
KS82C288	80286 Bus Controller	240
KS82C289	80286 Bus Arbiter	260
KS68C45S	CRT Controller	68

CROSS REFERENCE GUIDE

AMD	SAMSUNG
AM5380	KS53C80
D8237A D8237A-4 D8237A-5	KS82C37A-5 KS82C37A-5 KS82C37A-5
D82C54-8 D82C54-10	KS82C54A-8 KS82C54A-10
D8255A-2 D8255A-3	KS82C55A-5 KS82C55A-5
D8259A-5 D8259A-8	KS82C59A-8 KS82C59A-8
D8284A-8 D8284A-10	KS82C84A-8 KS82C84A-10
KS82C88-5	D8288-5

HARRIS	SAMSUNG
82C37A-5 82C37A-8	KS82C37A-5 KS82C37A-8
82C52	KS82C52
82C54-8	KS82C54-8
82C55A-5 82C55A-8	KS82C55A-5 KS82C55A-8
82C59A-5 82C59A-8	KS82C55A-8 KS82C55A-8
82C84A-8	KS82C54A-8
82C88-5 82C88-8	KS82C54A-5 KS82C54A-8

INTEL	SAMSUNG
82C37A 82C37A-4 82C37A-5	KS82C37A-5 KS82C37A-5 KS82C37A-5
8255A 8255A-5	KS82C55A-5 KS82C55A-5
82C54A	KS82C54-8
82C55A-8 82C55A-8	KS82C55A-8 KS82C55A-8
82C59A 82C59A-2 82C59A-8	KS82C59A-8 KS82C59A-8 KS82C59A-8
82C84 82C84A 82C84A-1	KS82C84A-5 KS82C84A-8 KS82C84A-10
82C88 8288	KS82C88-8 KS82C88-8

LOGIC DEVICES	SAMSUNG
L5380 L53C80	KS53C80 KS53C80

MITSUBISHI	SAMSUNG
82C37A-4 82C37A-5	KS82C37A-5 KS82C37A-5
82C54-6 82C54-8	KS82C54-8 KS82C54-8
82C55A-5 82C55A-8	KS82C55A-5 KS82C55A-8
82C59A-5 82C59A-8	KS82C59A-8 KS82C59A-8

NATIONAL	SAMSUNG
DP84C21	KS84C21
DP84C22	KS84C22

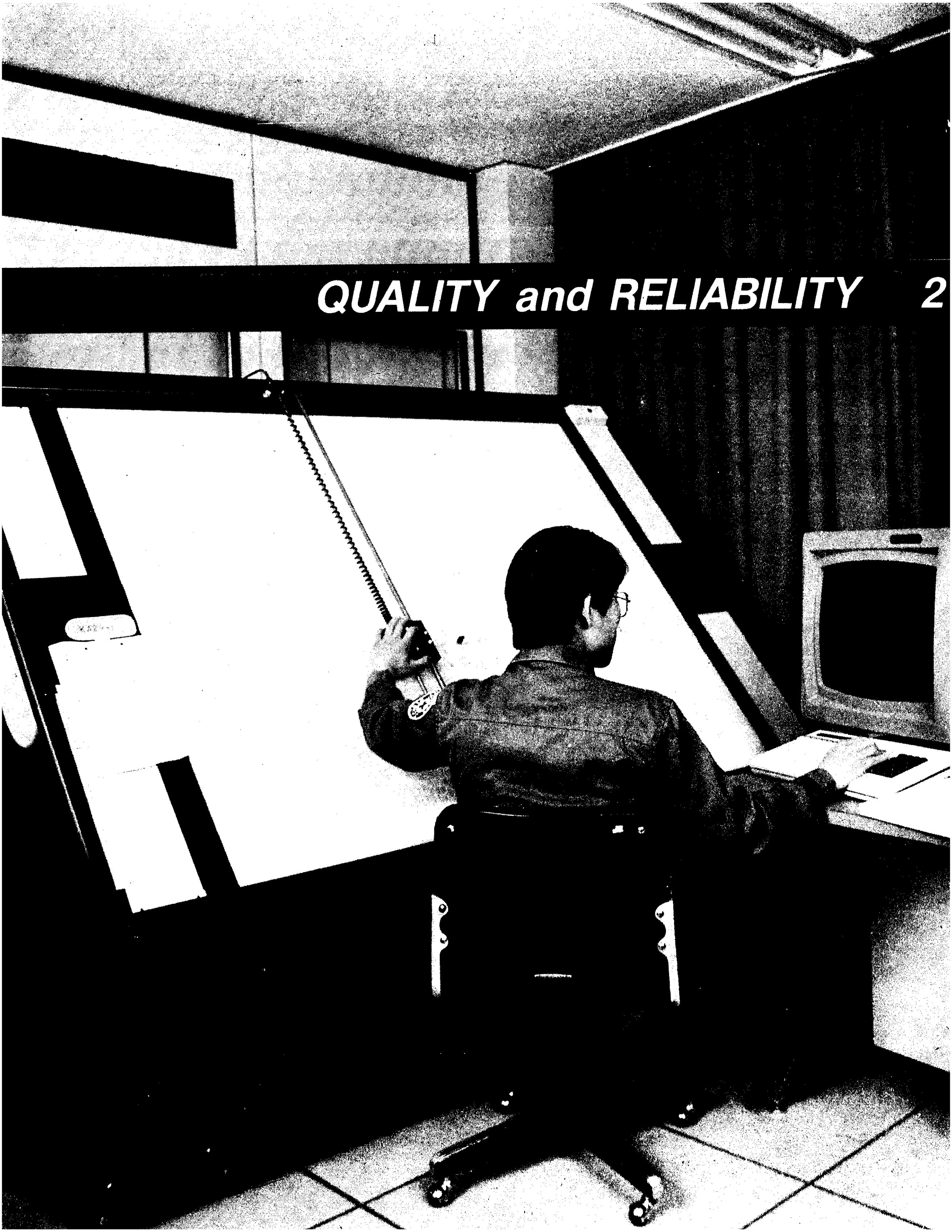
NCR	SAMSUNG
5380	KS53C80

NEC	SAMSUNG
82C37A-5	KS82C37A-5
82C54-8	KS82C54-8
82C55A-8	KS82C55A-8
82C59A-8	KS82C59A-8
82C84A-8	KS82C84A-8
82C88-8	KS82C88-8

OKI	SAMSUNG
M82C37A-5	KS82C37A-5
M82C54-8 M82C54-10	KS82C54A-8 KS82C54A-10
M82C55A-8	KS82C55A-8
M82C59A-5 M82C59A-8	KS82C59A-8 KS82C59A-8
M82C84A-5 M82C84A-8	KS82C84A-5 KS82C84A-8
M82C88-5 M82C88-8	KS82C88-5 KS82C88-8

UMC	SAMSUNG
UM8237A-3 UM8237A-4 UM8237A-5	KS8237A-5 KS82C37A-5 KS82C37A-5
UM8250A UM8250B	KS82C50 KS82C50
UM8254-2	KS82C54A-8
UM8255A	KS82C55A-5
UM8259A-5	KS82C59A-8
UM82C84AE-8 UM82C84AE-10	KS82C84A-8 KS82C84A-10
UM82C88-5	KS82C88-5

QUALITY and RELIABILITY 2



INTRODUCTION

Samsung's Microprocessor Peripheral products are among the most reliable in the industry. Extensive qualification, monitor, and outgoing product programs are used to scrutinize all areas of product quality and reliability. Additionally, stringent controls and subsequent supporting documentation are applied to every wafer fabrication and assembly lot.

RELIABILITY THEORY

This section is chiefly concerned with reliability. However, quality will be mentioned briefly, as reliability and quality are strongly interrelated.

The first concern of a customer is with the quality of incoming product. For this reason, Samsung utilizes tight outgoing quality procedures to assure all customers receive quality products. Details are outlined in another section. Additionally, lot-by-lot stressing, regular reliability monitors, exhaustive product qualification testing, and rigorous in-line process controls (details in another section) are all utilized to guarantee Samsung products are of the highest grade. Quality is Samsung's number one priority.

QUALITY AND RELIABILITY PROGRAM

Three topics of prime concern regarding Samsung's quality programs are detailed below:

A. Qualification Program

B. Monitor Program

C. Outgoing Quality Program

Qualification Program

In order for the Microprocessor Peripheral family to be qualified for mass production purposes, extensive reliability information has been compiled. The purpose was to simulate all relevant user conditions, via accelerated and standard methods, prior to customer shipments. In this way, the processing and design of VLSI devices are "wrung-out", and reliability strongly established, to ensure all product is of the highest quality.

The stresses used for qualification are detailed in another section (Reliability Test Results). Very stringent LTPD levels were applied to the various tests to guarantee a product quality level in the upper tier of the Microprocessor Peripheral market.

Monitor Program

Frequently devices duplicate their qualification tests to give long-term reliability data on CSPII technology. In this way historical data is collected and analyzed over all part types and thus assures the customer of ongoing device quality. Not only is the product therefore verified at its initial stages, but trends are noted to track continual process stability. These results are summarized in reliability reports issued periodically by Samsung Semiconductor.

Outgoing Quality Program

All wafer lots are required to pass a "QC-Reliability-Gate" prior to product shipment. The purpose is to track "lot-by-lot" quality and reliability to catch any potential product anomally at the factory site.

The customer can then expect only quality material to be delivered from Samsung. Any lot that fails the procedure listed below is heavily scrutinized, to make sure that corrective action takes place immediately.

By paying such close attention to every lot, product costs are kept at a minimum. Samsung's customer return rate is extremely low, which is where our tough outgoing policy is most powerful. Such a tight clamp to protect our customers is how we can assure that all Samsung's products are released with the highest confidence level possible.

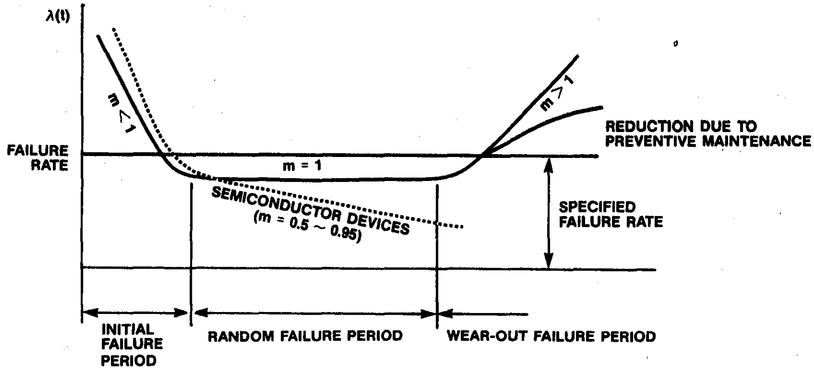
RELIABILITY AND PREDICTOR THEORY

Reliability

Reliability can be loosely characterized as long-term product quality.

There are two types of reliability tests: those performed during design and development, and those carried out in production. The first type is usually performed on a small sample, but for long periods or under very accelerated conditions to investigate wearout failures and to determine tolerances and limits in the design process. The second type of tests is performed periodically during production to check, maintain, and improve the assured quality and reliability levels. All reliability tests performed by Samsung are under conditions more severe than those encountered in the field, and although accelerated, are chosen to simulate stresses that devices will be subjected to in actual operation. Care is taken to ensure that the failure modes and mechanisms are unchanged.

Figure 1: Failure Rate Curve ("Bath Tub Curve")

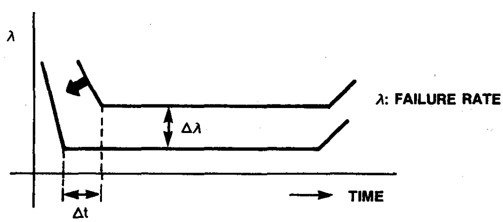


Fundamentals

A semiconductor device is very dependent on its conditions of use (*e.g., junction temperature, ambient temperature, voltage, current, etc.*). Therefore, to predict failure rates, accelerated reliability testing is generally used. In accelerated testing, special stress conditions are considered as parametrically related to actual failure modes. Actual operating life time is predicted using this method. Through accelerated stresses, component failure rates are ascertained in terms of how many devices (in percent) are expected to fail for every 1000 hours of operation. A failure rate versus time of activity graph is shown below (the so-called "bath tub curve").

During the initial time period, products are affected by "infant mortality", intrinsic to all semiconductor technologies. End users are very sensitive to this parameter, which causes early assembly/operation failures of their system. Periodically Samsung reviews and publishes life time results. The goal is a steady shift of the limits as shown below.

Figure 2: Failure Rate

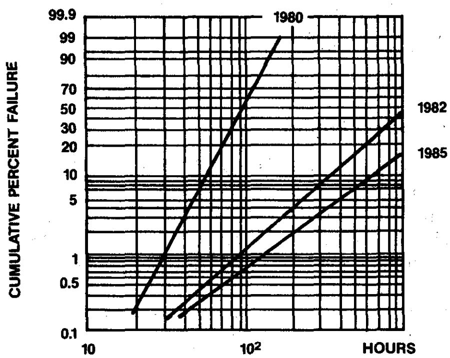


Accelerated Humidity Tests

To evaluate the reliability of products assembled in plastic packages. Samsung performs accelerated humidity stressing, such as the Pressure Cooker Test (PCT) and Wet High Temperature Life Test (WHOPL).

Figure 4 shows some results obtained with these tests, which illustrate the improvements in recent years. These improvements result mainly from the introduction of purer molding resins, new process methods, and improved cleanliness.

Figure 3: Improvement in Humidity Tests

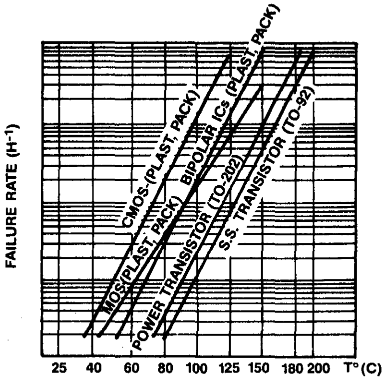


Accelerated Temperature Tests

Accelerated temperature tests are carried out at temperature in a range from 75° C to 200° C for up to 1000 hours. These tests allow Samsung to evaluate reliability rapidly and economically, as failure rates are strongly dependent on temperature.

The validity of these tests is demonstrated by the good correlation between data collected in the field and laboratory results obtained using the Arrhenius model. Figure 5 shows the relationship between failure rates and temperatures obtained with this model.

Figure 4: Failure Rate versus Temperature



FUNDAMENTAL THEORY FOR ACCELERATED TESTING

The accelerated life test is powerful because of its strong relation to failure physics. The Arrhenius model, which is generally used, is explained below.

1. Arrhenius Model

This model can be applied to accelerated Operating Life Tests and uses absolute (Kelvin) temperatures.

$L = A + Ea/K \cdot Tj$

L : Lifetime
A : Constant
Ea : Activation Energy
Tj : Absolute Junction temperature
K : Boltzman's constant

If life L1 and L2 correspond to T1, T2:

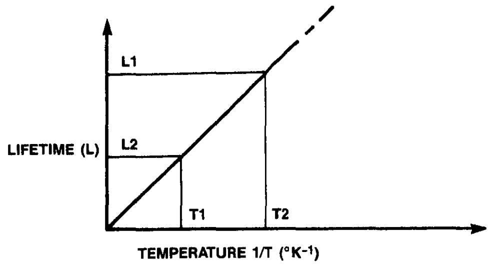
$$L1 = L2 \exp\left\{\frac{Ea}{K}\left(\frac{1}{T1} - \frac{1}{T2}\right)\right\}$$

The actual junction temperature should be used and can be computed using the following relationship:

$T_j = T_a + (P \times \theta ja)$

Where Tj = Junction Temperature
Ta = Ambient Temperature
P = Actual Power Consumption
θja = Junction to Ambient Thermal Resistance (typically 100°C/W for a 16-pin PDIP).

Figure 5: Operating Life Test



2. Activation Energy Estimate

Clearly the choice of an appropriate activation energy, Ea, is of paramount importance. The different mechanisms which could lead to circuit failure are characterized by specific activation energies whose values are published in the literature. The Arrhenius equation describes the rate of many processes responsible for the degradation and failure of electronic components. It follows that the transition of an item from an initially stable condition to a defined degraded state occurs by a thermally activated mechanism. The time for this transition is given by an equation of the form:

MTBF = B EXP (Ea/KT)
MTBF = Mean time between failures

The acceleration effect for a 125° C device junction test with respect to 70° C actual device junction operation is equal to 1000 for Ea = 1eV and 7 for Ea = 0.3eV.

Some words of caution are needed about published values of Ea:

A. They are often related to high-temp tests where a single Ea (with high value) mechanisms has become dominant.

B. They are specifically related to the devices produced by that supplier (and to its technology) for a given period of time.

C. They could be modified by the mutual action of other stresses (voltage, mechanical, etc.)

D. Field device-application conditions should be considered.

(Activation energy for each failure mode)

Failure Mechanism	Ea
Contamination	1 ~ 1.4 eV
Polarization	1 eV
Aluminum Migration	0.5 ~ 1 eV
Trapping	1 eV
Oxide Breakdown	0.3 eV
Silicon Defects	0.3 ~ 0.5 eV

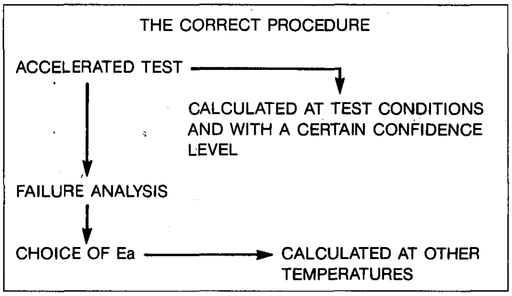
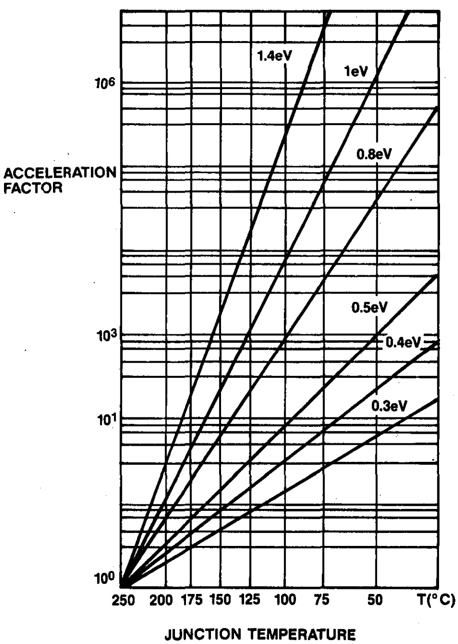


Figure 6: Life Hours



Failure Rate Predication

Accelerated testing projects the failure rate of products. By derating the data at different conditions, the life expectancy at actual operating conditions can be predicted. In its simplest form the failure rate (at a given temperature) is:

$$FR = \frac{N}{DH}$$

Where FR = Failure Rate
N = Number of failures
D = Number of components
H = Number of testing hours

If we intend to determine the FR at different temperatures, an acceleration factor must be considered. Some failure modes are accelerated via temperature stressing based upon the accelerations of the Arrhenius Law.

For two different temperatures:

$$FR\ (T1) = FR\ (T2)\ \exp\left\{\frac{Ea}{K}\left(\frac{1}{T1} - \frac{1}{T2}\right)\right\}$$

FR (T1) is a point estimate, but to evaluate this data for an interval estimate, we generally use X^2 (chi square) distribution. An example follows:

Failure Rate Evaluation

Unit: %/1000HR

Dev.×Hours at 125°C	Fail	Failure Rate at 60% Confidence Level			
1.7×10^6	2	Point Estimate	85°C	70°C	55°C
		0.18	0.0068	0.0018	0.00036

The activation energy, from analysis, was chosen as 1.0 eV based upon test results. The failure rate at the lower operating temperature can be extrapolated by an Arrhenius plot.

RELIABILITY TESTS

Samsung has established a comprehensive reliability program to monitor and ensure the ongoing reliability of the Microprocessor Peripheral family. This program involves not only reliability data collection and analysis on existing parts, but also rigorous in-line quality controls for all products.

Listed below are details of tests performed to ensure that manufactured product continues to meet Samsung's stringent quality standards. In-line quality controls are reviewed extensively in later sections.

The tests run by the Quality Department are accelerated tests, serving to model "real world" applications through boosted temperatures, voltages, and/or humidities. Accelerated conditions are used to derive device knowledge through means quicker than that of typical application situations. These accelerated conditions are then used to assess differing failure rate mechanisms that correlate directly with ambient conditions.

Following are summaries of various stresses (and their conditions) run by Samsung on Microprocessor Peripheral devices.

High Temperature Operating Life (V_{CC} = 7V, 125°C, Dynamic)

The high temperature operating life test is used to accelerate failure mechanisms by operating the devices at an elevated temperature. The data obtained by this life test is translated to device temperatures using the Arrhenius relationship; exp (-Ea/kT), where Ea is the activation energy, k is Bolzmann's constant, and T is the absolute temperature for the failure calculation. The important step in predicting the failure rate is to determine the failure mechanism and the corresponding failure activation energy.

Wet High Temperature Operating Life (V_{CC} = 5.5V, 85°C, 85% R.H., Static)

Wet high temperature operating life test is used to accelerate failure mechanisms by applying static bias on alternate pins at high temperature and humidity ambient (85°C/85% R.H.). This test checks for resistance to moisture penetration by using an electrolytic principle to accelerate corrosive mechanisms.

Pressure Cooker Test (Unbiased, 121°C, 15 PSIG, 100% R.H.)

The Pressure Cooker Test checks for resistance to moisture penetration. A highly pressurized vessel is used to force water (thereby promoting corrosion) into packaged devices located within the vessel.

High Temperature Storage (Unbiased, 150°C)

High Temperature Storage is utilized to test for both package and die weaknesses. For example, sensitivities to ionic contamination and bond integrity are closely scrutinized.

Temperature Cycling (Unbiased, -65°C to +150°C, air)

This stress uses a chamber with alternating temperatures of -65°C and +150°C (air ambient) to thermally cycle devices within it. No bias is applied. The cycling checks for mechanical integrity of the packaged device, in particular bond wires and die attach, along with metal/polysilcon microcracks.

Thermal Shock (Unbiased, -65°C to +150°C, liquid)

This stress uses a chamber with alternating temperatures of -65°C to +150°C (liquid ambient) to thermally cycle devices within it. No bias is applied. The cycling is very rapid, and primarily checks for die/package compatibility.

Wet High Temperature Storage (60°C, 90% R.H.)

Used to evaluate the moisture resistance of plastic-encapsulated components. This test independently and collectively looks at molding compounds, lead frames, and passivation, which are all connected via humidity resistances.

Electrostatic Damage Test (ESD) (1.5KΩ, 100pF, 5 stresses per voltage polarity, 100V increments)

ESD stressing tests the integrity of the input protection circuitry to withstand high voltage spikes. High values will ensure adequate resistance to handling, handlers, and other noisy environments where static voltage discharges commonly occur.

PROCESS CONTROL

General Process Control

The general purpose flow in Samsung is shown in Figure 9. This illustration contains the standard process flow from incoming parts and materials to customer shipment.

Wafer Fabrication

Process Controls

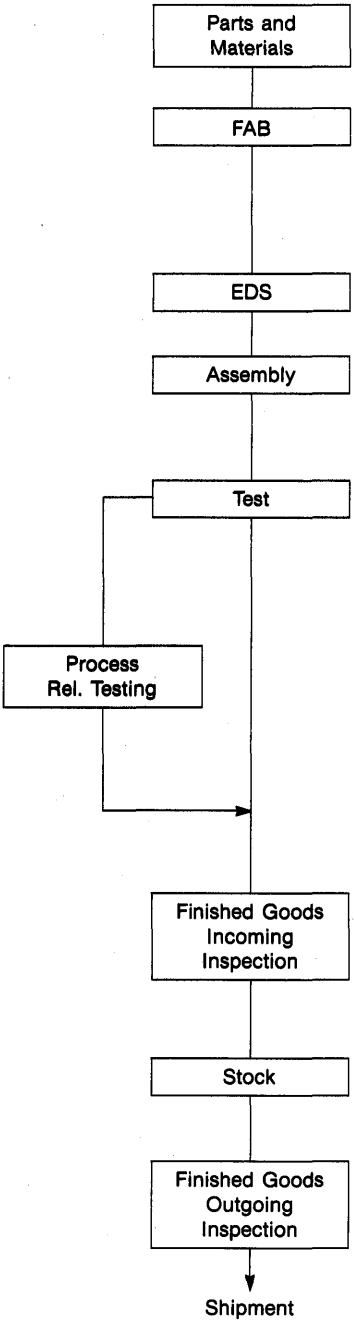
The Quality Control program utilizes the following methods of control to achieve its previously stated objectives: process audits, environmental monitors, process monitors, lot acceptance inspections, and process integrity audits.

Definitions

The essential method of the Quality Control Program is defined as follows:

1. Process audit-Performed on all operations critical to product quality and reliability.
2. Environmental monitor-Monitors concerning the process environment; i.e., water purity, temperature, humidity, particle counts.
3. Process monitor-Periodic inspection at designated process steps for verification of manufacturing inspection and maintenance of process average. These inspections provide both attribute and variable data.
4. Lot acceptance-Lot-by-lot sampling. This sampling method is reserved for those operations deemed as critical and require special attention.

Figure 7: General Process Flow Chart



Acceptance inspection (according to acceptance inspection plan)

Process quality control
- Check of each condition by process quality control procedures
- Process inspection
- Lot control
- Equipment calibration and maintenance

100% Electrical Die Sorting

Process Quality Control and screening of infant mortality defects
- Thermal screen
- Mechanical screen
- Burn-in screen

100% package sorting of electrical characteristics and marking

Reliability monitoring
1. PRT (Process Reliability Testing)
2. DRT (Device Reliability Testing)

- High Temperature Reverse Bias
- High Temperature Gate Bias
- Environmental Test
- Life Test

Sampling Inspection
- Dimensions
- Visual
- Electrical characteristics
- Periodic calibration of measuring equipment

Stock control
- Age control

Sampling Inspection (when applicable)

Environmental Monitor

Process	Control Item	Spec. Limit	Insp. Frequency
Clean Room	• Temperature • Humidity • Particle • Air Velocity	• Individual Spec. • Individual Spec. • Individual Spec. • Individual Spec.	24 Hrs. 24 Hrs. 24 Hrs. 24 Hrs.
D.I. Water	• Particle • Bacteria • Resistivity	• 5 ea/50ml (0.8μ) • 50 colonies/100ml (0.45μ) • Main (Line): More than 15 Mohm-cm • Using point: More than 14 Mohm-cm	24 Hrs. Weekly 24 Hrs. 24 Hrs.

* Instruments
  - FMS (Facility Monitoring System) HIAC/ROYCO
  - CPM (Central Particle Monitoring System-Dan Scientific)
  - Liquid Dust Counter Etch Rate
  - Filtration System for Bacterial check
  - Air Particle counter
  - Air Velocity meter

Process Monitor

Process	Control Item	Spec. Limit	Insp. Frequency
Photo	• Aligner N_2 Flow Rate • Aligner Vacuum • Aligner Air • Aligner Pressure • Aligner Intensity • Coater Soft Bake Temperature Vacuum	• Individual Spec. • Individual Spec. • Individual Spec. • Individual Spec. • Individual Spec. • Individual Spec. • Individual Spec. • Individual Spec.	Once/Shift Once/Shift Once/Shift Once/Shift Once/Shift Once/Shift Once/Shift Once/Shift
Etch	• Etchant Temp. • Etch Rate • Spin Dryer N_2 Flow RPM • Hard Bake Temp. N_2 Flow	• Individual Spec. • Individual Spec. • Individual Spec. • Individual Spec. • Individual Spec. • Individual Spec.	Once/Shift Once/Shift Once/Shift Once/Shift Once/Shift Once/Shift
Thin Film	• Cooling Water Temp. • Thickness	• 26 ± 3°C • Individual Spec.	Once/Shift Once/Shift
CVD	• Pin Hole • Thickness	• Individual Spec. • Individual Spec.	Once/Shift Once/Shift
Diffusion	• Tube Temp. • C-V Plot Run Tube • Sheet Resistance • Thickness	• Individual Spec. • Individual Spec. • Individual Spec. • Individual Spec. • Individual Spec.	Once/Shift Once/Shift Once/10 days Once/Shift Once/Shift

Raw Material Incoming Inspection

1. Mask Inspection

Defect Detection	• Pinhole & Clear-extension • Opaque Projection & Spots • Scratch/Particle/Stain • Substrate Crack/Glass-chip • Others	All Masks	• Defect Size ≤ 1.5μm • Defect Density ≤ 0.124EA/cm^2
Registration	• Run-out (X-Y Coordinate) • Orthogonality • Drop-in Accuracy • Die Fit/Rotation	20% • All New Masks	±0.75μm ±0.75μm ±0.50μm ±0.50μm
Critical Dimension	• Critical Dimension	All Masks	Purchasing Spec.

* Instrument
- Auto mask inspection system for defect-detection (NJS 5MD-44)
- Comparator for registration (MVG 7X7)
- Automatic linewidth measuring system for CD (MPV-CD)

2. Wafer Inspection

Purpose	Insp. Items	Sample	Remarks
Structural	• Crystallographic Defect	All Lots	• Sirtl Etch
Electrical	• Resistivity • Conductivity	All Lots	• Monitor Water
Dimensional	• Thickness • Diameter • Orientation • Flatness	All Lots	TTV, NTV, Epi-thickness
Visual	• Surface Quality • Cleanliness	All Lots	Purchasing Spec.

* Instrument
- 4 point probe for resistivity (Kokusai VR-40A, Tencor sonogage, ASM AFPP)
- Flatness measuring system (Siltec)
- Epi. layer thickness gauge (Digilab FTG-12, Qualimatic S-100)
- Automatic Surface Insp. System (Aeronca Wis-150)
- Non-contact thickness gauge (ADE6034)

In-Process Quality Inspection (FAB)

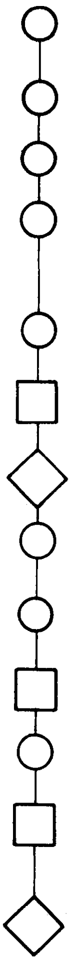
Manufacturing Section

Process Step	Process Control Insp.	Frequency
Oxidation	Oxide Thickness	All Lots
Diffusion	Oxide Thickness Sheet Resistance Visual	All Lots All Lots All Lots
Photo	Critical Dimension Visual Mask Clean Inspection	All Lots (MOS) All Lots All Masks with Spot Light (MOS) or Microscope (BIP)
Etch	Critical Dimension Visual	All Lots All Wafers
Thin Film	Metal Thickness Visual	All Lots All Lots
I_{ON} Implant	Sheet Resistance	All Lots (Test Wafer)
Low Temp. Oxide	Thickness	All Lots
	Visual	All Lots
E-Test	Electrical Characteristics	All Lots
Fab. Out	Visual	All Wafers

2. FAB, QC Monitor/Gate

Process Step	FAB, QC Insp.	Frequency
Oxidation	Oxide Thickness C-V Test on Tubes Visual	Once/Shift Once/10 Days and After CLN. Once/Shift
Diffusion	Oxide Thickness C-V Test on Tubes Visual	Once/Shift Once/10 Days and After CLN. Once/Shift
Photo	Critical Dimension Visual Mask CLN Inspection	All Lots (MOS) Once/Shift All Masks After 10 Times Use
Etch	Critical Dimension Visual	All Lots (MOS) All Lots
Thin Film	C-V Test on Tubes on Lots Reflectivity	Once/10 Days and After CLN. Once/Shift Once/Shift
Low Temp. Oxide	Refractive Index, Wt% of Phosphorus Visual	1 Test Wafer/Lot 1 Test Wafer/Lot 1 Test Wafer/Lot
E-Test	Measuring Data	All Lots
Calibration	Instrument for Thickness and C.D. Measuring	Once/week

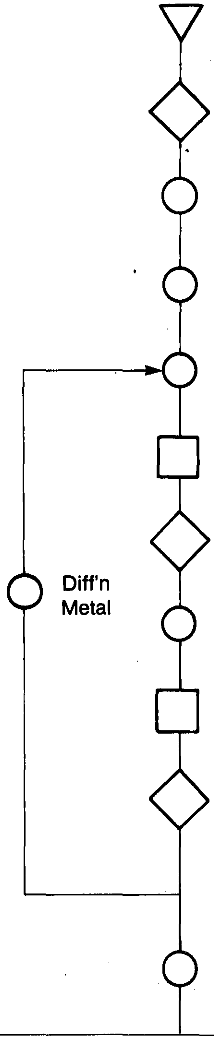
3. Photo/Etch process quality control

Process Flow	Process Step	MFG. Control Item	QC Monitor/Gate
	Prebake	Oven PM, Temperature Time	Oven-Particle Temp N_2 Flow Rate
	Photo Resist (PR) —spin	Thickness Machine PM	
	Soft Bake	Oven PM, Temperature Time	Temp. N_2 Flow Rate
	Align/Expose	Light Uniformity Alignment, Focus Test Mask Clean Inspection Mask Clean Exposure Light Intensity	Light Intensity Mask Clean Insp.
	Develop	Equipment PM Solution Control	Vacuum
	Develop Check	PRC.D.'S Alignment Particles Mask and Resist Defects	
	QC Inspection		Critical Dimension
	Hard Bake	Oven PM, Temperature Time	Temp. N_2 Flow Rate
	Etch	Etch rate, Equipment PM & Settings, Etch Time to Clear	Etchant Temp. Etch Rate
	Inspection	Over/Under	
	PR Strip	Machine-PM	
	Final Check	C.D.'S Over and under Etch, Particles, PR Residue, Defects, Scratches	
	QC Inspection		Same as Final Check. However, more intense on limited sample basis. (AQL 6.5%)

4. Reliability-related Interlayer Dielectric, Metallization, and Passivation Process Quality Control Monitor

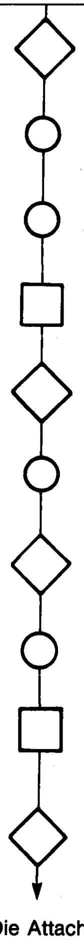
Item	Frequency
Wt% Phosphorus Content of the Dielectric Glass	1/Shift
Metallization Interconnect	1/Month
Al Step Coverage	1/Month
Metallization Reflectivity	1/Shift
Passivation Thickness and Composition	1/Shift
Thin Film Defect Density	1/Shift

Figure 8: General Wafer Fabrication Flow



Process Flow	Process Step	Major Control Item
	Wafer and Mask Input	
	Starting Material Incoming Inspection	Mask: (See mask Inspection) Wafer: (See wafer Inspection)
	Wafer Sorting and Labelling	Resistivity
	Initial Oxidation	Oxide Thickness
	Photo	• (See manufacturing section) • (See FAB, QC Monitor/gate)
	Inspection	• Critical Dimension • Visual/Mech — Major: AQL 1.0% — Minor: AQL 6.5%
	QC Gate	• Critical Dimension
	Etch	• (See manufacturing section) • (See FAB, QC Monitor/gate)
	Inspection	• Critical Dimension • Visual/Mech — Major: AQL 1.0% — Minor: AQL 6.5%
	QC Gate	• Critical Dimension • Visual/Mech
	Diffusion Metallization	• (See in-process Quality Inspection)
	E-test	• Electrical Characteristics

Figure 8: General Wafer Fabrication Flow (Continued)



Process Flow	Process Step	Major Control Item
	QC Gate	• Electrical Characteristics
	Back-Lap	• Thickness
	Back Side Evaporation	• Thickness, Time Evaporation Rate
	Final Inspection	• All Wafers Screened (Visual/Mech)
	QC Fab. Final Gate	• Visual/Mech. — Major: AQL 1.0% — Minor: AQL 6.5%
	EDS (Electrical Die Sorting)	
	QC Gate	• Function Monitor
	Sawing	
	Inspection	• Chip Screen
	QC Final Inspection	• AQL 1.0% • Fab. Defect • Test Defect • Sawing Defect

ASSEMBLY

The process control and inspection points of the assembly operation are explained and listed below:

1. Die Inspection:

   Following 100% inspection by manufacturing, in-process Quality Control samples each lot according to internal or customer specifications and standards.

2. Die Attach Inspection:

   Visual inspection of samples is done periodically on a machine/operator basis. Die Attach techniques are monitored and temperatures are verified.

3. Die Shear Strength:

   Following Die Attach, Die Shear Strength testing is performed periodically on a machine/operator basis. Either manual or automatic die attach is used.

4. Wire Bond Inspection:

   Visual inspection of samples is complemented by a wire pull test done periodically during each shift. These checks are also done on a machine/operator basis and XR data is maintained.

5. Pre-Seat/Pre-Encapsulation Inspection:

   Following 100% inspection of each lot, samples are taken on a lot acceptance basis and are inspected according to internal or customer criteria.

6. Seal Inspection:

   Periodic monitoring of the sealing operation checks the critical temperature profile of the sealing oven for both glass and metal seals.

7. Post-Seal Inspection:

   Subsequent to a 100% visual inspection, In-Process Quality Control samples each for conformance to visual criteria.

Sampling Plans

1. Sampling plans are based on an AQL (Acceptable Quality Level) concept and are determined by internal or by customer specifications.
2. Raw Material Incoming Inspection.

Material	Inspection Item	Acceptable Quality Level
Lead Frame	1) Visual Inspection 2) Dimension Inspection 3) Function Test 4) Work Test	LTPD 10%, C = 2 LTPD 20%, C = 0 LTPD 20%, C = 0 LTPD 20%, C = 0
Wafer	1) Visual Inspection	AQL 0.65%
Au/Al Wire	1) Visual Inspection 2) Bond Pull Strength Test 3) Bondability Test 4) Chemical Composition Analysis	n:5, C= 0 n:13, C= 0 Critical Defect: 0.65% Major Defect: 1.0% Minor Defect: 1.5% n:5, C = 0
Molding Compound	1) Visual Inspection 2) Moldability Test 3) Chemical Composition Analysis	n:5, C = 0 Critical Defect: 0.15% Major Defect: 1.0% Minor Defect: 1.5% n:5, C = 0
Packing Tube & Pin	1) Visual Inspection 2) Dimension Inspection 3) Electro-Static Inspection 4) Hardness Test	LTPD 15%, C = 2 LTPD 15% C = 2 n:5, C = 0 n:5, C = 0
Solder	1) Visual Inspection 2) Weight Inspection 3) Chemical Composition Analysis	LTPD 20% C = 0 LTPD 20% C = 0 LTPD 20% C = 0

2. Raw Material Incoming Inspection (continued)

Material	Inspection Item	Acceptable Quality Level
Flux	1) Acidity Test 2) Specific Gravity Test 3) Chemical Composition Analysis	LTPD 20% C = 0 LTPD 20% C = 0 LTPD 20% C = 0
Solder Preform	1) Visual Inspection 2) Work Test 3) Chemical Composition Analysis	AQL 1.0% AQL 1.0% AQL 1.0%
Coating Resin	1) Visual Inspection 2) Work Test 3) Chemical Composition Analysis	AQL 1.0% AQL 1.0% AQL 1.0%
Marking Ink	1) Work Test 2) Mark Permanency Test	Critical Defect: 0.15% Major Defect: 1.0% Minor Defect: 1.5% n:5, C = 0
Chip Carrier	1) Visual Inspection 2) Dimension Inspection 3) Electro-Static Inspection 4) Hardness Test	LTPD 15% C = 2 LTPD 15% C = 0 n:5, C = 0 n:5, C = 0
Vinyl Pack	1) Visual Inspection 2) Work Test 3) Electro-Static Inspection	LTPD 20% C = 0 LTPD 20% C = 0 LTPD 15% C = 0
Ag Epoxy	1) Work Test 2) Chemical Composition Analysis	n:8, C = 0 n:8, C = 0
Letter Marking	1) Visual Inspection 2) Work Test	
Spare Parts & Others	1) Dimension Inspection 2) Visual Inspection	n:5, C = 0 n:5, C = 0

3. In Process Quality Inspection

A. Assembly Lot Acceptance Inspection

(1) Acceptance quality level for wire bond gate inspection

Defect Class	Inspection Level	Type of Defect	
Critical Defect	AQL 0.65%	— Missing Metal — Chip Crack — No Probe — Epoxy on Die — Mixed Device — Wrong Bond — Missing Bond	— Diffusion Defect — Ink Die — Exposed Contact — Bond Short — Die Lift — Broken Wire
Major Defect	AQL 1.0%	— Metal Missing — Metal Adhesion — Pad Metal Discolored — Tilted Die — Die Orientation — Partial Bond	— Oxide Defect — Probe Damage — Metal Corrosion — Incomplete Wetting — Weakened Wire

3. In Process Quality Inspection (continued)

Defect Class	Inspection Level	Type of Defect	
Minor Defect	AQL 1.5%	— Adjacent Die — Passivation Glass — Die Attach Defect — Wire Loop Height — Extra Wire	— Contamination — Ball Size — Wire Clearance — Bond Deformation

(2) Acceptance quality level for Mold/Trim gate inspection

Defect Class	Inspection Level	Kind of Defect	
Critical Defect	AQL 0.15%	— Incomplete Mold — Void, Broken Package — Misalignment	— Deformation — No Plating — Broken Lead
Major Defect	AQL 0.4%	— Ejector Pin Defect — Package Burr — Flash on Lead	— Crack, Lead Burr — Rough Surface — Squashed Lead
Minor Defect	AQL 0.65%	— Lead Contamination — Poor Plating — Package Contamination	— Bent Lead

B. In-process monitor inspection

Inspection Item	Frequency	Reference
• Die Shear Test	Each Lot	MIL-STD-883C, 2019-2
• Bond Strength Test	Each Lot	MIL-STD-883C, 2011-4
• Solderability Test	Weekly	MIL-STD-883C, 2003-3
• Mark Permanency Test	Weekly	MIL-STD-883C, 2015-4
• Lead Integrity Test	Weekly	MIL-STD-883C, 2004-4
• In-Process Monitor Inspection for Product	4 Times/Shift/Each Process	Identify for Each Control Limit
• X-Ray Monitor Inspection for Molding	2 Times/Shift/Mold Press	Identify for Each Control Limit
• Monitor Inspection for Production Equipment	2 Times/Shift/Each Unit of Equipment	Identify for Each Control Limit

4. Outgoing quality inspection plan (LTPD)

Defect Class	Criteria	Kind of Defect
Critical Defect electrical visual	1%	Open, short Wrong configuration, no marking
Major Defect eletrical visual	1.5%	Items which affect reliability most strongly
Minor Defect electrical visual	2%	Items which minimally or do not affect reliability at all (cosmetic, appearance, etc.)

Figure 9: General Assembly Flow

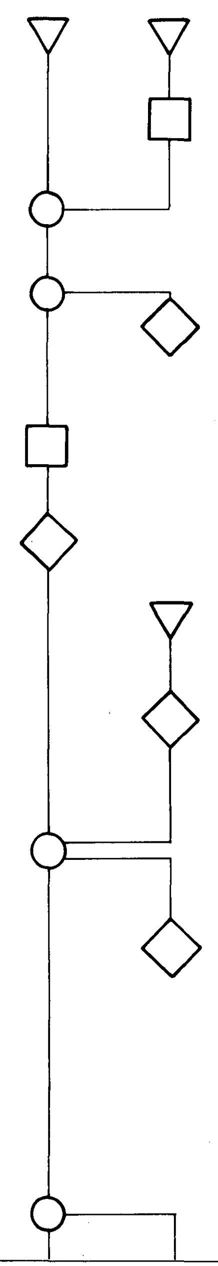
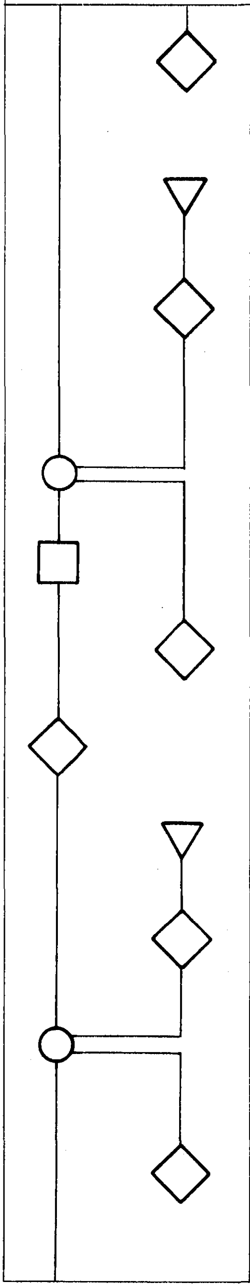
<table>
<tr><th>Process Flow</th><th>Process Step</th><th>Major Control Item</th></tr>
<tr><td rowspan="11"></td><td>Wafer</td><td></td></tr>
<tr><td>Wafer Incoming Inspection</td><td>Q.C. Wafer Incoming Inspection AQL 4.0%</td></tr>
<tr><td>Tape Mount</td><td></td></tr>
<tr><td>Sawing Q.C. Monitor</td><td>Q.C. Monitoring:
— Chip-out
— Crack
— Sawing-speed
— D.I. Purity
— Scratch
— Sawing Discoloration
— Cut Count
— CO_2 Bubble Purity</td></tr>
<tr><td>Visual Inspection</td><td>100% Screen:
— FAB Defect
— EDS Test Defect
— Sawing & Scratch Defect</td></tr>
<tr><td>Q.C. Gate</td><td>1st AQL 1.0%
Reinspection AQL: 0.65%</td></tr>
<tr><td>Lead Frame (L/F)</td><td></td></tr>
<tr><td>Lead Frame Incoming</td><td>* Q.C. L/F Incoming Inspection
Acceptance Quality Level
— Dimension: LTPD 20%, C = 0
— Visual & Mechanical: LTPD 10%, C = 2
— Functional Work Test: LTPD 10%, C = 2</td></tr>
<tr><td>Die Attach (D/A)</td><td></td></tr>
<tr><td>Q.C. Monitor</td><td>* Q.C. D/A Monitor Inspection
1. Bond force
2. Frequency: 4 Times/Station/Shift
3. Sample: 24 ea Time
4. Acceptance Criteria
<table>
<tr><td>Defect</td><td>Acceptance</td><td>Reject</td></tr>
<tr><td>Critical</td><td>0</td><td>1</td></tr>
<tr><td>Major</td><td>1</td><td>2</td></tr>
</table></td></tr>
<tr><td>Cure</td><td></td></tr>
</table>

Figure 9: General Assembly Flow (Continued)



Process Flow	Process Step	Major Control Item
	Q.C. Monitor	* Q.C. Cure Monitor Inspection 1. Control Item — Temperature — In/Out Time 2. Frequency — 1 Time/Shift
	Au Wire	
	Bonding Wire	* Q.C. Au Wire Incoming Inspection 1. Visual Inspection: N = 5, C = 0 2. Bond Pull Test Strength Test: N = 13, C = 0 3. Bond Ability Test — Critical Defect: AQL 0.65% — Major Defect: AQL 1.0% — Minor Defect: AQL 1.5%
	Wire Bonding (W/B)	
	100% Visual Inspection	
	Q.C. Monitor	* Q.C. W/B Monitor Inspection 1. Frequency: 6 Times/Machine/Shift
	Q.C. Gate	1. Q.C. Acceptance Quality Level — Critical Defect: AQL 0.65% — Major Defect: AQL 1.0% — Minor Defect: AQL 1.5%
	Mold Compound	
	Incoming Inspection Mold	* Moldability Test — Critical Defect: AQL 0.15% — Major Defect: AQL 1.0% — Minor Defect: AQL 1.5%
	Mold	
	Q.C. Monitor	* Q.C. Mold Monitor Inspection 1. In-Process Monitor Inspection — Frequency: 4 Times/Station/Shift — Sample: 200 Units/Time 2. Acceptance Quality Level — Critical Defect: AQL 0.25% — Major Defect: AQL 0.4%

2

Figure 9. General Assembly Flow (Continued)

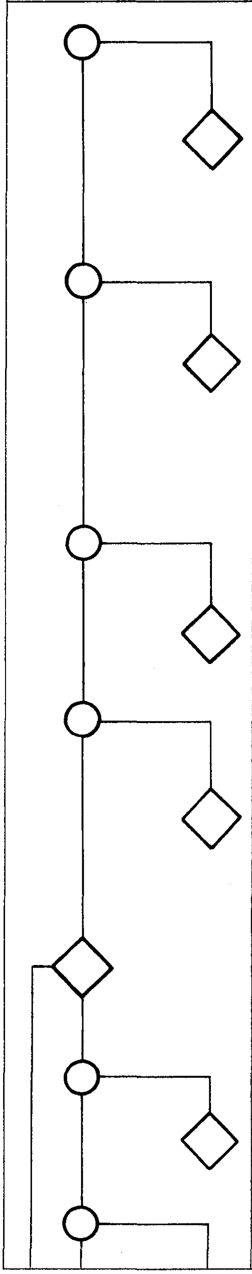
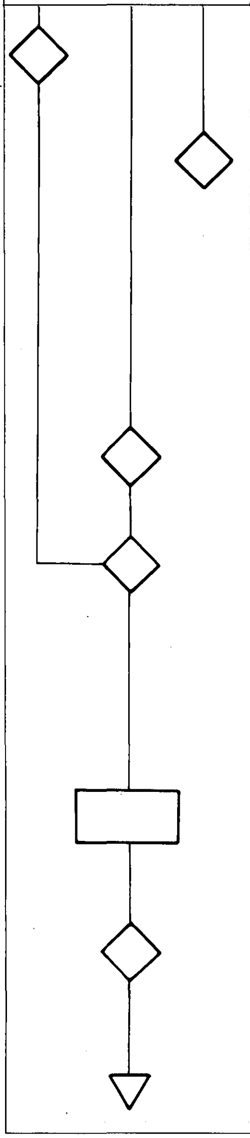
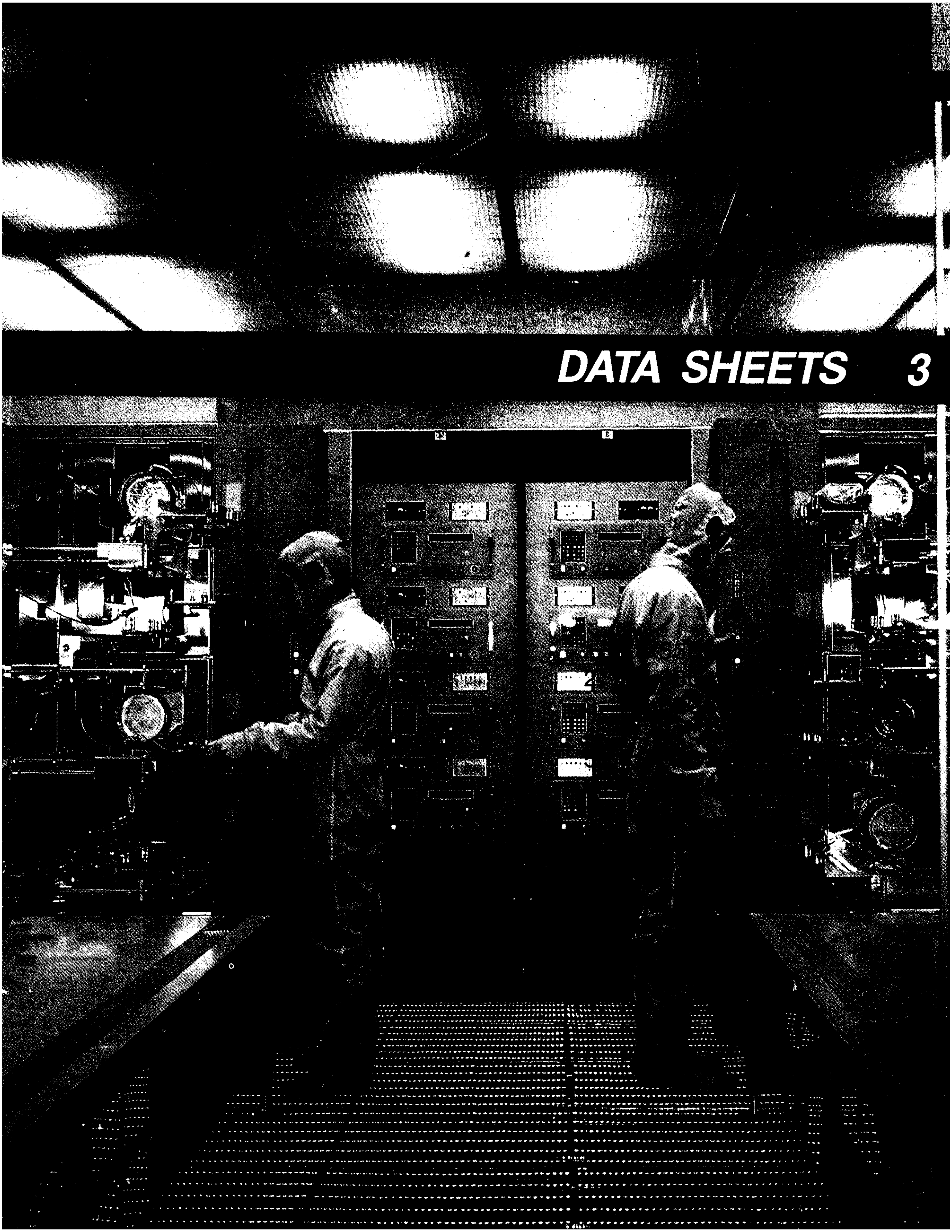
Process Flow	Process Step	Major Control Item
	Cure	
	Q.C. Monitor	*Q.C. Cure Monitor Inspection 1. Control Item — Temperature — In/Out Time 2. Frequency — 1 Time/Shift
	Deflash	
	Q.C. Monitor	*Q.C. Cure Monitor Inspection 1. Control Item — Pressure — Belt Speed — Visual/Mechanical Inspection 2. Frequency: 4 Times/Mach/Shift 3. Identify each Defect Control Limit
	TRIM/BEND	
	Q.C. Monitor	*Q.C. Trim/Bend Monitor Inspection 1. Visual Inspection 2. Frequency: 4 times/Station/Shift
	Solder	100% Visual Inspection
	Q.C. Monitor	*Q.C. Solder Monitor Inspection 1. Frequency: 4 Times/Mach/Shift 2. Criteria — Critical Defect: AQL 0.65% — Major Defect: AQL 1.0%
	Q.C. Gate	*Q.C. Mold Gate — Acceptance Criteria Critical Defect: AQL 0.15% Major Defect: AQL 0.4% Minor Defect: AQL 0.65%
	Test	100% Electrical Test
	Q.C. Monitor	Correlation Sample Reading for Initial Device Test
	Mark	100% Visual Inspection

Figure 9: General Assembly Flow (Continued)

<table>
<tr><th>Process Flow</th><th>Process Step</th><th>Major Control Item</th></tr>
<tr><td rowspan="8"></td><td>PRT Monitoring (Process Reliability Testing)</td><td>1. PRT for Microprocessor Peripheral
— HTRB (48 Hrs) HTGB (48 Hrs)
— other (when applicable)
2. Acceptance Criteria: LTPD 10%</td></tr>
<tr><td>Q.C. Monitor</td><td>* Q.C. Marking Monitor Inspection
— Frequency: 4 Times/Station/Shift
— Sample: 24 Units/Time
— Identify for Each C.L.
— Acceptance Criteria
<table><tr><th>Defect</th><th>Acceptance</th><th>Reject</th></tr><tr><td>Critical</td><td>0</td><td>1</td></tr><tr><td>Major</td><td>1</td><td>2</td></tr></table></td></tr>
<tr><td>Q.C. Gate</td><td>* Q.C. Final Acceptance Level
— Critical Defect: AQL 0.15%
— Major Defect: AQL 0.4%
— Minor Defect: AQL 0.65%</td></tr>
<tr><td>Q.A. Gate</td><td>* Q.A. Incoming Inspection for SFET
1. Critical Defect:
— Electrical Test: LTPD 2% (N = 116, C = 0)
— Visual Test: LTPD 2% (N = 116, C = 0)
2. Major Defect:
— Electrical Test: LTPD 3% (N = 116, C = 1)
— Visual Test: LTPD 3% (N = 116, C = 1)
3. Minor Defect:
— Electrical Test: LTPD 5% (N = 116, C = 2)
— Visual Test: LTPD 5% (N = 116, C = 2)</td></tr>
<tr><td>Stock</td><td>* Age Control</td></tr>
<tr><td>Q.A. Gate</td><td>* Q.A. Outgoing Inspection
1. Quantity
2. Customer
3. Packing
4. Sampling Inspection (when applicable)
— Sampling plan is same as incoming Inspection</td></tr>
<tr><td>Shipment</td><td></td></tr>
</table>

DATA SHEETS 3



PRODUCT INDEX

Device	Function	Page
KS 53C80	Small Computer System Interface	41
KS 68C45S	CRT Controller	68
KS 82C37A	Programmable DMA Controller	89
KS 82C50A	CMOS Asynchronous Communication Element	111
KS 82C52	CMOS Serial Controller Interface (SCC)	136
KS 82C54	Programmable Interval Timer	152
KS 82C55A	Programmable Perlpheral Interface	167
KS 82C59A	Programmable Interrupt Controller	185
KS 82C84A	Clock Generator and Driver	211
KS 82C88	Microprocessor Bus Controller	220
KS 82C284	Clock Generator and Ready Interface for 80286 Microprocessors	229
KS 82C288	Bus Controller for 80286 Microprocessors	240
KS 82C289	Bus Arbiter for 80286 Microprocessors Family	260
KS 84C21/22	Dynamic RAM Controllers	280
KS 84C31/32	Enhanced Dynamic RAM Controllers	309
KS 85C30	Serial Communication Controller (SCC)	348

PRODUCT FEATURES

- **Directly drives the SCSI bus**
- **Supports asynchronous operation, with data transfer rates of 1.5 or 3.0 megabytes per second**
- **Supports arbitration, selection/reselection**
- **Supports initiator and target roles**
- **Low-power CMOS technology**
- **Generates parity**

Processor Interface

- **Supports DMA or programmed I/O**
- **Generates optional interrupts**
- **Supports DMA transfers—normal mode or block mode**
- **Supports memory or I/O mapped interface**
- **Interfaces directly with the CPU**

PRODUCT OVERVIEW

The KS53C80 is a CMOS SCSI controller, designed to provide an interface between a central processing unit, and the physical layer of the Small Computer System Interface (SCSI) bus, as defined by the ANSI X3T9.2 committee. The device can function as both target and initiator, and can be used in host port, host adapter and formatter modes.

The KS53C80 looks like a peripheral device to the microprocessor. It has internal registers, addressed by the CPU as memory mapped I/O ports. By means of these registers, the KS53C80 controls the interface between the CPU and the SCSI bus, with a minimum of intervention from the processor. Figure 1 shows a functional block diagram of the device.

If the KS53C80 detects errors on the SCSI bus, it generates an interrupt to the CPU. The chip also supports direct memory access (DMA), in normal or block mode, providing an easy interface with DMA controllers.

With the high current open collector output driver, the KS53C80 can sink 48mA at 0.5V. The device can thus be connected directly to the SCSI bus. Additional ground lines increase noise immunity, and reduce ground bouncing.

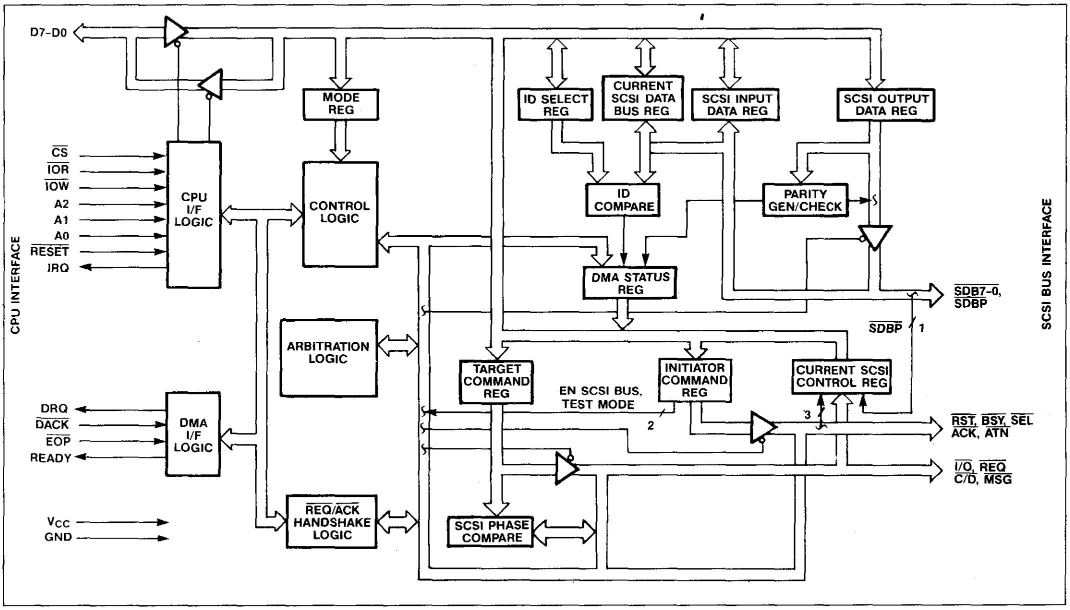


Figure 1. Functional Block Diagram of KS53C80

3

CMOS VERSUS NMOS FEATURES

The Samsung CMOS KS53C80 has a number of enhancements that differentiate it from NMOS devices. These differences are described below.

- Prevents Additional ACK Occurrences

  At the end of process, when a valid EOP is received, the NMOS device sets the end of DMA status bit and stops additional DMA requests (DRQs). This means that additional data transmitted without phase change may be lost. The KS53C80 inhibits ACK until the device is instructed to continue by a write operation to the Start DMA Initiator Receive register.

- Faster REQ/ACK Transition Times

  The KS53C80 achieves faster response times. This is partly a function of the intrinsically faster CMOS cells, but can also be attributed to design features of this particular device, such as the cell-placement priority for the handshaking signals (REQ and ACK), and the increased number of ground lines that minimize the noise factors.

- No Spurious RST Interrupt

  The KS53C80 has an internal 30μA pull up on the RST signal. This prevents an unwanted interrupt that can be caused by a floating condition on the input of the RST signal when it is not terminated on the SCSI bus.

- Verification of True End of DMA Send Operations

  The Samsung KS53C80 uses bit 7 of the Target Command Register to indicate that the last byte of the DMA transfer has actually been sent to the SCSI bus. The NMOS device does not have this feature, and if EOP is applied on the last byte, the END OF DMA status bit indicates only that the last byte has been received, and there is nothing to indicate whether this byte has been placed on the SCSI bus.

- Faster Transfer Rates

  There are two versions of the KS53C80. The slower version (1.5 megabytes per second) is the same as the N5380 NMOS device. The fast version is twice as efficient (3.0 megabytes per second).

INTERFACE SPECIFICATIONS

The KS53C80 SCSI Bus Controller is available in two packages: the first, shown in Figure 2 is a 44-pin PLCC (plastic leaded chip carrier) device. The second, shown in Figure 3 is a 48-pin DIP device.

Table 1 shows detailed pin allocations for the PLCC device, while Table 2 shows the DIP version. Table 3 provides the input/output signal definitions for the SCSI bus interface, and Table 4 for the CPU interface.

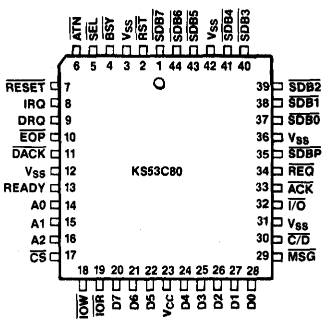


Figure 2. Physical Layout of the KS53C80 SCSI Bus Controller (PLCC Version)

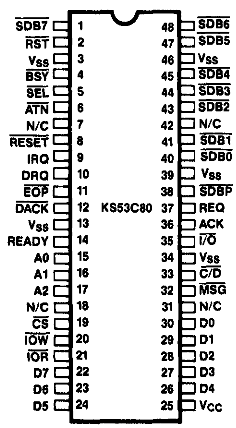


Figure 3. Physical Layout of the KS53C80 SCSI Bus Controller (DIP-48 Version)

Table 1. KS53C80 Pin Allocations PLCC Version

Pin No.	Signal Abbrev.	Signal Name
1	$\overline{SDB7}$	Data Bit 7 (SCSI)
2	$\overline{RST}$	Reset
3	V_{SS}	V_{SS}
4	$\overline{BSY}$	Busy
5	$\overline{SEL}$	Select
6	$\overline{ATN}$	Attention
7	$\overline{RESET}$	Reset
8	IRQ	Interrupt Request
9	DRQ	DMA Request
10	$\overline{EOP}$	End of Process
11	$\overline{DACK}$	DMA Acknowledge
12	V_{SS}	V_{SS}
13	READY	Ready
14	A0	Address 0
15	A1	Address 1
16	A2	Address 2
17	$\overline{CS}$	Chip Select
18	$\overline{IOW}$	I/O Write
19	$\overline{IOR}$	I/O Read
20	D7	Data 7 (CPU)
21	D6	Data 6 (CPU)
22	D5	Data 5 (CPU)
23	V_{CC}	V_{CC}
24	D4	Data 4 (CPU)
25	D3	Data 3 (CPU)
26	D2	Data 2 (CPU)
27	D1	Data 1 (CPU)
28	D0	Data 0 (CPU)
29	$\overline{MSG}$	Message
30	$\overline{C/D}$	Control/Data
31	V_{SS}	V_{SS}
32	$\overline{I/O}$	Input/Output
33	$\overline{ACK}$	Acknowledge
34	$\overline{REQ}$	Request
35	$\overline{SDBP}$	Data Bit Parity (SCSI)
36	V_{SS}	V_{SS}
37	$\overline{SDB0}$	Data Bit 0 (SCSI)
38	$\overline{SDB1}$	Data Bit 1 (SCSI)
39	$\overline{SDB2}$	Data Bit 2 (SCSI)
40	$\overline{SDB3}$	Data Bit 3 (SCSI)
41	$\overline{SDB4}$	Data Bit 4 (SCSI)
42	V_{SS}	V_{SS}
43	$\overline{SDB5}$	Data Bit 5 (SCSI)
44	$\overline{SDB6}$	Data Bit 6 (SCSI)

3

Table 2. KS53C80 Pin Allocations DIP Version

Pin No.	Signal Abbrev.	Signal Name
1	$\overline{SDB7}$	Data Bit 7 (SCSI)
2	$\overline{RST}$	Reset
3	V_{SS}	V_{SS}
4	$\overline{BSY}$	Busy
5	$\overline{SEL}$	Select
6	$\overline{ATN}$	Attention
7	N/C	Not Connected
8	$\overline{RESET}$	Reset
9	IRQ	Interrupt Request
10	DRQ	DMA Request
11	$\overline{EOP}$	End of Process
12	$\overline{DACK}$	DMA Acknowledge
13	V_{SS}	V_{SS}
14	READY	Ready
15	A0	Address 0
16	A1	Address 1
17	A2	Address 2
18	N/C	Not Connected
19	$\overline{CS}$	Chip Select
20	$\overline{IOW}$	I/O Write
21	$\overline{IOR}$	I/O Read
22	D7	Data 7 (CPU)
23	D6	Data 6 (CPU)
24	D5	Data 5 (CPU)
25	V_{CC}	V_{CC}
26	D4	Data 4 (CPU)
27	D3	Data 3 (CPU)
28	D2	Data 2 (CPU)
29	D1	Data 1 (CPU)
30	D0	Data 0 (CPU)
31	N/C	Not Connected
32	$\overline{MSG}$	Message
33	$\overline{C/D}$	Control/Data
34	V_{SS}	V_{SS}
35	$\overline{I/O}$	Input/Output
36	$\overline{ACK}$	Acknowledge
37	$\overline{REQ}$	Request
38	$\overline{SDBP}$	Data Bit Parity (SCSI)
39	V_{SS}	V_{SS}
40	$\overline{SDB0}$	Data Bit 0 (SCSI)
41	$\overline{SDB1}$	Data Bit 1 (SCSI)
42	N/C	Not Connected
43	$\overline{SDB2}$	Data Bit 2 (SCSI)
44	$\overline{SDB3}$	Data Bit 3 (SCSI)
45	$\overline{SDB4}$	Data Bit 4 (SCSI)
46	V_{SS}	V_{SS}
47	$\overline{SDB5}$	Data Bit 5 (SCSI)
48	$\overline{SDB6}$	Data Bit 6 (SCSI)

Table 3. Interface Signal Definitions—SCSI Bus

Note: I indicates that the signal is an input to the KS53C80 chip. O indicates that the signal is an output from the KS53C80 chip.

Symbol	Type	Description
SDB0-7	I/O	**Data Bits 0-7:** Eight-bit bidirectional data bus. SDB7 is the most significant bit, and has highest priority during arbitration.
SDBP	I/O	**Data Bit Parity:** This bit is used for parity checking. The bit is always generated when sending information, but parity checking when receiving is optional. Data parity is odd (the number of ones, including parity, is odd). Parity is not valid during arbitration.
SEL	I/O	**Select:** This bit is used by the initiator to select a target or by the target to reselect an initiator.
BSY	I/O	**Busy:** Indicates that the SCSI bus is being used, and may be driven by both the target and the initiator.
ACK	I/O	**Acknowledge:** ACK is asserted by the initiator during information transfer, in response to the assertion of REQ by the target. ACK is deasserted after REQ becomes inactive.
ATN	I/O	**Attention:** This signal is driven by the initiator after successful selection of the target.
RST	I/O	**Reset:** This input indicates a reset condition on the SCSI bus.
I/O	I/O	**Input/Output:** This signal indicates the direction of data flow on the SCSI bus, and is controlled by the target. When asserted, the data is transferred to the initiator. When deasserted, data is transferred to the target. The signal also distinguishes between the selection and reselection phases.
C/D	I/O	**Control/Data:** This signal is controlled by the target, and indicates that data (C/D deasserted) or control phase.
REQ	I/O	**Request:** Controlled by the target, REQ is asserted by the target to begin the handshake associated with data transfer. REQ is deasserted on receipt of ACK from the initiator. Data is latched on the falling edge of REQ for the initiator data receive operation.

Table 4. Interface Signal Definitions—CPU Bus

Symbol	Type	Description
D0-7	I/O	**Data 0-7:** This is an eight-bit bidirectional, tri-state data bus between the KS53C80 and the CPU (microprocessor). D7 is the most significant bit.
CS	I	**Chip Select:** This input from the CPU enables reading or writing of the internal register selected by address inputs A0-2.
DRQ	O	**DMA Request:** This signal is sent from the KS53C80 to the DMA controller, or the CPU, and requests a direct memory access (DMA) operation. It occurs only when the DMA Mode bit is set in the MODE Register. DRQ is cleared when DACK is asserted.
IRQ	O	**Interrupt Request:** Flags the CPU that one of the interrupt conditions has been met. This includes SCSI bus fault conditions, and events requiring CPU intervention.
READY	O	**Ready:** This signal is transferred from the KS53C80 to the CPU. It controls the speed of block mode DMA transfer and must be enabled by the CPU. It indicates that the chip is ready to send or receive data, and remains low (inactive) until the last byte has been sent, or until the DMA mode bit has been reset.
DACK	I	**DMA Acknowledge:** This input resets DRQ and, in conjunction with IOR or IOW, selects the data register to be accessed for the read or write operation. CS must be high.
EOP	I	**End of Process:** This input is sent to the KS53C80 by the CPU or DMA controller, to terminate the DMA transfer. If it is asserted during a DMA cycle, the byte being processed is sent, but no further bytes are requested. The KS53C80 can automatically generate an interrupt in response to receiving EOP.
A0-2	I	**Address 0-2:** These inputs from the CPU select one of eight internal registers in the KS53C80, in conjunction with IOR, IOW and CS.
IOR	I	**Input/Output Read:** This signal is sent from the CPU, and initiates a read operation in the register selected by A0-2 and CS.
IOW	I	**Input/Output Write:** This signal is sent from the CPU, and initiates a write operation in the register selected by A0-2 and CS.
RESET	I	**Reset:** This input clears all registers. It does not force the SCSI signal RST to become active, and thus affects only the local KS53C80.

REGISTERS

The KS53C80 is made up of eight physical registers, that are configured and addressed as 16 registers. The controlling CPU can read from or write to these registers to monitor and initiate SCSI bus activities.

There are four groups of registers:

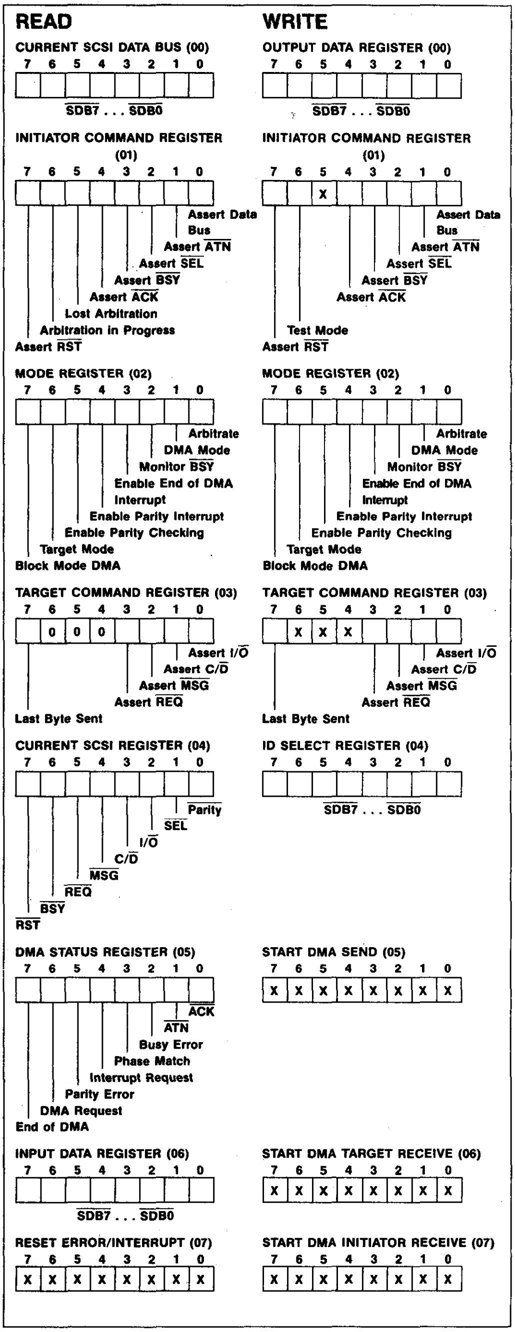
- Three **data registers**: Input Data Register, Output Data Register, and the Current SCSI Data Register.
- Three **control registers**: Mode Register, and Initiator Command Register, Target Command Register.
- Three **miscellaneous registers**: Current SCSI Bus Status Register, ID Select Register, Reset Error/ Interrupts Register.
- Four **DMA registers**: Start DMA Send Register, Start DMA Target Receive Register, Start DMA Initiator Receive Register, DMA Status Register.

Registers are selected by the address inputs, A0-2, when $\overline{CS}$ is asserted. A read operation is initiated by $\overline{IOR}$ and a write operation by $\overline{IOW}$, so that $\overline{IOR}$ and $\overline{IOW}$ act as virtual functional address bits. Table 5 shows the register addresses, and indicates the functions performed by each register. Table 6 is a register reference chart.

Table 5. Register Addresses

A2	A1	A0	Reg.	Register Name	Operation
1	1	1	7	Start DMA Initiator Receive	Write
1	1	1	7	Reset Error/Interrupt	Read
1	1	0	6	Start DMA Target Receive	Write
1	1	0	6	Input Data	Read
1	0	1	5	Start DMA Send	Write
1	0	1	5	DMA Status	Read
1	0	0	4	ID Select	Write
1	0	0	4	Current SCSI Control	Read
0	1	1	3	Target Command	Read/Write
0	1	0	2	Mode	Read/Write
0	0	1	1	Initiator Command	Read/Write
0	0	0	0	Current SCSI Data	Read
0	0	0	0	Output Data	Write

Table 6. Register Reference Chart



Note: X = Don't Care

Data Registers

Data registers are used to transfer data to and from the SCSI bus and the microprocessor bus.

Input Data Register—6 (Read Only)

FUNCTION:

Holds data received from the SCSI bus during a DMA operation. As an option, parity may be checked when the register is loaded.

When this register is functioning as a read-only input data register, data are latched into the register under the following conditions:

- $\overline{ACK}$ goes low — DMA target receive operation.
- $\overline{REQ}$ goes low — DMA initiator operation.
- DMA MODE bit is set.

The register can be read by asserting $\overline{IOR}$ and $\overline{DACK}$ at the same time or by a CPU read operation of address location 6. Note that $\overline{DACK}$ and $\overline{CS}$ must never be active simultaneously.

REGISTER CONFIGURATION

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X
$\overline{SDB7}$	$\overline{SDB6}$	$\overline{SDB5}$	$\overline{SDB4}$	$\overline{SDB3}$	$\overline{SDB2}$	$\overline{SDB1}$	$\overline{SDB0}$

Output Data Register—0 (Write Only)

FUNCTION:

Used for sending information to the SCSI bus. It is used to assert the ID bits during the arbitration and selection phases. Data is sent to the register using a normal write operation, or by asserting $\overline{IOW}$ and $\overline{DACK}$ at the same time, under DMA control, irrespective of Address and $\overline{CS}$. In I/O operation, this register is written when $\overline{IOW}$ is asserted, A0-2 = 000, and $\overline{CS}$ = 0.

REGISTER CONFIGURATION

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X
$\overline{SDB7}$	$\overline{SDB6}$	$\overline{SDB5}$	$\overline{SDB4}$	$\overline{SDB3}$	$\overline{SDB2}$	$\overline{SDB1}$	$\overline{SDB0}$

Current SCSI Data Register—0 (Read Only)

FUNCTION:

Enables the microprocessor to read the active SCSI data bus of any time. Used during programmed I/O data read, or arbitration. The SCSI bus data are not latched.

A read operation of this register is initiated when $\overline{CS}$ is low, and address 0 (A0-2 = 000) is sent from the CPU. $\overline{IOR}$ must be low to enable the read. This register is also read during arbitration to determine whether devices with higher priority are also arbitrating.

If parity checking is enabled, the SCSI bus parity is checked at the beginning of the read cycle. Parity error checking is not guaranteed during arbitration.

REGISTER CONFIGURATION

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X
$\overline{SDB7}$	$\overline{SDB6}$	$\overline{SDB5}$	$\overline{SDB4}$	$\overline{SDB3}$	$\overline{SDB2}$	$\overline{SDB1}$	$\overline{SDB0}$

Control Registers

These registers store the control signals that govern the operation of the CPU and SCSI buses.

Mode Register—2 (Read/Write)

FUNCTION:

Controls the operating modes of the chip, deciding whether the chip is to function as initiator or target; whether DMA transfers are to be used; and whether interrupts are to be generated for a number of error conditions. The register is set during a write operation ($\overline{IOW}$ = 0), and may be sampled during a read operation ($\overline{IOR}$ = 0), to check the value of the internal control bits.

REGISTER CONFIGURATION

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X
Block Mode DMA	Enable Target Mode	Enable Parity Checking	Enable Parity Interrupt	Enable $\overline{EOP}$ Interrupt	Monitor $\overline{BSY}$	Enable DMA Mode	Control arbitration

BIT 7—BLOCK MODE DMA

This bit must be used in conjunction with Bit 1 (DMA Mode)

<u>Normal DMA Mode</u>

BLOCK MODE DMA = 0 and DMA MODE bit = 1: The DMA handshake is the normal interlocked handshake. The rising edge of $\overline{DACK}$ indicates the end of each byte transfer.

Block DMA Mode

BLOCK MODE DMA = 1 and DMA MODE bit = 1: DACK is allowed to remain active during DMA operation, and READY can be used to request the next data transfer. The trailing edge of IOW or IOR indicates the end of each byte transfer.

This mode is compatible with the KS82C37 DMA Controller.

BIT 6—TARGET MODE

TARGET MODE = 1: C/D, I/O, MSG and REQ are asserted on the SCSI bus, and the chip acts as the SCSI device target.

TARGET MODE = 0: ATN, ACK are asserted on the SCSI bus, and the device acts as the SCSI device initiator.

BIT 5 - PARITY CHECK

PARITY CHECK = 1: Parity error is saved in the parity error latch whenever data is received under DMA control, or read out from the Current SCSI Data Register (0).

The state of the parity bit can be determined by reading the DMA status register (5), and can be reset by reading the Reset Error/Interrupt Register (7).

PARITY CHECK = 0: Parity error is not saved in the parity error latch.

BIT 4—ENABLE PARITY INTERRUPT

ENABLE INTERRUPT PARITY = 1: If a parity error is detected when this bit is set, and if PARITY CHECK is set, an interrupt (IRQ) is generated.

ENABLE INTERRUPT PARITY = 0: Disabled.

BIT 3—EOP INTERRUPT

INTERRUPT EOP = 1: If this bit is set, an interrupt is generated when the DMA controller asserts EOP. EOP is valid in conjunction with either IOR, IOW and DTACK.

INTERRUPT EOP = 0: Disabled.

BIT 2—BUSY MONITOR

BUSY MONITOR = 1: If BSY unexpectedly goes inactive for longer than 400 ns, but less than 1200ns, an interrupt is generated. This causes the lower six bits of the Initiator Command Register to be reset (0), and all signals are disabled on the SCSI bus until the Busy Error bit is reset. This feature allows the CPU to respond if the SCSI bus becomes available.

BUSY MONITOR = 0: Busy Monitor is disabled, and no interrupt is generated.

BIT 1—DMA MODE

DMA MODE = 1: If this bit is set, the KS53C80 is in DMA Mode, and the internal state machine controls ACK, REQ and the CPU signals DRQ and READY automatically. ASSERT DATA BUS (register 1, bit 0) must be active for all DMA transfers. TARGET MODE (Register 2, bit 6), must be active (1) for a write operation to port 6, and inactive (0) for a write operation to port 7 (initiator role). BSY must be active when this bit is set.

DMA Mode is not reset when EOP is received, but must be reset by the CPU. However, EOP automatically inhibits additional DMA cycles.

DMA MODE = 0: Stops all DMA transfers.

BIT 0—ARBITRATION

ARBITRATION = 1: Starts the arbitration process. Before this bit is set, the Output Data Register (0) should contain the correct SCSI device ID. The KS53C80 waits for the SCSI bus to be free before starting arbitration. The status of the arbitration phase can be checked by reading bit 5 and 6 in Register 1: Arbitration in Progress (bit 6), Lost Arbitration (bit 5).

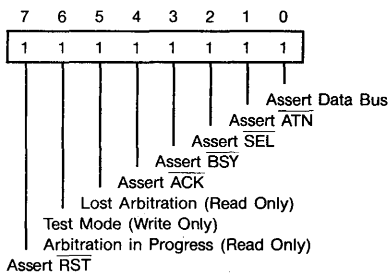
ARBITRATION = 0: Disabled

Initiator Command Register—1 (Read or Write)

FUNCTION:

Asserts and monitors certain initiator SCSI bus signals, and monitors bus arbitration.

REGISTER CONFIGURATION



BIT 7 - ASSERT RESET

ASSERT RESET = 1: RST is asserted on the SCSI bus, initializing all devices on the bus to the reset condition. IRQ goes active (high) indicating a SCSI reset. This interrupt cannot be disabled by masking it out. All control registers and logic are reset to '0' except the RST bit itself, and the Test Mode bit (Register 1, bit 6).

ASSERT RESET = 0: a). RST is disabled. b). External RESET may have been used.

BIT 6—ARBITRATION IN PROGRESS (Read Only)

ARBITRATION IN PROGRESS = 1: The arbitration bit is set, provided that the ARBITRATE bit (Register 2, bit 6) is also set. It indicates that the KS53C80 has detected a bus free phase, and is currently arbitrating for the bus. Resetting the ARBITRATE bit also resets ARBITRATION IN PROGRESS.

BIT 6—TEST MODE (Write Only)

TEST MODE = 1: When this bit is set, all output drivers, including SCSI and CPU signals are tristated. All writable registers can be accessed during Test Mode.

This function is used only during testing. When the bit is reset, the KS53C80 returns to normal operation. It can be reset by CPU signal RESET. It is not affected by RST on the SCSI bus, or by ASSERT RST bit in the Initiator Command Register.

BIT 5—LOST ARBITRATION (Read Only)

LOST ARBITRATION = 1: When this bit is asserted, it indicates that the KS53C80 has arbitrated for the bus, and detected that another device on the bus, with higher priority, has asserted the SEL line. The ARBITRATE bit (Register 2, bit 2) must be active at this time.

BIT 4—ASSERT ACK

ASSERT ACK = 1: When this bit is set, ACK is asserted on the SCSI bus. The TARGET MODE bit (Register 2, bit 6) must be reset at this time, indicating that the KS53C80 is the initiator.

BIT 3—ASSERT BSY

ASSERT BSY = 1: BSY is asserted on the SCSI bus. This only signifies that the process of selection or reselection has been completed.

BIT 2—ASSERT SEL

ASSERT SEL = 1: SEL is asserted on the SCSI bus. SEL is normally asserted after a successful arbitration.

ASSERT SEL = 0: Resetting this bit deasserts the SEL line.

BIT 1—ASSERT ATN

ASSERT ATN = 1: If the KS53C80 is the initiator (TARGET Mode bit, Register 2, bit 6 reset), ASSERT ATN asserts the ATN line to request a message out phase.

BIT 0—ASSERT DATA BUS

ASSERT DATA BUS = 1: If this bit is set, the open drain drives of SDB0-7 and the parity bit (Output Data Register) are enabled. Data and parity are asserted on the SCSI bus. For this to occur, the following conditions must exist:

- The phase signals (I/O, MSG, C/D) agree with ASSERT I/O, ASSERT C/D, and ASSERT MSG in the Target Command Register, meaning that there is no phase mismatch.
- The I/O is inactive, which means the output is to the target.
- TARGET MODE is inactive.

When the KS53C80 operates as target, the TARGET Mode bit must be set, and the outputs are asserted unconditionally. During arbitration, ASSERT DATA BUS bit has no influence.

Target Command Register—3 (Read/Write)

FUNCTION:

This register controls and monitors the SCSI information transfer phases.

The functions and the conditions governing the functions of this register differ, depending upon whether the KS53C80 is acting as initiator or target.

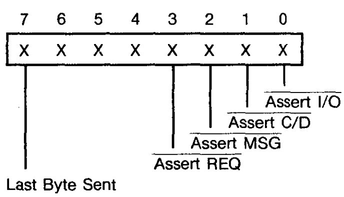
Initiator (Read):

The Target Command Register allows the target to monitor and set/reset the SCSI lines REQ, MSG, C/D and I/O. In addition, reading a '1' in bit 7 signals that the last byte has been send to the SCSI bus during a DMA write operation.

Target (Write):

When the device is in Target Mode, the register enables the CPU to control the SCSI bus information transfer phase asserted by the target.

REGISTER CONFIGURATION



BIT 7—LAST BYTE SENT

LAST BYTE SENT = 1: This bit is set to indicate that the last byte in a DMA transfer has been sent to the SCSI bus.

BITS 6-4—NOT USED

BIT 3—ASSERT REQ

ASSERT REQ = 1: REQ is asserted. Note that the REQ line is asserted only if the KS53C80 is in Target Mode (Register 2 bit 6 is set.)

ASSERT REQ = 0: REQ is deasserted.

BITS 2-0—ASSERT REQ, ASSERT MSG, ASSERT C/D

These bits are encoded to control a variety of SCSI bus functions.

MSG	C/D	I/O	Phase	Direction I(nitiator) ⇄ T(arget)
0	0	0	Data Out	I → T
1	0	0	Unspecified	
0	1	0	Command Transfer	I → T
1	1	0	Message Out	I → T
0	0	1	Data In	I ← T
1	0	1	Unspecified	
0	1	1	Status	I ← T
1	1	1	Message In	I ← T

I/O controls the bidirectional SCSI bus, and decides whether it is to function as an input or output bus to the KS53C80. When I/O is high, the SCSI bus functions as an input bus to the chip. When I/O is low (active) it is an output bus from the chip. The I/O line is asserted only if the Target Mode bit is set.

C/D determines whether control information or data is transferred on the bus. When C/D is high, control information is transferred on the bus. When C/D is low (active) data is transferred on the bus.

MSG selects between Message and Status or Command transfers on the bus. When it is high, status or commands are transferred. When MSG is low (active) messages are transferred.

When the KS53C80 is connected as Initiator and the DMA mode bit is true, a phase mismatch interrupt is generated when REQ goes active and the phase lines I/O, C/D and MSG are in different state than the appropriate bit in the Target command register.

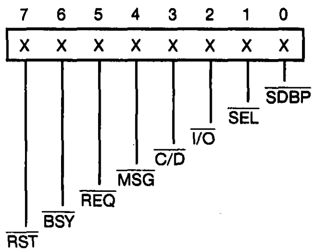
Miscellaneous Registers

Current SCSI Bus Control Register—4 (Read Only)

FUNCTION:

This register is used to monitor seven SCSI bus control signals, and the data parity bit. The SCSI control lines are not latched. The CPU may sample the register to determine the current bus phase, or poll REQ to see if a data transfer is pending. Note that the SCSI signals are true (low) if the appropriate bit is set in the register.

REGISTER CONFIGURATION



BIT 7—RST

RST = 1: SCSI bus is in a reset condition.
RST = 0: SCSI bus in not reset.

BIT 6—BSY

BSY = 1: SCSI bus is being used.
BSY = 0: SCSI bus is free.

BIT 5—REQ

REQ = 1: Indicates a request for a REQ/ACK data transfer has been received by the KS53C80.
REQ = 0: REQ is inactive.

BIT 4—MSG

MSG = 1: The bus transfer is in the message phase.
MSG = 0: The bus is not in message phase.

BIT 3—C/D

C/D = 1: Data is on the bus.
C/D = 0: Control signals are on the bus.

BIT 2—I/O

I/O = 1: Data is being transferred to the initiator.
I/O = 0: The bus is active as an input bus.

BIT 1—$\overline{SEL}$

$\overline{SEL}$ = 1: The initiator has selected a target, or a target has reselected an initiator.
$\overline{SEL}$ = 0: The device is not selected.

BIT 0—$\overline{SDBP}$

$\overline{SDBP}$ = 1/0: Indicates state of parity bit.

Note that parity is odd, so $\overline{SDBP}$ is set high or low, (depending upon the state of the eight data bits), to force an odd number of ones, including the parity bit.

ID Select Register—4 (Write Only)

FUNCTION:

Monitors a single device ID if selection or reselection is being attempted. An ID number is given to each SCSI device in a system, by assigning one bit of the ID register. If an ID match is found while a bus-free condition exists, $\overline{BSY}$ false and $\overline{SEL}$ is active, the KS53C80 will generate an interrupt to indicate a selection or reselection.

Parity is checked in the selected device if ENABLE PARITY CHECKING is appropriately set (active).

REGISTER CONFIGURATION

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X
SDB7	SDB6	SDB5	SDB4	SDB3	SDB2	SDB1	SDB0

Reset Error/Interrupt Register—7 (Read Only)

FUNCTION:

This is a dummy register. When the register is read, the following actions take place:

- Reset Interrupt Request (IRQ) signal.
- Interrupt Latch request bit reset in Register 5.
- Busy Error is reset in Register 5.
- Parity Error is reset in Register 5.

REGISTER CONFIGURATION

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X

DMA Registers

Three write-only registers initiate all DMA activity. The following Mode bits must be set appropriately, before a write operation is performed in any of these registers. Data (D0-7) are not valid and are meaningless when a write operation is being performed in one of the DMA registers.

Target Mode	DMA Mode	Block* Mode DMA	Register Selected
X	1	1/0	Start DMA Send
1	1	1/0	Start DMA Target Receive
0	1	1/0	Start DMA Initiator Receive

* This bit is set (1) to enable Block Mode DMA transfer. If it is 0, a normal DMA transfer is initiated.

Start DMA Send Register—5 (Write Only)

FUNCTION:

Initiates a DMA send from the DMA to the SCSI bus, during either a Target or an Initiator operation. The DMA MODE bit (Register 2, bit 1) must be set prior to starting a DMA operation.

REGISTER CONFIGURATION

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X

Start DMA Target Receive Register—6 (Write Only)

FUNCTION:

Initiates a DMA receive from the SCSI bus to the DMA, during Target mode only. Both the DMA Mode bit (Register 2, bit 1) and the TARGET Mode bit (Register 2, bit 6) must be set.

REGISTER CONFIGURATION

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X

Start DMA Initiator Receive Register—7 (Write Only)

FUNCTION:

Initiates a DMA receive from the SCSI bus to the DMA, during Initiator mode only. The DMA Mode Bit (Register 2, bit 1) must be set, and the TARGET Mode Bit (Register 2, bit 6) must be reset prior to this operation.

REGISTER CONFIGURATION

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X

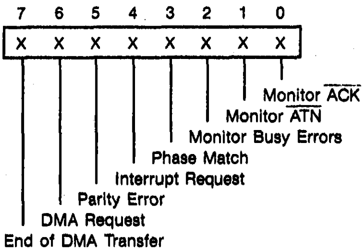
3

DMA Status Register—5 (Read Only)

FUNCTION:

Monitors the control signals not found in the Current SCSI Bus Status Register (ATN, ACK), and six status bits.

REGISTER CONFIGURATION



BIT 7—END OF DMA TRANSFER

END OF DMA TRANSFER = 1: This bit is set only if a valid EOP has been received: DACK, EOP and either the read initiate (IOR) or write initiate (IOW) signals are active at the same time. REQ and ACK should be monitored to make sure that the last byte has actually been transferred, since EOP may go active while the last byte is being sent to the Output Data Register.

This bit is reset by whenever the DMA MODE bit is reset in the Mode Register. This may occur when the busy condition is lost. Therefore, the DMA STATUS Register should be read before resetting the ASSERT BSY bit (Register 1, bit 3), at the conclusion of the DMA transfer.

BIT 6—DMA REQUEST

DMA REQUEST = 1: Permits the CPU to read the output pin DRQ.

The bit is cleared by resetting the DMA MODE bit in the Mode Register, or by asserting DACK and IOW for DMA send (write) operations, and DACK and IOR for DMA read operations. It is not reset if a Phase Mismatch Interrupt Occurs

BIT 5—PARITY ERROR

PARITY ERROR = 1: Indicates that a parity error has occurred during device selection, or during receipt of data.

It can be set only when the ENABLE PARITY CHECK bit is active. It is cleared by reading the RESET PARITY/INTERRUPT Register (7).

BIT 4—INTERRUPT REQUEST ACTIVE

INTERRUPT REQUEST ACTIVE = 1/0: Indicates the current state of the IRQ output.

The bit is cleared by reading the Reset Parity/Interrupt Register.

BIT 3—PHASE MATCH

PHASE MATCH = 1: When active, it indicates whether the lower three bits of the Target Command Register match the Current SCSI bus signals, MSG, C/D, I/O. This bit must be set before data is transferred on the SCSI bus. The bit is updated constantly, to reflect the current status. It is used by the initiator. (SCSI signals MSG, C/D and I/O indicate the current transfer phases.)

BIT 2—BUSY ERROR

BUSY ERROR = 1: Indicates the loss of the BSY signal. It is set if MONITOR BUSY is active (1) and BSY goes inactive for at least the bus-settle period of 400ns. When this bit is set, SCSI outputs are disabled, and DMA MODE is reset.

BIT 1—MONITOR ATN

MONITOR ATN = 1/0: Indicates the condition of the SCSI bus control signal ATN. This bit is monitored by the CPU.

BIT 0—MONITOR ACK

MONITOR ACK = 1/0: Indicates the state of the SCSI bus control signal ACK. This bit is monitored by the target device.

DATA TRANSFER MODES

The KS53C80 controls data transfer between SCSI bus devices. It supports four operating modes:

- Programmed Input/Output (I/O) transfer
- Normal Direct Memory Access (DMA) transfer
- Block DMA transfer
- Pseudo DMA transfer.

Programmed I/O Transfer

This transfer mode is used to transfer small data blocks, such as control, message or status.

To start an initiator send operation, bits C/D, I/O and MSG in the Target Command Register are set to enable control or data to be placed on the bus; to enable the SCSI bus as an input or an output device; and to determine whether the transfer is a message or non-message transfer.

For an operation to start, there must be a phase match; ASSERT DATA BUS must be active, and the I/O signal must be inactive. The handshake signals REQ and ACK are monitored and asserted individually, by reading the CPU and writing the appropriate register bits.

The data to be transferred is loaded into the Output Data Register (0). The processor waits until REQ is asserted (Register 4, bit 5), and then looks for a Phase Match. If there is an appropriate match, ASSERT ACK is asserted, to complete the handshake. The CPU samples REQ until it becomes inactive, indicating that the request for transfer has been met. At that point, ASSERT ACK is reset.

Normal DMA Transfer

DMA transfers are generally used to transfer large blocks of data. The DMA Mode bit must be set, and the BLOCK Mode bit must be reset.

To initiate a DMA transfer the KS53C80 generates a DMA request (DRQ) to transfer a byte to or from the DMA Controller. This DRQ is output to the DMA Controller. The DMA Controller acknowledges receipt, with the DACK handshaking signal, and asserts either IOR or IOW, to enable a read or a write operation, respectively. DRQ is terminated when DACK goes active, and DACK is terminated at the end of the minimum pulse width for IOR or IOW. This procedure is followed for each byte transferred. Note that DACK must not be active while CS is active.

DMA Block Transfer

To increase transfer rate, an external DMA device, such as the KS82C37 can go into block mode transfer, and perform sequential DMA transfers, without giving up the bus to the CPU. Block mode transfers are supported for both Target and Initiator roles. In this mode, the BLOCK Mode bit must be set.

At the start of the transfer, DRQ is asserted, as for normal transfer. DACK is then asserted, to acknowledge request, and remains active during the entire transfer. While DACK is active, the CPU cannot gain access to the system bus. IOR or IOW is asserted, to initiate the read or write operation. When the read or write initiate is terminated, READY goes active, indicating that the KS53C80 is ready for another data transfer. READY is used to insert wait states in a read or write cycle as long as READY is low.

To get the best performance in block mode, the DMA logic may optionally use the normal DMA mode DRQ-DACK handshaking.

Block Mode transfers end when IOR or IOW goes inactive. This means that another transfer can be initiated, without waiting for DACK, thus increasing the data throughput rate.

READY will be false (low) whenever the Input Data Register (R6) or the byte in the Output Data Register (R0) is not sent to the SCSI data bus.

Care must be taken when using READY as a DMA request signal. If a phase mismatch error occurs during transfer, READY will remain inactive and INT will be asserted. In this instance, the control has to given back from the DMA Controller to the CPU so that the interrupt can be received.

3

Emulated DMA Mode Transfer During I/O Transfers

To improve performance during I/O transfers, and avoid continually monitoring and asserting REQ and ACK, the system may be set up to emulate DMA mode during I/O transfers.

The KS53C80 operates in DMA mode, and uses the CPU to generate the DMA handshake signals. DRQ is then monitored by polling the DMA REQ bit (6) in the DMA Status Register (5); by sampling the signal through an external IO port; or by using it to generate a CPU interrupt.

When DRQ is detected, the CPU can proceed with a DMA read or write transfer. External decoding is used to generate the appropriate IOR, IOW and DACK signals. Since external logic is often needed to generate CS, the designer can take advantage of the same logic to generate DACK at no extra cost.

Halting DMA Operation

The DMA operation may be halted in a number of ways, as described below.

Using the EOP Signal

To halt DMA operation, EOP is asserted for the required minimum time while IOR or IOW and DACK are simultaneously active. If EOP goes active and neither IOR or IOW is active, an interrupt is generated, but the DMA transfer continues.

The EOP signal does not reset the DMA MODE bit, so provisions must be made to do this. In addition, since EOP may go active during the last byte sent to the Output Data Register, the REQ and ACK signals should be monitored to make sure that the last byte has actually been sent. In addition, LAST BYTE SEND (Register 3, bit 7) can be monitored. Note that this bit is not implemented in all 5380-type SCSI controllers.

Bus Phase Mismatch Interrupt

Bus phase mismatch halts a DMA transfer. This method can be used if the KS53C80 is operating as an initiator. It prevents recognition of REQ, and disables all the SCSI data and parity drivers. If REQ becomes active, an interrupt will be generated. The DMA transfer is stopped, however the DMA MODE bit must be reset by the CPU or by a valid EOP signal.

Resetting the DMA MODE Bit

A DMA mode transfer may be terminated at any time by resetting the DMA MODE bit. This bit should also be reset if the operation was halted by EOP or by a phase mismatch interrupt.

If the DMA MODE bit is used instead of EOP during a Target role operation, the time when the bit is reset is critical, and in most instances, it is easier to use EOP when the device is in Target Mode. If the KS53C80 is receiving data as the target device, DMA MODE should be reset when the last DRQ is received, and before DACK is asserted. Otherwise, an additional REQ will occur. When DMA MODE is reset, DRQ is terminated. However, the last byte received will remain in the Input Data Register, and may be obtained either by performing a normal CPU read operation, or by cycling DACK and IOR.

The DMA MODE bit must be set before writing to any of the Start DMA registers for subsequent bus phases.

INTERRUPTS

The KS53C80 generates an interrupt signal (IRQ) which it sends to the processor when a task has been completed or if an abnormal operating condition is detected. The following occurrences will cause IRQ to be asserted:

- The KS53C80 is selected or reselected
- The. operation is completed and EOP is asserted during a DMA transfer
- The SCSI bus is disconnected and the BSY signal is lost
- A parity error is detected
- The SCSI bus is reset
- There is a SCSI bus phase mismatch.

When the CPU receives an interrupt (IRQ), it reads the DMA Status Register and the Current SCSI Bus Status Register, to determine what was the cause of the interrupt.

IRQ is reset by writing to the Reset Error/Interrupt Register (7), or by driving RESET active to implement an external reset.

Selection/Reselection Interrupt

A select interrupt occurs when the select signal (SEL) is active; the device ID is valid, and the SCSI bus is not busy (BSY inactive for a bus-settle delay of at least 400 nanoseconds). If I/O is active, this is considered to be a reselect interrupt.

ID status is decided by a match in the ID Select Register (4). A single-bit match is adequate to enable the interrupt. SCSI bus protocol requires that not more than two devices be active during the selection process. The Current SCSI Data Register (0) is read to make sure that this condition is met.

If parity checking is supported, parity is also expected to be good during the selection phase. So if ENABLE PARITY BIT (Register 2, bit 5) is set, the PARITY ERROR bit should be sampled to make sure that there is no parity error.

The appropriate settings for the DMA Status Register and Current SCSI Bus Register during a selection/reselection interrupt are shown below.

DMA Status Register—5 Read Only

7	6	5	4	3	2	1	0
0	0	0	1	X	0	X	0
End of DMA	DMA Request	Parity Error	Interrupt Request Active	Phase Match	Busy Error	ATN	ACK

Current SCSI Bus Status Register—4 Read Only

7	6	5	4	3	2	1	0
0	0	0	X	X	X	1	X
RST	BSY	REQ	MSG	C/D	I/O	SEL	SDBP

The select interrupt is disabled by writing all zeros into the ID Select Register (4)

End of Process (EOP) Interrupt

An end of process signal (EOP) occurring during a DMA transfer (DMA MODE active), sets the END OF DMA status bit (Register 5, bit 7) and generates an interrupt. ENABLE EOP INTERRUPT bit (Register 2, bit 3) is set. EOP is not recognized unless EOP, DACK and either IOR or IOW are concurrently active time. DMA transfers will still occur if EOP is asserted.

The appropriate settings for the DMA Status Register and the Current SCSI Bus Status Register during an EOP interrupt, are shown below.

DMA Status Register—5 Read Only

7	6	5	4	3	2	1	0
1	0	0	1	0	0	0	X
End of DMA	DMA Request	Parity Error	Interrupt Request Active	Phase Match	Busy Error	ATN	ACK

Current SCSI Bus Status Register—4 Read Only

7	6	5	4	3	2	1	0
0	1	X	X	X	X	0	X
RST	BSY	REQ	MSG	C/D	I/O	SEL	SDBP

This interrupt is disabled by resetting the ENABLE EOP INTERRUPT bit.

Loss of Busy Interrupt

This interrupt is generated if the BSY signal goes false (indicating disconnection of the SCSI bus) for at least a bus-settle delay period of 400 nanoseconds.

The appropriate settings for the DMA Status Register and the Current SCSI Bus Status Register during a loss of BSY interrupt, are shown below.

DMA Status Register—5 Read Only

7	6	5	4	3	2	1	0
0	0	0	1	X	1	0	0
End of DMA	DMA Request	Parity Error	Interrupt Request Active	Phase Match	Busy Error	ATN	ACK

Current SCSI Bus Status Register—4 Read Only

7	6	5	4	3	2	1	0
0	0	0	X	X	X	1	X
RST	BSY	REQ	MSG	C/D	I/O	SEL	SDBP

The Loss of Busy Interrupt is disabled by resetting the MONITOR BUSY bit.

Parity/Error Interrupt

Parity status is checked by reading the Current SCSI Data Register. If the PARITY ERROR bit is set, an interrupt will be generated, provided that the ENABLE PARITY CHECK bit (5) and ENABLE PARITY INTERRUPT bit (Register 2, bit 4) are set in the Mode Register (Register 2, bit 5). The parity checking feature can be used without generating a parity error interrupt if the ENABLE PARITY CHECK bit is disabled.

The appropriate settings for the DMA Status Register and the Current SCSI Bus Status Register during Parity Error interrupt, are shown below.

DMA Status Register—5 Read Only

7	6	5	4	3	2	1	0
0	X	1	1	1	0	X	X
End of DMA	DMA Request	Parity Error	Interrupt Request Active	Phase Match	Busy Error	$\overline{\text{ATN}}$	$\overline{\text{ACK}}$

Current SCSI Bus Status Register—4 Read Only

7	6	5	4	3	2	1	0
0	0	0	X	X	X	1	X
$\overline{\text{RST}}$	$\overline{\text{BSY}}$	$\overline{\text{REQ}}$	$\overline{\text{MSG}}$	$\overline{\text{C/D}}$	$\overline{\text{I/O}}$	$\overline{\text{SEL}}$	$\overline{\text{SDBP}}$

SCSI Bus Reset Interrupt

$\overline{\text{RST}}$ going active generates the SCSI Bus Reset Interrupt. After a bus clear delay of 800 nanoseconds, the KS53C80 releases all bus signals. This type of interrupt may also be generated by setting ASSERT $\overline{\text{RST}}$ (Register 1, bit 7). Since $\overline{\text{RST}}$ is not latched in the Current SCSI Bus Status Register, this bit may not be set when the register is read. The reset status may then be decided by default.

The appropriate settings for the DMA Status Register and the Current SCSI Bus Status Register during SCSI Bus Reset interrupt, are shown below.

DMA Status Register—5 Read Only

7	6	5	4	3	2	1	0
0	0	0	X	X	X	1	X
End of DMA	DMA Request	Parity Error	Interrupt Request Active	Phase Match	Busy Error	$\overline{\text{ATN}}$	$\overline{\text{ACK}}$

Current SCSI Bus Status Register—4 Read Only

7	6	5	4	3	2	1	0
0	0	0	X	X	X	1	X
$\overline{\text{RST}}$	$\overline{\text{BSY}}$	$\overline{\text{REQ}}$	$\overline{\text{MSG}}$	$\overline{\text{C/D}}$	$\overline{\text{I/O}}$	$\overline{\text{SEL}}$	$\overline{\text{SDBP}}$

This interrupt may not be disabled.

SCSI Bus Phase Mismatch Interrupt

The SCSI bus phases are controlled by $\overline{\text{I/O}}$, $\overline{\text{C/D}}$ and $\overline{\text{MSG}}$. These signals are constantly compared with corresponding bits in the Target Command Register (ASSERT I/O, ASSERT C/D, ASSERT MSG). The results of the comparison are stored in DMA Status Register (PHASE MATCH).

If a phase mismatch is detected during a DMA transfer (DMA MODE active) when $\overline{\text{REQ}}$ is active, an interrupt is generated. $\overline{\text{REQ}}$ is not recognized during a phase mismatch, and the KS53C80 is disconnected from the SCSI bus during an initiator send operation. $\overline{\text{SDB0-7}}$ cannot be driven, even if ASSERT DATA BUS is active.

This interrupt is significant only when the device is acting as initiator. It may occur in Target mode, if another device is driving the phase lines to a different state.

The appropriate settings for the DMA Status Register and the Current SCSI Bus Status Register during Bus Phase Mismatch interrupt, are shown below.

DMA Status Register—5 Read Only

7	6	5	4	3	2	1	0
0	0	0	1	0	0	X	0
End of DMA	DMA Request	Parity Error	Interrupt Request Active	Phase Match	Busy Error	$\overline{\text{ATN}}$	$\overline{\text{ACK}}$

Current SCSI Bus Status Register—4 Read Only

7	6	5	4	3	2	1	0
0	1	1	X	X	X	0	X
$\overline{RST}$	$\overline{BSY}$	$\overline{REQ}$	$\overline{MSG}$	$\overline{C/D}$	$\overline{I/O}$	$\overline{SEL}$	$\overline{SDBP}$

The bus phase mismatch interrupt is disabled by resetting the DMA MODE bit.

RESETS CONDITIONS

There are three ways in which the KS53C80 can be reset.

Chip Reset

The chip is reset when the $\overline{RESET}$ input from the processor goes active and remains active for a minimum time. The chip is initialized, and all internal registers and control logic are cleared. This signal does not reset the SCSI bus.

SCSI Bus Reset ($\overline{RST}$) Received

The $\overline{RST}$ input from the SCSI bus generates an interrupt (IRQ), and resets all internal logic and registers in the chip, with the exception of the IRQ latch, and the ASSERT RST bit 7 in the Initiator Command Register.

SCSI Bus Reset ($\overline{RST}$) Issued

$\overline{RST}$ may also go active on the SCSI bus if the CPU sets ASSERT RST (bit 7) in the Initiator Command Register. $\overline{RST}$ clears all internal logic and registers, as described above, with the exception of IRQ and ASSERT RST. $\overline{RST}$ generated in this way remains active until either ASSERT RST is reset, or until a chip reset is initiated.

DC CHARACTERISTICS

This section provides the DC power characteristics for the KS53C80 SCSI Controller.

Absolute Maximum Ratings

Supply Voltage .... -0.5V to 7.0V
Input Voltage .... 0V to 5.5V
Output Voltage .... 0V to V_{CC}
Storage Temperature .... -65°C to 150°C

Power Requirements

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{CC}	Supply Voltage		4.5	5.0	5.5	V
I_{DD}*	Supply Current		—	10	20	mA
T_A	Ambient Temperature		0.0	25	70	°C

* All input pins should not be floating.

Input Requirements

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	Input High Level		2.0	—	5.25	V
V_{IL}	Input Low Level		-0.3	—	0.8	V
SCSI Bus						
I_{IH}	Input High Level	V_{IH} = 5.5V	—	—	50	μA
I_{IL}	Input Low Level	V_{IL} = 0V	—	—	-50	μA
Other Pins						
I_{IH}	Input High Level	V_{IH} = 5.5V	—	—	10	μA
I_{IL}	Input Low Level	V_{IL} = 0V	—	—	-10	μA

Output Requirements

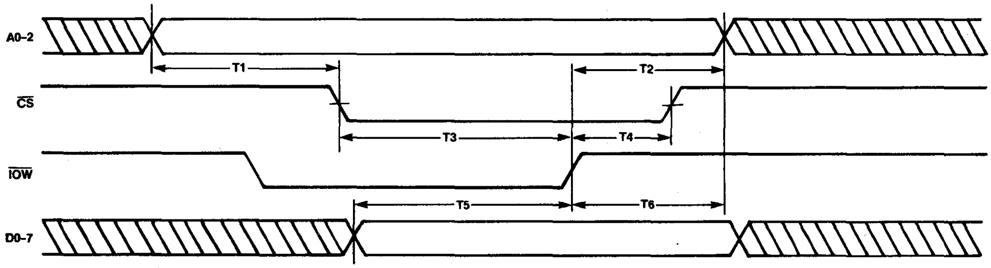
Symbol	Parameter	Condition	Min	Typ	Max	Unit
SCSI Bus						
V_{OL}	Output High Level	V_{CC} = Min., I_{OL} = 48.0mA	—	—	0.5	V
Other Pins						
V_{OH}	Output High Level	V_{SS} = Min., I_{OH} = -3.0mA	2.4	—	—	V
V_{OL}	Output Low Level	V_{SS} = Min., I_{OL} = 7.0mA	—	—	0.5	V

AC SWITCHING CHARACTERISTICS

Figures 4 through 12 provide switching characteristics for a number of typical KS53C80 operations:

- Figure 4. CPU Write Cycle Timing
- Figure 5. CPU Read Cycle Timing
- Figure 6. DMA Read (Block Mode) Target Receive Timing
- Figure 7. DMA Write (Block Mode) Target Send Timing
- Figure 8. DMA Read (Non-Block Mode) Target Receive Timing
- Figure 9. DMA Write (Non-Block Mode) Target Send Timing
- Figure 10. DMA Read (Non-Block Mode) Initiator Receive Timing
- Figure 11. DMA Write (Non-Block Mode) Initiator Send Timing
- Figure 12. Arbitration Timing
- Figure 13. Reset Timing

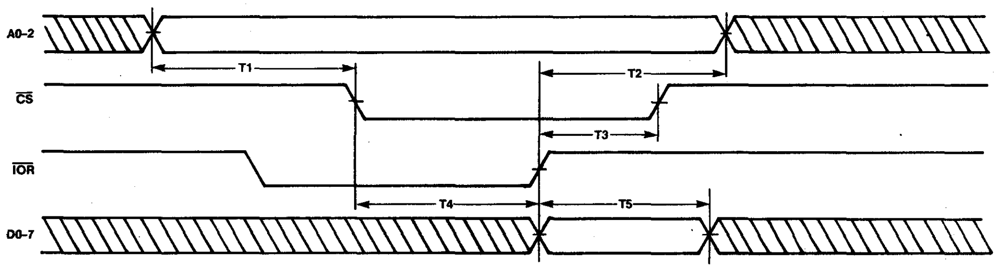
Figure 4. CPU Write Cycle Timing



Name	Description	1.5M/sec			3.0M/sec			Units
		Min	Typ	Max	Min	Typ	Max	
T1	Address Setup to Write Enable	20			10			ns
T2	Address Hold from End Write Enable	20			10			ns
T3	Write Enable Width	70			35			ns
T4	Chip Select Hold from End of $\overline{IOW}$	0			0			ns
T5	Data Setup to End of Write Enable	50			20			ns
T6	Data Hold Time from End of $\overline{IOW}$	30			10			ns

Note: Write enable is the occurrence of $\overline{CS}$ and $\overline{IOW}$.

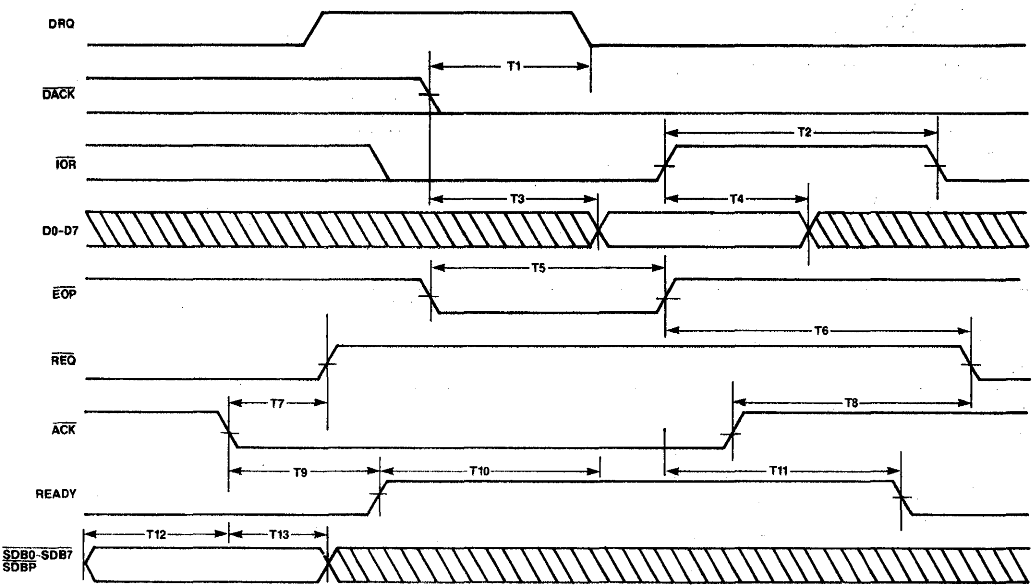
Figure 5. CPU Read Cycle Timing



Name	Description	1.5M/sec			3.0M/sec			Units
		Min	Typ	Max	Min	Typ	Max	
T1	Address Setup to Read Enable	20			10			ns
T2	Address Hold from End Read Enable	20			10			ns
T3	Chip Select Hold from End of $\overline{IOR}$	0			0			ns
T4	Data Access Time from Read Enable			130			65	ns
T5	Data Hold Time from End of $\overline{IOR}$	20			10			ns

Note: Read enable is the occurrence of $\overline{CS}$ and $\overline{IOR}$.

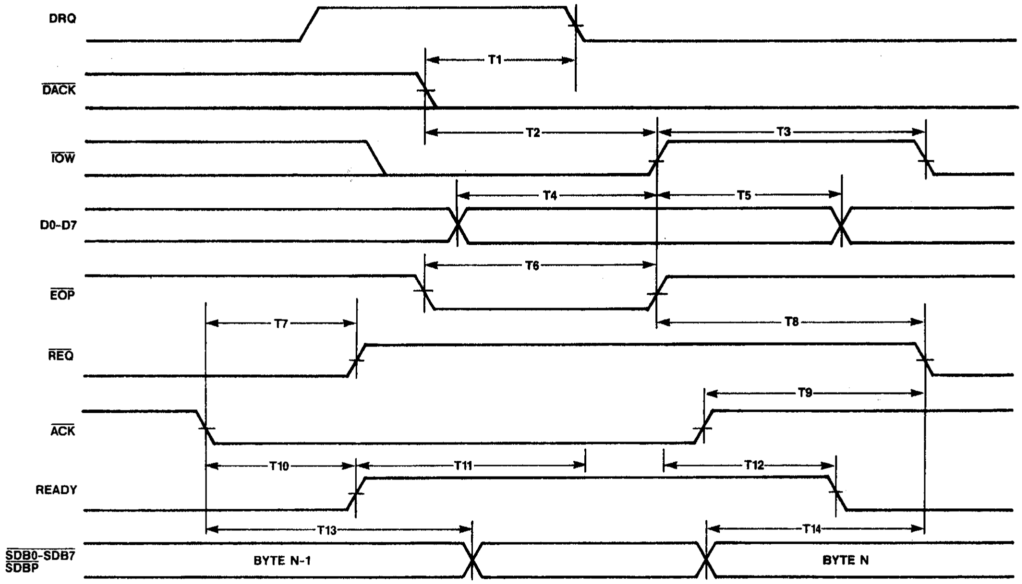
Figure 6. DMA Read (Block Mode) Target Receive Timing



Name	Description	1.5M/sec Min	1.5M/sec Typ	1.5M/sec Max	3.0M/sec Min	3.0M/sec Typ	3.0M/sec Max	Units
T1	DRQ False from $\overline{\text{DACK}}$ True			130			60	ns
T2	$\overline{\text{IOR}}$ Recovery Time	120			60			ns
T3	Data Access Time from Read Enable		100	110			50	ns
T4	Data Hold Time from End of $\overline{\text{IOR}}$	20			10			ns
T5	Width of $\overline{\text{EOP}}$ Pulse	100			50			ns
T6	$\overline{\text{IOR}}$ False to $\overline{\text{REQ}}$ True ($\overline{\text{ACK}}$ False)			190			70	ns
T7	$\overline{\text{ACK}}$ True to $\overline{\text{REQ}}$ False			125			50	ns
T8	$\overline{\text{ACK}}$ False to $\overline{\text{REQ}}$ True ($\overline{\text{IOR}}$ False)			170			70	ns
T9	$\overline{\text{ACK}}$ True to READY True			140			60	ns
T10	READY True to Valid CPU Data			50			20	ns
T11	$\overline{\text{IOR}}$ False to READY False	20	125	140			70	ns
T12	SCSI DATA Setup Time to $\overline{\text{ACK}}$ True	20			10			ns
T13	SCSI DATA Hold Time from $\overline{\text{ACK}}$ True	50			20			ns

Note: $\overline{\text{DACK}}$, $\overline{\text{IOR}}$, and $\overline{\text{EOP}}$ = 1, for at least T5 for $\overline{\text{EOP}}$ pulse recognition. Read enable is $\overline{\text{DACK}}$ and $\overline{\text{IOR}}$ occurrence.

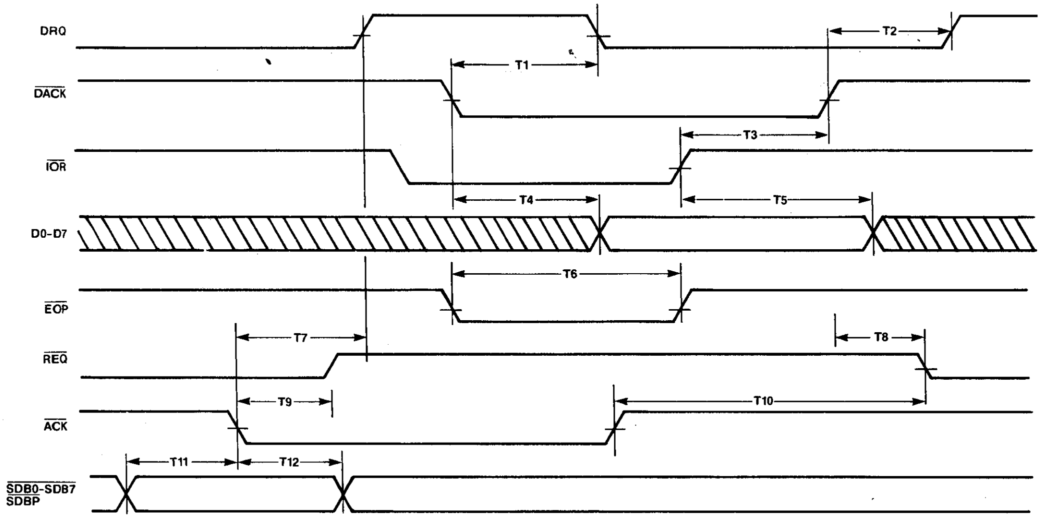
Figure 7. DMA Write (Block Mode) Target Send Timing



Name	Description	1.5M/sec			3.0M/sec			Units
		Min	Typ	Max	Min	Typ	Max	
T1	DRQ False from DACK True	100		130			60	ns
T2	Write Enable Width	100			50			ns
T3	Write Recovery Time	120			60			ns
T4	Data Setup to End of Write Enable	50			20			ns
T5	Data Hold Time from End of IOW	40			20			ns
T6	Width of EOP Pulse	100			50			ns
T7	ACK True to REQ False			125			60	ns
T8	REQ from End of IOW (ACK False)			180			100	ns
T9	REQ from End of ACK (IOW False)			170			90	ns
T10	ACK True to READY True			140			70	ns
T11	READY True to IOW False	70			30			ns
T12	IOW False to READY False	20	130	140			70	ns
T13	DATA Hold Time from ACK True	40			20			ns
T14	Data Setup to REQ True	60			30			ns

Note: DACK, IOW, and EOP = 1, for at least T6 for EOP pulse recognition. Write enable is DACK and IOW occurrence.

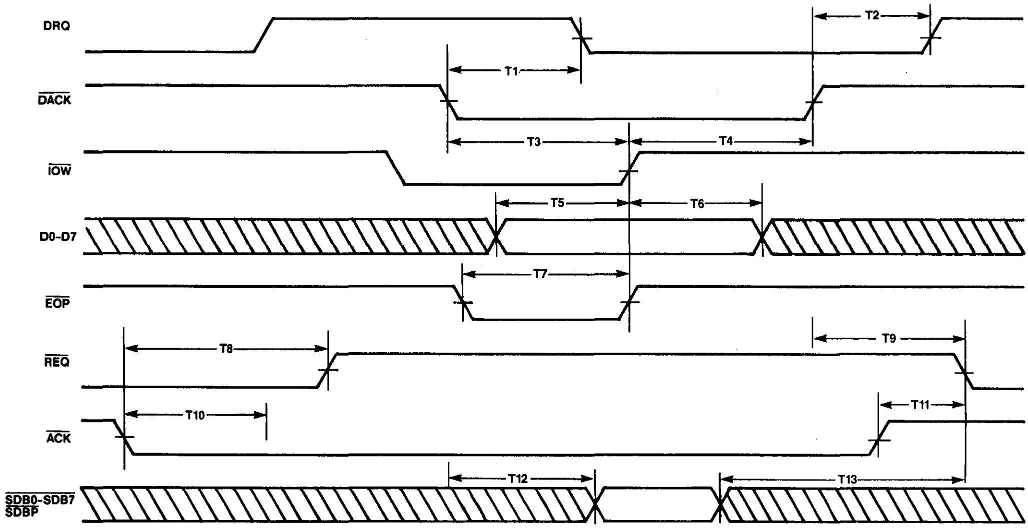
Figure 8. DMA Read (Non-Block Mode) Target Receive Timing



Name	Description	1.5M/sec			3.0M/sec			Units
		Min	Typ	Max	Min	Typ	Max	
T1	DRQ False from DACK and IOR True			130			60	ns
T2	DACK False to DRQ True	30			20			ns
T3	DACK Hold Time from End of IOR	0			0			ns
T4	Data Access Time from Read Enable (IOR and DACK Low)			115			60	ns
T5	Data Hold Time from End of IOR	20			10			ns
T6	Width of EOP Pulse	100			50			ns
T7	ACK True to DRQ True			110			60	ns
T8	DACK False to REQ True (ACK False)			150			70	ns
T9	ACK True to REQ False			125			60	ns
T10	ACK False to REQ True (DACK False)			150			70	ns
T11	SCSI DATA Setup Time to ACK	20			10			ns
T12	SCSI DATA Hold Time from ACK	50			20			ns

Note: DACK, IOR, and EOP = 1, for at least T6 for EOP pulse recognition. Write enable is DACK and IOR occurrence.

Figure 9. DMA Write (Non-Block Mode) Target Send Timing

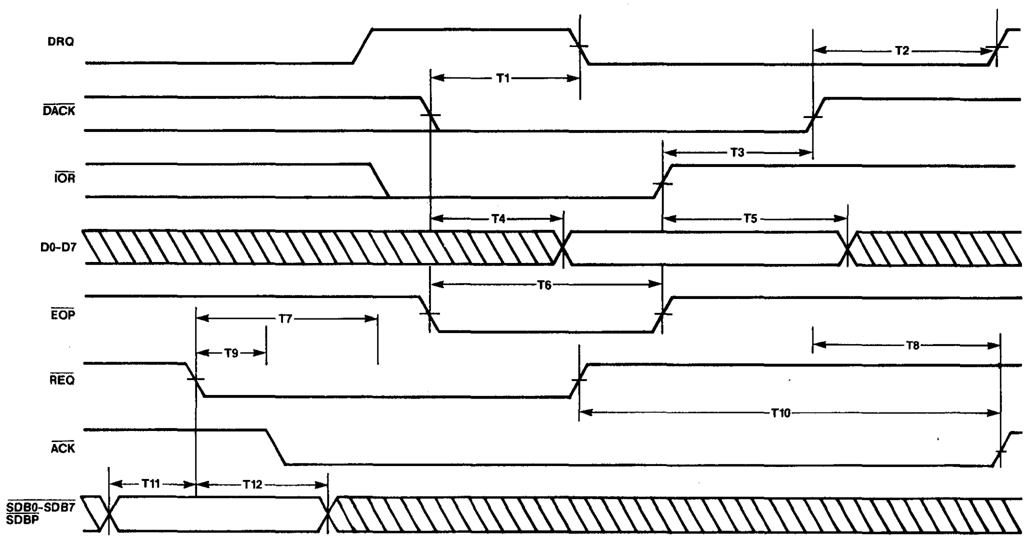


Name	Description	1.5M/sec Min	1.5M/sec Typ	1.5M/sec Max	3.0M/sec Min	3.0M/sec Typ	3.0M/sec Max	Units
T1	DRQ False from $\overline{\text{DACK}}$ True			130			60	ns
T2	$\overline{\text{DACK}}$ False to DRQ True	30			20			ns
T3	Write Enable Width	100			50			ns
T4	$\overline{\text{DACK}}$ Hold from End of $\overline{\text{IOW}}$	0			0			ns
T5	Data Setup to End of Write Enable	50			20			ns
T6	Data Hold Time from End of $\overline{\text{IOW}}$	40			20			ns
T7	Width of $\overline{\text{EOP}}$ Pulse	100			50			ns
T8	$\overline{\text{ACK}}$ True to $\overline{\text{REQ}}$ False			125			60	ns
T9	$\overline{\text{REQ}}$ from End of $\overline{\text{DACK}}$ ($\overline{\text{ACK}}$ False)			150			70	ns
T10	$\overline{\text{ACK}}$ True to DRQ True			110			50	ns
T11	$\overline{\text{REQ}}$ from End of $\overline{\text{ACK}}$ ($\overline{\text{DACK}}$ False)			150			70	ns
T12	SCSI DATA Hold Time from Write Enable	15			10			ns
T13	SCSI DATA Setup to $\overline{\text{REQ}}$ True	60			30			ns

Note: $\overline{\text{DACK}}$, $\overline{\text{IOW}}$, and $\overline{\text{EOP}}$ = 1, for at least T7 for $\overline{\text{EOP}}$ pulse recognition. Write enable is $\overline{\text{DACK}}$ and $\overline{\text{IOW}}$ occurrence.

3

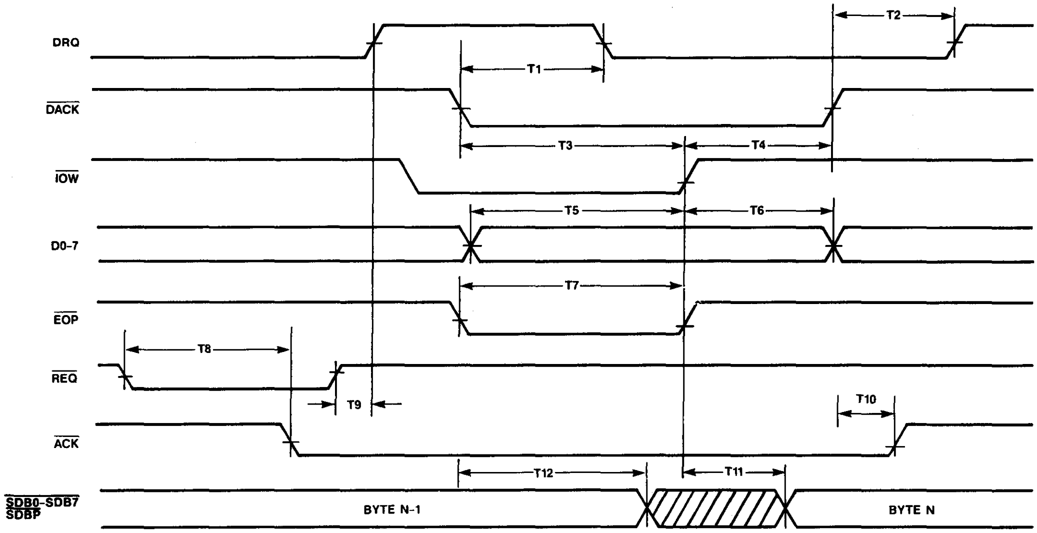
Figure 10. DMA Read (Non-Block Mode) Initiator Receive Timing



Name	Description	1.5M/sec			3.0M/sec			Units
		Min	Typ	Max	Min	Typ	Max	
T1	DRQ False from $\overline{\text{DACK}}$ True			130			60	ns
T2	$\overline{\text{DACK}}$ and $\overline{\text{IOR}}$ False to $\overline{\text{DRQ}}$ True	30			20			ns
T3	$\overline{\text{DACK}}$ Hold Time from End.of $\overline{\text{IOR}}$	0			0			ns
T4	Data Access Time from Read Enable			115			60	ns
T5	Data Hold Time from End of $\overline{\text{IOR}}$	20			10			ns
T6	Width of $\overline{\text{EOP}}$ Pulse	100			50			ns
T7	$\overline{\text{REQ}}$ True to DRQ True			150			70	ns
T8	$\overline{\text{DACK}}$ False to $\overline{\text{ACK}}$ ($\overline{\text{REQ}}$ False)			160			80	ns
T9	$\overline{\text{REQ}}$ True to $\overline{\text{ACK}}$ True			160			80	ns
T10	$\overline{\text{REQ}}$ False to $\overline{\text{ACK}}$ False ($\overline{\text{DACK}}$ False)			140			70	ns
T11	SCSI DATA Setup Time to $\overline{\text{REQ}}$	20			10			ns
T12	SCSI DATA Hold Time from $\overline{\text{REQ}}$	50			20			ns

Note: $\overline{\text{DACK}}$, $\overline{\text{IOR}}$, and $\overline{\text{EOP}}$ = 1, for at least T6 for $\overline{\text{EOP}}$ pulse recognition. Write enable is $\overline{\text{DACK}}$ and $\overline{\text{IOR}}$ occurrence.

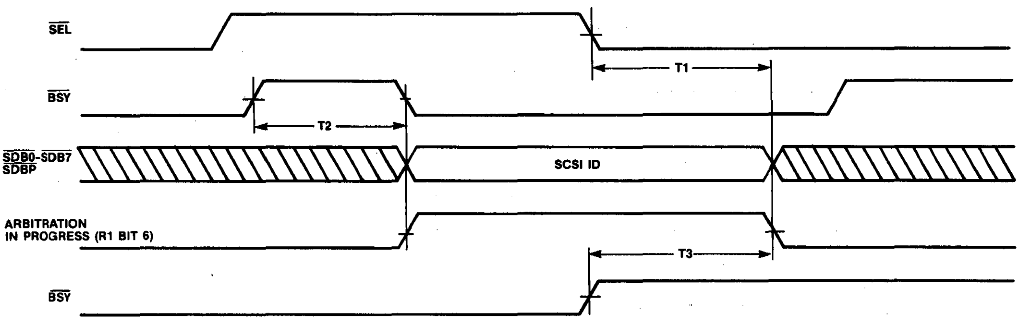
Figure 11. DMA Write (Non-Block Mode) Initiator Send Timing



Name	Description	1.5M/sec			3.0M/sec			Units
		Min	Typ	Max	Min	Typ	Max	
T1	DRQ False from $\overline{DACK}$ True			130			60	ns
T2	$\overline{DACK}$ False to DRQ True	30			20			ns
T3	Write Enable Width	100			50			ns
T4	$\overline{DACK}$ Hold from End of $\overline{IOW}$	0			0			ns
T5	Data Setup to End or Write Enable	50			20			ns
T6	Data Hold Time from End of $\overline{IOW}$	40			20			ns
T7	Width of $\overline{EOP}$ Pulse	100			50			ns
T8	$\overline{REQ}$ True to $\overline{ACK}$ True			160			80	ns
T9	$\overline{REQ}$ False to DRQ True			110			50	ns
T10	$\overline{DACK}$ False to $\overline{ACK}$ False			150			70	ns
T11	$\overline{IOW}$ False to Valid SCSI Data			100			50	ns
T12	DATA Hold Time from Write Enable	15			10			ns

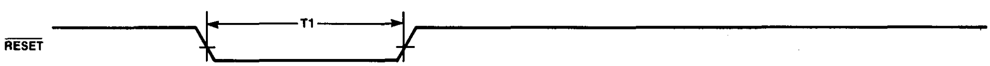
Note: $\overline{DACK}$, $\overline{IOW}$, and $\overline{EOP}$ = 1, *for at least T7 for* $\overline{EOP}$ pulse recognition. Write enable is $\overline{DACK}$ and $\overline{IOW}$ occurence.

Figure 12. Arbitration Timing



Name	Description	1.5M/sec			3.0M/sec			Units
		Min	Typ	Max	Min	Typ	Max	
T1	SCSI Bus Clear from $\overline{SEL}$ True			0.6			0.6	μs
T2	ARBITRATE Start from $\overline{BSY}$ False	1.2		2.2	1.2		2.2	μs
T3	SCSI Bus Clear from $\overline{BSY}$ False	0.4		1.1	0.4		1.1	μs

Figure 13. Reset Timing



Name	Description	1.5M/sec			3.0M/sec			Units
		Min	Typ	Max	Min	Typ	Max	
T1	Minimum Width of Reset	100			50			ns

3

PACKAGING

The Samsung KS53C80 SCSI controller is available in two packages. Figure 13 shows the dimensions of the 44-pin PLCC package. Figure 14 shows the dimensions of the 48-pin DIP package.

Figure 14. KS53C80 44-Pin PLCC Package

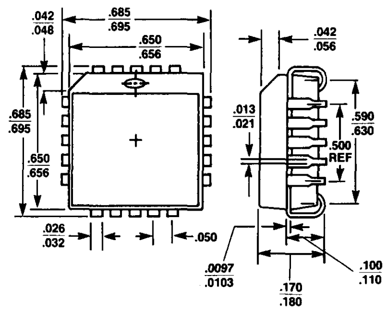
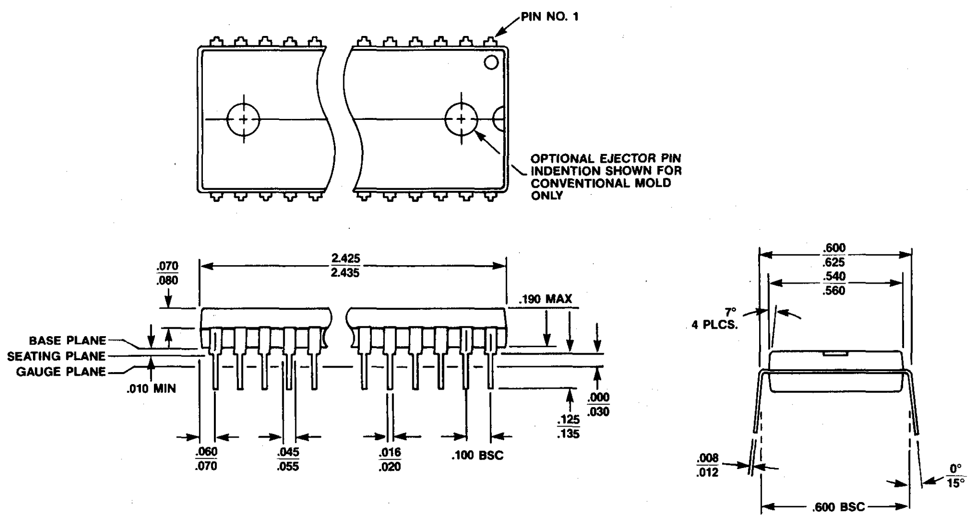


Figure 15. KS53C80 48-Pin DIP Package



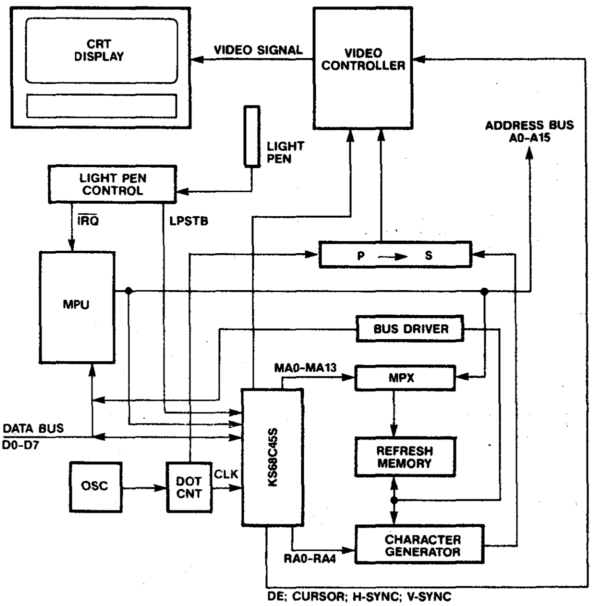
KS68C45S

CRT CONTROLLER

FEATURES/BENEFITS

- **Programmable:**
  - **— Number of characters displayed**
  - **— Interlace or non-interlace scan modes**
  - **— Cursor format and blink rate**
  - **— Cursor skew**
  - **— Horizontal and vertical SYNC signal**
  - **— Display timing**
- **3.7 or 6 MHz display operation**
- **Bufferless line refresh**
- **No DMA required**
- **Built-in light-pen detection function**
- **Supports paging and scrolling by page, line, or character**
- **TTL-compatible low-power CMOS**
- **512K address space for graphic systems**
- **16K refresh memory for character or semi-graphic displays**
- **Single +5V power supply**

Figure 1. System Block Diagram



DESCRIPTION

The KS68C45S CRT Controller (CRTC) provides an interface for computers to raster-scan type CRT displays. The Controller's data and control lines are fully compatible with the 6800 MPU. The Controller generates timing signals necessary for the raster-scan type CRT display based on specifications programmed into the Controller's registers.

Because it is programmable, the CRT Controller is capable of a wide-range of CRT display-types from small character displays up to raster-type full-graphic displays as well as large, limited-graphic displays.

Figure 2a: KS68C45S 44-Pin PLCC

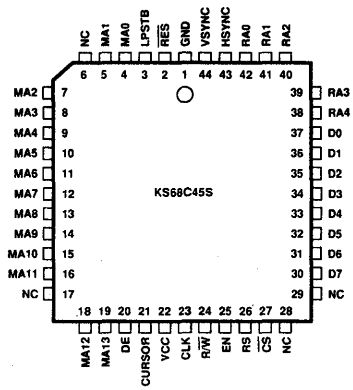


Figure 2b: KS68C45S Pin DIP

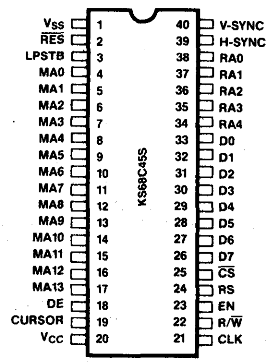


Table 1: KS68C45S Signal Descriptions

The CRTC provides 13 signals to the MPU and 25 interface signals to the CRT display.

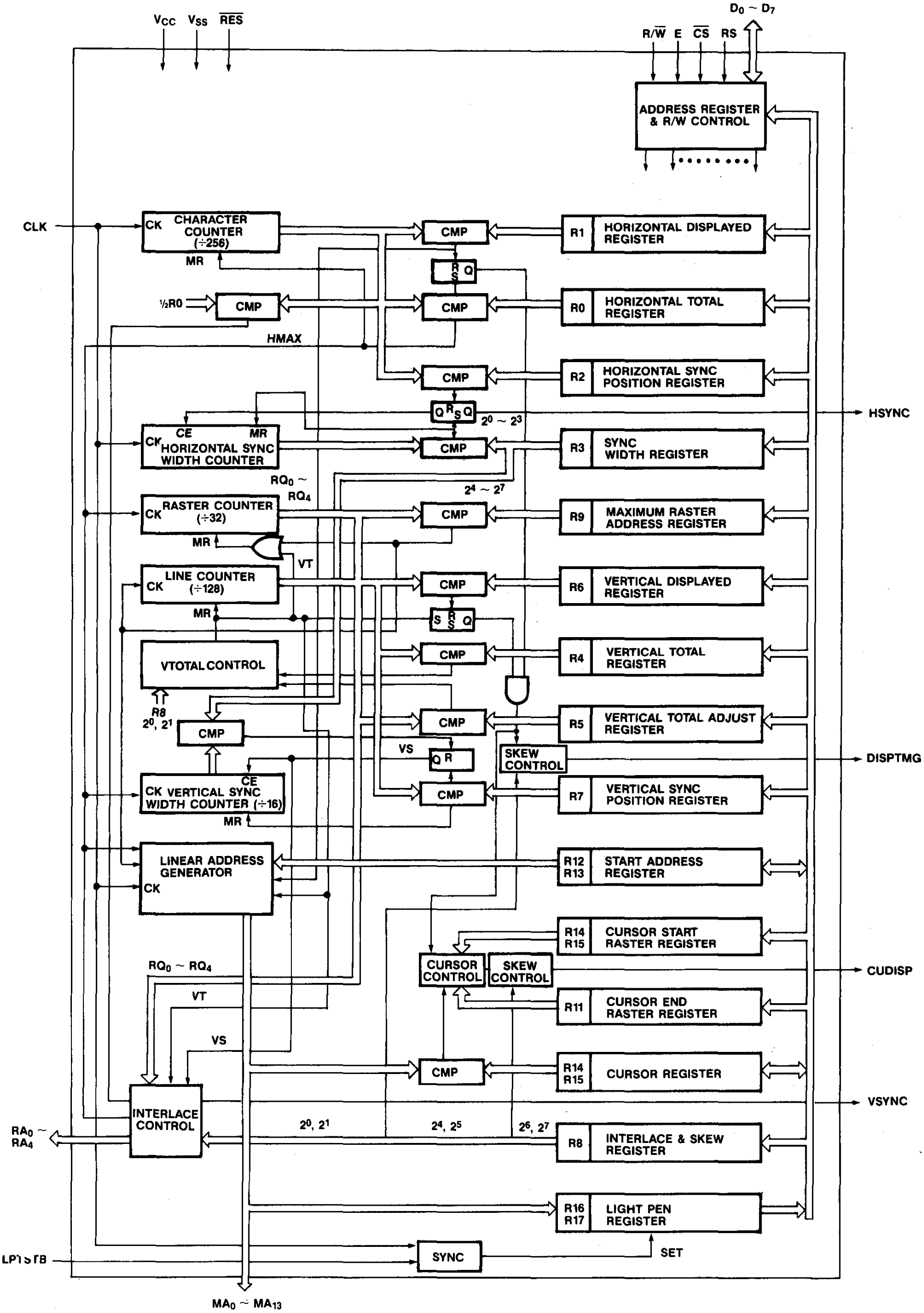
<table>
<tr><th>Symbol</th><th>Type</th><th>Name and Function</th></tr>
<tr><td colspan="3">Processor Interface</td></tr>
<tr><td>D_0–D_7</td><td>I/O</td><td>Bi-directional Data Lines: Used for data transfer between the CRTC and MPU. Outputs of the data bus are 3-state buffers that remain in the high-impedance state unless the MPU performs a CRTC read operation.</td></tr>
<tr><td>EN</td><td>I</td><td>Enable: Input which enables the data bus input/output buffers and clocks data to and from the CRTC. This signal is usually derived from the processor clock. The HIGH-to-LOW transition is the active edge.</td></tr>
<tr><td>$\overline{CS}$</td><td>I</td><td>Chip Select: Input which selects the CRTC, when LOW, to read or write to the internal register file. This signal should only be active when there is a valid stable address being decoded from the processor.</td></tr>
<tr><td>RS</td><td>I</td><td>Register Select: Input used to access internal registers. A LOW on this pin allows writes into the Address Register and allows reads from the Status Register. When HIGH, the data register is selected. The contents of the Address Register = the identity of the register accessed when RS is high.</td></tr>
<tr><td>R/$\overline{W}$</td><td>I</td><td>Read/Write: Input which determines whether the internal register file is written to (LOW) or read from (HIGH).</td></tr>
<tr><td>$\overline{RES}$</td><td>I</td><td>Reset: When LOW, forces the CRTC into the following status:
1) All counters in the CRTC are cleared and the device stops the display operation.
2) All outputs go LOW.
Control registers in the CRTC are not affected, and remain unchanged.
This signal has the following restrictions for usage:
1) $\overline{RES}$ is effective only when Light-Pen Strobe (LPSTB) is LOW.
2) The CRTC starts the display operation immediately after $\overline{RES}$ goes HIGH. Display Enable (DE) and the cursor are not active until after the first frame has been displayed.
The $\overline{RES}$ input and the LPSTB input are encoded as shown:
<table>
<tr><th>$\overline{RES}$</th><th>LPSTB</th><th>Operating Mode</th></tr>
<tr><td>0</td><td>0</td><td>Reset</td></tr>
<tr><td>0</td><td>1</td><td>Test Mode</td></tr>
<tr><td>1</td><td>0</td><td>Normal Mode</td></tr>
<tr><td>1</td><td>1</td><td>Normal Mode</td></tr>
</table>
After $\overline{RES}$ has gone LOW (and LPSTB = 0), MA_0–MA_{13} and RA_0–RA_4 will be driven low on the falling edge of CLK. $\overline{RES}$ must remain low for at least one cycle of the character clock (CLK).</td></tr>
</table>

3

Table 1: KS68C45S Signal Descriptions (Continued)

Symbol	Type	Name and Function
Internal Signals to the CRT Display		
CLK	I	**Character Clock:** A standard clock input signal which defines character timing for the CRTC display operation. This signal is normally derived from the external dot-timing logic.
H-SYNC	O	**Horizontal Sync:** Provides horizontal synchronization for the display device.
V-SYNC	O	**Vertical Sync:** Provides vertical synchronization for the display device.
DE	O	**Display Enable:** Defines the display period in horizontal and vertical raster scanning. When HIGH, this signal enables the video signal.
MA_0-MA_{13}	O	**Refresh Memory Address 0-13:** Used to address up to 16K-words of frame buffer for character storage and display refresh operations. The starting scan address is fully programmable and the ending scan address is determined by the total number of characters displayed, which is also programmable in terms of characters/line and lines/frame. The buffer can support up to 8 pages at 2000 characters per page.
RA_0-RA_4	O	**Raster Address 0-4:** Selects the raster of the character generator or graphic-pattern generator.
CURSOR	O	**Cursor:** Used to display the cursor on the CRT screen. This output is inhibited while DE is LOW. This output is normally mixed with the video signal. The cursor may be programmed to any character in the address field. Within the character, the cursor may be programmed to be any block of scan lines, since the start-scan line and the end-scan line are both programmable.
LPSTB	I	**Light Pen Strobe:** Edge-sensitive input which accepts a strobe pulse detected by the light-pen control circuit. When this signal is activated, the refresh memory address (MA_0-MA_{13}) is stored in the 14-bit light-pen register. Software must correct the stored refresh-memory address for the delay time of the display device, light pen, and light-pen control circuits.
V_{CC}		5V ± 5%.
V_{SS}		Ground.

Figure 3. CRTC Block Diagram



REGISTER DESCRIPTION

Table 2: Internal Registers Assignment

CS	RS	Address Register 4	3	2	1	0	Register #	Register Name	Program Unit	Read	Write	Data Bit 7	6	5	4	3	2	1	0
1	X	X	X	X	X	X			—	—	—								
0	0	X	X	X	X	X	AR	Address Register	—	X	O								
0	1	0	0	0	0	0	R0	Horizontal Total*	Character	X	O								
0	1	0	0	0	0	1	R1	Horizontal Displayed	Character	X	O								
0	1	0	0	0	1	0	R2	Horizontal Sync* Position	Character	X	O								
0	1	0	0	0	1	1	R3	Sync Width	Vertical-Raster, Horizontal-Character	X	O	wv3	wv2	wv1	wv0	wh3	wh2	wh1	wh0
0	1	0	0	1	0	0	R4	Vertical Total*	Line	X	O								
0	1	0	0	1	0	1	R5	Vertical Total Adjust	Raster	X	O								
0	1	0	0	1	1	0	R6	Vertical Displayed	Line	X	O								
0	1	0	0	1	1	1	R7	Vertical Sync* Position	Line	X	O								
0	1	0	1	0	0	0	R8	Interlace & Skew	—	X	O	C1	C0	D1	D0			V	S
0	1	0	1	0	0	1	R9	Maximum Raster Address	Raster	X	O								
0	1	0	1	0	1	0	R10	Cursor Start Raster	Raster	X	O		B	P					
0	1	0	1	0	1	1	R11	Cursor End Raster	Raster	X	O								
0	1	0	1	1	0	0	R12	Start Address (H)	—	O	O								
0	1	0	1	1	0	1	R13	Start Address (L)	—	O	O								
0	1	0	1	1	1	0	R14	Cursor (H)	—	O	O								
0	1	0	1	1	1	1	R15	Cursor (L)	—	O	O								
0	1	1	0	0	0	0	R16	Light Pen (H)	—	O	X								
0	1	1	0	0	0	1	R17	Light Pen (L)	—	O	X								

Notes:
1. The Registers marked *: (Written Value) = (Specified Value) - 1
2. Written Value of R9 is mentioned below.
   1) Non-interlace Mode
      Interlace Sync Mode (Written Value Nr) = (Specified Value) - 1
   2) Interlace Sync & Video Mode
      (Written Value Nr) = (Specified Value) - 2
3. C0 and C1 specify skew of CUDISP output signal.
   D0 and D1 specify skew of DISPTMG output signal.
   When S is "1", V specifies video mode. S specifies the Interlace Sync Mode.
4. B specifies the cursor blink. P specifies the cursor blink period.
5. wv0 ~ wv3 specify the pulse width of Vertical Sync Signal.
   wh0 ~ wh3 specify the pulse width of Horizontal Sync Signal.
6. R0 is ordinally programmed to be odd number in interlace mode.
7. O: Yes, X; No
8. The X bits are don't care.

FUNCTIONAL DESCRIPTION

The KS68C45S CRT Controller consists of programmable horizontal and vertical timing generators, a programmable linear address register, programmable cursor logic, a light-pen capture register, and control circuitry for interface to a processor bus.

All CRTC timing is derived from the CLK, usually the output of an external dot-race counter. Coincidence circuits continuously compare counter contents to the contents of the programmable register file, R_0-R_{17}. For horizontal timing generation, comparisons result in: 1) horizontal synch pulse (H-SYNC) of a frequency, position, and width determined by the registers; and 2) horizontal display signal of a frequency, position, and duration determined by the registers.

The horizontal counter produces H clock which drives the scan-line counter and vertical control. The contents of the raster counter are continuously compared to the maximum scan-line address register. A coincidence resets the raster counter and clocks the vertical counter.

Comparisons of vertical counter contents and vertical registers result in: 1) vertical sync pulse (V-SYNC) of a frequency and position determined by the registers; and, 2) vertical display signal of a frequency and position determined by the registers.

The vertical control logic has two other functions:

1) To generate row selects, RA_0-RA_4, from the raster counter for the corresponding interface or non-interlace modes.
2) To extend the number of scan lines in the vertical total by the amount programmed in the vertical-total adjust register.

The linear address generator is driven by the CLK and locates the relative positions of characters in memory with their positions on the screen. Fourteen lines, MA_0-MA_{13}, are available for addressing four pages of 4K characters each, eight pages of 2K characters each, or any combination totalling 16K characters. The linear address generator repeats the same sequence of addresses for each scan line of a character row.

The cursor logic determines the cursor location, size, and clock rate on the screen. These features are all programmable.

The light-pen strobe going HIGH causes the current contents of the address counter to be latched in the light-pen register. The contents of the light-pen register are subsequently read by the processor.

Internal CRT Controller registers are programmed by the processor through the data bus, D_0-D_7, and the control signals: R/$\overline{W}$, $\overline{CS}$, RS, and EN.

OPERATIONAL DESCRIPTION

Control Modes

There are four control modes:

1) Non-interlace Mode
2) Interlace Sync Mode
3) Interlace Sync and Video Mode (even)
4) Interlace Sync and Video Mode (odd)

Non-Interlace Mode

In Non-Interlace Mode each field is scanned twice, and addresses RA_0-RA_4 are counted up one, from zero.

Interlace Sync Mode

In Interlace Sync Mode, the raster address in the even and odd fields is the same as that addressed in the Non-Interlace Mode. One character pattern is displayed in both fields, but, the displayed position of that character is 1/2 the raster space down from its position in the even field.

Interlace Sync and Video Mode (even)

TRN (total number of rasters) is programmed to be even. An even-field is output by even raster-addressing.

Interlace Sync and Video Mode (odd)

TRN is programmed to be odd. An odd-field is output by odd raster-addressing. Odd and even addresses are reversed to the odd and even lines in each field. This reversal creates a more stable interlace display than when TRN is programmed even.

Cursor Control

Start and end values are programmed to the raster register and must meet the condition Cursor Start $\leq$ Cursor End $\leq$ Maximum raster address register.

Internal Registers

Internal registers are:

Register Symbol	Register Name
AR	Address Register
R_0	Horizontal Total Register
R_1	Horizontal Displayed Register
R_2	Horizontal Sync Position Register
R_3	Sync Width Register
R_4	Vertical Total Register
R_5	Vertical Total Adjust Register
R_6	Vertical Displayed Register
R_7	Vertical Sync Position Register
R_8	Interlace and Skew Register
R_9	Maximum Raster Address Register
R_{10}	Cursor Start Raster Register
R_{11}	Cursor End Raster Register
R_{12}, R_{13}	Start Address Register
R_{14}, R_{15}	Cursor Register
R_{16}, R_{17}	Light Pen Register

Table 3: Functional Description of Internal Registers

AR — Address Register

A 5-bit register used to select the internal control registers (R_0-R_{17}). This register is the address of one of the control registers. In order to access the control registers, the address of the control register must be written to the Address Register. (Programming data from binary 8 to binary 13 into the Address Register produces no results.)

To select AR, RS and $\overline{CS}$ must equal 0.

R_0 — Horizontal Total Register

An 8-bit register used to program the total number of horizontal characters per line. This number must include the retrace period and is programmed according to the CRT specification. If N is the total number of characters, N-1 is programmed to this register. N must be even for the Interlace Mode.

R_1 — Horizontal Displayed Register

An 8-bit register used to program the number of horizontal displayed characters per line. Any number less than the total number of horizontal characters can be programmed.

R_2 — Horizontal Sync Position Register

An 8-bit register used to program the horizontal sync position as a multiple of the character clock period. Any number less than the total horizontal number can be programmed. If H is the character number of the horizontal sync position, H-1 is programmed to this register.

The value of this register determines the optimum horizontal position. The display position on the CRT screen moves to the left if the programmed value of this register is increased. The display position on the CRT screen moves to the right if the programmed value of this register is decreased.

R_3 — Sync Width Register

7							0
V	V	V	V	H	H	H	H

An 8-bit register used to program the horizontal and vertical sync pulse width. The horizontal sync (H-SYNC) width is programmed to the least-significant 4 bits of R_3 as multiples of the character clock period. Zero cannot be programmed. The vertical sync (V-SYNC) is programmed to the most-significant 4 bits of R_3 as multiples of the raster period. If 0 is programmed in the most-significant 4 bits, a raster period of 16 (16H) is specified.

Table 4: Raster Scan Mode

Raster Scan Mode (2^1, 2^0)	V	S
Non-Interlace Mode	0 1	0 0
Interlace Sync Mode	0	1
Interlace Sync & Video Mode	1	1

R_4 — Vertical Total Register

A 7-bit register used to program the total number of lines per frame, including the vertical retrace period. This register must be programmed according to the CRT specification. If L is the total number of lines, L-1 is programmed to this register.

R_5 — Vertical Total Adjust Register

A 5-bit register used to program the optimum number to adjust the total number of rasters per field. This register is also used to decide the vertical deflection frequency.

R_6 — Vertical Displayed Register

A 7-bit register used to program the number of displayed character rows on the CRT screen. Any number less than the total number of vertical characters can be programmed.

R_7 — Vertical Sync Position Register

A 7-bit register used to program the vertical sync position on the screen as multiples of the horizontal character line period. Any number less than the total number of vertical characters can be programmed. If V is the character number of the vertical sync position, V-1 is programmed to this register.

If the programmed value of this register is decreased, the display position is moved down on the CRT screen. If the programmed value of this register is increased, the display position is moved up on the screen.

Table 5: Pulse Width of Vertical Sync Signal

Vertical Sync Signal

Pulse Width	VSW			
	2^7	2^6	2^5	2^4
16H	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

H: Raster Period

Table 6: Pulse Width of Horizontal Sync Signal

Horizontal Sync Signal

Pulse Width	HSW			
	2^3	2^2	2^1	2^0
—	0	0	0	0
1 CH	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

CH: Character Clock Period
HSW = 0 cannot be used

R_8 — Interlace and Skew Register

7							0
C1	C0	D1	D0			V	S

An 8-bit register used to program the raster scan mode, the skew of CURSOR, and Display Enable (DE).

In Table 7, bits 4 and 5 specify DE output delay (skew). Bits 6 and 7 specify CURSOR output delay (skew) in two characters, starting from 0. If 3 is programmed to these bits, the signal is not output.
Bits 2 and 3 are not used.
Bits 0 and 1 (V, S) specify scan modes.

3

Table 7: DE and Cursor Skew

DE Skew (2^5, 2^4)	D0	D1
Non-skew	0	0
One-character skew	1	0
Two-character skew	0	1
Non-output	1	1
Cursor Skew Bits (2^7, 2^6)	**C0**	**C1**
Non-skew	0	0
One-character skew	1	0
Two-character skew	0	1
Non-output	1	1

R_9 — Maximum Raster Address Register

A 5-bit register used to program the maximum raster address and to define the total number of rasters per character, including line space.

In Interlace Sync Mode where TNR equals the Total Number of Rasters, TNR equals 5. Where Nr equals the raster number and equals the programmed value, Nr equals 4. Where X equals TNR, X - 1 is programmed.

In Non-interlace Mode, TNR = 5, Nr = 4, X - 2 is programmed.

In Interlace and Video Mode, TNR = 5, Nr = 3, X - 1 is programmed.

R_{10} — Cursor Start Raster Register

7							0
\	B	P					

A 7-bit register. The cursor start raster address is programmed in the least-significant 5 bits. The cursor display mode is programmed to the most-significant 2 bits.

Table 8: Cursor Display Mode

Cursor Display Mode (2^6, 2^5)	B	P
Non-blink	0	0
Cursor Non-display	0	1
Blink 16 Field Period	1	0
Blink 32 Field Period	1	1

R_{11} — Cursor End Raster Register

A 5-bit register used to program the cursor end raster address.

R_{12}, R_{13} — Start Address Register

The two registers form a single 16-bit register used to program the first address to be read out of refresh memory, and used to program for paging and scrolling. The most significant two bits of R_{12} are always 0.

R_{14}, R_{15} — Cursor Register (Read/Write)

The two registers form a single 16-bit register used to store the cursor location. The most significant two bits of R_{14} are always 0.

R_{16}, R_{17} — Light-Pen Register (Read Only)

The two registers form a single 16-bit register used to store the detected address of the light pen. The most significant two bits of R_{16} are always 0.

Table 9: Programmed Values into the Registers

Register Name	Register	Value
Horizontal Total Horizontal Displayed Horizontal Sync Position	R0 R1 R2	Nht Nhd Nhsp
Sync Width	R3	Nvsw, Nhsw
Vertical Total Vertical Total Adjust Vertical Displayed Vertical Sync Position	R4 R5 R6 R7	Nvt Nadj Nvd Nvsp
Interlace & Skew Max. Raster Address	R8 R9	 Nr
Cursor Start Raster Cursor End Raster	R10 R11	
Start Address (H) Start Address (L)	R12 R13	0 0
Cursor (H) Cursor (L)	R14 R15	
Light Pen (H) Light Pen (L)	R16 R17	

Table 10: Raster Address Output

No. of Rasters in a Line		Odd Field	Even Field
Even		Odd Address	Even Address
Odd	Odd Line	Even Address	Odd Address
	Even Line	Odd Address	Even Address

Restrictions on Internal Register Programming

$0 \leq Nhsp \leq Nht$
$0 \leq Nvsp \leq Nvt$ (see note 1)
$0 < Nhd < Nht + 1 \leq 256$
$0 < Nvd < Nvt + 1 \leq 128$
$0 \leq Ncs \leq Nce \leq Nr$ (for Non-interlace and Interlace Sync Modes)
$0 \leq Ncs \leq Nce \leq Nr + 1$ (for Interlace Sync and Video Mode)
$2 \leq Nr \leq 30$ (Interlace Sync and Video Mode)
$3 \leq Nht$ (not for Non-Interlace Mode)
$5 \leq Nht$ (Non-interlace Mode only)

Notes:
1. The pulse width is changed ±1/2 the raster time when the vertical sync signal extends over two fields in the Interlace Mode.
2. Ncs = Cursor start, Nce = Cursor end

Figure 4: Video Signal and Character Display

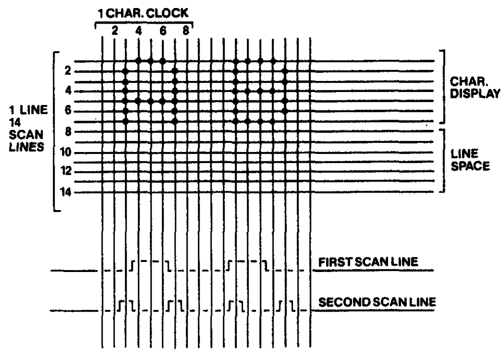
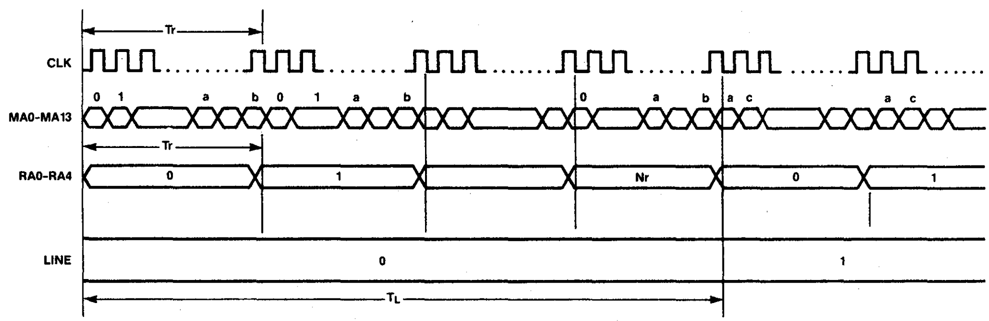


Figure 5: Raster Line Period Timing Chart



Notes:
Tr = Raster Period
T_L = Line Period = (Nr + 1) * Tr
a = Nhd
b = Nht
c = Nhd + 1
Nr = Max. Raster Address

Figure 6: CRT Screen Format

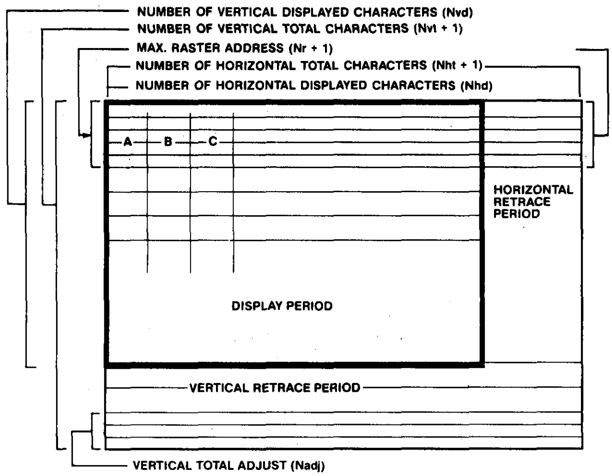
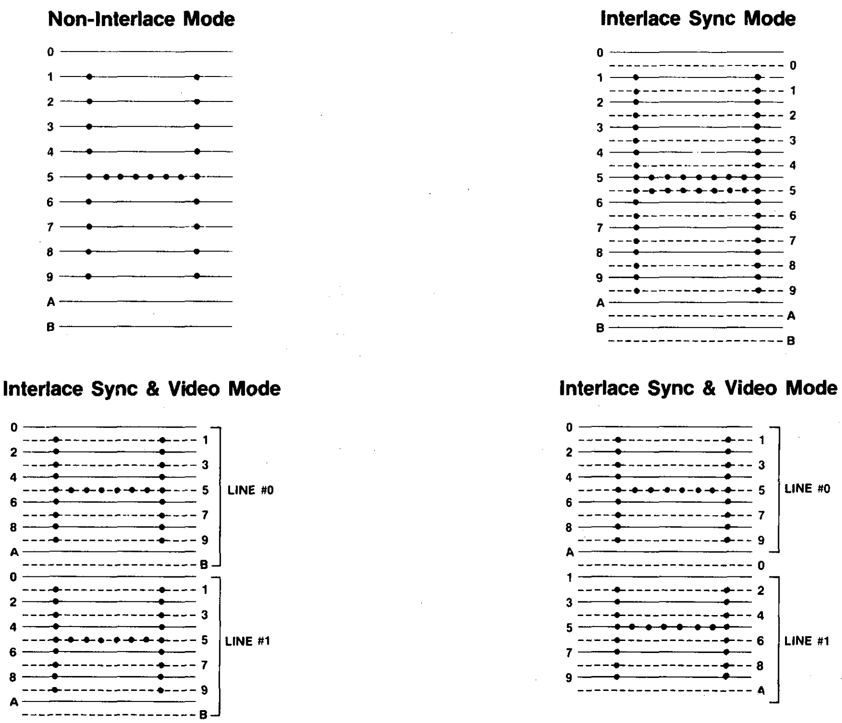


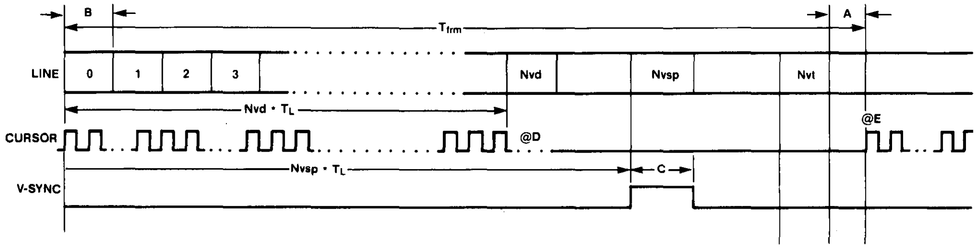
Figure 7: Raster Scan Display



Total number of rasters in a line is even.

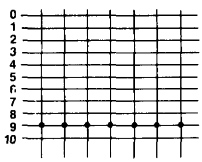
Total number of rasters in a line is odd.

Figure 8: Vertical Timing Chart

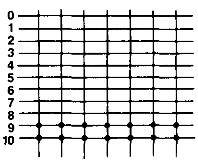


Note:
Nvd = Number of vertical displayed characters
Nvsp = Vertical sync position
Nvt = Number of vertical total characters
Tadj = Nadj * Tr = Fine adjustment period of frame
Tvsw = Nvsw * Tr = Vertical sync pulse width
T_{frm} = (Nvt + 1) * T_L + Tadj = Frame period
A = T_{adj}
B = T_L
@D = See Fig. 9a for the expansion of this region
@E = See Fig. 9b for the expansion of this region

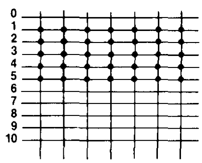
Figure 9: Cursor Control



Cursor Start Address = 9
Cursor End Address = 9



Cursor Start Address = 9
Cursor End Address = 10



Cursor Start Address = 1
Cursor End Address = 5

Figure 10:

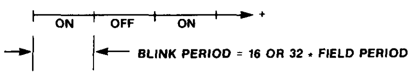
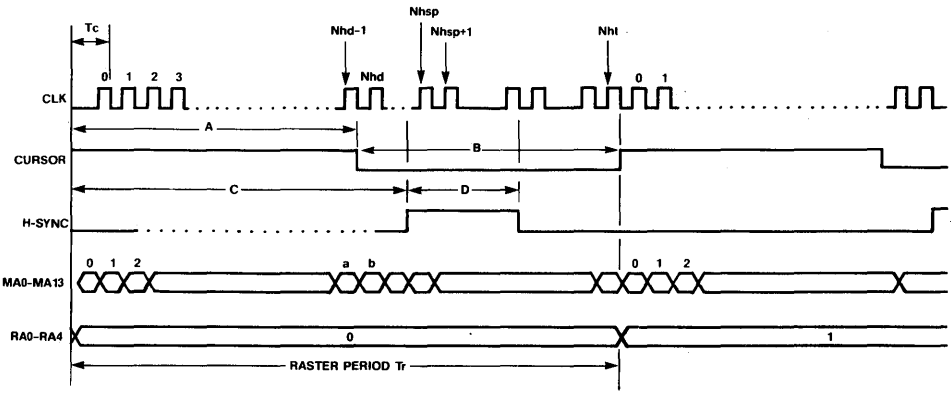
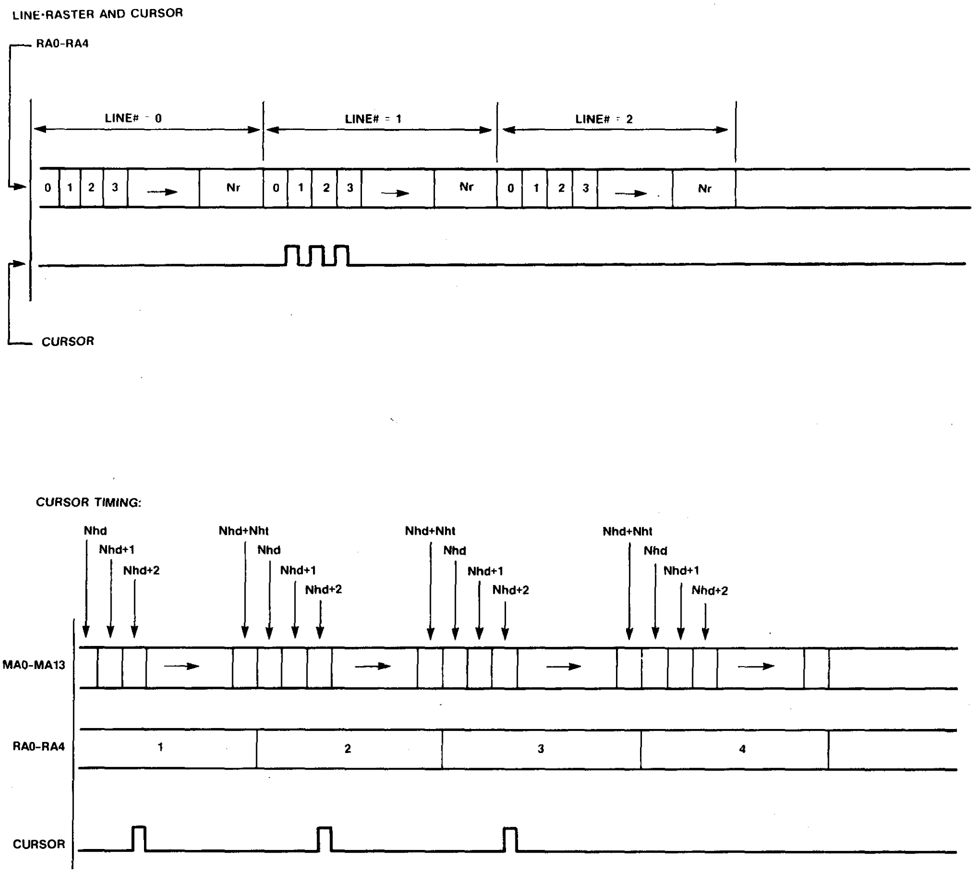


Figure 11: Horizontal Timing Chart



Notes:
Tc = Character clock period
A = Horizontal display period Nht - Tc
B = Horizontal Retrace Period
C = Nhsp * Tc
D = Nhsw * Tc
a = Nhd - 1
b = Nhd
Nhd = Number of Horizontal Displayed Characters
Nhsp = Horizontal Sync Position
Nht = Number of Horizontal Total Characters
Tr = Raster Period = (Nht + 1) * Tc

Figure 12a: Cursor Timing



Note:

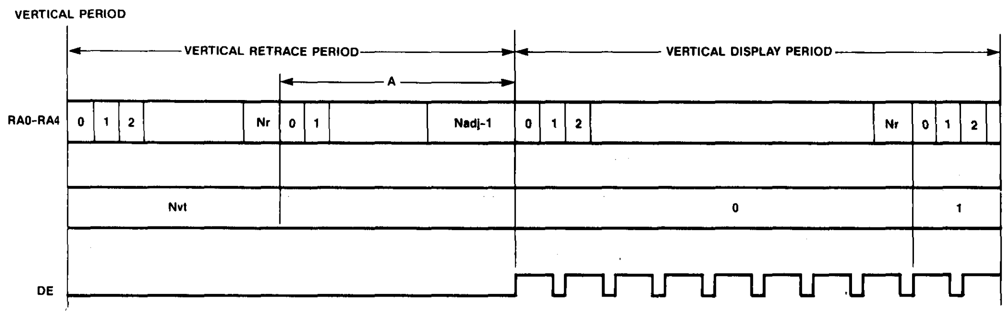
The following are programmed in Cursor Display Mode:

Cursor Start: Raster Register = 1. Cursor End: Raster Register = 3

Cursor Register = Nhd + 2

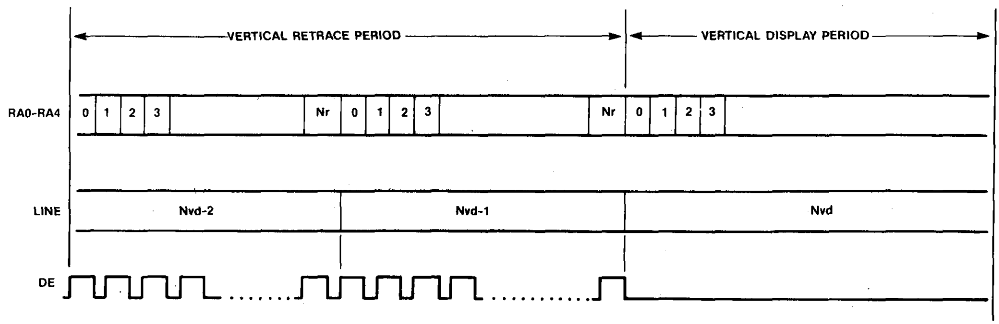
In Blink mode: When field period is 16 or 32 time period, it is changed into display or non-display mode.

Figure 12b: Fine Adjustment Period of Frame



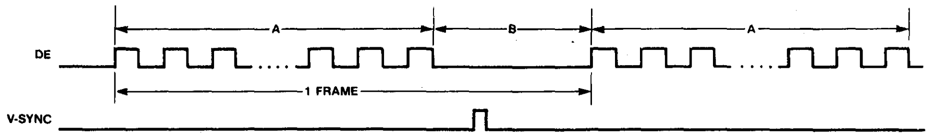
Note:
A = Fine adjustment period of Frame Period.
Tadj = Nadj • Tr

Figure 13a: Switching from Vertical Period to Vertical Retrace Period



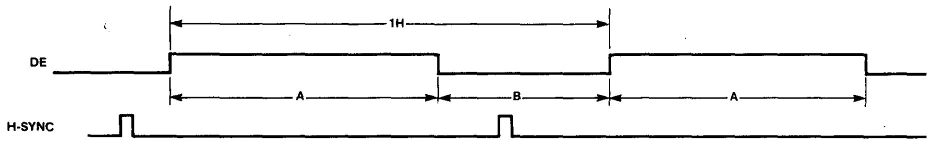
Notes:
A = Fine adjustment period of Frame Period.
Tadj = Nadj • Tr

Figure 13b: V-Sync Timing Chart



Notes:
A = Vertical Display Period
B = Vertical Retrace Period

Figure 13c: H-Sync Timing Chart



Notes:
A = Horizontal Display Period
B = Horizontal Retrace Period

Figure 14: Refresh Memory Addressing (MA0-MA13) Stage Chart

	HORIZONTAL DISPLAY (1 CHAR.)				HORIZONTAL RETRACE PERIOD (NON DISPLAY)		
0 [0 ↓ Nr]	0 ↓↑ 0	1 ↓↑ 1	→	Nhd-1 ↓↑ Nhd-1	Nhd ↓↑ Nhd	→	Nht ↓↑ Nht
1 [0 ↓ Nr]	Nhd ↓↑ Nhd	Nhd+1 ↓↑ Nhd+1	→	2•Nhd-1 ↓↑ 2•Nhd-1	2•Nhd ↓↑ 2•Nhd	→	Nhd+Nht ↓↑ Nhd+Nht
2 [0 ↓ Nr]	2•Nhd ↓↑ 2•Nhd	2•Nhd+1 ↓↑ 2•Nhd+1	→	3•Nhd-1 ↓↑ 3•Nhd-1	3•Nhd ↓↑ 3•Nhd	→	2Nhd+Nht ↓↑ 2Nhd+Nht
	↓	↓		↓	↓		↓
Nvd-1 [0 ↓ Nr]	(Nvd-1)Nhd ↓↑ (Nvd-1)Nhd	(Nvd-1)Nhd+1 ↓↑ (Nvd-1)Nhd+1	→	Nvd•Nhd-1 ↓↑ Nvd•Nhd-1	Nvd•Nhd ↓↑ Nvd•Nhd	→	(Nvd-1)Nhd+Nht ↓↑ (Nvd-1)Nhd+Nht
Nvd [0 ↓ Nr]	Nvd•Nhd ↓↑ Nvd•Nhd	Nvd•Nhd+1 ↓↑ Nvd•Nhd+1	→	(Nvd+1)Nhd-1 ↓↑ (Nvd+1)Nhd-1	(Nvd+1)Nhd ↓↑ (Nvd+1)Nhd	→	Nvd•Nhd+Nht ↓↑ Nvd•Nhd+Nht
Nvt [0 ↓ Nr]	Nvt•Nhd ↓↑ Nvt•Nhd	Nvt•Nhd+1 ↓↑ Nvt•Nhd+1	→	(Nvt+1)Nhd-1 ↓↑ (Nvt+1)Nhd-1	(Nvt+1)Nhd ↓↑ (Nvt+1)Nhd	→	Nvt•Nhd+Nht ↓↑ Nvt•Nhd+Nht
0 ↓ Nadj-1	(Nvt+1)Nhd ↓↑ (Nvt+1)Nhd	(Nvt+1)Nhd+1 ↓↑ (Nvt+1)Nhd+1	→	(Nvt+2)Nhd-1 ↓↑ (Nvt+2)Nhd-1	(Nvt+2)Nhd ↓↑ (Nvt+2)Nhd	→	(Nvt+2)Nhd+Nht ↓↑ (Nvt+2)Nhd+Nht

Notes:
0 — Nr; 0 — Nadj = Raster Address
0, 1, 2 — Nvd-1 = Line Number
0 — Nvd-1 = Vertical Display Period
Nvd — Nadj-1 = Vertical Display Period
Thick line square indicates valid refresh memory address (0 → Nvd•Nhd-1). Refer to Cursor Timing.

Table 11: DC Characteristics
V_{CC} = 5.0V ± 5%, V_{SS} = 0V, T_A = -20°C to 75°C

Item	Symbol	Test Condition	Min	Typ	Max	Unit
Input High Voltage	V_{IH}		2.0	—	V_{CC}	V
Input Low Voltage	V_{IL}		-0.3	—	0.8	V
Input Leakage Current	I_{IN}	V_{IN}[a] = 0V - 5.25V	-2.5	—	2.5	μA
3-State Input Current (Off-State)	I_{TSI}	V_{IN} = 0.4V - 2.4V V_{CC}[b] = 5.25V	-10	—	10	μA
Output High Voltage	V_{OH}	I_{LOAD}[b] = -205μA I_{LOAD}[c] = -100μA	2.4	—	—	V
Output Low Voltage	V_{OL}	I_{LOAD} = 1.6mA	—	—	0.4	V
Input Capacitance	C_{IN}	V_{IN} = 0V F = 1.0MHz, T_A = 25°C—	— —	— 10.0	12.5[c] pF	pF
Output Capacitance	C_{OUT}	V_{IN} = 0V F = 1.0MHz, T_A = 25°C	—	—	10.0	pF
Power Dissipation	P_D		—	600	1000	mW

Typical Condition: T_A = 25°C, V_{CC} = 5.0V

Note:
(a) = Except D0-D7
(b) = D0-D7
(c) = Other Inputs

Table 12: AC Characteristics

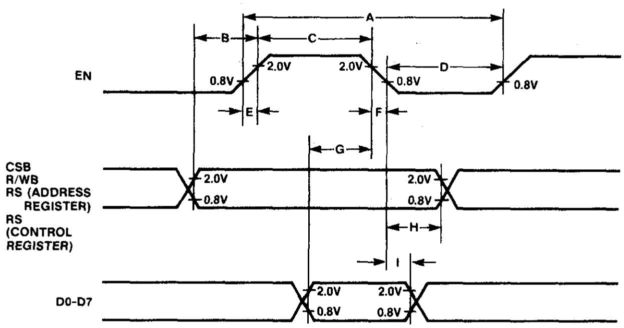
Item	Symbol	Test Condition	3.7 MHz			6 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
CRTC Timing									
Light Pen Strobe Pulse Width	PW_{LPH}		60	—	—	60	—	—	ns
Light Pen Strobe	T_{LPD1}		—	—	70	—	—	70	ns
Uncertain Time of Acceptance	T_{LPD2}		—	—	0	—	—	0	ns
Raster Address Delay Time	T_{RAD}		—	—	160	—	—	105	ns
Memory Address Delay Time	T_{MAD}		—	—	160	—	—	105	ns
DE Delay Time	T_{DTD}		—	—	250	—	—	165	ns
CURSOR Delay Time	T_{CDD}		—	—	250	—	—	165	ns
V-SYNC Delay Time	T_{VSD}		—	—	250	—	—	165	ns
Horizontal Sync Delay Time	T_{HSD}		—	—	200	—	—	132	ns
Rise and Fall Time for CLK Input	T_{CR}, T_{CF}		—	—	20	—	—	14	ns
Clock Low Pulse Width	PW_{CL}		130	—	—	86	—	—	ns
Clock High Pulse Width	PW_{CH}		130	—	—	86	—	—	ns
Clock Cycle Time	T_{CYC}		270	—	—	178	—	—	ns

Table 12: AC Characteristics (Continued)

Item	Symbol	Test Condition	3.7 MHz			6 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
MPU Write Timing									
Enable Cycle Time	T_{CYCE}		1.0	—	—	0.375	—	—	μs
Enable High Pulse Width	PW_{EH}		0.45	—	—	0.165	—	—	μs
Enable Low Pulse Width	PW_{EL}		0.40	—	—	0.158	—	—	μs
Enable Rise and Fall Time	T_{ER}, T_{EF}		—	—	25	—	—	15	ns
Address Setup Time	T_{AS}		140	—	—	30	—	—	ns
Data Setup Time	T_{DSW}		195	—	—	45	—	—	ns
Data Hold Time	T_H		10	—	—	10	—	—	ns
Address Hold Time	T_{AH}		10	—	—	10	—	—	ns
MPU Read Timings									
Enable Cycle Time	T_{CYCE}		1.0	—	—	0.375	—	—	μs
Enable High Pulse Width	PW_{EH}		0.45	—	—	0.165	—	—	μs
Enable Low Pulse Width	PW_{EL}		0.40	—	—	0.158	—	—	μs
Enable Rise and Fall Time	T_{ER}, T_{EF}		—	—	25	—	—	15	ns
Address Setup Time	T_{AS}		140	—	—	30	—	—	ns
Enable Data Delay	T_{DDR}		—	—	320	—	—	90	ns
Data Hold Time	T_H		10	—	—	10	—	—	ns
Address Hold Time	T_{AH}		10	—	—	10	—	—	ns
Data Access Time	T_{ACC}		—	—	460	—	—	120	ns

V_{CC} = 5V ± 5%, T_A = -20°C to 75°C

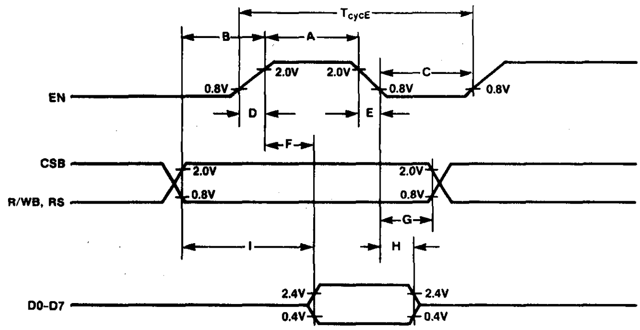
Figure 15: Write Timing Sequence



Notes:

A = T_{cycE}
B = T_{AS}
C = PW_{EH}
D = PW_{EL}
E = T_{Er}
F = T_{Ef}
G = T_{DSW}
H = T_{AH}
I = T_H

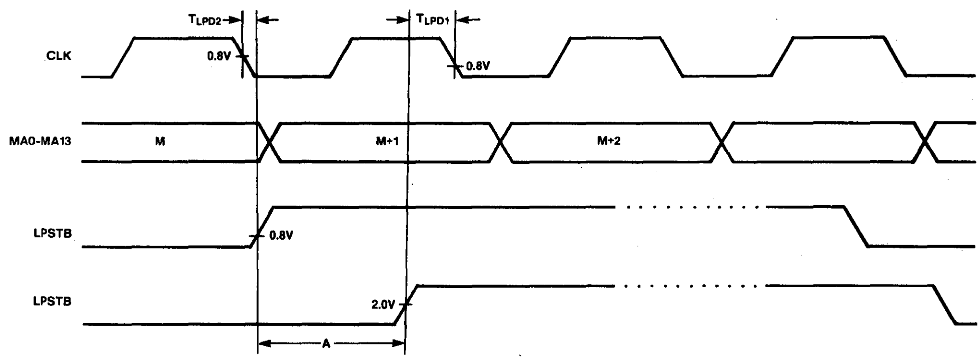
Figure 16: Read Sequence



Notes:

A = PW_{EH}
B = T_{AS}
C = PW_{EL}
D = T_{Er}
E = T_{Ef}
F = T_{DDR}
G = T_{AH}
H = T_H
I = T_{ACC}

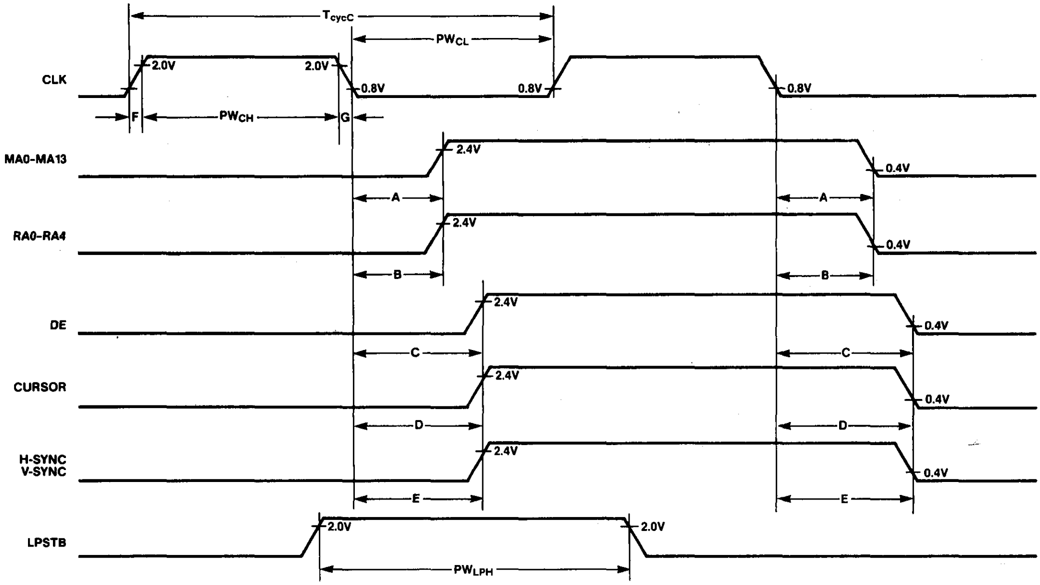
Figure 17: CLK, MA0-MA13, and LPSTB Timing



Note:

A — Sets Refresh Memory Address (M+2) into the light pen registers.

Figure 18: CRTC Timing Chart

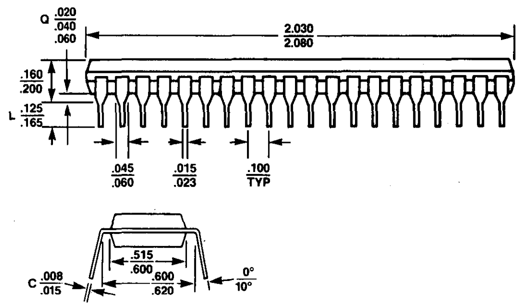


Notes:

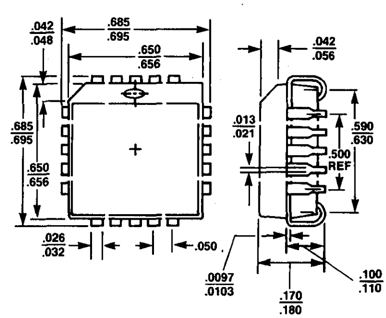
A = T_{MAD}
B = T_{RAD}
C = T_{DTD}
D = T_{CDD}
E = T_{HSD}
F = T_{CR}
G = T_{CF}

PACKAGE DIMENSIONS

40-pin DIP



44-pin PLCC



ORDERING INFORMATION AND PRODUCT CODE

KS 68C45S X X X

- **KS** — **SAMSUNG SEMICONDUCTOR**
- **68C45S** — **Part Number**
- **X** — **Speed**
  - -4 4MHz
  - -6 6MHz
- **X** — **Temperature**
  - C — Commercial (0°C to +70°C)
  - I — Industrial (-40°C to +85°C)
- **X** — **Packaging**
  - P — Plastic DIP
  - L — Plastic Leaded Chip Carrier (PLCC)

SAMSUNG products are designated by a Product Code. When ordering, please refer to products by their full code. For unusual, and/or specific packaging or processing requirements not covered by the standard product line, please contact the SAMSUNG MOS Product Group.

KS82C37A

PROGRAMMABLE DMA CONTROLLER

FEATURES/BENEFITS

- **Pin and functional compatibility with the industry standard 8237/8237A**
- **High Speed — 5MHz, 8MHz and 10MHz versions available**
- **Four independent maskable DMA channels with autoinitialize capability**
- **Independent polarity control for DREQ and DACK signals**
- **Address increment or decrement selection**
- **Cascadable to any number of channels**
- **Memory-to-memory transfer**
- **Fixed or rotating DMA request priority**
- **Low power CMOS implementation**
- **TTL input/output compatibility**
- **8080/85, 8086/88, 80186/286/386 compatible**

DESCRIPTION

The KS82C37A is a high performance, programmable Direct Memory Access (DMA) controller offering pin-for-pin functional compatibility with the industry standard 8237/8237A. It features four channels, each independently programmable, and is cascadable to any number of channels. Each channel can be programmed to autoinitialize following DMA termination.

In addition, the KS82C37A supports both memory-to-memory transfer capability and memory block initialization, as well as a programmable transfer mode.

The KS82C37A is manufactured using a proven CMOS technology to produce a powerful, reliable product. It is designed to improve system performance by allowing external devices to transfer data directly from the system memory. High speed and very low power consumption make it an attractive addition in portable systems or systems with low power standby modes.

3

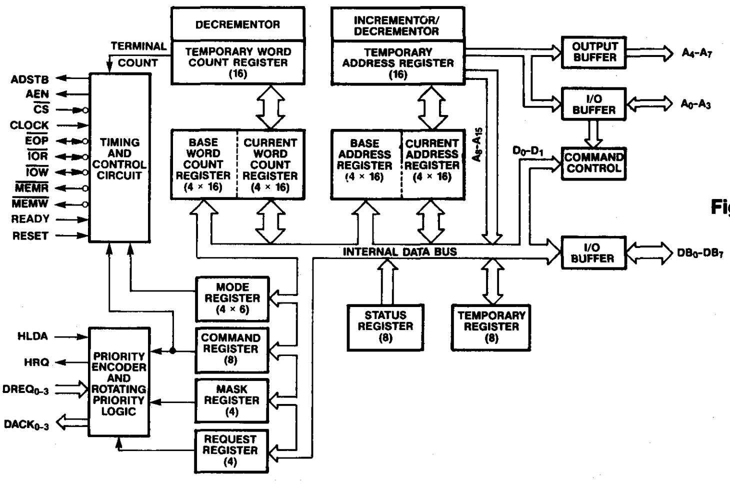


Figure 1: KS82C37A Block Diagram

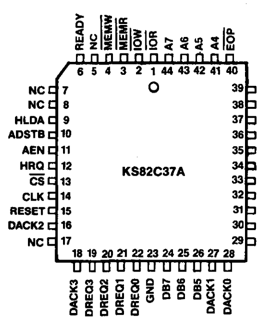


Figure 2: 44 Pin PLCC Configuration

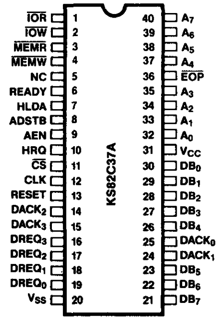


Figure 3: 40 Pin DIP

Table 1a: 40-Pin DIP Pin Assignment

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
1	$\overline{IOR}$	8	ADSTB	15	$DACK_3$	22	DB_6	29	DB_1	36	$\overline{EOP}$
2	$\overline{IOW}$	9	AEN	16	$DREQ_3$	23	DB_5	30	DB_0	37	A_4
3	$\overline{MEMR}$	10	HRQ	17	$DREQ_2$	24	$DACK_1$	31	V_{CC}	38	A_5
4	$\overline{MEMW}$	11	$\overline{CS}$	18	$DREQ_1$	25	$DACK_0$	32	A_0	39	A_6
5	N.C.	12	CLK	19	$DREQ_0$	26	DB_4	33	A_1	40	A_7
6	READY	13	RESET	20	V_{SS}	27	DB_3	34	A_2		
7	HLDA	14	$DACK_2$	21	DB_7	28	DB_2	35	A_3		

Table 1b: 44-Pin PLCC Pin Assignment

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
1	$\overline{IOR}$	9	HLDA	17	N.C.	25	DB_6	33	DB_1	41	A_4
2	$\overline{IOW}$	10	ADSTB	18	$DACK_3$	26	DB_5	24	DB_0	42	A_5
3	$\overline{MEMR}$	11	AEN	19	$DREQ_3$	27	$DACK_1$	35	V_{CC}	43	A_6
4	$\overline{MEMW}$	12	HRQ	20	$DREQ_2$	28	$DACK_0$	36	A_0	44	A_7
5	N.C.	13	$\overline{CS}$	21	$DREQ_1$	23	N.C.	27	A_1		
6	READY	14	CLK	22	$DREQ_0$	30	DB_4	38	A_2		
7	N.C.	15	RESET	23	GND	31	DB_3	39	A_3		
8	N.C.	16	DACK2	24	DB_7	32	DB_2	40	$\overline{EOP}$		

Table 2: Pin Descriptions

Symbol	Type	Name and Function
A_{0-3}	I/O	**Low Address Bus:** Bi-directional, 3-state signals. The 4 least significant address lines. *Idle Cycle (Inputs).* Addresses the KS82C37A control register to be loaded or read. *Active Cycle (Outputs).* Lower 4 bits of the transfer address.
A_{4-7}	O	**High Address Bus:** 3-state output signals. The 4 most significant address lines representing the upper 4 bits of the transfer address. Enabled during DMA service only.
ADSTB	O	**Address Strobe:** Active HIGH output signal to control latching of the upper address byte. Drives the strobe input of external transparent octal latches. During block operations, ADSTB is activated only if the upper address byte needs updating, eliminating S_1 states and accelerating operation.
AEN	O	**Address Enable:** Active HIGH output signal to enable the 8-bit latch containing the higher order address byte onto the system address bus. During DMA transfers, it can disable other system bus drivers.
CLK	I	**Clock Input:** Generates timing signals to control internal operations and data transfer rate. Input can be driven from DC to maximum frequency. CLK may be stopped in Active or Idle Cycle for standby operation.

Table 2: Pin Descriptions (Continued)

Symbol	Type	Name and Function
$\overline{CS}$	I	**Chip Select:** Active LOW input signal to select the KS82C37A as an I/O device (Idle Cycle) for CPU communication on the data bus.
$DACK_{0-3}$	O	**DMA Acknowledge:** Individual channel active LOW (RESET) or HIGH output lines. Informs a peripheral that the requested DMA transfer has been granted.
DB_{0-7}	I/O	**Data Bus:** Bi-directional 3-state data lines connected to the system data bus. *Idle Cycle.* During I/O Read (Program condition), outputs are enabled and contents of KS82C37A internal registers are read by the CPU. In I/O Write, outputs are disabled and data from the data bus are written into the registers. *Active Cycle.* The upper byte of the transfer address is output to the data bus during DMA I/O device-to-memory transfers. In memory-to-memory transfers, data is read into the KS82C37A Temporary Register from data bus inputs during the read-from-memory transfer, and written to the new memory location by data bus outputs during the write-to-memory transfer.
$DREQ_{0-3}$	I	**DMA Request:** Asynchronous DMA service request input lines from I/O devices. DMA service is requested by activation of the channel from a specific device. DREQ must be maintained until DACK (service acknowledge) is activated. *I/O Device Priority.* Order of service is programmable. Priority may be fixed (descending order from channel 0 or rotating (most recent channel served gets the lowest priority).
$\overline{EOP}$	I/O	**End of Process:** Active Low bi-directional 3-state signal. The KS82C37A terminates DMA service when $\overline{EOP}$ is activated. *Internal $\overline{EOP}$ (Output).* $\overline{EOP}$ is activated when the word count for any channel turns over from 0000(H) to FFFF(H) and a TC pulse is generated. In memory-to-memory transfer, service is terminated when TC for channel 1 occurs. *External $\overline{EOP}$ (Input).* An external $\overline{EOP}$ signal pulling $\overline{EOP}$ LOW terminates active DMA service. An $\overline{EOP}$ signal also resets the DMA request. If autoinitialize is enabled, the base registers are written to the current register of the channel. If the channel is not programmed for autoinitialize, the mask bit (Mask Register) and TC bit (Status Register) are set for the currently active channel. The mask bit is not changed if the channel is set for autoinitialize. Since $\overline{EOP}$ is driven by an *open drain transistor* on-chip, it should be maintained HIGH with a pull-up resistor in order to avoid erroneous $\overline{EOP}$ inputs.
HLDA	I	**Hold Acknowledge:** Active HIGH input signal from the CPU, following an HRQ. Notifies the KS82C73A that the CPU has released control of the system buses.
HRQ	O	**Hold Request:** Active HIGH output signal to the CPU. Requests control of the system buses. HRQ is issued following a request for DMA service (DREQ) from a peripheral, and is acknowledged by the HLDA signal.
$\overline{IOR}$	I/O	**$\overline{IOR}$ Read:** Active LOW bi-directional, 3-state signal. *Idle Cycle.* CPU input control signal for reading the Control Registers. *Active Cycle.* Output control signal to read data from a peripheral device during a DMA cycle.
$\overline{IOW}$	I/O	**$\overline{IOW}$ Write:** Active LOW bi-directional, 3-state signal. *Idle Cycle.* CPU input control signal for loading information into the KS82C37A. *Active Cycle.* Output control signal to load data to a peripheral device during a DMA cycle.

Table 2: Pin Descriptions (Continued)

Symbol	Type	Name and Function
$\overline{MEMR}$	O	**Memory Read:** Active LOW 3-state output signal. KS82C37A reads data from a selected memory address during a DMA read or memory-to-memory transfer.
$\overline{MEMW}$	O	**Memory Write:** Active LOW 3-state output signal. KS82C37A writes data to a selected memory address during a DMA write or memory-to-memory transfer.
READY	I	**Ready:** A LOW ready signal extends the memory read and write pulse widths from the KS82C37A to accommodate slow I/O peripherals or memories. Transition must not be made during the specified setup/hold time.
RESET	I	**Reset:** Active HIGH asynchronous input signal. Clears the Command, Status, Request and Temporary Register, the Mode Register Counter, and the First/Last Flip-Flop. The Mask Register is set to ignore DMA requests. The KS82C37 is in Idle Cycle following Reset.
V_{CC}	—	**Power:** 5V ± 10% DC supply.
V_{SS}	—	**Ground:** 0V

FUNCTIONAL DESCRIPTION

The KS82C37A DMA controller is a state-driven address and control signal generator designed to accelerate data transfer in systems moving data from an I/O device to memory, or a block memory to an I/O device. Data transfer is direct, bypassing storage in a temporary register.

The KS82C37A also mediates memory-to-memory block transfers and will move data from a single location to a memory block. Temporary storage of data is required, but the transfer rate is significantly faster than CPU processes. The device provides operating modes to carry out both single byte transfers and memory block transfers, allowing it to control data movement with software transparency. An operational flowchart of the KS82C37A is shown in Figure 3.

The organization of the KS82C37A is outlined in the block diagram. It is composed of three logic blocks, a series of internal registers and a counter selection. The logic blocks include the Timing and Control and Priority Encoder circuits.

The Timing Control block generates internal timing signals from the clock input and produces external control signals.

Command Control decodes incoming instructions from the CPU, and the Priority Encoder block regulates DMA channel priority.

The internal registers hold internal states and instruction from the CPU. Addresses and word counts are computed in the counter section.

OPERATIONAL DESCRIPTION

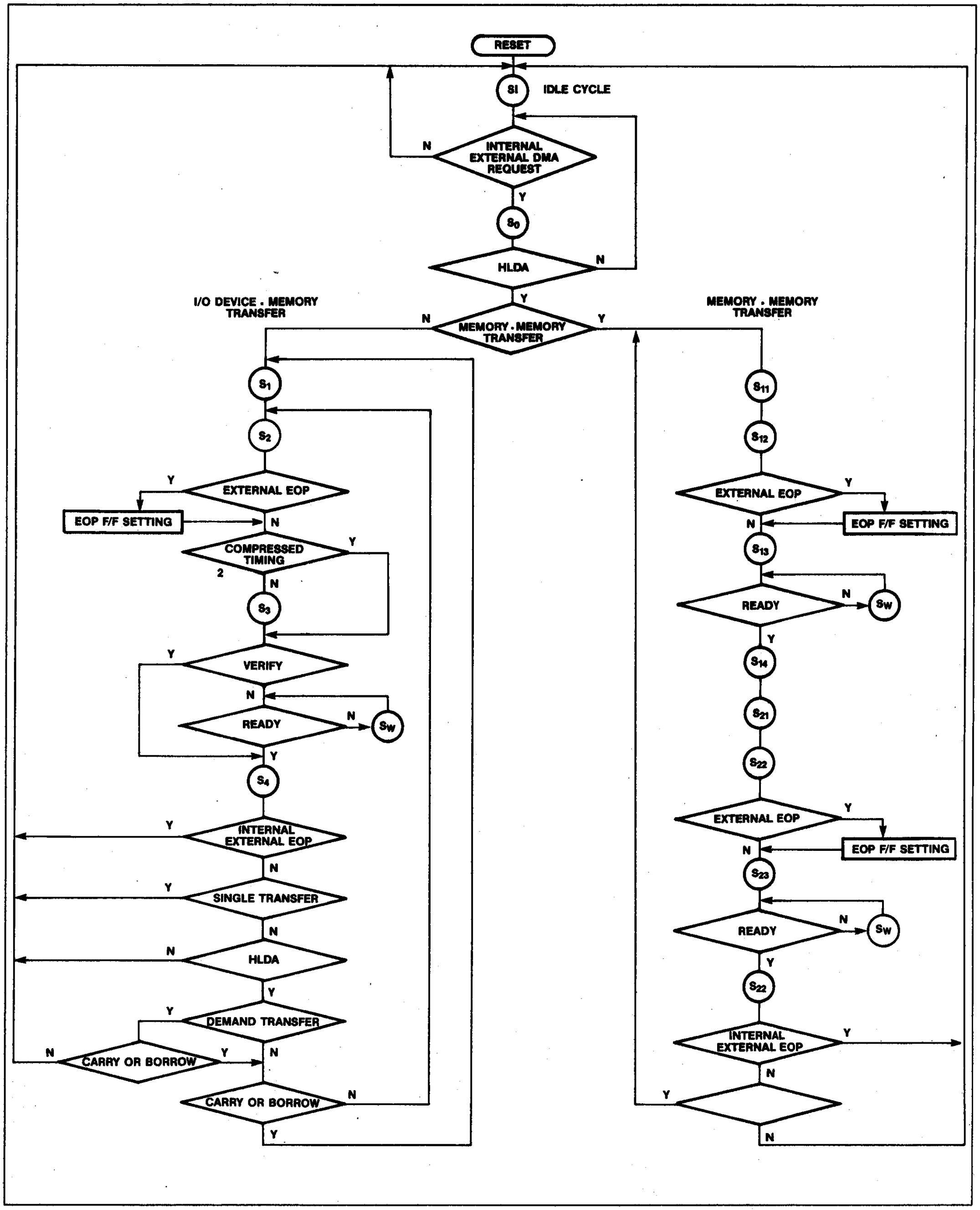
DMA Operation

In a system, the KS82C37A address and control outputs and data bus pins are usually connected in parallel with the system buses with an external latch required for the upper address byte. When inactive, the controller's outputs are in a high impedance state. When activated by a DMA request (and bus control has been relinquished by the host), the KS82C37A drives the buses and generates the control signals to perform the data transfer. The operation performed by activating one of the four DMA request inputs has previously been programmed into the controller via the Command Mode Address, and Word Count Registers.

For example, if a block of data is to be transferred from RAM to an I/O device, the starting address of the data is loaded into the KS82C37A current and Base Address Registers for a particular channel, and the length of the block is loaded into that channel's Word Count Register. The corresponding Mode Register is programmed for a memory-to-I/O operation (read transfer), and various options are selected by the Command Register and other Mode Register bits. The channel's mask bit is cleared to enable recognition of a DMA request (DREQ). The DREQ can be generated by a hardware signal or by a Software Command.

Once initiated, the block DMA transfer proceeds as the controller outputs the data address, simultaneous $\overline{MEMR}$ and $\overline{IOW}$ pulses, then selects an I/O device via the DMA acknowledge (DACK) outputs. The data byte flows directly from the RAM to the I/O device. After each byte

Figure 3: Operational Flowchart



is transferred, the address is automatically incremented (or decremented) and the Word Count is decremented. The operation is then repeated for the next byte. The controller stops transferring data when the Word Count Register underflows, or an external EOP is applied.

To better understand KS82C37A operation, consider the states generated by each clock cycle. The DMA controller operates in two major cycles, active and idle. After being programmed, the controller is normally idle until a DMA request occurs on an unmasked channel, or a software request is given. The KS82C37A then requests control of the system buses and enters the active cycle. The active cycle is composed of several internal states, depending on the options that have been selected and the type of operation that has been requested.

When performing I/O-to-memory or memory-to-I/O DMA the KS82C37A can enter seven distinct states, each composed of one full clock period. State 1 (S_1) is the idle state. It is entered when the KS82C37A has no valid DMA requests pending, at the end of a transfer sequence, or when a Reset or Master Clear occurs. While in S_1, the DMA controller is inactive, though it may be in the process of being programmed by the processor (Program Condition).

State 0 (S_0) is the first state of a DMA service. The KS82C37A has requested a hold but the processor has not yet returned an acknowledge. The KS82C37A may still be programmed until it has received HLDA from the CPU. An acknowledge from the CPU will signal that DMA transfers may begin. S_1, S_2, S_3, and S_4 are the working states of the DMA service. If more time is needed to complete a transfer than is available with normal timing, wait states (S_W) can be inserted prior to the execution of the S_4 cycle by use of the Ready line on the KS82C37A.

Note that the data is transferred directly from the I/O device to memory (or vice versa) with $\overline{IOR}$ and $\overline{MEMW}$ (or $\overline{MEMR}$ and $\overline{IOW}$) being active at the same time. The data is neither read into nor driven out of the KS82C37A in I/O-to-memory or memory-to-I/O transfers.

Table 3: Memory-to-Memory Transfer States

Transfer States	State Numbers	Notes
Read-from-Memory	S_{11}, S_{12} S_{13}, S_{14}	Memory-to-Memory transfers require 8 states per transfer. 4 states for the Read-from-Memory portion, and 4 Write-to-Memory states to complete the transfer.
Write-to-Memory	S_{21}, S_{22} S_{23}, S_{24}	

The KS82C37A can enter eight distinct states when performing memory-to-memory DMA, each composed of one full clock period. Four states are required for the read-from-memory step, and four for the write-to-memory operations. Data bytes in transit are stored in the Temporary register.

Idle Cycle

When none of the channels are requesting service, the KS82C37A enters the Idle cycle and performs S_1 states. In this cycle, the KS82C37A samples the DREQ lines on the falling edge of every clock cycle to determine if any channel is requesting a DMA service.

Note that DMA requests will be ignored in standby operation where the clock has been stopped. The device will respond to a $\overline{CS}$ (chip select), in case of an attempt by the microprocessor to write or read the internal registers of the KS82C37A. When $\overline{CS}$ is low and HLDA is low, the KS82C37A enters the Program Condition. The CPU can then establish, change or inspect the internal definition of the part by reading or writing the internal registers.

The KS82C37A may be programmed with the clock stopped, provided HLDA is low and at least one rising clock edge occurred after HLDA was driven low, so the controller is in an S_1 state. Address lines A_0 - A_3 are inputs to the device and select which registers are read or written. The $\overline{IOR}$ and $\overline{IOW}$ lines are used to select and time the read or write operations.

Due to the number and size of the internal registers, an internal flip-flop is used to generate an additional address bit. This bit is used to determine the upper or lower byte of the 16-bit Address and Word Count Registers. The flip-flop is reset by a Master Clear or Reset. Separate software commands can also set or reset this flip-flop.

Special software commands can be executed by the KS82C37A in the Program Condition. These commands are decoded as sets of addresses with $\overline{CS}$, $\overline{IOR}$, $\overline{IOW}$, and do not make use of the data bus. The commands include: Set and Clear First/Last Flip-Flop, Master Clear, Clear Mode Register Counter, and Clear Mask Register.

Active Cycle

When the KS82C37A is in the Idle cycle, and a software requests or an unmasked channel requests a DMA service, the device outputs an HRQ to the microprocessor and enters the Active cycle. It is in this cycle that the DMA service will take place, in one of the four modes described below:

Single Transfer Mode

In Single Transfer Mode, the device is programmed to make one transfer only. The Word Count is decremented and the address decremented or incremented following each transfer. When the Word Count rolls over from zero to FFFFH, a terminal count bit in the status register is set, an $\overline{EOP}$ pulse is generated, and the channel autoinitializes if this option has been selected. If not programmed to Autoinitialize, the mask bit is set, along with the TC bit and an $\overline{EOP}$ pulse is generated.

DREQ must be held active until DACK becomes active. If DREQ is held active throughout the single transfer, HRQ goes inactive and releases the bus to the system. It again goes active and, upon receipt of a new HLDA, another single transfer is performed, unless a higher priority channel takes over. In 8080A, 8085A, or 8088/86 systems, this ensures one full machine cycle execution between DMA transfers. Details of the timing between the KS82C37A and other bus control protocols depends upon the characteristics of the microprocessor involved.

Block Transfer Mode

In Block Transfer Mode, the KS82C37A is activated by DREQ or software request and continues making data transfers during the service until a TC, caused by word count going to FFFFH, or an external End of Process ($\overline{EOP}$) is encountered. DREQ need only be held active until DACK becomes active. Again, Autoinitialization occurs at the end of the service if the channel has been programmed for that option.

Demand Transfer Mode

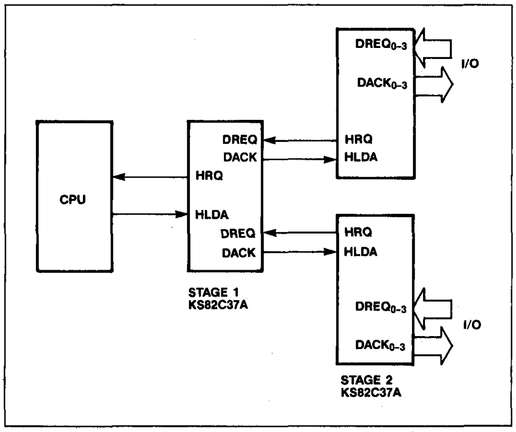
In Demand Transfer Mode the KS82C37A continues making transfers until a TC or an external $\overline{EOP}$ is encountered, or until DREQ goes inactive. Thus, transfers continue until the I/O device has exhausted its data capacity. When the I/O device has caught up, DMA service is reestablished by means of a DREQ. In the interim between services when the microprocessor is allowed to operate, the intermediate values of address and word count are stored in the KS82C37A Current Address and Current Word Count registers.

Higher priority channels may intervene in the demand process, once DREQ has gone inactive. Only an $\overline{EOP}$ can cause an Autoinitialization at the end of the service. The $\overline{EOP}$ is generated either by TC or by an external signal.

Cascade Mode

This mode is used to cascade more than one KS82C37A for simple system expansion. The HRQ and HLDA signals from additional KS82C37A devices are connected to the DREQ and DACK signals respectively of a channel for the initial KS82C37A. This allows the DMA requests of the additional devices to propagate through the priority network circuitry of the preceding device. The priority chain is preserved and the new device must wait for its turn to acknowledge requests. Since the cascade channel of the initial KS82C37A is used only for setting the priority of additional devices, it does not output an address or control signals of its own. These could conflict with the outputs of the active channel in the extra devices.

Figure 4: Cascaded KS82C37As



The KS82C37A will respond to DREQ and generate DACK but all other outputs except HRQ will be disabled. An external $\overline{EOP}$ will be ignored by the initial device, but will have the usual effect on the added device.

Figure 4 shows two additional devices cascaded with an initial device and using two of the initial device's channels. This forms a two-level DMA system. More KS82C37As could be added at the second level by using the remaining channels of the first level. Additional devices can also be added by cascading into the channels of the second level devices, forming a third level.

When programming cascaded controllers, start with the first level device (the one closet to the microprocessor). After Reset, the DACK outputs are programmed to be active low and are held in the high state. If they are used to drive HLDA directly, the second level device(s) cannot be programmed until DACK polarity is selected as active high on the initial device. In addition, the initial device's mask bits funciton normally on cascaded channels, so they may be used to inhibit second-level services.

Transfer Types

Each of the three active transfer modes can perform three different types of transfers. These are Read, Write and Verify. Write transfers move data from an I/O device to the memory by activating $\overline{MEMW}$ and $\overline{IOR}$. Read transfers move data from memory to an I/O device by activating $\overline{MEMR}$ and $\overline{IOW}$ (refer to Table 4).

Verify transfers are pseudo-transfers. The KS82C37A operates like Read or Write transfers, generating addresses and responding to $\overline{EOP}$, etc., however the memory and I/O control lines all remain inactive. Verify mode is not allowed for memory-to-memory operation. Note that Ready is ignored during verify transfers.

Autoinitialize

By programming a bit in the mode register, a channel may be set up as an Autoinitialize channel. During Autoinitialization, the original values of the Current Address and Current Word Count Registers are automatically restored from the Base Address and Base Word Count Registers of that channel following $\overline{EOP}$. The Base Registers are loaded at the same time as the Current Registers by the microprocessor and remain unchanged throughout the DMA service. The mask bit is not set when the channel is in Autoinitialize. Following Autoinitialization, the channel is ready to perform another DMA service, without CPU intervention, as soon as a valid DREQ is detected, or software request is made.

Memory-to-Memory

The KS82C37A incorporates a memory-to-memory transfer feature, to perform block moves of data from one memory address space to another with minimum of program effort and time. Programming bit 0 in the Command Register selects channels 0 and 1 to operate as memory-to-memory transfer channels.

The transfer is initiated by setting the software or hardware DREQ for channel 0. The KS82C37A requests a DMA service in the normal manner. When HLDA goes high, the device, using four-state transfers in Block Transfer mode, reads data from the memory. The channel 0 Current Address Register is the source for the address used and is decremented or incremented in the normal manner. The data byte read from the memory is stored in the KS82C37A internal Temporary Register. Another four-state transfer moves the data to memory using the address in the channel 1 Current Address Register. The Current Address is incremented or decremented in the normal manner, and the channel 1 Current Word Count is decremented.

When the word count of channel 1 goes to FFFFH, a TC is generated, causing an $\overline{EOP}$ output which terminates the service. When Channel 0 word count decrements to FFFFH the channel 0 TC bit in the status register is not set nor is an $\overline{EOP}$ generated in this mode. However, channel 0 is Autoinitialized, if that option has been selected.

Table 4: I/O-Memory Transfer States*

Operational State	Description	Notes
S_1	AEN High Low Order Bits: A_0 - A_7 High Order Bits: DB_0 - DB_7 ADSTB High DACK Active	S_1 state is omitted if there is no change in the 8 high order bit transfer address during demand and block mode transfers.
S_2	$\overline{IOR}$ Low or $\overline{MEMR}$ goes Low	S_2 State (and S_3) are I/O or memory I/O timing control states.
S_3	$\overline{IOW}$ Low or $\overline{MEMW}$ goes Low	S_3 is omitted when compressed timing is used.
S_4	$\overline{IOR}$ High $\overline{IOW}$ High $\overline{MEMR}$ High $\overline{MEMW}$ High Word Count Register Decremented by 1 Address Register Incremented (or Decremented) by 1	S_4 state completes the DMA transfer of one word.

* In I/O memory transfers, data is transferred directly without being handled by the KS82C37A.

If full Autoinitialization for a memory-to-memory operation is desired, the channel 0 and channel 1 word counts must be set to the same value before the transfer begins. Otherwise, should channel 0 underflow before channel 1, it Autoinitializes and sets the data source address back to the beginning of the block. Should the channel 1 word count underflow before channel 0, the memory-to-memory DMA service terminates, and channel 1 Autoinitializes but not channel 0.

In memory-to-memory mode, Channel 0 may be programmed to retain the same address for all transfers, allowing a single byte to be written to an entire block of memory. This channel 0 Address Hold feature is selected by bit 1 in the command register.

The KS82C37A responds to external $\overline{EOP}$ signals during memory-to-memory transfers, but only relinquishes the system buses after the transfer is complete (i.e. after an S_{24} state). Data comparators in block search schemes may use this input to terminate the service when a match is found. The timing of memory-to-memory transfers is found in Figure 14b. Memory-to-memory operations can be detected as an active AEN with no DACK outputs.

Priority

The KS82C37A has two types of priority encoding available as software selectable options. The first is Fixed Priority which fixes the channels in priority order based upon the descending value of their numbers. The channel with the lowest priority is 3 followed by 2, 1 and the highest priority channel, 0. After a channel has been recognized for service, the other channels are prevented from interfering with the service until it is completed.

The second scheme is Rotating Priority. The last channel to get service becomes the lowest priority channel with the others rotated accordingly. The next lower channel from the channel serviced has highest priority on the following request: Priority rotates every time control of the system buses is returned to the CPU.

With Rotating Priority in a single chip DMA system, any device requesting service is guaranteed to be recognized after no more than three higher priority services have occurred. Thus any one channel is prevented from monopolizing the system.

Note that regardless of which priority scheme is chosen, priority is evaluated every time a HLDA is returned to the KS82C37A.

Compressed Timing

In order to achieve even greater throughput where system characteristics permit, the KS82C37A can compress the transfer time to two clock cycles. From Figure 3, it can be seen that state S_3 is used to extend the access time of the read pulse. By removing state S_3, the read pulse width is made equal to the write pulse width and a transfer consists only of state S_2 to change the address and state S_4 to perform the read/write. S_1 states will still occur when A_8 - A_{15} need updating (see Address Generation). Timing for compressed transfers is found in Figure 3. $\overline{EOP}$ will be output in S_2 if compressed timing is selected. Compressed timing is not allowed for memory-to-memory transfers.

Table 5: Priority Decision Modes

Priority Mode		Fixed	Rotating			
Service Terminated Channel		—	CH_0	CH_1	CH_2	CH_3
Order of Priority or next DMA	Highest	CH_0	CH_1	CH_2	CH_3	CH_0
		CH_1	CH_2	CH_3	CH_0	CH_1
		CH_2	CH_3	CH_0	CH_1	CH_2
	Lowest	CH_3	CH_0	CH_1	CH_2	CH_3

Address Generation

In order to reduce the pin count, the KS82C37A multiplexes the eight higher order address bits on the data lines. State S_1 is used to output the higher order address bits to an external latch from which they may be placed on the address bus. The falling edge of Address Strobe (ADSTB) is used to load these bits from the data lines to the latch. Address Enable (AEN) is used to enable the bits onto the address bus through a three-state enable. Lower order address bits are output by the KS82C37A directly. Lines A_0 - A_7 should be connected to the address bus. The timing diagram of Figure 3 shows the time relationships between CLK, AEN, ADSTB, DB_0 - DB_7 and A_0 - A_7.

During Block and Demand Transfer mode service, which include multiple transfers, the addresses generated will be sequential. For many transfers the data held in the external address latch will remain the same. This data need only change when a carry or borrow from A_7 to A_8 takes place in the normal sequence of addresses. To save time and speed transfers, the KS82C37A executes the S_1 states only when updating of A_8 - A_{15} in the latch is necessary. This means for long services, S_1 states and ADSTB may occur only once every 256 transfers, a saving of 255 clock cycles for each 256 transfers.

External $\overline{EOP}$ Operation

The $\overline{EOP}$ pin is bidirectional and open drain, and can be driven by external signals to terminate DMA operation. It is important to note that the KS82C37A will not accept external $\overline{EOP}$ signals when it is in an S_I (Idle) state. The controller must be active to latch external $\overline{EOP}$. Once latched, the external $\overline{EOP}$ will be acted upon during the next S_2 state, unless the KS82C37A enters an idle state first. In the latter case, the latched $\overline{EOP}$ is cleared. External $\overline{EOP}$ pulses that occur between active DMA transfers in demand mode are not recognized, since the KS82C37A is in an S_1 state.

INTERNAL REGISTERS

The KS82C37A contains 27 registers that are used internally for control and temporary data storage. These registers are listed in Table 6 below, and described in the subsections following.

Base Address and Base Word Count Registers

Each of the four (4) channels has a pair of Base Address and Base Word Count Registers. These 16-bit registers store the original value of their associated current registers. During Autoinitialize these values are used to restore the current registers to their original values.

The base registers are written simultaneously with their corresponding current register (in 8-bit bytes) by the microprocessor when in the Program Condition. These registers cannot be read by the microprocessor.

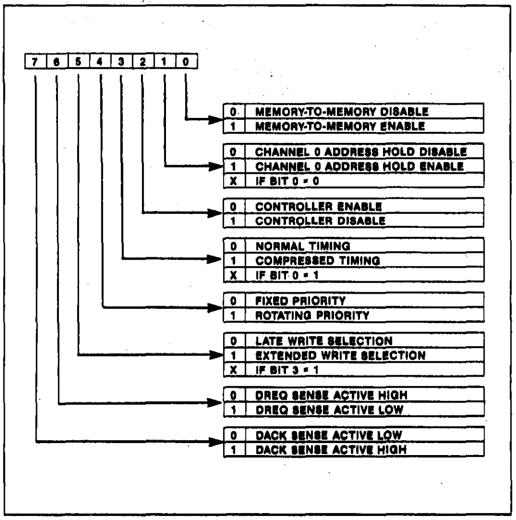
Table 6: Internal Registers

Name	Number	Size
Base Address Registers	4	16-Bit
Base Word Count Registers	4	16-Bit
Command Register	1	8-Bit
Current Address Registers	4	16-Bit
Current Word Count Registers	4	16-Bit
Mask Register	1	4-Bit
Mode Registers	4	6-Bit
Request Register	1	4-Bit
Status Register	1	8-Bit
Temporary Address Register	1	16-Bit
Temporary Register	1	8-Bit
Temporary Word Count Register	1	16-Bit

Command Register

The operation of the KS82C37A is controlled by the 8-bit Command Register. It is programmed by the microprocessor and is cleared by a Reset or a Master Clear instruction. Figure 5 lists the function of the command bits, while Table 7 contains the Read and Write addresses.

Figure 5: Command Register



Current Address Register

Each of the channels has a 16-bit Current Address register. This register holds the value of the address used during DMA transfers. The address is automatically incremented or decremented after each transfer, with the values of the address stored in the Current Address register during the transfer.

This register is written or read by the microprocessor in successive 8-bit bytes. It may also be reinitialized (by an Autoinitialize) back to its original value, where an Autoinitialize takes place only after an $\overline{EOP}$.

In memory-to-memory mode, the channel 0 current address register can be prevented from incrementing or decrementing by setting the address hold bit in the command register.

Current Word Register

Each of the channels also has a 16-bit Current Word Count register which is used to determine the number of transfers to be performed. The actual number of transfers is one more than the number programmed in the Current Word Count register (i.e. programming a count of 100 will result in 101 transfers). The word count is decremented after each transfer, and when the value in the register goes from zero to FFFFH, a terminal count (TC) is generated.

This register is loaded or read in successive 8-bit bytes by the microprocessor in the Program Condition.

Following the end of a DMA service it may also be reinitialized by an Autoinitialization back to its original value. Autoinitialization can occur only after an $\overline{EOP}$ or TC. If not Autoinitialized, this register will have a count of FFFFH after TC.

Mask Register

Each of the channels has associated with it one mask bit in the 4-bit Mask register which can be set to disable an incoming DREQ. Each mask bit is set when its associated channel produces an $\overline{EOP}$ if the channel is not programmed to Autoinitialize. Each Mask register bit may also be set or cleared separately or simultaneously under software control.

The entire register is also set by a Reset or Master Clear. This disables all hardware DMA requests until a clear Mask register instruction allows them to occur. The instruction to separately set or clear the mask bits is similar in form to that used with the Request register. Refer to the Figure 6 and Table 7 for details.

When reading the mask register, bits 4-7 will always read as logical ones, and bits 0-3 will display the mask bits of channel 0-3, respectively. The 4 bits of the mask register may be cleared simultaneously by using the Clear Mask Register command (see software commands section).

Figure 6: Mask Register

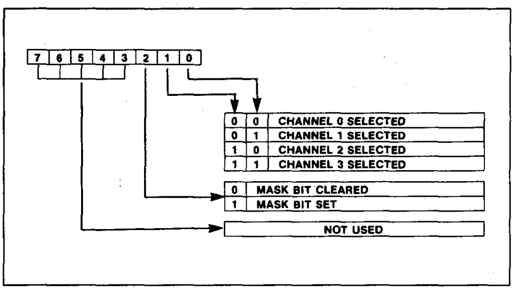
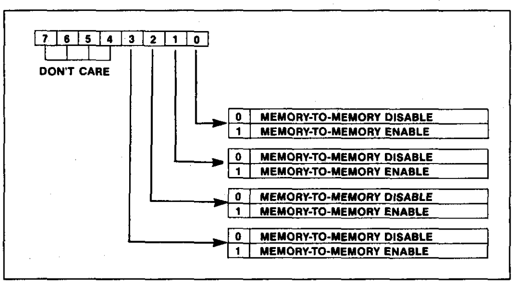


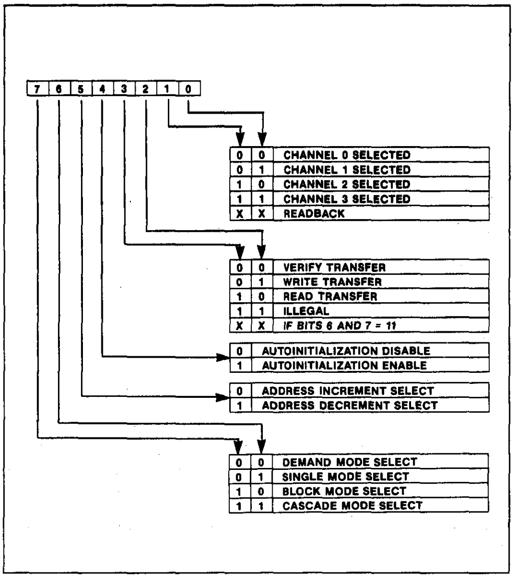
Figure 7: All Four Size Bits of the Mask Register May Also Be Written with a Simple Command



Mode Register

Each of the channels has a 6-bit mode register associated with it. When this register is being written to by the microprocessor in the Program Condition, bits 0 and 1 determine which channel Mode register is to be written. When the processor reads a mode register, bits 0 and 1 are both ones. See Figure 8 and Table 7 for mode register functions and addresses.

Figure 8: Mode Register

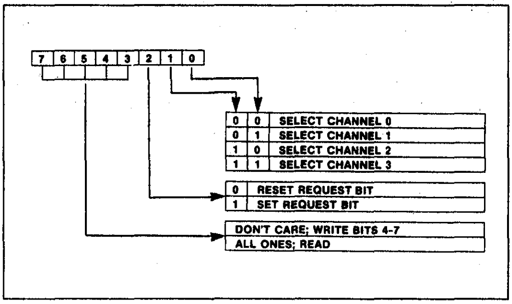


Request Register

The KS82C37A responds to requests for DMA service initiated by the software and by a DREQ. Each channel has a non-maskable request bit associated with it in the 4-bit Request Register. These are subject to prioritization by the priority Encoder network with each bit set or reset separately under software control. To set or reset a bit, the software loads the proper form of the data word. The entire register is cleared by a Reset. See Table 7 for register address coding, and Figure 9 for request register format.

A software request for DMA operation can be made in block or single modes. For memory-to-memory transfers, the software request for channel 0 should be set. When reading the request register, bits 4-7 will always read as ones, and bits 0-3 will display the request bits of channels 0-3 respectively.

Figure 9: Request Register



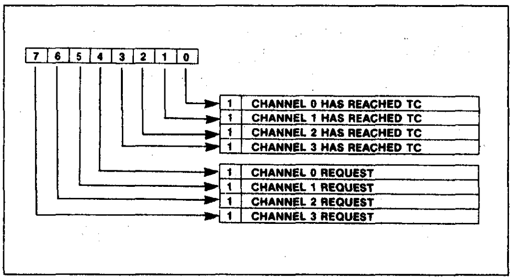
Status Register

The KS82C37A Status register can be read by the microprocessor. It contains information about which channels have reached a terminal count and which channels have pending DMA requests.

Bits 0-3 are set every time a TC is reached by that channel or an external $\overline{EOP}$ is applied. These bits are cleared upon Reset, Master Clear, and on each Status Read.

Bits 4-7 are set whenever their corresponding channel is requesting service, regardless of the mask bit state. If the mask bits are set, software can poll the status register to determine which channels have DREQs, and selectively clear a mask bit, thus allowing user defined service priority. Status bits 4-7 are updated while the clock is high, and latched on the falling edge. Status Bits 4-7 are cleared upon Reset or Master Clear.

Figure 10: Status Register



Temporary Register

The Temporary Register is used to hold data during memory-to-memory transfers. When the transfers are completed, the last word moved can be read by the microprocessor.

Note that the Temporary Register always contains the last byte transferred in the previous memory-to-memory operation, unless cleared by a Reset or Master Clear.

Figure 11: Definition of Register Codes

Register	Operation	SIGNALS						
		$\overline{CS}$	$\overline{IOR}$	$\overline{IOW}$	A_3	A_2	A_1	A_0
Command	Write	0	1	0	1	0	0	0
Mode	Write	0	1	0	1	0	1	1
Request	Write	0	1	0	1	0	0	1
Mask	Set/Reset	0	1	0	1	0	1	0
Mask	Write	0	1	0	1	1	1	1
Temporary	Read	0	0	1	1	1	0	1
Status	Read	0	0	1	1	0	0	0

PROGRAMMING

The KS82C37A accepts programming from the host processor any time that HLDA is inactive, and at least one rising clock edge has occurred after HLDA has gone low. It is necessary for the host processor to ensure that programming and HLDA are mutually exclusive.

Note that a problem can occur if a DMA request occurs on an unmasked channel while the KS82C37A is being programmed. For example: Where the CPU is starting to re-program the two byte address register of channel 1 when channel 1 receives a DMA request: If the KS82C37A is enabled (bit 2 in the Command register is set to 0), and channel 1 is unmasked, then a DMA service will occur after only one byte of the Address register has been reprogrammed. This condition can be avoided by disabling the controller (bit 2 in the Command register is set to 1) or masking the channel before programming any of its registers. Once the programming is complete, the controller can be enabled or the channel unmasked.

Software Commands

There are special software commands which can be executed by reading or writing to the KS82C37A. These commands do not depend on the specific data pattern on the data bus, but are activated by the I/O operation itself.

The KS82C37A Software Commands are summarized below:

Clear First/Last Flip-Flop

This command is executed prior to writing or reading new Address or Word Count information to the KS82C37A. This initializes the flip-flop to a known state so that subsequent accesses to register contents by the micro processor will address upper and lower bytes in the correct sequence.

Table 7: Software Command Codes and Register Codes

Operation	A_3	A_2	A_1	A_0	$\overline{IOR}$	$\overline{IOW}$
Read Status Register	1	0	0	0	0	1
Write Command Register	1	0	0	0	1	0
Read Request Register	1	0	0	1	0	1
Write Request Register	1	0	0	1	1	0
Read Command Register	1	0	1	0	0	1
Write Single Bit Mask	1	0	1	0	1	0
Read Mode Register	1	0	1	1	0	1
Write Mode Register	1	0	1	1	1	0
Set Byte Pointer F/F	1	1	0	0	0	1
CLR Byte Pointer F/F	1	1	0	0	1	0
Read Temporary Register	1	1	0	1	0	1
Master Clear	1	1	0	1	1	0
CLR Mode Register Counter	1	1	1	0	0	1
CLR Mask Register	1	1	1	0	1	0
Read All Mask Bits	1	1	1	1	0	1
Write All Mask Bits	1	1	1	1	1	0

Set First/Last Flip-Flop

This command will set the flip-flop to first select the high byte first on read and write operations to Address and Word Count Registers.

Master Clear

This software instruction has the same effect as the hardware Reset. The Command, Status, Request, and Temporary Registers, and Internal First/Last Flip-Flop and Mode Register counter are cleared and the Mask Register is set. The device then enters the Idle cycle.

Clear Mode Register

This command clears the mask bits of all four channels, enabling them to accept DMA requests.

Clear Mode Register Counter

Since only one address location is available for reading Mode Registers, an internal two-bit counter is included to select Mode Registers during read operations.

To read the Mode Registers, first execute the Clear Mode Register Counter Command, then do consecutive reads until the desired channel is read. Read order is channel 0 first, channel 3 last. The lower two bits on all Mode Registers will read as ones.

APPLICATIONS

Figure 12 shows an application for a DMA system utilizing the KS82C37A DMA controller and an 80C88 microprocessor. The KS82C37A DMA controller is used here to improve system performance by allowing an I/O device to transfer data directly to or from the system memory.

Components

The system clock is generated by the KS82C84A clock driver and is inverted to meet the clock high and low times required by the KS82C37A DMA controller. The four OR gates are used to support an 80C88 microprocessor in minimum mode by producing the control signals used by the processor to access memory or I/O. A decoder is used to generate the chip select for the DMA controller and memory.

Since the most significant bits of the address are output on the address/data bus, an octal latch is used to demultiplex the address. Hold Acknowledge (HLDA) and Address Enable (AEN) are ORed together to insure that the DMA controller does not encounter bus contention with the microprocessor.

Operation

A DMA request (DREQ) is generated by the I/O device. After receiving the DMA request, the DMA controller issues a Hold Request (HRQ) to the microprocessor. The system buses are not released to the DMA controller until a Hold Acknowledge signal is returned to the DMA controller from the 80C88 processor. After the Hold Acknowledge has been received, addresses and control signals are generated by the DMA controller to accomplish the DMA transfers. Data is transferred directly from the I/O device to memory (or vice versa) with $\overline{IOR}$ and $\overline{MEMW}$ (or $\overline{MEMR}$ and $\overline{IOW}$) being active. Recall that data is not read into or driven out of the DMA controller in I/O-to-memory or memory-to-I/O data transfers.

3

Table 8: Word Count and Address Register Command Codes

Channel	Register	Operation	SIGNALS $\overline{CS}$	$\overline{IOR}$	$\overline{IOW}$	A_3	A_2	A_1	A_0	Internal Flip-Flop	Data Bus DB_0-DB_7
0	Base and Current Address	Write	0	1	0	0	0	0	0	0	A_0 - A_7
			0	1	0	0	0	0	0	1	A_8 - A_{15}
	Current Address	Read	0	0	1	0	0	0	0	0	A_0 - A_7
			0	0	1	0	0	0	0	1	A_8 - A_{15}
	Base and Current Word Count	Write	0	1	0	0	0	0	1	0	W_0 - W_7
			0	1	0	0	0	0	1	1	W_8 - W_{15}
	Current Word Count	Read	0	0	1	0	0	0	1	0	W_0 - W_7
			0	0	1	0	0	0	1	1	W_8 - W_{15}
1	Base and Current Address	Write	0	1	0	0	0	1	0	0	A_0 - A_7
			0	1	0	0	0	1	0	1	A_8 - A_{15}
	Current Address	Read	0	0	1	0	0	1	0	0	A_0 - A_7
			0	0	1	0	0	1	0	1	A_8 - A_{15}
	Base and Current Word Count	Write	0	1	0	0	0	1	1	0	W_0 - W_7
			0	1	0	0	0	1	1	1	W_8 - W_{15}
	Current Word Count	Read	0	0	1	0	0	1	1	0	W_0 - W_7
			0	0	1	0	0	1	1	1	W_8 - W_{15}
2	Base and Current Address	Write	0	1	0	0	1	0	0	0	A_0 - A_7
			0	1	0	0	1	0	0	1	A_8 - A_{15}
	Current Address	Read	0	0	1	0	1	0	0	0	A_0 - A_7
			0	0	1	0	1	0	0	1	A_8 - A_{15}
	Base and Current Word Count	Write	0	1	0	0	1	0	1	0	W_0 - W_7
			0	1	0	0	1	0	1	1	W_8 - W_{15}
	Current Word Count	Read	0	0	1	0	1	0	1	0	W_0 - W_7
			0	0	1	0	1	0	1	1	W_8 - W_{15}
3	Base and Current Address	Write	0	1	0	0	1	1	0	0	A_0 - A_7
			0	1	0	0	1	1	0	1	A_8 - A_{15}
	Current Address	Read	0	0	1	0	1	1	0	0	A_0 - A_7
			0	0	1	0	1	1	0	1	A_8 - A_{15}
	Base and Current Word Count	Write	0	1	0	0	1	1	1	0	W_0 - W_7
			0	1	0	0	1	1	1	1	W_8 - W_{15}
	Current Word Count	Read	0	0	1	0	1	1	1	0	W_0 - W_7
			0	0	1	0	1	1	1	1	W_8 - W_{15}

Figure 12: Application for DMA System

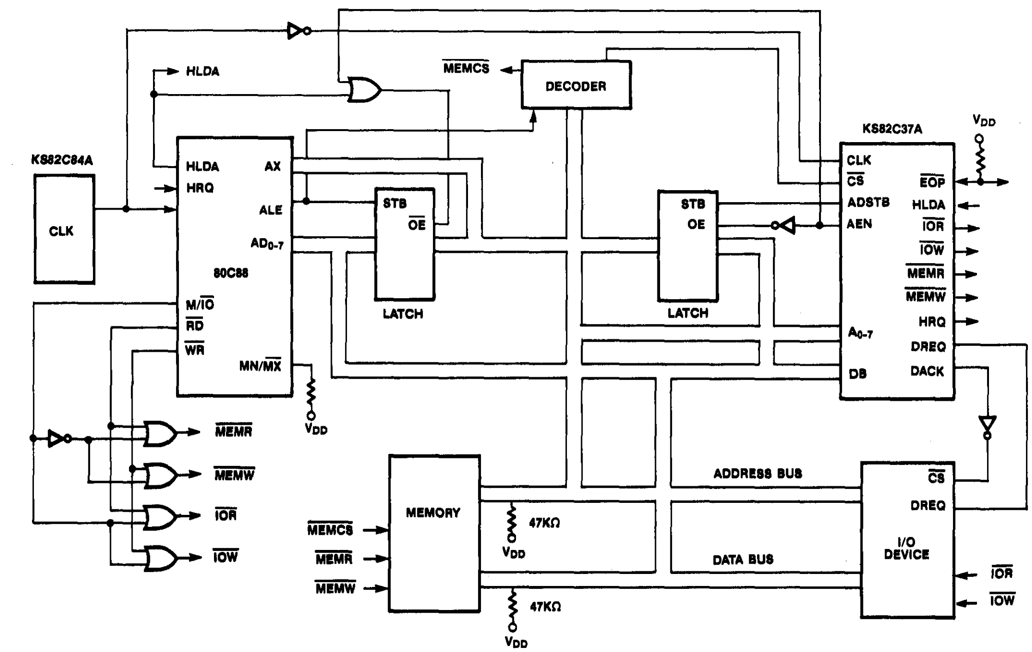


Table 9: Recommended Operating Conditions

DC Supply Voltage		+4.0V to +6.0V
Operating Temperature Range	Commercial	0°C to 70°C
	Industrial	-40°C to +85°C

Table 10: Absolute Maximum Ratings

DC Supply Voltage	+7.0V
Input, Output or I/O Voltage Applied	V_{SS} - 0.5V to V_{CC} + 0.5V
Storage Temperature Range	-65°C to +150°C
Maximum Package Power Dissipation	1W

Note: Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 11: Capacitance (T_A = 25°C, V_{CC} = 0V, V_{IN} = +5V or V_{SS})

Symbol	Parameter	Test Conditions	Typ	Units
$C_{I/O}$	I/O Capacitance	FREQ = 1MHz Unmeasured Pins Returned to V_{SS}	20	pF
C_{IN}	Input Capacitance		5	pF
C_{OUT}	Output Capacitance		15	pF

Table 12: DC Characteristics (T_A = 0°C to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Symbol	Parameter	Test Conditions	Limits Min	Limits Max	Units
I_{DD}	Operating Power Supply Current	V_{CC} = 5.5V V_{IN} = V_{CC} or V_{SS} Outputs Open	—	2.0	mA/MHz
I_{DDSB}	Standby Power Supply Current	V_{CC} = 5.5V V_{IN} = V_{CC} or V_{SS} Outputs Open	—	100	μA
I_{IL}	Input Leakage Current for Unidirectionals	0V ≤ V_{IN} ≤ V_{CC}	-1.0	+1.0	μA
I_{ILIO}	Input Leakage Current for Bidirectionals	0V ≤ V_{IN} ≤ V_{CC}	-10.0	+10.0	μA
I_{OL}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}	-10.0	+10.0	μA
V_{IH}	Logical One Input Voltage		2.0	—	V
V_{IL}	Logical Zero Input Voltage		—	0.8	V
V_{OH}	Output High Voltage	I_{OH} = -2.5mA I_{OH} = -100μA	2.4 V_{CC} - 0.4	— —	V V
V_{OL}	Output Low Voltage	I_{OL} = +3.2mA	—	0.4	V

Notes:
1. Input timing parameters assume rise and fall transition times of 20ns or less.
2. The net $\overline{IOW}$ or $\overline{MEMW}$ pulse width for a normal write will be t_{CY} - 100ns, and for an extended write will be 2 · t_{CY} - 100ns. The net $\overline{IOR}$ or $\overline{MEMR}$ pulse width for a normal read will be 2 · t_{CY} - 50ns and for a compressed read will be t_{CY} - 50ns.
3. DREQ should be held active until DACK is returned.
4. DREQ and DACK signals may be active HIGH or active LOW. The timing diagrams assume active HIGH.
5. Successive read and/or write operations by the external processor to program or examine the controller must be timed to allow at least 100ns (KS82C37A-10) and 200ns (KS82C37A-5) as recovery time between active read or write pulses.
6. $\overline{EOP}$ is an open drain output, and requires a pullup resistor to V_{CC}.
7. Pin 5 can be either tied to V_{DD}, or left unconnected.

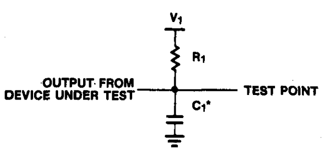
Table 13: AC Characteristics, DMA (Master) Mode (T_A = 0 to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Symbol	Parameter	Limits (5MHz) Min	Limits (5MHz) Max	Limits (8MHz) Min	Limits (8MHz) Max	Limits (10MHz) Min	Limits (10MHz) Max	Units
t_{AEL}	AEN HIGH from CLK LOW (S_1) Delay Time	—	175	—	105	—	90	ns
t_{AET}	AEN LOW from CLK HIGH (S_1) Delay Time	—	130	—	80	—	80	ns
t_{AFAB}	ADR Active to Float Delay from CLK HIGH	—	90	—	55	—	55	ns
t_{AFC}	$\overline{READ}$ or $\overline{WRITE}$ Float Delay from CLK HIGH	—	120	—	75	—	75	ns
t_{AFDB}	DB Active to Float Delay from CLK HIGH	—	170	—	135	—	100	ns
t_{AHR}	ADR from $\overline{READ}$ HIGH Hold Time	t_{CY}-100	—	t_{CY}-75	—	t_{CY}-75	—	ns
t_{AHS}	DB from ADSTB LOW Hold Time	30	—	25	—	20	—	ns
t_{AHW}	ADR from $\overline{WRITE}$ HIGH Hold Time	t_{CY}-50	—	t_{CY}-50	—	t_{CY}-50	—	ns
t_{AK}	DACK Valid from CLK LOW Delay Time	—	170	—	105	—	90	ns
	$\overline{EOP}$ HIGH from CLK HIGH Delay Time	—	170	—	105	—	90	ns
	$\overline{EOP}$ LOW from CLK HIGH Delay Time	—	100	—	60	—	60	ns
t_{ASM}	ADR Stable from CLK HIGH	—	110	—	60	—	60	ns
t_{ASS}	DB to ADSTB LOW Setup Time	100	—	85	—	75	—	ns
t_{CH}	CLK HIGH Time	70	—	55	—	45	—	ns
t_{CL}	CLK LOW Time	70	—	50	—	45	—	ns
t_{CY}	CLK Cycle Time	200	—	125	—	100	—	ns
t_{DCL}	CLK HIGH to $\overline{READ}$ or $\overline{WRITE}$ LOW Delay	—	190	—	120	—	90	ns
t_{DCTR}	$\overline{READ}$ HIGH from CLK HIGH (S_1) Delay Time	—	190	—	115	—	95	ns
t_{DCTW}	$\overline{WRITE}$ HIGH from CLK HIGH (S_1) Delay Time	—	130	—	80	—	80	ns
t_{DQ1}	HRQ Valid from CLK HIGH Delay Time	—	120	—	75	—	75	ns
t_{DQ2}	HRQ Valid from CLK HIGH Delay Time	—	120	—	75	—	75	ns
t_{EPS}	$\overline{EOP}$ LOW from CLK LOW Setup Time	40	—	25	—	25	—	ns
t_{EPW}	$\overline{EOP}$ Pulse Width (ext. $\overline{EOP}$)	220	—	135	—	80	—	ns
t_{FAAB}	ADR Float to Active Delay from CLK HIGH	—	110	—	60	—	60	ns
t_{FAC}	$\overline{READ}$ or $\overline{WRITE}$ Active from CLK HIGH	—	150	—	90	—	90	ns
t_{FADB}	DB Float to Active Delay from CLK HIGH	—	110	—	60	—	60	ns
t_{HS}	HLDA Valid to CLK HIGH Setup Time	75	—	45	—	45	—	ns
t_{IDH}	Input Data from $\overline{MEMR}$ HIGH Hold Time	0	—	0	—	0	—	ns
t_{IDS}	Input Data to $\overline{MEMR}$ HIGH Setup Time	155	—	90	—	80	—	ns
t_{ODH}	Output Data from $\overline{MEMW}$ HIGH Hold Time	15	—	15	—	15	—	ns
t_{ODV}	Output Data Valid to $\overline{MEMW}$ HIGH	125	—	85	—	65	—	ns
t_{QS}	DREQ to CLK LOW (S_1, S_4) Setup Time	0	—	0	—	0	—	ns
t_{RH}	CLK to READY LOW Hold Time	20	—	20	—	10	—	ns
t_{RS}	READY to CLK LOW Setup Time	60	—	35	—	35	—	ns
t_{STL}	ADSTB HIGH from CLK HIGH Delay Time	—	80	—	50	—	50	ns
t_{STT}	ADSTB LOW from CLK HIGH Delay Time	—	90	—	90	—	90	ns

Table 14: AC Characteristics, Peripheral (Slave) Mode (T_A = 0 to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Symbol	Parameter	Limits (5MHz)		Limits (8MHz)		Limits (10MHz)		Units
		Min	Max	Min	Max	Min	Max	
t_{AR}	ADR Valid or $\overline{CS}$ LOW to $\overline{READ}$ LOW	10	—	10	—	0	—	ns
t_{AW}	ADR Valid to $\overline{WRITE}$ HIGH Setup Time	130	—	100	—	60	—	ns
t_{CW}	$\overline{CS}$ LOW to $\overline{WRITE}$ HIGH Setup Time	130	—	100	—	85	—	ns
t_{DW}	Data Valid to $\overline{WRITE}$ HIGH Setup Time	130	—	100	—	90	—	ns
t_{RA}	ADR or $\overline{CS}$ Hold from $\overline{READ}$ HIGH	0	—	0	—	0	—	ns
t_{RDE}	Data Access from $\overline{READ}$	—	140	—	120	—	95	ns
t_{RDF}	DB Float Delay from $\overline{READ}$ HIGH	0	70	0	70	0	70	ns
t_{RSTD}	Power Supply HIGH to RESET LOW Setup Time	500	—	500	—	500	—	ns
t_{RSTS}	RESET to First $\overline{IOWR}$	$2 \cdot t_{CY}$	—	$2 \cdot t_{CY}$	—	$2 \cdot t_{CY}$	—	ns
t_{RSTW}	RESET Pulse Width	300	—	200	—	100	—	ns
t_{RW}	I/O Read Width	200	—	155	—	120	—	ns
t_{WA}	ADR from $\overline{WRITE}$ HIGH Hold Time	0	—	0	—	0	—	ns
t_{WC}	$\overline{CS}$ HIGH from $\overline{WRITE}$ HIGH Hold Time	0	—	0	—	0	—	ns
t_{WD}	Data from $\overline{WRITE}$ HIGH Hold Time	10	—	10	—	10	—	ns
t_{WWS}	$\overline{WRITE}$ Width	150	—	100	—	90	—	ns

Figure 13: AC Test Circuits



PINS	V_1	R_1	C_1
All Outputs Except $\overline{EOP}$	1.7V	520Ω	100pF
$\overline{EOP}$	V_{CC}	1.6KΩ	50pF

Figure 14: AC Testing Input, Output Waveforms

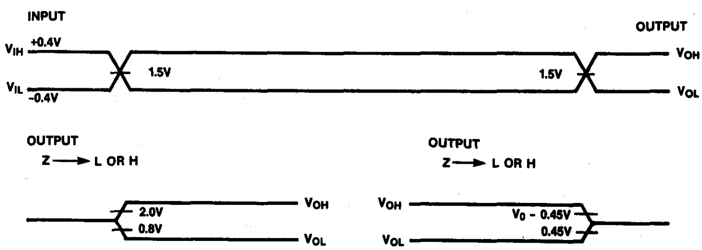
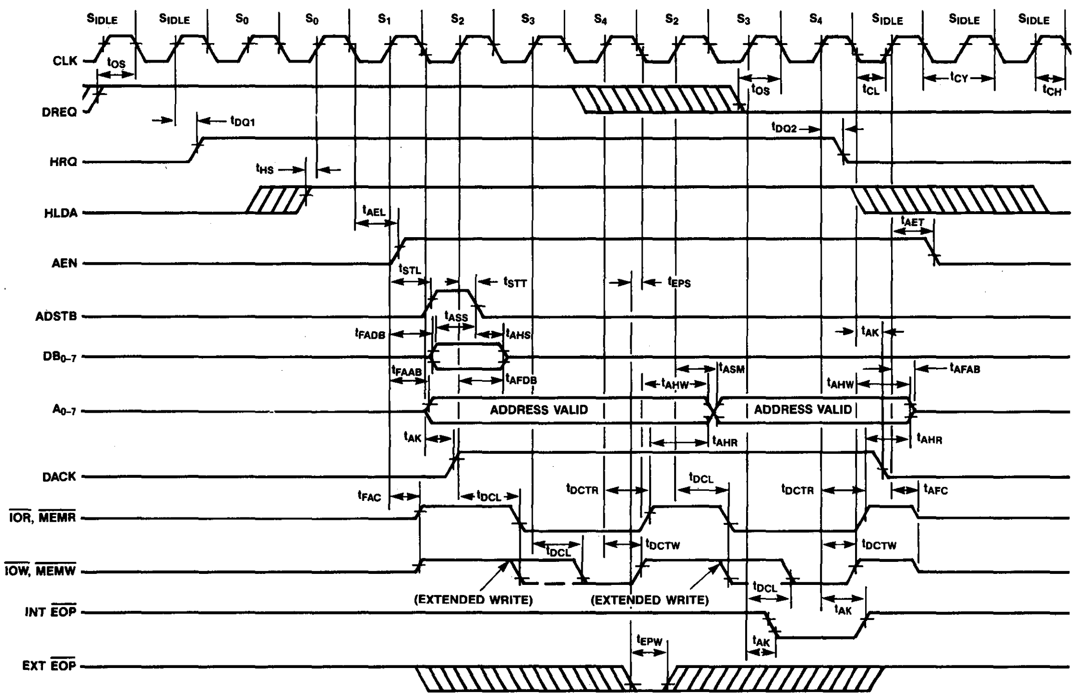
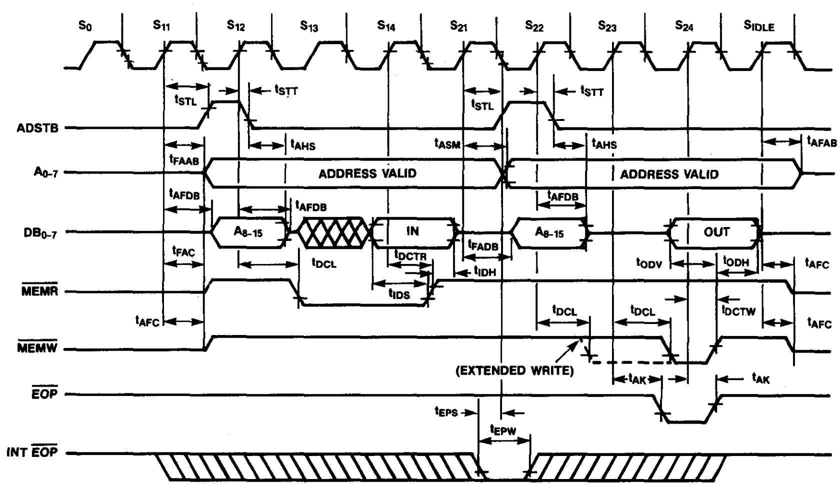


Figure 15: Timing Diagrams (Master Mode)

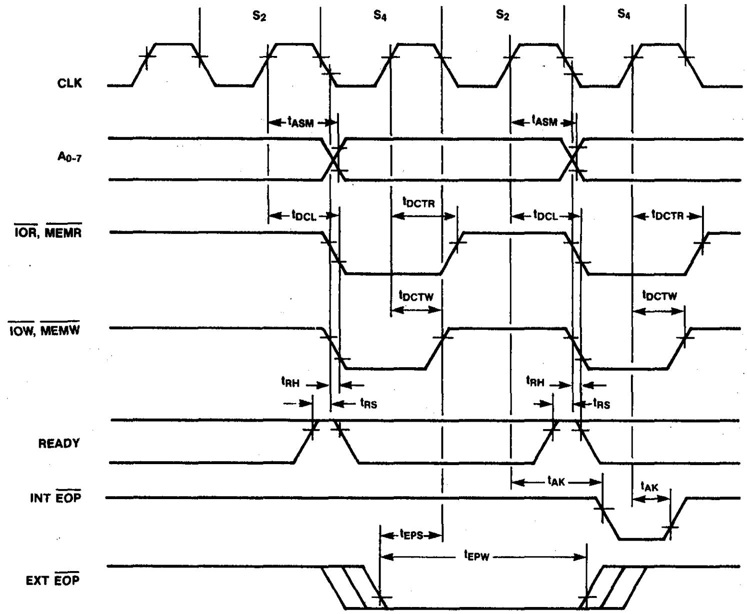
a) DMA Transfer Timing



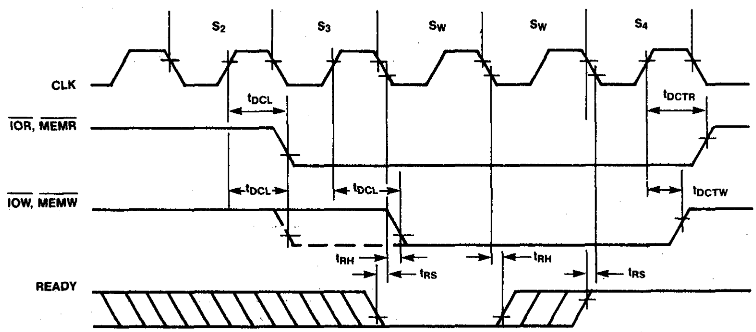
b) Memory-to-Memory Transfer Timing



c) Compressed Transfer Timing



d) Ready Timing



e) Reset Timing

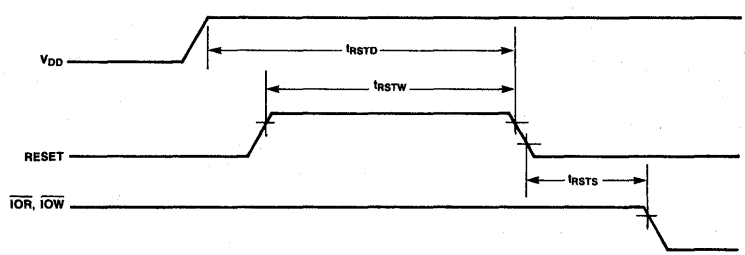
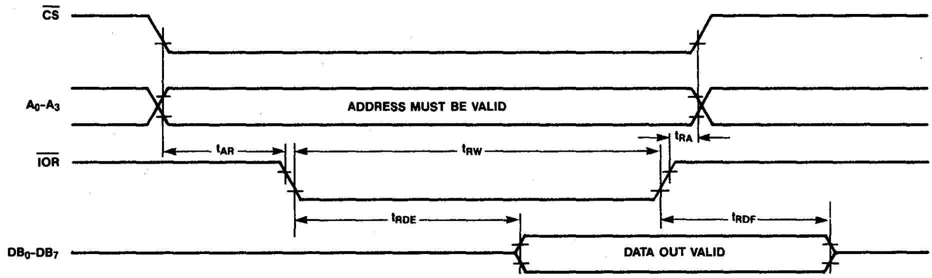
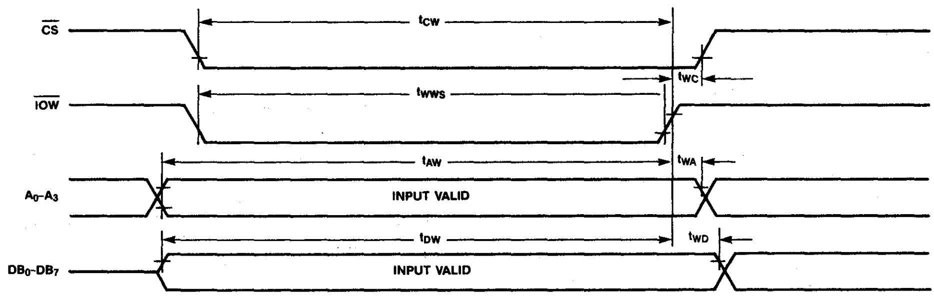


Figure 16: Timing Diagrams (Slave Mode)

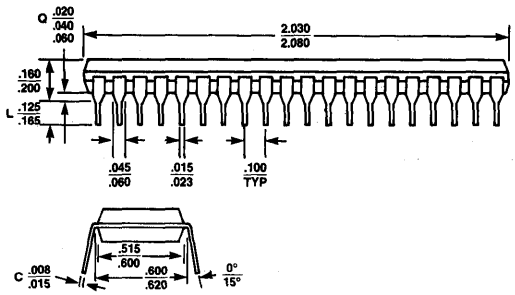
a) Slave Mode Read Timing



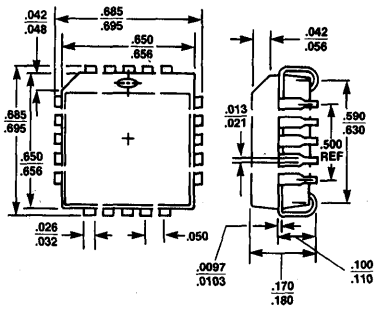
b) Slave Mode Write Timing



PACKAGE DIMENSIONS



Plastic Package



44 Pin PLCC

ORDERING INFORMATION & PRODUCT CODE DIMENSIONS

KS 82C37A X X X

- **SAMSUNG SEMICONDUCTOR** — KS
- **Part Number** — 82C37A
- **Speed**
  - -5 5MHz
  - -8 8MHz
  - -10 10MHz
- **Temperature**
  - C — Commercial (0°C to +70°C)
  - I — Industrial (-40°C to +85°C)
- **Packaging**
  - P — Plastic DIP
  - L — Plastic Leaded Chip Carrier (PLCC)

SAMSUNG products are designated by a Product Code. When ordering, please refer to products by their full code. For unusual, and/or specific packaging or processing requirements not covered by the standard product line, please contact the SAMSUNG MOS Products Group.

KS82C50A

ASYNCHRONOUS COMMUNICATION ELEMENT

Preliminary

FEATURES

- **Single Chip UART/BRG**
- **DC to 10 MHz Operation (DC to 625K Baud)**
- **Crystal or External Clock Input**
- **On Chip Baud Rate Generator 1 to 65535 Divisor Generates 16x Clock**
- **Prioritized Interrupt Mode**
- **Fully TTL/CMOS Compatible**
- **Microprocessor Bus Oriented Interface**
- **80C86/80C88 Compatible**
- **Low Power CMOS Implementation (1 mA/MHz Typ)**
- **Modem Interface**
- **Line Break Generation and Detection**
- **Loopback Mode**
- **Double Buffered Transmitter and Receiver**
- **Single 5V Supply**

DESCRIPTION

The 82C50A Asynchronous Communications Element (ACE) is a high performance programmable Universal Asynchronous Receiver/Transmitter (UART) and Baud Rate Generator (BRG) on a single chip. The device supports data rates from DC to 625K baud (0 - 10 MHz clock).

The ACE receiver circuitry converts start, data, stop and parity bits into a parallel data word. The transmitter circuitry converts a parallel data word into serial form and appends the start, parity and stop bits. The word length is programmable to 5, 6, 7 or 8 data bits. Stop bit selection provides a choice of 1, 1.5 or 2 stop bits.

The Baud Rate Generator divides the clock by a divisor programmable from 1 to $2^{16}-1$ to provide standard RS-232C baud rates when using any one of three industry standard baud rate crystals (1.8432 MHz, 2.4576 MHz or 3.072 MHz). The BAUDOUT programmable clock output provides a buffered oscillator or a 16x (16 times the data rate) baud rate clock for general purpose system use.

To meet the system requirements of a CPU interfacing to an asynchronous channel, the modem control signals RTS, CTS, DSR, DTR, RI, DCD are provided. Inputs and outputs have been designed with full TTL/CMOS compatability in order to facilitate mixed TTL/NMOS/CMOS system design.

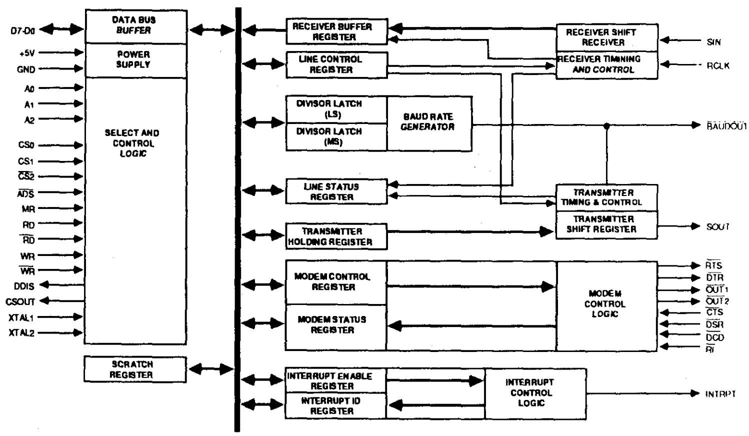


Figure 1 : BLOCK DIAGRAM OF KS82C50A

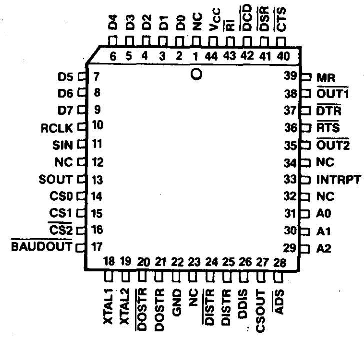


Figure 2a : PLCC CONFIGURATION

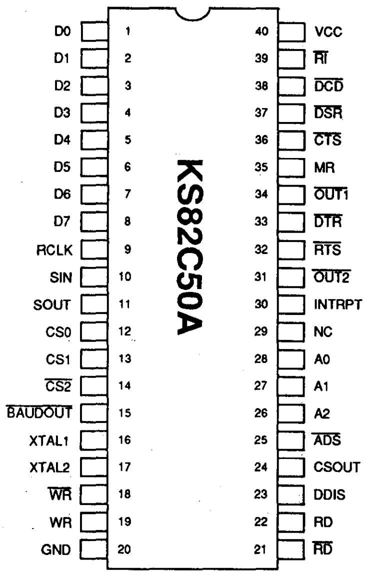


Figure 2b : 40-PIN DIP CONFIGURATION

Table 1 : PIN DESCRIPTIONS

Symbol	Pin(s)	Type	Name and Function
$\overline{RD}$, RD	22, 21	I	$\overline{Read}$, Read: $\overline{RD}$, RD are read inputs which cause the KS82C50A to output data to the data bus (D_0 - D_7). The data output depends upon the register selected by the address inputs A_0, A_1 and A_2. The chip select inputs CS0, CS1 and CS2 enable the $\overline{RD}$, RD inputs. Only an active $\overline{RD}$ or RD, not both, is used to receive data from the KS82C50A during a read operation. If RD is used as the read input, $\overline{RD}$ should be tied high. If $\overline{RD}$ is used as the active read input, RD should be tied low.
$\overline{WR}$, WR	19,18	I	$\overline{Write}$, Write: $\overline{WR}$, WR are write inputs which cause data from the data bus (D_0 - D_7) to be input to the KS82C50A. The data input depends upon the register selected by the address inputs A_0, A_1 and A_2. The chip select inputs CS_0, CS_1 and $\overline{CS_2}$ enable the $\overline{WR}$, WR inputs. Only an active $\overline{WR}$ or WR, not both, is used to transmit data to the KS82C50A during a write operation. If WR is used as the write input, $\overline{WR}$ should be tied high. If $\overline{WR}$ is used as the write input, WR must be tied low.
D_0 - D_7	1 - 8	I/O	Data Bus: The Data Bus provides eight, 3-state input/output lines for the transfer of data, control and status information between the KS82C50A and the CPU. For character formats of less than 8 bits, D7, D6 and D5 are *don't cares* for data write operations and zero for data read operations. These lines are normally in a high impedance state except during read operations. D0 is the Least Significant Bit (LSB) and is the first serial data bit to be received or transmitted.
A_0, A_1, A_2	28, 27,26	I	Register Select: The address lines select the internal registers during CPU bus operations.
$XTAL_1$, $XTAL_2$	16, 17	I, O	Crystal/Clock: Crystal connections for the internal Baud Rate Generator. XTAL1 can also be used as an external clock input, in which case XTAL2 should be left open.
SOUT	11	O	Serial Data Output: Serial data ouputput from the KS82C50A transmitter circuitry. A Mark (1) is a logic one (high) and Space (0) is a logic zero (low). SOUT is held in the Mark condition when the transmitter is disabled, MR is true, the Transmitter Register is empty, or when in the Loop Mode. SOUT is not affected by the $\overline{CTS}$ input.
V_{SS}	20	-	Ground: Power supply ground, 0V
$\overline{CTS}$	36	I	$\overline{Clear\ to\ Send}$: An active low signal, the logical state of the $\overline{CTS}$ pin is reflected in the CTS bit of the (MSR) Modem Status Register (CTS is bit 4 of the MSR, written MSR[4]). A change of state in the $\overline{CTS}$ pin since the previous reading of the MSR causes the setting of DCTS (MSR[0]) of the Modem Status Register. When $\overline{CTS}$ is active (low), the modem is indicating that data on SOUT can be transmitted on the communications link. If $\overline{CTS}$ pin goes inactive (high), the CA82C50A should not be allowed to transmit data out of SOUT. $\overline{CTS}$ pin does not affect Loop Mode operation.
$\overline{DSR}$	37	I	$\overline{Data\ Set\ Ready}$: An active low signal, the logical state of the $\overline{DSR}$ pin is reflected in MSR[5] of the Modem Status Register. DDSR (MSR[1]) indicates whether the DSR pin has changed state since the previous reading of the MSR. When the $\overline{DSR}$ pin is active (low), the modem is indicating that it is ready to exchange data with the CA82C50A, while the $\overline{DSR}$ pin inactive (high) indicates that the modem is not ready for data exchange. The active condition indicates only the condition of the local Data Communications Equipment (DCE), and does not imply that a data circuit has been established with remote equipment.

Table 1 : PIN DESCRIPTIONS con't

Symbol	Pin(s)	Type	Name and Function
DTR	33	O	Data Terminal Ready: An active low signal, the DTR pin can be set (low) by writing a logic one to MCR[0]. Modem Control Register bit 0. This signal is cleared (high) by writing a logic zero to the DTR bit (MCR[0]) or whenever a MR active (high) is applied to the KS82C50A. When active (low), DTR pin indicates to the DCE that the KS82C50A is ready to receive data. In some instances, DTR pin is used as a power on indicator. The inactive (high) state causes the DCE to disconnect the modem from the telecommunications circuit.
RTS	32	O	Request to Send: An active low signal, RTS is an output used to enable the modem. The RTS pin is set low by writing a logic one to MCR[1] bit 1 of the Modem Control Register. The RTS pin is reset high by Master Reset. When active, the RTS pin indicates to the DCE that the KS82C50A has data ready to transmit. In half duplex operations, RTS is used to control the direction of the line.
BAUDOUT	15	O	BAUDOUT: This active low output signal is a 16x clock out used for the transmitter section (16x = 16 times the data rate). The BAUDOUT clock rate is equal to the reference oscillator frequency divided by the specified divisor in the Baud Rate Generator Divisor Latches DLL and DLM. BAUDOUT may be used by the receiver section by tying this output to RCLK.
OUT1	34	O	Output 1: This is an active low general purpose output that can be programmed active (low) by setting MCR[2] (OUT1) of the Modem Control Register to a high level. The OUT1 pin is set high by Master Reset. The OUT1 pin is inactive (high) during loop mode operation.
OUT2	31	O	Output 2: This a an active low general purpose output that can be programmed active (low) by setting MCR[3] (OUT2) of the Modem Control Register to a high level. The OUT2 pin is set high by Master Reset. The OUT2 signal is inactive (high) during loop mode operation.
RI	39	I	Ring Indicator: When low, RI indicates that a telephone ringing signal has been received by the modem or data set. The RI signal is a modem control input whose condition is tested by reading MSR[6] (RI). The Modem Status Register output TERI (MSR[2]) indicates whether the RI input has changed from a low to high since the previous reading of the MSR. If the interrupt is enabled (IER[3] = 1) and RI changes from a high to low, an interrupt is generated. The active (low) state of RI indicates that the DCE is receiving a ringing signal. RI will appear active for approximately the same length of time as the active segment of the ringing cycle. The inactive state of RI will occur during the inactive segments of the ringing cycle, or when ringing is not detected by the DCE. This circuit is not disabled by the inactive condition of DTR.
DCD	38	I	Data Carrier Detect: When active (low), DCD indicates that the data carrier has been detected by the modem or data set. DCD is a modem input whose condition can be tested by the CPU by reading MSR[7] (DCD) of the Modem Status Register, MSR[3] (DDCD) of the Modem Status Register indicates whether the DCD input has changed since the previous reading of the MSR. DCD has no effect on the receiver. If the DCD changes state with the modem status interrupt enabled, an interrupt is generated. When DCD is active (low), the received line signal from the remote terminal is within the limits specified by the DCE manufacturer. The inactive (high) signal indicates that the signal is not within the specified limits, or is not present.

3

Table 1 : PIN DESCRIPTIONS con't

Symbol	Pin(s)	Type	Name and Function
MR	35	I	Master Reset: The MR input forces the KS82C50A into an idle mode in which all serial data activities are suspended. The Modem Control Register (MCR) along with its associated outputs are cleared. The Line Status Register (LSR) is cleared except for the THRE and TEMT bits, which are set. The KS82C50A remains in an idle state until programmed to resume serial data activities. The MR input is a TTL compatible Schmitt trigger.
INTRPT	30	O	Interrupt Request: The INTRPT output goes active (high) when one of the following interrupts has an active (high) condition and is enabled by the Interrupt Enable Register: Receiver Error flag. Received Data Available, Transmitter Holding Register Empty and Modem Status. The INTRPT is reset low upon appropriate service or a MR operation.
SIN	10	I	Serial Data Input: The SIN input is the serial data input from the communication line or modem to the KS82C50A receiver circuits. A Mark (1) is high, and a Space (0) is low. Data inputs on SIN are disabled when operating in the loop mode.
V_{DD}	40	-	Power Supply: +5V ±10% DC Supply. A 0.1 µA decoupling capacitor from V_{DD} (pin 40) to V_{SS} (pin 20) is recommended.
CS_0, CS_1, $\overline{CS_2}$	12, 13, 14	I	Chip Select: The Chip Select inputs act as enable signals for the write ($\overline{WR}$, WR) and read ($\overline{RD}$, RD) input signals. The Chip select inputs are latched by the $\overline{ADS}$ input.
NC	29	-	Do Not Connect
CSOUT	24	O	Chip Select Out: When active (high), this pin indicates that the chip has been selected by active CS_0, CS_1 and $\overline{CS_2}$ inputs. No data trasfer can be initiated until CSOUT is a logic one, active (high).
DDIS	23	O	Driver Disable: This output is inactive (low) when the CPU is reading data from the KS82C50A. An active (high) DDIS output can be used to disable an external transceiver when the CPU is reading data.
$\overline{ADS}$	25	I	Address Strobe: When active (low), $\overline{ADS}$ latches the Register Select (A0, A1 and A2) and Chip Select (CS_0, CS_1 and $\overline{CS_2}$) inputs. An active $\overline{ADS}$ is required when the Register Select pins are not stable for the duration of the read or write operation, multiplexed mode. If not required, the $\overline{ADS}$ input should be tied low, non-multiplexed mode.
RCLK	9	I	This input is the 16x Baud Rate Clock for the receiver section of the KS82C50A. This input may be provided from the $\overline{BAUDOUT}$ output or an external clock.

Table 2a : AC CHARACTERISTICS: READ AND WRITE (T_A=0°C to +70°C, V_{DD}=5.0V ±10%)

Symbol	Parameter	Test Conditions	Limits (10 MHz)		Units
			Min	Max	
tADS	Address strobe width		50	-	ns
tAH	Address hold time		0	-	ns
tAR	RD, $\overline{RD}$ delay from address	Note 1	60	-	ns
tAS	Address setup time	Note 1	60	-	ns
tAW	WR, $\overline{WR}$ delay from address	Note 1	60	-	ns
tCH	Chip select hold time		0	-	ns
tCS	Chip select setup time	Note 1	60	-	ns
tCSC	Chip select output delay from select	Note 1	-	100	ns
tCSR	RD, $\overline{RD}$ delay from chip select	Note 1	50	-	ns
tCSW	WR, $\overline{WR}$ delay from select	Note 1	50	-	ns
tDD	RD, $\overline{RD}$ to driver disable delay		-	75	ns
tDDD	Delay from RD, $\overline{RD}$ to data		-	120	ns
tDH	Data hold time		60	-	ns
tDIW	RD, $\overline{RD}$ strobe width		150	-	ns
tDOW	WR, $\overline{WR}$ strobe width		150	-	ns
tDS	Data setup time		90	-	ns
tHZ	RD, $\overline{RD}$ to floating data delay		10	75	ns
tRA	Address hold time from RD, $\overline{RD}$	Note 1	20	-	ns
tRC	Read cycle delay	Note 1	270	-	ns
tRCS	Chip select hold time from RD, $\overline{RD}$	Note 1	20	-	ns
tWA	Address hold time from WR, $\overline{WR}$	Note 1	20	-	ns
tWC	Write cycle delay	Note 1	270	-	ns
tWCS	Chip select hold time from WR, $\overline{WR}$	Note 1	20	-	ns
RC	Read cycle = tAR + tDIW + tRC		500	-	ns
WC	Write cycle = tAW + tDOW + tWC		500	-	ns

Notes: 1. When using the KS82C50A in the multiplexed mode ($\overline{ADS}$ operational), it will operate in 80C86/88 systems with a maximum 3 MHz operating frequency.

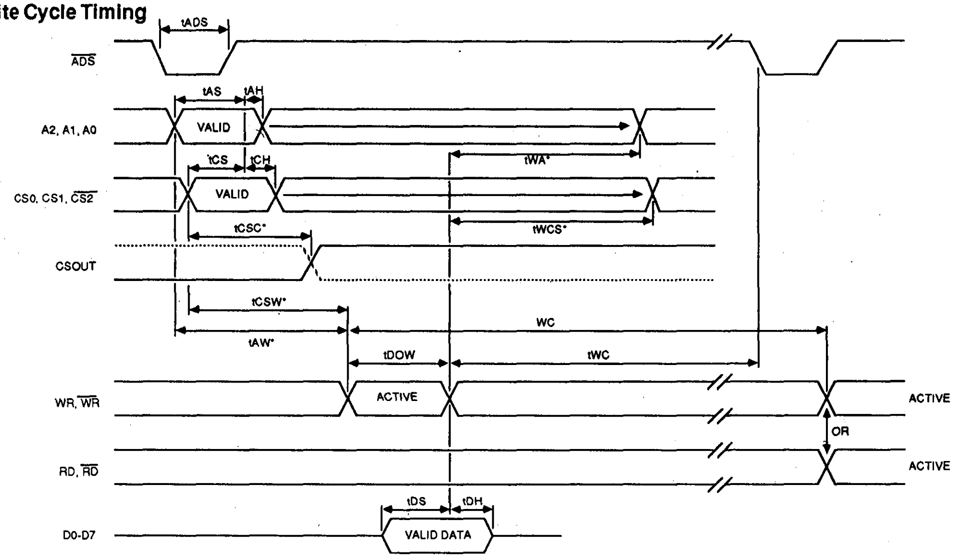
Table 2b : AC CHARACTERISTICS: BRG, RCVR,XMTR & MODEM CONTROL (T_A=0°C to +70°C, V_{DD}=5.0V ±10%)

Symbol	Parameter	Test Conditions	Limits (10 MHz) Min	Limits (10 MHz) Max	Units
N	Baud divisor		1	2^{16}-1	
tBHD	Baud output positive edge delay		-	175	ns
tBLD	Baud output negative edge delay		-	175	ns
tHW	Baud output up time	f_X = 3 MHz	250	-	ns
tLW	Baud output down time	f_X = 3 MHz	425	-	ns
tRINT	Delay from RD, $\overline{RD}$ (RD RBR or RD LSR to Reset Interrupt)		-	1	μs
tSCD	Delay from RCLK to sample time		-	2	μs
tSINT	Delay from stop to Set Interrupt		-	1	RCLK Cycles
tHR	Delay from WR, $\overline{WR}$ (WR THR) to Reset Interrupt		-	175	ns
tIR	Delay from RD, $\overline{RD}$ (RD IIR) to Reset Interrupt (THRE)		-	250	ns
tIRS	Delay from initial INTR reset to Transmit Start		24	40	$\overline{BAUDOUT}$ Cycles
tSI	Delay from initial write to interrupt	Note 1	16	24	$\overline{BAUDOUT}$ Cycles
tSTI	Delay from stop to interrupt (THRE)		8	8	$\overline{BAUDOUT}$ Cycles
tMDO	Delay from WR, $\overline{WR}$ (WR MCR) to output		-	200	ns
tRIM	Delay to Reset Interrupt from RD, $\overline{RD}$ (RD MSR)		-	250	ns
tSIM	Delay to Set Interrupt from MODEM input		90	-	ns

Notes: 1. tSI is a minimum of 16 and a mximum of 48 BAUDOUT Cycles.

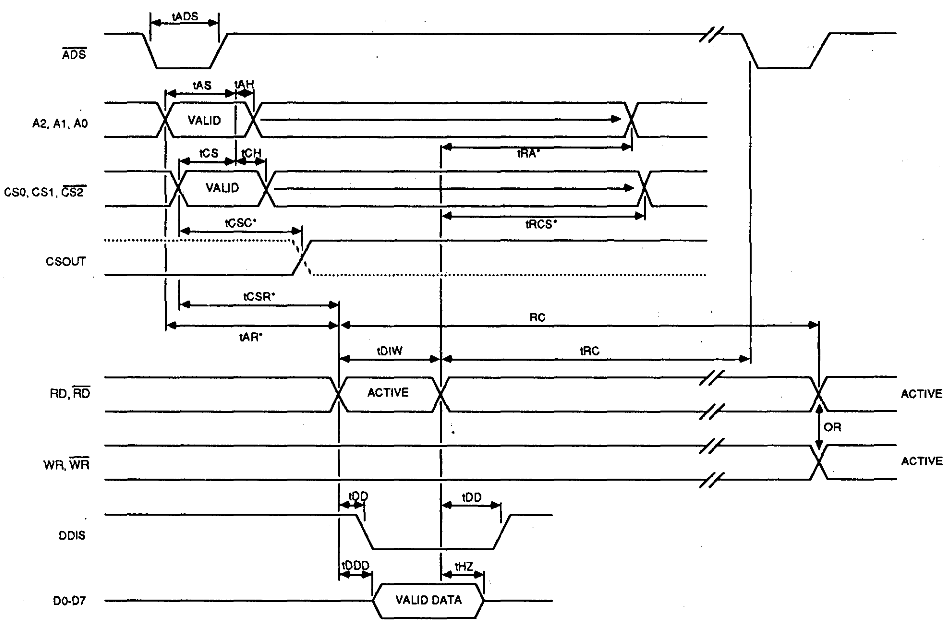
Figure 3 : TIMING DIAGRAMS

a) Write Cycle Timing



* Applicable only when ADS is low

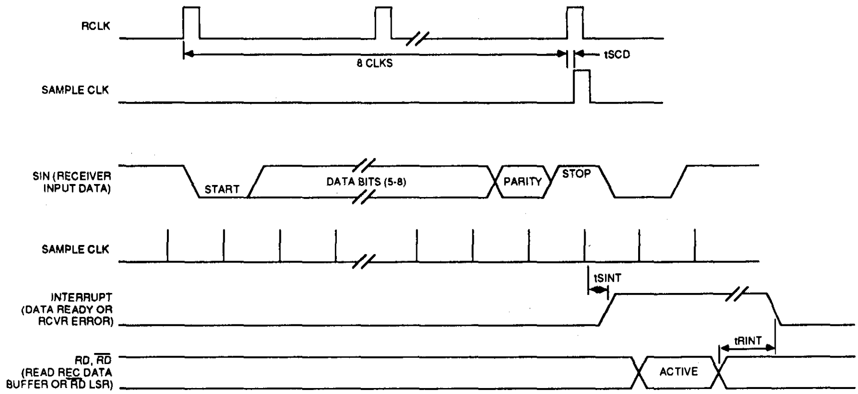
b) Read Cycle Timing



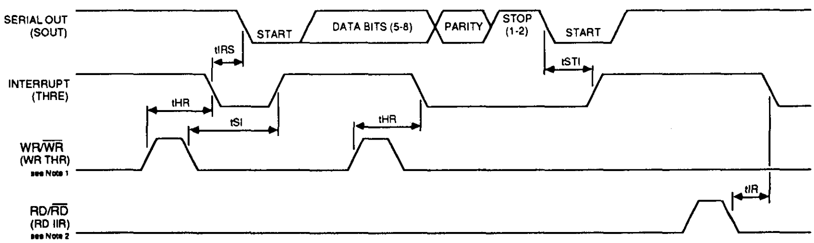
* Applicable only when ADS is low

Figure 3 : TIMING DIAGRAMS con't

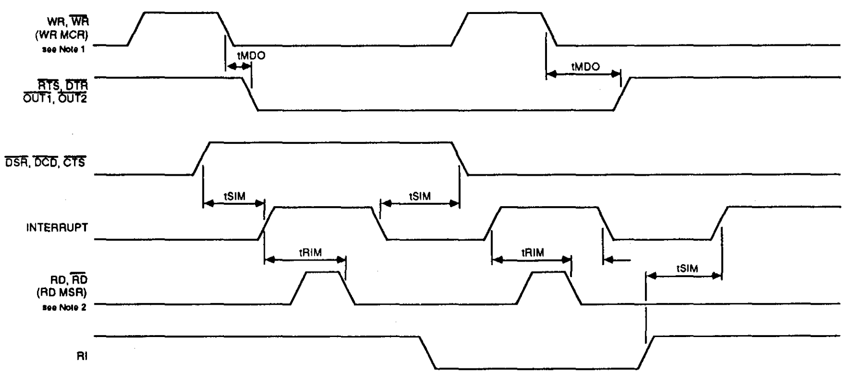
c) Receiver Timing



d) Transmitter Timing



e) Modem Controls Timing



Notes: 1. See Write Cycle Timing
2. See Read Cycle Timing

Figure 3 : TIMING DIAGRAMS con't

f) $\overline{\text{BAUDOUT}}$ Timing

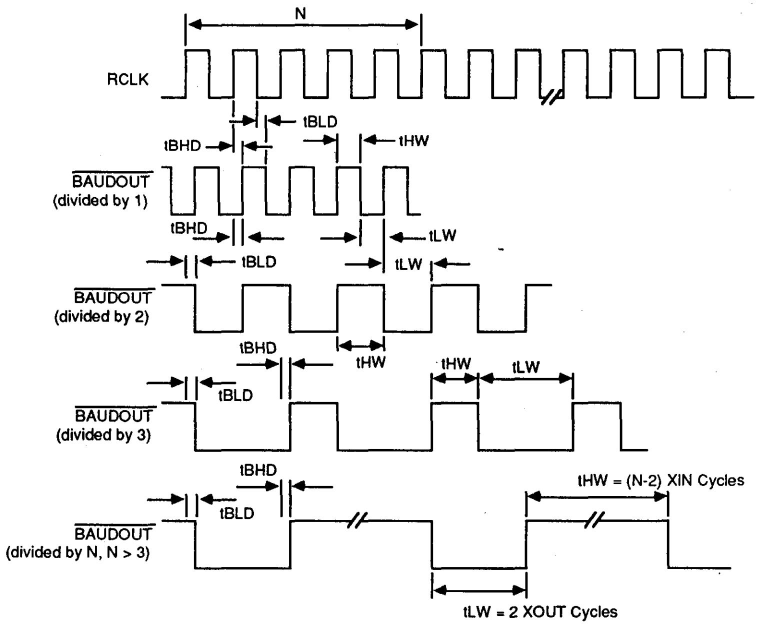


Table 3 : CAPACITANCE (TA=25°C, VDD=VSS=0V, VIN=+5V or VSS)

Symbol	Parameter	Test Conditions	Typical Values	Units
CIN	Input capacitance	Freq = 1 MHz	15	pF
COUT	Output capacitance	Unmeasured pins	15	pF
CI/O	I/O capacitance	returned to VSS	20	pF

3

Table 4 : OPERATING CONDITIONS

Operating Voltage Range	+4.5V to +5.5V
Operating Temperature Range	
Commercial	0°C to +70°C
Industrial	-40°C to +85°C
Military	-55°C to +125°C

Table 5 : ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0 Volts
Input, Output or I/O Voltage Applied	V_{SS} -0.5V to V_{DD} +0.5V
Storage Temperature Range	-65°C to +150°C
Maximum Package Power Dissipation	1 Watt
Junction Temperature	+150°C
Lead Temperature (Soldering, 10 seconds)	+260°C
θjc	12°C/W (Cerdip), 17°C/W (LCC)
θja	36°C/W (Cerdip), 41°C/W (LCC)

Table 6 : DC CHARACTERISTICS (T_A=0°C to +70°C, V_{DD}=5.0V ±10%)

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
VIH	Logical one input voltage		2.0	-	V
VIL	Logical zero input voltage		-	0.8	V
VTH	Schmitt trigger logic one input voltage	MR input	2.0	-	V
VTL	Schmitt trigger logic zero input voltage	MR input	-	0.8	V
VIH (CLK)	Logical one clock voltage	External Clock	V_{DD}-0.8	-	V
VIL (CLK)	Logical zero clock voltage	External Clock	-	0.8	V
VOH	Output high voltage	IOH=-2.5 mA	3.0	-	V
		IOH=-100 μA	V_{DD}-0.4	-	V
VOL	Output low voltage	IOL=+2.5 mA	-	0.4	V
II	Input leakage current	$V_{IN}=V_{SS}$ or V_{DD}	-1.0	+1.0	μA
IO	Input/output leakage current	$V_{OUT}=V_{SS}$ or V_{DD}	-10.0	+10.0	μA
IDDOP	Operating power supply current	External Clock, Freq=2.4576 MHz, V_{DD}=5.5V, $V_{IN}=V_{DD}$ or V_{SS}, Outputs open	-	6	mA
IDDSB	Standby supply current	V_{DD}=5.5V, $V_{IN}=V_{DD}$ or V_{SS}, Outputs open	-	100	μA

REGISTERS

The three types of internal registers in the KS82C50A used in the operation of the device are control, status and data registers. The control registers are the Bit Rate Select Register DLL and DLM, Line Control Register, Interrupt Enable Register and the Modem Control registers, while the status registers are the Line Status Registers and the Modem Status Register. The data registers are the Receiver Buffer Register and Transmitter Holding Register. The Address, Read and Write inputs are used in conjunction with the Divisor Latch Access Bit in the Line Control Register (LCR[7]) to select the register to be written or read (see Table 7). Individual bits within these registers are referred to by the register mnemonic and the bit number in square brackets. An example, LCR[7] refers to Line Control Register Bit 7.

The Transmitter Buffer Register and Receiver Buffer Register are data registers holding from 5 to 8 data bits. If less than eight data bits are transmitted, data is right justified to the LSB. Bit 0 of a data word is always the first serial data bit received and transmitted. The KS82C50A data registers are double buffered so that read and write operations can be performed at the same time the UART is performing the parallel to serial and serial to parallel conversion. This provides the microprocessor with increased flexibility in its read and write timing.

Table 7 : ACCESSING KS82C50A INTERNAL REGISTERS

Mnemonic	Register	DLAB	A2	A1	A0
RBR	Receiver Buffer Register (read only)	0	0	0	0
THR	Transmitter Holding Register (write only)	0	0	0	0
IER	Interrupt Enable Register	0	0	0	1
IIR	Interrupt Identification Register (read only)	X	0	1	0
LCR	Line Control Register	X	0	1	1
MCR	Modem Control Register	X	1	0	0
LSR	Line Status Register	X	1	0	1
MSR	Modem Control Register	X	1	1	0
SCR	Scratch Register	X	1	1	1
DLL	Divisor Latch (LSB)	1	0	0	0
DLM	Divisor Latch (MSB)	1	0	0	1

Notes: 1. X = Don't Care
2. 0 = Logic Low
3. 1 = Logic High

Line Control Register (LCR)

The format of the data character is controlled by the Line Control Register. The contents of the LCR may be read, eliminating the need for separate storage of the line characteristics in system memory. The contents of the LCR are described in Table 8.

LCR[0] and LCR[1] word length select bit 0, word length select bit 1: The number of bits in each transmitted or received serial character is programmed per Table 9.

LCR[2] Stop Bit Select: LCR[2] specifies the number of stop bits in each transmitted character. If LCR[2] is a logic zero, one stop bit is generated in the transmitted data. If LCR[2] is a logic one when a 5-bit word length is selected, 1.5 stop bits are generated. If LCR[2] is a logic one when either a 6-, 7- or 8-bit word length is selected, two stop bits are generated. The receiver checks for two stop bits if programmed.

LCR[3] Parity Enable: When LCR[3] is high, a parity bit between the last data word bit and stop bit is generated and checked.

LCR[4] Even Parity Select: When parity is enabled (LCR[3]=1), LCR[4]=0 selects odd parity, and LCR[4]=1 selects even parity.

LCR[5] Stick Parity: When LCR[3, 4 and 5] are logic one the Parity bit is transmitted and checked as a logic zero. If LCR[3 and 5] are one and LCR[4] is a logic zero then the parity bits is transmitted and checked as a logic one. If LCR[5] is a logic zero Stick Parity is disabled.

LCR[6] Break Control: When LCR[6] is set to logic one, the serial output (SOUT) is forced to the spacing (logic zero) state. The break is disabled by setting LCR[6] to a logic zero. The Break Control bit acts only on SOUT and has no effect on the transmitter logic. Break Control enables the CPU to alert a terminal in a computer communications system. If the following sequence is used, no erroneous or extraneous characters will be transmitted because of the break.

1. Load an all 0s pad character in response to THRE.
2. Set break in response to the next THRE.
3. Wait for the transmitter to be idle, (TTEMT=1), and clear break when normal transmission has to be restored.

During the break, the transmitter can be used as a character timer to accurately establish the break duration.

LCR[7] Divisor Latch Access Bit (DLAB): LCR[7] must be set high (logic one) to access the Divisor Latches DLL and DLM of the Baud Rate Generator during a read or write operation. LCR[7] must be input low to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

3

Table 8 : LCR BIT DEFINITIONS

Bit Number	Function
0	Word Length Select Bit 0 (WLS0)
1	Word Length Select Bit 1 (WLS1)
2	Stop Bit Select (STB)
3	Parity Enable (EN)
4	Even Parity Select (EPS)
5	Stick Parity
6	Set Break
7	Divisor Latch Access Bit (DLAB)

Table 9 : LCR WORD LENGTH SELECTION

LCR[1]	LCR[2]	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

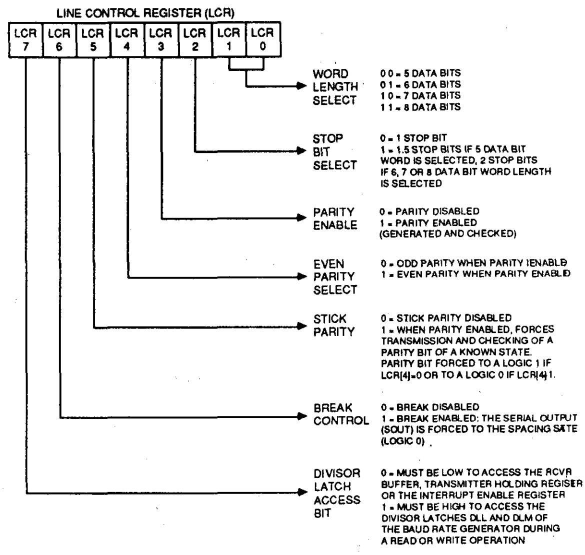


Figure 4 : LINE CONTROL REGISTER

Line Status Register (LSR)

The LSR is a single register that provides status indications. The LSR is usually the first register read by the CPU to determine the cause of an interrupt or to poll the status of the CA82C50A.

Three error flags OE, FE and PE provide the status of any error conditions detected in the receiver circuity. During reception of the stop bits, the error flags are set high by an error condition. The error flags are not reset by the absence of an error condition in the next received character. The flags reflect the last charater only if no overrun occurred. The Overrun Error (OE) indicates that a character in the Receiver Buffer Register has been overwritten by a character from the Receiver Shift Register before being read by the CPU. The character is lost. Framing Error (FE) indicates that the last character received contained incorrect (low) stop bits. This is caused by the absence of the required stop bit or by a stop bit too short to be detected. Parity Error (PE) indicates that the last character received contained a parity error based on the programmed and calculated parity of the received character.

The Break Interrupt (BI) status bit indicates that the last character received was a break character. A break character is an invalid data character, with the entire character, including parity and stop bits, logic zero.

The Transmitter Holding Register Empty (THRE) bit indicates that the THR register is empty and ready to receive another character. The Transmission Shift Register Empty (TEMT) bit indicates that the Transmitter Shift Register is empty, and the KS82C50A has completed transmission of the last character. If the interrupt is enabled (IER[1]), an active THRE causes an interrupt (INTRPT).

The Data Ready (DR) bit indicates that the RBR has been loaded with a received character (included Break) and that the CPU may access this data.

Reading LSR clears LSR[1] - LSR[4], (OE, PE, FE and BI).

The contents of the Line Status Register are indicated in Table 10, and are described below.

LSR[0] Data Ready (DR): Data Ready is set high when an incoming character has been received and transferred into the Receiver Buffer Register. LSR[0] is reset low by a CPU read of the data in the Receiver Buffer Register.

LSR[1] Overrun Error (OE): Overrun Error indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, overwriting the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

LSR[2] Parity Error (PE): PE indicates that the received data character does not have the correct even or odd parity, as selected by the Even Parity Select bit (LCR[4]). The PE bit is set high upon detection of a parity error, and is reset low when the CPU reads the contents of the LSR.

LSR[3] Framing Error (FE): FE indicates that the received character did not have a valid stop bit. LSR[3] is set high when the stop bit following the last data bit or parity bit is detected as a zero bit (spacing level). The FE indicator is reset low when the CPU reads the contents of the LSR.

LSR[4] Break Interrupt (BI): BI is set high when the received data input is held in the spacing (logic zero) state for longer than a full word transmission time (start bit+data bits+parity+stop bits). The BI indicator is reset when the CPU reads the contents of the Line Status Register.

LSR[1] – LSR[4] are the error conditions that produce a Receiver Line Status interrupt (priority 1 interrupt in the Interrupt Identification Register (IIR)) when any of the conditions are detected. This interrupt is enabled by setting IER[2]=1 in the Interrupt Enable Register.

LSR[5] Transmitter Holding Register Empty (THRE): THRE indicates that the KS82C50A is ready to accept a new character for transmission. The THRE bit is set high when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. LSR[5] is reset low when the CPU loads the Transmitter Holding Register. LSR[5] is not reset by a CPU read of the LSR.

When the THRE interrupt is enabled (IER[1]=1), THRE causes a priority 3 interrupt in the IIR. If THRE is the interrupt source indicated in IIR, INTRPT is cleared by a read of the IIR.

LSR[6] Transmitter Empty (TEMT): TEMT is set high when the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty. LSR[6] is reset low when a character is loaded into the THR and remains low until the character is trasferred out of SOUT. TEMT is not reset low by a CPU read of the LSR.

LSR[7]: This bit is permanently set to logic zero.

Table 10 : LSR BIT DEFINITIONS

Bit Number	Function	Logic 1	Logic 0
0	Data Ready (DR)	Ready	Not Ready
1	Overrun Error (OE)	Error	No Error
2	Parity Error (PE)	Error	No Error
3	Framing Error (FE)	Error	No Error
4	Break Interrupt (BI)	Break	No Break
5	Transmitter Holding Register Empty (THRE)	Empty	Not Empty
6	Transmitter Empty (TEMT)	Empty	Not Empty
7	Not Used		

Modem Control Register (MCR)

The MCR controls the interface with the modem or data set as described below. The MCR can be written and read. The $\overline{RTS}$, $\overline{DTR}$, $\overline{OUT1}$ and $\overline{OUT2}$ outputs are directly controlled by their control bits in this register. A high input asserts a low (true) at the output pins.

MCR[0]: When MCR[0] is set high, the $\overline{DTR}$ output is forced low. When MCR[0] is reset low, the $\overline{DTR}$ output is forced high. The $\overline{DTR}$ output of the KS82C50A may be input into an EIA inverting line driver as the 1488 to obtain the proper polarity input at the modem or data set.

MCR[1]: When MCR[1] is set high, the $\overline{RTS}$ output is forced low. When MCR[1] is reset low, the $\overline{RTS}$ output is forced high. The $\overline{RTS}$ output of the KS82C50A may be input into an EIA inverting line driver as the 1488 to obtain the proper polarity input at the modem or data set.

MCR[2]: When MCR[2] is set high, the $\overline{OUT1}$ output is forced low. When MCR[2] is reset low, the $\overline{OUT1}$ output is forced high. $\overline{OUT1}$ is a user designated output.

MCR[3]: When MCR[3] is set high, the $\overline{OUT2}$ output is forced low. When MCR[3] is reset low, the $\overline{OUT2}$ output is forced high. $\overline{OUT2}$ is a user designated output.

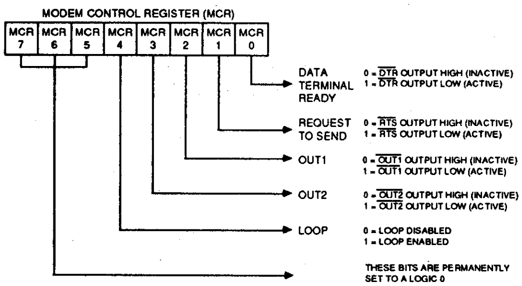


Figure 5 : MODEM CONTROL REGISTER

MCR[4]: MCR[4] provides a local loopback feature for diagnostic testing of the KS82C50A. When MCR[4] is set high. Serial Output (SOUT) is set to the marking (logic one) state, and the receiverr data input Serial Input (SIN) is disconnected. The output of the Transmitter Shift Register is looped back into the Receiver Shift Register input. The four modem control inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$ and $\overline{RI}$) are disconnected. The four modem control outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OUT1}$ and $\overline{OUT2}$) are internally connected to the four modem control inputs. The modem control output pins are forced to their inactive state (high). In the diagnostic mode, data transmitted is immediately received. This allows the CPU to verify KS82C50A transmit and receive data paths.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The modem control interrupts are also operational, but the interrupt sources are now the lower four bits of the MCR instead of the four modem control inputs. The interrupts are still controlled by the Interrupt Enable Register.

MCR[5] – MCR[7]: Bits are permanently set to logic zero.

Table 11 : MCR BIT DEFINITIONS

Bit Number	Function	Logic 1	Logic 0
0	Data Terminal Ready (DTR)	$\overline{DTR}$ Output Low	$\overline{DTR}$ Output High
1	Request to Send (RTS)	$\overline{RTS}$ Output Low	$\overline{RTS}$ Output High
2	OUT1	$\overline{OUT1}$ Output Low	$\overline{OUT1}$ Output High
3	OUT2	$\overline{OUT2}$ Output Low	$\overline{OUT2}$ Output High
4	LOOP	LOOP Enabled	LOOP Disabled
5	0		
6	0		
7	0		

3

Modem Status Register (MSR)

The MSR provides the CPU with status of the modem input lines from the modem or peripheral device. The MSR allows the CPU to read the modem signal inputs by accessing the data bus interface of the KS82C50A. In addition to the current status information, four bits of the MSR indicate whether the modem inputs have changed since the last reading of the MSR. The delta status bits are set high when a control input from the modem changes state, and reset low when the CPU reads the MSR.

The modem input lines are $\overline{CTS}$ (pin 36), $\overline{DSR}$ (pin 37), $\overline{RI}$ (pin 39) and $\overline{DCD}$ (pin 38). MSR[4] – MSR[7] are status indications of these lines. The status indications follow the status of the input lines. If the modem status interrupt in the Interrupt Enable Register is enabled (IER[3]), a change of state in a modem input signals will be reflected by the modem status bits in the IIR register and an interrupt (INTRPT) is generated. The MSR is a priority 4 interrupt. The contents of the Modem Status Register are described in Table 12.

Note that the state (high or low) of the status bits are inverted versions of the actual input pins.

MSR[0] Delta Clear to Send (DCTS): DCTS indicates that the CTS input (pin 36) to the KS82C50A has changed state since the last time it was read by the CPU.

MSR[1] Delta Data Set Ready (DDSR): DDSR indicates that the DSR input (pin 37) to the KS82C50A has changed state since the last time it was read by the CPU.

MSR[2] Trailing Edge of Ring Indicator (TERI): TERI indicates that the RI input (pin 39) to the KS82C50A has changed state (L→H) since the last time it was read by the CPU.

MSR[3] Delta Data Carrier Detect (DDCD): DDCD indicates that the DCD input (pin 38) to the KS82C50A has changed state since the last time it was read by the CPU.

MSR[4] Clear to Send (CTS): CTS is the status of the CTS input (pin 36) from the modem indicating to the KS82C50A that the modem is ready to receive data from the transmitter output (SOUT). If the KS82C50A is in the loop mode (MCR[4]=1), MSR[4] is equivalent to RTS in the MCR.

MSR[5] Data Set Ready (DSR): DSR is a status of the DSR input (pin 37) from the modem to the KS82C50A which indicates that the modem is ready to provide received data to the receiver circuitry. If KS82C50A is in the loop mode (MCR[4]=1), MSR[5] is equivalent to DTR in the MCR.

MSR[6] Ring Indicator (RI): RI indicates the status of the RI input (pin 39). If the KS82C50A is in the loop mode (MCR[4]=1), MSR[6] is equivalent to OUT1 in the MCR.

MSR[7] Data Carrier Detect (DCD): DCD indicates the status of the Data Carrier Detect (DCD) input (pin 38). If the KS82C50A is in the loop mode (MCR[4]=1), MSR[4] is equivalent to OUT2 of the MCR.

The modem status inputs (RI, DCD, DSR and CTS) reflect the modem input lines with any change of status. Reading the MSR register well clear the delta modem status indications but has no effect on the status bits. The status bits reflect the state of the input pins regardless of the mask control signals. If a DCTS, DDSR, TERI or DDCD are true and a state change occurs during a read operation (DISTR, DISTR), the state change is not indicated in the MSR. If DCTS, DDSR, TERI or DDCD are false and a state change occurs during a read operation, the state change is indicated after the read operation.

For LSR and MSR, the setting of status bits is inhibited during status register read (DISTR, DISTR) operations. If a status condition is generated during a read (DISTR, DISTR) operation, the status bit is not set until the trailing edge of the read (DISTR, DISTR).

If a status bit is set during a read (DISTR, DISTR) operation, and the same status condition occurs, that status bit will be cleared at the trailing edge of the read (DISTR, DISTR) instead of being set again.

Table 12 : MSR BIT DEFINITIONS

Bit Number	Function
0	Delta Clear to Send (DCTS)
1	Delta Data Set Ready (DDSR)
2	Trailing Edge of Ring Indicator (TERI)
3	Delta Data Carrier Detect (DDCD)
4	Clear to Send (CTS)
5	Data Set Ready (DSR)
6	Ring Indicator (RI)
7	Data Carrier Detect (DCD)

Baud Rate Select Register (BRSR)

The KS82C50A contains a programmable Baud Rate Generator (BRG) that divides the clock (DC to 10 MHz) by any divisor from 1 to $2^{16}-1$ (see BRG description). The output frequency of the BRG is 16x the data rate:

Divisor # = Frequency Input ÷ (Baud Rate x 16)

Table 13: DIVISOR LATCH BIT DEFINITIONS

Least Significant Bit		Most Significant Bit	
Bit Number	Function	Bit Number	Function
0	DLL[0]	8	DLM[0]
1	DLL[1]	9	DLM[1]
2	DLL[2]	10	DLM[2]
3	DLL[3]	11	DLM[3]
4	DLL[4]	12	DLM[4]
5	DLL[5]	13	DLM[5]
6	DLL[6]	14	DLM[6]
7	DLL[7]	15	DLM[7]

Two 8-bit registers store the divisor in 16-bit binary format. These Divisor Latch registers must be loaded during initialization. On loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded, preventing long counts on initial load.

Sample Divisor Number Calculation:

Given:	Desired Baud Rate 1200 Baud Frequency Input 1.8432 MHz
Formula:	Divisor # = Frequency Input ÷ (Baud Rate x 16) Divisor # = 1843200 ÷ (1200 x 16)
Answer:	Divisor # = 96 = 60_{HEX} → DLL = 01100000 DLM = 00000000
Check:	The Divisor #96 will divide the input frequency 1.8432 MHz down to 19200 which is 16 times the desired baud rate.

Receiver Buffer Register (RBR)

The receiver circuitry in the KS82C50A is programmable for 5, 6, 7 or 8 data bits per character. For words of less than 8 bits, the data is right justified to the least significant bit (LSB = Data Bit 0, RBR[0]). Data Bit 0 of a data word (RBR[0]) is the first data bit received. The unused bits in a character less than 8 bits are output low to the parallel output by the KS82C50A.

Received data at the SIN input pin is shifted into the Receiver Shift Register by the 16x clock provided at the RCLK input. This clock is synchronized to the incoming data based on the position of the start bit. When a complete character is shifted into the Receiver Shift Register, the assembled data bits are parallel loaded into the Receiver Buffer Register. The DR flag in the LSR register is set.

Double buffering of the received data permits continuous reception of data without losing received data. While the Receiver Shift Register is shifting a new character into the KS82C50A, the Receiver Buffer Register is holding a previously received character for the CPU to read. Failure to read the data in the RBR before complete reception of the next character result in the loss of the data in the Receiver Register. The OE flag in the LSR register indicates the overrun condition.

Table 14 : RBR BIT DEFINITIONS

Bit Number	Function
0	Data - RBR[0]
1	Data - RBR[1]
2	Data - RBR[2]
3	Data - RBR[3]
4	Data - RBR[4]
5	Data - RBR[5]
6	Data - RBR[6]
7	Data - RBR[7]

Transmitter Holding Register (THR)

The Transmitter Holding Register (THR) holds parallel data from the data bus (D0 – D7) until the Transmitter Shift Register is empty and ready to accept a new character for transmission. The transmitter and receiver word length and number stop bits are the same. If the character is less than eight bits, unused bits at the microprocessor data bus are ignored by the transmitter.

Data Bit 0 (THR[0]) is the first serial data bit transmitted. The THRE flag (LSR[5]) reflects the THR status, the TEMT flag (LSR[5]) indicates if both THR and TSR are empty.

Table 15 : THR BIT DEFINITIONS

Bit Number	Function
0	Data - THR[0]
1	Data - THR[1]
2	Data - THR[2]
3	Data - THR[3]
4	Data - THR[4]
5	Data - THR[5]
6	Data - THR[6]
7	Data - THR[7]

Scratchpad Register (SCR)

This 8-bit Read/Write register has no effect on the KS82C50A. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

Table 16 : SCR BIT DEFINITIONS

Bit Number	Function
0	Data - SCR[0]
1	Data - SCR[1]
2	Data - SCR[2]
3	Data - SCR[3]
4	Data - SCR[4]
5	Data - SCR[5]
6	Data - SCR[6]
7	Data - SCR[7]

INTERRUPT STRUCTURE

Interrupt Identification Register (IIR)

The KS82C50A has interrupt capability for interfacing to current microprocessors. In order to minimize software overhead during data character transfers, the KS82C50A prioritizes interrupts into four levels:

- Receiver Line Status (priority 1)
- Received Data Ready (priority 2)
- Transmitter Holding Register Empty (priority 3)
- Modem Status (priority 4)

Information indicating that a prioritized interrupt is pending and the type of interrupt is stored in the Interrupt Identification Register (IIR). When addressed during chip select time, the IIR indicates the highest priority interrupt pending. No other interrupts are acknowledged until the interrupt is serviced by the CPU. The contents of the IIR are indicated in Table 17 and are described below.

IIR[0]: IIR[0] can be used in either a hardwired prioritized or polled environment to indicate if an interrupt is pending. When IIR[0] is low, an interrupt is pending, and IIR contents may be used as a pointer to the appropriate interrupt service routine. When is high, no interrupt is pending.

IIR[1] and IIR[2]: IIR[1] and IIR[2] are used to identify the highest priority interrupt pending as indicated in Table 17.

IIR[3] – IIR[7]: These five bits of the IIR are logic zero.

Interrupt Enable Register (IER)

The Interrupt Enable Register (IER) is a Write register used to independently enable the four KS82C50A interrupts which activate the interrupt (INTRPT) output. All interrupts are disabled by resetting IER[0] – IER[3] of the Interrupt Enable Register. Interrupts are enabled by setting the appropriate bits of the IER high. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output. All other system functions operate in their normal manner, including the setting of the Line Status and Modem Status Registers. The contents of the Interrupt Enable Register are indicated in Table 18 and are described below.

IER[0]: When programmed high (IER[0] = Logic 1), IER[0] enables Received Data Available interrupt.

IER[1]: When programmed high (IER[1] = Logic 1), IER[1] enables the Transmitter Holding Register Empty interrupt.

IER[2]: When programmed high (IER[2] = Logic 1), IER[2] enables the Receiver Line Status interrupt.

IER[3]: Wehn programmed high (IER[3] = Logic 1), IER[3] enables the Modem Status interrupt.

IER[4] – IER[7]: These four bits of the IER are logic zero.

Table 17 : INTERRUPT IDENTIFICATION REGISTER

Interrupt Identification				Interrupt Set and Reset Functions		
Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Flag	Interrupt Source	Interrupt Reset Control
X	X	1		None	None	
1	1	0	First	Receiver Line Status	OE, PE, FE or BI	LSR Read
1	0	0	Second	Received Data Available	Receiver Data Available	RBR Read
0	1	0	Third	THRE	THRE	IIR Read if THRE is interrupt source or THR Write
0	0	0	Fourth	Modem Status	$\overline{CTS}$, $\overline{DSR}$, $\overline{RI}$, $\overline{DCD}$	MSR Read

Note: X - Don't Care

Table 18 : REGISTER SUMMARY

Register Mnemonic	Register Bit Number							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RBR (Read Only)	Data Bit 7 (MSB)	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0 (LSB)[1]
THR (Write Only)	Data Bit 7	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0
DLL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DLM	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
IER	0	0	0	0	EDSSI (Enable Modem Status Interrupt)	ELSI (Enable Receiver Line Status Interrupt)	ETBEI (Enable Transmitter Holding Register Empty Interrupt)	ERBFI (Enable Received Data Available Interrupt)
IIR (Read Only)	0	0	0	0	0	Interrupt ID Bit 1	Interrupt ID Bit 0	'0' - if Interrupt Pending
LCR	DLAB (Divisor Latch Access Bit)	Set Break	Stick Parity	EPS (Even Parity Select)	PEN (Parity Enable)	STB (Number of Stop Bits)	WLSB1 (Word Length Select) Bit 1	WLSB0 (Word Length Select) Bit 0
MCR	0	0	0	LOOP	OUT2	OUT1	RTS (Request to Send)	DTR (Data Terminal Ready)
LSR	0	TEMT (Transmitter Empty)	THRE (Transmitter Holding Register Empty)	BI (Break Interrupt)	FE (Framing Error)	PE (Parity Error)	OE (Overrun Error)	DR (Data Ready)
MSR	DCD (Data Carrier Detect)	RI (Ring Indicator)	DSR (Data Set Ready)	CTS (Clear to Send)	DDCD (Delta Data Carrier Detect)	TERI (Trailing Edge Ring Indicator)	DDSR (Delta Data Set Ready)	DCTS (Delta Clear to Send)
SCR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Note: 1. LSB, Data Bit 0 is the first bit transmitted or received

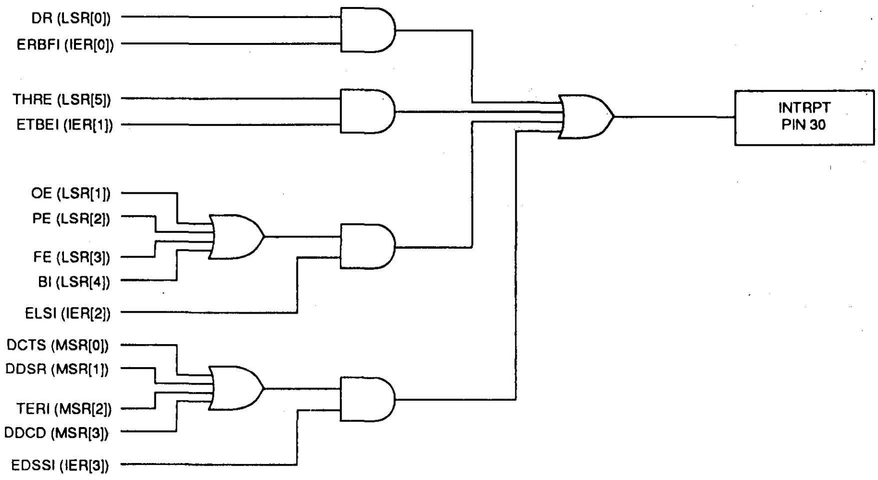


Figure 6 : 82C50A INTERRUPT CONTROL STRUCTURE

Transmitter

The serial transmitter section consists of a Transmitter Holding Register (THR). Transmitter Shift Register (TSR) and associated control logic. The Transmitter Holding Register Empty (THRE) and Transmitter Shift Register Empty (TEMT) are two bits in the Line Status Register which indicate the status of THR and TSR. To transmit a 5 - 8 bit word, the word is written through D0 - D7 to the THR. The microprocessor should perform a write operation only if THRE is high. The THRE is set high when the word is automatically transferred from the THR to the TSR during the transmission of the start bit.

When the transmitter is idle, both THRE and TEMT are high. The first word written causes THRE to be reset to zero. After completion of the transfer, THRE returns high. TEMT remains low for at least the duration of the transmission of the data word. If a second character is transmitted to the THR, the THRE is reset low. Since the data word cannot be transferred from the THR to the TSR until the TSR is empty, THRE remains low until the TSR has completed transmission of the word. When the last word has been transmitted out of the TSR, TEMT is set high. THRE is set high one THR to TSR transfer time later.

Receiver

Serial asynchronous data is input into the SIN pin. The idle state of the line providing the input into SIN is high. A start bit detect circuit continually searches for a H → L transition from the idle state. When a transition is detected, a counter is reset, and counts the 16x clock to $7^1/_2$, which is the center of the start bit. The start bit is valid if the SIN is still low at the mid bit sample of the start bit. The start bit is verified to prevent the receiver from assembling an incorrect data character due to a low going noise spike on the SIN input.

The Line Control Register determines the number of data bits in a character (LCR[0], LCR[1]), number of stop bits LCR[2], if parity is used LCR[3], and the polarity of parity LCR[4]. Status information for the receiver is provided in the Line Status Register. When a character is transferred from the Receiver Shift Register to the Receiver Buffer Register, the Data Received indication in LSR[0] is set high. The CPU reads the Receiver Buffer Register through D0 - D7. Thes read resets LSR[0]. If D0 - D7 are not read prior to a new character transfer from the RSR to RBR, the overrun error status indication is set in LSR[1]. The parity check tests for even or odd parity on the parity bit, which precedes the first stop bit. If there is a parity error, the parity error is set in LSR[2]. There is circuitry which tests whether the stop bit is high. If it is not, a framing error indication is generated in LSR[3].

The center of the start bit is defined as clock count $7^1/_2$. If data into the SIN is a symmetrical square wave, the data cell centers will occur within ±3.125% of the actual center, giving an error margin of 46.875%. The start bit can begin as much as one 16x clock cycle prior to being detected.

Baud Rate Generator (BRG)

The BRG generates the clocking for the UART function, at standard ANSI/CCITT bit rates. The oscillator driving the BRG may be provided with an external crystal to the XTAL1 and XTAL2 pins, or an external clock into XTAL1. In either case, a buffered clock output, BAUDOUT is provided for other system clocking. If two KS82C50As are used on the same board, one can use a crystal, with the buffered clock output routed directly to XTAL1 of the other KS82C50A.

The data rate is determined by the Divisor Latch registers DLL and DLM and the external frequency or crystal input, with the BAUDOUT providing an output 16x the data rate. The bit rate is selected by programming the two divisor latches, Divisor Latch Most Significant Byte and Divisor Latch Least Significant Byte. Setting DLL=1 and DLM=0 selects the divisor to divide by 1 (divide by 1 gives maximum baud rate for a given input frequency at XTAL1). The on-chip oscillator is optimized for a 10 MHz crystal.

The BRG can use any of three different popular crystals to provide standard baud rates. The frequency of these three common crystals on the market are 1.8432 MHz, 2.4576 MHz and 3.072 MHz. With these standard crystals, standard bit rates from 50 to 38.5 kbps are available. The following tables illustrate the divisors needed to obtain standard rates using these three crystal frequencies.

Table 19 : BAUD RATES WITH 1.8432 MHZ CRYSTAL

Desired Baud Rate	Divisor Used to Generate 16 x Clock	Percentage Error Difference Between Desired and Actual
50	2304	-
75	1536	-
110	1047	0.026
134.5	857	0.058
150	768	-
300	384	-
600	192	-
1200	96	-
1800	64	-
2000	58	0.69
2400	48	-
3600	32	-
4800	24	-
7200	16	-
9600	12	-
19200	6	-
38400	3	-
56000	2	2.86

3

Table 20 : BAUD RATES WITH 2.4576 MHZ CRYSTAL

Desired Baud Rate	Divisor Used to Generate 16 x Clock	Percentage Error Difference Between Desired and Actual
50	3072	-
75	2048	-
110	1396	0.026
134.5	1142	0.0007
150	1024	-
300	512	-
600	256	-
1200	128	-
1800	85	0.392
2000	77	0.260
2400	64	-
3600	43	0.775
4800	32	-
7200	21	1.587
9600	16	-
19200	8	-
38400	4	-

Table 21 : BAUD RATES WITH 3.072 MHZ CRYSTAL

Desired Baud Rate	Divisor Used to Generate 16 x Clock	Percentage Error Difference Between Desired and Actual
50	3840	-
75	2560	-
110	1745	0.026
134.5	1428	0.034
150	1280	-
300	640	-
600	320	-
1200	160	-
1800	107	0.312
2000	96	-
2400	80	-
3600	53	0.628
4800	40	-
7200	27	1.23
9600	20	-
19200	10	-
38400	5	-

Reset

After powerup, the KS82C50A Master Reset schmitt trigger input (MR) should be held high for TMRW ns to reset the KS82C50A circuits to an idle mode unitl initialization. A high on MR causes the following:

- Initializes the transmitter and receiver internal clock counters.
- Clears the Line Status Register (LSR), except for Transmitter Shift Register Empty (TEMT) and Transmit Holding Register Empty (THRE), which are set. The Modem Control Register (MCR) and Line Control Register (LCR) are also cleared. All of the discrete lines, memory elements and miscellaneous logic associated with these register bits are also cleared or turned off. The Divisor Latches, Receiver Buffer Register, Transmitter Buffer Register are not effected.

Following removal of the reset condition (MR low), the KS82C50A remains in the idle mode until programmed.

A hardware reset of the KS82C50A sets the THRE and TEMT status bit in the LSR. When interrupts are subsequently enabled, an interrupt occurs due to THRE.

A summary of the effect of a Master Reset on the KS82C50A is given in Table 22.

Table 22 : RESET OPERATIONS

Register/Signal	Reset Control	Reset
Interrupt Enable Register	Master Reset	All Bits Low (0-3 forced, 4-7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is High, Bits 1 and 2 Low Bits 3-7 Permanently Low
Line Control Register	Master Reset	All Bits Low
MODEM Control Register	Master Reset	All Bits Low
Line Status Register	Master Reset	Bits 5 and 6 High, all other Bits Low
MODEM Status Register	Master Reset	Bits 0-3 Low, Bits 4-7 Input Signal
SOUT	Master Reset	High
Interrupt (RCVR Errors)	Read LSR/MR	Low
Interrupt (RCVR Data Ready)	Read RBR/MR	Low
Interrupt (THRE)	Read IIR, Write THR/MR	Low
Interrupt (Modem Status Changes)	Read MSR/MR	Low
$\overline{\text{OUT2}}$	Master Reset	High
$\overline{\text{RTS}}$	Master Reset	High
$\overline{\text{DTR}}$	Master Reset	High
$\overline{\text{OUT1}}$	Master Reset	High

PROGRAMMING

The KS82C50A is programmed by the control registers LCR, IER, DLL, DLM and MCR. These control words define the character length, number of stop bits, parity, baud rate and modem interface.

While the Control registers can be written in any order, the IER should be written to last because it controls the interrupt enables. Once the KS82C50A is programmed and operational, these registers can be updated any time the KS82C50A is not transmitting or receiving data.

The control signals required to access KS82C50A internal registers are shown below.

Software Reset

A software reset of the KS82C50A is a useful method for returning to a completely known state without a system reset. Such a reset consists of writing to the LCR, Divisor Latches and MCR registers. The LSR and RBR registers should be read prior to enabling interrupts in order to clear out any residual data or status bits which may be invalid for subsequent operation.

Crystal Operation

The KS82C50A crystal oscillator circuitry is designed to operate with a fundamental mode, parallel resonant crystal. Table 23 shows the required crystal parameters and crystal circuit configuration, respectively.

When using an external clock source, the XTAL1 input is driven and the XTAL2 output is left open. Power consumption when using an external clock is typically 50% of that required when using a crystal. This is due to the sinusoidal nature of the drive circuitry when using a crystal.

The maximum frequency of the KS82C50A is 10 MHz with an external clock or a crystal attached to XTAL1 and XTAL2. Using the external clock or crystal, and a divide by one divisor, the maximum BAUDOUT is 10 MHz and the maximum data rate is 625 kbps.

Table 23 : TYPICAL CRYSTAL OSCILLATOR CIRCUIT

Parameter	
Frequency	1.0 to 10 MHz
Type of Operation	Parallel resonant, Fundamental mode
Load Capacitance (C_L)	20 or 32 pF (typical)
R_{SERIES} (Max)	100 (f = 10 MHz, C_L = 32 pF) 200 (f = 10 MHz, C_L = 20 pF)

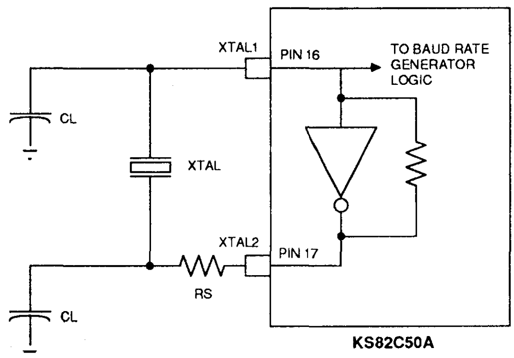


Figure 7 : CRYSTAL OSCILLATOR CIRCUIT

PACKAGE DIMENSIONS

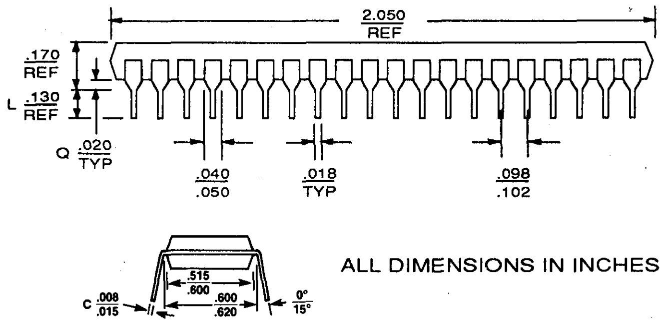


Figure 8 : PLASTIC PACKAGING

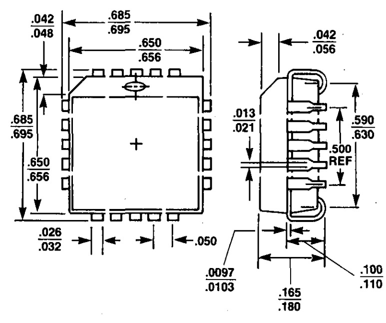


Figure 9 : PLCC PACKAGING

ORDERING INFORMATION and PRODUCT CODE

KS 82CXXX- X X X

Samsung Semiconductor, Inc. — KS

Part Number — 82CXXX

Speed
−10 10 MHz

Temperature
C - Commercial (0 °C to + 70 °C)
I - Industrial (-40 °C to + 85 °C)

Packaging
P - Plastic DIP
L - Plastic Leaded Chip Carrier (PLCC)

Samsung Semiconductor products are designated by a Product Code. When ordering, refer to products by their full code. For unusual, and/or specific packaging or processing requirements not covered by the standard product line, please contact the *Samsung Semiconductor Microprocessor Peripherals Product Group.*

FEATURES

- **Pin and functional compatibility with the industry standard 8252**
- **TTL Input/output compatibility**
- **Low power CMOS implementation**
- **High speed - DC to 16 MHz operation**
- **Single chip UART/BRG**
- **Crystal or external clock input**
- **On chip baud rate generator featuring 72 selectable baud rates**
- **Interrupt mode with mask capability**
- **Microprocessor bus oriented interface**
- **Line break generation and detection**
- **Loopback and echo modes**
- **Fully static operation**

DESCRIPTION

The KS82C52 is a high performance, single chip programmable Universal Asynchronous Receiver/Transmitter (UART) and Baud Rate Generator (BRG). The Baud Rate Generator can be programmed for one of 72 different baud rates using a single industry standard crystal or external frequency source. A programmable buffered clock output is available and can be programmed to provide either a buffered oscillator or 16X baud rate clock for general purpose system usage.

The KS82C52 features full TTL/CMOS compatibility, allowing it to be designed into mixed TTL/NMOS/CMOS system environments. Its high speed and high performance make it ideally suited for aerospace and defense applications, while a very low power consumption suits it to portable systems and systems with low power standby modes.

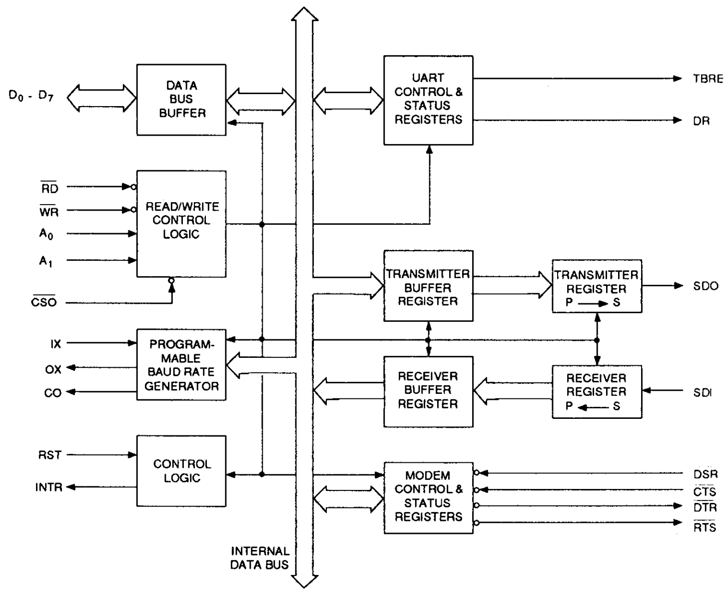


Figure 1 : KS82C52 BLOCK DIAGRAM

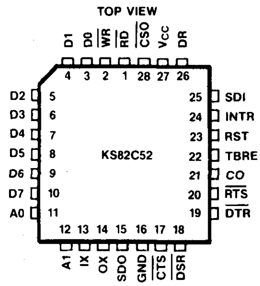


Figure 2 a: PLCC CONFIGURATION

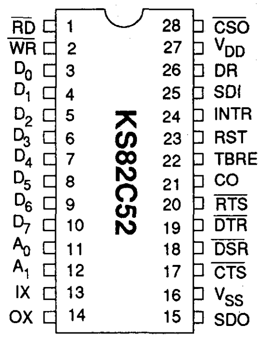


Figure 2 b: 28-PIN DIP CONFIGURATION

Table 1 : PIN DESCRIPTIONS

Symbol	Pin(s) 28-Pin DIP	Type	Name and Function
A_0, A_1	11, 12	I	**Address Inputs:** The address lines select the various internal registers during CPU bus operations.
CO	21	O	**Clock Out:** This output is user programmable to provide either a buffered IX output or a buffered Baud Rate Generator (16x) clock output. The buffered IX (Crystal or external clock source) output is provided when the Baud Rate Select Register (BRSR) bit 7 is set to a zero. Writing a logic one to BRSR bit 7 causes the CO output to provide a buffered version of the internal Baud Rate Generator clock which operates at sixteen times the programmed baud rate.
$\overline{CSO}$	28	I	**Chip Select:** The chip select input acts as an enable signals for the $\overline{RD}$ and $\overline{WR}$ input signals.
$\overline{CTS}$	17	I	**Clear to Send:** The logical state of the $\overline{CTS}$ line is reflected in the $\overline{CTS}$ bit of the Modem Status Register. Any change of state in $\overline{CTS}$ causes INTR to be set true when INTEN and MIEN are true. A false level on $\overline{CTS}$ will inhibit transmission of data on the SDO output and will hold SDO in the Mark (high) state. If $\overline{CTS}$ goes false during transmission, the current character being transmitted will be completed. $\overline{CTS}$ does not affect Loop Mode operation.
D_0 - D_7	3 - 10	I/O	**Data Bits 0 - 7:** The Data Bus provides eight, 3-state input/output lines for the transfer of data, control and status information between the KS82C52 and the CPU. For character formats of less than 8 bits, the corresponding D_7, D_6 and D_5 are considered *don't cares* for data *write* operations and are 0 for data *read* operations. These lines are normally in a high impedance state except during read operations. D_0 is the Least Significant Bit (LSB) and is the first serial data bit to be received or transmitted.
DR	26	O	**Data Ready:** A true level indicates that a character has been received, transferred to the RBR and is ready for transfer to the CPU. DR is reset on a data READ of the Receiver Buffer Register (RBR) or when RST is true.
$\overline{DSR}$	18	I	**Data Set Ready:** The logical state of the $\overline{DSR}$ line is reflected in the Modem Status Register. Any change of state of $\overline{DSR}$ will cause INTR to be set if INTEN and MIEN are true. The state of this signal does not affect any other circuitry within the KS82C52.
$\overline{DTR}$	19	O	**Data Terminal Ready:** The $\overline{DTR}$ signal can be set *low* by writing a logic 1 to the appropriate bit in the Modem Control Register (MCR). This signal is cleared *high* by writing a logic 0 to the $\overline{DTR}$ bit in the MCR or whenever a RST (high) is applied to the KS82C52.
INTR	24	O	**Interrupt Request:** The INTR output is enabled by the INTEN bit in the Modem Control Register (MCR). The MIEN bit selectively enables modem status changes to provide an input to the INTR logic. Figure 15 shows the overall relationship of these interrupt control signals.
IX, OX	13, 14	I/O	**Crystal/Clock:** Crystal connections for the internal Baud Rate Generator. IX can also be used as an external clock input in which case OX should be left open.
$\overline{RD}$	1	I	**Read:** The $\overline{RD}$ input causes the KS82C52 to output data to the data bus (D_0 - D_7). The data output depends upon the state of the address inputs (A_0, A_1). $\overline{CSO}$ enables the RD input.
RST	23	I	**Reset:** The RST input forces the KS82C52 into an *Idle* mode in which a serial data activities are suspended. The Modem Control Register (MCR) along with its associated outputs are cleared. The UART Status Register (USR) is cleared except for the TBRE and TC bits, which are set. The KS82C52 remains in an *Idle* state until programmed to resume serial data activities. The RST input is a Schmitt trigger input.
$\overline{RTS}$	20	O	**Request to Send:** The $\overline{RTS}$ signal can be set *low* by writing a logic 1 to the appropriate bit in the MCR. This signal is cleared *high* by writing a logic 0 to the $\overline{RTS}$ bit in the MCR or whenever a reset RST (high) is applied to the KS82C52.

Table 1 : PIN DESCRIPTIONS con't

Symbol	Pin(s) 28-Pin DIP	Type	Name and Function
SDI	25	I	**Serial Data Input:** Serial data input to the KS82C52 receiver circuits. A Mark (1) is high, and a Space (0) is *low*. Data inputs on SDI are disabled when operating in the loop mode or when RST is true.
SDO	15	O	**Serial Data Output:** Serial data output from the KS82C52 transmitter circuitry. A Mark (1) is a logic one (*high*) and Space (0) is a logic zero (*low*). SDO is held in the Mark condition when the transmitter is disabled, when $\overline{CTS}$ is false, RST is true, when the Transmitter Register is empty, or when in the Loop Mode.
TBRE	22	O	**Transmitter Buffer Register Empty:** The TBRE output is set *high* whenever the Transmitter Buffer Register (TBR) has transferred its data to the Transmitter Register. Application of a reset (RST) to the KS82C52 will also set the TBRE output. TBRE is cleared *low* whenever data is written to the TBR.
V_{CC}	27		**Power:** 5V ± 10% DC Supply

FUNCTIONAL DESCRIPTION

The KS82C52 UART contains a programmable baud rate generator that provides clocking for the transmitter and receiver circuits. The clock output, CO, is a buffered version of either the clock input (IX) to the device or a clock rate that is 16 x the actual baud rate generated.

The transmitter is used for sending serial data out through the SDO pin. The Transmitter Buffer Register accepts 5- to 8-bit wide parallel data from the data bus and transfers it to the Transmitter Register which then shifts the data out serially through the SDO pin. This form of double buffering technique allows continuous data flow transmission.

The receiver accepts serial data via the SDI pin and converts it to parallel form for the system CPU to read. Data is received serially into the Receiver Shift Register from the SDI pin, then sent to the Receiver Buffer Register for access by the CPU. The receiver also detects parity errors, overrun errors, frame errors and break characters.

The Modem Control and Status block provides the means for communicating with the modem or data set. The Modem Control Register is used to select one of four modes of communication: normal mode, loop mode, echo mode and transmit break. The Modem Control Register defines which interrupts will be enabled and will also set the modem control output lines, $\overline{RTS}$ and $\overline{DTR}$. The Modem Status Register keeps track of any changes in the modem control inputs lines, $\overline{CTS}$ and $\overline{DSR}$, as well as allowing the CPU to read their inputs.

The format of the data character being transmitted (eg: number of data bits, parity control and the number of stop bits) is controlled by the UART Control Register. Changes in the status of the device at any given time is reflected in the UART Status Register.

Operating Modes

Normal Mode: Configures the KS82C52 for normal full or half-duplex communications. Data will not be looped back in any form between the serial data input pin and the serial data output pin (see Figure 3a).

Transmit Break: This mode of operation causes the transmitter to transmit break characters only. A break character is composed of all logical zeros for the start, data, parity and stop bits.

Echo Mode: When selected, echo mode causes the KS82C52 to re-transmit data received on the SDI pin out to the SDO pin. In this mode of operation, any data written to the Transmitter Buffer Register will not be sent out on the SDO pin (Figure 3b).

Loop Test Mode: This mode internally re-directs data that would normally be transmitted back to the receiver circuitry. The transmitted data will not appear at the SDO pin. Also, data that is received on the SDI pin will be ignored by the device. This mode of operation is useful for performing self test(s) on the device (Figure 3c).

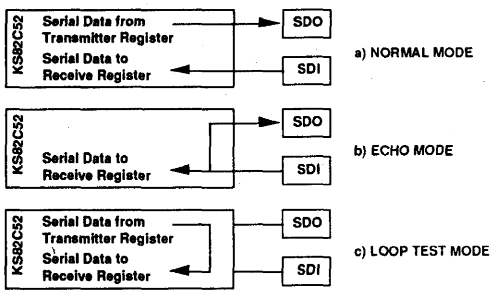


Figure 3 : OPERATING MODES

Table 2 : RECOMMENDED OPERATING CONDITIONS

Operating Voltage Range		+4 V to +7 V
Operating Temperature Range	Commercial	0 °C to +70 °C

Table 3 : ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage (V_{cc})	+8.0 V
Input (V_{IN}) or I/O Voltage Applied	V_{SS} - 0.5 V to V_{DD} + 0.5 V
Output (V_{OUT}) Voltage Applied	V_{SS} - 0.5 V to V_{DD} + 0.5 V
Maximum Power Dissipation	1 Watt
Storage Temperature	-65 °C to +150 °C

Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 4 : DC CHARACTERISTICS (T_A = 0 to 70 °C, V_{cc}= 5V ± 10%, V_{ss} = 0V)

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
I_{DD}	Operating Power Supply Current	External Clock F = 2.45576 MHz V_{DD} = 5.5 V, V_{IN} = V_{DD} or V_{SS} Outputs Open		3	mA
I_{IL}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS} on input pins	- 1.0	+1.0	µA
I_{OL}	I/O Leakage Current	V_{OUT} = V_{DD} or V_{SS} on 3-state pins	-10.0	+10.0	µA
V_{IH}	Input HIGH Voltage		2.0		V
V_{IH} (CLK)	Input HIGH Voltage Clock	External Clock	V_{DD} - 0.5		V
V_{IL}	Input LOW Voltage			0.8	V
V_{IL} (CLK)	Input LOW Voltage Clock	External Clock		V_{SS} + 0.5	V
V_{OH}	Output HIGH Voltage	I_{OH} = -2.5 mA	3.0		V
		I_{OH} = -100 µA	V_{DD} - 0.4		
V_{OL}	Output LOW Voltage	I_{OL} = +2.5 mA		0.4	V
V_{TH}	Schmitt Trigger Input HIGH Voltage	Reset Input	V_{DD} - 0.5		V
V_{TL}	Schmitt Trigger Input LOW Voltage	Reset Input		V_{SS} + 0.5	V

I_{DD} is typically ≤ 1 ma/MHz

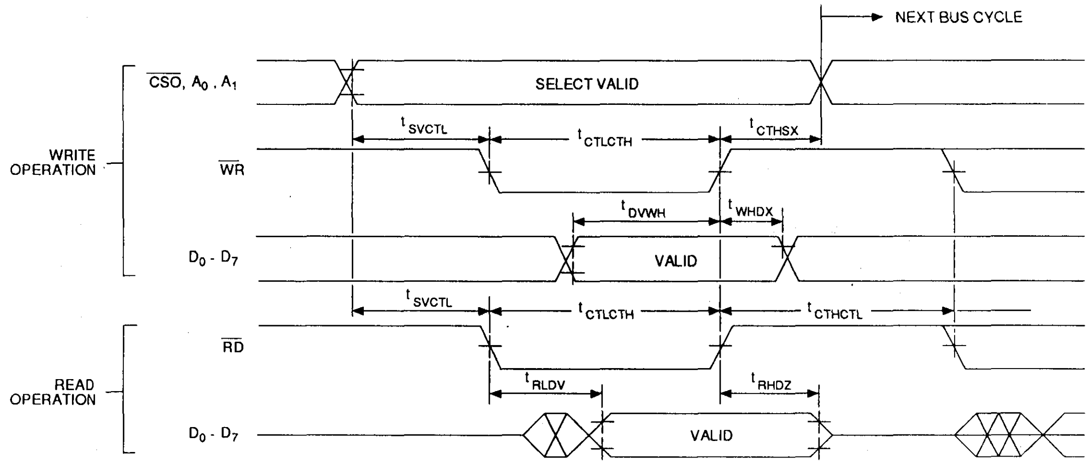
Table 5 : AC CHARACTERISTICS (T_A = 0 to 70 °C, V_{DD} = 5V ± 10%, V_{SS} = 0V)

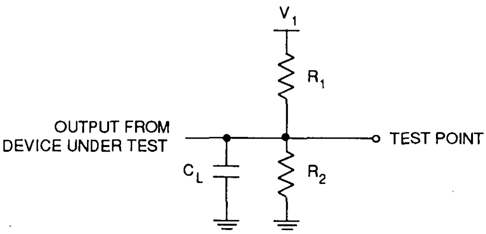
Symbol	Parameter	Test Conditions	Limits (16 MHz)		Units
			Min	Max	
FC	Clock Frequency	$t_{CHCL} + t_{CLCH}$ must be ≥ 62.5 ns	0	16	MHz
t_{CHCL}	Clock High Time		25		ns
t_{CLCH}	Clock Low Time		25		ns
t_{CTHCTL}	Control Disable to Control Enable		100		ns
t_{CTHSX}	Select Hold From Control Trailing Edge		50		ns
t_{CTLCTH}	Control Pulse Width	Control Consists of $\overline{RD}$ or WR	150		ns
t_{DVWH}	Data Setup Time		50		ns
t_{FCO}	Clock Output Fall Time	C_L = 50 pf		15	ns
t_{RCO}	Clock Output Rise Time	C_L = 50 pf		15	ns
t_{RHOZ}	Read Disable	2	0	60	ns
t_{RLDV}	Read Low to Data Valid	1		120	ns
T_R/T_F	IX Input Rise/Fall Time (External Clock)	tx ≤ $^1/_6$FC or 50 ns, whichever is smaller		tx	ns
t_{SVCTL}	Select Setup to Control Leading Edge		30		ns
t_{WHDX}	Data Hold Time		20		ns

Table 6 : CAPACITANCE (T_A = 0 to 70 °C, V_{DD} = 5V ± 10%, V_{SS} = 0V)

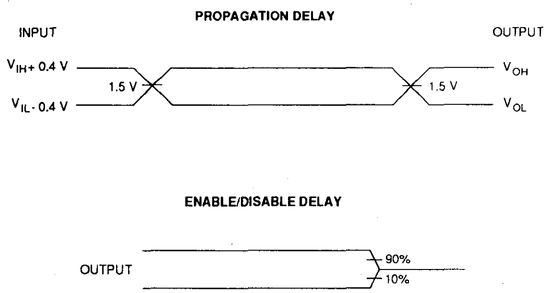
Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
C_{IN}	Input Capacitance	Freq = 1 MHz		10	pF
$C_{I/O}$	I/O Capacitance	Unmeasured pins are		20	pF
C_{OUT}	Output Capacitance	returned to V_{SS} (GND)		15	pF

Figure 4 : BUS OPERATION TIMING DIAGRAM





	TEST CONDITION	V_1	R_1	R_2	C_L
1	Propagation Delay	1.7 V	520	∞	100 pF
2	Disable Delay	V_{DD}	5 K	5 K	50 pF



A.C. Testing: All input signals must switch between V_{IL} 0.4 V and V_{IH} + 0.4 V TR and TF must be ≤ 15 ns.

Figure 5 : AC TEST CIRCUITS

Figure 6 : AC TESTING I/O WAVEFORM

PROGRAMMING INSTRUCTIONS

Reset

During and after power-up, the KS82C52 Reset input (RST) should be held high for at least two IX clock cycles in order to initialize and drive the KS82C52 circuits to an idle mode until proper programming can be done. A high on RST causes the following events to occur:

- Resets the internal Baud Rate Generator (BRG) circuits, clock counters and bit counters. The Baud Rate Select Register (BRSR) is not affected.
- Clears the UART Status Register (USR) except for Transmission Complete (TC) and Transmit Buffer Register Empty (TBRE) which are set. The Modem Control Register (MCR) is also cleared. All of the discrete lines, memory elements and miscellaneous logic associated with these register bits are also cleared or turned off. Note that the UART Control Register (UCR) is not affected.

Following removal of the reset condition (RST = low), the KS82C52 remains in the idle mode until programmed to its desired system configuration.

Control Words

The complete functional definition of the KS82C52 is programmed by the systems software. A set of control words (UCR, BRSR and MCR) must be sent out by the CPU to initialize the KS82C52 to support the desired communication format. These control words will program the character length, number of stop bits, even/odd/no parity, baud rate etc. Once programmed, the KS82C52 is ready to perform its communication functions.

The control registers can be written to in any order. However, the MCR should be written to last because it controls the interrupt enables, modem control outputs and the receiver enable bit. Once the KS82C52 is programmed and operational, these registers can be updated any time the KS82C52 is not immediately transmitting or receiving data.

3

Table 7 : CONTROL SIGNALS

$\overline{CSO}$	A_1	A_0	$\overline{WR}$	$\overline{RD}$	Operation
0	0	0	0	1	Data Bus ⇒ Transmitter Buffer Register (TBR)
0	0	0	1	0	Receiver Buffer Register (RBR) ⇒ Data Bus
0	0	1	0	1	Data Bus ⇒ UART Control Register (UCR)
0	0	1	1	0	UART Status Register ⇒ Data Bus
0	1	0	0	1	Data Bus ⇒ Modem Control Register (MCR)
0	1	0	1	0	Modem Control Register (MCR) ⇒ Data Bus
0	1	1	0	1	Data Bus ⇒ Bit Rate Select Register (BRSR)
0	1	1	1	0	Modem Status Register (MSR) ⇒ Data Bus

Table 7 shows the control signals required to access the KS82C52 internal registers.

UART Control Register (UCR)

The UCR is a write only register which configures the UART transmitter and receiver circuits. Data bits D_7 and D_6 are not used but should always be set to a logic zero (0) in order to ensure software compatibility with future product upgrades. During the Echo Mode, the transmitter always repeats the received word and parity, even when the UCR is programmed with different or no parity.

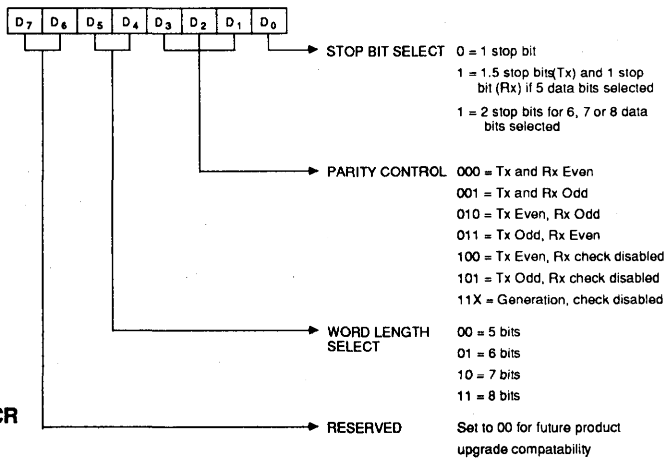


Figure 7 : UCR

Baud Rate Select Register (BRSR)

The KS82C52 is designed to operate with a single crystal or external clock driving the IX input pin. The Baud Rate Select Register is used to select the divide ratio (one of 72) for the internal Baud Rate Generator circuitry. The internal circuitry is separated into two separate counters, a Prescaler and a Divisor Select. The Prescaler can be set to any one of four division rates: ÷ 1, ÷ 3, ÷ 4 or ÷ 5.

The prescaler design has been optimized to provide standard baud rates using any one of three popular crystals. Using one of these system clock frequencies: 1.8432 MHz, 2.4576 MHz or 3.072 MHz and Prescaler divide ratios of ÷ 3, ÷ 4, or ÷ 5 respectively, the Prescaler output will provide a constant 614.4 KHz. When this frequency is further divided by the Divisor Select counter, any of the standard baud rates from 50 Baud to 38.4 KBaud can be selected (Table 8). Non-standard baud rates up to 1 Mbaud can be selected using different input frequencies (crystal or external frequency input up to 16 MHz) and/or different Prescaler and Divisor Select ratios.

Regardless of the baud rate, the baud rate generator provides a clock which is 16 times the desired baud rate. For example, in order to operate at a 1 Mbaud data rate, a 16 MHz crystal, a Prescale rate of ÷ 1, and a Divisor Select rate of *external is* used. This provides a 16 MHz clock as the output of the Baud Rate Generator to the Transmitter and Receiver circuits.

The CO select bit in the BRSR determines if the buffered version of the external frequency input (IX input) or the Baud Rate Generator output (16x baud rate clock) is output on the CO output. The Baud Rate Generator output is always a 50% nominal duty cycle except when *external* is selected and the Prescaler is set to ÷ 3 or ÷ 5.

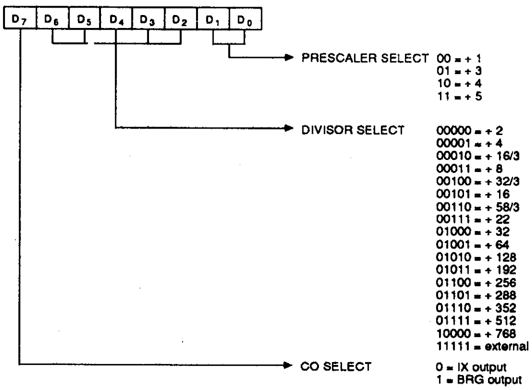


Figure 8 : BRSR

Table 8 : BAUD RATE DIVISORS

Baud Rate	Divisor
38.4 K	external
19.2 K	2
9600	4
7200	16/3
4800	8
3600	32/3
2400	16
2000	58/3
1800	22
1200	32
600	64
300	128
200	192
150	256
134.5*	288
110*	352
75	512
50	768

Note: These baud rates are based upon the following input frequency/Prescale divisor combinations:

1.8432 MHz and Prescale = ÷ 3
2.4576 MHz and Prescale = ÷ 4
3.072 MHz and Prescale = ÷ 5

*All baud rates are exact except for those in Table 9.

Table 9 : BAUD RATE % ERROR

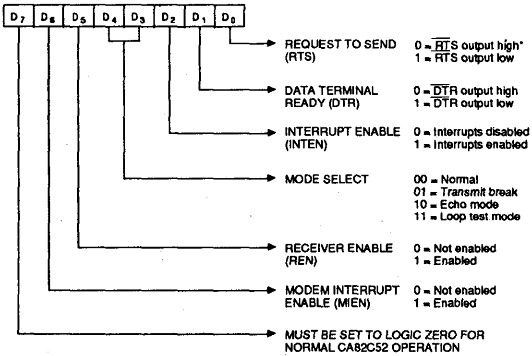
Baud Rate	Actual	Percent Error
2000	1986.2	0.69%
134.5	133.33	0.87%
110	109.71	0.26%

Modem Control Register

The MCR is a general purpose control register which can be written to and read from. The RTS and DTR outputs are directly controlled by their associated bits in this register. Note that a logic one asserts a true logic level (low) at these output pins. The Interrupt Enable (INTEN) bit is the overall control for the INTR output pin. When INTEN is false, INTR is held false (low).

The Operating Mode bits configure the KS82C52 into one of four possible modes. "Normal" configures the KS82C52 for normal full or half duplex communications. "Transmit Break" enables the transmitter to only transmit break characters (Start, Data and Stop bits are all logic zero). The Echo Mode causes any data that is received on the SDI input pin to be re-transmitted on the SDO output pin. Note that this output is a buffered version of the data seen on the SDI input and is not a resychronized output. Also note that normal UART transmission via the Transmitter Register is disabled when operating in the Echo mode (Figure 10). The Loop Test Mode internally routes transmitted data to the receiver circuitry for the purpose of self test. The transmit data is disabled from the SDO output pin. The Receiver Enable (REN) bit gates off the input to the receiver circuitry when in the false state.

Modem Interrupt Enable will permit any change in modem status line inputs (CTS, DSR) to cause an interrupt when this bit is enabled. Bit D_7 must always be written to with a logic zero to ensure correct KS82C52 operation.



* See Modem Status Register description for a description of register flag images with respect to output pins.

Figure 9 : MCR

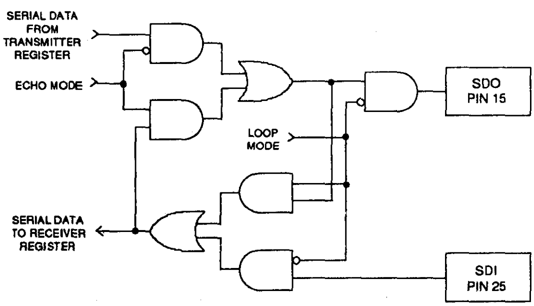


Figure 10 : LOOP AND ECHO MODE FUNCTIONALITY

UART Status Register (USR)

The USR provides a single register that the controlling system can examine to determine if errors have occurred or if other status changes in the KS82C52 require attention. For this reason, the USR is usually the first register read by the CPU to determine the cause of an interrupt or to poll the status of the KS82C52.

Three error flags OE, FE and PE report the status of any error conditions detected in the receiver circuitry. These error flags are updated with every character received during reception of the stop bits. The Overrun Error (OE) indicates that a character in the Receiver Register has been received and cannot be transferred to the Receiver Buffer Register (RBR) because the RBR was not read by the CPU. Framing Error (FE) indicates that the last character received contained improper stop bits. This could be caused by the absence of the required stop bit(s) or by a stop bit(s) that was too short to be properly detected. Parity Error (PE) indicates that the last character received contained a parity error based on the programmed parity of the receiver and the calculated parity of the received character data and parity bits.

The Received Break (RBRK) status bit indicates that the last character received was a break character. A break character would be considered to be an invalid data character in that the entire character including parity and stop bits are a logic zero.

The Modem Status bit is set whenever ~~a transition~~ is detected on any of the modem input lines (CTS or DSR). A subsequent read of the Modem Status Register will show the state of these two signals. Assertion of this bit will cause an interrupt (INTR) to be generated if the MIEN and INTEN bits in the MCR register are enabled.

The Transmission Complete (TC) bit indicates that both the TBR and Transmitter Registers are empty and the KS82C52 has completed transmission of the last character it was commanded to transmit. The assertion of this bit will cause an interrupt (INTR) if the INTEN bit in the MCR register is true.

The Transmitter Buffer Register Empty (TBRE) bit indicates that the TBR register is empty and ready to receive another character.

The Data Ready (DR) bit indicates that the RBR has been loaded with a received character (including Break) and that the CPU may access this data.

Assertion of the TBRE or DR bits do not affect the INTR logic and associated INTR output pin since the KS82C52 has been designed to provide separate requests via the DR and TBRE output pins. If a single interrupt for any status change in the KS82C52 is desired this can be accomplished by "ORing" DR, TBRE and INTR together.

3

Reading the USR clears all of the status bits in the USR register but does not affect associated output pins.

Modem Status Register (MSR)

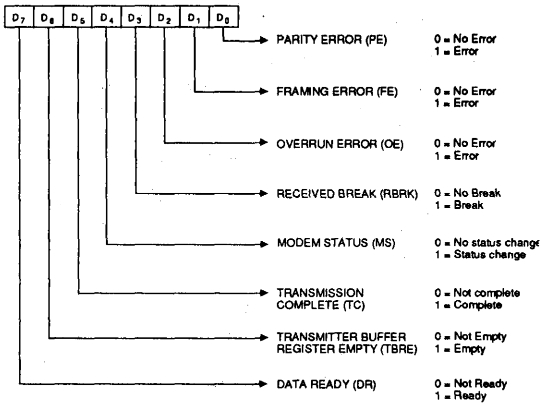


Figure 11 : USR

The MSR allows the CPU to read the modem signal inputs by accessing the data bus interface of the KS82C52. Like all of the register images of external pins in the KS82C52, true logic levels are represented by a high (1) signal level. By following this consistent definition, the system software need not be concerned with whether external signals are high or low true. In particular, the modem signal inputs are low true, thus a 0 (true assertion) at a modem input pin is represented by a 1 (true) in the MSR.

Any change of state in any modem input signals will set the Modem Status (MS) bit in the USR register. When this happens, an interrupt (INTR) will be generated if the MIEN and INTEN bits of the MCR are enabled.

The Data Set Ready (DSR) input is a status indicator from the modem to the KS82C52 which indicates that the modem is ready to provide received data to the KS82C52 receiver circuitry.

Clear to Send (CTS) is both a status and control signal from the modem that tells the KS82C52 that the modem is ready to receive transmit data from the KS82C52 transmitter output (SDO). A high (false) level on this input will inhibit the KS82C52 from beginning transmission and if asserted in the middle of a transmission will only permit the KS82C52 to finish transmission of the current character.

Receiver Buffer Register (RBR)

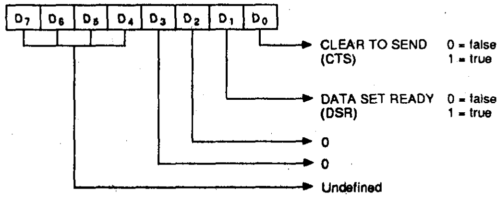
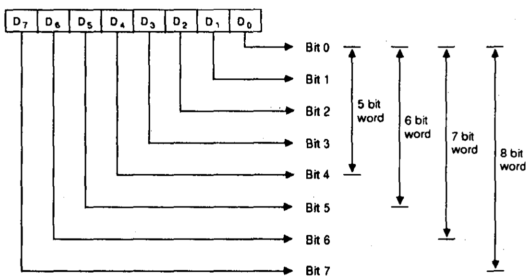


Figure 12 : MSR

The receiver circuitry in the KS82C52 is programmable for 5, 6, 7 or 8 data bits per character. For words of less than 8 bits, the data is right justified to the Least Significant Bit (LSB = D_0). Bit D_0 of a data word is always the first data bit received. The unused bits in a less than 8 bit word, at the parallel interface, are set to a logic zero (0) by the KS82C52.

Received data at the SDI input pin is shifted into the Receiver Register by an internal 1 x clock which has been synchronized to the incoming data based on the position of the start bit. When a complete character has been shifted into the Receiver Register, the assembled data bits are parallel loaded into the Receiver Buffer Register. Both the DR output pin and DR flag in the USR register are set. This double buffering of the received data permits continuous reception of data without losing any of the received data.

While the Receiver Register is shifting a new character into the KS82C52, the Receiver Buffer Register is holding a previously received character for the system CPU to read. Failure to read the data in the RBR before complete reception of the next character can result in the loss of the data in the Receiver Register. The OE flag in the USR register indicates the overrun condition.



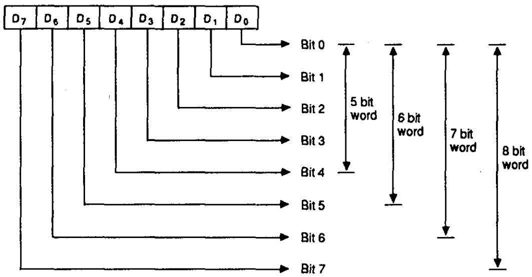
Note: The LSB, Bit 0 is the first serial data bit received.

Figure 13 : RBR

Transmitter Buffer Register (TBR)

The Transmitter Buffer Register (TBR) accepts parallel data from the data bus (D_0-D_7) and holds it until the Transmitter Register is empty and ready to accept a new character for transmission. The transmitter always has the same word length and number of stop bits as the receiver. For words of less than 8 bits the unused bits at the microprocessor data bus are ignored by the transmitter.

Bit 0, which corresponds to D_0 at the data bus, is always the first serial data bit transmitted. Provision is made for the transmitter parity to be the same or different from the receiver. The TBRE output pin and flag (USR register) reflect the status of the TBR. The TC flag (USR register) indicates when both the TBR and TR are empty.



Note: The LSB, Bit 0 is the first serial data bit transmitted.

Figure 14 : TBR

INTERRUPT STRUCTURE

The KS82C52 has provisions for software masking of interrupts generated for the INTR output pin. Two control bits in the MCR register, MIEN and INTEN, control modem status interrupts and overall KS82C52 interrupts respectively. Figure 15 illustrates the logical control function provided by these signals.

The modem status inputs ($\overline{DSR}$ and $\overline{CTS}$) will trigger the edge detection circuitry with any change of status. Reading the MSR register will clear the detect circuit but has no effect on the status bits themselves. These status bits always reflect the state of the input pins regardless of the mask control signals. Note that the state (high or low) of the status bits are inverted versions of the actual input pins.

The edge detection circuits for the USR register signals will trigger only for a positive edge (true assertion) of these status bits. Reading the USR register not only clears the edge detect circuit but also clears (sets to 0) all of the status bits. The output pins associated with these status bits are not affected by reading the USR register.

A hardware reset of the KS82C52 sets the TC status bit in the USR. When interrupts are subsequently enabled an interrupt can occur due to the fact that the positive edge detection circuitry in the interrupt logic has detected the setting of the TC bit. If this interrupt is not desired the USR should be read prior to enabling interrupts. This action resets the positive edge detection circuitry in the interrupt control logic (Figure 15).

Note: For USR and MSR, the setting of status bits is inhibited during status register READ operations. If a status condition is generated during a READ operation, the status bit is not set until the trailing edge of the RD pulse.

If the bit was already set at the time of the READ operation, and the same status condition occurs, that status bit will be cleared at the trailing edge of the RD pulse instead of being set again.

3

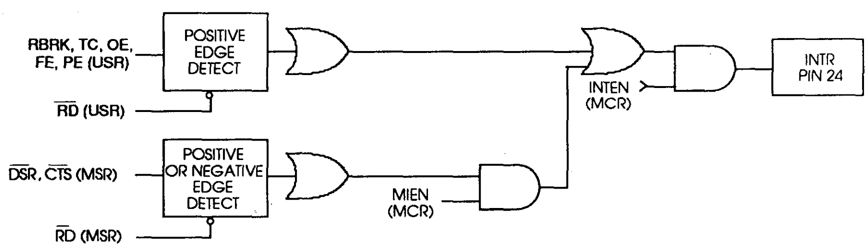


Figure 15 : INTERRUPT STRUCTURE

SOFTWARE RESET

A software reset of the KS82C52 is a useful method for returning to a completely known state without exercising a complete system reset. Such a reset would consist of writing to the UCR, BRSR and MCR registers. The USR and RBR registers should be read prior to enabling interrupts in order to clear out any residual data or status bits which may be invalid for subsequent operation.

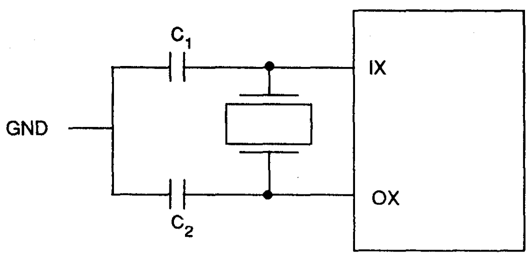
CRYSTAL OPERATION

The KS82C52 crystal oscillator circuitry is designed to operate with a fundamental mode, parallel resonant crystal. To summarize, Table 10 and Figure 16 show the required crystal parameters and crystal circuit configuration respectively.

When using an external clock source, the IX input is driven and the OX output is left open. Power consumption when using an external clock is typically 50% of that required when using a crystal. This is due to the sinusoidal nature of the drive circuitry when using a crystal.

Table 10 : CRYSTAL SPECIFICATIONS

Parameter	Typical Crystal Specs
Frequency	1.0 to 16 MHz
Type of Operation	Parallel resonant, Fundamental mode
Load Capacitance (C_L)	20 or 32 pF (typ.)
R_{series} (Max.)	100 Ω (f = 16 MHz, C_L = 32 pF) 200 Ω (f = 16 MHz, C_L = 20 pF)



* C1 = C2 = 20 pf for C_L = 20 pf
* C1 = C2 = 47 pf for C_L = 32 pf

Figure 16 : TYPICAL CRYSTAL CIRCUIT

APPLICATIONS

The following example (Figure 17) shows the interface for an KS82C52 in an 80C86 system.
Use of the Samsung Interrupt Controller (KS82C59A) is optional and necessary only if an interrupt driven system is desired.

By using the Samsung KS82C84A clock generator, the system can be built with a single crystal providing both the processor clock and the clock for the 82C52. The 82C52 has special divider circuitry which is designed to supply industry standard baud rates with a 2.4576 MHz input frequency. Using a 15 MHz crystal as shown, results in less than a 2% frequency error which is adequate for many applications. For more precise baud rate requirements, a 14.7456 MHz crystal will drive the 80C86 at 4.9 MHz and provide the 82C52 with the standard baud rate input frequency of 2.4576 MHz. If baud rates above 156 Kbaud are desired, the OSC output can be used instead of the PCLK (÷6) output for asynchronous baud rates up to 1 Mbaud.

3

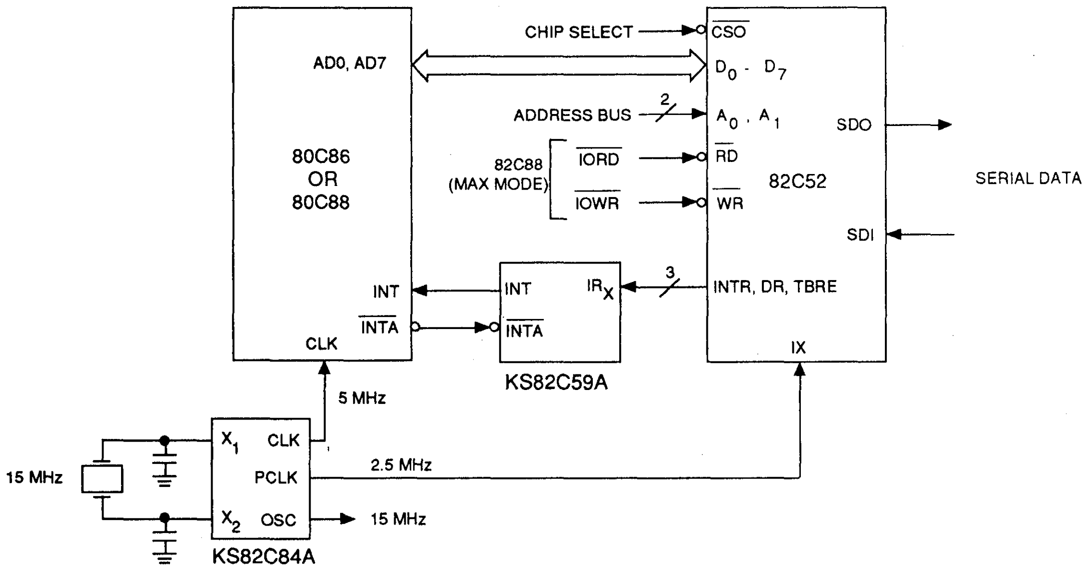


Figure 17 : 80C86/KS82C52 INTERFACE

MECHANICALS

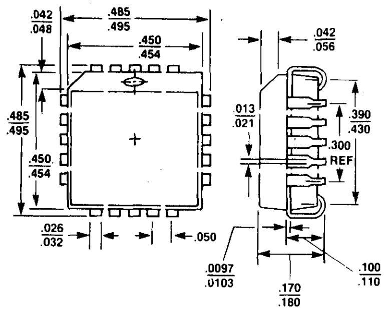


Figure 17 : PLCC PACKAGING

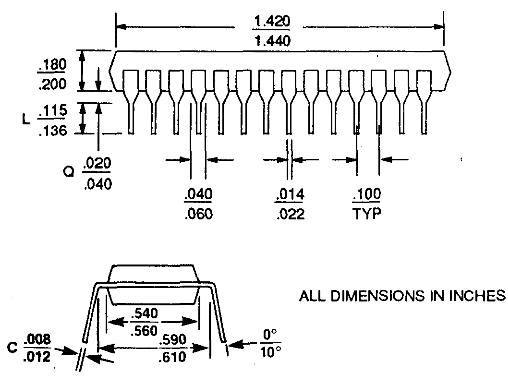


Figure 18 : PLASTIC PACKAGING

ORDERING INFORMATION

KS 82C52 X X X

Samsung Semiconductor Inc. — KS

Part Number — 82C52

Speed
- 16 16 MHz

Temperature
C - Commercial (0 °C to + 70 °C)
I - Industrial (-40 °C to + 85 °C)

Packaging
P - Plastic DIP
L- Plastic Leaded Chip Carrier (PLCC)

Samsung products are designated by a Product Code. When ordering, refer to products by their full code. For unusual, and/or specific packaging or processing requirements not covered by the standard product line, contact the *Samsung Microprocessor Peripherals Product Marketing.*

3725 North First Street
San Jose, CA 95134-1708
Telephone: (408) 434-5400
(800) 669-5400
Fax: (408) 434-5650

FEATURES/BENEFITS

- **A high performance device featuring pin and functional compatibility with the industry standard 8254**
- **High Speed — 8MHz and 10MHz versions**
- **Low power CMOS implementation**
- **TTL input/output compatibility**
- **Compatible with 8080/85, 8086/88, 80286/386 and 680X0μP families**
- **Fully static operation**
- **Three independent 16 bit counters**
- **Six programmable counter modes**
- **Status read-back command**
- **Binary or BCD counting**

DESCRIPTION

The KS82C54 is a counter/timer device that includes complete pin and functional compatibility with the industry standard 8254. Designed for fast 10MHz operation, it has three independently programmable 16 bit counters and six programmable counter modes. Counting can be performed in both binary and BCD formats.

The KS82C54 offers a very flexible, hardware solution to the generation of accurate time delays in microprocessor systems. A general purpose, multi-timing element, it can be used to implement event counters, elapsed time indicators, waveform generators plus a host of other functions.

The low power consumption of the KS82C54 makes it ideally suited to portable systems or those with low power standby modes. It is manufactured using proven CMOS process technology to produce a solid, reliable product.

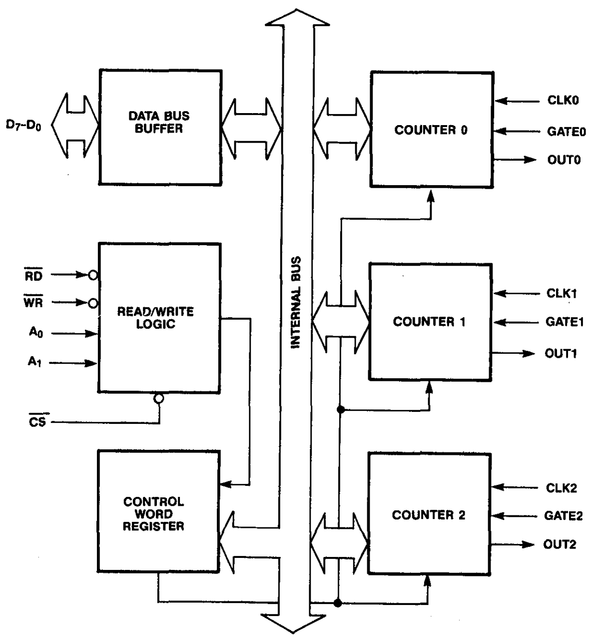


Figure 2: KS82C54 Block Diagram

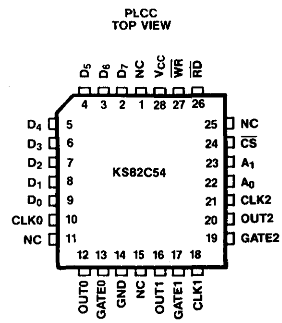


Figure 1a: Plastic Leaded Chip Carrier

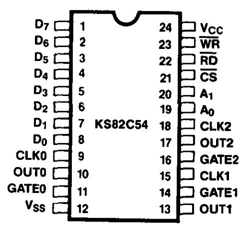


Figure 1b: 24-Pin Configuration

Table 1a: 28-Pin PLCC Pin Assignment

Pin #	I/O	Pin Name	Pin #	I/O	Pin Name
1	—	NC	15	—	NC
2	I/O	D_7	16	O	OUT1
3	I/O	D_6	17	I	GATE1
4	I/O	D_5	18	I	CLK1
5	I/O	D_4	19	I	GATE2
6	I/O	D_3	20	O	OUT2
7	I/O	D_2	21	I	CLK2
8	I/O	D_1	22	I	A_0
9	I/O	D_0	23	I	A_1
10	I	CLK0	24	I	$\overline{CS}$
11	—	NC	25	—	NC
12	O	OUT0	26	I	$\overline{RD}$
13	I	GATE0	27	I	$\overline{WR}$
14	—	GND	28	—	V_{CC}

Table 1b: 24-Pin DIP Pin Assignment

Pin #	I/O	Pin Name	Pin #	I/O	Pin Name
1	I/O	D_7	13	O	OUT1
2	I/O	D_6	14	I	GATE1
3	I/O	D_5	15	I	CLK1
4	I/O	D_4	16	I	GATE2
5	I/O	D_3	17	O	OUT2
6	I/O	D_2	18	I	CLK2
7	I/O	D_1	19	I	A_0
8	I/O	D_0	20	I	A_1
9	I	CLK0	21	I	$\overline{CS}$
10	O	OUT0	22	I	$\overline{RD}$
11	I	GATE0	23	I	$\overline{WR}$
12	—	V_{SS}	24	—	V_{CC}

3

Table 2: Pin Descriptions

Symbol	Type	Name and Function
A_0, A_1	I	**Address:** These two address pins are used to select the Control Word Register (for read or write operations), or one of the three counters. They are normally connected to the system address bus. <table><tr><th>A_1</th><th>A_0</th><th>Selects</th></tr><tr><td>0</td><td>0</td><td>Counter 0</td></tr><tr><td>0</td><td>0</td><td>Counter 1</td></tr><tr><td>0</td><td>1</td><td>Counter 2</td></tr><tr><td>1</td><td>1</td><td>Control Word Register</td></tr></table>
$\overline{CS}$	I	**Chip Select:** Active LOW control signal to enable the KS82C54 to respond to RD and WR signals. If CS is not LOW, RD and WR are ignored.
D_7 - D_0	I/O	**Data:** Bi-directional 3-state data bus lines, connected to system data bus.
CLK0	I	**Clock 0:** Clock input of Counter 0.
CLK1	I	**Clock 1:** Clock input of Counter 1.
CLK2	I	**Clock 2:** Clock input of Counter 2.
GATE0	I	**Gate 0:** Gate input of Counter 0.
GATE1	I	**Gate 1:** Gate input of Counter 1.

Table 2: Pin Descriptions (Continued)

Symbol	Type	Name and Function
GATE2	I	**Gate 2:** Gate input of Counter 2.
OUT0	O	**Output 0:** Output of Counter 0.
OUT1	O	**Output 1:** Output of Counter 1.
OUT2	O	**Output 2:** Output of Counter 2.
$\overline{RD}$	I	**Read Control:** Active LOW control signal used to enable the KS82C54 for read operations by the CPU.
$\overline{WR}$	I	**Write Control:** Active LOW control signal used to enable the KS82C54 to be written to by the CPU.
V_{CC}	—	**Power:** 5V ± 10% DC Supply.
V_{SS}	—	**Ground:** 0V.

FUNCTIONAL DESCRIPTION

The KS82C54 is a versatile programmable interval timer/counter designed for use in high speed 8, 16 and 32-bit microprocessor systems. It provides a means of generating accurate time delays in hardware that is fully software configurable. It can be treated as an array of I/O ports, with minimal software overhead.

The internal structure of the KS82C54 is illustrated in the block diagram of Figure 2. Major functional blocks include a data bus buffer, read/write logic, control word register, and three programmable counters.

Data bus Buffer Block

The 8-bit, 3-state data bus buffer provides controllable, bidirectional interface between the KS82C54 and the microprocessor system bus.

Read/Write Logic Block

The read/write logic block generates internal control signals for the different functional blocks using address and control information obtained from the system. The active LOW signals: $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$ are used to select the KS82C54 for operation, read a counter, and write to a counter (or the control word register) respectively. $\overline{CS}$ must be LOW for $\overline{RD}$ or $\overline{WR}$ to be recognized. Note that $\overline{RD}$ and $\overline{WR}$ must not be active at the same time.

The inputs A_0 and A_1 are used to select the Control Word Register, or one of the three counters that is to be written to or read from (see Table 4). A_0 and A_1 connect directly to the corresponding signals of the microprocessor address bus, while $\overline{CS}$ is derived from the address bus using either a linear select method, or an address decoder device.

Control Word Register

The Control Word Register is a write only register that is selected by the read/write logic block when A_0 and A_1 = 1. When $\overline{CS}$ and $\overline{WR}$ are LOW, data is written into the KS82C54 Control Word Register from the CPU via the data bus buffer. Control word data is interpreted as a number of different commands which are used to program the various device functions. For example, status information is available with the Read-Back Command. These are discussed further in the section on programming.

Counter Blocks

The KS82C54 contains three identical, independent counter blocks. Each counter provides the same functions, but can be programmed to operate in different modes relative to each other. A typical KS82C54 counter is illustrated in Figure 3, and contains the following functional elements: control logic, counter, output latches, count registers and status register.

The Control Logic provides the interface between the Counter Element, the program instructions contained in the Control Word Register and the external signals CLKn, GATEn and OUTn. It also keeps the Status Register information current, controls the access of OL and CR to the internal data bus, and the loading of CE from the CR registers.

The Counter Element (shown in the Figure 3 as CE, for Counting Element) is a 16-bit presettable synchronous down counter.

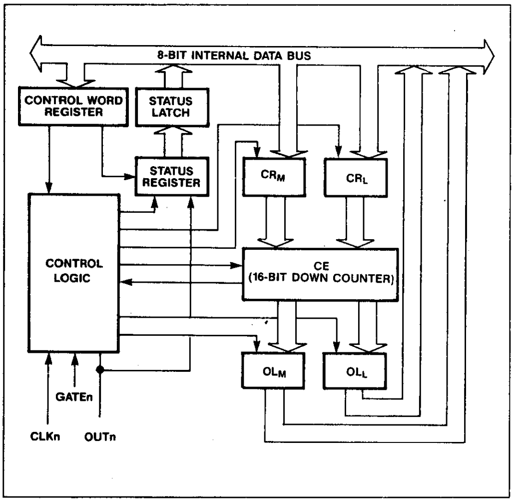
The Output Latches (shown as OL_M and OL_L) provide a mechanism whereby the CPU can read the current contents of the CE. These two 8-bit latches (M for most significant byte and L for least significant byte) together form a 16-bit latch capable of holding the complete content of the CE. Note that this arrangement is also used for communicating 16-bit values over the 8-bit internal data bus.

During normal operation, the contents of OL track with the contents of CE. When a Counter Latch Command is issued by the CPU to a particular counter, its OL latches the current value of CE so that it can be read by the CPU (the CE cannot be read directly). OL then returns to tracking with CE. Note that only one latch (OL_M followed by OL_L) at a time is enabled by the counter's control logic.

The Count Registers (shown as CR_M and CR_L) behave as input latches to the CE, and provide a mechanism whereby the initial count value can be downloaded from the CPU to the CE. Similar in operation to OL, CR is controlled by the counter control logic. When a two byte initial count is to be downloaded, it is transferred one byte at a time across the internal KS82C54 data bus to the appropriate register (CR_M if the most significant byte, CR_L otherwise). CE is loaded by transferring both bytes simultaneously from CR. Note that CR is the interface between CE and the data bus, since CE cannot be accessed directly.

Both CR_M and CR_L are cleared automatically when the counter is programmed and a new initial count is to be written. Thus, regardless of the counter's previous programming, both CR bytes will be initialized to a known zero state. This is important in the case where one byte counts are programmed (either most significant or least significant byte), so that the unused byte is always zero, and won't corrupt the initial count value loaded into CE.

Figure 3: Block Diagram of a Counter



The Status Register and Status Latch is used to hold the current contents of the Control Word Register and the status of the output and null count flag (see section on Programming). The contents of the Status Register must be latched to become available to the data bus, where they can be read by the CPU.

Note that the Control Word Register is also shown in the Counter block diagram. While not a part of the Counter Element, its contents determine the functional operation of the counter, including mode selection programmed.

OPERATIONAL DESCRIPTION

The following operations are common to all modes.

Control Word: When a Control Word is written to a Counter, all Control Logic is Reset, and OUT is initialized to a known state. No CLK pulses are needed.

Gate: The GATE input is always sampled on the rising edge of CLK. In modes 0, 2, 3, and 4 the GATE input is level sensitive, and the logic level is sampled on the rising edge of CLK. In modes 1, 2, 3, and 5 the GATE input is rising-edge sensitive. In these modes, a rising edge of GATE (trigger) sets an edge-sensitive flip-flop in the Counter. This flip-flop is sampled on the next rising edge of CLK, then is immediately reset. In this way, a trigger will be detected no matter when it occurs and a high logic level does not have to be maintained until the next CLK pulse. A summary is given in Table 5.

Note that in Modes 2 and 3, the GATE input is both edge-and level-sensitive. If a CLK source other than the system clock is used in modes 2 and 3, GATE should be pulsed immediately after the $\overline{WR}$ for a new count value.

Counter: New Counts are loaded, with the largest possible initial COUNT being 0; (equivalent to 2^{16} for binary counting and 10^4 for BCD counting, as in Table 3)

Counters decremented on the falling edge of CLK do not stop when they reach zero. In Modes 0, 1, 4, and 5 the Counters wrap around to the highest count (either FFFF hex for binary counting or 9999 for BCD counting), then continue counting. Modes 2 and 3 are periodic; the Counters reload themselves with the initial count, then continue counting from there.

Table 3: MIN and MAX Initial Counts

Mode	Minimum Count	Maximum Count*
0	1	0
1	1	0
2	2	0
3	2	0
4	1	0
5	1	0

* 0 is equivalent to 2^{16} for binary counting and 10^4 for BCD counting.

Table 4: Read/Write Operations Summary

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_1	A_0	
0	1	0	0	0	Write into Counter 0
0	1	0	0	1	Write into Counter 1
0	1	0	1	0	Write into Counter 2
0	1	0	1	1	Write Control Word
0	0	1	0	0	Read from Counter 0
0	0	1	0	1	Read from Counter 1
0	0	1	1	0	Read from Counter 2
0	0	1	1	1	No-Operation (3-State)
1	X	X	X	X	No-Operation (3-State)
0	1	1	X	X	No-Operation (3-State)

If both the Count and Status Registers of a counter are latched, the first read operation of that counter will return the latched status, regardless of which was latched first. The next one or two reads (the counter can be programmed for one or two type counts) will return the latched count. Subsequent reads will return an unlatched count. Read and write operations are summarized in Table 4.

PROGRAMMING THE KS82C54

The KS82C54 is programmed by writing a Control Word into the Control Word Register (selected by A_0, A'1, 1') and an initial count to the Counter to be written into. A_0 and A_1 are used to select the appropriate Counter. The format of the count depends on the Control Word used.

Write Operation

As mentioned previously, programming of the KS82C54 is performed in two steps:

- Each counter requires a Control Word before the initial count can be written into the selected Counter.
- The initial count must follow the convention in the Control Word for the particular Counter; i.e., LSB or MSB only or LSB and then MSB.

The instruction sequence has to be followed as shown above, however, the sequence of programming the Counter can be random, since every Counter has its associated Control Word Register. A new initial count may be written to the Counter without rewriting the Control Word for that Counter. Of course, the new count must follow the programmed count format.

Table 5: Gate Pin Operations Summary

Signal Status Modes	Low, or Going Low	Rising	High
0	—	• Disables counting	• Enables counting
1	—	• Initiates counting • Resets output after next clock	—
2	• Disables counting • Sets output immediately high	• Initiates counting	• Enables counting
3	• Disables counting • Sets output immediately high	• Initiates counting	• Enables counting
4	• Disables counting	—	• Enables counting
5	—	• Initiates counting	—

Figure 4: Control Word Format

$A_1, A_0 = 11$, $\overline{CS} = 0$, $\overline{RD} = 1$, $\overline{WR} = 0$

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC-SELECT COUNTER

0	0	SELECT COUNTER 0
0	1	SELECT COUNTER 1
1	1	SELECT COUNTER 2
1	1	READ-BACK COMMAND (SEE OPERATIONS)

M-MODE

0	0	0	MODE 0
0	0	1	MODE 1
X	1	0	MODE 2
X	1	1	MODE 3
1	0	0	MODE 4
1	0	1	MODE 5

RW-READ/WRITE

RW1	RW0	
0	0	COUNTER LATCH COMMAND (SEE READ OPERATIONS)
0	1	READ/WRITE LEAST SIGNIFICANT BYTE ONLY
1	0	READ/WRITE MOST SIGNIFICANT BYTE ONLY
1	1	READ/WRITE LEAST SIGNIFICANT BYTE FIRST THEN MOST SIGNIFICANT BYTE

BCD

0	BINARY COUNTER 16-BITS
1	BINARY CODED DECIMAL (BCD) COUNTER (4-DECADES)

Note: Don't care bits (X) should be 0 to ensure compatibility with future Samsung products.

If a Counter is programmed as a 16 bit counter, the Control Register should not be accessed between writing the first and second byte count. Otherwise, the Counter will be loaded incorrectly.

Read Operation

There are three methods of reading the Counters:

- by a simple read operation
- by a Counter Latch Command
- by a Read-Back Command

The first method is performed just by performing a read of the desired Counter Register. The value read is the current status and may be changing if the CLK input is not inhibited.

Counter Latch Command

This method of reading the Counter requires a write command to the Control Word Register of the Counter selected by SC0 and SC1 in the Control Word and RW0 and RW1 = '0'. See Figure 5. The selected counter output will be latched in the OL latch of the Counter at the time the Control Word is received and is held until it is read by the CPU or the Counter is reprogrammed. The OL latch is then loaded according to the Counter Element. This allows reading the Counter at any time without affecting counting. More than one Latch Command may be issued since all counter blocks are built identical. Latching the count by the Latch Command does not influence the programmed Mode of the Counter. Multiple successive Latch Commands do not overwrite the value latched at the first Latch Command. Only a read of the OL or reprogramming of the Counter will alter the latched Counter value. It is also important that two read commands have to be issued if the Counter is programmed as a 16 bit counter. A program may not transfer commands between the two read cycles. Otherwise, an incorrect count value will be read.

Read-Back Command

A third method of reading the count value requires issuing a Read-Back Command prior to the read operation. See Figure 6. If the $\overline{\text{COUNT}}$ bit is set, the appropriate count values of the Counter selected by CNT0, 1, 2 are latched. The status of the Counter are latched if the STATUS bit is '1'. Multiple counters may be selected.

The Counter Status format is shown in Figure 7. D0 to D5 contain the Mode of the counter as programmed by the last Control Word.

D6 (Null Count) indicate when the last Count Register (CR) has been loaded into the Counting Element (CE). See also Mode Definition.

Figure 5: Counter Latching Command Format

$A_1, A_0 = 11$; $\overline{CS} = 0$; $\overline{RD} = 1$; $\overline{WR} = 0$

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC00	0	0	X	X	X	X

SC1, SC0—SPECIFY COUNTER TO BE LATCHED

SC1	SC0	COUNTER
0	0	0
0	1	1
1	0	1
1	1	READ-BACK COMMAND

D5, D4-00 DESIGNATED COUNTER LATCH COMMAND
X — DON'T CARE

Note: Don't care bits (X) should be 0 to ensure compatibility with future Samsung products.

3

'1' After a write to the Word Control Register (Note 1)
'1' After a write to the Counter Register (CR) (Note 2)
'0' After a new count is loaded into the Count Element (CR → CE).

Note 1: Only the Counter specified by the Control Word is affected.
Note 2: If the Counter is programmed for two byte counts, the $\overline{\text{COUNT}}$ bit goes to '1' after the second byte is written.

The output OUT of the selected counter can be read by D7 (OUTPUT) of the Status byte. If both $\overline{\text{COUNT}}$ and $\overline{\text{STATUS}}$ has been selected, the first read operation of that Counter will return the latched status and the next one or two read will return the latched count. Subsequent reads return unlatched counts.

Figure 6: Read-Back Command Format

$A_1, A_0 = 22$; $\overline{CS} = 0$; $\overline{RD} = 1$; $\overline{WR} = 0$

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	$\overline{\text{COUNT}}$	$\overline{\text{STATUS}}$	CNT2	CNT1	CNT0	0

D_5 : 0 = Latch count of selected conter(s)
D_4 : 0 = Latch status of selected counter(s)
D_3 : 1 = Select Counter 2
D_2 : 1 = Select Counter 1
D_1 : 1 = Select Counter 0
D_0 : Reserved for future expansion; Must be 0

Figure 7: Status Byte

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
OUTPUT	NULL COUNT	RW1	RW0	M2	M1	M0	BCD

D_7 : 1 = OUT Pin is 1
0 = OUT Pin is 0
D_6 : 0 = OUT Pin is 0
0 = Count Available for Reading
D_5-D_0 : Counter Programmed Mode (See Figure 4)

MODE DEFINITIONS

The following terms are useful in describing the operation of the KS82C84.

- CLK pulse: A rising edge, followed by a falling edge, of a Counter's CLK input.
- Trigger: A rising edge of a Counter's GATE input.
- Counter loading: Transfer of a count from the CR to the CE (see Functional Description)

Mode 0: Interrupt on Terminal Count

Mode 0 is typically used for event counting. After the Control Word is written, OUT is set low, and remains low until the Counter reaches zero. OUT then goes high and remains high until a new count or a new Mode 0 Control Word is written into the Counter.

GATE = 1 enables counting while GATE = 0 disables counting. GATE has no effect on OUT.

After a Control Word and initial count are written to a Counter, the initial count is loaded on the next CLK pulse. Since this CLK pulse does not decrement the count, OUT does not go high until N + 1 CLK pulses after the initial count is written (where N is the initial count value).

If a new count is written to the Counter, it is loaded on the next CLK pulse and counting continues from the new count. If a two-byte count is written, the following happens:

1. Writing the first byte disables counting. OUT is set low immediately (no clock pulse required).
2. Writing the second byte allows the new count to be loaded on the next CLK pulse.

This allows the counting sequence to be synchronized by software. Again, OUT does not go high until N + 1 CLK pulses after the new count of N is written.

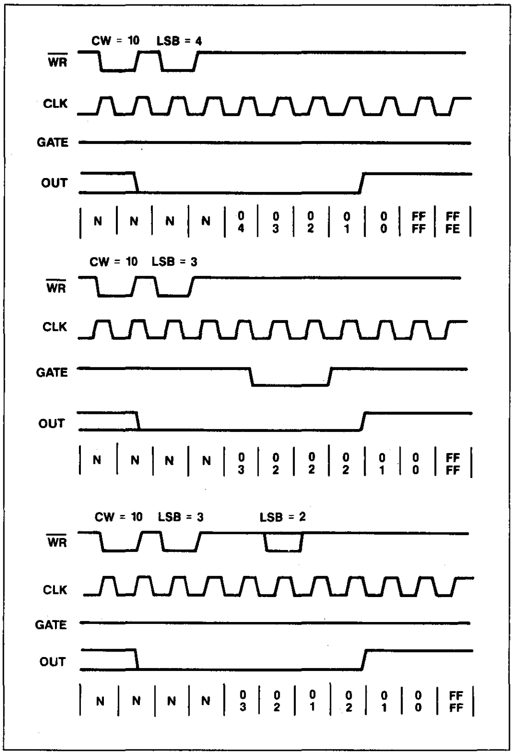
If an initial count is written while GATE = 0, it will still be loaded on the next CLK pulse. When GATE goes high, OUT will go high N CLK pulses later. A CLK pulse is not required to load the Counter as this has already been done.

Mode 1: Hardware Retriggerable One-Shot

OUT is initially high. To begin the one-shot pulse, OUT goes low on the CLK pulse following a trigger and remains low until the Counter reaches zero. OUT then goes high and remains high until the CLK pulse following the next trigger.

After a Control Word and intial count have been written, the Counter is armed. A trigger causes the Counter to be loaded and OUT to be set low on the next CLK pulse, starting the one-shot pulse. An initial count of N results in a one-shot pulse N CLK cycles long. Since the one-shot is retriggerable, OUT remains low for N CLK pulses after any trigger. The one-shot pulse can be repeated without rewriting the same count into the counter. GATE has no effect on OUT.

Figure 8: Mode 0 Timing



Notes: These conventions apply to all mode timing diagrams:

1. Counters are programmed for binary (not BCD) counting and for reading/writing least significant byte (LSB) only.
2. The counter is always selected (CS always low).
3. CW stands for Control Word; CW = 10 means a control word of 10, hex is written to the counter.
4. LSB is the Least Significant Byte of count.
5. Numbers below diagrams are count values. The lower number is the least significant byte. The upper number is the most significant byte. Since the counter is programmed to read/write only, the most significant byte cannot be read.
6. N stands for an undefined count. Vertical lines show transitions between count values.

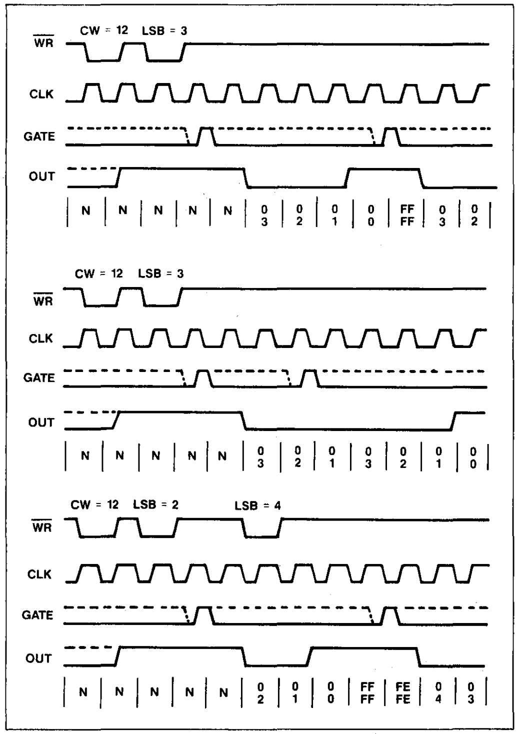
If a new count is written to the Counter during a one-shot pulse, the current one-shot is not affected unless the Counter is retriggered. In this case, the new count is loaded into the Counter and the one-shot pulse continues for the duration of the count.

Mode 2: Rate Generator

This mode functions like a divide-by-N counter and is typically used for generating Real Time Clock Interrupts. OUT is initially high. When the initial count has decremented to 1, OUT goes low for one CLK pulse, then high again. The Counter reloads the initial count and the process is repeated. Mode 2 is periodic, with the same sequence repeated indefinitely. For an initial count of N, the sequence repeats every N CLK cycles.

GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low during an output pulse, OUT is set high immediately. A trigger reloads the initial count into the Counter on the next CLK pulse; OUT goes low N CLK pulses after the trigger. Thus the GATE input can be used to synchronize the Counter.

Figure 9: Mode 1 Timing



3

After a Control Word and intial count have been written, the Counter is loaded on the next CLK pulse. OUT goes low N CLK pulses after the initial count is written, which allows the Counter to be synchronized by software.

Writing a new count while counting does not affect the current counting sequence. If a trigger is received after a new count is written but before the end of the current period, the Counter is loaded with the new count on the next CLK pulse and counting continues from the new count. Otherwise, the new count is loaded at the end of the current counting cycle. In Mode 2, a COUNT of 1 is illegal.

Mode 3: Square Wave Mode

Mode 3 is typically used for Baud rate generation, and is similar to Mode 2 except for the duty cycle of OUT. OUT is initially high. When half the initial count has expired, OUT goes low for the remainder of the count. Mode 3 is also periodic, with the sequence above repeated indefinitely. An initial count of N results in a square wave with a period of N CLK cycles.

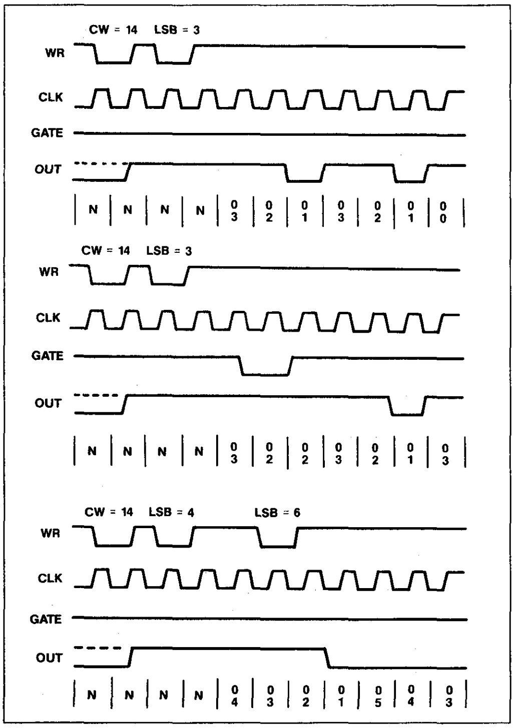
GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low while OUT is low, OUT is set high immediately (no CLK pulse is needed). A trigger reloads the Counter with the initial count on the next CLK pulse. Thus the GATE input can be used to synchronize the Counter.

The Counter is loaded on the next CLK pulse after a Control Word and initial count have been written. This allows the Counter to be synchronized by software.

Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current half-cycle of the square wave, the Counter is loaded with the new count on the next CLK pulse and counting continues from the new count. Otherwise, the new count is loaded at the end of the current half-cycle.

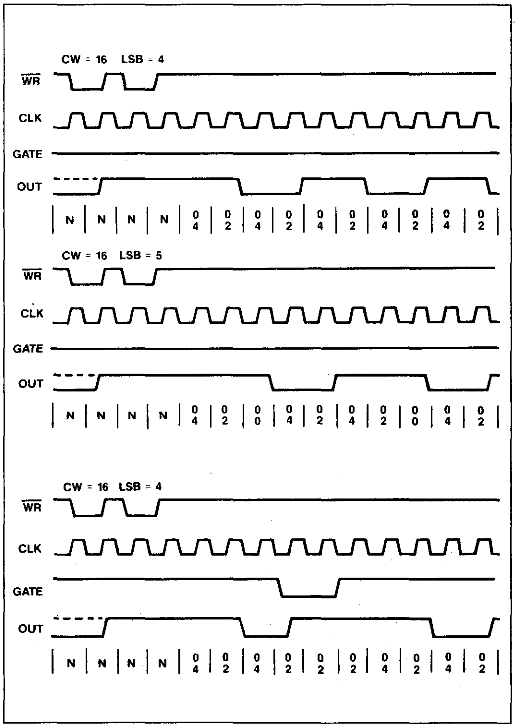
Mode 3 is implemented as follows according to whether the initial count value is even or odd:

Figure 10: Mode 2 Timing



Note: A gate transition should not occur one clock cycle prior to reaching the terminal count (TC).

Figure 11: Mode 3 Timing



Note: A gate transition should not occur one clock cycle prior to reaching the terminal count (TC).

Even counts: OUT is initially high. The initial count is loaded on one CLK pulse and then decremented by two on succeeding CLK pulses. When the count expires, OUT goes low and the counter is reloaded with the initial count. The above process is repeated indefinitely.

Odd counts: OUT is initially high. The initial count minus one (to given an even number) is loaded on one CLK pulse and then decremented by two on succeeding CLK pulses. One CLK pulse after the count expires, OUT goes low and the Counter is reloaded with the initial count minus one. Succeeding CLK pulses decrement the count by two. When the count expires, OUT goes high again and the Counter is reloaded with the initial count minus one. The above process is repeated indefinitely. So for odd counts, OUT is high for (N + 1)/2 counts and low for (N - 1)/2 counts.

Mode 4: Software Triggered Strobe

OUT is initially high. When the initial count expires, OUT goes low for one CLK pulse and then goes high again. The counting sequence is triggered by writing the initial count.

GATE = 1 enables counting; GATE = 0 disables counting. GATE has no effect on OUT.

The Counter is loaded on the next CLK pulse after a Control Word and initial count have been written. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N + 1 CLK pulses after the initial count is written.

If a new count is written during counting, it is loaded on the next CLK pulse and counting continues from the new count. If a two-byte count is written, the following events occur:

3

Figure 12: Mode 4 Timing

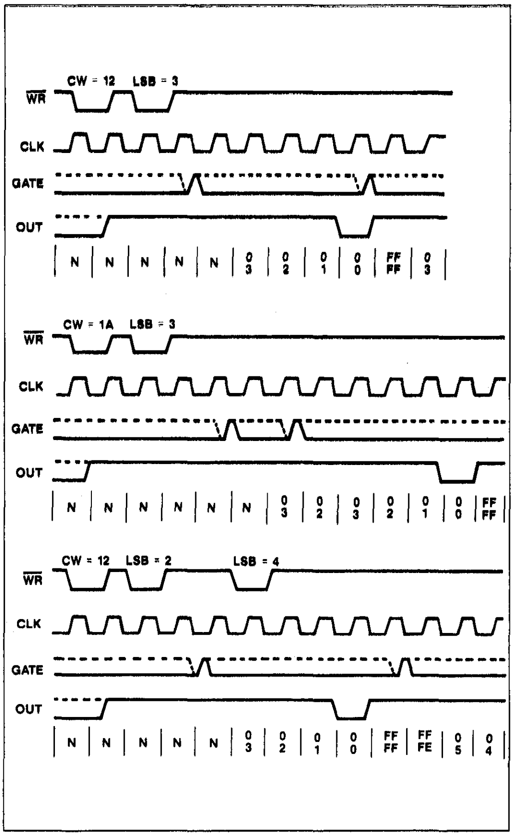
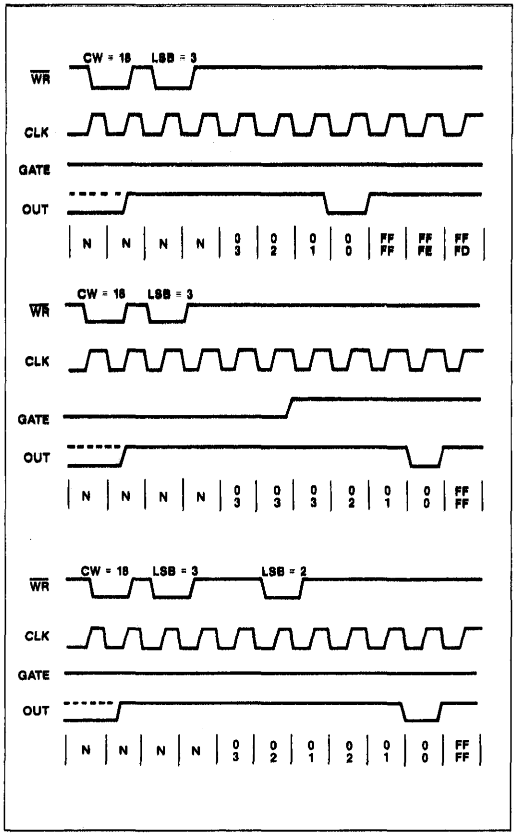


Figure 13: Mode 5 Timing



1. Writing the first byte has no effect on counting.
2. Writing the second byte allows the new count to be loaded on the next CLK pulse.

This allows the sequence to be retriggered by software. OUT strobes low N + 1 CLK pulses after the new count of N is written.

OUT is initially high. Counting is triggered by a rising edge of GATE. When the initial count has expired, OUT goes low for one CLK pulse, then goes high again.

After a Control Word and initial count has been written, the counter is loaded on the first CLK pulse following a trigger. This CLK pulse does not decrement the count, so, given an initial count of N, OUT does not strobe low until N + 1 CLK pulses after a trigger.

A trigger causes the Counter to be loaded with the initial count on the next CLK pulse. The counting sequence is retriggerable, so OUT will not go low until N + 1 CLK pulses after any trigger. GATE has no effect on OUT.

If a new count is written during counting, the current counting sequence will not be affected. If a trigger occurs after the new count is written, but before the current count expires, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from there.

Table 6: Recommended Operating Conditions

DC Supply Voltage		+4.0V to +6.0V
Operating Temperature Range	Commercial	0°C to 70°C
	Industrial	-40°C to +85°C

Table 7: Absolute Maximum Ratings

DC Supply Voltage	+7.0V
Input, Output or I/O Voltage Applied	V_{SS} – 0.5V to V_{CC} + 0.5V
Storage Temperature Range	-65°C to +150°C
Maximum Package Power Dissipation	1W

3

Note: Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 8: Capacitance (T_A = 25°C, V_{CC} = 0V, V_{IN} = +5V or V_{SS})

Symbol	Parameter	Test Conditions	Typ	Units
$C_{I/O}$	I/O Capacitance	FREQ = 1MHz Unmeasured Pins Returned to V_{SS}	20	pF
C_{IN}	Input Capacitance		10	pF
C_{OUT}	Output Capacitance		20	pF

Table 9: DC Characteristics (T_A = 0°C to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
I_{CC}	V_{CC} Supply Current		—	20	mA
I_{CCSB}	Standby Supply Current		—	10	μA
I_{IL}	Input Load Current	V_{IN} = V_{CC} to 0V	—	±20	μA
I_{OFL}	Output Float Leakage	V_{OUT} = V_{CC} to 0.45V	—	±10	μA
V_{IH}	Input High Voltage		2.0	V_{CC}+0.5V	V
V_{IL}	Input Low Voltage		-0.5	0.8	V
V_{OH}	Output High Voltage	I_{OH} = -400μA I_{OH} = -2.5mA	3.0 2.4	— —	V V
V_{OL}	Output Low Voltage	I_{OL} = 2.5mA	—	0.4	V

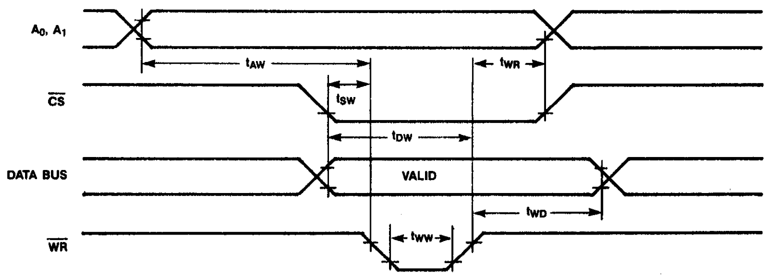
Table 10: AC Characteristics (T_A = 0°C to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V) Bus Parameters[1]

Symbol	Parameter	Test Conditions	Limits (8MHz)		Limits (10MHz)		Units
			Min	Max	Min	Max	
t_{AD}	Data delay from address		—	220	—	185	ns
t_{AR}	Address stable before $\overline{RD}$↓		45	—	30	—	ns
t_{AW}	Address stable before $\overline{WR}$		0	—	0	—	ns
t_{CL}	CLK setup for count latch		-40	45	-40	40	ns
t_{CLK}	Clock period		125	DC	100	DC	ns
t_{DF}	$\overline{RD}$↑ to data floating		5	90	5	65	ns
t_{DW}	Data setup time before $\overline{WR}$↑		120	—	95	—	ns
t_F	Clock fall time		—	25	—	25	ns
t_{GH}	Gate hold time after CLK↑	Note 2	50	—	50	—	ns
t_{GL}	Gate width low		50	—	50	—	ns
t_{GS}	Gate setup time to CLK↑		50	—	40	—	ns
t_{GW}	Gate width high		50	—	50	—	ns
t_{OD}	Output delay from CLK↓		—	150	—	100	ns
t_{ODG}	Output delay from GATE↓		—	120	—	100	ns
t_{PWH}	High pulse width	Note 3	60	—	30	—	ns
t_{PWL}	Low pulse width	Note 3	60	—	50	—	ns
t_R	Clock rise time		—	25	—	25	ns
t_{RA}	Address hold time after $\overline{RD}$↑		0	—	0	—	ns
t_{RD}	Data delay from $\overline{RD}$↓		—	120	—	85	ns
t_{RR}	$\overline{RD}$ pulse width		150	—	95	—	ns
t_{RV}	Command recovery time		200	—	165	—	ns
t_{SR}	$\overline{CS}$ stable before $\overline{RD}$↓		0	—	0	—	ns
t_{SW}	$\overline{CS}$ stable before $\overline{WR}$↓		0	—	0	—	ns
t_{WA}	Address hold time $\overline{WR}$↑		0	—	0	—	ns
t_{WC}	CLK delay for loading		0	55	0	55	ns
t_{WD}	Data hold time after $\overline{WR}$↑		0	—	0	—	ns
t_{WG}	Gate delay for sampling		-5	50	-5	40	ns
t_{WO}	OUT delay from Mode Write		—	260	—	240	ns
t_{WW}	$\overline{WR}$ pulse width		150	—	95	—	ns

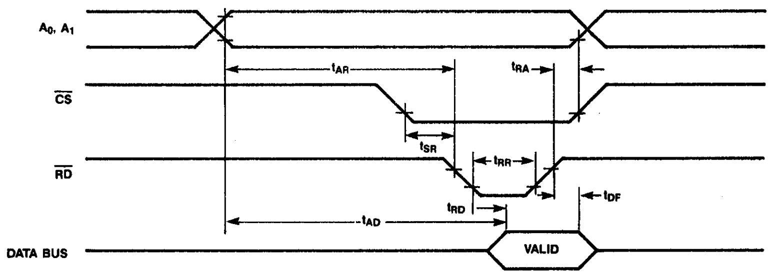
Notes:
1. AC timings measured at V_{OH} = 2.0V, V_{OL} = 0.8V.
2. In modes 1 and 5, triggers are sampled on each rising clock edge. A second trigger within 120ns of the rising clock edge may not be detected (70ns for KS82C54-10).
3. Low-going glitches that violate t_{PWH}, t_{PWL} may cause errors requiring counter reprogramming.

Figure 14: Timing Diagrams

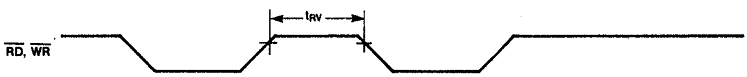
a) Write Timing



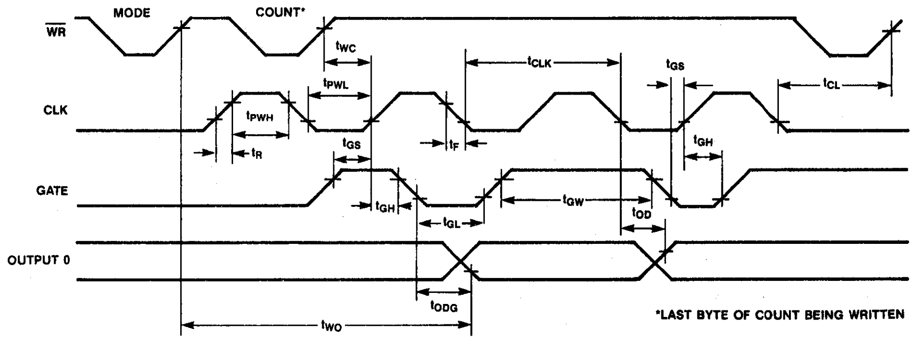
b) Read Timing



c) Recover Timing



d) Clock and Gate Timing



PACKAGE DIMENSIONS

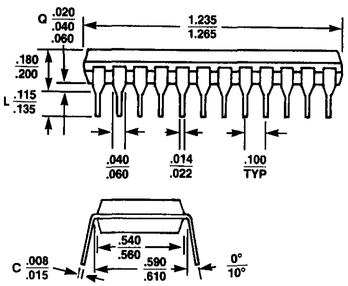


Figure 15: Plastic Package

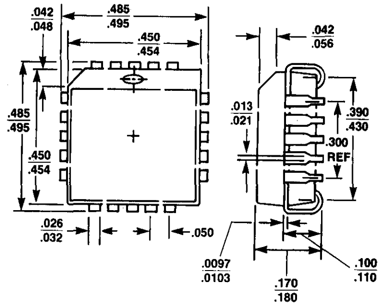


Figure 16: PLCC Package

ORDERING INFORMATION & PRODUCT CODE

KS 82C54 X X X

- **SAMSUNG SEMICONDUCTOR** — KS
- **Part Number** — 82C54
- **Speed**
  - -8 8MHz
  - -10 10MHz
- **Temperature**
  - C — Commercial (0°C to +70°C)
  - I — Industrial (-40°C to +85°C)
- **Packaging**
  - P — Plastic DIP
  - L — Plastic Leaded Chip Carrier (PLCC)

SAMSUNG products are designated by a Product Code. When ordering, please refer to products by their full code. For unusual, and/or specific packaging or processing requirements not covered by the standard product line, please contact the SAMSUNG MOS Products Group.

FEATURES/BENEFITS

- **Pin and functional compatibility with the industry standard 8255A**
- **Provides support for 8080/85, 8086/8 and 80186 286/386**
- **Very high speed — 5MHz, 8MHz and 10MHz version**
- **Low power CMOS implementation**
- **TTL input/output compatibility**
- **24 programmable I/O pins**
- **Direct bit set/reset capability**
- **Bidirectional bus operation**
- **Enhanced control word read capability**
- **Bus-hold circuitry on all I/O ports eliminates pull-up resistors**

DESCRIPTION

The KS82C55A Programmable Peripheral Interface is a high performance CMOS device offering pin for pin functional compatibility with the industry standard 8255A. It includes 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. Bus hold circuitry on all I/O ports together with TTL compatibility over the full temperature range eliminates the need for pull-up resistors.

The KS82C55A is a general purpose programmable I/O device designed for use with many different microprocessors. Also makes it an attractive addition in portable systems or systems with low power standby modes.

3

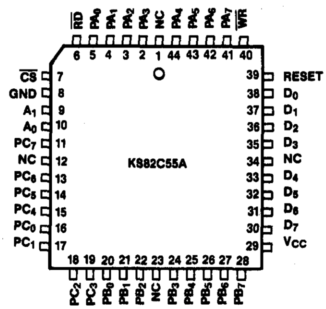


Figure 1a: 44-Pin PLCC Configuration

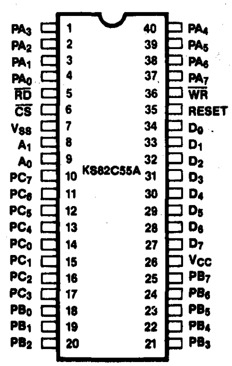


Figure 1b: 40-Pin DIP Configuration

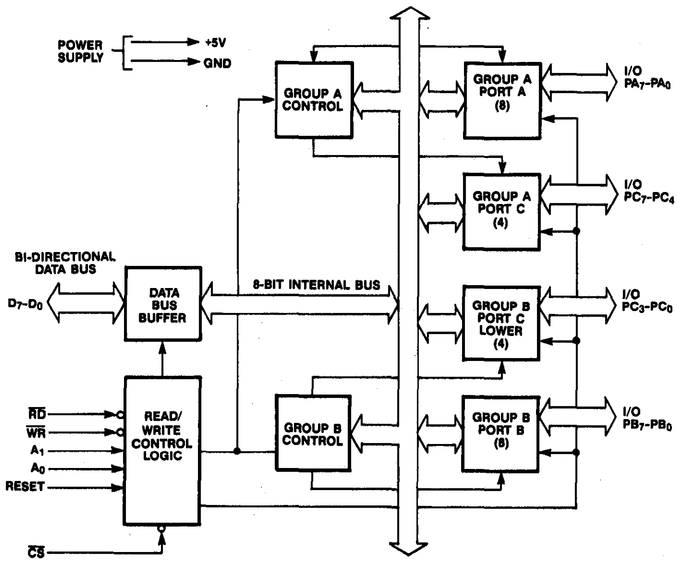


Figure 2: KS82C55A Block Diagram

Table 1a: 44-Pin PLCC Pin Assignment

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
1	NC	9	A_1	17	PC_1	25	PB_4	33	D_4	41	PA_7
2	PA_3	10	A_0	18	PC_2	26	PB_5	34	NC	42	PA_6
3	PA_2	11	PC_7	19	PC_3	27	PB_6	35	D_3	43	PA_5
4	PA_1	12	NC	20	PB_0	28	PB_7	36	D_2	44	PA_4
5	PA_0	13	PC_6	21	PB_1	29	V_{CC}	37	D_1		
6	$\overline{RD}$	14	PC_5	22	PB_2	30	D_7	38	D_0		
7	$\overline{CS}$	15	PC_4	23	NC	31	D_6	39	RESET		
8	V_{SS}	16	PC_0	24	PB_3	32	D_5	40	$\overline{WR}$		

Table 1b: 40-Pin DIP Pin Assignment

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
1	PA_3	8	A_1	15	PC_1	22	PB_4	29	D_5	36	$\overline{WR}$
2	PA_2	9	A_0	16	PC_2	23	PB_5	30	D_4	37	PA_7
3	PA_1	10	PC_7	17	PC_3	24	PB_6	31	D_3	38	PA_6
4	PA_0	11	PC_6	18	PB_0	25	PB_7	32	D_2	39	PA_5
5	$\overline{RD}$	12	PC_5	19	PB_1	26	V_{CC}	33	D_1	40	PA_4
6	$\overline{CS}$	13	PC_4	20	PB_2	27	D_7	34	D_0		
7	V_{SS}	14	PC_0	21	PB_3	28	D_6	35	RESET		

FUNCTIONAL DESCRIPTION

General

The KS82C55A is a programmable peripheral interface device designed for use in high speed, low power microcomputer systems. It is a general purpose I/O component which functions to interface peripheral equipment to the microcomputer system bus. The functional configuration of the KS82C55A is programmed by the system software such that no external logic is necessary to interface peripheral devices.

Data Bus Buffer

This 3-state bidirectional 8-bit buffer is used to interface the KS82C55A to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. The data bus buffer also transfers control words and status information.

Read/Write and Control Logic

This block manages all of the internal and external transfers of both Data and Control or Status Words. It accepts inputs from the CPU Address and Control buses and issues commands to both of the Control Groups.

Group A and Group B Controls

The functional configuration of each port is programmed by the system software. The CPU outputs a Control Word to the KS82C55A. The Control Word contains information such as code, bit set, bit reset, etc., that initializes the functional configuration of the KS82C55A.

Each of the Control blocks (Group A and Group B) accepts commands from the Read/Write Control Logic, receives Control Words from the internal data bus and issues the proper commands to its associated ports.

- Control Group A - Port A and Port C upper (C_7-C_4)
- Control Group B - Port B and Port C lower (C_3-C_0)

Table 2: Pin Descriptions

Symbol	Type	Name and Function
A_0, A_1	I	**Address:** These input signals in conjunction with $\overline{RD}$ and $\overline{WR}$, control the selection of one of the three ports or the Control Word Registers.

A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	Input Operation (Read)
0	0	0	1	0	Port A - Data Bus
0	1	0	1	0	Port B - Data Bus
1	0	0	1	0	Port C - Data Bus
1	1	0	1	0	Control Word - Data Bus

A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	Output Operation (Write)
0	0	1	0	0	Data Bus - Port A
0	1	1	0	0	Data Bus - Port B
1	0	1	0	0	Data Bus - Port C
1	1	1	0	0	Data Bus - Control

A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	Disable Function
X	X	X	X	1	Data Bus - 3-State
X	X	1	1	0	Data Bus - 3-State

Symbol	Type	Name and Function
$\overline{CS}$	I	**Chip Select:** A low on this input enables the KS82C55A to respond to $\overline{RD}$ and $\overline{WR}$ signals. $\overline{RD}$ and $\overline{WR}$ are ignored otherwise.
D_{0-7}	I/O	**Data Bus:** Bi-directional, 3-state data bus lines, connected to system data bus.
PA_{0-7}	I/O	**Port A, Pins 0-7:** An 8-bit data output latch/buffer and an 8-bit data input buffer.
PB_{0-7}	I/O	**Port B, Pins 0-7:** An 8-bit data output latch/buffer and an 8-bit data input buffer.
PC_{0-3}	I/O	**Port C, Pins 0-3:** Lower nibble of an 8-bit data output latch/buffer and an 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B.
PC_{4-7}	I/O	**Port C, Pins 4-7:** Upper nibble of Port C.
$\overline{RD}$	I	**Read Control:** This input is low during CPU read operations.
$\overline{WR}$	I	**Write Control:** This input is low during CPU write operations.
RESET	I	**Reset:** A high on this input clears the control register and all ports are set to the input mode.
V_{CC}	—	**Power:** 5V ± 10% DC Supply.
V_{SS}	—	**Ground:** 0V.

The Control Word Register can be both written and read as shown in the address decode table in the pin descriptions (Table 2). The Control Word format for both read and write operations is shown in Figure 8. Bit D_7 will always be a logic ONE when the Control Word is read, as this implies control word mode information.

Ports A, B, and C

The KS82C55A contains three 8-bit ports (A, B, and C). All three ports can be configured in a wide variety of functional characteristics by the system software, but each also has its own special features.

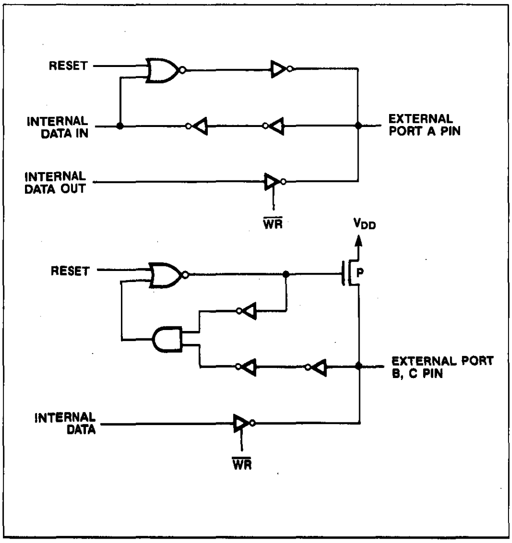
Port A: One 8-bit data output buffer and one 8-bit input buffer. Both pull-up and pull-down bus-hold devices are present on Port A.

Port B: One 8-bit data output buffer and one 8-bit data input buffer. Only pull-up bus-hold devices are present on Port B.

Port C: One 8-bit data output buffer and one 8-bit data input buffer (no latch for input). Port C can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B. Only pull-up bus-hold devices are present on Port C.

See Figure 3 for the bus-hold circuit configuration for Ports A, B, and C.

Figure 3: Port A, B, C, Bus-Hold Configuration



OPERATIONAL DESCRIPTION

Mode Selection

There are three basic modes of operation that can be selected by the system software:

- Mode 0 - Basic Input/Output
- Mode 1 - Strobed Input/Output
- Mode 2 - Bidirectional Bus

When the Reset input goes high, all ports will be set to the input mode with all 24 port lines held at a logic one level by the internal bus hold devices. After the reset is removed, no additional initialization is required for the KS82C55A to remain in the input mode. No pull-up or pull-down devices are required. During execution, any of the other modes may be selected by using a single output instruction. This allows a single KS82C55A to service a variety of peripheral devices with a simple software maintenance routine.

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed. Modes may be combined such that their functional definition can be tailored to almost any I/O structure. For example, Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, and Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.

Single Bit Set/Reset Feature

Any of the eight bits of Port C can be Set or Reset using a single output instruction. This feature reduces the software requirements in control-based applications.

When Port C is being used as status/control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation as if they were data output ports.

Interrupt Control Functions

When the KS82C55A is operating in Mode 1 or Mode 2, control signals are provided for use as interrupt request inputs to the CPU. The interrupt request signals, generated from Port C, can be inhibited or enabled by setting or resetting the associated INTE flip-flop using the Bit Set/Reset function of Port C.

This function allows the Programmer to Enable or Disable a specific I/O device to interrupt the CPU without affecting any other device in the interrupt structure.

Figure 4: Mode Definitions & Bus Interface

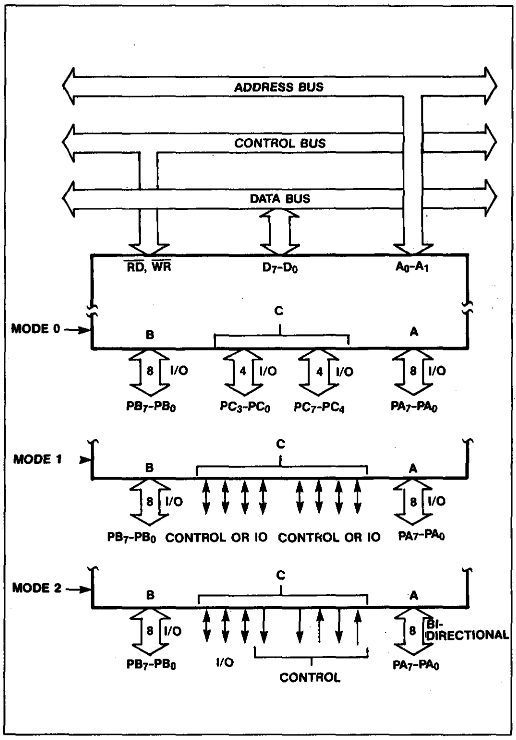
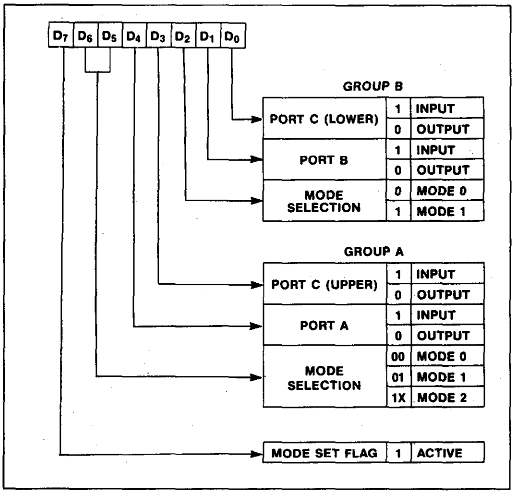


Figure 5: Mode Definition Format



INTE Flip-Flop Definition:

(Bit-Set) - INTE is Set - Interrupt enable
(Bit-Reset) - INTE is Reset - Interrupt disable

Note: All mask flip-flops are automatically reset during mode selection and device reset.

Mode 0 (Basic Input/Output)

This mode provides simple input and output operations for each of the three ports. No handshaking is required. Data is simply written to or read from a specified port.

Mode 0 Basic Functional Definitions:

- Two 8-bit ports and two 4-bit ports
- Any port can be input or output
- Outputs are latched
- Inputs are not latched
- 16 different Input/Output configurations are possible in this mode.

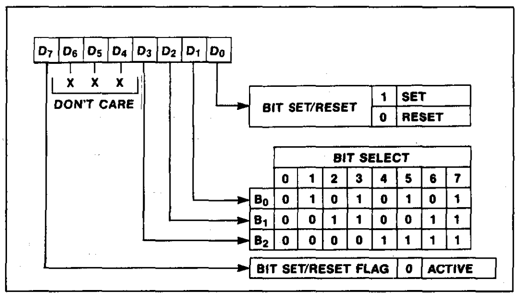
Mode 1 (Strobed Input/Output)

This mode transfers I/O data to or from a specified port in conjunction with strobes or handshaking signals. In Mode 1, Port A and Port B use the lines on Port C to generate or accept these handshaking signals.

Mode 1 Basic Functional Definitions:

- Two Groups (Group A and Group B).
- Each group contains one 8-bit data port and one 4-bit control/data port.
- The 8-bit data port can be either input or output. Both inputs and outputs are latched.
- The 4-bit port is used for control and status of the 8-bit data port.

Figure 6: Bit Set/Reset Format



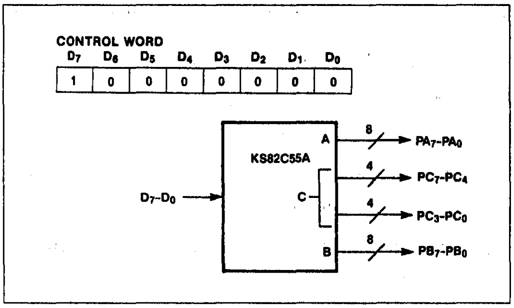
3

Input Control Signal Definitions

STB (Strobe Input): A LOW on this input loads data into the input latch.

IBF (Input Buffer Full F/F): A HIGH on this output indicates that the data has been loaded into the input latch. IBF is set by the STB input being LOW and is RESET by the rising edge of the RD input.

Figure 7: Mode 0 Configuration



INTR (Interrupt Request): A HIGH on this output can be used to interrupt the CPU when an input device is requesting service. INTR is set by the STB being a ONE, IBF is a ONE, and INTE is a ONE. It is RESET by the falling edge of RD. This procedure allows an input device to request service from the CPU by simply strobing its data into the Port.

INTE A: Controlled by bit Set/Reset of PC_4.

INTE B: Controlled by bit Set/Reset of PC_2.

Output Control Signal Definition

OBF (Output Buffer Full F/F): The OBF output will go LOW to indicate that the CPU has written data out to the specified port. The OBF F/F will be set by the rising edge of the WR input and reset by the ACK input being low.

ACK (Acknowledge Input): A LOW on this input informs the KS82C55A that the data from Port A or Port B has been accepted. (i.e., a response from the peripheral device indicating that it has received the data output by the CPU).

Table 3: Mode 0 Port Definition

Control Word #	Control Word Bits								Port Direction			
		Group A				Group B			Group A		Group B	
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	PA_7-PA_0	PC_7-PC_4	PC_3-PC_0	PB_7-PB_0
0	1	0	0	0	0	0	0	0	OUTPUT	OUTPUT	OUTPUT	OUTPUT
1	1	0	0	0	0	0	0	1	OUTPUT	OUTPUT	INPUT	OUTPUT
2	1	0	0	0	0	0	1	0	OUTPUT	OUTPUT	OUTPUT	INPUT
3	1	0	0	0	0	0	1	1	OUTPUT	OUTPUT	INPUT	INPUT
4	1	0	0	0	1	0	0	0	OUTPUT	INPUT	OUTPUT	OUTPUT
5	1	0	0	0	1	0	0	1	OUTPUT	INPUT	INPUT	OUTPUT
6	1	0	0	0	1	0	1	0	OUTPUT	INPUT	OUTPUT	INPUT
7	1	0	0	0	1	0	1	1	OUTPUT	INPUT	INPUT	INPUT
8	1	0	0	1	0	0	0	0	INPUT	OUTPUT	OUTPUT	OUTPUT
9	1	0	0	1	0	0	0	1	INPUT	OUTPUT	INPUT	OUTPUT
10	1	0	0	1	0	0	1	0	INPUT	OUTPUT	OUTPUT	INPUT
11	1	0	0	1	0	0	1	1	INPUT	OUTPUT	INPUT	INPUT
12	1	0	0	1	1	0	0	0	INPUT	INPUT	OUTPUT	OUTPUT
13	1	0	0	1	1	0	0	1	INPUT	INPUT	INPUT	OUTPUT
14	1	0	0	1	1	0	1	0	INPUT	INPUT	OUTPUT	INPUT
15	1	0	0	1	1	0	1	1	INPUT	INPUT	INPUT	INPUT

INTR (Interrupt Request): A HIGH on this output can be used to interrupt the CPU when an output device has accepted data transmitted by the CPU. INTR is set when $\overline{ACK}$ is a ONE, $\overline{OBF}$ is a ONE and INTE is a ONE. It is Reset by the falling edge of $\overline{WR}$.

INTE A: Controlled by bit Set/Reset of PC_4.

INTE B: Controlled by bit Set/Reset of PC_2.

Mode 2 (Strobed Bidirectional Bus I/O)

This mode provides a means for communicating with a peripheral device on a single 8-bit bus to facilitate both transmitting and receiving of data (bi-directional bus I/O). Handshaking signals maintain proper bus flow discipline in a similar manner to Mode 1. Interrupt generation and enable/disable functions are also available.

Mode 2 Basic Functional Definitions:

- Used in Group A only.
- One 8-Bit, bi-directional bus port (Port A) and a 5-bit control port (Port C).
- Both inputs and outputs are latched.
- The 5-bit control port (Port C) is used for control and status of the 8-bit, bi-directional bus port (Port A).

Bidirectional Bus I/O Control Signal Definition

INTR (Interrupt Request): A HIGH on this output can be used to interrupt the CPU for input or output operations.

Output Operations

$\overline{OBF}$ (Output Buffer Full): The $\overline{OBF}$ output will go LOW to indicate that the CPU has written data into Port A.

$\overline{ACK}$ (Acknowledge): A LOW on this input enables the 3-state output buffer of Port A to send out the data. Otherwise, the output buffer will be in the high impedance state.

INTE1 (The INTE Flip-Flop Associated with OBF): Controlled by bit Set/Reset of PC_6.

Input Operations

$\overline{STB}$ (Strobe Input): A LOW on this input loads data into the input latch.

IBF (Input Buffer Full F/F): A HIGH on this output indicates that data has been loaded into the input latch.

INTE2 (The INTE Flip-Flop Associated with IBF): Controlled by bit Set/Reset of PC_4.

3

Figure 8: Mode 1 Input

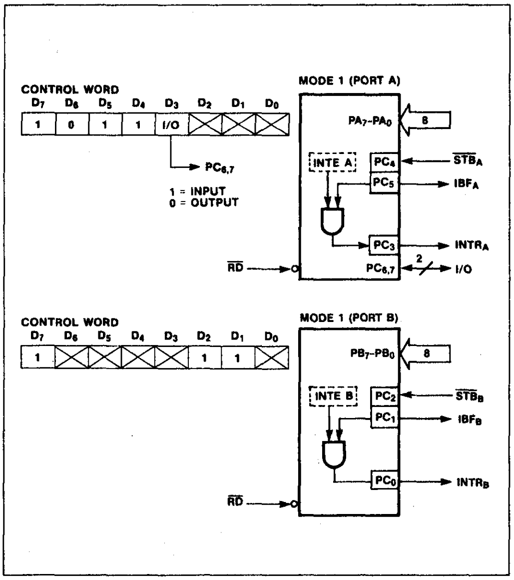
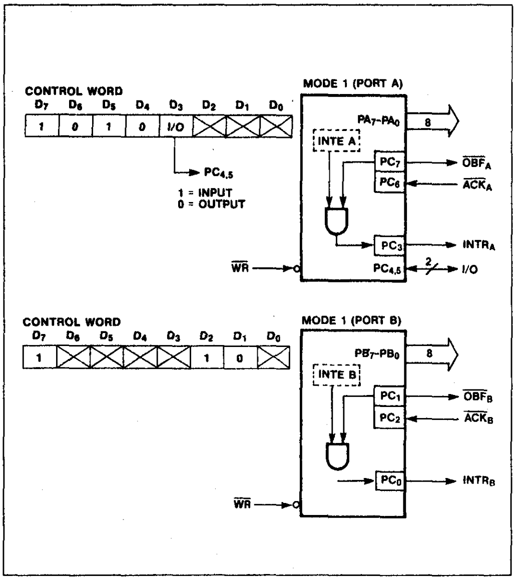


Figure 9: Mode 1 Output



Special Mode Combination Considerations

Several combinations of modes are possible. For any combination, some or all of the Port C lines are used for control or status. The remaining bits are either inputs or outputs as defined by a Set Mode command.

The state of all the Port C lines, except the $\overline{ACK}$ and $\overline{STB}$ lines, will be placed on the data bus during a read of Port C. In place of the $\overline{ACK}$ and $\overline{STB}$ line states, flag status will appear on the data bus in the PC_2, PC_4, and PC_6 bit positions as shown in Table 4.

Through a Write Port C command, only the Port C pins programmed as outputs in a Mode 0 group can be written. No other pins can be affected by a Write Port C command, and the interrupt enable flags cannot be accessed. The Set/Reset Port C Bit command must be used to write to any Port C output programmed as an output in a Mode 1 group or to change an interrupt enable flag.

With a Set/Reset Port C Bit command, any Port C line programmed as an output (including INTR, IBF and $\overline{OBF}$) can be written, or an interrupt enable flag can be set or reset. Port C lines programmed as inputs, including $\overline{ACK}$ and $\overline{STB}$ lines, are not affected by a Set/Reset Port C Bit command. Writing to the corresponding Port C bit positions of the $\overline{ACK}$ and $\overline{STB}$ lines with the Set/Reset Port C Bit command will affect the Group A and Group B interrupt enable flags (see Table 5).

Current Drive Capability

Any output on Port A, B or C can sink or source 2.5mA. Thus the KS82C55A can directly drive Darlington type drivers and high-voltage displays that require such sink or source current.

Reading Port C Status

In Mode 0, Port C transfers data to or from the peripheral device. When the KS82C55A is in Modes 1 or 2, Port C generates or accepts handshaking signals with the peripheral device. Reading Port C allows the programmer to test or verify the status of each peripheral device and change the program flow accordingly.

There is not special instruction to read the status information from Port C. This function is performed by executing a normal read operations of Port C.

Figure 10: Combinations of Mode 1

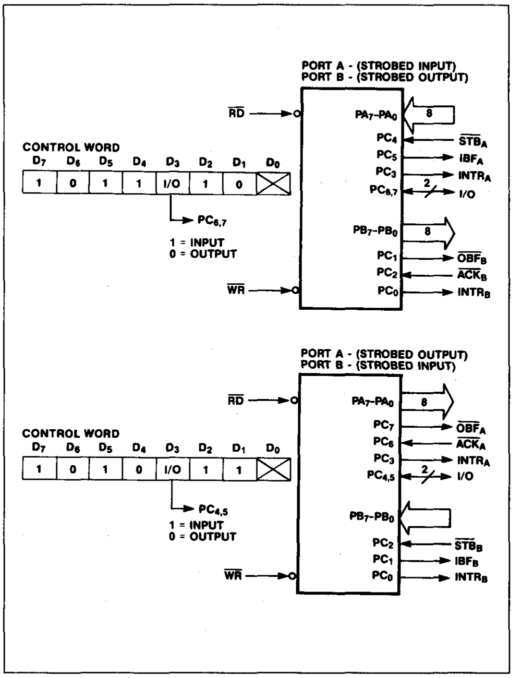


Figure 11: Mode Control Word

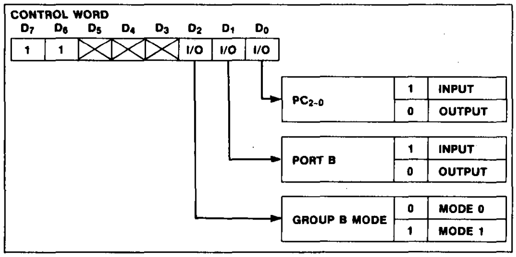


Figure 12: Mode 2

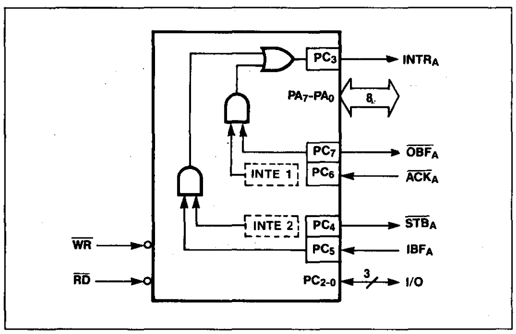


Figure 13: Mode 1/4 Combinations

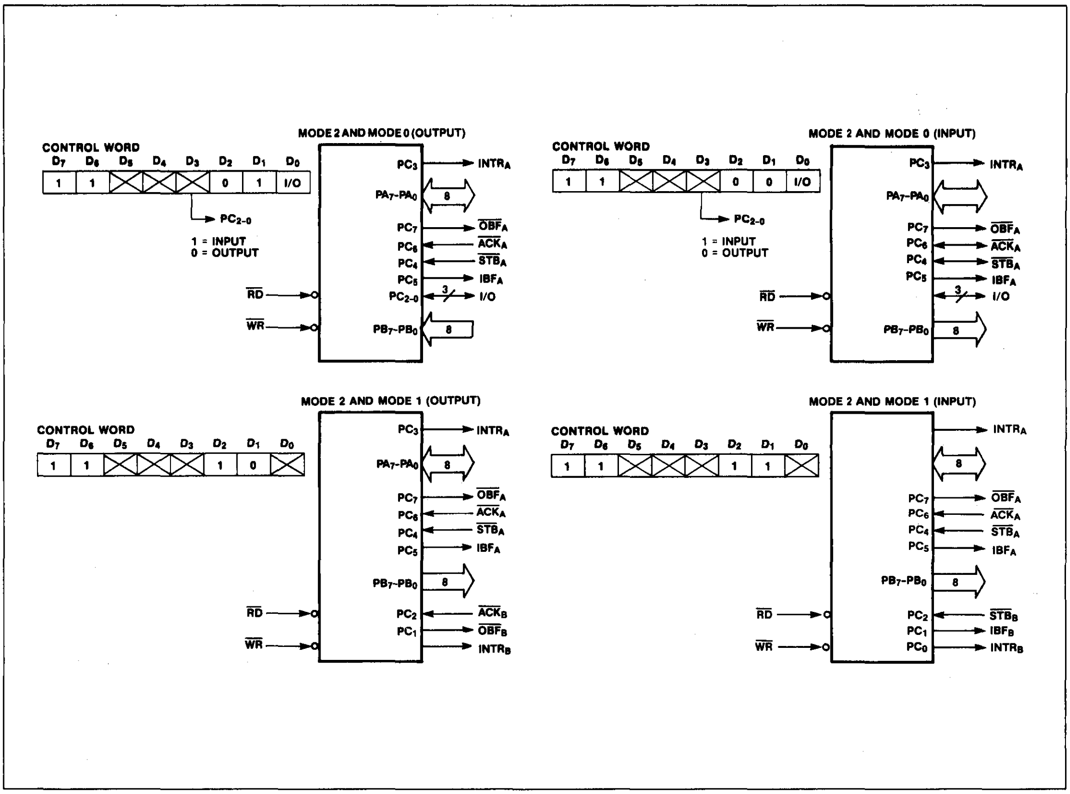


Figure 14: Mode 1 Status Word Format

INPUT CONFIGURATION

D7	D6	D5	D4	D3	D2	D1	D0
I/O	I/O	IBFA	INTEA	INTRA	INTEB	IBFB	INTRB
GROUP A					GROUP B		

INPUT CONFIGURATION

D7	D6	D5	D4	D3	D2	D1	D0
OBFA	INTEA	I/O	I/O	INTRA	INTEB	OBFB	INTRB
GROUP A					GROUP B		

Figure 15: Mode 2 Status Word Format

D7	D6	D5	D4	D3	D2	D1	D0
OBFA	INTE1	IBFA	INTE2	INTRA			
GROUP A					GROUP B		

(DEVINED BY MODE 0 OR MODE 1 SELECTION)

Table 4: Mode Definition Summary

PORT		MODE 0	MODE 1				MODE 2
PORT A	PA_0 PA_1 PA_2 PA_3 PA_4 PA_5 PA_6 PA_7	All IN or All OUT	All IN or All OUT				All BIDIRECTIONAL
PORT B	PB_0 PB_1 PB_2 PB_3 PB_4 PB_5 PB_6 PB_7	All IN or All OUT	All IN or All OUT				MODE 0 or MODE 1 only
			A IN, B IN	A IN, B OUT	A OUT, B IN	A OUT, B OUT	
PORT C	PC_0	All IN	$INTR_B$	$INTR_B$	$INTR_B$	$INTR_B$	I/O
	PC_1	or	IBF_B	OBF_B	IBF_B	OBF_B	I/O
	PC_2	All OUT	STB_B	ACK_B	STB_B	ACK_B	I/O
	PC_3		$INTR_A$	$INTR_A$	$INTR_A$	$INTR_A$	$INTR_A$
	PC_4	All IN	STB_A	STB_A	I/O	I/O	STB_A
	PC_5	or	IBF_A	IBF_A	I/O	I/O	IBF_A
	PC_6	All OUT	I/O	I/O	ACK_A	ACK_A	ACK_A
	PC_7		I/O	I/O	OBF_A	OBF_A	OBF_A

Table 5: Interrupt Enable Flags in Modes 1 and 2

Interrupt Enable Flag	Position	Alternate Port C Pin Signal (Mode)
$INTE_B$	PC_2	$\overline{ACK}_B$ (Output Mode 1) or STB_B (Input Mode 1)
$INTE_{A2}$	PC_4	$\overline{STB}_A$ (Input Mode 1 or Mode 2)
$INTE_{A1}$	PC_6	$\overline{ACK}_A$ (Output Mode 1 or Mode 2)

APPLICATIONS

The KS82C55A is a very powerful device for interfacing peripheral equipment to the microcomputer system. It is flexible enough to interface almost any I/O device without the need for additional external logic.

Each peripheral device in a microcomputer system usually has a service routine associated with it. The routine manages the software interface between the device and the CPU. The functional definition of the KS82C55A is programmed by the I/O service routine and becomes an extension of the system software. By examining the interface characteristics of the I/O device for both data transfer and timing, and matching this information to the examples and tables in the Operational Description, a Control Word can easily be developed to intialize the KS82C55A to exactly fit the application. Figures 16 through 22 illustrate a few examples of typical KS82C55A applications.

Figure 16: Keyboard and Display Interface

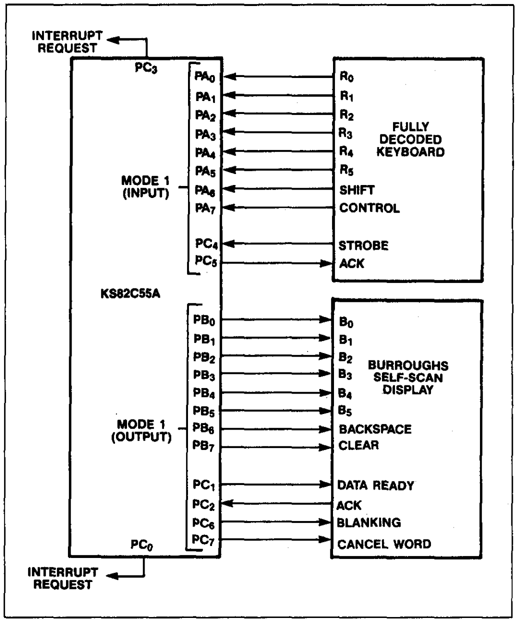


Figure 17: Printer Interface

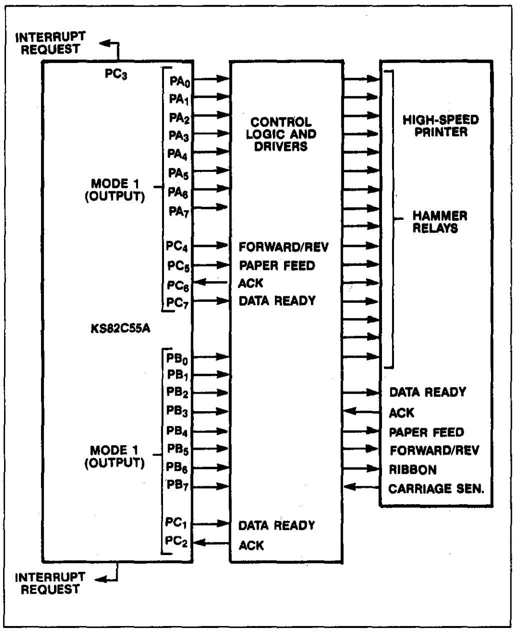


Figure 18: Keyboard and Terminal Address Interface

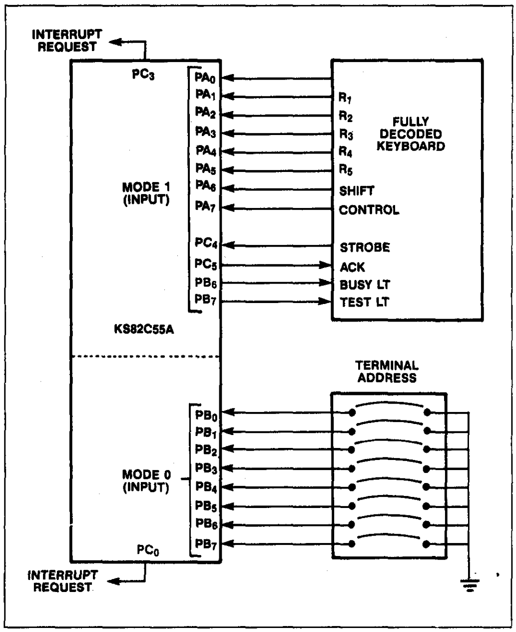


Figure 19: D/A, A/D

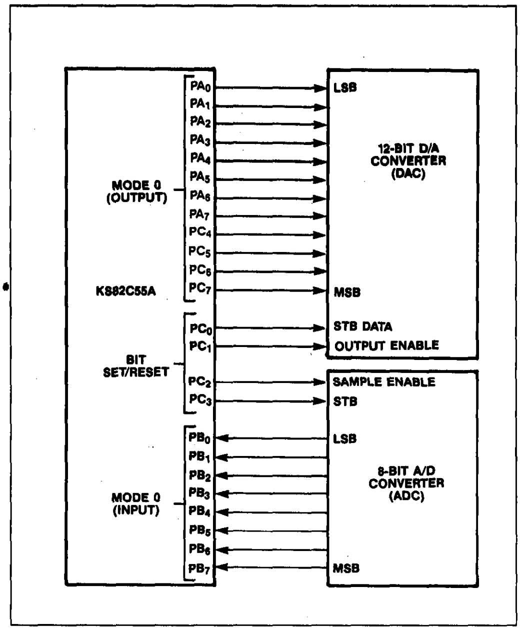


Figure 20: Basic Floppy Disc Interface

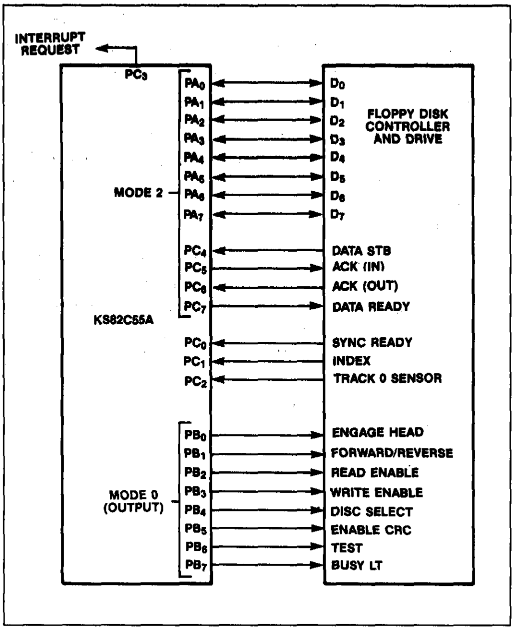


Figure 21: Basic CRT Controller Interface

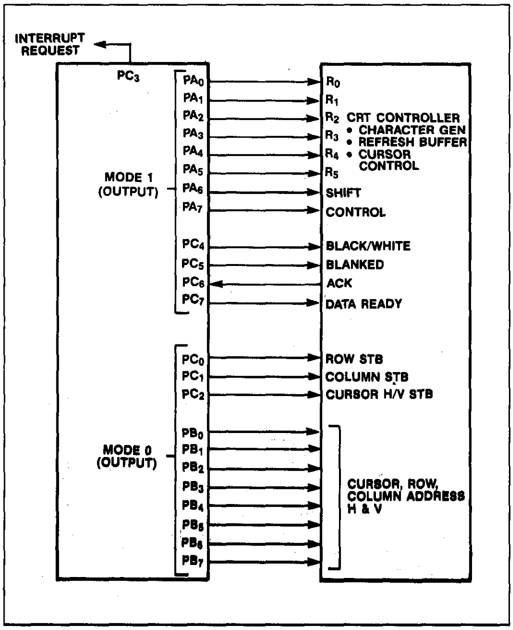


Figure 22: Machine Tool Controller

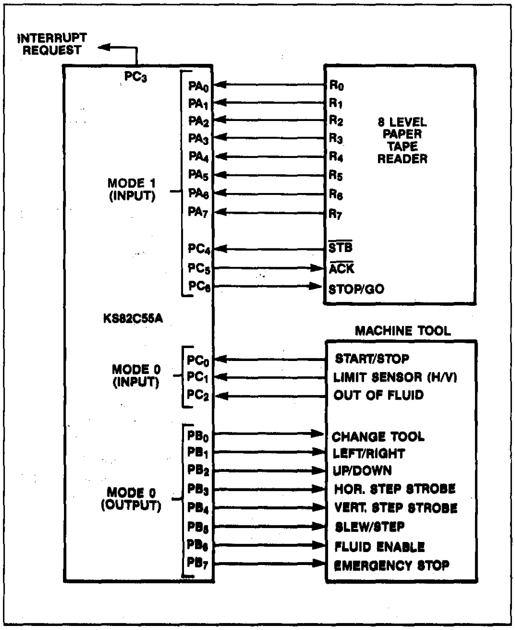


Table 6: Recommended Operating Conditions

DC Supply Voltage		+4.0V to +6.0V
Operating Temperature Range	Commercial	0°C to 70°C
	Industrial	-40°C to +85°C

Table 7: Absolute Maximum Ratings

DC Supply Voltage	+7.0V
Input, Output or I/O Voltage Applied	V_{SS} - 0.5V to V_{CC} + 0.5V
Storage Temperature Range	-65°C to +150°C
Maximum Package Power Dissipation	1W

Note: Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 8: Capacitance (T_A = 25°C, V_{CC} = 0V, V_{IN} = +5V or V_{SS})

Symbol	Parameter	Test Conditions	Typ	Units
$C_{I/O}$	I/O Capacitance	Unmeasured Pins Returned to V_{SS}	20	pF
C_{IN}	Input Capacitance		10	pF

Table 9: DC Characterisitcs (T_A = 0°C to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Symbol	Parameter	Test Conditions	Limits Min	Limits Max	Unit
I_{CC}	V_{CC} Supply Current	(Note 3)		10	mA
I_{CCSB}	V_{CC} Supply Current-Standby	V_{CC} = 5.5V, V_{IN} = V_{CC} or V_{SS} Port Conditions: If I/P = Open/High — O/P = Open Only With Data Bus = High/Low — CS = High — Reset = Low Pure Inputs = Low/High		10	μA
I_{DAR}	Darlington Drive Current	Ports A, B, C R_{EXT} = 750Ω, V_{EXT} = 1.5V	±2.5		mA
I_{IL}	Input Leakage Current	V_{IN} = V_{CC} to 0V (Note 1)		±1	μA
I_{OFL}	Output Float Leakage Current	V_{IN} = V_{CC} to 0V (Note 2)		±10	μA
I_{PHH}	Port Hold High Leakage Current	V_{OUT} = 3.0V (Ports A, B, C)	-50	-300	μA
I_{PHHO}	Port Hold High Overdrive Current	V_{OUT} = 3.0V	+350		μA
I_{PHL}	Port Hold Low Leakage Current	V_{OUT} = 1.0V (Port A Only)	+50	+300	μA
I_{PHLO}	Port Hold Low Overdrive Current	V_{OUT} = 0.8V	-350		μA
V_{IH}	Input High Voltage		2.0	V_{CC}	V
V_{IL}	Input Low Voltage		-0.5	0.8	V
V_{OH}	Output High Voltage	I_{OH} = -2.5mA I_{OH} = -100μA	3.0 V_{CC} - 0.4		V V
V_{OL}	Output LOW Voltage	I_{OL} = 2.5mA		0.4	V

Notes: 1. Pins A1, A0, $\overline{CS}$, $\overline{WR}$, $\overline{RD}$, Reset. 2. Data Bus; Ports B, C. 3. Outputs Open.

Table 10: AC Characteristics (T_A = 0°C to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

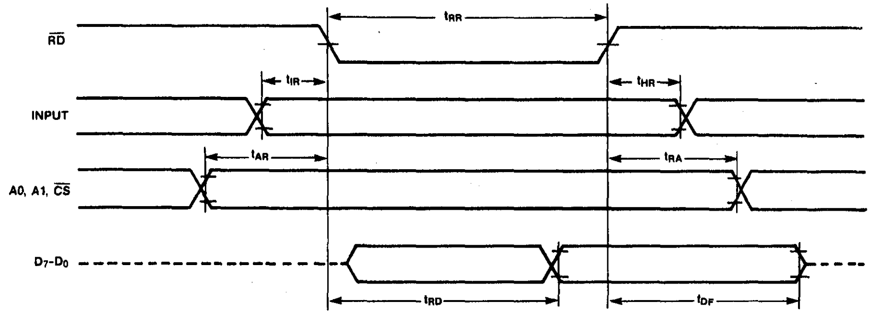
Symbol	Parameter	Test Conditions	Limits (8MHz)		Limits (10MHz)		Units
			Min	Max	Min	Max	
t_{AD}	$\overline{ACK}$ = 0 to Output			175		125	ns
t_{AIT}	$\overline{ACK}$ = 1 to INTR = 1			150		100	ns
t_{AK}	$\overline{ACK}$ Pulse Width		200		100		ns
t_{AOB}	$\overline{ACK}$ = 0 to $\overline{OBF}$ = 1			150		100	ns
t_{AR}	Address Strobe Before $\overline{RD}\downarrow$		0		0		ns
t_{AW}	Address Strobe Before $\overline{WR}\downarrow$		0		0		ns
t_{DF}	$\overline{RD} \neq$ Data Floating $\overline{RD}\uparrow$ to Data Floating		10	75	10	75	ns
t_{DW}	Data Setup Time Before $\overline{WR}\uparrow$		100		50		ns
t_{HR}	Peripheral Data After $\overline{RD}$		0		0		ns
t_{IR}	Peripheral Data Before $\overline{RD}$		0		0		ns
t_{KD}	$\overline{ACK}$ = 1 to Output Float		20	250	20	175	ns
t_{PH}	Peripheral Data After $\overline{STB}$ High		50		40		ns
t_{PS}	Peripheral Data Before $\overline{STB}$ High		20		20		ns
t_{RA}	Address Hold Time After $\overline{RD}\uparrow$		0		0		ns
t_{RD}	Data Delay from $\overline{RD}\downarrow$			120		95	ns
t_{RES}	Reset Pulse Width	See Note 2	500		400		ns
t_{RIB}	$\overline{RD}$ = 1 to IBF = 0			150		120	ns
t_{RIT}	$\overline{RD}$ = 0 to INTR = 0			200		160	ns
t_{RR}	$\overline{RD}$ Pulse Width		150		100		ns
t_{RV}	Recovery Time Between $\overline{RD}/\overline{WR}$		200		100		ns
t_{SIB}	$\overline{STB}$ = 0 to IBF = 1			150		100	ns
t_{SIT}	$\overline{STB}$ = 1 to INTR = 1			150		100	ns
t_{ST}	$\overline{STB}$ Pulse Width		100		50		ns
t_{WA}	Address Hold Time After $\overline{WR}\uparrow$	Ports A & B Port C	20 20		10 10		ns ns
t_{WB}	$\overline{WR}$ = 1 to Output			350		150	ns
t_{WD}	Data Hold Time After $\overline{WR}\uparrow$	Ports A & B Port C	30 30		20 20		ns ns
t_{WIT}	$\overline{WR}$ = 0 to INTR = 0	See Note 1		200		160	ns
t_{WOB}	$\overline{WR}$ = 1 to $\overline{OBF}$ = 0			150		120	ns
t_{WW}	$\overline{WR}$ Pulse Width		100		70		ns

Notes: 1. INTR↑ may occur as early as $\overline{WR}\downarrow$.
2. Width of initial Reset pulse after power on must be at least 50μsec. Subsequent Reset pulses may be 500ns minimum.

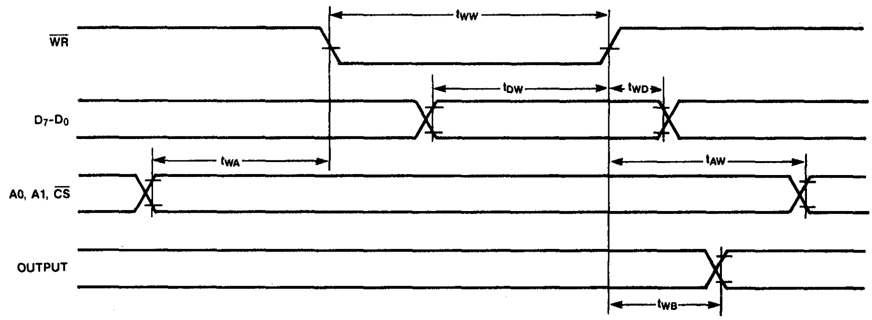
3

Figure 23: Timing Diagrams

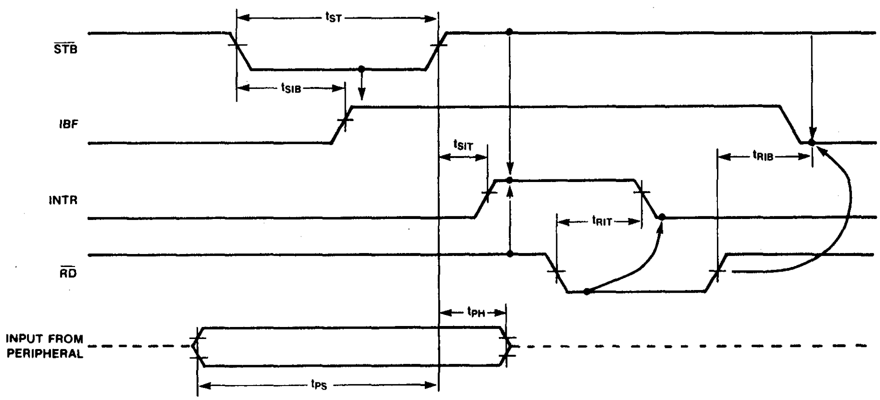
a) Mode 0 (Basic Input)



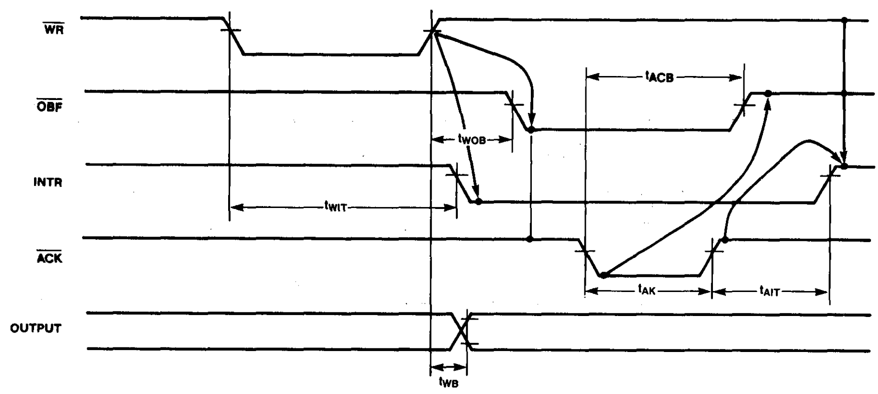
b) Mode 0 (Basic Output)



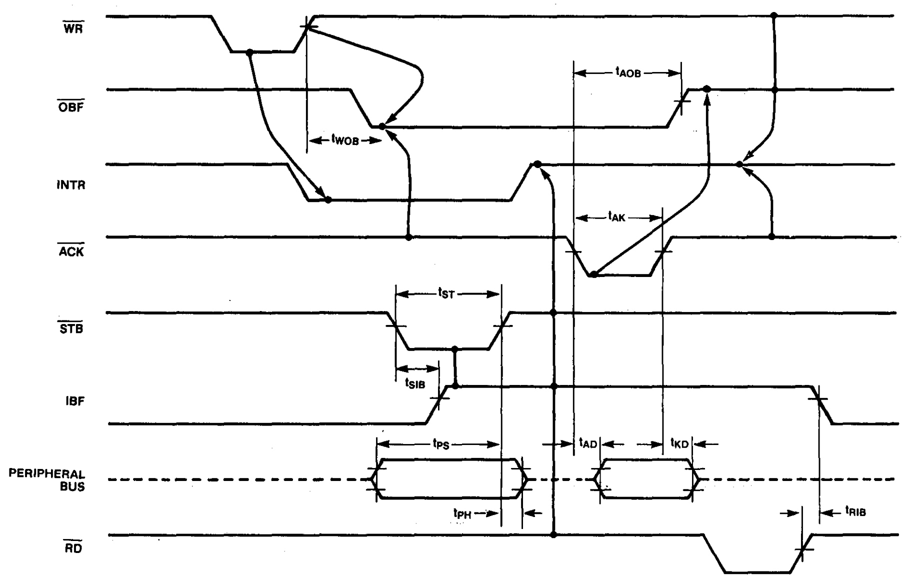
c) Mode 1 (Strobed Input)



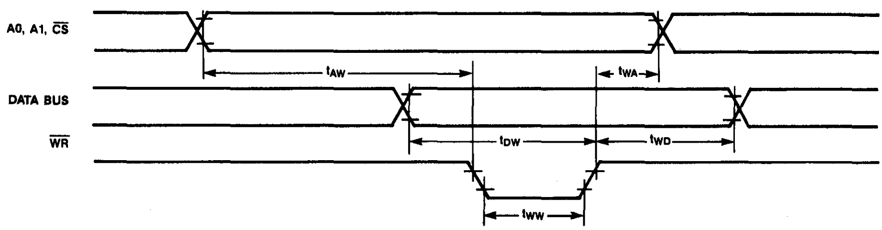
d) Mode 1 (Strobed Output)



e) Mode 2 (Bidirectional)



f) Write Timing



g) Read Timing

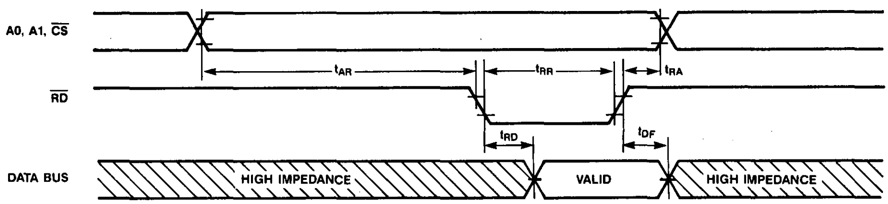
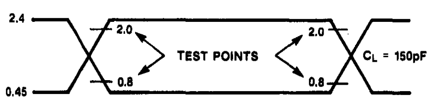
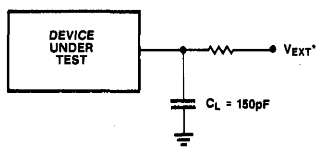


Figure 24: AC Testing I/O Waveform



A.C. Testing Inputs are driven at 2.4V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at 2.0V for a logic 1 and 0.8V for logic 0.

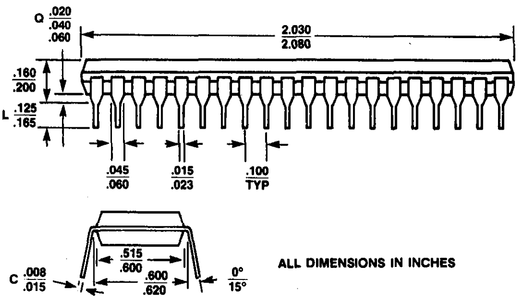
Figure 25: AC Testing Load Circuit



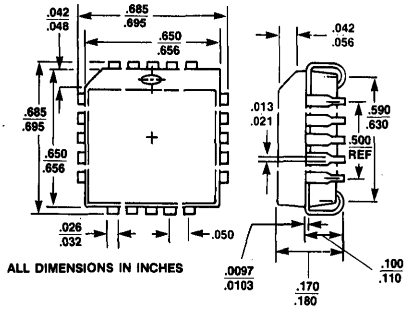
* V_{EXT} is set at various voltages during testing to guarantee the specification. C_L includes jig capacitance.

3

PACKAGE DIMENSIONS



Plastic Package



PLCC Package

ORDERING INFORMATION & PRODUCT CODE DIMENSIONS

KS 82C55A X X X

- **KS** — SAMSUNG SEMICONDUCTOR
- **82C55A** — Part Number
- **X** — **Speed**
  - -8 8MHz
  - -10 10MHz
- **X** — **Temperature**
  - C — Commercial (0°C to +70°C)
  - I — Industrial (-40°C to +85°C)
- **X** — **Packaging**
  - P — Plastic DIP
  - L — Plastic Leaded Chip Carrier (PLCC)

SAMSUNG products are designated by a Product Code. When ordering, please refer to products by their full code. For unusual, and/or specific packaging or processing requirements not covered by the standard product line, please contact the SAMSUNG MOS Products Group.

KS82C59A

PROGRAMMABLE INTERRUPT CONTROLLER

FEATURES

- Pin and functional compatibility with the industry standard 8259/8259A
- TTL input/output compatibility
- Low power CMOS implementation
- Compatible with 8080/85, 8086/88, 80286/386 and 68000 family microprocessor systems
- Eight level priority controller
- Expandable to 64 levels
- Programmable interrupt modes, with each interrupt maskable
- Edge- or level-triggered interrupt request inputs
- Polling operation
- Fully static design

DESCRIPTION

The KS82C59A is a high performance, completely programmable interrupt controller. It can process eight interrupt request inputs, assigning a priority level to each one, and is cascadable up to 64 interrupt requests. Individual interrupting sources are maskable. Its two modes of operation (Call and Vector) allow it to be used with a wide variety of microprocessors.

Featuring fully static, very high speed operation, the KS82C59A is designed to relieve the system CPU from polling in a multi-level priority interrupt system. Its very low power consumption makes it useful in portable systems and systems with low power standby modes.

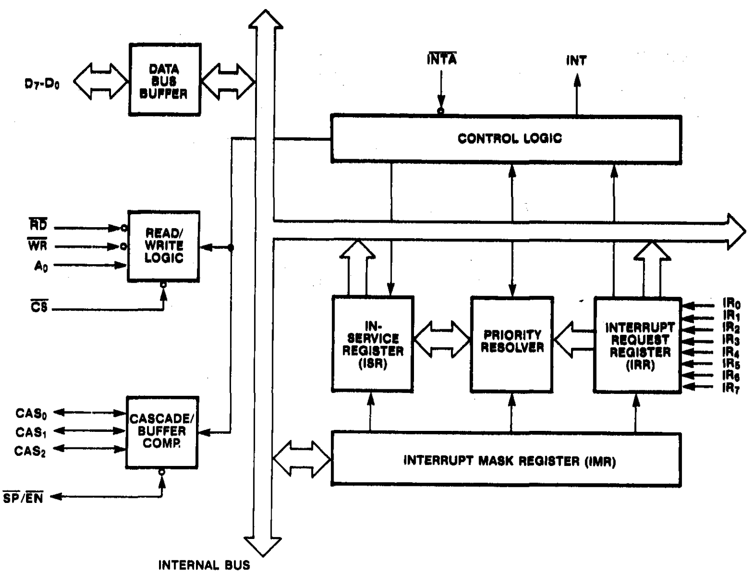


Figure 1: Block Diagram of KS82C59A

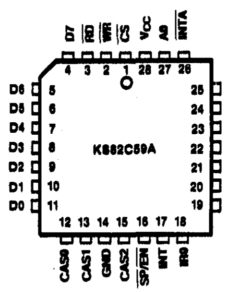


Figure 2a: 28-Lead PLCC

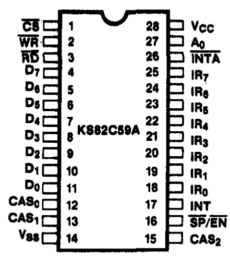


Figure 2b: Pin Configuration

Table 1: Pin Descriptions

Symbol	Pin (28-Pin DIP)	Type	Name and Function
A_0	27	I	**A_0 Address Line:** This signal acts in conjunction with the $\overline{CS}$, $\overline{WR}$ and $\overline{RD}$ signals. It is used by the KS82C59A to decipher various Command Words written by the CPU, and Status information read by the CPU. It is typically connected to the CPU-A_0 address line.
CAS_{0-2}	12, 13, 15	I/O	**Cascade Line:** These signals are outputs for the master KS82C59A, and inputs for slaved KS82C59As. The CAS lines are used as a private bus by a KS82C59A master to control a multiple KS82C59A system structure.
$\overline{CS}$	1	I	**Chip Select:** An active LOW signal used to enable $\overline{RD}$ and $\overline{WR}$ communication between the CPU and the KS82C59A. Note that $\overline{INTA}$ functions are independent of $\overline{CS}$.
D_7–D_0	4-11	I/O	**Data Bus:** Bidirectional, 3-state, 8-bit data bus for the transfer of control, status and interrupt vector information.
INT	17	O	**Interrupt:** This signal goes HIGH when a valid interrupt request is asserted. It is used to interrupt the CPU, thus, it is connected to the CPU's interrupt pin.
$\overline{INTA}$	26	I	**Interrupt Acknowledge:** Signal used to enable the KS82C59A interrupt vector data onto the data bus by a sequence of interrupt acknowledge pulses issued by the CPU.
IR_{0-7}	18–25	I	**Interrupt Requests:** Asynchronous input signals. An interrupt request is executed by raising an IR input (LOW to HIGH), and holding it HIGH until it is acknowledged (Edge Triggered Mode), or just by a HIGH level on an IR input (Level Triggered Mode).
$\overline{RD}$	3	I	**Read:** Active LOW signal used to enable the KS82C59A to output status information onto the data bus for the CPU.
$\overline{SP}/\overline{EN}$	16	I/O	**Slave Program/Enable Buffer:** Active LOW, dual function control signal. When in the *Buffered Mode* its can be used as an output to control buffer transceivers ($\overline{EN}$). When not in the buffered mode it is used as an input to designate a master (SP = 1) or a slave (SP = 0).
V_{CC}	28	—	**Power:** 5V ± 10% DC Supply.
V_{SS}	14	—	**Ground:** 0V.
$\overline{WR}$	2	I	**Write:** Active LOW signal used to enable the KS82C59A to accept command words from the CPU.

FUNCTIONAL DESCRIPTION

The KS82C59A Programmable Interrupt Controller is designed for use in interrupt-driven micro-computer systems. Acting as an overall peripherals manager, its functions include:

- Accepting interrupt requests from assorted peripheral devices
- Determining which is the highest priority
- Establishing whether or not the new interrupt is of a higher priority than any interrupt which might be currently being serviced, and if so,
- Issuing an interrupt to the CPU
- Then providing the CPU with the *interrupt service routine* address of the interrupting peripheral

Each peripheral device usually has a specific interrupt service routine which is particular to its operational or functional requirements within the system. The KS82C59A can be programmed to hold a pointer to the service routine addresses associated with each of the peripheral devices under its control. Thus when a peripheral interrupt is passed through to the CPU, the KS82C59A can set the CPU Program Counter to the interrupt service routine required. These *pointers* (or vectors) are addresses in a vector table.

The KS82C59A is intended to run in one of two major operational modes, according to the type of CPU being used in the system. The *CALL Mode* is used for 8085 type microprocessor systems, while the *VECTOR Mode* is reserved for those systems using more sophisticated processors such as the 8088/86, 80286/386 or 68000 family.

In either mode, the KS82C59A can manage up to eight interrupt request levels individually, with a maximum capability of up to 64 interrupt request levels when cascaded with other KS82C59As. A selection of priority modes is also available such that interrupt requests can be processed in a number of different ways to meet the requirements of a varity of system configurations.

Priority modes can be changed or reconfigured dynamically at any time during system operation using the operation command words (OCWs), allowing the overall interrupt structure to be defined for a complete system. Note that the KS82C59A is programmed by the system software *as an I/O peripheral.*

The major functional components of the KS82C59A are laid out in the block diagram of Figure 1. Vector data and device programming information are transferred from the system bus to the KS82C59A via the 3-state, bi-directional Data Bus Buffer which is connected to the internal bus of the controller. Control data between the KS82C59A and the CPU, and between master and slave KS82C59A devices, is managed by one of three functional blocks:

- The Read/Write Control block processes CPU-initiated reads and writes to the KS82C59A registers
- The Control Logic block receives and generates the signals that control the sequence of events during an interrupt
- The Cascade Control block is used to operate a private bus (CAS_0-CAS_2) connecting a master and up to 8 slave KS82C59As.

Programming data passed over the system bus is saved in the initialization and Command Word Registers. Note that the contents of these registers cannot be read back by the CPU.

Peripheral interrupt requests (IR_0-IR_7) are handled by the functional blocks comprising the Interrupt Request Register (IRR), the Interrupt Mask Register (IMR), the In-Service Register (ISR) and the Priority Decision Logic block. Interrupt requests are received at the IRR, the IMR masks those interrupts which cannot be accepted by the KS82C59A, and the ISR shows those interrupt priority levels which are being serviced. These three registers can all be read by the CPU under software control. The Priority Decision Logic block determines which interrupt will be processed next according to a variety of indicators which include the current priority, mode status, current interrupt mask and interrupt service status.

The actual operation of the KS82C59A and its many modes are described in the section following device specifications and characteristics.

OPERATIONAL DESCRIPTION

The KS82C59A is designed to operate in one of two mutually exclusive modes, selected according to the type of system processor used: **Call Mode** for 8080/85 type processors, and **Vector Mode** for 8088/86 and 80286/386 type processors. The major difference between

3

these two modes is the way in which interrupt service routine address data is passed to the system CPU. Unless specifically programmed to the contrary, the KS82C59A defaults to the CALL Mode of operation, (see section on Programming).

Call Mode

In CALL mode, the *interrupt service routine address* is passed in two steps, in response to three Interrupt Acknowledge (INTA) signals sent by the CPU to the KS82C59A. In a system containing a single Interrupt Controller, the sequence of steps to respond to a peripheral interrupt request is outlined below, and shown graphically in Figure 4. The itnerrupt service routine addresses are loaded into the KS82C59A during the initialization procedures.

Step	Event Sequence
1	One or more interrupt request lines (IR_0-IR_7) are raised HIGH, setting corresponding IRR bits.
2	The requests are evaluated by the KS82C59A, and if their priority is high enough, and if they are not masked, the INT signal is sent to the CPU.
3	The CPU acknowledges the INT with an interrupt acknowledge (INTA).
4	On receipt of the first INTA, the KS82C59A sets the highest priority ISR bit, and resets the corresponding IRR bit. In addition, the KS82C59A sends a CALL instruction 0CDH) to the CPU via the data bus.
5	The CALL instruction causes the CPU to send two more INTA signals to the KS82C59A.
6	On receipt of the second INTA signal, the KS82C59A sends the low order 8-bit address byte to the CPU via the data bus. On receipt of the third INTA, the high order address byte is sent to the CPU.
7	This completes the 3-byte CALL instruction procedure. The ISR bit is reset at the end of the interrupt sequence by EOI command, except in the Automatic EOI mode, where the ISR bit is reset automatically at the end of the third INTA.

Vector Mode

In VECTOR mode, the interrupt service routine address is calculated by the CPU from a one byte *interrupt vector* supplied by the KS82C59A. The significant bits T_{7-3} of the interrupt vectors are loaded into the KS82C59A during the initialization procedures.

Note that no data is transferred by the KS82C59A to the CPU at the first INTA signal (the KS82C59A data bus buffers are disabled). It is similar to the CALL mode in that this cycle is used for internal operations that freeze the state of the interrupts for priority resolution and leaves the data bus buffers disabled or, in cascaded mode: to issue the interrupt code on the cascade lines (CAS_{0-2}).

The sequence of steps that occur to respond to a peripheral interrupt request in Vector mode are outlined below and illustrated in Figure 7.

Step	Event Sequence
1	One or more interrupt request lines (IR_0-IR_7) are raised HIGH, setting corresponding IRR bits.
2	The requests are evaluated by the KS82C59A, and if their priority is high enough, and if they are not masked, an INT signal is sent to the CPU.
3	The CPU acknowledges the INT with an interrupt acknowledge (INTA).
4	Upon receipt of the first INTA signal from the CPU, the KS82C59A sets the highest priority ISR bit and resets the corresponding IRR bit. The KS82C59A data bus buffer is *not* active during this cycle (high impedance state).
5	Upon receipt of the second INTA signal generated by the CPU, the KS82C59A sends an 8-bit *interrupt vector* to the CPU via the data bus.
6	This completes the 1-byte VECTOR mode procedure. In the Automatic End-of-Interrupt (AEOI) mode, the ISR bit is reset at the end of the second INTA. In EOI mode, the ISR bit remains set until an appropriate EOI command is received at the end of the interrupt sequence.

The interrupt sequence procedures, when several KS82C59As are cascaded together, is shown for both CALL and VECTOR modes in Figures 5 and 8, respectively.

Figure 4: CALL Mode Operation (Single KS82C59A Systems)

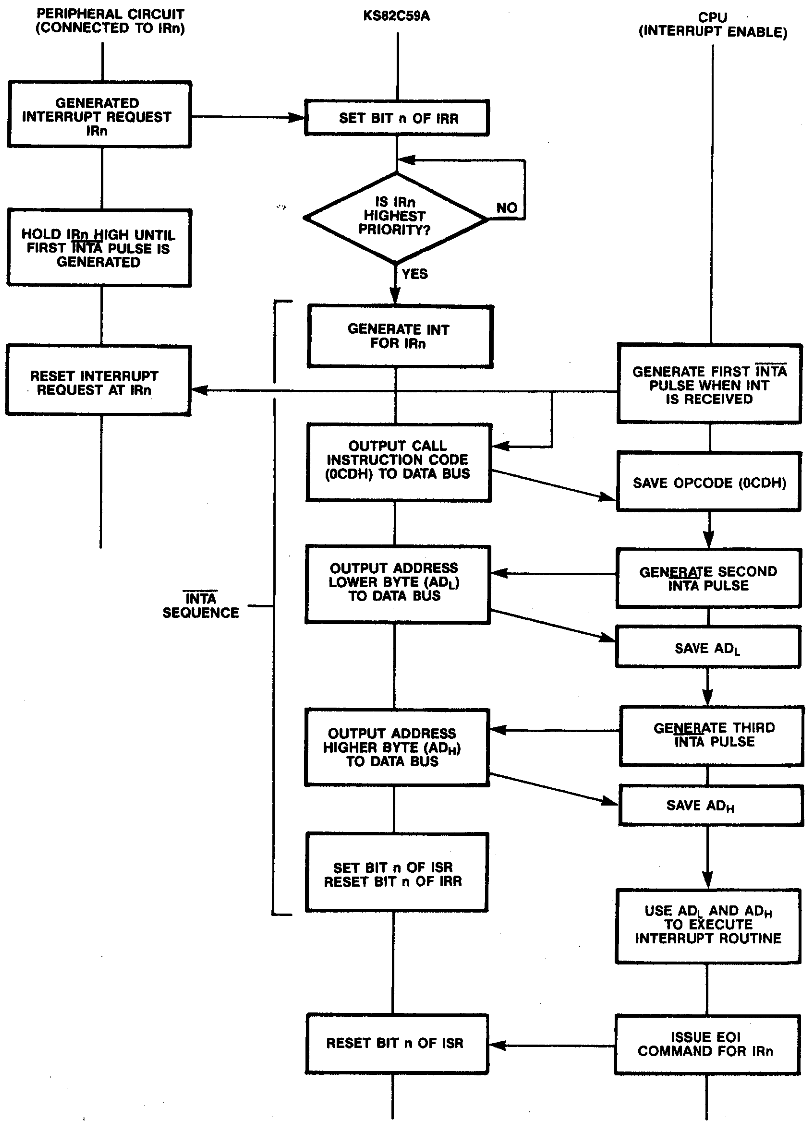


Figure 5: CALL Mode Operation (Cascaded KS82C59A Systems)

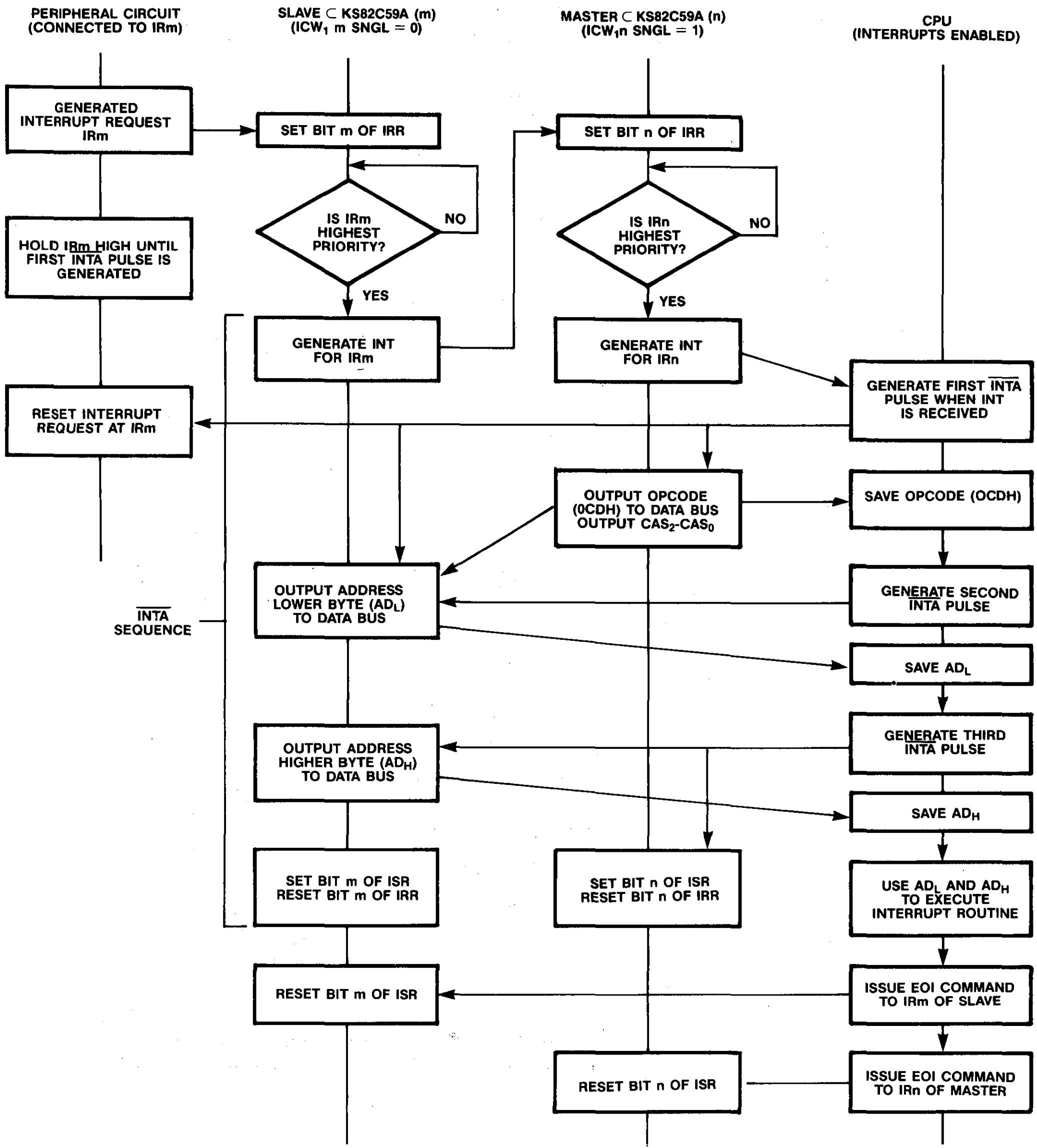


Figure 6: CALL Mode Address Byte Sequence

CONTENTS OF FIRST INTERRUPT VECTOR BYTE

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CALL CODE	1	1	0	0	1	1	0	1

The lower address of the appropriate service routine is enabled onto the data bus during the second INTA pulse.

When the *Interval = 4*, bits A_5-A_7 are programmed, and A_0-A_4 are inserted automatically by the KS82C59A.

When the *Interval = 8*, bits A_6 and A_7 only are programmed, with A_0-A_5 inserted automatically by the KS82C59A.

3

CONTENTS OF SECOND INTERRUPT VECTOR BYTE

IR	INTERVAL = 4							
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
7	A_7	A_6	A_5	1	1	1	0	0
6	A_7	A_6	A_5	1	1	0	0	0
5	A_7	A_6	A_5	1	0	1	0	0
4	A_7	A_6	A_5	1	0	0	0	0
3	A_7	A_6	A_5	0	1	1	0	0
2	A_7	A_6	A_5	0	1	0	0	0
1	A_7	A_6	A_5	0	0	1	0	0
0	A_7	A_6	A_5	0	0	0	0	0

IR	INTERVAL = 8							
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
7	A_7	A_6	1	1	1	0	0	0
6	A_7	A_6	1	1	0	0	0	0
5	A_7	A_6	1	0	1	0	0	0
4	A_7	A_6	1	0	0	0	0	0
3	A_7	A_6	0	1	1	0	0	0
2	A_7	A_6	0	1	0	0	0	0
1	A_7	A_6	0	0	1	0	0	0
0	A_7	A_6	0	0	0	0	0	0

During the third INTA pulse, the higher address of the appropriate service routine is enabled onto the bus. This address was initially programmed as byte 2 of the initialization sequence (A_8-A_{15}).

CONTENTS OF THIRD INTERRUPT VECTOR BYTE

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8

Figure 7: Vector Mode Operation (Single KS82C59A Systems)

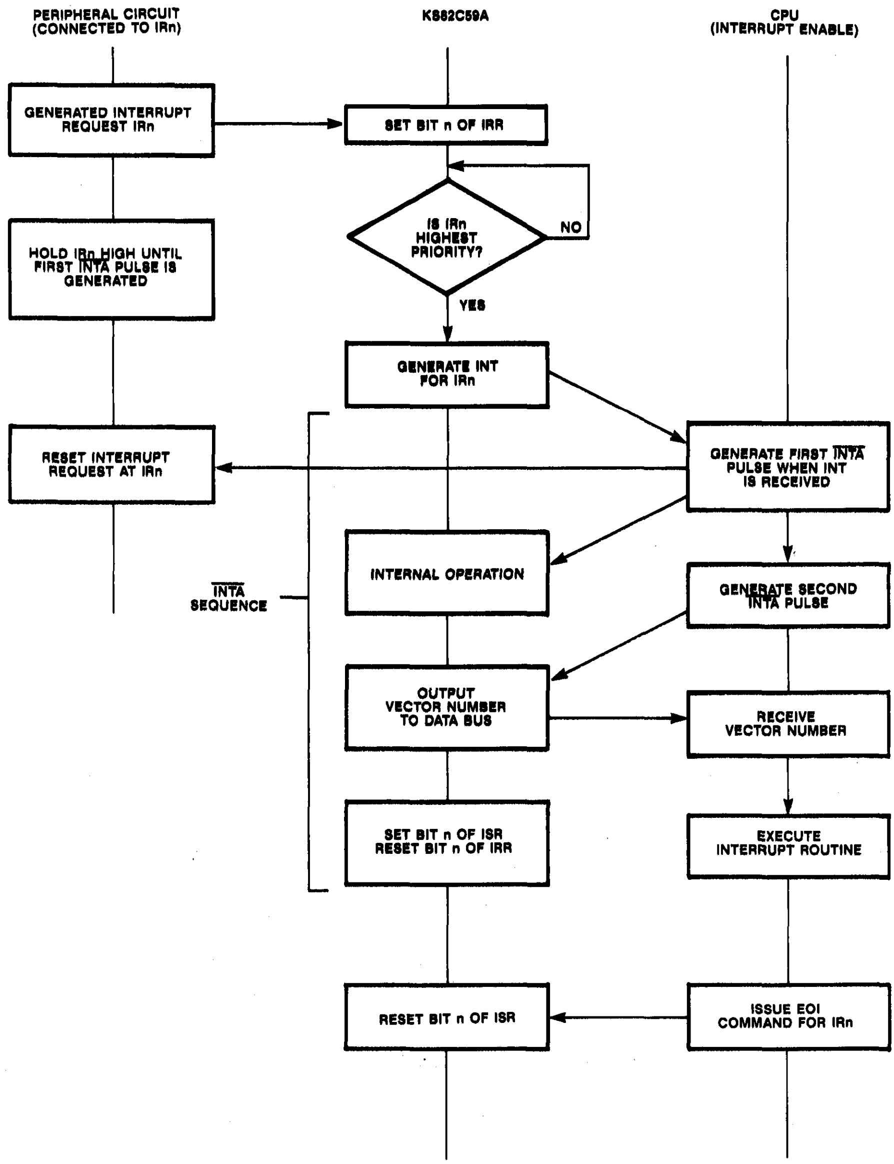
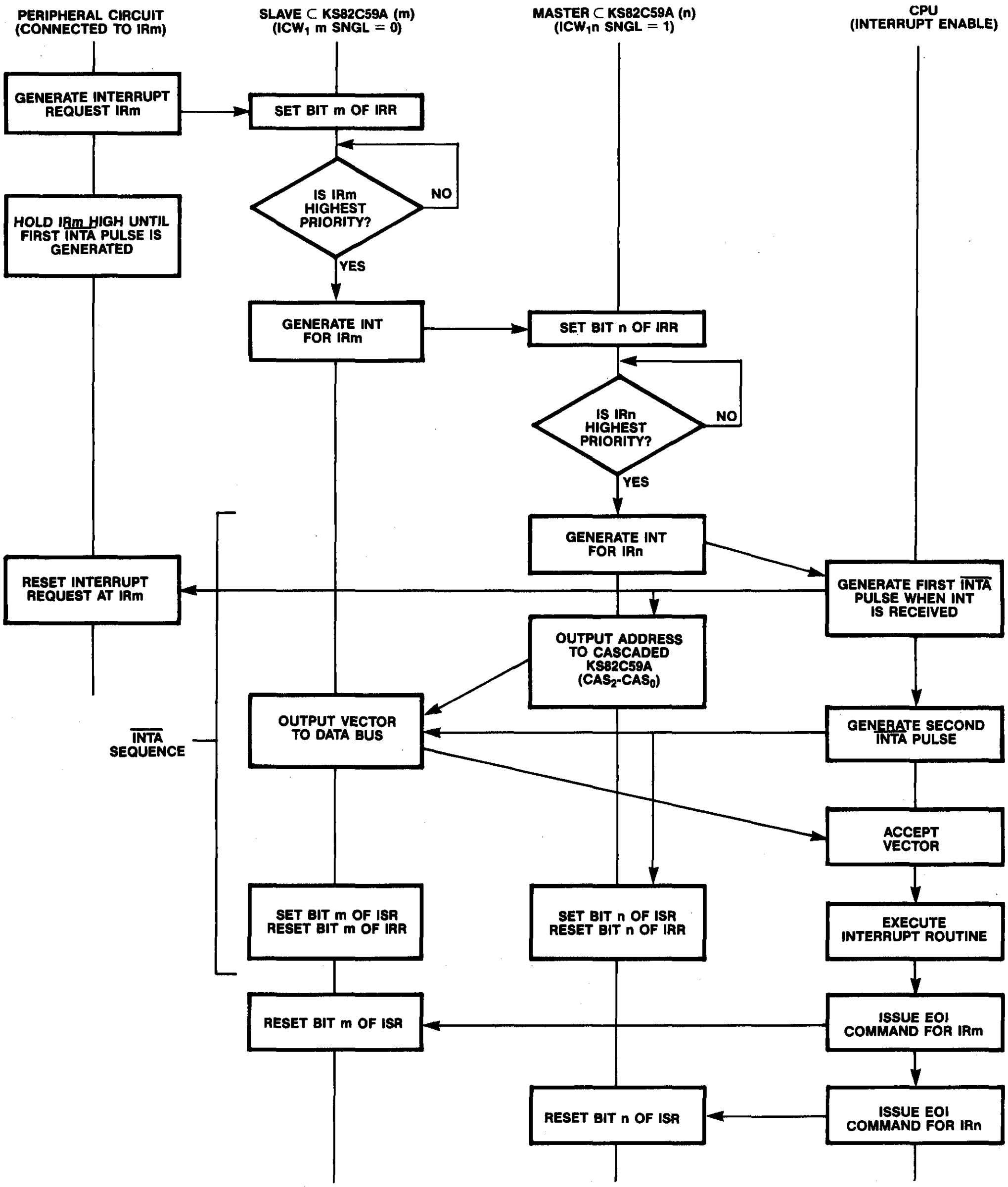


Figure 8: Vector Mode Operation (Cascaded KS82C59A Systems)



3

Figure 9: Vector Mode Address Byte

CONTENTS OF FIRST INTERRUPT VECTOR BYTE 8086, 8088, 80286 MODE

IR	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
7	T_7	T_6	T_5	T_4	T_3	1	1	1
6	T_7	T_6	T_5	T_4	T_3	1	1	0
5	T_7	T_6	T_5	T_4	T_3	1	0	1
4	T_7	T_6	T_5	T_4	T_3	1	0	0
3	T_7	T_6	T_5	T_4	T_3	0	1	1
2	T_7	T_6	T_5	T_4	T_3	0	1	0
1	T_7	T_6	T_5	T_4	T_3	0	0	1
0	T_7	T_6	T_5	T_4	T_3	0	0	0

The value T_7 to T_3 is programmed during byte 2 of the initialization (ICW_2). During the second INTA pulse, the interrupt vector of the appropriate service routine is enabled onto the bus. The low order three bits are supplied by the KS82C59A according to the IR input causing the interrupt.

REGISTERS

The KS82C59A contains a number of registers, used to keep track of interrupts which are being serviced, or pending, as well as those which are masked. These registers are described in Table 7. They can be written to using the *command word* structure, or in the case of IRR, are set by external peripheral devices requesting interrupt service. The contents of all registers can be read by the CPU for status updates (see Table 9).

Table 7: KS82C59A Registers

Symbol	Name	Function
IMR	Interrupt Mask Register	An 8-bit wide register that contains the interrupt request lines which are masked.
IRR	Interrupt Request Register	An 8-bit wide register that contains the levels requesting an interrupt to be acknowledged. The highest request level is reset from the IRR when an interrupt is acknowledged, (not affected by IMR).
ISR	In-Service Register	An 8-bit wide register that contains the priority levels which are being serviced. The ISR is updated when an *End of Interrupt* Command (EOI) is received.

Table 8: Register Read/Write Operations

Operations			Bit Programming			
KS82C59A	**CPU**	**Other Conditions**	$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_0
IRR to Data Bus ISR to Data Bus	IRR Read ISR Read	IRR set by OCW_3 ISR set by OCW_3	0	0	1	0
Polling data to Data Bus	Polling	Polling data is read instead of IRR and ISR				
IMR to Data Bus	IMR Read		0	0	1	1
Data Bus to ICW_1 Reg. Data Bus to OCW_2 Reg. Data Bus to OCW_3 Reg.	ICW_1 Write OCW_2 Write OCW_3 Write	Set ICW_1 (D_4 = 1) Set OCW_2 (D_4, D_3 = 0) Set OCW_3 (D_4 = 0, D_3 = 1)	0	1	0	0
Data Bus to ICW_2 Reg. Data Bus to ICW_3 Reg. Data Bus to ICW_4 Reg.	ICW_2 Write ICW_3 Write ICW_4 Write	Refer to section on Control Words for ICW_2-ICW_4 writing procedure	0	1	0	1
Data Bus to IMR	OCW_1 Write	After initialization				
Data Bus set to High Impedance State			0 1	1 X	1 X	X X
Illegal State			0	0	0	X

PROGRAMMING COMMANDS

The KS82C59A is initialized and programmed with special command words issued by the CPU. These commands fall into two major categories: *Initialization Command Words* (ICW_1-ICW_4), and *Operational Command Words* (OCW_1-OCW_3). Initialization commands are used to bring the KS82C59A to a known state when the system is first activated, or after a system restart.

Operational commands are used once the KS82C59A is in operation (and *after* it has been initialized), to set, or alter specific interrupt program modes. The format and use of these two command types is described below.

INITIALIZATION COMMANDS

The KS82C59A is initialized by a sequence of 2 to 4 command words (ICWs), where the actual number of commands sent depends on the system configuration, and the initial operating modes to be programmed. Note that *each* KS82C59A in the system *must* be initialized before operations begin in earnest (Figure 11).

The initialization sequence is started when the CPU sends A_0 = 0 and ICW_1 with D_4 = 1 (Figure 10). During initialization, the events below occur automatically:

- Edge sense circuit is reset. Thus, after initialization, an interrupt request must make a LOW-to-HIGH transition to be recognized.
- IMR is cleared (Interrupts enabled).
- The priority of IR_7 is set to 7 (the lowest priority).
- Special Mask Mode is reset.
- Status read is set to IRR.
- If SNGL bit of ICW_1 = 1, then no ICW_3 will be issued.
- If IC_4 bit of ICW_1 = 0, then functions selected in ICW_4 are reset: Non-buffered Mode, no Automatic EOI, Call Mode operation.
- If IC_4 = 1, then KS82C59A will expect ICW_4.

Bit Definitions (ICW_1, ICW_2)

- IC_4 — Set if ICW_4 is to be issued. This bit *must* be set for systems operating in Vector Mode.
- SNGL — Set if this KS82C59A is not cascaded to other KS82C59As in the system (ICW_3 not issued). When KS82C59As are cascaded, SNGL is reset and ICW_3 is issued.
- ADI — CALL Address Interval. If ADI = 1, then interval = 4. If ADI = 0, then interval = 8.
- LTIM — Level Trigger Mode. If LTIM = 1, edge detect logic on the IR inputs is disabled, and the KS82C59A operates in level triggered mode.
- A_{5-15} — Service routine *Page Starting Address* (Call Mode). In a single KS82C59A system, the 8 interrupt request levels generate CALLs to 8 equally spaced locations in memory. These are spaced at intervals of either 4 or 8 memory locations according to the ADI value. Thus, the vector tables associated with each KS82C59A in the system occupy pages of 32 or 64 byte, respectively.

  Bits A_0-A_4 are automatically inserted to give an address length of 2 bytes (A_0-A_{15}).

  Note that the 8-byte interval is compatible with KS80C85B restart instructions.
- A_{11-15} — Service routine *Vector Address Byte*. In the vector mode, bits A_{11}-A_{15} are inserted in the five most significant places of the vector byte. The three least significant bits are inserted by the KS82C59A according to the interrupt request level. The ADI (Address Interval) and A_5-A_{10} bits are ignored.

Bit Definitions (ICW_3)

This word is read only when SNGL = 0 in ICW_1 (cascading is used).

- **Master Mode:** Sent to the master KS82C59A, each bit of ICW_3 represents a potential slave device connected to an IR input. If a slave exists, the corresponding bit in ICW_3 is set. Where a slave is not attached to an IR input of the master, the corresponding bit is reset.

  In operation, the master outputs byte 1 of the interrupt sequence to the bus, then enables the appropriate slave (via the cascade bus CAS_{0-2}) to output bytes 2 and 3 (Call Mode) or byte 2 only (Vector Mode).
- **Slave Mode:** When sent to a slave KS82C59A, bits ID_{0-2} contain the slave address on the cascade bus. Each slave device in the system *must* be initialized with a unique address. Remaining bits are not used.

  In operation, the slave compares the cascade input to its 3-bit address and if they match, outputs byte 2 and 3 (Call Mode), or byte 2 only (Vector Mode) to the bus.

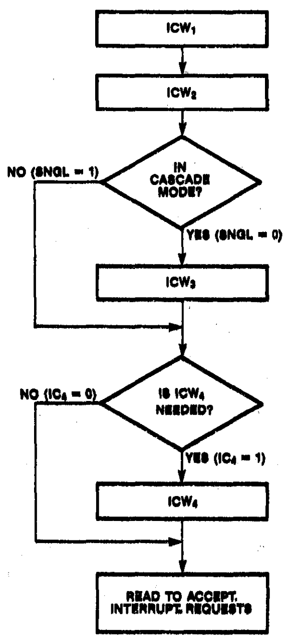
Bit Definitions (ICW_4)

This word is used only when bit IC_4 in ICW_1 is set. Note that only five bits are used.

3

- μPM Microprocessor System Mode: μPM = 0 for Call Mode, μPM = 1 for Vector Mode.
- AEOI This bit is set if the *Automatic End of Interrupt Mode* is to be programmed.
- M/S When the Buffered Mode is selected, the M/$\overline{S}$ bit is used to determine the master/slave programming. That is: M/$\overline{S}$ = 1 indicates the device is a master, while M/$\overline{S}$ = 0 indicates a slave. If the BUF bit is not set, M/$\overline{S}$ is not used.
- BUF The Buffered Mode is programmed by setting BUF = 1. In buffered mode, the output pin $\overline{SP}/\overline{EN}$ becomes an enable output, and the M/S bit determines whether the device is a master or a slave.
- SFNM Special Fully Nested Mode is programmed by setting SFNM = 1.

Figure 10: Initialization Flow Chart



OPERATIONAL COMMANDS

Once the KS82C59A has been initialized, it can accept and process interrupt requests received on its IR input lines. Interrupts are processed according to the modes programmed during the initialization process. A number of commands, sent to the KS82C59A from the CPU, allow the programmed modes or the interrupt request priorities to be changed *on the fly* during operation. These commands are described below (and Figure 12):

Bit Definitions (OCW_1)

OCW_1 is used to set and clear mask bits in the IMR, thus enabling or disabling specific IR inputs. In the *Special Mask Mode*, the ISR is also masked.

- M_{0-7} Bits M_{0-7} correspond to the 8 IR inputs. If bit M_n = 1, the IR_n input is disabled. If M_n = 0, the IR_n input is enabled.

Bit Definitions (OCW_2)

OCW_2 is used to program the different End of Interrupt (EOI) Modes, and alter the interrupt request priorities.

- L_{0-2} These bits determine the interrupt level to be acted upon when bit SL = 1 (active).
- EOI The End of Interrupt command is issued by the CPU, rather than by the KS82C59A (in automatic EOI mode). Note that this bit is used in conjunction with bits R and SL to control the interrupt priority assignments and rotations.
- SL Set Interrupt Level bit. This lowest priority interrupt is assigned to the IR input corresponding to the octal value of L_{0-2}.
- R This bit determines if interrupt priority rotation is in effect. R = 1 indicates priorities will be rotated, perhaps combined with other modes.

Bit Definitions (OCW_3)

OCW_3 is used to program the Special Mask Mode, the Polling Mode, and select internal registers to be read by the CPU.

- RIS If RIS = 1, select ISR. IF RIS = 0, select IRR.
- RR Read Register bit. If RR = 1, output the contents of the register selected by bit RIS onto the bus. The register selection is retained, so OCW_3 does not have to be reissued in order to read the same register again.

- P If P = 1, the Polling Mode is selected for this KS82C59A. In this mode the CPU will poll for new interrupt requests, rather than having the KS82C59A actively set the CPU *INT* input.
- SMM If *Special Mask Mode* is enabled (ESMM = 1), then SMM = 1 programs the special mask mode, and SMM = 0 clears the special mask mode.
- ESMM If ESMM = 1, then the special mask mode is enabled, and can be set or reset by the SMM bit. If ESMM = 0, the special mask mode is disabled and SMM is ignored.

OPERATIONAL MODES

The KS82C59A can be programmed to operate in a number of different modes which are summarized and described below. Depending on the mode, some are set during initialization, and some during operation.

Mode	Location Set	
Buffer Mode	BUF, M/S	(ICW_4)
Cascaded Mode	SNGL	(ICW_1)
• Master Mode	S_{0-7}	(ICW_3)
• Slave Mode	ID_{0-2}	(ICW_3)
End of Interrupt (EOI) Modes	EOI	(OCW_2)
• Automatic EOI Mode	AEOI	(ICW_4)
• Non-specific EOI	EOI, SL, R	(OCW_2)
• Specific EOI	EOI, SL, R	(OCW_2)
Nested Modes		
• Fully Nested Mode	default mode	
• Special Fully Nested Mode	SFNM	(ICW_4)
	AEOI	(ICW_4)
Polling Mode	P	(OCW_3)
Rotation Modes		
• Automatic Rotation Mode	R, SL, EOI	(OCW_2)
• Specific Rotation Mode	R, SL, L_{0-2}	(OCW_2)
Special Mask Mode	ESMM, SMM	(OCW_3)
System Modes		
• CALL Mode	μPM	(ICW_4)
• VECTOR Mode	μPM	(ICW_4)
	IC_4	(ICW_1)
Trigger Modes		
• Edge Triggered Mode	LTIM	(ICW_1)
• Level Triggered Mode	LTIM	(ICW_1)

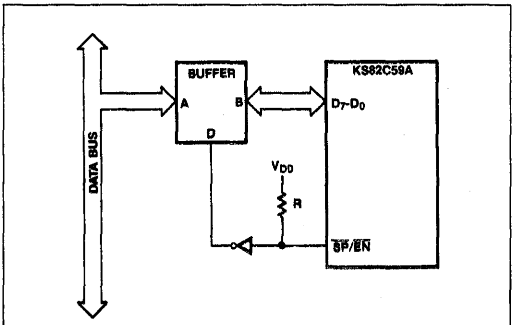
Buffer Mode

In larger systems the KS82C59A may be required to drive the data bus through a buffer. To handle this situation, the *Buffer Mode* is programmed during initialization (using the BUF and M/S bits in ICW_4).

When in buffer mode, $\overline{SP}/\overline{EN}$ is used to enable the data bus buffers, and determine the direction of data flow through the buffer (Figure 13). This signal is active when the output ports of the KS82C59A are activated.

Note that when *cascaded* KS82C59As are required to be used in the buffer mode, the master/slave selection is done using the M/S bit of ICW_4, (and SNGL bit of ICW_1 is set to 1). M/S is set to 1 for the master mode and 0 for the slave mode.

Figure 13: Buffer Mode

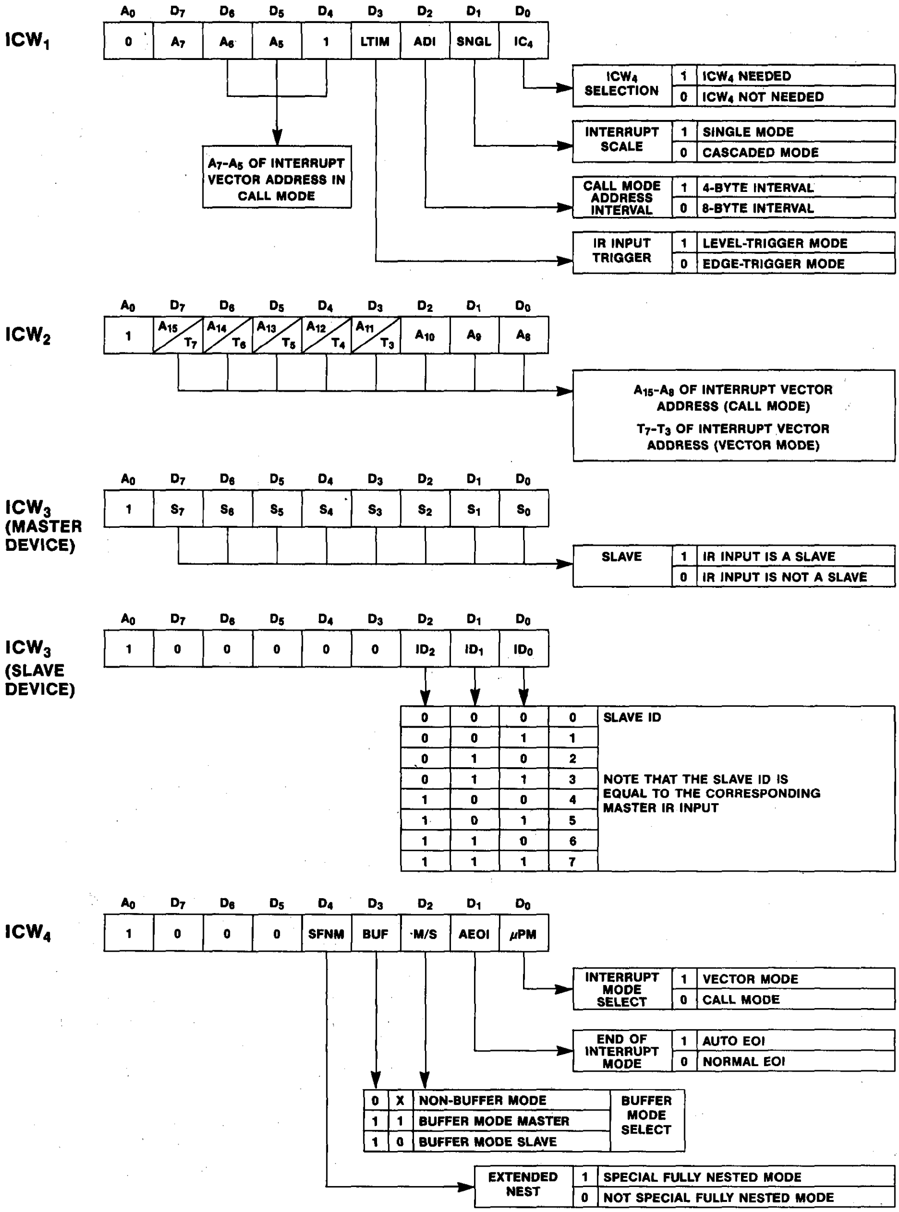


Notes:
1. D determines the data direction
   Low Level: A → B; High Level: B → A
2. The KS82C59A is set to input $\overline{SP}/\overline{EN}$ in its initial state, and is pulled up by R to set D to the low level during initialization.

Cascaded Mode

In systems that contain more than 8 priority interrupt levels, several KS82C59A devices can be easily cascaded together to handle a maximum of 64 interrupt levels. In a cascaded configuration, one KS82C59A serves as a *master*, controlling up to 8 *slaves* (able to handle 8 interrupts each). The master selects the slaves via the cascade local bus (CAS_{0-2}), enabling the corresponding slave to output the interrupt service routine address (or vector) following each of the second and third $\overline{INTA}$ signals (second $\overline{INTA}$ signal only in Vector mode). At the end of the interrupt cycle, the EOI command must be issued *twice*, one for the master, and one for the appropriate slave.

Figure 11. Initialization Command Word Format



3

Figure 12. Operation Command Word Format

OCW_1

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	M7	M6	M5	M4	M3	M2	M1	M0

INTERRUPT MASK		
	1	SET (DISABLED) MASK
	0	RESET (DISABLE) MASK

OCW_2

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	R	SL	EOI	0	0	L_2	L_1	L_0

L_2	L_1	L_0		INTERRUPT REQUEST (IR) LEVEL TO BE ACTED UPON
0	0	0	0	
0	0	1	1	
0	1	0	2	
0	1	1	3	
1	0	0	4	
1	0	1	5	
1	1	0	6	
1	1	1	7	

PRIORITY ROTATION AND EOI COMMAND	R	SL	EOI				
	0	0	1	EOI COMMAND	NO LEVEL DESIGNATION	NO ROTATION	NORMAL EOI COMMAND
	1	0	1			ROTATION	ROTATE ON NORMAL EOI COMMAND
	*0	1	1		WITH LEVEL DESIGNATION	NO ROTATION	SPECIFIC EOI COMMAND
	*1	1	1			ROTATION	ROTATE ON SPECIFIC EOI COMMAND
	0	1	0	NON-EOI COMMAND		NO ROTATION	NO OPERATION
	*1	1	0			ROTATION	SET PRIORITY COMMAND
*L_2-L_0 ARE USED	0	0	0		NO LEVEL DESIGNATION	NO ROTATION	ROTATE IN AUTOMATIC EOI MODE (CLEAR)
	1	0	0			ROTATION	ROTATE IN AUTOMATIC EOI MODE (SET)

OCW_3

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	ESMM	SMM	0	1	P	RR	RIS

RR	RIS		READ REGISTER COMMAND
0	X	NO OPERATION	
1	1	READ IS-REG ON NEXT $\overline{RD}$	
1	0	READ IR-REG ON NEXT $\overline{RD}$	

POLLING		
	1	POLLING COMMAND
	0	NO POLLING

ESMM	SMM		SPECIAL MASK MODE
0	X	NO OPERATION	
1	1	SET SPECIAL MASK	
1	0	RESET SPECIAL MASK	

The CAS_{0-2} bus lines are normally held in a LOW state, and activated only for slave inputs (non-slave inputs to the master do not affect the cascade bus). The slave address will be held on the cascade bus from the trailing edge of the first $\overline{INTA}$ signal to the trailing edge of the last $\overline{INTA}$ signal (either second or third depending on the system mode).

Within the system, each slave can be programmed to operate in a different mode (except AEOI), independently of other slave devices. The interrupt output (INT) of each slave is tied to one of the interrupt request lines (IR_{0-7}) of the master device. Unused IR pins on the master device can be connected to other peripheral devices (as in the single standalone mode of operation), or left unconnected.

Note that an address decoder is required to activate the chip select ($\overline{CS}$) input of each KS82C59A in the system.

Master Mode

A KS82C59A operating in the *Master Mode* can be controlling both peripheral interrupts as well as other KS82C59A slave devices. Since both types of interrupts are connected to the IR_{0-7} pins, it is necessary to differentiate between the two. This is accomplished in the initialization control word (ICW_3) sent out to the master. ICW_3 sets the S_n bits corresponding to IR_n pins connected to slaves equal to one (1), while S_m bits corresponding to IR_m pins connected to peripheral inputs are reset to zero (0).

Peripheral interrupt requests to IR_m pins (S_m = 0) are handled by the master as if it were operating singly. That is, the CAS line remain LOW, and the master provides the interrupt or vector as required.

Slave interrupt requests to IR_n pins (S_n = 1) are handled as follows: the master sends an interrupt to the CPU if the slave requesting the interrupt has priority. If so, the master outputs the slave address *n* to the CAS bus on the first $\overline{INTA}$ signal, then lets the slave complete the remainder of the interrupt cycle. Note that two EOI commands are required to terminate the sequence, one each for the master and slave.

Slave Mode

When a slave KS82C59A receives a peripheral interrupt request, and it has no higher interrupt requests pending, the slave sends an interrupt request to the master via its INT output. This interrupt request is passed by the master to the CPU, which then initiates the interrupt cycle, in turn causing the master to output the slave's address on the CAS bus. Each slave in the system continuously monitors the CAS bus, comparing the addresses thereon until a match is found with its own address. When the slave initiating the interrupt request finds an address match, it completes the interrupt sequence as though it were a single KS82C59A.

Note: Since the master holds the CAS bus LOW (corresponding to CAS address 0) when processing peripheral interrupt requests, address 0 should not be used as a slave address unless the system contains the full complement of 8 slaves.

End of Interrupt (EOI) Modes

The *EOI Modes* are used to terminate teh *request* for *interrupt service* sequence, update the ISR register and alter the interrupt priorities. The EOI mode selected depends on the *nesting mode* currently programmed. The options are discussed below:

Automatic EOI (AEOI) Mode

In *AEOI Mode*, the ISR bit corresponding to the interrupt is set and reset automatically during the final $\overline{INTA}$ signal. This means that the CPU does not have to issue an EOI command at the end of the interrupt routine.

Caution is urged in using AEOI however, as the ISR does not save the *routine currently in service* in this mode. Thus, unless the interrupts are disabled by the interrupt service routine, a stack overflow situation can result from newly generated interrupts (which bypass the priority structure), or from level triggered interrupts.

The Automatic EOI mode is programmed by setting the AEOI bit in ICW_4.

Non-specific (Normal) EOI Mode

When the KS82C59A is operated in the *Fully Nested Mode*, it can easily determine which ISR bit is to be reset at the conclusion of an interrupt sequence. In this case, the non-specific EOI command is used to reset the highest priority level selected from the interrupts in service, (the valid assumption is made that the last interrupt level acknowledged and serviced necessarily corresponds to the highest priority ISR bit set).

A *Non-specific EOI Mode* is selected via OCW_2, where EOI = 1, SL = 0 and R = 0. Refer to Figure 14a, c.

Specific EOI Mode

The *Specific EOI Mode* is required when the fully nested (normal) mode is not used, and the KS82C59A is unable to determine the last interrupt level acknowledged (such as might be encountered if the *Special Mask Mode* is programmed). The Specific EOI command identifies the ISR bit (interrupt level) to be reset using bits L_{0-2} of OCW_2, which also has the following bit settings: EOI = 1, SL = 1 and R = 0. Refer to Figure 14b, d.

Figure 14: EOI Commands

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
OCW_2	0	0	1	0	0	X	X	X

a) Non-specific EOI Command

OCW_2	0	1	1	0	0	L_2	L_1	L_0

b) Specific EOI Command

OCW_2	1	0	1	0	0	X	X	X

c) Rotate on Non-specific EOI Command

OCW_2	1	1	1	0	0	L_2	L_1	L_0

d) Rotate on Specific Command

Mask Modes

The *Mask Modes* are used to selectively enable or disable interrupt requests. This is distinct from the automatic disabling of an interrupt which is in effect while a request from the same interrupt is being serviced.

Normal Mask Mode

Interrupt request lines IR_{0-7} can be individually masked in the Interrupt Mask Register (IMR), using OCW_1. Each bit in IMR masks one interrupt request line if it is set, with no effect on the other interrupt request lines. Bit 0 masks IR_0, bit 1 masks IR_1 etc.

Special Mask Mode

The *Special Mask Mode* is used to dynamically alter the interrupt priority structure under software control during program execution. In this mode, when a mask bit is set in OCW_1, it disables further interrupts at that level, and enables interrupts from all other levels that are not masked. This includes those interrupts which are lower (as well as higher) in priority.

The *Special Mask Mode* is set by ESMM = 1 and SMM = 1 in OCW_3. To clear this mode, the CPU must issue another OCW_3 with ESMM = 1 and SMM = 0. Setting ESMM = 0 alone has no effect. To correctly enter the *Special Mask Mode*, use the following procedure:

1. CPU reads the ISR
2. CPU writes the ISR data from (1) to the IMR (OCW_1)
3. CPU selects *Special Mask Mode* by issuing OCW_3 with ESMM = 1 and SMM = 1.

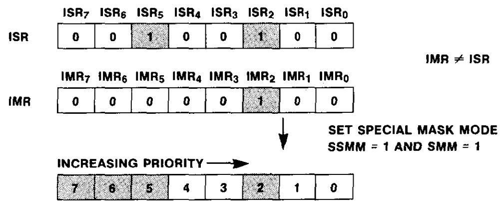
This procedure ensures that all interrupt requests not currently in service will be enabled.

Note that if IMR is not set equal to ISR when *Special Mask Mode* is selected, bits which may be set in the ISR will be ignored. If a corresponding bit is not set in IMR, that interrupt request may be serviced, causing all interrupts of lower priority to be effectively disabled. This is illustrated in Figure 15.

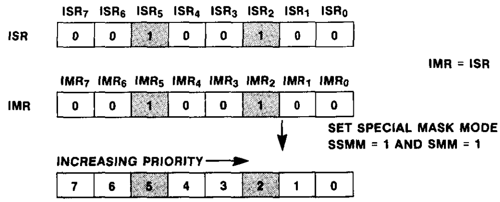
When the *Special Mask Mode* is selected, the *Specific EOI Mode* must be used to terminate the interrupt sequence, so the CPU can explicitly specify which ISR bit is to be reset.

3

Figure 15: Special Mask Mode



Interrupt request IR_6 and IR_7 cannot be accepted when IMR ≠ ISR, even with the Special Mask Mode set



All interrupt requests, except those being serviced can be accepted when IMR = ISR, and the Special Mask Mode is set

Priority Levels That Can Interrupt (White Boxes)

Nested Modes

The nesting modes are used to determine, and change, the priority of incoming interrupt requests.

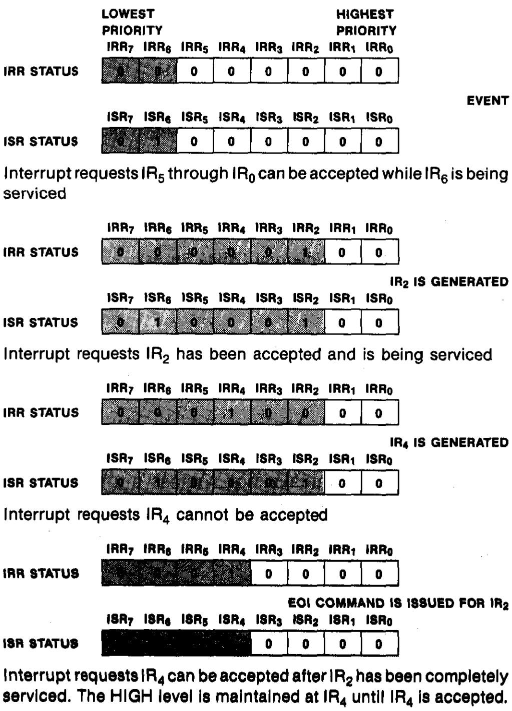
Fully Nested Mode

This is the default nesting mode which is entered automatically after initialization, unless another mode has been programmed. In the *Fully Nested Mode*, the interrupt request priorities are set in descending order from 0 to 7. That is; IR_0 is the highest priority interrupt, IR_7 the lowest.

When an interrupt is acknowledged, the highest priority request is selected, the corresponding ISR bit is set, and the service routine address information is output to the data bus. The ISR bit is reset by the EOI command from the CPU, or automatically if *AEOI Mode* is programmed, at the completion of the interrupt sequence. While the ISR bit is set, all interrupt requests of equal or lower priority are inhibited. Interrupt requests of higher priority will generate an interrupt to the CPU, but whether or not these will be acknowledged depends on the system software. Interrupt priorities can be altered in this mode using one of the *Rotation Modes*.

Note that fully nested interrupt priorities are not necessarily preserved in those systems containing cascaded KS82C59As, as it is possible for interrupts of higher priority than the one being serviced to be ignored. This situation occurs when a slave accepts a peripheral interrupt request (and passes the request to the master). When the master accepts the request, it locks out further interrupts from that slave. Should an interrupt of higher priority come in to the same slave, it will not be recognized until the interrupt being serviced has completed processing. To preserve interrupt priorities in this situation, use the *Special Fully Nested Mode*.

Figure 16: Fully Nested Mode



Special Fully Nested Mode

This mode is very similar to the *Fully Nested Mode*, but is used in systems with cascaded KS82C59's, so as to preserve the interrupt priorities within each slave, as well as within the master. The *Special Fully Nested Mode* is programmed by setting the SFNM bit in the ICW_4 word in both the master and the slave during initialization. This allows interrupt requests of a higher level than the one being serviced to be accepted by the master from the same slave. That is, the slave is not locked out from the priority logic in the master, and higher priority interrupts within the slave will be recognized by the master, which will generate an interrupt to the CPU.

Caution should be exercised in this mode during the End Of Interrupt processing. It is essential that the system software check whether or not the interrupt just serviced was the *only* one from that slave. After the first non-specific EOI has been issued to the slave, the CPU should read the slave's ISR and check that no other bits are set (ISR = 0). Only if the slave ISR is zero, *can a non-specific EOI be sent to the master to complete the interrupt sequence*. If bits are set in the slave ISR, no EOI should be sent to the master.

Polling Mode

The *Polling Mode* is used to bypass the KS82C59A Interrupt control logic in favour of PCU software control over interrupt request processing. This allows systems to be built up with more than one master KS82C59A, and consequently, the sytem can contain more than 64 interrupt priority levels (since each master can handle 64 levels individually). In this case, the CPU polls each master looking for the highest priority interrupt request within the realm of each master.

In the *Polling Mode*, the INT outputs of the KS82C59A masters, and the INT input of the CPU are disabled. Interrupt service to individual peripheral devices is accomplished by system software using the *Poll Command* (Bit 'P' = 1 in OCW_3). When a poll command has been issued, the KS82C59A waits for the CPU to perform a register read. This read is treated by the KS82C59A as an interrupt acknowledge, and it sets the appropriate ISR bit and determines the priority level if there is an interrupt request pending. It then outputs the polling data byte onto the data bus (see Figure 17), including the binary code of the highest priority level requesting service. The CPU then processes the interrupt according to the polling data read, terminating the interrupt sequence with an EOI. Interrupt is frozen from WR to RD.

Figure 17: Poll Command

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
OCW_3	INT	0	0	0	0	W_2	W_1	W_0

Notes:
1. W_0-W_2 is binary code of highest priority level requesting service.
2. **INT** is equal to one (1) if there is an interrupt.

Rotation Modes

The different *Rotation Modes* allow the interrupt request priorities to be changed either automatically, or under software control. This is particularly useful for situations where there are a number of equal priority devices, or where a particular application may call for a specific priority change.

Automatic Rotation Mode

The *Automatic Rotation Mode* is recommended where there are a number of equal priority devices. In this mode the device is assigned the lowest priority immediately after it has had an interrupt request serviced. Its priority is subsequently increased as other devices have their interrupt requests serviced, and are then rotated to the bottom of the priority list. In the worst case, a device would have to wait for a maximum of seven other device interrupts of equal priority to be serviced *once*, before it was serviced. The effect of rotation on interrupt priority is illustrated in Figure 18.

Automatic Rotation can be activated in one of two ways, both using the command word OCW_2, and both combined with EOI modes:

- Rotation in Non-specific EOI Mode (R = 1, SL = 0 and EOI = 1)
- Rotation in Automatic EOI Mode (R = 1, SL = 0 and EOI = 0). This mode must be cleared by the CPU (accomplished by sending OCW_2 with: R = 0, SL = 0 and EOI = 1.

Specific Rotation Mode

The Specific Rotation Mode provides a mechanism to arbitrarily change interrupt priority assignments. This is accomplished by programming the lowest priority interrupt request line (specified by bits L_{0-2} in OCW_2), thereby fixing the other priorities. That is, if IR_4 is programmed as the lowest priority device, then IR_5 will have the highest priority.

Caution: because this change in priority levels is different from the normal *Fully Nested Mode*, it is *essential* that the user manage the interrupt nesting via the system software.

Specific rotation can be activated in one of two ways, both using the command word OCW_2:

- The *Set Priority* command is issued in OCW_2 with: R = 1, SL = 1 and L_{0-2} equal to the binary code of the lowest priority device.
- As part of the *Specific EOI Mode*, with OCW_2, (Rotate on Specific EOI command) values: R = 1, SL = 1, EOI = 1 and L_{0-2} equal to the binary priority level code of the lowest priority device. When the specific EOI is issued by the CPU, the KS82C59A resets the ISR bit designated by bits L_{0-2} in OCW_2, then rotates the priorities so that the interrupt just reset becomes the lowest priority.

Figure 18: Effect of Rotation

	ISR_7	ISR_6	ISR_5	ISR_4	ISR_3	ISR_2	ISR_1	ISR_0
ISR STATUS	0	1	0	1	0	0	0	0
PRIORITY STATUS	7 (LOWEST PRIORITY)	6	5	4	3	2	1	0 (HIGHEST PRIORITY)

BEFORE ROTATE: IR_4 is the highest priority requiring service

AFTER ROTATE: IR_4 was serviced, all other priorities have been rotated correspondingly

	ISR_7	ISR_6	ISR_5	ISR_4	ISR_3	ISR_2	ISR_1	ISR_0
ISR STATUS	0	1	0	0	0	0	0	0
PRIORITY STATUS	2	1	0 (HIGHEST PRIORITY)	7 (LOWEST PRIORITY)	6	5	4	3

Figure 18: Rotation Commands

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
OCW_2	1	0	0	0	0	X	X	X

a) Rotate in Automatic EOI Mode (Set)

OCW_2	0	0	0	0	0	X	X	X

b) Rotate in Automatic EOI Mode (Reset)

OCW_2	1	0	1	0	0	X	X	X

c) Rotate on Non-specific EOI Command

OCW_2	1	1	1	0	0	L_2	L_1	L_0

d) Rotate on Specific Command

OCW_2	1	1	0	0	0	L_2	L_1	L_0

e) Set Priority Command (Specific Rotation)

System Modes

The KS82C59A *must* operate in the system mode that corresponds to the processor type used in the system. *Call Mode* is used for 8085 type systems (and features an interrupt cycle controlled by three $\overline{INTA}$ signals), while *Vector Mode* is used for more sophisticated 8088/86 and 80286/386 type systems (and features an interrupt cycle controlled by only two $\overline{INTA}$ signals). These modes are described in more detail back in the Operational Description section.

Trigger Modes

In the KS82C59A, the interrupt request lines ($IR_{0\text{-}7}$) can be programmed for either edge or level triggering sensitivity, with the requirement that all IR lines must be in the same mode. That is, all edge triggered, or all level triggered. Figure 21 illustrates the priority cell diagram which shows a conceptual circuit of the level sensitive and edge sensitive input circuitry of the IR lines.

Note that to ensure a valid interrupt request is registered by the KS82C59A, it is essential that the IR input remain HIGH until after the first $\overline{INTA}$ has been received. In both modes, if the IR input goes LOW before this time, the interrupt will be registered as a *default* IR_7 regardless of which IR input initiated the interrupt request. This *default* IR_7 can be used to detect (and subsequently ignore) spurious interrupt signals such as those caused by glitches or noise on the IR input lines. The technique is described below:

- If the IR_7 input is not used, it can be assigned solely to intercepting spurious interrupt requests, invoking a simple service routine that contains a return only, thus effectively ignoring the interrupt.
- If IR_7 is used for a peripheral interrupt, a default IR_7 is detected with the extra step of reading the ISR. A normal IR_7 interrupt causes the corresponding bit to be set in the ISR, while a default IR_7 interrupt does not. It is necessary that the system software keep track of whether or not the IR_7 service routine has been entered. In the event that another IR_7 interrupt occurs before servicing is complete, it will be a default IR_7 interrupt (and should be ignored).

Edge Triggered Mode

Programmed by setting the LTIM bit in ICW_1: LTIM = 0 for *low-to-high-transition* edge triggering. An interrupt request is detected by a rising edge on an IR line. The IR line must remain HIGH until after the falling edge of the first $\overline{INTA}$ signal has been received from the CPU. This is required to latch the corresponding IRR bit. It is recommended that the IR line be kept HIGH to help filter out noise spikes that might cause spurious interrupts. To send the next interrupt request, temporarily lower the IR line, then raise it.

Level Triggered Mode

Programmed by setting the LTIM bit in ICW_1: LTIM = 1 for level triggering. An interrupt request is detected by a HIGH level on an IR line. This HIGH level must be maintained until the falling edge of the first $\overline{INTA}$ signal (as in the edge-triggered mode), to ensure the appropriate IRR bit is set. However, in the level triggered mode, interrupts are requested *as long as* the IR line remains HIGH. Thus, care should be exercised so as to prevent a stack overflow condition in the CPU.

Figure 20: Trigger Mode Timing

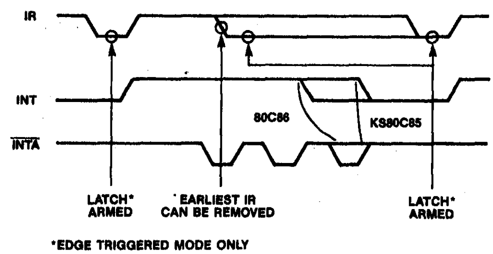
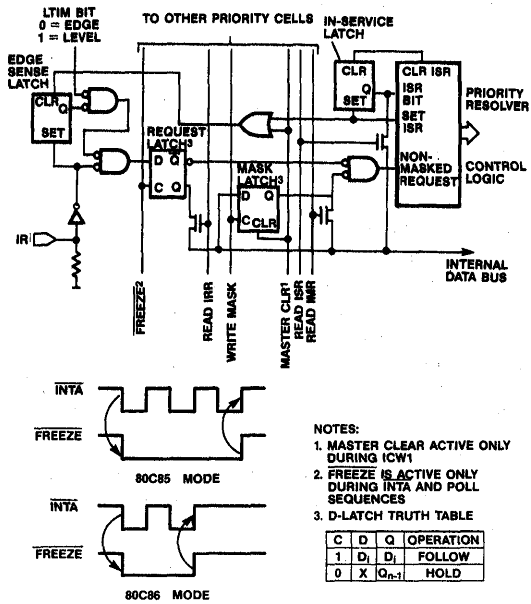


Figure 21: Priority Cell Structure



NOTES:
1. MASTER CLEAR ACTIVE ONLY DURING ICW1
2. $\overline{FREEZE}$ IS ACTIVE ONLY DURING $\overline{INTA}$ AND POLL SEQUENCES
3. D-LATCH TRUTH TABLE

C	D	Q	OPERATION
1	D_i	D_i	FOLLOW
0	X	Q_{n-1}	HOLD

APPLICATION DIAGRAMS

Figure 22: KS82C59A in Standard System Configuration

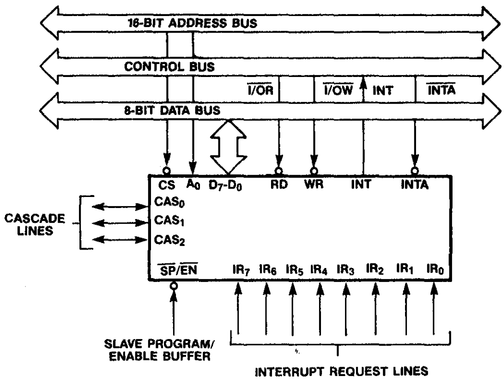
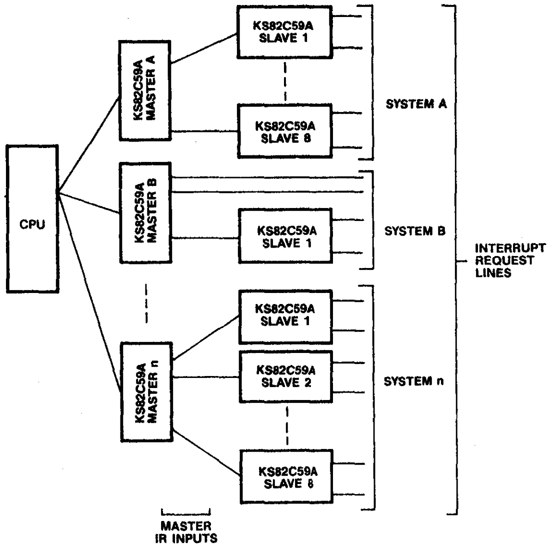


Figure 24: Multiple KS82C59A Masters in a Polled System



Notes:

1. Master KS82C59As in Poll Mode
2. Maximum of 64 Inputs per System
3. Total Capacity Limited by CPU

Figure 23: Multiple KS82C59As in a Cascaded System

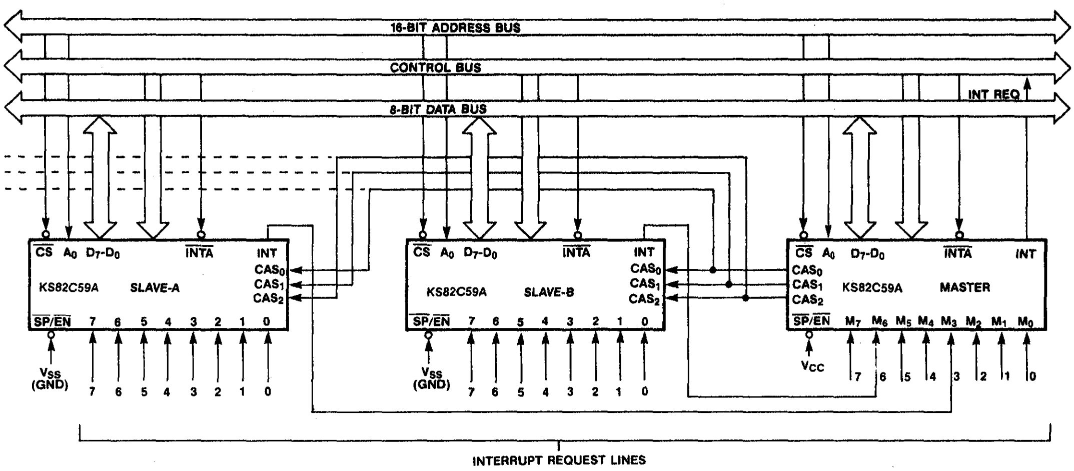


Table 5: Recommended Operating Conditions

DC Supply Voltage		+4.0V to +6.0V
Operating Temperature Ranges	Commercial	0°C to 70°C
	Industrial	-40°C to +85°C

Table 6: Absolute Maximum Ratings

DC Supply Voltage	-0.5 to +7.0V
Input, Output or I/O Voltage Applied	V_{SS} - 0.5V to V_{CC} + 0.5V
Storage Temperature Range	-65°C to +150°C
Maximum Package Power Dissipation	1W

Note: Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 7: Capacitance (T_A = 25°C, V_{CC} = 0V, V_{IN} = +5V or V_{SS})

Symbol	Parameter	Test Conditions	Typ	Units
$C_{I/O}$	I/O Capacitance	FREQ = 1MHz Unmeasured Pins Returned to V_{SS}	20	pF
C_{IN}	Input Capacitance		7	pF
C_{OUT}	Output Capacitance		15	pF

Table 8: DC Characteristics (T_A = 0°C to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Conditions	Limits		Unit
			Min	Max	
I_{CC}	V_{CC} Supply Current	V_{IN} = 0V/V_{CC}, C_L = 0pF	—	1	mA/MHz
I_{CCSB}	Standby Power Supply Current	CS = V_{CC}, IR = V_{CC} V_{IL} = 0V, V_{IH} - V_{CC}	—	10	μA
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	-1.0	+1.0	μA
I_{LIR}	IR Input Load Current	V_{IN} = 0V V_{IN} = V_{CC}, All temp ranges	— —	-300 10	μA μA
I_{LOL}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}	-10.0	+10.0	μA
V_{IH}	Input HIGH Voltage		2.2	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage		-0.5	0.8	V
V_{OH}	Output HIGH Voltage	I_{OH} = -2.5mA I_{OH} = -100μA	3.0 V_{CC} - 0.4	— —	V V
V_{OL}	Output LOW Voltage	I_{OL} = +2.5mA	—	0.4	V

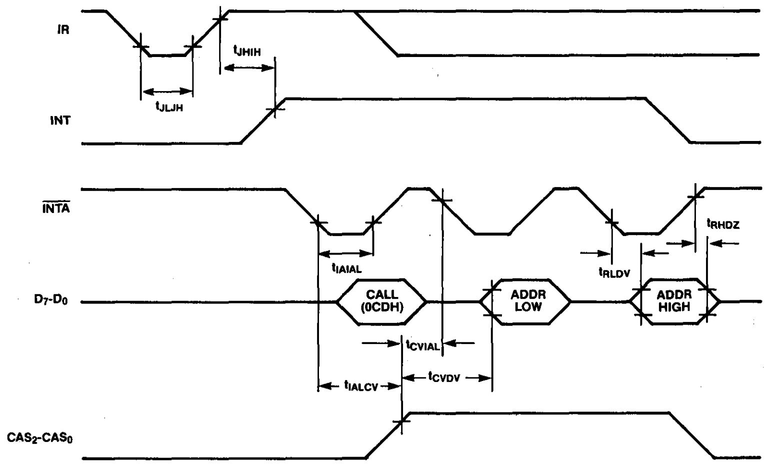
Table 9: AC Characteristics (T_A = 0°C to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Conditions	Limits (8MHz) Min	Limits (8MHz) Max	Limits (10MHz) Min	Limits (10MHz) Max	Units
t_{AHDV}	Data Valid from Stable Address		—	200	—	160	ns
t_{AHRL}	$A_0/\overline{CS}$ Setup to $\overline{RD}/\overline{INTA}$↓		10	—	10	—	ns
t_{AHWL}	$A_0/\overline{CS}$ Setup to $\overline{WR}$↓		0	—	0	—	ns
t_{CHCL}	End of Command to next Command (Not same command type) End of $\overline{INTA}$ Sequence to Next $\overline{INTA}$ sequence (same as T_{RV2})	Note 1	200	—	160	—	ns
t_{CVDV}	Cascade Valid to Valid Data	Slave, C_L = 100pF	—	200	—	130	ns
t_{CVIAL}	Cascade Setup to Second or Third $\overline{INTA}$↓ (Slave only)	Slave	40	—	30	—	ns
t_{DVWH}	Data Setup to $\overline{WR}$↑		160	—	100	—	ns
t_{IAIAH}	$\overline{INTA}$ Pulse Width HIGH	$\overline{INTA}$ Sequence	160	—	100	—	ns
t_{IAIAL}	$\overline{INTA}$ Pulse Width LOW		160	—	100	—	ns
t_{IALCV}	Cascade Valid from First $\overline{INTA}$↓ (Master Only)	Master, C_L = 100pF	—	260	—	160	ns
t_{JHIH}	Interrupt Output Delay	C_L = 100pF	—	200	—	120	ns
t_{JLJH}	Interrupt Request Width (LOW)	Note 2	100	—	100	—	ns
t_{RHAX}	$A_0/\overline{CS}$ Hold After $\overline{RD}/\overline{INTA}$↑		0	—	0	—	ns
t_{RHDZ}	Data Float After $\overline{RD}/\overline{INTA}$↑	C_L = 100pF	10	85	10	65	ns
t_{RHEH}	Enable Inactive from $\overline{RD}$↑ or $\overline{INTA}$↑		—	50	—	50	ns
t_{RHRL}	End of $\overline{RD}$ to next $\overline{RD}$ End of $\overline{INTA}$ to next $\overline{INTA}$ within $\overline{INTA}$ sequence only		160	—	100	—	ns
t_{RLDV}	Data Valid from $\overline{RD}/\overline{INTA}$↓	C_L = 100pF	—	120	—	95	ns
t_{RLEL}	Enable Active from $\overline{RD}$↓ or $\overline{INTA}$↓		—	100	—	70	ns
t_{RLRH}	$\overline{RD}$ Pulse Width		160	—	100	—	ns
t_{RV1}	Command Recovery Time	Note 3	200	—	160	—	ns
t_{RV2}	$\overline{INTA}$ Recovery Time	Note 4	200	—	160	—	ns
t_{WHAX}	$A_0/\overline{CS}$ Hold After $\overline{WR}$↑		0	—	0	—	ns
t_{WHDX}	Data Hold After $\overline{WR}$↑		0	—	0	—	ns
t_{WHWL}	End of $\overline{WR}$ to next $\overline{WR}$		160	—	100	—	ns
t_{WLWH}	$\overline{WR}$ Pulse Width		160	—	100	—	ns

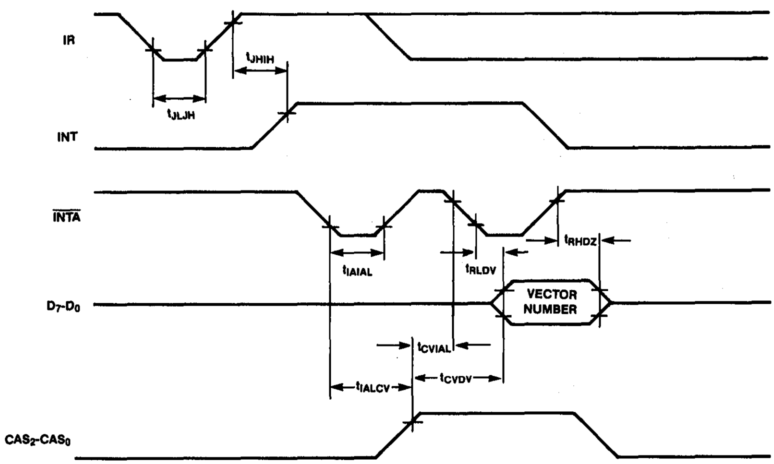
Notes:
1. The time to move $\overline{INTA}$ to/from command (read/write).
2. The time to clear the input latch in edge-triggered mode.
3. The time to move from read to write operation.
4. The time to move to the next $\overline{INTA}$ operation.

Figure 25: Timing Diagrams

a) Interrupt Cycle (CALL Mode)

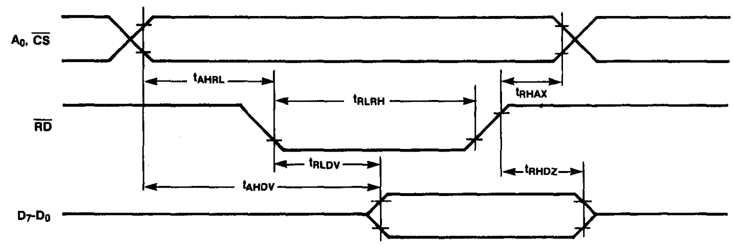


b) Interrupt Cycle (VECTOR Mode)

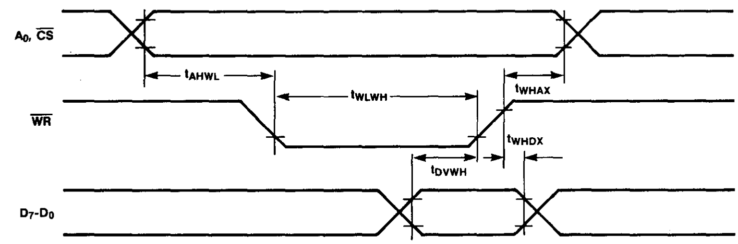


Note that **IR** input should remain at a high level until the leading edge of the first $\overline{\text{INTA}}$ pulse.

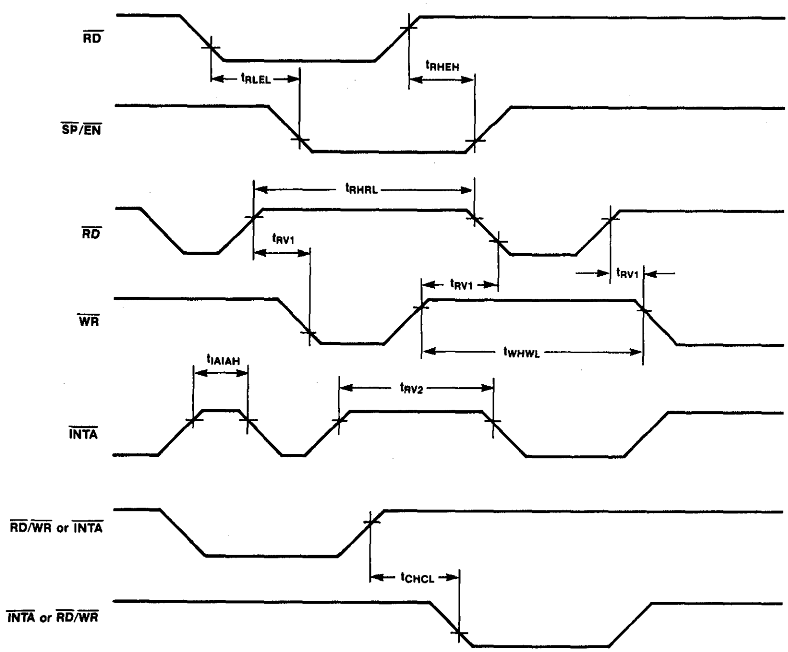
c) Read Cycle



d) Write Cycle



e) Other Timing



PACKAGE DIMENSIONS

Figure 26: Plastic Packaging DIP-28

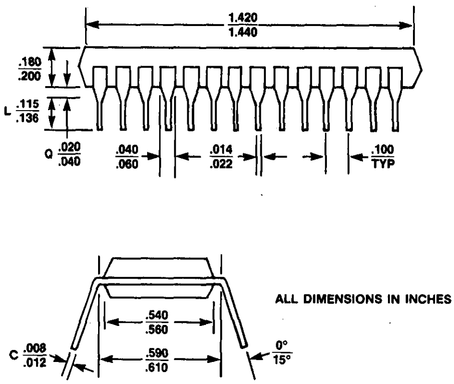
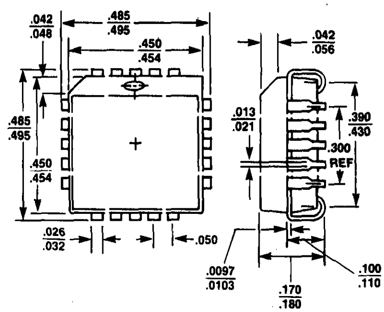


Figure 27: PLCC-28 Package



ORDERING INFORMATION AND PRODUCT CODE

KS 82C59A X X X

- **SAMSUNG SEMICONDUCTOR** — KS
- **Part Number** — 82C59A
- **Speed** — X
  - -8 8MHz
  - -10 10MHz
- **Temperature** — X
  - C — Commercial (0°C to +70°C)
  - I — Industrial (-40°C to +85°C)
- **Packaging** — X
  - P — Plastic DIP
  - L — Plastic Leaded Chip Carrier (PLCC)

SAMSUNG products are designated by a Product Code. When ordering, please refer to products by their full code. For unusual, and/or specific packaging or processing requirements not covered by the standard product line, please contact the SAMSUNG MOS Product Group.

FEATURES

- Pin and functional compatibility with the industry standard 82C84/82C84A
- Very high speed — 8 and 10MHz
- Low power CMOS implementation
- TTL input/output compatibility
- 5V ± 10% power supply
- Provides Local READY and Multibus™ READY Synchronization
- Generates System Reset Output from Schmitt Trigger Input
- Capable of Clock Synchronization with other 8284As
- Uses a Crystal or a TTL signal for frequency source

DESCRIPTION

The KS82C84A is a high performance, single chip clock generator/driver for the 8088/86 type processors, offering pin-for-pin functional compatibility with the industry standard 8284/8284A. It features a crystal-controlled oscillator, a divide-by-three counter, complete Multibus™ Ready synchronization, and reset logic.

The KS82C84A is manufactured using CMOS technology. Its very low power consumption also makes it suitable for portable systems and systems with low power standby modes.

3

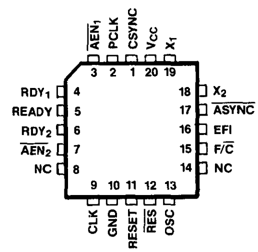


Figure 1a: 20-Pin PLCC Configuration

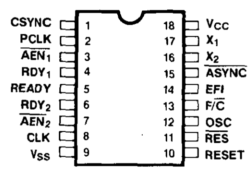


Figure 1b: 18-Pin DIP Configuration

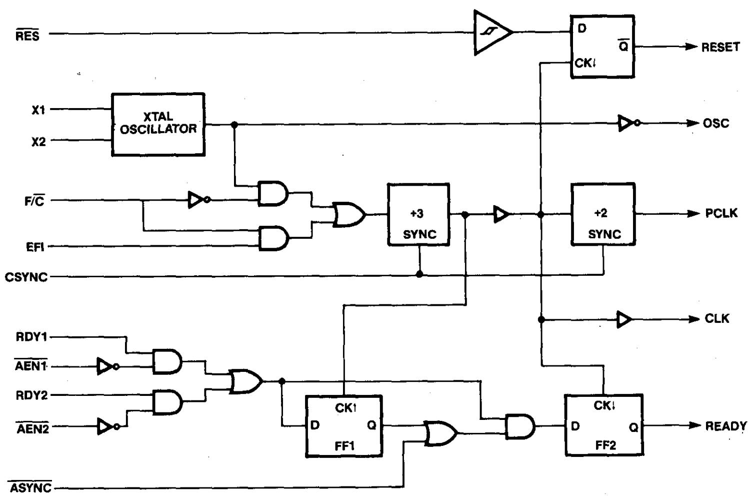


Figure 2: KS82C84A Block Diagram

Multibus is a trademark of Intel

Table 1a: 20-Pin PLCC Pin Assignment

Pin #	I/O	Pin Name	Pin #	I/O	Pin Name
1	I	CSYNC	11	O	RESET
2	O	PCLK	12	I	$\overline{RES}$
3	I	$\overline{AEN1}$	13	O	OSC
4	I	RDY1	14	—	NC
5	O	READY	15	I	F/$\overline{C}$
6	I	RDY2	16	I	EFI
7	I	$\overline{AEN2}$	17	I	$\overline{ASYNC}$
8	—	NC	18	I	X2
9	O	CLK	19	I	X1
10	—	V_{SS}	20	—	V_{CC}

Table 1b: 18-Pin DIP Pin Assignment

Pin #	I/O	Pin Name	Pin #	I/O	Pin Name
1	I	CSYNC	10	O	RESET
2	I	PCLK	11	O	$\overline{RES}$
3	I	$\overline{AEN1}$	12	O	OSC
4	O	RDY1	13	O	F/$\overline{C}$
5	O	READY	14	I	EFI
6	I	RDY2	15	O	$\overline{ASYNC}$
7	O	$\overline{AEN2}$	16	O	X2
8	O	CLK	17	I	X1
9	—	V_{SS}	18	—	V_{CC}

Table 2: Pin Descriptions

Symbol	Type	Name and Function
$\overline{AEN1}$, $\overline{AEN2}$	I	**Address Enable:** $\overline{AEN}$ is an active LOW signal which qualifies its respective Bus Ready Signal. $\overline{AEN1}$ validates RDY1 while $\overline{AEN2}$ validates RDY2. Two $\overline{AEN}$ signal inputs are useful in system configurations with two multi-master System Buses. In non-multi-master configurations the $\overline{AEN}$ signal inputs are tied true (LOW).
$\overline{ASYNC}$	I	**Ready Synchronization Select:** $\overline{ASYNC}$ defines the synchronization mode of the READY logic. When $\overline{ASYNC}$ is LOW, two stages of READY synchronization are provided. When HIGH or open a single stage of READY synchronization is provided.
CLK	O	**Processor Clock:** CLK is used by the processor and all devices which connect directly to the processor's local bus. CLK has an output frequency of 1/3 the crystal or EFI input frequency and a 1/3 duty cycle. An output HIGH of 4.5 volts (V_{CC} = 5V) is provided to drive MOS devices.
CSYNC	I	**Clock Synchronization:** CSYNC is an active HIGH signal which allows multiple 8284As to be synchronized to provide clocks that are in phase. When CSYNC is HIGH the internal counters are reset. When CSYNC goes LOW the internal counters are allowed to resume counting. CSYNC must be externally synchronized to EFI. When using the internal oscillator, CSYNC should be hardwired to ground.
EFI	I	**External Frequency:** When F/$\overline{C}$ is strapped HIGH, CLK is generated from the input frequency appearing on this pin. This input signal is a square wave 3x the frequency of the desired CLK output. EFI should be connected to V_{CC} or V_{SS} if F/$\overline{C}$ is LOW.
F/$\overline{C}$	I	**Frequency/Crystal Select:** F/$\overline{C}$ is a strapping option. When strapped LOW, F/$\overline{C}$ permits the processor clock to be generated by the crystal. When strapped HIGH, CLK is generated form the EFI input.
OSC	O	**Oscillator Output:** OSC is the TTL level output of the internal oscillator circuitry. Its frequency is equal to that of the crystal.
PCLK	O	**Peripheral Clock:** PCLK is a TTL level peripheral clock signal whose output frequency is 1/2 that of CLK and has a 50% duty cycle.

Table 2: Pin Descriptions (Continued)

Symbol	Type	Name and Function
RDY1, RDY2	I	**Bus Ready:** (Transfer Complete) RDY is an active HIGH signal which indicates that data from a device located on the system data bus has been received, or is available. RDY1 is qualified by $\overline{\text{AEN1}}$ while RDY2 is qualified by $\overline{\text{AEN2}}$.
READY	O	**Ready:** READY is an active HIGH signal which is synchronized to the RDY signal input. READY is cleared after the guaranteed hold time to the processor has been met.
$\overline{\text{RES}}$	I	**Reset In:** $\overline{\text{RES}}$ is an active LOW signal used to generate RESET. The KS82C84A provides a Schmitt trigger input so that an RC connection can be used to establish the power-up reset of proper duration.
RESET	O	**Reset:** RESET is an active HIGH signal which is used to reset the 8086 family processors. Its timing characteristics are determined by $\overline{\text{RES}}$.
X1, X2	I	**Crystal In:** X1 and X2 are the pins to which a crystal is attached. The crystal frequency is 3x the desired processor clock frequency. (If no crystal is attached, then X1 should be tied to V_{CC} or V_{SS} and X2 should be left open.)
V_{CC}	—	**Power:** 5V ± 10% DC Supply.
V_{SS}	—	**Ground:** 0V.

FUNCTIONAL DESCRIPTION

Oscillator

The oscillator of the KS82C84A is designed for use with an external parallel resonant, fundamental mode crystal from which the basic operating frequency is derived.

The crystal frequency should be selected to be 3X the required CPU clock frequency. X1 and X2 are the two crystal inputs. For the most stable operation of OSC, two capacitors (C1 = C2), as shown in the waveform figures, are recommended. The output of the oscillator is buffered and brought out on OSC so that other system timing signals can be derived from this stable, crystal-controlled source.

Capacitors C1, C2 are chosen such that their combined capacitance:

$$CT = \frac{C1 \cdot C2}{C1 + C2} \text{ (Including Stray Capacitance)}$$

matches the load capacitance as specified by the crystal manufacturer. This insures operation within the frequency tolerance specified by the crystal manufacturer.

Clock Generator

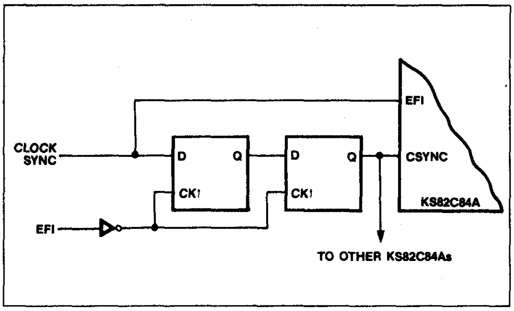
The clock generator consists of a synchronous divide-by-three counter with a special clear input that inhibits the counting. This clear input (CSYNC) allows the output clock to be synchronized with an external event (such as another KS82C84A clock). The ASYNC input to the EFI clock external to the KS82C84A is synchronized using two Schottky flip-flops. The counter output is a 33% duty cycle clock at one-third the input frequency.

The F/$\overline{\text{C}}$ input is a strapping pin that selects either the crystal oscillator or the EFI input as the clock for the ÷3 counter. If the EFI input is selected as the clock source, the oscillator section can be used independently for another clock source with output taken from OSC.

Clock Outputs

The CLK output is a 33% duty cycle clock driver designed to drive the 8088/86 processors directly. PCLK is a TTL level peripheral clock signal with a frequency of 1/2 CLK, and a 50% duty cycle.

Figure 3: CSYNC Synchronization



Reset Logic

The reset logic provides a Schmitt trigger input ($\overline{RES}$) and a synchronizing flip-flop to generate the reset timing. The reset signal is synchronized to the falling edge of CLK. Utilizing this function, a simple RC network can be used to provide a power-on reset.

READY Synchronization

Two READY Inputs (RDY1, RDY2) are provided to accommodate two multi-master system buses. Each input has a qualifier ($\overline{AEN1}$ and $\overline{AEN2}$, respectively). The $\overline{AEN}$ signals validate their respective RDY signals. If a multi-master system is not being used, the $\overline{AEN}$ pin should be tied LOW.

Synchronization is required for all asynchronous active-going edges of either RDY input to guarantee that the RDY setup and hold times are met. Inactive-going edges of RDY in normally ready systems do not require synchronization, but must satisfy RDY setup and hold.

The $\overline{ASYNC}$ input defines two modes of READY synchronization operation: When $\overline{ASYNC}$ is LOW, two stages of synchronization are provided for active READY input signals. Positive-going asynchronous READY inputs are first synchronized to flip-flop one at the rising edge of CLK, and then synchronized to flip-flop two at the next falling edge of CLK, after which the READY output goes active (HIGH). Negative-going asynchronous READY inputs are synchronized directly to flip-flop two at the falling edge of CLK, after which the READY output goes inactive. This mode of operation is intended for asynchronous (normally not ready) devices in the system which cannot be guaranteed by design to meet the required RDY setup timing, t_{R1VCL}, on each bus cycle.

When $\overline{ASYNC}$ is HIGH or open, the first READY flip-flop is bypassed in the READY synchronization logic. READY inputs are synchronized by flip-flop two on the falling edge of CLK before they are presented to the processor. This mode is available for synchronous devices that can be guaranteed to meet the required RDY setup time.

$\overline{ASYNC}$ can change at every bus cycle to set the correct synchronization mode for each device in the system.

Table 3: Recommended Operating Conditions

DC Supply Voltage		+4.0V to +6.0V
Operating Temperature Range	Commercial	0°C to 70°C
	Industrial	-40°C to +85°C

Table 4: Absolute Maximum Ratings

DC Supply Voltage	+7.0V
Input, Output or I/O Voltage Applied	V_{SS} - 0.5V to V_{CC} + 0.5V
Storage Temperature Range	-65°C to +150°C
Maximum Package Power Dissipation	1W

Note: Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 5: DC Characteristics (T_A = 0°C to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Symbol	Parameter		Test Conditions	Limits Min	Limits Max	Unit
C_{IN}	Input Capacitance		freq = 1MHz		7	pF
I_{CC}	Operating Supply Current: 5MHz 10MHz		15MHz xtal, C_L = 0 30MHz xtal, C_L = 0		10 40	mA mA
I_{CCS}	Standby Supply Current (Note 1)				100	μA
I_{LI}	Input Leakage Current: (Note 2)	ASYNC Only	ASYNC = V_{CC}		10	μA
			ASYNC = V_{SS}		-130	μA
		All Other Pins	0V ≤ V_{IN} ≤ V_{CC}		±1.0	μA
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.5	V
V_{IHR}	Reset Input HIGH Voltage			0.6V_{CC}		V
V_{IHR}-V_{ILR}	RES Input Hysteresis			0.25		V
V_{IL}	Input LOW Voltage				0.8	V
V_{OH}	Output HIGH Voltage		CLK: I_{OH} = -4mA Others: I_{OH} = -2.5mA	V_{CC}-0.4		V
V_{OL}	Output LOW Voltage		CLK: I_{OL} = 4mA Others: I_{OL} = 2.5mA		0.4	V

Notes:
1. V_{IH}, F/$\overline{C}$ X1 ≥ V_{CC} - 0.2V; V_{IL} X2 ≤ 0.2V; $\overline{ASYNC}$ = V_{CC} or $\overline{ASYNC}$ = Open.
2. An internal pull-up resistor is implemented on the $\overline{ASYNC}$ input.

Table 6: AC Characteristics, DMA (Master) Mode (T_A = 0°C to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

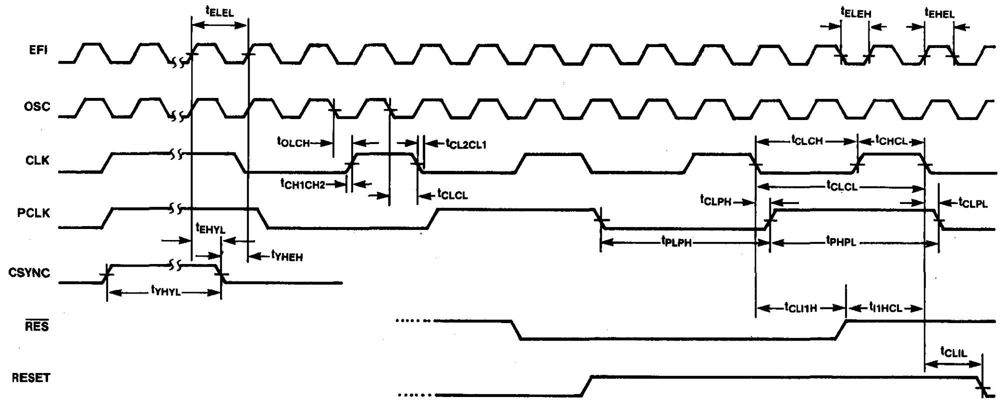
Symbol	Parameter	Test Conditions	Limits (8MHz)		Limits (10MHz)		Units
			Min	Max	Min	Max	
t_{A1VR1V}	$\overline{AEN1}$, $\overline{AEN2}$ Setup to RDY1, RDY2		15		15		ns
t_{AYVCL}	$\overline{ASYNC}$ Setup to CLK		50		50		ns
t_{CH1CH2} t_{CL2CL1}	CLK Rise or Fall Time	1.0V to 3.5V		10		10	ns
t_{CHCL}	CLK HIGH Time		$\frac{1}{3}t_{CLCL}+2$		$\frac{1}{3}t_{CLCL}+2$		ns
t_{CLA1X}	$\overline{AEN1}$, $\overline{AEN2}$ Hold to CLK		0		0		ns
t_{CLAYX}	$\overline{ASYNC}$ Hold to CLK		0		0		ns
t_{CLCH}	CLK LOW Time		$\frac{2}{3}t_{CLCL}-15$		$\frac{2}{3}t_{CLCL}-15$		ns
t_{CLCL}	CLK Cycle Period		125		100		ns
t_{CLI1H}	$\overline{RES}$ Hold to CLK	(Note 2)	10		10		ns
t_{CLIL}	CLK to Reset Delay			40		40	ns
t_{CLR1X}	RDY1, RDY2 Hold to CLK		0		0		ns
t_{CLPH}	CLK to PCLK HIGH Delay			22		22	ns
t_{CLPL}	CLK to PCLK LOW Delay			22		22	ns
t_{EHEL}	External Frequency HIGH Time	90%–90% V_{IN}	13		13		ns
t_{EHYL}	CSYNC Hold to EFI		10		10		ns
t_{ELEH}	External Frequency LOW Time	10%–10% V_{IN}	13		13		ns
t_{ELEL}	EFI Period	(Note 1)	36		33		ns
t_{I1HCL}	$\overline{RES}$ Setup to CLK	(Note 2)	65		65		ns
t_{IHIL}	Input Fall Time	(Note 1)		15		15	ns
t_{ILIH}	Input Rise Time	(Note 1)		15		15	ns
t_{OLCH}	OSC to CLK HIGH Delay		-5	22	-5	22	ns
t_{OLCL}	OSC to CLK LOW Delay		2	35	2	35	ns
t_{OLOH}	Output Rise Time (except CLK)	From 0.8V to 2.0V		15		15	ns
t_{OHOL}	Output Fall Time (except CLK)	From 2.0V to 0.8V		15		15	ns
t_{PHPL}	PCLK HIGH Time		$t_{CLCL}-20$		$t_{CLCL}-20$		ns
t_{PLPH}	PCLK LOW Time		$t_{CLCL}-20$		$t_{CLCL}-20$		ns
t_{R1VCH}	RDY1, RDY2 Active Setup to CLK	$\overline{ASYNC}$ = LOW	35		35		ns
t_{R1VCL}	RDY1, RDY2 Active Setup to CLK	$\overline{ASYNC}$ = HIGH	35		35		ns
t_{RYHCH}	Ready Active to CLK	(Note 3)	$\frac{2}{3}t_{CLCL}-15$		$\frac{2}{3}t_{CLCL}-15$		ns
t_{RYLCL}	Ready Inactive to CLK	(Note 4)	-8		-8		ns
t_{YHEH}	CSYNC Setup to EFI		20		20		ns
t_{YHYL}	CSYNC Width		$2 \cdot t_{ELEL}$		$2 \cdot t_{ELEL}$		ns
	XTAL Frequency		2.4	25	2.4	30	MHz

Notes:
1. Transition between V_{IL} (Max) - 0.4V and V_{IH} (Min) + 0.4V.
2. Setup and hold necessary only to guarantee recognition at next clock.
3. Applies only to T_3 and T_W states.
4. Applies only to T_2 states.

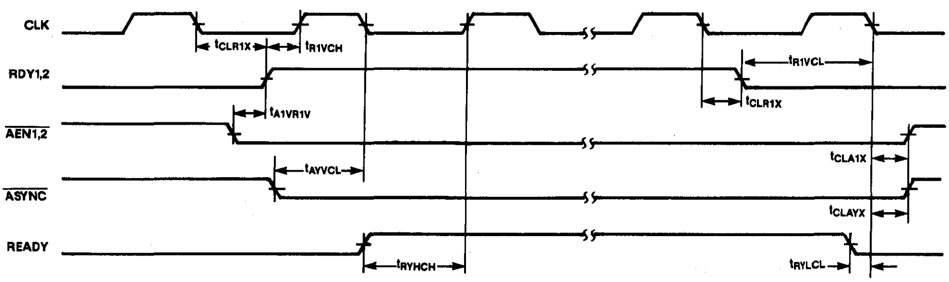
3

Figure 4: Timing Diagrams

a) Clocks and Reset Signals



b) Ready Signals (for Asynchronous Devices)



c) Ready Signals (for Synchronous Devices)

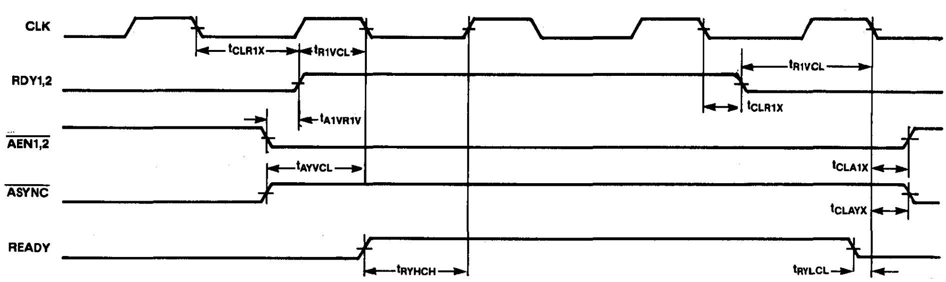
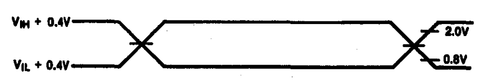
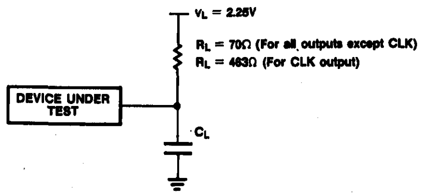


Figure 5: AC Testing I/O Waveform



A.C. Testing: All input signals must switch between 0.45V and 2.4V. T_{RISE} and T_{FALL} must be ≤ 15ns. All timing measurements are made at 0.8V and 2.0V.

Figure 6: AC Testing Loading Circuit



C_L = 100pF for CLK
C_L = 10pF for READY
C_L includes probe and jig capacitance

Figure 7: Clock High & Low Time (Using X1, X2)

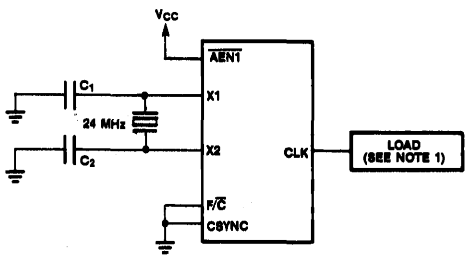


Figure 8: Clock High & Low Time (Using EFI)

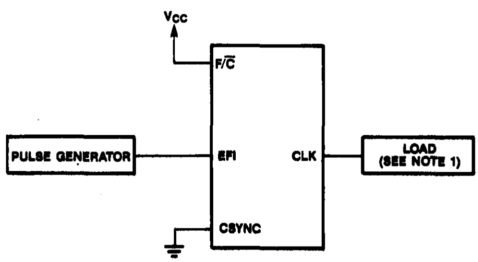


Figure 9: Ready to Clock (Using X1, X2)

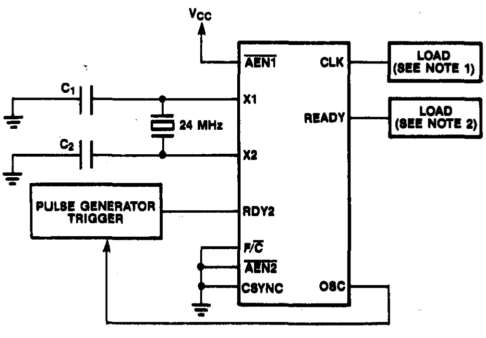
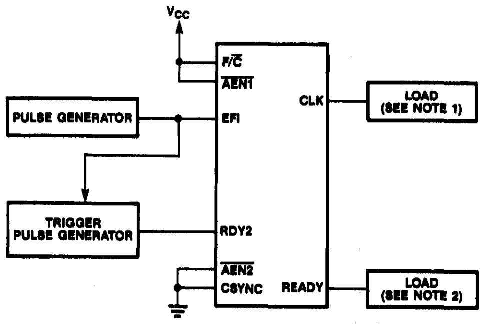
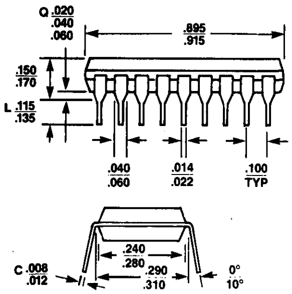


Figure 10: Ready to Clock (Using EFI)



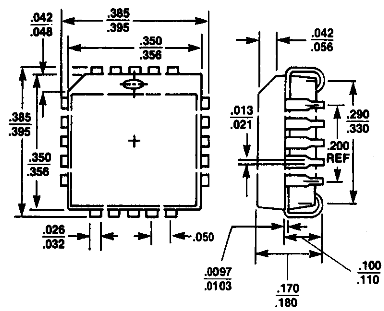
Notes: 1. C_L = 100pF
2. C_L = 30pF

PACKAGE DIMENSIONS



ALL DIMENSIONS IN INCHES

Plastic Package



ALL DIMENSIONS IN INCHES

PLCC Package

ORDERING INFORMATION AND PRODUCT CODE

KS 82C84A X X X

- **KS** — **SAMSUNG SEMICONDUCTOR**
- **82C84A** — **Part Number**
- **X** — **Speed**
  - -8 8MHz
  - -10 10MHz
- **X** — **Temperature**
  - C — Commercial (0°C to +70°C)
  - I — Industrial (-40°C to +85°C)
- **X** — **Packaging**
  - P — Plastic DIP
  - L — Plastic Leaded Chip Carrier (PLCC)

SAMSUNG products are designated by a Product Code. When ordering, please refer to products by their full code. For unusual, and/or specific packaging or processing requirements not covered by the standard product line, please contact the SAMSUNG MOS Product Group.

FEATURES/BENEFITS

- **Pin and functional compatibility with the industry standard 8288**
- **Very high speed — 8MHz and 10MHz**
- **Low power CMOS implementation**
- **Bipolar drive capability**
- **TTL I/O compatibility**
- **3-state command output drivers**
- **Configurable for use with an I/O bus**
- **Facilitates interface to one or two multi-master buses**

DESCRIPTION

The KS82C88 Bus Controller is a 20-pin CMOS component which includes command and control timing generation as well as a bipolar bus drive capability while optimizing system performance. A strapping option on the bus controller configures it for use with a multi-master system bus and separate I/O bus.

The KS82C88 is manufactured using advanced CMOS technology. Fully static, with very high speed operation, the KS82C88 is designed for use in medium-to-large 8088/86 microprocessor systems.

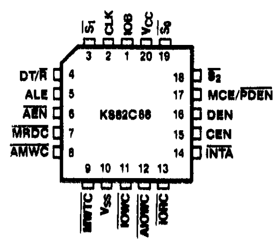


Figure 1a: 20-Pin PLCC Configuration

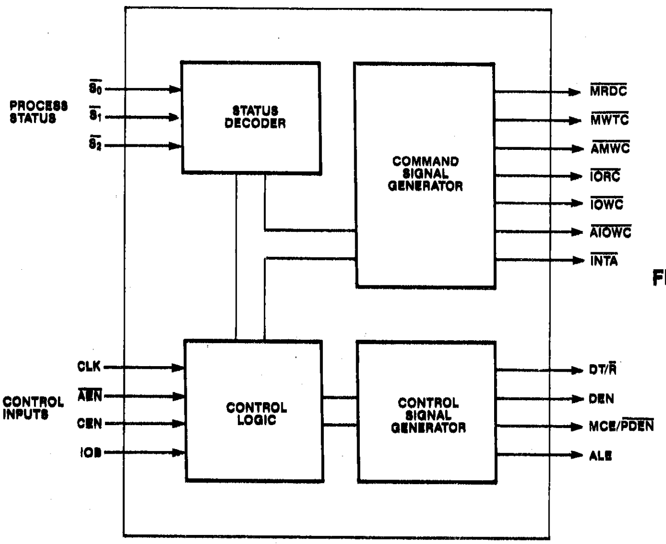


Figure 2: KS82C88 Block Diagram

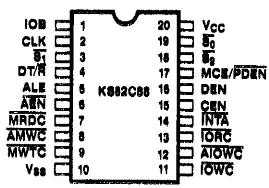


Figure 1b: 20-Pin DIP Configuration

Table 1a: PLCC Pin Assignment

Pin #	I/O	Pin Name	Pin #	I/O	Pin Name
1	I	IOB	11	O	$\overline{\text{IOWC}}$
2	I	CLK	12	O	$\overline{\text{AIOWC}}$
3	I	$\overline{S_1}$	13	O	$\overline{\text{IORC}}$
4	O	DT/$\overline{\text{R}}$	14	O	$\overline{\text{INTA}}$
5	O	ALE	15	I	CEN
6	I	$\overline{\text{AEN}}$	16	O	DEN
7	O	$\overline{\text{MRDC}}$	17	O	MCE/$\overline{\text{PDEN}}$
8	O	$\overline{\text{AMWC}}$	18	I	$\overline{S_2}$
9	O	$\overline{\text{MWTC}}$	19	I	$\overline{S_0}$
10	—	V_{SS}	20	—	V_{CC}

Table 1b: 20-Pin DIP Pin Assignment

Pin #	I/O	Pin Name	Pin #	I/O	Pin Name
1	I	IOB	11	O	$\overline{\text{IOWC}}$
2	I	CLK	12	O	$\overline{\text{AIOWC}}$
3	I	$\overline{S_1}$	13	O	$\overline{\text{IORC}}$
4	O	DT/$\overline{\text{R}}$	14	O	INTA
5	O	ALE	15	I	CEN
6	I	$\overline{\text{AEN}}$	16	O	DEN
7	O	$\overline{\text{MRDC}}$	17	O	MCE/$\overline{\text{PDEN}}$
8	O	$\overline{\text{AMWC}}$	18	I	$\overline{S_2}$
9	O	$\overline{\text{MWTC}}$	19	I	$\overline{S_0}$
10	—	V_{SS}	20	—	V_{CC}

Table 2: Pin Descriptions

Symbol	Type	Name and Function
$\overline{\text{AEN}}$	I	**Address Enable:** $\overline{\text{AEN}}$ enables the KS82C88 command outputs at least t_{AELCV} (Table 4) after it becomes active (LOW). When $\overline{\text{AEN}}$ goes inactive, the command output drivers are immediately 3-stated. $\overline{\text{AEN}}$ does not affect the I/O command lines if the KS82C88 is in the I/O Bus mode (IOB tied HIGH).
$\overline{\text{AIOWC}}$	O	**Advanced I/O Write Command:** The $\overline{\text{AIOWC}}$ issues an I/O Write command earlier in the machine cycle to give I/O devices an early indication of a write instruction. Its timing is the same as a read command signal. This signal is active LOW.
ALE	O	**Address Latch Enable:** This signal serves to strobe an address into the address latches. It is active HIGH and latching occurs on the falling (HIGH to LOW) transition. ALE is intended for use with transparent D type latches.
$\overline{\text{AMWC}}$	O	**Advanced Memory Write Command:** This active LOW signal is used to issue a memory write command earlier in the machine cycle to give memory devices an early indication of a write instruction. Its timing is the same as a read command signal.
CEN	I	**Command Enable:** When LOW all KS82C88 command outputs, and the control outputs DEN and $\overline{\text{PDEN}}$ are forced to the inactive state. When HIGH, these outputs are enabled.
CLK	I	**Clock:** This clock signal from the KS82C88 clock generator is used to determine when command and control signals are generated.
DEN	O	**Data Enable:** This active HIGH signal enables data transceivers onto either the local or system data bus.
DT/$\overline{\text{R}}$	O	**Data Transmit/Receive:** This signal establishes the direction of data flow through the transceivers. HIGH indicates Transmit (write to I/O or memory), LOW indicates Receive (Read).
$\overline{\text{INTA}}$	O	**Interrupt Acknowledge:** This active LOW signal tells an interrupting device that its interrupt has been acknowledged and that it should drive vector information onto the data bus.
IOB	I	**Input/Output Bus Mode:** When IOB is strapped HIGH the KS82C88 functions in the I/O Bus mode. When strapped LOW, the KS82C88 functions in the System Bus mode. (See sections on I/O Bus and System Bus modes)

Table 2: Pin Descriptions (Continued)

Symbol	Type	Name and Function
$\overline{\text{IORC}}$	O	**I/O Read Command:** This active LOW signal instructs an I/O device to drive its data onto the data bus.
$\overline{\text{IOWC}}$	O	**I/O Write Command:** This active LOW signal instructs an I/O device to read the data on the data bus.
MCE/$\overline{\text{PDEN}}$	O	**MCE (IOB is tied LOW):** Master Cascade Enable occurs during an interrupt sequence and serves to read a Cascade Address from a master PIC (Priority Interrupt Controller) onto the data bus. The MCE signal is active HIGH. **$\overline{\text{PDEN}}$ (IOB is tied HIGH):** Peripheral Data Enable enables the data bus transceiver for the I/O bus that DEN performs.
$\overline{\text{MRDC}}$	O	**Memory Read Command:** This active LOW signal instructs the memory to drive its data onto the data bus.
$\overline{\text{MWTC}}$	O	**Memory Write Command:** This active LOW signal instructs the memory to record the data present on the data bus.
$\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$	I	**Status Input Pins:** These are status input pins from 8088/86/89 processors. The KS82C88 decodes these inputs to generate command and control signals at the appropriate time. These pins are HIGH when not in use. Internal pull-up resistors hold these lines HIGH when no other driving source is present.
V_{CC}	—	**Power:** 5V ± 10% DC Supply.
V_{SS}	—	**Ground:** 0V.

FUNCTIONAL DESCRIPTION

Command and Control Logic

The KS82C88 decodes the status line signals ($\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$) common to the 8086/88/89 processors to determine what command is to be issued, (Table 3).

Table 3: KS82C88 Commands

$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	Processor State	8288 Command
0	0	0	Interrupt Acknowledge	$\overline{\text{INTA}}$
0	0	1	Read I/O Port	$\overline{\text{IORC}}$
0	1	0	Write I/O Port	$\overline{\text{IOWC}}$, $\overline{\text{AIOWC}}$
0	1	1	Halt	None
1	0	0	Code Access	$\overline{\text{MRDC}}$
1	0	1	Read Memory	$\overline{\text{MRDC}}$
1	1	0	Write Memory	$\overline{\text{MWTC}}$, $\overline{\text{AMWC}}$
1	1	1	Passive	None

Operating Modes

The KS82C88 can be operated in one of two modes, I/O Bus Mode or System Bus Mode according to the system hardware configuration.

I/O Bus Mode: *(IOB Strapped HIGH)*

In the I/O Bus (IOB) mode the I/O command lines ($\overline{\text{IORC}}$, $\overline{\text{IOWC}}$, $\overline{\text{AIOWC}}$, $\overline{\text{INTA}}$) are always enabled (not dependent on $\overline{\text{AEN}}$). When an I/O command is initiated by the processor, the KS82C88 immediately activates the command lines using $\overline{\text{PDEN}}$ and DT/$\overline{\text{R}}$ control the I/O bus transceiver. Since no arbitration is present, the I/O command lines should not be used to control the sytem bus in this mode. This mode allows one KS82C88 to handle two external buses. No waiting is involved when the CPU wants to gain access to the I/O bus. Normal memory access requires a Bus Ready signal ($\overline{\text{AEN}}$ LOW) before proceeding. The IOB mode is aimed at applications where I/O or peripherals dedicated to one processor exist in a multi-processor system.

System Bus Mode: *(IOB Strapped LOW)*

In this mode no commands are issued until t_{AELCV} (Table 4) after the $\overline{\text{AEN}}$ Line is activated (LOW). This mode assumes that bus arbitration logic will inform the bus controller (on the $\overline{\text{AEN}}$ line) when the bus is free for use. Both memory and I/O commands wait for bus arbitration. This mode is used when only one bus exists, and both I/O and memory are shared by more than one processor.

Table 4: Command Outputs

$\overline{\text{MRDC}}$	Memory Read Command
$\overline{\text{MWTC}}$	Memory Write Command
$\overline{\text{IORC}}$	I/O Read Command
$\overline{\text{IOWC}}$	I/O Write Command
$\overline{\text{AMWC}}$	Advanced Memory Write Command
$\overline{\text{AIOWC}}$	Advanced I/O Write Command
$\overline{\text{INTA}}$	Interrupt Acknowledge

Command Outputs

Advanced write commands prevent the processor from entering unnecessary wait states. They are available to initiate write procedures early in the machine cycle.

$\overline{\text{INTA}}$ (Interrupt Acknowledge) acts as an I/O read during an interrupt cycle. $\overline{\text{INTA}}$ informs an interrupting device that it should place service vectors onto the data bus.

Control Outputs

KS82C88 control outputs include Data Enable (DEN), Data Transmit/Receive (DT/$\overline{\text{R}}$) and Master Cascade Enable/Peripheral Data Enable (MCE/$\overline{\text{PDEN}}$). DEN determines when the external bus should be enabled onto the local bus and DT/$\overline{\text{R}}$ determines the direction of data transfer. These two signals are usually connected to the transceiver chip select and direction pins.

MCE/$\overline{\text{PDEN}}$ alters its function with the operating mode. In the IOB mode, the $\overline{\text{PDEN}}$ signal serves as a dedicated data enable signal for the I/O or Peripheral System Bus.

In the System Bus Mode, MCE is used during interrupt acknowledge cycles. Two interrupt acknowledge cycles occur back to back during interrupt sequences, with no data or address transfers during the first cycle. Thus logic should be provided to mask off MCE. Just before the second cycle, MCE gates a master Priority Interrupt Controller's (PIC) cascade address onto the processor's local bus where ALE strobes it into the address latches. On the leading edge of the second interrupt cycle, the addressed slave PIC gates an interrupt vector onto the system data bus where it is read by the processor.

If the system contains only one PIC, MCE is not used and the second Interrupt Acknowledge signal gates the interrupt vector onto the processor bus.

Address Latch Enable (ALE) and Halt

ALE occurs every machine cycle and strobes the current address into the address latches. ALE also strobes $\overline{S}_0$, $\overline{S}_1$, $\overline{S}_2$ into a latch for halt state decoding.

Command Enable (CEN)

CEN is a command qualifier for the KS82C88. If CEN is HIGH, the KS82C88 functions normally, and all command lines are held in their inactive state (not 3-state). This feature can be used to implement memory partitioning and to eliminate address conflicts between system bus and resident bus devices.

Table 5: Recommended Operating Conditions

DC Supply Voltage		+4.0V to +6.0V
Operating Temperature Range	Commercial	0°C to 70°C
	Industrial	-40°C to +85°C

Table 6: Absolute Maximum Ratings

DC Supply Voltage	+7.0V
Input, Output or I/O Voltage Applied	V_{SS}-0.5V to V_{CC}+0.5V
Storage Temperature Range	-65°C to +150°C
Maximum Package Power Dissipation	1W

Note: Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 7: DC Characteristics (T_A = 0°C to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Symbol	Parameter	Test Conditions	Limits Min	Limits Max	Units
C_{IN}	Input Capacitance	Freq. = 1MHz Unmeasured pins at V_{SS}		5	pF
C_{OUT}	Output Capacitance			15	pF
I_{BHH}	Input Leakage Current (Bus Hold High)	V_{IN} = 2.0V (Notes 3, 4)	-50	-300	μA
I_{BHHO}	Bus Hold High Overdrive	(Notes 3, 5)	-600		μA
I_{CC}	Operating Supply Current	V_{IN} = V_{CC} or V_{SS}, V_{CC} = 5.5V Outputs Unloaded, Freq 5MHz		5	mA
I_{CCS}	Standby Supply Current	V_{IN} = V_{CC} or V_{SS}, V_{CC} = 5.5V Outputs Unloaded		100	μA
I_{LI}	Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$ (Notes 1, 2)		±10	μA
I_{LO}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$		±10	μA
V_{CH}	V_{IH} for Clock, $\overline{S}_0$, $\overline{S}_1$, $\overline{S}_2$		3.0	V_{CC}+0.3	V
V_{CL}	V_{IL} for Clock, $\overline{S}_0$, $\overline{S}_1$, $\overline{S}_2$			0.2V_{CC}	V
V_{IH}	Input High Voltage		2.2	V_{CC}+0.3	V
V_{IL}	Input Low Voltage		-0.3	0.8	V
V_{OH}	Output High Voltage — Command Outputs	I_{OH} = -5mA I_{OH} = -1mA	3.7 3.7		V V
	Output High Voltage — Control Outputs	I_{OH} = -4mA I_{OH} = -2.5mA	3.0 V_{CC}-0.4		V V
V_{OL}	Output LOW Voltage	I_{OL} = 12mA I_{OL} = 8mA		0.45 0.44	V V

Notes:
1. Except $\overline{S}_0$, $\overline{S}_1$, $\overline{S}_2$.
2. During input leakage test, maximum input rise and fall time should be 15ns between V_{CC} and V_{SS}.
3. $\overline{S}_0$, $\overline{S}_1$, $\overline{S}_2$ only.
4. Raise inputs to V_{CC}, then lower to 2.0V.
5. An external driver must sink at least I_{BHHO} to toggle a status line from HIGH to LOW.

Table 8: AC Characteristics, (T_A = 0°C to 70°C, V_{DD} = 5V ± 10%, V_{SS} = 0V)

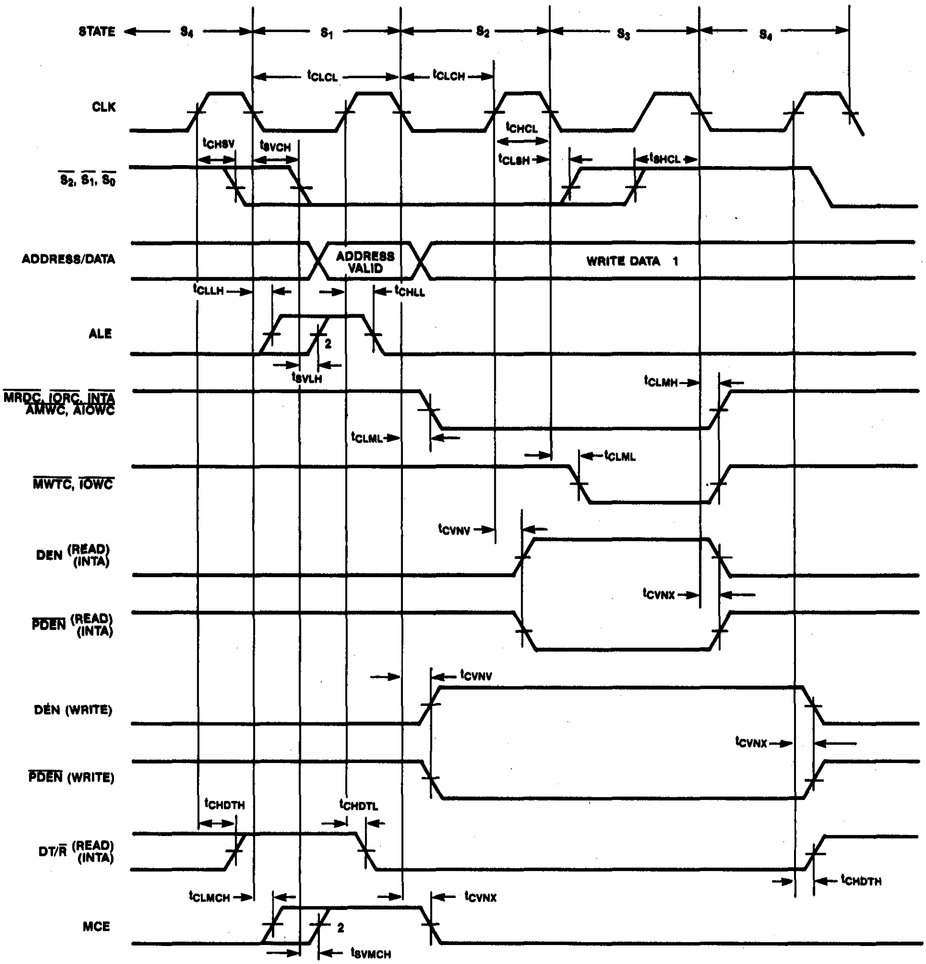
Symbol	Parameter	Test Conditions	Limits (8MHz)		PRELIMINARY Limits (10MHz)		Units
			Min	Max	Min	Max	
t_{AEHCZ}	Command Disable Time	D (Note 2)		40		40	ns
t_{AELCH}	Command Enable Time	C (Note 1)		40		40	ns
t_{AELCV}	Enable Delay Time	B	100	250	100	200	ns
t_{AEVNV}	$\overline{AEN}$ to DEN	A		25		20	ns
t_{CELRH}	CEN to Command	B		t_{CLML}+10		t_{CLML}	ns
t_{CEVNV}	CEN to DEN, $\overline{PDEN}$	A		25		25	ns
t_{CHCL}	CLK High Time		40		30		ns
t_{CHDTH}	Direction Control Inactive Delay	A		30		30	ns
t_{CHDTL}	Direction Control Active Delay	A		50		50	ns
t_{CHLL}	ALE Inactive Delay	A (Note 3)	2	25	2	15	ns
t_{CHSV}	Status Inactive Hold Time		10		10		ns
t_{CLCH}	CLK Low Time		66		50		ns
t_{CLCL}	CLK Cycle Period		125		100		ns
t_{CLLH}	ALE Active Delay (from CLK)	A		20		20	ns
t_{CLMCH}	MCE Active Delay (from CLK)	A		25		20	ns
t_{CLMH}	Command Inactive Delay	B	2	35	2	35	ns
t_{CLML}	Command Active Delay	B	5	35	5	35	ns
t_{CLSH}	Status Active Hold Time		10		10		ns
t_{CVNV}	Control Active Delay	A	2	45	2	45	ns
t_{CVNX}	Control Inactive Delay	A	5	45	5	45	ns
t_{MHNL}	Command Inactive to DEN Low Delay	Command: B, DEN: E	t_{CLCH}-5		t_{CLCH}-5		ns
t_{OHOL}	Output, Fall Time	From 2.0V to 0.8V		15		20	ns
t_{OLOH}	Output, Rise Time	From 0.8V to 2.0V		15		12	ns
t_{SHCL}	Status Inactive Setup Time		35		35		ns
t_{SVCH}	Status Active Setup Time		35		35		ns
t_{SVLH}	ALE Active Delay (from Status)	A		20		20	ns
t_{SVMCH}	MCE Active Delay (from Status)	A		30		20	ns

Refer to Figure 5 for Test Conditions Definition Table.

Notes: 1. t_{AELCH} measurement is between 1.5V and 2.5V.
2. t_{AEHCZ} measured at 0.5V change in V_{OUT}.
3. In 5MHz 80C86/88 systems, minimum ALE HIGH time = t_{CLCL} − (t_{CHSV}(max) + t_{SVLH}) + t_{CHLL}(min) = 74ns.

Figure 3: Timing Diagrams

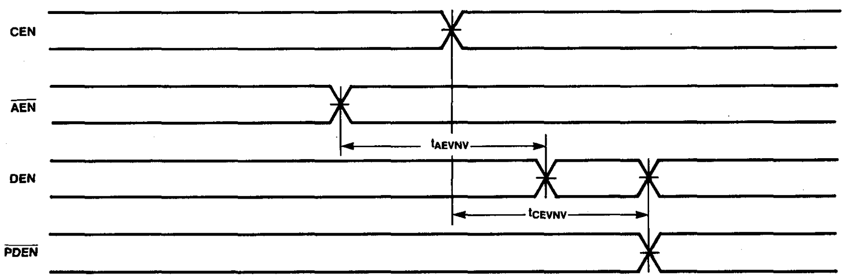
a) Read/Write Timing



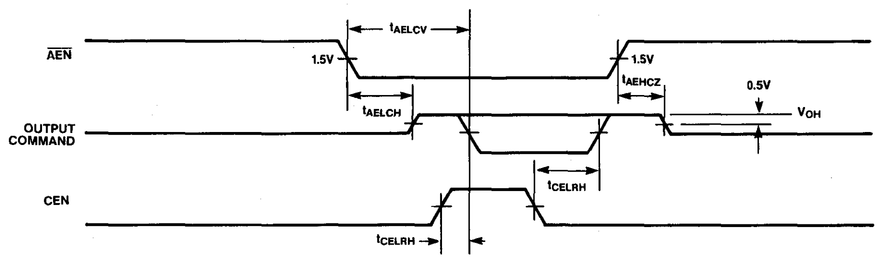
Notes: 1. Address/Data bus is shown only for reference purposes.
2. Leading edge of ALE and MCE is determined by the falling edge of CLK or STATUS going active, whichever occurs last.

Figure 3: Timing Diagrams (Continued)

b) DEN, PDEN Qualification Timing

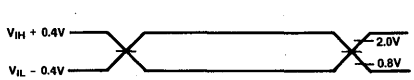


c) Address Enable Timing (3-State Enable/Disable)



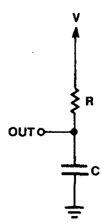
Note: CEN must be LOW or valid prior to S_2 to prevent the command from being generated.

Figure 4: AC Testing I/O Waveform



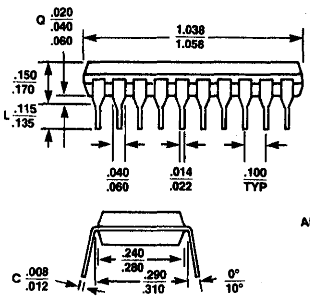
AC Testing: Inputs are driven at V_{IH} + 0.4V for a logic "1", and V_{IL} - 0.4V for a logic "0". The clock is driven at 3.9V and 0.4V. Timing measurements are made at 2.0V and 0.8V. Input rise and fall times should be ≤15ns measured between 0.8V and 2.0V.

Figure 5: Test Load Circuits 3-State Command Output Test Load



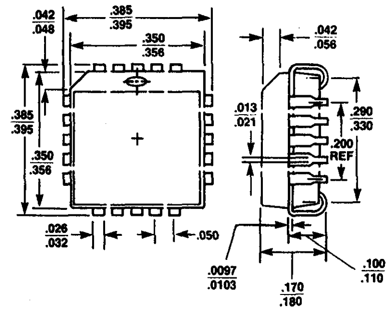
Test Condition	I_{OH}	I_{OL}	V (V)	R (Ω)	C (pF)
A	-4.0mA	+8.0mA	2.13	220	80
B	-8.0mA	+20.0mA	2.29	91	300
C	-8.0mA	—	1.5	187	300
D	-8.0mA	—	1.5	187	50
E	-1.0μA	+1.0μA	2.13	870K	30

PACKAGE DIMENSIONS



ALL DIMENSIONS IN INCHES

Plastic Package



PLCC Package

ORDERING INFORMATION & PRODUCT CODE

KS 82C88 X X X

- **SAMSUNG SEMICONDUCTOR** — KS
- **Part Number** — 82C88
- **Speed**
  - -8 8MHz
  - -10 10MHz
- **Temperature**
  - C — Commercial (0°C to +70°C)
  - I — Industrial (-40°C to +85°C)
- **Packaging**
  - P — Plastic DIP
  - L — Plastic Leaded Chip Carrier (PLCC)

SAMSUNG products are designated by a Product Code. When ordering, please refer to products by their full code. For unusual, and/or specific packaging or processing requirements not covered by the standard product line, please contact the SAMSUNG MOS Products Group.

KS82C284

CLOCK GENERATOR AND READY INTERFACE FOR 80286 MICROPROCESSORS

FEATURES/BENEFITS

- Generates system clock for 80286 processors
- Uses crystal or TTL signal for frequency source
- Provides local READY and IEEE-796 (Multibus®) READY synchronization
- Generates system RESET output from Schmitt trigger input
- Single +5V power supply
- Low power CMOS
- Works with KS82C288 Bus Controller and KS82C289 Bus Arbiter
- 10, 12.5, and 16 MHz versions
- 20-lead PLCC or 18-pin plastic DIP

DESCRIPTION

The KS82C284 clock generator/driver provides clock signals for 80286 processors and support components. It also supplies the READY signal to the CPU from either synchronous or asynchronous sources. The KS82C284 supplies synchronous RESET from an asynchronous input with hysteresis.

Figure 1. KS82C284 Block Diagram

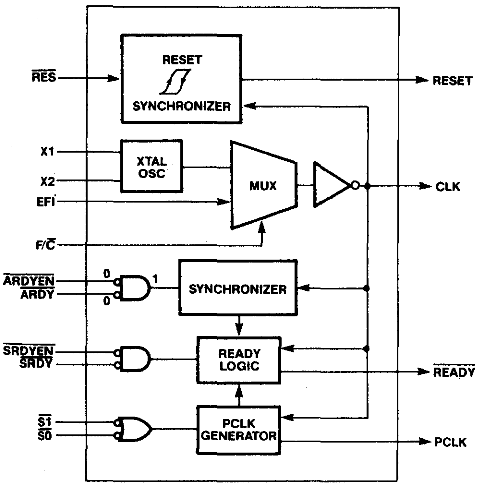


Figure 2a. KS82C284 PLCC Pin Diagram

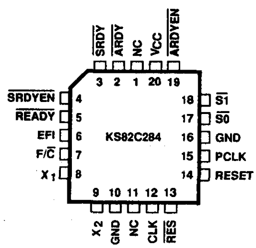


Figure 2b. KS82C284 Plastic DIP Pin Diagram

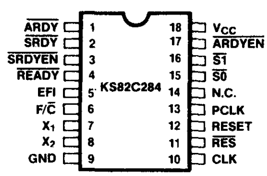


Table 1: KS82C284 Interface Signal Descriptions

Symbol	Type	Name and Function
CLK	O	**System Clock:** This signal is used by the processor and support devices (which must be synchronous with the processor). The frequency of the CLK output is twice the processor's desired internal clock frequency. CLK can drive both TTL- and MOS-level inputs.
F/$\overline{C}$	I	**Frequency/Crystal Select:** This is a strapping option that selects the source for the CLK output. When F/$\overline{C}$ is strapped LOW, the internal crystal oscillator drives CLK. When F/$\overline{C}$ is strapped HIGH, EFI drives the CLK output.
X1, X2	I	**Crystal in 1, Crystal in 2:** A parallel resonant fundamental mode crystal is attached to these pins for the internal oscillator. When F/$\overline{C}$ is LOW, the internal oscillator will drive the CLK output at the crystal frequency. The crystal frequency must be twice the processor's desired internal clock frequency.
EFI	I	**External Frequency In:** This signal drives the CLK when the F/$\overline{C}$ input is strapped HIGH. The EFI input frequency must be twice the processor's desired internal clock frequency.
PCLK	O	**Peripheral Clock:** Provides a 50% duty-cycle clock with 1/2 the frequency of CLK. PCLK will be in phase with the internal processor clock following the first bus cycle after the processor has been reset.
$\overline{ARDYEN}$	I	**Asynchronous Ready Enable:** Qualifies the Asynchronous Ready ($\overline{ARDY}$) input. $\overline{ARDYEN}$ selects $\overline{ARDY}$ as the source of $\overline{READY}$ for the current bus cycle. Inputs to $\overline{ARDYEN}$ may be applied asynchronously to CLK. Setup and hold times must be observed in order to assure a guaranteed response to synchronous inputs.
$\overline{ARDY}$	I	**Asynchronous Ready:** Used to terminate the current bus cycle. The $\overline{ARDY}$ input is qualified by $\overline{ARDYEN}$. Input to $\overline{ARDY}$ may be applied asynchronously to CLK. Setup and hold times must be observed in order to assure a guaranteed response to synchronous outputs.
$\overline{SRDYEN}$	I	**Synchronous Ready Enable:** Qualifies the Synchronous Ready ($\overline{SRDY}$) input. $\overline{SRDYEN}$ selects $\overline{SRDY}$ as the source for $\overline{READY}$ to the CPU for the current bus cycle. Setup and hold times must be observed for proper operation.
$\overline{SRDY}$	I	**Synchronous Ready:** Terminates the current bus cycle. The $\overline{SRDY}$ input is qualified by the $\overline{SRDYEN}$ input. Setup and hold times must be observed for proper operation.
$\overline{READY}$	O	**Ready:** Signals that the current bus cycle is completed. The $\overline{SRDY}$, $\overline{SRDYEN}$, $\overline{ARDY}$, $\overline{ARDYEN}$, $\overline{S1}$, $\overline{S0}$, and $\overline{RES}$ inputs control $\overline{READY}$ as explained in the $\overline{READY}$ generator section of this data sheet. $\overline{READY}$ is an open-drain output requiring an external pull-up resistor.
$\overline{S0}$, $\overline{S1}$	I	**Status 0, Status 1:** These signals prepare the KS82C284 for a subsequent bus cycle. $\overline{S0}$ and $\overline{S1}$ synchronize PCLK to the internal processor clock and control $\overline{READY}$. These inputs have internal pull-up resistors to keep them HIGH if nothing is driving them. Setup and hold times must be observed for proper operation.
RESET	O	**Reset:** Derived from the $\overline{RES}$ input. RESET is used to force the system into an initial state. When RESET is active (HIGH), $\overline{READY}$ will be active (LOW).
$\overline{RES}$	I	**Reset In:** Generates the system reset signal, RESET. Signals to $\overline{RES}$ may be applied asynchronously to CLK. A Schmitt trigger input is provided on $\overline{RES}$ so that an RC circuit can be used to provide a time delay. Setup and hold times must be observed to assure a guaranteed response to synchronous inputs.
V_{CC}	I	5V ± 5%.
GND	I	Ground.

FUNCTIONAL DESCRIPTION

Clock Generator

The CLK output provides the basic timing control for an 80286-based system. CLK has output characteristics sufficient to drive MOS devices. CLK is generated by either an internal crystal oscillator or an external source as selected by the $F/\overline{C}$ strapping option. When $F/\overline{C}$ is LOW, the crystal oscillator drives the CLK output. When $F/\overline{C}$ is HIGH, the EFI drives the CLK output.

The KS82C284 provides a second clock output, PCLK, for peripheral devices. PCLK is CLK divided by two. PCLK has a duty cycle of 50% and MOS output drive characteristics. PCLK is normally synchronized to the internal processor clock.

After RESET, the PCLK signal may be out of phase with the internal processor clock. The $\overline{S0}$ and $\overline{S1}$ signals of the first bus cycle are used to synchronize PCLK to the internal processor clock. The phase of the PCLK output changes by extending its HIGH time beyond one system clock (see waveforms). PCLK is forced HIGH whenever either $\overline{S0}$ or $\overline{S1}$ have been active (LOW) for the two previous CLK cycles. PCLK continues to oscillate when both $\overline{S0}$ and $\overline{S1}$ are HIGH.

Since the phase of the internal processor clock will not change except during RESET, the phase of PCLK will not change except during the first bus cycle after RESET.

Oscillator

The KS82C284 incorporates a linear Pierce oscillator which requires an external parallel-resonant, fundamental mode, crystal. The output of the oscillator is internally buffered. The crystal frequency should be twice the required internal processor clock frequency. The crystal should have a typical load capacitance of 32pF.

X1 and X2 are the oscillator crystal connections. For stable operation of the oscillator, two loading capacitors are recommended, as shown in Table 2.

The sum of the board-capacitance and loading-capacitance should equal the values shown. Stray board capacitances (not including the effect of the loading capacitors or crystal capacitance) should be limited to less than 10pF between the X1 and X2 pins.

Decouple V_{CC} and GND as close to the KS82C284 as possible.

OPERATIONAL DESCRIPTION

CLK Termination

The CLK output has a very fast rise and fall time, so the CLK line be properly terminated at frequencies above 10MHz to avoid signal reflections and ringing. To terminate the CLK, insert a small resistor (typically 10Ω-74Ω) in series with the output, as shown in Figure 3. This type of termination is called series termination. The resistor value plus the circuit output impedance should be made equal to the impedance of the transmission line.

Figure 3. Series Termination

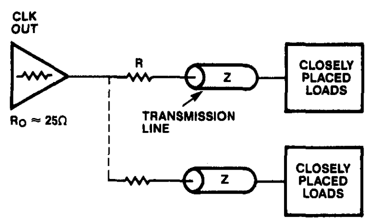


Table 2. KS82C284 Crystal Loading Capacitance Values

Crystal Frequency	C1 Capacitance X1	C2 Capacitance X2
1 to 8 MHz	60pF	40pF
8 to 20 MHz	25pF	15pF
Above 20 MHz	15pF	15pF

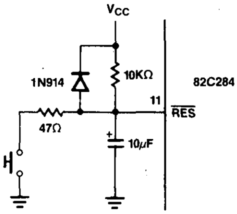
Note: Capacitance values must include stray board-capacitance.

Reset Operation

The reset logic provides the RESET output to force the system into a known, initial state. When the $\overline{RES}$ input is active (LOW), the RESET output goes active (HIGH). $\overline{RES}$ is synchronized internally at the falling edge of CLK before generating the RESET output (see waveforms). Synchronization of the RES input introduces a one- or two-CLK delay before affecting the RESET output.

On power-up, the system's V_{CC} and CLK are unstable. To prevent spurious activity, $\overline{RES}$ should be asserted until V_{CC} and CLK stabilize at their operating values. 80286 processors and support components also require their RESET inputs to be HIGH a minimum of 16 CLK cycles. An RC network, as shown in Figure 4, will keep $\overline{RES}$ LOW long enough to satisfy both the stability and CLK cycle requirements.

Figure 4. Typical RC $\overline{RES}$ Timing Circuit



An internal Schmitt trigger input with hysteresis on $\overline{RES}$ assures a single transition of RESET with an RC circuit on $\overline{RES}$. The hysteresis separates the input voltage-level at which the circuit output switches from HIGH to LOW from the input voltage level at which the circuit output switches from LOW to HIGH. The $\overline{RES}$ HIGH-to-LOW input transition voltage is lower than the $\overline{RES}$ LOW-to-HIGH input transition voltage. As long as the slope of the $\overline{RES}$ input voltage remains in the same direction (increasing or decreasing) around the $\overline{RES}$ input transition voltage, the RESET output will make a single transition.

Ready Operation

The KS82C284 accepts two ready sources for the system $\overline{READY}$ signal which terminates the current bus cycle. Either a synchronous ($\overline{SRDY}$) or an asynchronous ready ($\overline{ARDY}$) source may be used. Each ready input has an enable ($\overline{SRDYEN}$ and $\overline{ARDYEN}$) for selecting the type of ready source required to terminate the current bus cycle. An address decoder would normally select one of the enable inputs.

$\overline{READY}$ is enabled (LOW) if either $\overline{SRDY}$ + $\overline{SRDYEN}$ = 0 or $\overline{ARDY}$ + $\overline{ARDYEN}$ = 0 when sampled by the KS82C284 $\overline{READY}$ generation logic. $\overline{READY}$ will remain active for at least two CLK cycles.

The $\overline{READY}$ output has an open-drain driver allowing other ready circuits to be wire OR'ed with it, as shown in Figure 5. The $\overline{READY}$ signal of an 80286 system requires an external pull-up resistor. To force the $\overline{READY}$ signal inactive (HIGH) at the start of a bus cycle, the $\overline{READY}$ output floats when either $\overline{S0}$ or $\overline{S1}$ are sampled LOW at the falling edge of CLK. Two system clock periods are allowed for the pull-up resistor to pull the $\overline{READY}$ signal to V_{IH}. When RESET is active, $\overline{READY}$ is forced active one CLK later (see waveforms).

Figure 5. Recommended Crystal and $\overline{READY}$ Connections

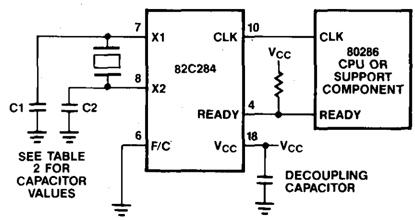


Figure 6 illustrates the operation of $\overline{SRDY}$ and $\overline{SRDYEN}$. These inputs are sampled on the falling edge of CLK when $\overline{S0}$ and $\overline{S1}$ are inactive (HIGH) and PCLK is HIGH. $\overline{READY}$ is forced active when both $\overline{SRDY}$ and $\overline{SRDYEN}$ are sampled as LOW.

Figure 7 shows the operation of $\overline{ARDY}$ and $\overline{ARDYEN}$. These inputs are sampled by an internal synchronizer at each falling edge of CLK. The output of the synchronizer is then sampled when PCLK is HIGH. If the synchronizer resolved both the $\overline{ARDY}$ and $\overline{ARDYEN}$ as active, the $\overline{SRDY}$ and $\overline{SRDYEN}$ inputs are ignored. Either $\overline{ARDY}$ or $\overline{ARDYEN}$ must be HIGH at the end of T_S (see Figure 7).

$\overline{READY}$ remains active until either $\overline{S0}$ or $\overline{S1}$ are sampled LOW, or the ready inputs are sampled as inactive.

Figure 6. Synchronous $\overline{\text{READY}}$ Operation

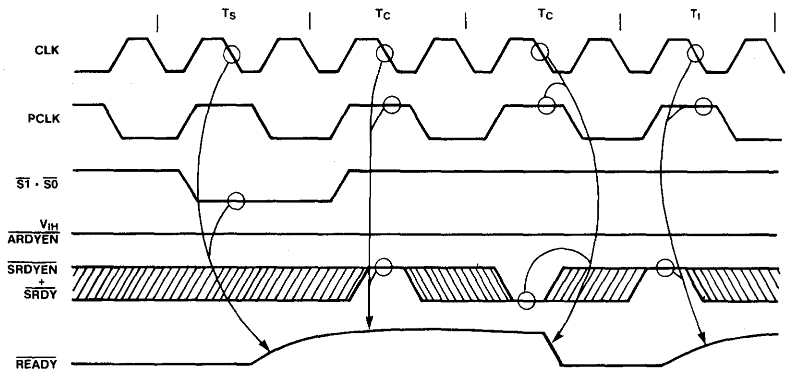
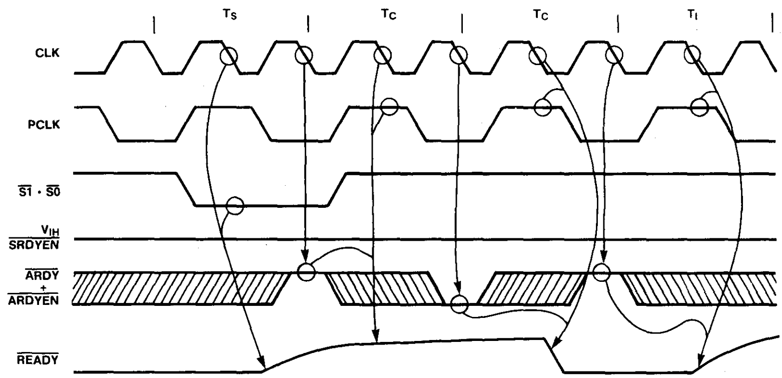


Figure 7. Asynchronous $\overline{\text{READY}}$ Operation



Absolute Maximum Ratings*

Temperature Under Bias .... 0°C to +70°C
Storage Temperature .... -65°C to +150°C
All Output and Supply Voltages .... -0.5V to +7V
All Input Voltages .... -1.0V to +5.5V
Power Dissipation .... 1 Watt

***Note:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTICE: Specifications contained within the following tables are subject to change.

DC Characteristics (T_{CASE} = 0°C to +85°C,* V_{CC} = 5V ± 5%)

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input LOW Voltage			0.8	V
V_{IH}	Input HIGH Voltage		2.0		V
V_{IHR}	$\overline{RES}$ and EFI Input HIGH Voltage		2.6		V
V_{HYS}	$\overline{RES}$ Input Hysteresis		0.25		V
V_{OL}	RESET, PCLK Output LOW Voltage	I_{OL} = 5 mA		0.45	V
V_{OH}	RESET, PCLK Output HIGH Voltage	I_{OH} = -1 mA	2.4		V
		I_{OH} = -0.2 mA	V_{CC}-0.5		V
V_{OLR}	$\overline{READY}$, Output LOW Voltage	I_{OL} = 9 mA		0.45	V
V_{OLC}	CLK Output LOW Voltage	I_{OL} = 5 mA		0.45	V
V_{OHC}	CLK Output HIGH Voltage	I_{OH} = -800 μA	4.0		V
I_{IL}	Input Sustaining Current on $\overline{S0}$ and $\overline{S1}$ Pins	V_{IN} = 0V	30	500	μA
I_{LI}	Input Leakage Current	$0 \leq V_{IN} \leq V_{CC}$(1)		±10	μA
I_{CC}	Power Supply Current	at 32 MHz Output CLK Frequency		75	mA
C_I	Input Capacitance	F_C = 1 MHz		10	pF

*T_A is guaranteed from 0°C to +70°C as long as T_{CASE} is not exceeded.

Note:
1. Status lines $\overline{S0}$ and $\overline{S1}$ excluded because they have internal pull-up resistors.

AC CHARACTERISTICS (V_{CC} = 5V ± 5%, T_{CASE} = 0°C to +85°C*)

Timing are referenced to 0.8V and 2.0V points of signals as illustrated in the datasheet waveforms, unless otherwise noted.

82C284 AC Timing Parameters

No.	Parameter	Test Conditions	8.0 MHz		10.0 MHz		12.5 MHz Preliminary		16.0 MHz Preliminary		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
1	EFI to CLK Delay	At 1.5V[1]		25		25		25		25	ns
2	EFI LOW Time	At 1.5V[1, 7]	28		22.5		13		10		ns
3	EFI HIGH Time	At 1.5V[1, 7]	28		22.5		22		17		ns
4	CLK Period		62	500	50	500	40	500	62	500	ns
5	CLK LOW Time	At 1.0V[1, 2, 7, 8, 9, 10]	15		12		11		9		ns
6	CLK HIGH Time	At 3.6V[1, 2, 7, 8, 9, 10]	25		16		13		10		ns
7	CLK Rise Time	1.0V to 3.6V[1, 2, 10, 11]		10		8		8		6	ns
8	CLK Fall Time	3.6V to 1.0V[1, 9, 10, 11]		10		8		8		6	ns
9	Status Setup Time	(Note 1)	22		—		—		—		ns
9a	Status Setup Time for Status Going Active	(Note 1)	—		20		22		18		ns
9b	Status Setup Time for Status Going Inactive	(Note 1)	—		20		18		14		ns
10	Status Hold Time	(Note 1)	1		1		3		3		ns
11	$\overline{\text{SRDY}}$ or $\overline{\text{SRDYEN}}$ Setup Time	(Note 1)	17		15		15		12		ns
12	$\overline{\text{SRDY}}$ or $\overline{\text{SRDYEN}}$ Hold Time	(Notes 1, 11)	0		0		0		0		ns
13	$\overline{\text{ARDY}}$ or $\overline{\text{ARDYEN}}$ Setup Time	(Notes 1, 3)	0		0		0		0		ns
14	$\overline{\text{ARDY}}$ or $\overline{\text{ARDYEN}}$ Hold Time	(Notes 1, 3)	30		30		25		20		ns
15	$\overline{\text{RES}}$ Setup Time	(Notes 1, 3)	20		20		18		15		ns
16	$\overline{\text{RES}}$ Hold Time	(Notes 1, 3)	10		10		8		6		ns
17	$\overline{\text{READY}}$ Inactive Delay	At 0.8V[4]	5		5		5		5		ns
18	$\overline{\text{READY}}$ Active Delay	At 0.8V[4]	0	24	0	24	0	18	0	15	ns
19	PCLK Delay	(Note 5)	0	45	0	35	0	23	0	18	ns
20	RESET Delay	(Note 5)	5	34	5	27	3	22	3	17	ns
21	PCLK LOW Time	(Notes 5, 6)	t4-20		t4-20		t4-20		t4-20		ns
22	PCLK HIGH Time	(Notes 5, 6)	t4-20		t4-20		t4-20		t4-20		ns

*T_A is guaranteed from 0°C to 70°C as long as T_{CASE} is not exceeded.

Notes:

1. CLK loading: C_L = 100 pF. The 82C284's X_1 and X_2 inputs are designed primarily for parallel-resonant crystals. Serial-resonant crystals may also be used, however, they may oscillate up to 0.01% faster than their nominal frequencies when used with the 82C284. For either type of crystal, capacitive loading should be as specified by Table 2.

Notes:

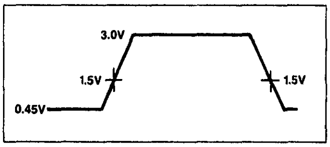
2. With the internal crystal oscillator using recommended crystal and capacitive loading; or with the EFI input meeting specifications t2 and t3. The recommended crystal loading for CLK frequencies of 8 MHz-20 MHz are 25 pF from pin X_1 to ground, and 15 pF from pin X_2 to ground; for CLK frequencies above 20 MHz 15 pF from pin X_1 to ground, and 15 pF from pin X_2 to ground. These recommended values are ±5 pF and include all stray capacitance. Decouple V_{CC} and GND as close to the 82C284 as possible.
3. This is an asynchronous input. This specification is given for testing purposes only, to assure recognition at specific CLK edge.
4. Pull-up resistor values for READY pin:

CPU Frequency	8 MHz	10 MHz	12.5 MHz	16.0 MHz
Resistor	910Ω	700Ω	600Ω	560Ω
C_L	150 pF	150 pF	150 pF	150 pF
I_{OL}	7 mA	7 mA	9 mA	9 mA

5. PCLK and RESET loading: C_L = 75 pF
6. t4 refers to any allowable CLK period.
7. When driving the 82C284 with EFI, provide minimum EFI HIGH and LOW times as follows:

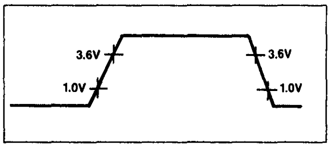
CLK Output Frequency	16 MHz	20 MHz	25 MHz	32 MHz
Min. Required EFI HIGH Time	28 ns	22.5 ns	22 ns	20 ns
Min. Required EFI LOW Time	28 ns	22.5 ns	13 ns	10 ns

Reset Drive EFI Drive and Measurement Points



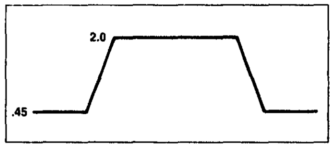
Note 9

CLK Output Measurement Points



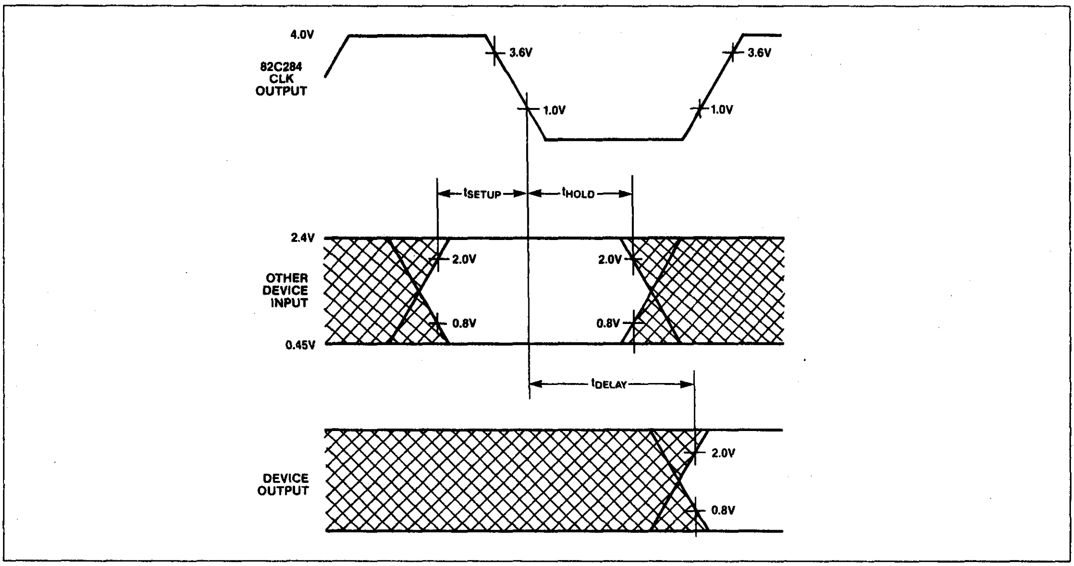
Note 10

F/$\overline{C}$ Drive Points



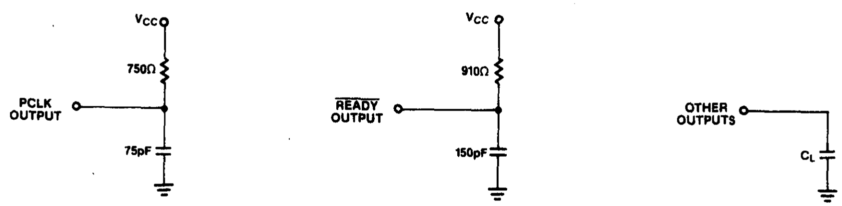
Note 11

AC Setup, Hold and Delay Time Measurement — General



Note 12

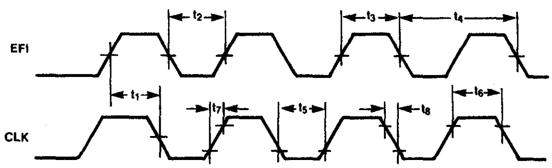
AC Test Loading on Outputs



Note 13

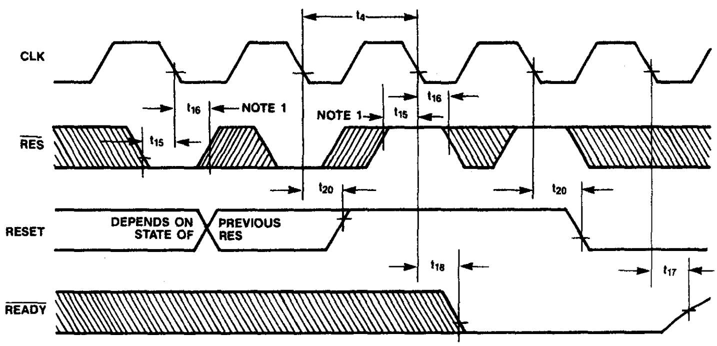
WAVEFORMS

CLK as a Function of EFI



Note:
The EFI input LOW and HIGH times as shown are required to guarantee the CLK LOW and HIGH times shown.

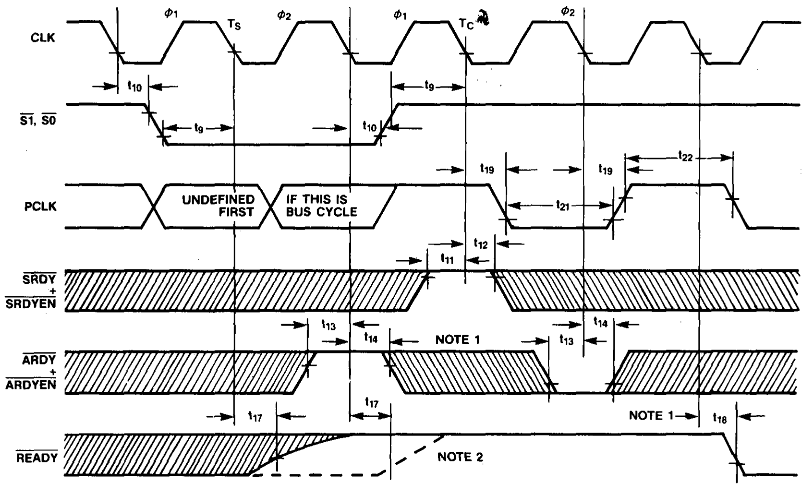
RESET and READY Timing as a Function of RES with S1, S0, ARDY + ARDYEN, and SRDY + SRDYEN High



Note:
1. This is an asynchronous input. The setup and hold times shown are required to guarantee the response shown.

WAVEFORMS (Continued)

$\overline{READY}$ and PCLK Timing with $\overline{RES}$ High

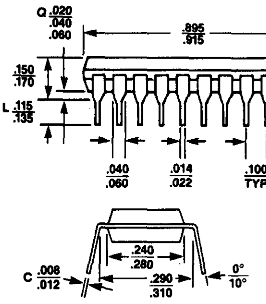


Notes:

1. This is an asynchronous input. The setup and hold times shown are required to guarantee the response shown.
2. If $\overline{SRDY}$ + $\overline{SRDYEN}$ or $\overline{ARDY}$ + $\overline{ARDYEN}$ are active before and/or during the first bus cycle after RESET, $\overline{READY}$ may not be deasserted until the falling edge of $\phi 2$ of T_S.

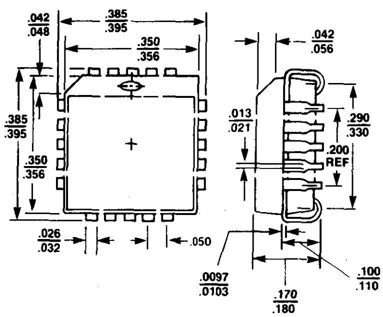
3

PACKAGE DIMENSIONS



18-pin DIP

ALL DIMENSIONS IN INCHES



20-pin PLCC

ORDERING INFORMATION AND PRODUCT CODE

KS 82C284 X X X

- **SAMSUNG SEMICONDUCTOR** — KS
- **Part Number** — 82C284
- **Speed**
  - -8.0 8.0MHz
  - -10.0 10.0MHz
  - -12.5 12.5MHz
  - -16.0 16.0MHz
- **Temperature**
  - C — Commercial (0°C to +70°C)
  - I — Industrial (-40°C to +85°C)
- **Packaging**
  - P — Plastic DIP
  - L — Plastic Leaded Chip Carrier (PLCC)

SAMSUNG products are designated by a Product Code. When ordering, please refer to products by their full code. For unusual, and/or specific packaging or processing requirements not covered by the standard product line, please contact the SAMSUNG MOS Product Group.

KS82C288

BUS CONTROLLER
FOR 80286 MICROPROCESSORS

FEATURES/BENEFITS

- **Provides commands and control for local and system bus in 80286-based machines**
- **Flexible command timing**
- **Works with KS82C289 Bus Arbiter and KS82C284 Clock Generator**
- **Optional IEEE-796 (Multibus®) compatible timing**
- **10, 12.5 and 16 MHz versions**
- **Supports high-speed, non-Multibus systems**
- **Control drivers with 16 mA I_{OL} and 3-state command drivers with 32 mA I_{OL}**
- **Single +5V supply**
- **Low-power CMOS**
- **20-lead PLCC or plastic DIP**

DESCRIPTION

The 20-pin CMOS KS82C288 controls buses in 80286-based computer systems. The Bus Controller provides command and control outputs with flexible timing options. Separate outputs are used for memory and I/O devices. The data bus is controlled with separate direction-control and data-enable signals.

Using a strapping option, the KS82C288 can be used for either Multibus-compatible bus cycles or high-speed bus cycles.

Figure 1. Block Diagram of KS82C288

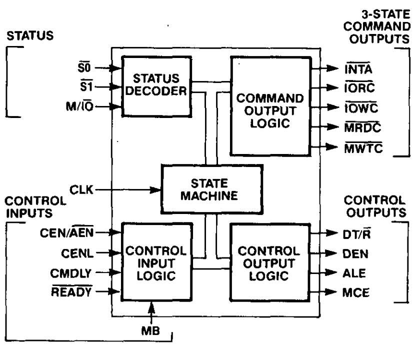


Figure 2a. KS82C288 PLCC Pin Diagram

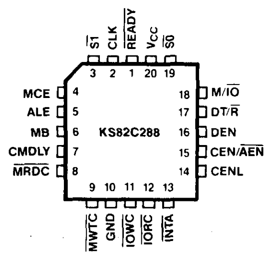


Figure 2b. KS82C288 DIP Pin Diagram

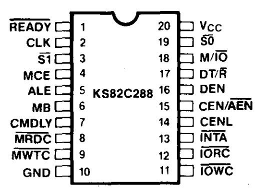


Table 1: KS82C288 Interface Signal Descriptions

<table>
<tr><th>Symbol</th><th>Type</th><th>Name and Function</th></tr>
<tr><td>CLK</td><td>I</td><td>System Clock: Provides the basic timing control for the KS82C288 in an 80286-based system. Its frequency is twice the internal processor clock frequency. The falling edge of CLK establishes when inputs are sampled and command and control outputs change.</td></tr>
<tr><td>$\overline{S0}$, $\overline{S1}$</td><td>I</td><td>Status Signal 0, Status Signal 1: These are bus cycle status signals that, along with M/$\overline{IO}$, start a bus signal and define the type of bus cycle. These signals are active LOW. A bus cycle is started when either $\overline{S0}$ or $\overline{S1}$ is sampled LOW at the falling edge of CLK. Setup and hold times must be met for these signals to operate properly.

There are eight bus cycles defined by $\overline{S0}$, $\overline{S1}$, and M/$\overline{IO}$, as described below:

80286 Bus Cycles
<table>
<tr><th>M/$\overline{IO}$</th><th>$\overline{S1}$</th><th>$\overline{S0}$</th><th>Type of Bus Cycle</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Interrupt Acknowledge</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>I/O Read</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>I/O Write</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>None; Idle</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Halt, or Shutdown</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Memory Read</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Memory Write</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>None; Idle</td></tr>
</table></td></tr>
<tr><td>M/$\overline{IO}$</td><td>I</td><td>Memory or I/O Select: This signal determines whether the current bus cycle is in the memory space or in the I/O space. When LOW, the current bus cycle is in the I/O space. When HIGH, the current bus cycle is in the memory space. Setup and hold times must be met for proper operation.</td></tr>
<tr><td>MB</td><td>I</td><td>Multibus Mode Select: Determines the timing of the command and control outputs. When HIGH, the bus controller operates with Multibus I-compatible timings. When LOW, the bus controller optimizes the command and control output timing for short bus cycles. The function of the CEN/$\overline{AEN}$ pin is selected by this signal.

This input is typically a strapping option and is not dynamically changed.</td></tr>
<tr><td>CENL</td><td>I</td><td>Command Enable Latched: A bus controller select signal which allows the Bus Controller to respond to the current bus cycle being initiated. CENL is an active-HIGH input latched internally at the end of each T_S cycle. CENL is used to select the appropriate bus controller for each bus cycle in a system where the CPU has more than one bus it can use. To select this KS82C288 for all transfers, connect CENL to V_{CC}.

No control inputs affect CENL. Setup and hold times must be met for proper operation.</td></tr>
<tr><td>CMDLY</td><td>I</td><td>Command Delay: CMDLY allows the start of a command to be delayed. If sampled HIGH (active), the command output is not activated and CMDLY is again sampled at the next CLK cycle.

When sampled LOW, the selected command is enabled.

If $\overline{READY}$ is detected LOW before the command output is activated, the KS82C288 will terminate the bus cycle, even if no command was issued. If no delays are required before starting a command, CMDLY should be connected to GND. This input has no effect on KS82C288 control outputs. Setup and hold times must be satisfied for proper operation.</td></tr>
</table>

Table 1: KS82C288 Interface Signal Descriptions (Continued)

Symbol	Type	Name and Function
$\overline{READY}$	I	**Ready:** Indicates the end of the current bus cycle. Multibus I-mode requires at least one wait state to allow the command outputs to become active. $\overline{READY}$ must be active (LOW) during reset to force the KS82C288 into an idle state. Setup and hold times must be satisfied for proper operation. The KS82C284 Clock Generator drives $\overline{READY}$ LOW during RESET.
CEN/$\overline{AEN}$	I	**Command Enable, Address Enable:** Controls the command and DEN outputs of the KS82C288. CEN/$\overline{AEN}$ inputs may be asynchronous to CLK. Setup and hold times must be satisfied to assure a guaranteed response to synchronous inputs. When MB is HIGH, CEN/$\overline{AEN}$ has the $\overline{AEN}$ function. Active LOW, $\overline{AEN}$ indicates that the CPU has been granted the use of a shared bus and the bus controller command outputs may exit 3-state OFF and become inactive (HIGH). $\overline{AEN}$ HIGH indicates that the CPU does not have control of the shared bus and forces the command outputs into 3-state OFF and DEN inactive (LOW). When MB is LOW, this input has the CEN function. CEN is unlatched active HIGH input which allows the Bus Controller to activate its command and DEN outputs. With MB LOW, CEN LOW forces the command and DEN outputs inactive but does not tristate them. This input may be connected to V_{CC} or to GND.
ALE	O	**Address Latch Enable:** This signal controls the address latches used to hold an address stable during a bus cycle. ALE will not be issued for the halt bus cycle and is not affected by any of the control inputs.
MCE	O	**Master Cascade Enable:** Signals that a cascade address from a master KS82C59A interrupt controller may be placed onto the CPU address bus for latching by the address latches under ALE control. The CPU's address bus may then be used to broadcast the cascade address to slave interrupt controllers so only one of them will respond to the interrupt acknowledge cycle. MCE is only active during interrupt acknowledge cycles and is not affected by any control input. Using MCE to enable cascade address drivers requires latches which save the cascade address on the falling edge of ALE.
DEN	O	**Data Enable:** Controls when the data transceivers connected to the local data bus are enabled. DEN is delayed for write cycles in the Multibus I-mode.
DT/$\overline{R}$	O	**Data Transmit/Receive:** Establishes the direction of data flow to or from the local data bus. When HIGH, this control output indicates that a write bus cycle is being performed. When LOW, a read bus cycle is being performed. DEN is always inactive when DT/$\overline{R}$ changes states. This output is HIGH when no bus cycle is active. DT/$\overline{R}$ is not affected by any of the control inputs.
$\overline{IOWC}$	O	**I/O Write Command:** Instructs and I/O device to read the data on the data bus. The MB and CMDLY inputs control when this output becomes active. $\overline{READY}$ controls when this output becomes inactive.
$\overline{IORC}$	O	**I/O Read Comand:** Instructs an I/O device to place data onto the data bus. The MB and CMDLY inputs control when this output becomes active. $\overline{READY}$ controls when this output becomes inactive.
$\overline{MWTC}$	O	**Memory Write Command:** Instructs a memory device to read the data on the data bus. The MB and CMDLY inputs control when this output becomes active. $\overline{READY}$ controls when it becomes inactive.

Table 1: KS82C288 Interface Signal Descriptions (Continued)

Symbol	Type	Name and Function
MRDC	O	**Memory Read Command:** Instructs the memory device to place data onto the data bus. The MB and CMDLY inputs control when this output becomes active. READY controls when it becomes inactive.
INTA	O	**Interrupt Acknowledge:** Tells an interrupting device that its interrupt request is being acknowledged. The MB and CMDLY inputs control when this output becomes active. READY controls when it becomes inactive.
V_{CC}	—	5V ± 5%.
GND	—	Ground.

Table 2. Command and Control Outputs for Each Type of Bus Cycle

Type of Bus Cycle	M/IO	S1	S0	Command Activated	DT/R State	ALE, DEN Issued?	MCE Issued?
Interrupt Acknowledge	0	0	0	INTA	LOW	Yes	Yes
I/O Read	0	0	1	IORC	LOW	Yes	No
I/O Write	0	1	0	IOWC	HIGH	Yes	No
None; Idle	0	1	1	None	HIGH	No	No
Halt/Shutdown	1	0	0	None	HIGH	No	No
Memory Read	1	0	1	MRDC	LOW	Yes	No
Memory Write	1	1	0	MWTC	HIGH	Yes	No
None; Idle	1	1	1	None	HIGH	No	No

FUNCTIONAL DESCRIPTION

The KS82C288 Bus Controller provides 80286-based systems with address latch control, data transceiver control, and standard level-type command outputs. The Bus Controller can drive either IEEE-796 Multibus I buses or non-IEEE-796 buses. Command outputs have sufficient drive capabilities for large TTL buses.

A special Multibus I mode is provided to satisfy the address/data setup and hold time requirements of the IEEE-796 Standard.

Command timing may be tailored to special needs through the Bus Controller's CMDLY input (to determine the start of a command) and READY (to determine the end of a command).

Connection to multiple buses is supported with a latched enable input (CENL). An external address decoder can determine which, if any, Bus Controller should be enabled for the bus cycle. The CENL input is latched to allow the address decoder to take advantage of pipelined timing on the 80286 local bus.

Buses shared by several Bus Controllers are supported. The KS82C288's AEN input prevents the Bus Controller from driving the shared-bus command and data signals except when enabled by an external bus arbiter such as the KS82C289.

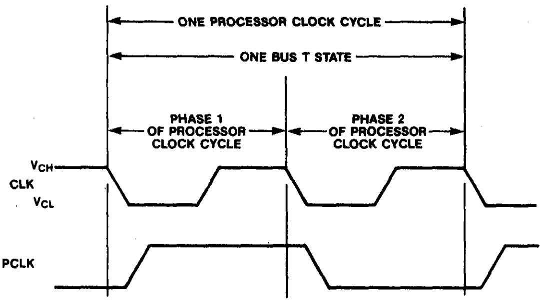
Data transceivers for all the buses are controlled by separate DEN and DT/R outputs. Bus contention is eliminated by disabling DEN before changing DT/R. DEN timing allows enough time for tri-state bus-drivers to enter 3-state OFF before allowing other drivers onto the same bus.

CPU refers to any 80286 processor or 80286 support component which may become an 80286 bus master and thereby drive the KS82C288 status inputs S0, S1, and M/IO.

OPERATIONAL DESCRIPTION

Any CPU driving the local bus uses and internal clock which is one half the frequency of the system clock (CLK). One 80286 processor bus cycle is equal to one bus T-state (see Figure 3). The local bus master informs the Bus Controller of its internal clock phase when it asserts the status signals. Status signals are always asserted at the beginning of Phase 1 of the local bus master's internal clock.

Figure 3. CLK Relationship to the Processor Clock and Bus T-States



KS82C288 Bus States

The KS82C288 has three bus states (see Figure 4). The three bus states are: Idle (T_I), Status (T_S), and Command (T_C). Each bus state is two CLK cycles long.

The T_I bus state occurs when no bus cycle is currently active on the 80286 local bus. This state may be repeated indefinitely. When control of the local bus is being passed between masters, the bus remains in the T_I state.

KS82C288 Bus Cycles

The $\overline{S0}$ and $\overline{S1}$ inputs from the master processor signal the start of a bus cycle. When either input goes LOW, a bus cycle is started. The T_S bus state is defined to be the two CLK cycles during which either $\overline{S0}$ or $\overline{S1}$ are active (see Figure 5). These inputs are sampled by the KS82C288 at every falling edge of CLK. When either $\overline{S0}$ or $\overline{S1}$ are sampled LOW, the next CLK cycle is considered the second phase of the internal CPU clock cycle.

The local bus enters the T_C bus state after the T_S state. The shortest bus cycle may have one T_S state and one T_C state. Longer bus cycles are formed by repeating the T_C state after the T_S state. A repeated T_C bus state is called a wait state.

The $\overline{READY}$ input determines whether the current T_C bus state will be repeated. The $\overline{READY}$ input has the same timing and effect for all bus cycles. $\overline{READY}$ is sampled at the end of each T_C bus state to see if it is active. If sampled HIGH, the T_C bus state is repeated to insert a wait state. Control and command outputs do not change during wait states.

When $\overline{READY}$ is sampled LOW, the current bus cycle is terminated.

The Bus Controller may enter the T_S bus state directly from T_C if the status lines are sampled active (LOW) at the next falling edge of CLK.

Figure 4. KS82C288 Bus States

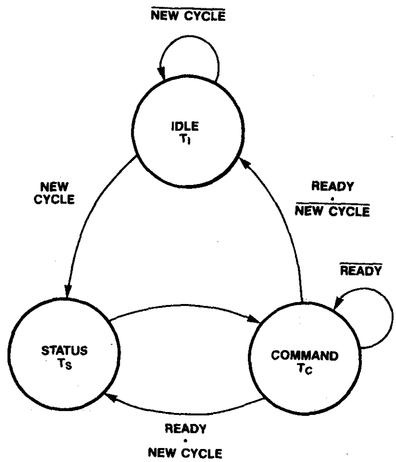
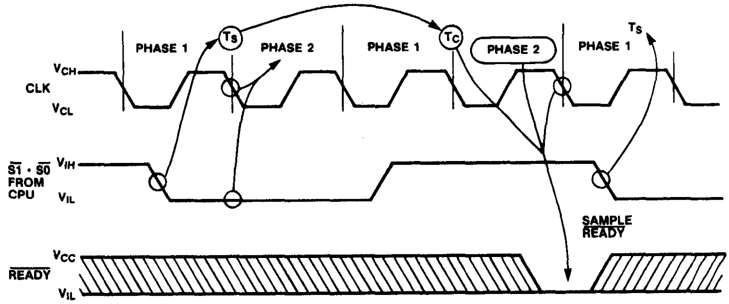


Figure 5. Bus Cycle Definition



Figures 6 through 10 show the basic command and control output timing for read and write bus cycles including the basic idle-read-idle and idle-write-idle bus cycles. Halt bus cycles are not shown because they activate no outputs.

The signal label CMD represents the appropriate command output for the bus cycle.

For figures 6 through 10, the CMDLY input is connected to GND and CENL is connected to V_{CC}. The effects of CENL and CMDLY are described in the section on control inputs.

Figures 6, 7, and 8 show non-Multibus I cycles. MB is connected to GND and CEN is connected to V_{CC} in non-Multibus cycles. Figure 6 shows a read cycle with no wait states while figure 7 shows a write cycle with one wait state. The READY input is shown to illustrate how wait states are added.

Figure 6. Idle-Read-Idle Bus Cycles with MB = 0

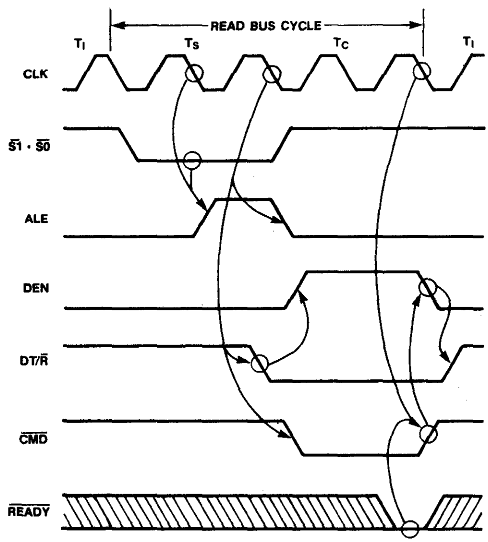


Figure 7. Idle-Write-Idle Bus Cycles with MB = 0

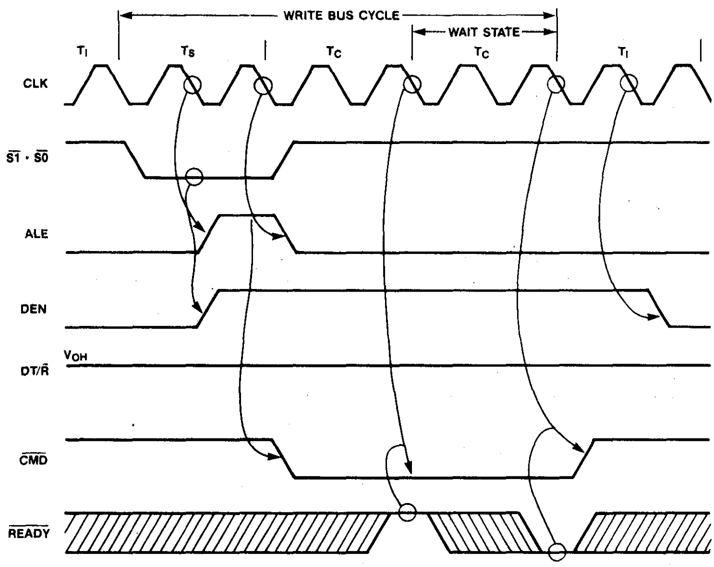
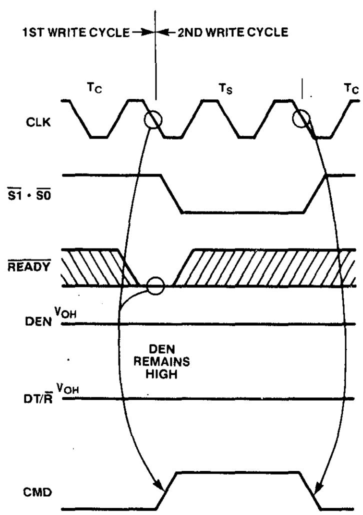


Figure 8. Write-Write Bus Cycles with MB = 0



Bus cycles can occur back-to-back with no T_I bus states between T_C and T_S. Back-to-back cycles do not affect the timing of the command and control outputs. Command and control outputs always match the states shown for the same clock edge (within T_S, T_C) or falling bus state of a bus cycle.

A special case in control timing occurs for back-to-back write cycles when MB = 0 (non-Multibus mode). In this case, DT/R̄ and DEN remain HIGH between the bus cycles (see Figure 8). The command and ALE output timings do not change.

Figures 9 and 10 show a Multibus cycle (MB = 1). AEN and CMDLY are connected to GND. The effects of CMDLY and AEN are described in the section on control inputs. Figure 9 shows a read cycle with one wait state and Figure 10 shows a write cycle with two wait states. The second wait state of the write cycle is not required and is shown only for example. The READY input shows how wait states are added.

Figure 9. Idle-Read-Idle Bus Cycles with 1 Wait State and with MB = 1

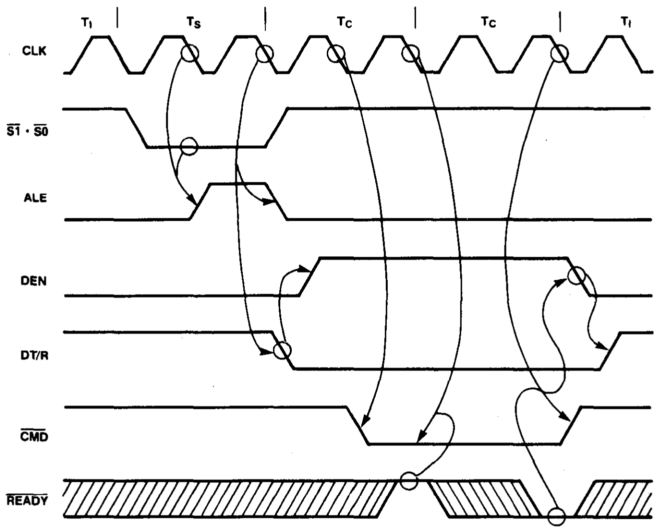
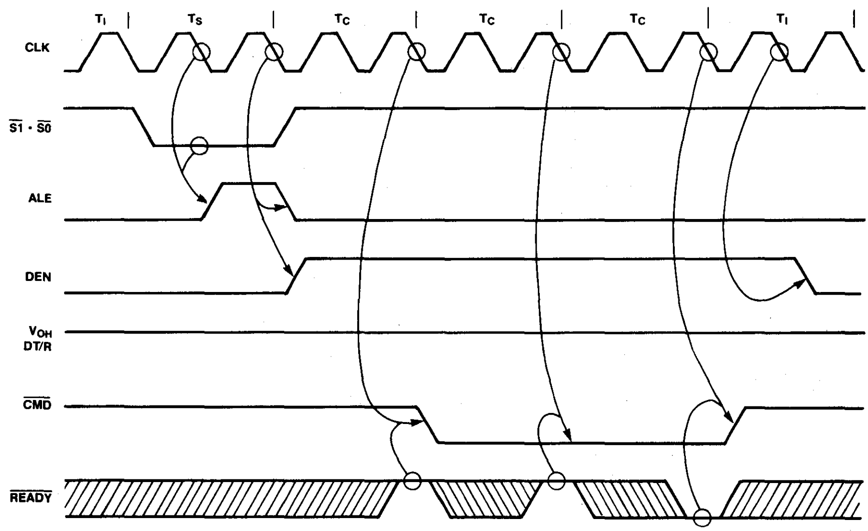


Figure 10. Idle-Write-Idle Bus Cycles with 2 Wait States in Multibus Mode (MB = 1)



The MB control input affects the timing of the command and DEN outputs. These outputs are automatically delayed in Multibus 1 mode to satisfy three requirements:

1) 50 ns minimum setup time for valid address before any command output becomes active
2) 50 ns minimum setup time for valid write data before any write command output becomes active
3) 65 ns maximum time from when any read command becomes inactive until the slave's read data drivers reach 3-state OFF.

Three signal transitions are delayed by MB = 1:

1) The HIGH-to-LOW transition of the read command outputs ($\overline{IORC}$, $\overline{MRDC}$, and $\overline{INTA}$) are delayed by one CLK cycle
2) The HIGH-to-LOW transition of the write command outputs ($\overline{IOWC}$ and $\overline{MWTC}$) are delayed by two CLK cycles.
3) The LOW-to-HIGH transition of DEN for write cycles is delayed one CLK cycle.

Back-to-back bus cycles with MB = 1 do not change the timing of any of the command or control outputs. DEN always becomes inactive between bus cycles with MB = 1.

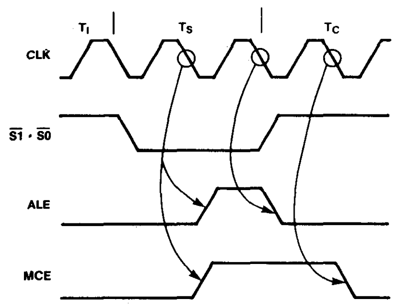
ALE will be issued during the second half of T_S for any bus cycle except for a halt (shutdown) bus cycle. ALE becomes inactive at the end of T_S to allow latching the address to keep it stable during the entire bus cycle. The address outputs may change during Phase 2 of any T_C bus state. ALE is not affected by any control input.

Figure 11 shows how MCE is timed during Interrupt Acknowledge ($\overline{INTA}$) bus cycles. MCE is one CLK cycle longer than ALE to hold the cascade address from a master KS82C59A Programmable Interrupt Controller valid after the falling edge of ALE. With the exception of the MCE control output, an $\overline{INTA}$ bus cycle is identical in timing to a read bus cycle. MCE is not affected by any control input.

Control Inputs

The control inputs (CENL, CMDLY, $\overline{READY}$, CEN/$\overline{AEN}$) can alter the basic timing of command outputs, allow interfacing to multiple buses, and share a bus between different masters. In many 80286-based systems, each CPU has more than one bus which may be used to perform a bus cycle. Normally, a CPU will have only one Bus Controller active for each bus cycle. Some buses may be shared by more than one CPU, as in Multibus configurations, requiring only one of them to use the bus at a time.

Figure 11. MCE Operation for an $\overline{INTA}$ Bus Cycle



Systems with multiple and shared buses use two control input signals from the KS82C288 bus controller, CENL and $\overline{AEN}$ (see figure 12). CENL enables the Bus Controller to control the current bus cycle. The $\overline{AEN}$ input prevents a bus controller from driving its command outputs. $\overline{AEN}$ HIGH means that another bus controller may be driving the shared bus.

Figure 12 shows two buses: a local bus and a Multibus I. Only one bus is used for each CPU bus cycle. The CENL inputs of the Bus Controller select which bus controller is to perform the bus cycle. An address decoder determines which bus to use for each bus cycle. The Bus Controller connected to the shared Multibus I must be selected by CENL and be given access to the Multibus I by $\overline{AEN}$ before it will begin a Multibus I operation.

CENL must be sampled HIGH at the end of the bus state (see waveforms) to allow the bus controller to activate its command and control outputs. If sampled LOW, the commands and DEN will not go active and DT/$\overline{R}$ will remain HIGH. In this situation, the Bus Controller will ignore the CMDLY, CEN, and $\overline{READY}$ inputs until another bus cycle is started via $\overline{S0}$ and $\overline{S1}$. Since an address decoder is commonly used to identify which bus is required for each bus cycle, CENL is latched internally, so the input does not have to be latched.

The CENL input can affect the DEN control output. When MB = 0, DEN normally becomes active during Phase 2 of T_S in write bus cycles. This transition occurs before CENL is sampled. If CENL is sampled LOW, then the DEN output will be forced LOW during T_C as shown in the timing waveforms.

When MB = 1, CEN/$\overline{AEN}$ becomes $\overline{AEN}$. $\overline{AEN}$ controls when the Bus Controller command outputs enter and exit 3-state OFF. $\overline{AEN}$ should be driven by a Multibus I type bus arbiter such as the KS82C289, which assures only one bus controller is driving the shared bus at any one time.

When $\overline{\text{AEN}}$ makes a LOW-to-HIGH transition, the command outputs immediately enter 3-state OFF and DEN is forced inactive. An inactive DEN should force the local data transceivers connected to the shared data bus into 3-state OFF (see figure 12). The LOW-to-HIGH transition of $\overline{\text{AEN}}$ should occur during T_I or T_S bus states.

The HIGH-to-LOW transition of $\overline{\text{AEN}}$ signals that the Bus Controller may now drive the shared bus command signals. Since a bus cycle may be active or be in the process of starting, $\overline{\text{AEN}}$ can become active during any T-state. $\overline{\text{AEN}}$ LOW immediately allows DEN to go to the appropriate state. Three CLK edges later, the command outputs will go active (see timing waveforms). The Multibus I requires this delay for the address and data to be valid on the bus before the command becomes active.

When MB = 0 (non-Multibus mode), CEN/$\overline{\text{AEN}}$ becomes CEN. CEN is an asynchronous input which immediately affects the command and DEN outputs. When CEN makes a HIGH-to-LOW transition, the commands and DEN are immediately forced inactive. When CEN makes a LOW-to-HIGH transition, the commands and DEN outputs immediately go to the appropriate state (see timing waveforms). $\overline{\text{READY}}$ must still become active to terminate a bus cycle if CEN remains LOW for a selected bus controller (CENL was latched HIGH).

Some memory or I/O systems may require more address or write data setup time than provided by the basic command output timing. To provide flexible command timing, the CMDLY input can delay the activation of command outputs. The CMDLY input must be sampled LOW to activate the command outputs. CMDLY does not affect the control outputs ALE, MCE, DEN, and DT/$\overline{\text{R}}$.

CMDLY is first sampled on the falling edge of the CLK ending T_S. If sampled HIGH, the command output is not activated, and CMDLY is again sampled on the next falling edge of CLK. Once sampled LOW, the proper command output becomes active immediately if MB = 0. If MB = 1, the proper command goes active no earlier than shown in figures 9 and 10.

$\overline{\text{READY}}$ can terminate a bus cycle before CMDLY allows a command to be issued. When $\overline{\text{READY}}$ does terminate a bus cycle before CMDLY allows a command to be issued, no commands are issued and the bus controller deactivates DEN and DT/$\overline{\text{R}}$ in the same manner as if a command had been issued.

Waveforms

The waveforms show the timing relationships of inputs and outputs. They do not show all possible transitions of all signals in all modes. Instead, all signal timing relationships are shown through general cases. Special cases are shown when necessary. Most functional descriptions of the KS82C288 are provided in figures 5 through 11, but the waveforms also provide some functional descriptions of the KS82C288.

To find the timing specification for a signal transition in a particular mode, first look for a special case in the waveforms. If no special case applies, then use a timing specification for the same or related function in another mode.

Figure 12. System Use of AEN and CENL

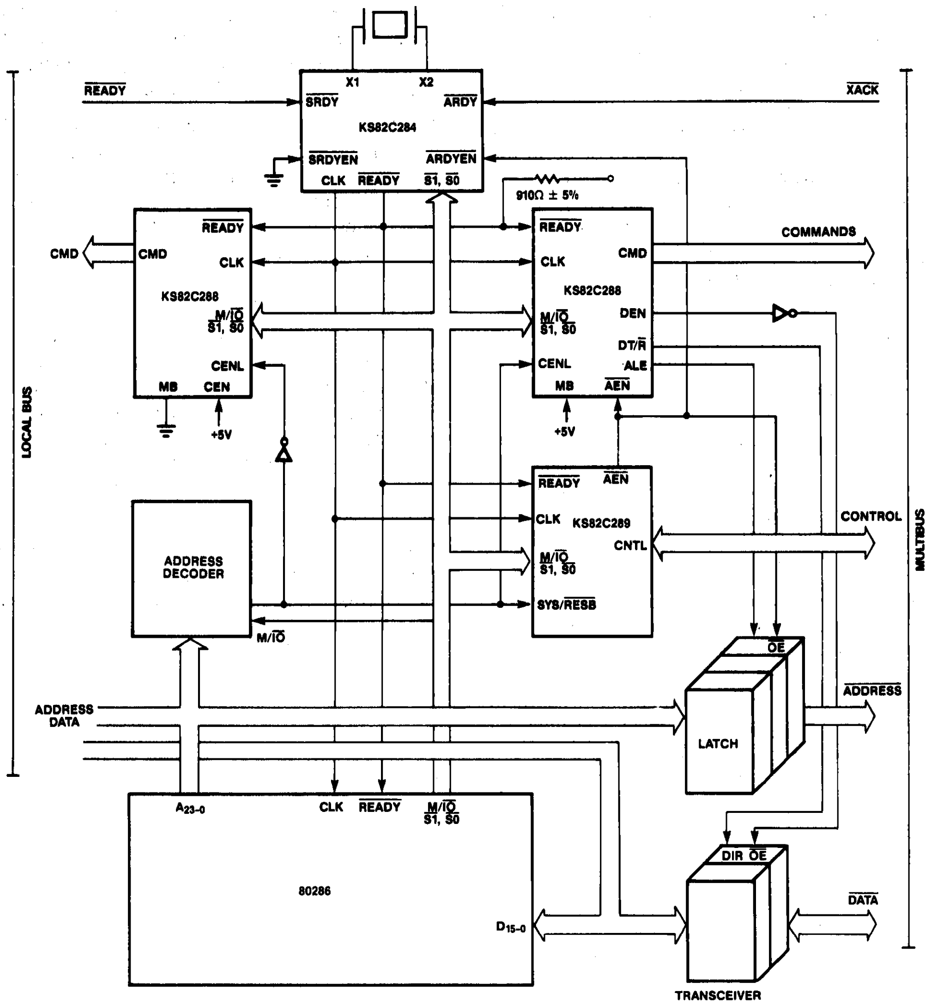


Table 3: Recommended Operating Conditions

DC Supply Voltage		+4.0V to +6.0V
Operating Temperature Range	Commercial	0°C to 70°C
	Industrial	-40°C to +85°C

Table 4: Absolute Maximum Ratings

DC Supply Voltage	+7.0V
Input, Output or I/O Voltage Applied	V_{SS}-0.5V to V_{CC}+0.5V
Storage Temperature Range	-65°C to +150°C
Maximum Package Power Dissipation	1W

Note: Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

3

Table 5: DC Characteristics (T_A = 0°C to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{IL}	Input LOW Voltage		−0.5	0.8	V
V_{IH}	Input HIGH Voltage		2.0	V_{CC} + 0.5	V
V_{ILC}	CLK Input LOW Voltage		−0.5	0.6	V
V_{IHC}	CLK Input HIGH Voltage		3.8	V_{CC} + 0.5	V
V_{OL}	Output LOW Voltage Command Outputs Control Outputs	 I_{OL} = 32 mA (Note 1) I_{OL} = 16 mA (Note 2)		 0.45 0.45	 V V
V_{OH}	Output HIGH Voltage Command Outputs Control Outputs	 I_{OH} = -5 mA (Note 1) I_{OH} = −1 mA (Note 1) I_{OH} = −1 mA (Note 2) I_{OH} = −0.2 mA (Note 2)	 2.4 V_{CC} - 0.5 2.4 V_{CC} - 0.5		 V V V V
I_{IL}	Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$		±10	μA
I_{LO}	Output Leakage Current	$0.45V \leq V_{OUT} \leq V_{CC}$		±10	μA
I_{CC}	Power Supply Current			75	mA
I_{CCS}	Power Supply Current (Static)	(Note 3)		1	mA
C_{CLK}	CLK Input Capacitance	F_C = 1 MHz		12	pF
C_I	Input Capacitance	F_C = 1 MHz		10	pF
C_O	Input/Output Capacitance	F_C = 1 MHz		20	pF

* T_A is guaranteed from 0°C to +70°C as long as T_{CASE} is not exceeded.

Notes:
1. Command Outputs are $\overline{INTA}$, $\overline{IORC}$, $\overline{IOWC}$, $\overline{MRDC}$ and MWRC.
2. Control Outputs are DT/$\overline{R}$, DEN, ALE and MCE.
3. Tested while outputs are unloaded, and inputs at V_{CC} or V_{SS}.

Table 6: AC Characteristics (T_A = 0°C to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Symbol	Parameter	Test Condition	8 MHz		10 MHz		12.5 MHz		16 MHz (Preliminary)		Unit
			-8 Min	-8 Max	-10 Min	-10 Max	-12 Min	-12 Max	-16 Min	-16 Max	
1	CLK Period		62	250	50	250	40	250	62	250	ns
2	CLK HIGH Time	at 3.6V	20		16		13		10		ns
3	CLK LOW Time	at 1.0V	15		12		11		9		ns
4	CLK Rise Time	1.0V to 3.6V		10		8		8		6	ns
5	CLK Fall Time	3.6V to 1.0V		10		8		8		6	ns
6	M/$\overline{IO}$ and Status Setup Time		22		18		15		12		ns
7	M/$\overline{IO}$ and Status Hold Time		1		1		1		1		ns
8	CENL Setup Time		20		15		15		15		ns
9	CENL Hold Time		1		1		1		1		ns
10	$\overline{READY}$ Setup Time		38		26		18		14		ns
11	$\overline{READY}$ Hold Time		25		25		20		16		ns
12	CMDLY Setup Time		20		15		15		12		ns
13	CMDLY Hold Time		1		1		1		1		ns
14	$\overline{AEN}$ Setup Time	(Note 3)	20		15		15		12		ns
15	$\overline{AEN}$ Hold Time	(Note 3)	0		0		0		0		ns
16	ALE, MCE Active Delay from CLK	(Note 4)	3	20	3	16	3	16	3	13	ns
17	ALE, MCE Inactive Delay from CLK	(Note 4)		25		19		19		15	ns
18	DEN (Write) Inactive from CENL	(Note 4)		35		23		23		18	ns
19	DT/$\overline{R}$ LOW from CLK	(Note 4)		25		23		23		18	ns
20	DEN (Read) Active from DT/$\overline{R}$	(Note 4)	5	35	5	21	5	21	5	17	ns
21	DEN (Read) Inactive Delay from CLK	(Note 4)	3	35	3	21	3	19	3	15	ns
22	DT/$\overline{R}$ HIGH from DEN Inactive	(Note 4)	5	35	5	20	5	18	5	14	ns
23	DEN (Write) Active Delay from CLK	(Note 4)		30		23		23		18	ns
24	DEN (Write) Inactive Delay from CLK	(Note 4)	3	30	3	19	3	19	3	15	ns
25	DEN Inactive from CEN	(Note 4)		35		25		25		20	ns
26	DEN Active from CEN	(Note 4)		30		24		24		19	ns
27	DT/$\overline{R}$ HIGH from CLK (when CEN = LOW)	(Note 4)		35		25		25		20	ns
28	DEN Active from $\overline{AEN}$	(Note 4)		30		26		26		20	ns

Table 6: AC Characteristics (T_A = 0°C to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V) (Continued)

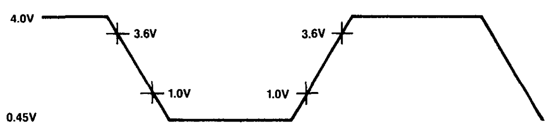
Symbol	Parameter	Test Condition	8 MHz -8 Min	8 MHz -8 Max	10 MHz -10 Min	10 MHz -10 Max	12.5 MHz -12 Min	12.5 MHz -12 Max	16 MHz (Preliminary) -16 Min	16 MHz (Preliminary) -16 Max	Unit
29	$\overline{\text{CMD}}$ Active Delay from CLK	(Note 5)	3	25	3	21	3	21	3	17	ns
30	$\overline{\text{CMD}}$ Inactive Delay from CLK	(Note 5)	5	20	5	20	5	20	5	16	ns
31	$\overline{\text{CMD}}$ Active from CEN	(Note 5)		25		25		25		20	ns
32	$\overline{\text{CMD}}$ Inactive from CEN	(Note 5)		25		25		25		20	ns
33	$\overline{\text{CMD}}$ Inactive Enable from $\overline{\text{AEN}}$	(Note 5)		40		40		40		35	ns
34	$\overline{\text{CMD}}$ Float Delay from $\overline{\text{AEN}}$	(Note 6)		40		40		40		35	ns
35	MB Setup Time		20		20		20		20		ns
36	MB Hold Time		0		0		0		0		ns
37	Command Inactive Enable from MB↓	(Note 5)		40		40		40		35	ns
38	Command Float Time from MB↑	(Note 6)		40		40		40		35	ns
39	DEN Inactive from MB↑	(Note 4)		30		26		26		20	ns
40	DEN Active from MB↓	(Note 4)		30		30		30		24	ns

*T_A is guaranteed from 0°C to +70°C as long as T_{CASE} is not exceeded.

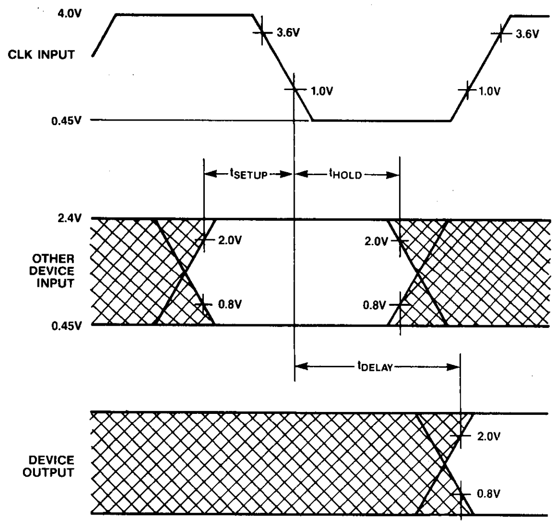
Notes:

3. $\overline{\text{AEN}}$ is an asynchronous input. This specification is for testing purposes only, to assure recognition at a specific CLK edge.
4. Control output load: CL = 150 pF.
5. Command output load: CL = 300 pF.
6. Float condition occurs when output current is less than I_{LO} in magnitude.
7. AC Drive and Measurement Points — CLK Input
8. AC Setup, Hold and Delay Time Measurement — General
9. AC Test Loading on Outputs

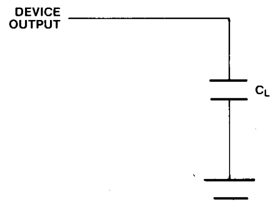
Note 7: AC Drive and Measurement Points — CLK Input



Note 8: AC Setup, Hold and Delay Time Measurement — General

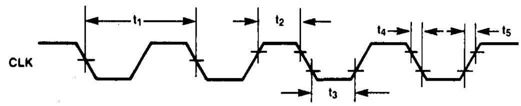


Note 9: AC Test Loading on Outputs

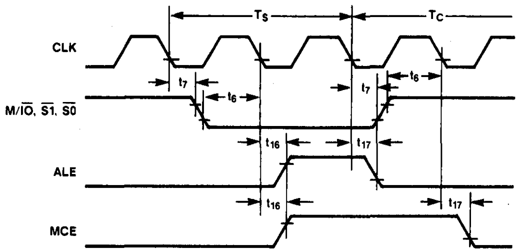


WAVEFORMS

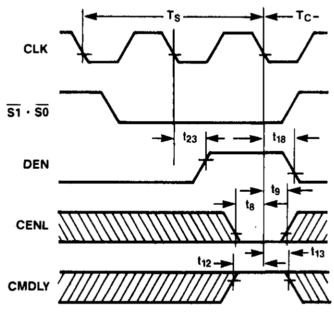
CLK Characteristics



Status, ALE, MCE Characteristics

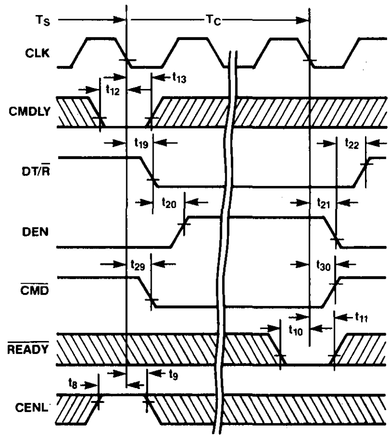


CENL, CMDLY, DEN Characteristics with MB = 0 and CEN = 1 During Write Cycle

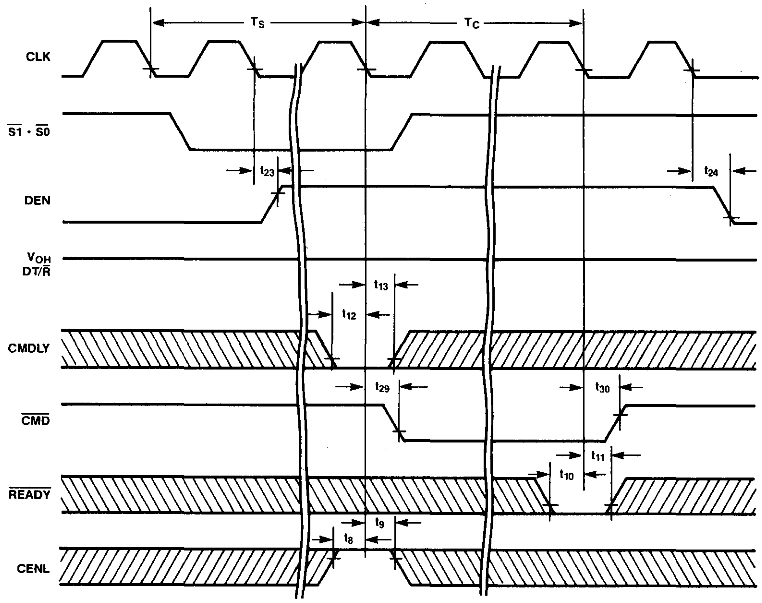


WAVEFORMS (Continued)

Read Cycle Characteristics with MB = 0 and CEN = 1

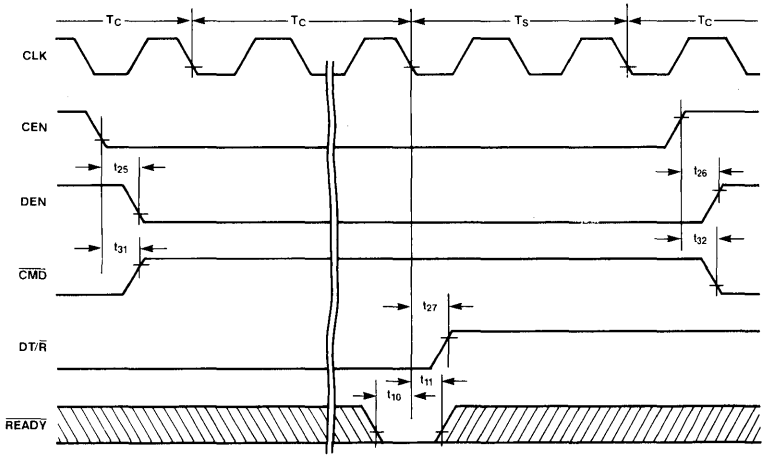


Write Cycle Characteristics with MB = 0 and CEN = 1

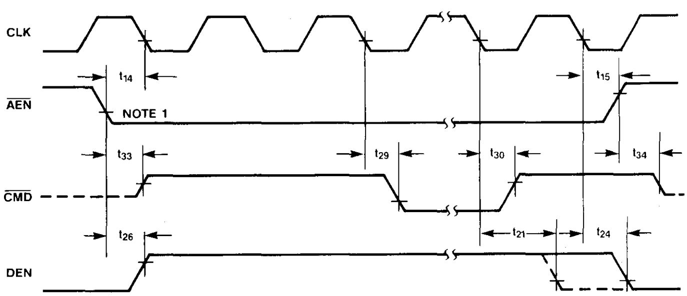


WAVEFORMS (Continued)

CEN Characteristics with MB = 0



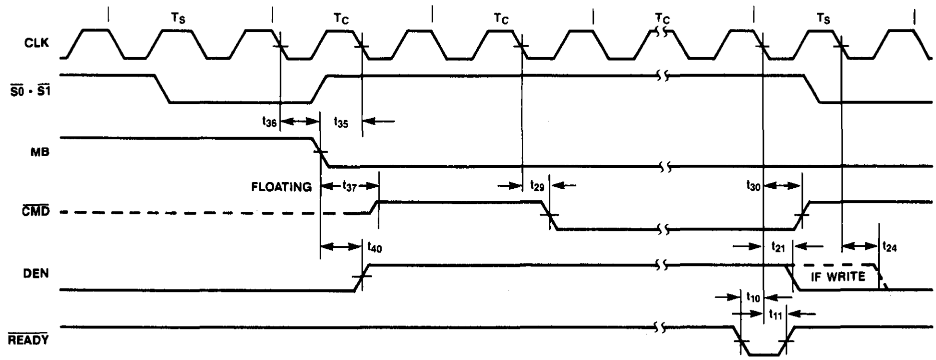
AEN Characteristics with MB = 1

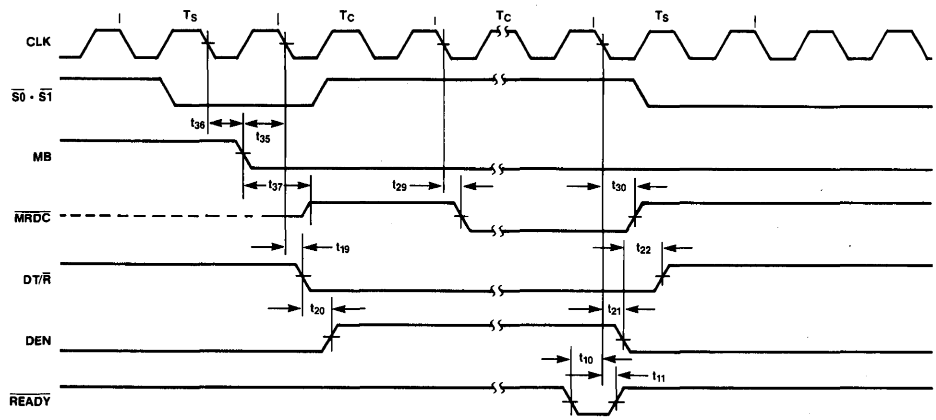


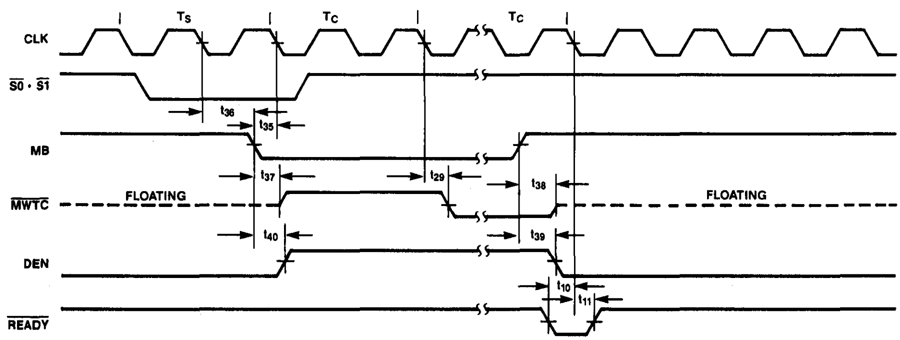
Note:
1. AEN is an asynchronous input. AEN setup and hold time is specified to guarantee the response shown in the waveforms.

WAVEFORMS (Continued)

MB Characteristics with $\overline{AEN}$/CEN = High

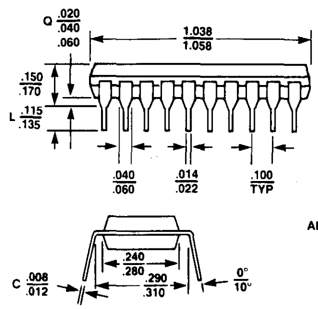






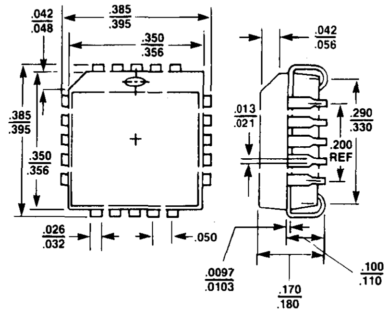
Note:
1. MB is an asynchronous input. MB setup and hold times specified to guarantee the response shown in the waveforms.
2. If the setup time, t35, is met two clock cycles will occur before $\overline{CMD}$ becomes active after the falling edge of MB.

PACKAGE DIMENSIONS



20-Pin DIP

ALL DIMENSIONS IN INCHES



20-Pin PLCC

ORDERING INFORMATION AND PRODUCT CODE

KS 82C288 X X X

SAMSUNG SEMICONDUCTOR — KS

Part Number — 82C288

Speed

-8.0	8.0MHz
-10.0	10.0MHz
-12.5	12.5MHz
-16.0	16.0MHz

Temperature
C — Commercial (0°C to +70°C)
I — Industrial (-40°C to +85°C)

Packaging
P — Plastic DIP
L — Plastic Leaded Chip Carrier (PLCC)

SAMSUNG products are designated by a Product Code. When ordering, please refer to products by their full code. For unusual, and/or specific packaging or processing requirements not covered by the standard product line, please contact the SAMSUNG MOS Product Group.

FEATURES/BENEFITS

- **Supports serial, parallel, and rotating priority resolving schemes**
- **Three modes of bus release operation**
- **Supports multi-master system bus arbitration protocol**
- **Compatible with IEEE 796 (MULTIBUS™) Standard**
- **Available in 20-pin plastic DIP**
- **8, 10, 12.5 and 16 MHz versions**
- **Low power CMOS**

DESCRIPTION

The Samsung KS82C289 20-pin CMOS Bus Arbiter signals to request, possess, and release the system bus. External logic determines which bus cycle requires the system bus and sets the priority of requests for control of the system bus.

The KS82C289 has processor-interface and Multibus state machines which support bus request and bus release logic.

The KS82C289 Bus Arbiter requires a Bus Controller, Clock Generator, and processor (bus master) to interface to the Multi-master System Bus.

Figure 1. KS82C289 Block Diagram

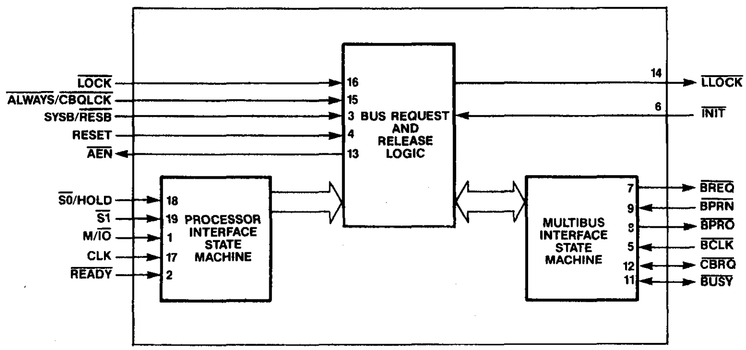


Figure 2a: 20-pin PLCC Configuration

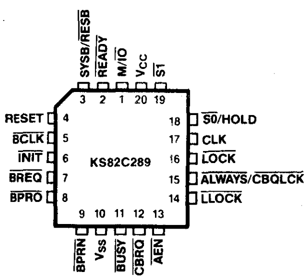
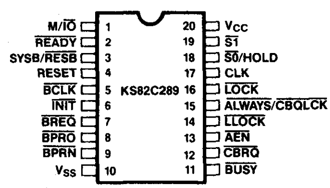


Figure 2b: 20-pin DIP Configuration



MULTIBUS is a trademark of Intel, Corp.

Table 1. KS82C289 Pin Allocations in a 20-pin Plastic DIP

Note on Conventions: A bar over the signal name is used to denote an active low signal ($\overline{S0}$). Active high signals are shown with no bar (HOLD).

Pin No.	Signal Abbrev.	Signal Name
1	M/$\overline{IO}$	Memory or I/O Select
2	$\overline{READY}$	Ready
3	SYSB/$\overline{RESB}$	System Bus/Resident Bus
4	RESET	Reset
5	$\overline{BCLK}$	Bus Clock
6	$\overline{INIT}$	Initialize
7	$\overline{BREQ}$	Bus Request
8	$\overline{BPRO}$	Bus Priority Out
9	$\overline{BPRN}$	Bus Priority In
10	V_{SS}	Ground
11	$\overline{BUSY}$	Busy
12	$\overline{CBRQ}$	Common Bus Request
13	$\overline{AEN}$	Address Enable
14	$\overline{LLOCK}$	Level Lock
15	$\overline{ALWAYS}$/ $\overline{CBQLCK}$	Always Release/Common Bus Request Clock
16	$\overline{LOCK}$	Lock
17	CLK	System Clock
18	$\overline{S0}$/HOLD	Status Input S0/Hold
19	$\overline{S1}$	Status Input S1
20	V_{CC}	VCC

3

Table 2. KS82C289 Signal Descriptions

Note: I indicates that the signal is an input to the KS82C289 chip. O indicates that the signal is an output from the KS82C289 chip.

<table>
<tr><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td>CLK</td><td>I</td><td>System Clock: Receives the CLK signal from the clock generator as a timing reference. The processor interface state machine (see Figure 1) is synchronous to the falling edge of CLK.</td></tr>
<tr><td>$\overline{S0}$/HOLD</td><td>I</td><td>Status Input S0 or Hold: Becomes active if $\overline{S0}$ is received from the processor or HOLD is received from the bus master.
HOLD is selected if the $\overline{S0}$/HOLD pin is high at the falling edge of the processor RESET.
$\overline{S0}$ is selected if $\overline{S0}$/HOLD pin is low at the falling edge of the processor reset.</td></tr>
<tr><td>$\overline{S1}$, M/$\overline{IO}$</td><td>I</td><td>Status Input 1, Memory or Input/Output Select: $\overline{S0}$, $\overline{S1}$, and M/$\overline{IO}$ are the status input signals from the processor. These inputs are decoded, along with $\overline{S0}$/HOLD, to start a bus request or to release the bus.
If either $\overline{S1}$ or $\overline{S0}$ is low at the falling edge of the clock, a bus cycle is started.
Bus Cycle Status Encoding
<table>
<tr><th>M/$\overline{IO}$</th><th>$\overline{S0}$</th><th>$\overline{S0}$/HOLD</th><th>Type of Bus Cycle</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Interrupt acknowledge</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>I/O Read</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>I/O Write</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>None; bus idle</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Halt or shutdown</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Memory read</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Memory write</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>None; bus idle</td></tr>
</table></td></tr>
<tr><td>SYSB/$\overline{RESB}$</td><td>I</td><td>System Bus/Resident Bus: Decides when the multi-master system bus is needed for the current bus cycle.
If SYSB/$\overline{RESB}$ is high at the end of the T_S bus state, the arbiter will request or retain the multi-master system bus.
SYSB/$\overline{RESB}$ is sampled at every falling edge of the CLK which starts at the end of the T_S bus state until the bus cycle is finished by the $\overline{READY}$ signal or SYSB/$\overline{RESB}$ becomes high (inactive).</td></tr>
<tr><td>$\overline{READY}$</td><td>I</td><td>Ready: Indicates the end of the bus cycle if $\overline{READY}$ is low (active). The processor does not require the $\overline{READY}$ signal to end the bus cycle.</td></tr>
<tr><td>$\overline{LOCK}$</td><td>I</td><td>Lock: If $\overline{LOCK}$ is active (low), the arbiter is prevented from releasing the multi-master system bus to any other arbiters having higher priority. $\overline{LOCK}$ is sampled at the end of every bus state.</td></tr>
</table>

Table 2. KS82C289 Signal Descriptions (Continued)

Symbol	Type	Description
ALWAYS	I	**Always Release:** Must be programmed during the falling edge of the processor reset by setting this pin low. Arbiter will release the multi-master system bus after each bus transfer cycle. Arbiter will be in the Always Release mode until reprogrammed.
CBQLCK	I	**Common Bus Request Lock:** Is programmed if this pin is set high during the falling edge of the processor reset. CBQLCK is active on and prevents the arbiter from releasing the multi-master system bus to any other arbiters.
INIT	I	**Initialize:** If INIT is low (active), all the arbiters on the multi-master system bus are reset. Releases the multi-master system bus but, pending a bus request, it cannot be cleared. Hence, arbiters can regain the multi-master system bus immediately, if necessary. INIT is not synchronous to CLK. **Note:** LLOCK (Level Lock) is not affected by this signal.
RESET	I	**Reset:** If RESET is high (active), BREQ, BUSY, and AEN are cleared and become inactive. RESET will also stop any current bus cycle without waiting for it to end. The bus cycle terminated by RESET will not be completed when RESET becomes inactive.
BCLK	I	**Bus Clock:** BCLK is the multi-master system bus clock. All of the multi-master bus interface signals are synchronized to BCLK. BCLK may not be synchronous to CLK. The multi-master system bus interface state machine (see Figure 1) is asynchronous to the falling edge of BCLK.
BREQ	O	**Bus Request:** The arbiter keeps the BREQ low (active) until it releases the multi-master system bus. BREQ is essential in the rotating and parallel priority resolving technique.
BPRN	I	**Bus Priority In:** When low (active), this arbiter has the highest priority. When high, another arbiter with higher priority is requesting the multi-master system bus.
CBRQ	I/O	**Common Bus Request:** An open-drain input/output which requires an external pull-up resistor. As an input: Another arbiter is requesting the multi-master system bus. It is enabled by the CBRQ. As an output: This arbiter is requesting the multi-master system bus. When BREQ (Bus Request) is issued, the CBRQ is pulled low. When the arbiter gains the multi-master system bus, the CBRQ is released.
BPRO	O	**Bus Priority Out:** BPRO low (active) is used for the serial priority technique. BPRO is connected to the BPRN (Bus Priority In) of the immediately lower priority to decide the status of the priority for that arbiter.
LLOCK	O	**Level Lock:** LLOCK cannot be cleared by the INIT, but can be cleared by RESET. When buffered with a tri-state buffer enabled by the AEN (Address Enable), LLOCK can be used as a multi-master system bus lock. LLOCK is active low and it is decoded from the processor LOCK.

Table 2. KS82C289 Signal Descriptions (Continued)

Symbol	Type	Description
AEN	O	**Address Enable:** Connected to the clock generator, bus controller, and the processor's address latches. When low (active), can be used as Hold ACK (Hold Acknowledge) to a bus master. When high, indicates to the bus master that the arbiter has released the system bus. AEN becomes active relative to BCLK (Bus Clock). AEN becomes inactive relative to CLK (System Clock).
BUSY	I/O	**Busy:** An open-drain input/output which requires an external pull-up resistor. As an input: Low (active) indicates that the multi-master system bus is in use. As an output: When high, indicates that this arbiter has taken control of the multi-master system bus.
V_{SS}	—	**Ground.**
V_{CC}	—	+5 volts supply voltage.

OPERATIONAL DESCRIPTION

Arbitration Between Bus Masters

The KS82C289 Bus Arbiter is a priority controlling device which allows the multi-master system bus to be used for multi-processing. Both higher and lower priority bus masters are allowed to gain the system bus, depending on the release mode. Ordinarily, the higher priority master acquires the system bus immediately after any lower priority master finishes its present cycle. Therefore, at the end of each transfer cycle, the Arbiter can keep the system bus or release it depending on the bus arbitration inputs, arbiter strapping options, and the processor state.

Releasing the Multi-Master System Bus

The Bus Arbiter can retain or release control of the multi-master system bus following every transfer cycle. There are three modes in which the Arbiter can release the multi-master system bus.

These three modes cannot release the multi-master system bus if the cycles are LOCKed.

Mode 1

Always Release Mode

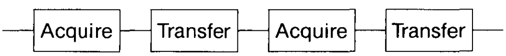


Figure 3. Always Release Mode

Releases the multi-master system bus at the end of each transfer cycle. Mode 1 must be programmed at the falling edge of the processor RESET.

Mode 2

Releases the multi-master system bus if either condition, below, is met:

a) a lower priority bus master demands the bus by pulling CBRQ low.

b) BPRN = 1, which indicates that the higher priority bus master is asking for the multi-master system bus.

Mode 3

Mode 3 is the same as Mode 2, only CBRQ has no effect.

Gaining Control of the Multi-Master System Bus

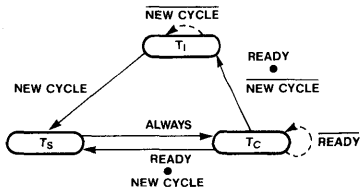
The CBRQ signal indicates whether or not another Arbiter wishes to gain control of the multi-master system bus. To perform this function, CBRQ must be connected to all other Arbiter CBRQ pins. Therefore, if any Bus Arbiter activates the CBRQ pin, it will pull down the CBRQ line to low.

Besides the CBRQ line, only the BPRN indicates if other, higher-priority, masters are requesting the bus.

A lower priority master can gain the bus in between the bus master's transfer cycles if the bus master has terminated its use of the bus. Then the bus must gain BCLK again at the beginning of the next transfer cycle.

This requires two $\overline{BCLK}$ periods if no other master demands the bus. This step of giving up and getting back the bus is wasteful and unnecessary. To bypass this problem $\overline{CBRQ}$ is useful. The Bus Arbiter does not need to release the bus if the $\overline{CBRQ}$ is not asserted. This alleviates the inefficient delay of getting back the multi-master system bus.

Figure 4. Bus States and the $\overline{READY}$ Signal



Bus States

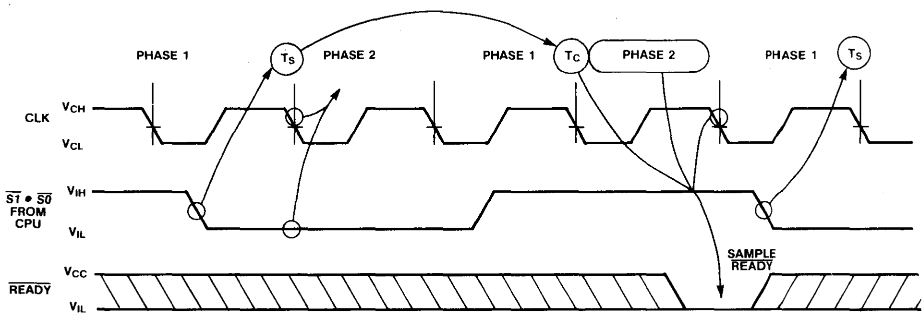
The Bus Arbiter has three processor bus states:

a) T_I (Idle)
b) T_S (Status)
c) T_C (Command)

Each bus cycle is two CLK cycles long.

Internal CPU processor clock phases correspond to the bus state phases.

Figure 5. 80286 Bus Cycle Definition (without wait states)



Bus Cycles

The $\overline{S1}$ and $\overline{S0}$ status inputs are sampled only at the falling edge of the CLK. $\overline{S1}$ and $\overline{S0}$ indicate the start of the bus cycle by going active (low).

The arbiter enters the T_S state if either the $\overline{S1}$ or $\overline{S0}$ is active (low) during the two CLK cycles.

The arbiter enters the T_C state after T_S is exited.

The shortest bus cycle is one T_S and one T_C. The longest bus cycle is one T_S followed by multiple T_C states. A repeated T_C bus state is referred to as a wait state.

The $\overline{READY}$ input determines whether the current T_C is to be repeated. It is sampled at the end of every T_C state if it is high. If it is high (1), then the T_C is repeated. When $\overline{READY}$ is sampled low, the current bus cycle is aborted.

If the $\overline{S1}$ and $\overline{S0}$ status lines are low at the next falling edge of the CLK, then the Bus Arbiter enters the T_S state immediately after the current bus cycle is aborted.

If none of the status lines are sampled active (low) at the next falling edge of the CLK, then the Bus Arbiter enters the T_I state. T_I is repeated until the status lines are sampled active (low).

Bus Masters

MULTIBUS protocols allow multiple processing elements to share access to common system resources. When a common system resource such as the system bus is "BUSY", local processors must wait for access.

The Bus Arbiter sets priorities and schedules access to the multi-master system bus. The bus arbiter supplies access to the system bus depending upon the release mode and the higher or lower priority of each bus master.

When the bus arbiter is used, higher priority bus masters access the system bus before lower priority bus masters or when the current lower priority bus master completes its transfer cycle. Lower priority bus masters access the system bus when there are no higher priority bus masters or when the proper surrender conditions exist.

The bus arbiter arranges scheduling and access transparently to the bus master.

The bus arbiter retains or releases the system bus at the end of each transfer cycle. The processor state, bus arbitration inputs, and arbiter strapping options are the factors used by the bus arbiter to determine release status. Refer to section "Release Modes" for more specific information.

Establishing Priority

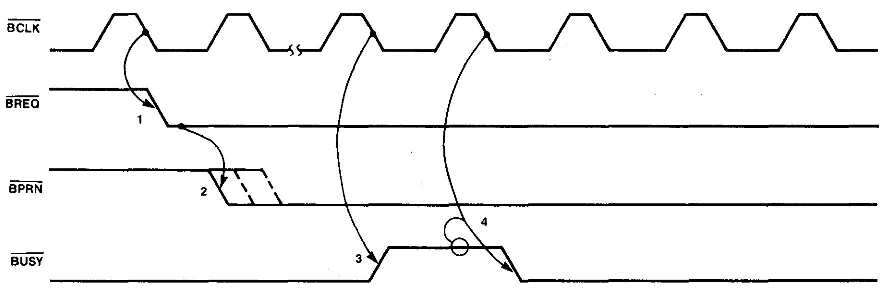
The Bus Arbiter establishes the priority level of the bus masters that are competing for access to a multi-master bus. To do this, the bus arbiter uses parallel, serial, and rotating techniques. Each of these techniques assumes that at any point in time, one bus master has priority over all other bus masters.

The highest priority arbiter is the arbiter with a $\overline{BPRN}$ input (low). The arbiter with the highest priority cannot access the system bus until the system bus is released from its current transaction.

When the system bus completes its current transaction, the present bus owner releases $\overline{BUSY}$. $\overline{BUSY}$ is an active-low 'Wired-OR' MULTIBUS signal which indicates that the system bus is inactive. This signal is sent to every bus arbiter in the system.

When the arbiter with the highest priority ($\overline{BPRN}$ low) receives the $\overline{BUSY}$ signal, it seizes the system bus by pulling $\overline{BUSY}$ (low). Figure 6 is a graphic representation of the Bus Exchange Timing.

Figure 6. Bus Exchange Timing for the MULTIBUS®



BUS EXCHANGE TIMING

A multi-master bus request is initiated when two conditions occur. 1) a processor signals the status for memory read, memory write, I/O read, I/O write, or interrupt acknowledge. 2) an SYSB/$\overline{RESB}$ (high) at the end of T_S.

An interrupt acknowledge cycle does not always require the MULTIBUS each time the status input indicates. To determine when to request the MULTIBUS, the arbiter uses external logic, through the SYSB/$\overline{RESB}$ input.

When the arbiter samples SYSB/$\overline{RESB}$, and it is (high), the MULTIBUS is requested. When the arbiter samples SYSB/$\overline{RESB}$ and it is not (high), the arbiter continues to sample SYSB/$\overline{RESB}$ until either SYSB/$\overline{RESB}$ is (high) or the bus cycle is terminated. The arbiter does not request the MULTIBUS if the bus cycle is completed before SYSB/$\overline{RESB}$ returns (high). Figure 7 is an example of an SYSB/$\overline{RESB}$ sampled repeatedly.

The bus arbiter generates and uses only one $\overline{BREQ}$ from the time it requests the system bus through the entire time it has access to the system bus. The bus arbiter does not generate a separate $\overline{BREQ}$ for each bus cycle. All multi-master system bus requests using $\overline{BREQ}$ are synchronized to the system bus clock, $\overline{BCLK}$.

Parallel Priority Technique

In order to use the parallel technique for determining bus master priority, each bus arbiter on the multi-master system bus must have its own bus request line (BREQ). Figure 8 is a representation of the parallel technique.

Each BREQ line is fed into a priority encoder. The encoder generates the binary address of the active BREQ line with the highest priority. Then a decoder uses the binary address to identify the BPRN line corresponding to the requesting bus arbiter with the highest priority. The BPRO output is not used with the parallel priority resolving technique.

When an arbiter receives the highest priority, BPRN (low) and the system bus is released, the arbiter's associated bus master is allowed onto the multi-master system.

The only limiting factor, for the number of bus masters that can be handled by the parallel technique, is the external circuitry. The external circuitry must be able to resolve the bus priorities within one BCLK period. Otherwise the parallel priority resolving technique can be used for any number of bus masters.

Serial Priority Technique

The serial priority technique does not require external circuitry. The arbiters are connected in a daisy chain fashion. The highest priority arbiter has its BPRO output connected to the BPRN input of the next lower priority arbiter. That next lower arbiter has its BPRO output connected to the BPRN input of the next lower priority arbiter after itself, etc. Figure 9 is a representation of serial technique connection.

This technique establishes a fixed position of priority. The highest priority bus arbiter has its BPRN tied (low), ensuring that it always receives highest priority when it requests the system bus. Figure 10 illustrates serial priority bus behavior.

A lower priority arbiter receives temporary higher priority status from the fixed higher priority arbiter. When the arbiter with the higher priority is not accessing or requesting the system bus, it asserts its BPRO signal (low). This asserts the BPRN signal of the fixed lower priority arbiter, allowing it to have the highest priority, temporarily.

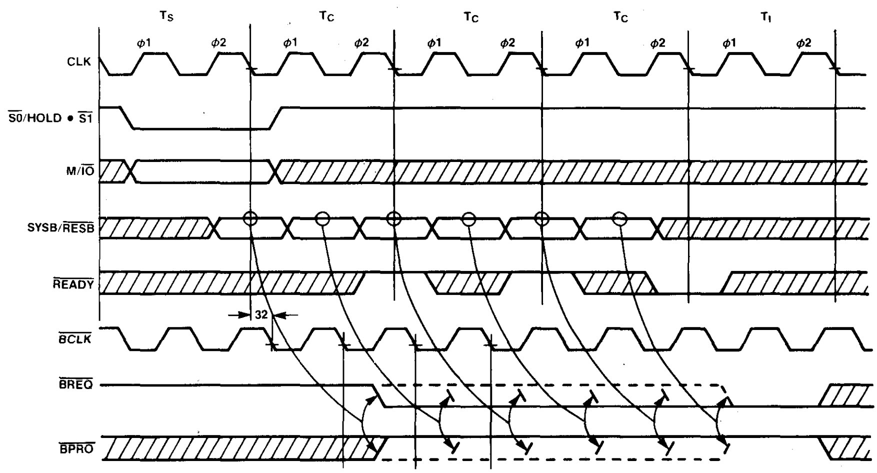
When its BPRO goes inactive, a fixed higher priority arbiter retrieves its priority status from a fixed lower priority arbiter. The BPRO of an arbiter becomes inactive when it either requests access to the system bus or when its BPRN goes inactive because the BPRO from the next higher arbiter goes inactive. This allows for a trickle down effect from fixed higher priority arbiters down to the fixed lowest priority arbiter.

BREQ output is not used for the serial technique.

The number of bus arbiters connected in serial for priority resolution is limited by propagation delay between BPRN and BPRO, 18ns, because priority must be established within one BCLK period. Therefore the maximum number of bus arbiters equals BCLK period divided by BPRN to BPRO delay.

$$\text{number of bus arbiters} = \frac{\overline{\text{BCLK}}\ \text{period}}{\overline{\text{BPRN}}\ \text{to}\ \overline{\text{BPRO}}\ \text{delay}}$$

Figure 7. Bus Request Timing During an Interrupt Acknowledge Cycle



3

Figure 8. Parallel Priority Resolving Technique

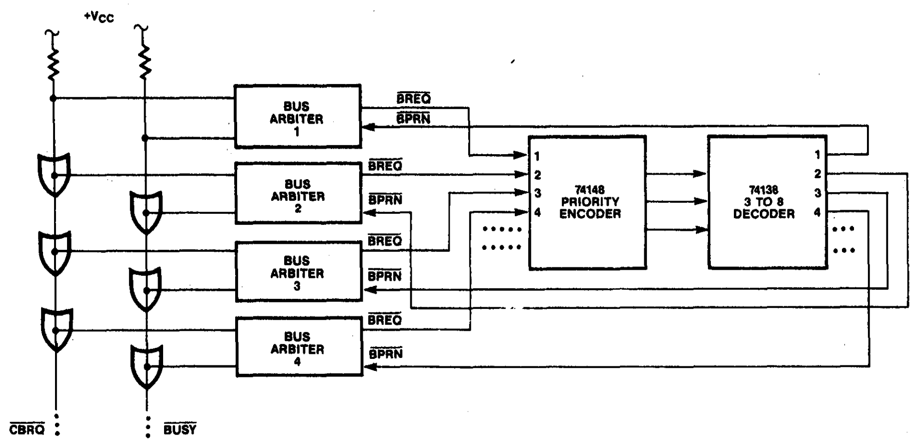


Figure 9. Connections for Serial Priority Resolving Technique

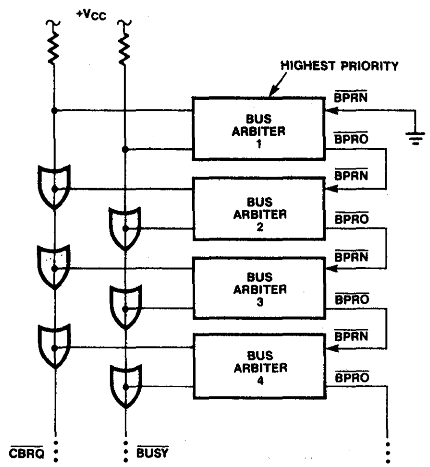
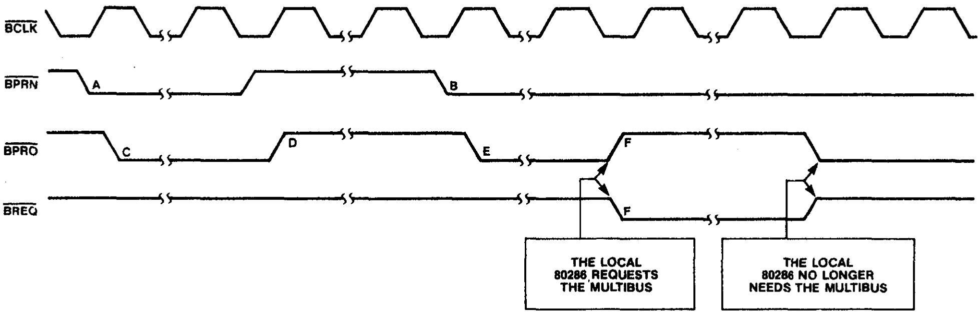


Figure 10. Serial Priority Bus Behavior



3

Note: Events A through F described above.

Rotating Priority Technique

The rotating priority technique requires external circuitry, similar to the parallel priority technique. The rotating technique assigns and re-assigns priority to the arbiters dynamically.

The priority encoder used in the rotating technique is a more complex circuit than the one used in the parallel technique. The circuit rotates priority between requesting arbiters. This provides each arbiter with an equal chance to use the multi-master system bus over a specified amount of time.

Choosing a Priority Technique

Each priority technique, parallel, serial, and rotating provides a trade-off between using complex external circuitry and allowing equal access to the system bus by each bus master.

The parallel priority technique does not require extensive external logic circuits, does allow for re-assignment of priority status for each bus master, and can accommodate a relatively large number of bus masters.

The serial priority technique does not require any external logic circuits but has fixed priority settings assigned to each bus master and can accommodate a limited number of bus masters.

The rotating priority technique does requires more complicated external logic circuits but does provide equal access between each of the bus masters and the system bus.

Releasing the MULTIBUS

The bus arbiter can either release or retain control of the system bus after the completion of a data transfer cycle on the MULTIBUS. Whether the bus arbiter releases control of the system bus depends upon the release mode selected and the priority settings in effect for the release mode selected.

There are three release modes. Table 3 describes the release modes and the mode settings which enable release of the system bus.

Table 3. Release Modes

Release Mode	Acceptable Release Conditions
Mode 1	The bus arbiter always releases the bus at the end of the transfer cycle.
Mode 2	The bus arbiter retains the system bus until: • a higher-priority bus master requests the system bus. This drives the $\overline{BPRN}$ (high) • a lower priority bus master requests the system by pulling $\overline{CBRQ}$ (low)
Mode 3	The bus arbiter retains the system bus until: • a higher priority bus master requests the system bus. This drives the $\overline{BPRN}$ (high) • $\overline{CBRQ}$ (low) is ignored **Note:** If the cycles are $\overline{LOCK}$ed, the bus arbiter does not release the system bus, even if the mode release conditions are met.

The arbiter will surrender the MULTIBUS after each complete transfer cycle if the "Always Release" mode 1 is programmed.

If the "Always Release" mode 1 is not programmed, the arbiter will not surrender the MULTIBUS until one of the following occur:

- the processor enters a halt state
- the arbiter is forced off because the BPRN becomes (high) and mode 2 or mode 3 is programmed into the arbiter
- the arbiter is forced off because a common bus request CBRQ input is enabled and mode 2 is programmed into the arbiter

CBRQ reduces bus exchanges. The present bus master retains the sytem bus as long as CBRQ is (high). CBRQ remains (high) until another master requests the system bus.

BPRN indicates if a bus master of higher priority is requesting the system bus. It does not indicate if a bus master of lower priority is requesting the system bus.

In order to allow lower priority bus masters access to the system bus, bus masters must release the system bus at the end of each transfer cycle and re-establish priority to access the system bus again and wait for a current transfer cycle opening. This release, re-establishing priority and re-accessing can take approximately two BCLK periods.

CBRQ eliminates unnecessary releasing of a bus master from the system bus. When a bus master requires the system bus it must assert CBRQ (low). If CBRQ remains (high), the current bus master does not have to release the system bus at the end of each transfer cycle.

LOCK overrides any of the release mode options. As long as LOCK is asserted, the arbiter will not release control of the MULTIBUS to any other requesting bus master.

INIT or RESET signals cause the arbiter to surrender the MULTIBUS. The release mode and arbiter input status are ignored.

The three bus release modes operate the same irregardless of the type of microprocessor used.

Choosing a Release Mode

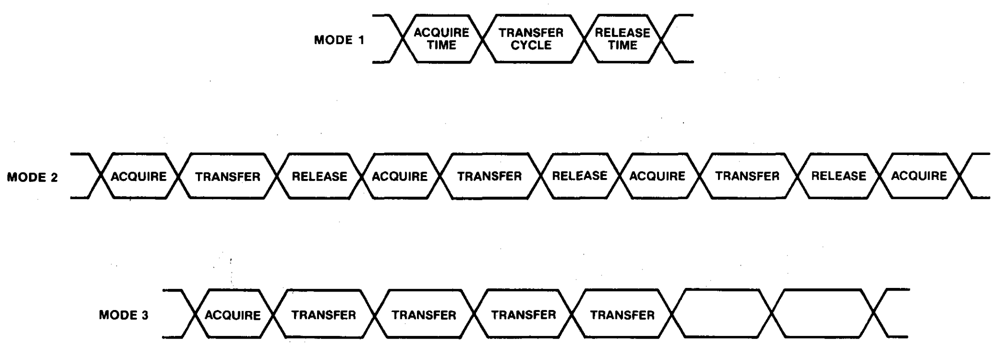
The release mode affects subsystem bus utilization and the system as a whole. The acquire and release times specified for each of the release modes impacts the system bus efficiency. Figure 11 illustrates the differences caused the release and acquisition times for each release mode.

Mode 1 requires a request and release phase for every transfer cycle. This allows lower priority bus masters to access the system bus, but it reduces the overall bus efficiency.

Modes 2 and 3 let the bus master retain the system bus for multiple transfer cycles. A bus master releases the system bus when it is forced off by another bus master's request.

Each release mode allows the designer to optimize the system use of the MULTIBUS.

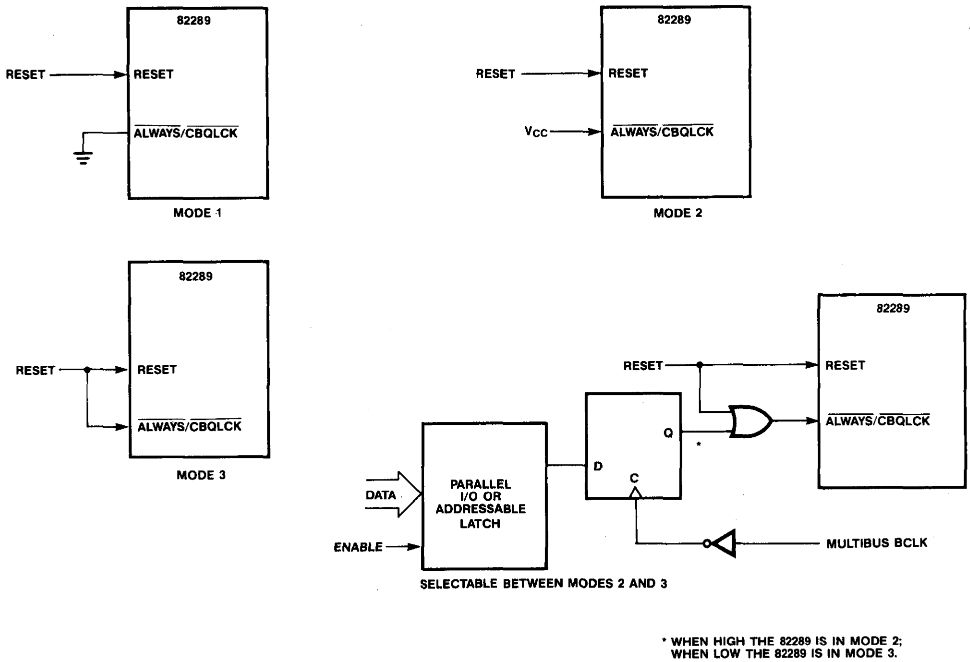
Figure 11. Effects of Bus Release Mode on Bus Efficiency



Configuring Release

The bus arbiter does not require any additional hardware to configure in any of the three release modes. In addition, the processor can be configured to switch between mode 2 and mode 3 by software control. This requires that a parallel port or addressable latch is used to drive the ALWAYS/CBQLCK input pin of the processor. Figure 12 illustrates the three release mode configurations.

Figure 12. 82289 Release Mode Configurations



LOCK and LLOCK

The three modes of releasing the multi-master system bus can be nulled by the LOCK input. But, LOCK will not surrender control of the multi-master system bus to any other Arbiter. The Bus Arbiter will surrender the multi-master system bus if RESET or INIT becomes active. RESET and INIT are independent of the states of the Arbiter inputs or the current release mode.

The LOCK signal can be asserted to the bus arbiter synchronous with the CLK and independent of the three release modes to prevent the release of the multi-master system bus to other bus masters regardless of their order of priority.

The LLOCK output signal can be asserted at all the bus cycles that are LOCKed. LLOCK is 1 if LOCK is 1, and 0 if LOCK is 0. Once LLOCK is active, it will wait until the end of the current transfer cycle before becoming inactive.

RESET and Initialization (INIT)

INIT (active low) is an asynchronous signal from the multi-master system bus. BREQ, BUSY, and AEN are cleared and become inactive when INIT is active (low). The Bus Arbiter will not clear any pending bus request from other bus masters while INIT is active. INIT can interrupt an active bus cycle, but, it will not prevent the Arbiter from requesting the multi-master system bus when it becomes inactive and completing the bus cycle.

RESET (active high) is synchronous to the CLK and can be synchronous to the processor. BREQ, BUSY, and AEN are cleared and become inactive when RESET is asserted. Also, RESET will clear the LLOCK signal and clear any pending bus request, unlike the INIT signal. RESET will stop any current bus cycle without waiting for the cycle to end. And, the bus cycle terminated by RESET will not be completed after the RESET becomes inactive.

DC ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Storage Temperature .... -65°C to +150°C
Ambient Temperature Under Bias ...... 0°C to 70°C
Case Temperature .... 0°C to 85°C

Note: Operation at absolute maximum ratings may cause permanent damage to the device.

Table 4. DC Electrical Characteristics

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{ILC}	CLK Input Low Voltage			0.6	V
V_{IHC}	CLK Input High Voltage		3.0	V_{CC}	V
V_{OL}	Output Low Voltage: $\overline{BUSY}$, $\overline{CBRQ}$, $\overline{BPRO}$ $\overline{BPRO}$, $\overline{BREQ}$, $\overline{AEN}$ $\overline{LLOCK}$	 I_{OL} = 32 mA I_{OL} = 16 mA I_{OL} = 5 mA		 0.45 0.45 0.45	 V V V
V_{OH}	Output High Voltage	I_{OH} = 400 μA	2.4		V
I_{LI}	Input Leakage Current	$V_{SS} < V_{IN} < V_{CC}$		+1	μA
I_O	Output Leakage Current	$V_{OUT} = V_{SS}$ or V_{CC}		+10	μA
I_{CC1}	Quiescent Current	CLK, V_{IN} - V_{CC} or V_{SS}		+10	μA
I_{CC2}	Supply Current			+80	mA
C_{CLK}	CLK, $\overline{BCLK}$ Input Capacitance	FC = 1 MHz		12	pF
C_{IN}	Input Capacitance	FC = 1 MHz		10	pF
C_O	Input/Output Capacitance	FC = 1 MHz		20	pF

AC SWITCHING CHARACTERISTICS

Table 5. KS82C289 AC Switching Characteristics

No.	Parameter	Test Conditions	8.0 MHz		10.0 MHz		12.5 MHz		16.0 MHz (Preliminary)		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
01	CLK Cycle Period		60	BCLK+50	50	BCLK+50	40	BCLK+50	31	BCLK+50	ns
02	CLK Low Time	at 1.0V	15	230	15	230	10		8		ns
03	CLK High Time	at 3.6V	20	235	15	230	12		9		ns
04	CLK Rise/Fall Time	1 to 3.6V		10		10		9		7	ns
05	$\overline{BCLK}$ Cycle Time		100		100		100	∞	100	∞	ns
06	$\overline{BCLK}$ High/Low Time		30		25		20		16		ns

Table 5. KS82C289 AC Switching Characteristics (Continued)

No.	Parameter	Test Conditions	8.0 MHz		10.0 MHz		12.5 MHz		16.0 MHz (Preliminary)		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
07	$\overline{S0}$/HOLD, $\overline{S1}$, M/$\overline{IO}$ Setup Time		22		15		13		10		ns
08	$\overline{S0}$/HOLD, $\overline{S1}$, M/$\overline{IO}$ Hold Time		1		1		1		1		ns
09	$\overline{READY}$ Setup Time		38		30		24		19		ns
10	$\overline{READY}$ Hold Time		25		20		16		13		ns
11	$\overline{LOCK}$, SYSB/$\overline{RESB}$ Setup Time		20		15		12		10		ns
12	$\overline{LOCK}$, SYSB/$\overline{RESB}$ Hold Time		1		1		1		1		ns
13	RESET Setup Time		20		15		12		10		ns
14	RESET Hold Time		1		1		1		1		ns
15	RESET Active Pulse Width		16		16		16		16		CLKs
16	$\overline{INIT}$ Setup Time	Note 2	45		45		45		45		ns
17	$\overline{INIT}$ Hold Time	Note 2	1		1		1		1		ns
18	$\overline{INIT}$ Active Pulse Width		$3(t_1)+(t_{14})$		$3(t_1)+(t_{14})$		$3(t_1)+(t_{14})$		$3(t_1)+(t_{14})$		ns
19	$\overline{BUSY}$, $\overline{BPRN}$, $\overline{CBRQ}$, CBQCLK/$\overline{ALWAYS}$ Hold Time to $\overline{BCLK}$ or (RESET)		20		18		15		12		ns
20	$\overline{BUSY}$, $\overline{BPRN}$, $\overline{CBRQ}$, CBQCLK/$\overline{ALWAYS}$ Hold Time to $\overline{BCLK}$ or (RESET)		1		1		1		1		ns
21	$\overline{BCLK}$ to $\overline{BREQ}$ Delay	C = 60 pF		30		30		25		20	ns
22	$\overline{BCLK}$ to $\overline{BPRO}$ Delay	C = 60 pF		35		35		28		22	ns
23	$\overline{BPRN}$ to $\overline{BPRO}$ Delay	C = 60 pF		25		25		20		16	ns
24	$\overline{BCLK}$ to $\overline{BUSY}$ Active Delay	C = 300 pF	1	60	1	60	1	50	1	38	ns
25	$\overline{BCLK}$ to $\overline{BUSY}$ Float Delay	Note 1		35		35		28		22	ns
26	$\overline{BCLK}$ to $\overline{CBRQ}$ Active Delay	C = 300 pF		55		55		45		35	ns
27	$\overline{BCLK}$ to $\overline{CBRQ}$ Float Delay	Note 1		35		35		28		22	ns
28	$\overline{BCLK}$ to $\overline{AEN}$ Active Delay	C = 150 pF	1	25		25	1	20		16	ns
29	CLK to $\overline{AEN}$ Inactive Delay	C = 150 pF	3	25		25	3	20		16	ns
30	CLK to $\overline{LLOCK}$ Delay	C = 50pF		20		20		16		13	ns
31	RESET to $\overline{LLOCK}$ Delay	Note 2		35		35		28		22	ns
32	CLK to $\overline{BCLK}$ Setup Time	Note 3	38		38		35		25		ns

T_A = 0°C to 70°C
T_{CASE} = 0°C to 85°C
V_{CC} = 5V ± 5%

Notes: AC timing is referenced to 0.8V and 2.0V points.
1. When $I_O \leq I_{LO}$, float condition occurs.
2. CLK and $\overline{BCLK}$ are asynchronous to each other in actual use. But, this specification is required for component testing.
3. $\overline{INIT}$ is asynchronous to CLK and to $\overline{BCLK}$ during actual use. But, this specification is required for component testing.

Figure 13. AC Drive and Measurement Points CLK Input (BCLK Input)

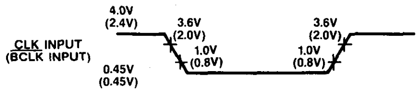


Figure 14. AC Setup, Hold and Delay Time Measurement

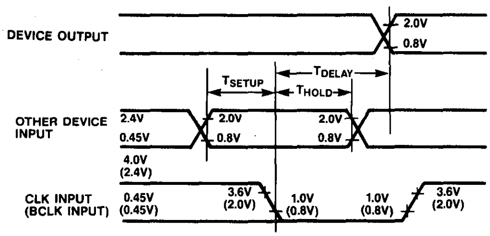
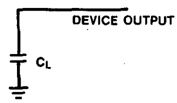


Figure 15. AC Test Loading on Outputs



WAVEFORMS

The following waveforms, Figures 16 through 24, contain examples of general cases of the timing relationships of the inputs and the outputs. These figures do not represent all the possible input and output transitions of all signals in all modes.

Refer to the identified special cases or a timing specification for the same or related function in another mode for examples of specific transitions.

The bus arbiter serves as an interface between the iAPX subsystem and MULTIBUS. The iAPX 286 subsystem operates synchronously to the CLK signal. The MULTIBUS operates synchronous to the BCLK signal.

CLK and BCLK operate asynchronously to each other and at different frequencies. The relative phase and frequency of CLK and BCLK at the time the input is sensed effects the exact clock period where a synchronous input to one clock will cause a synchronous response in the other clock.

The CLK period cannot be too long, relative to the BCLK period, t_1 greater than t_5 + 50ns, in order to maintain proper MULTIBUS arbitration. If the CLK period is too long relative to the BCLK period, another arbiter could gain control of the system bus before the current arbiter releases AEN synchronous to its CLK.

The AEN release is synchronous to the fall of the CLK edge after the processor cycle ends. The BREQ and BUSY releases are synchronous to the fall of the BCLK after the processor cycle ends.

However, all 286 speed selections are MULTIBUS compatible because any CLK frequency greater than 6.66 MHz, processor speeds greater than 3.33 MHz, avoids conflict with 10 MHz BCLKs.

Figure 16. MULTIBUS® Acquisition and Always-Release Operation

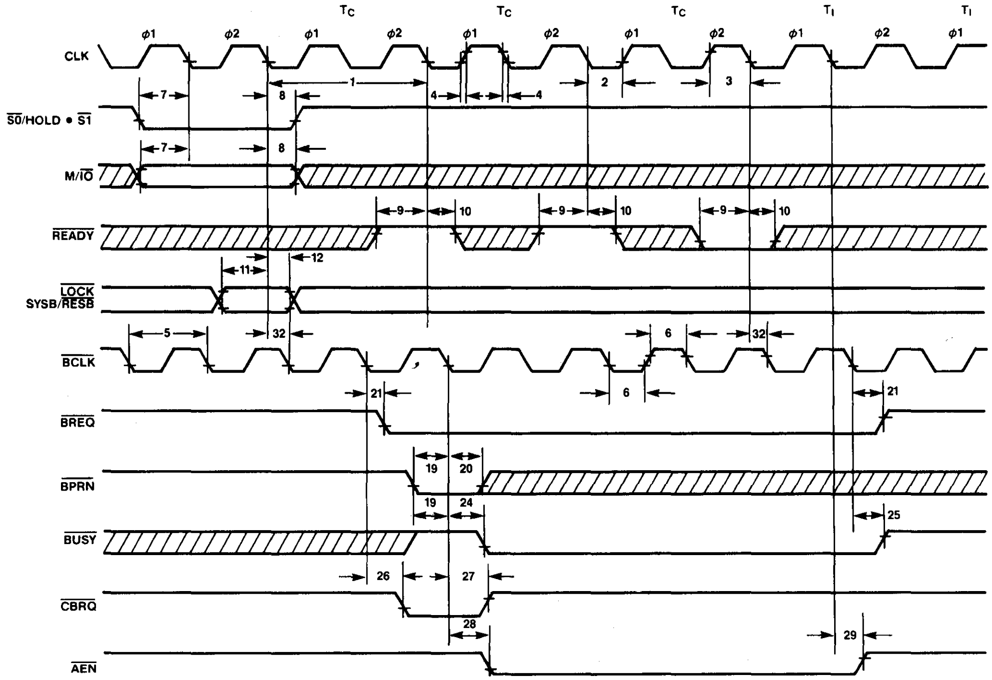


Figure 17. MULTIBUS® Release due to BPRN Inactive

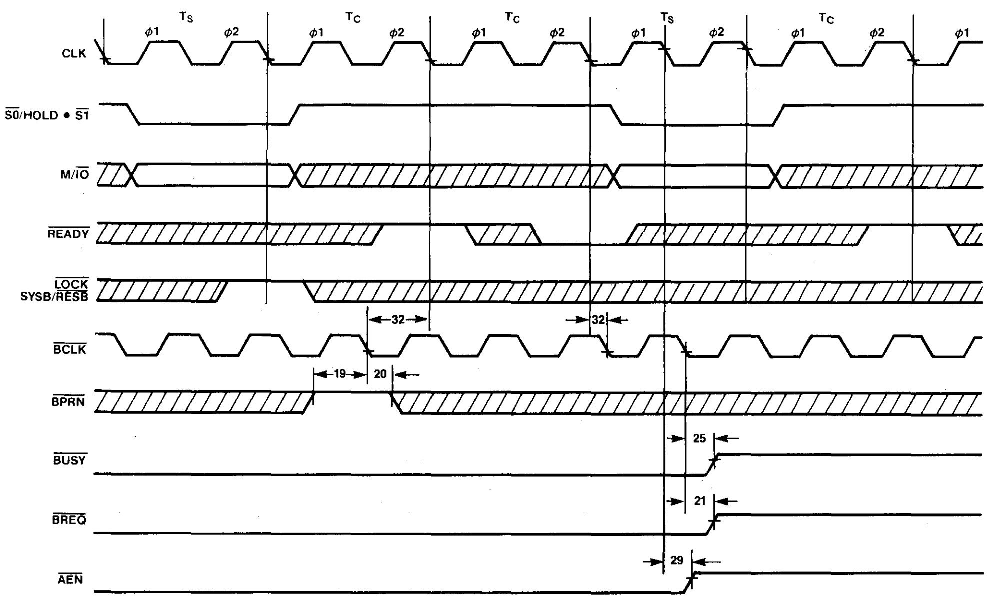


Figure 18. MULTIBUS® Release due to $\overline{CBRQ}$ Active

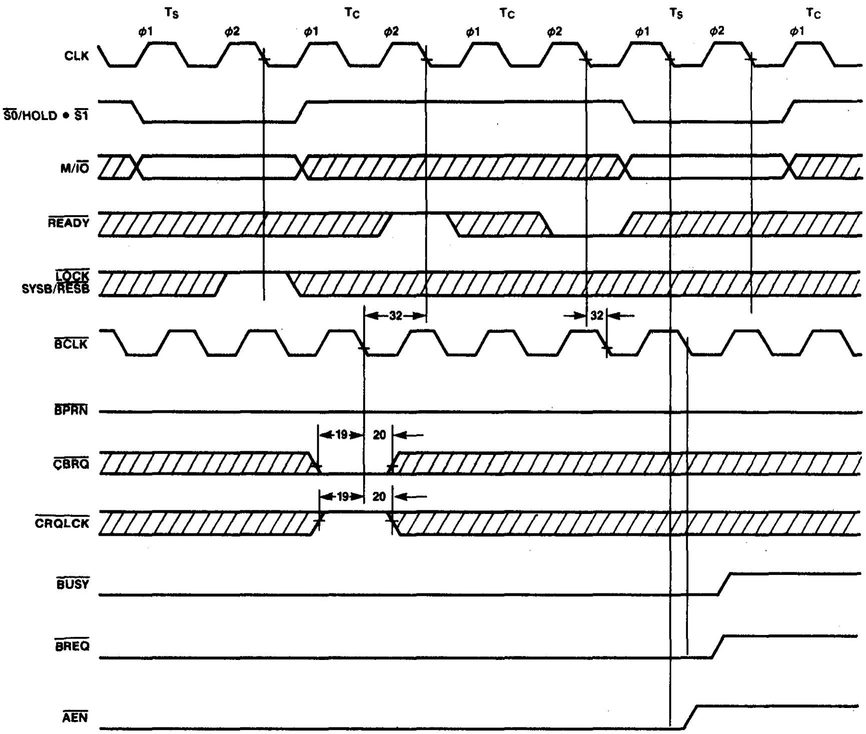


Figure 19. MULTIBUS® Acquisition During 80286 INTA Cycles

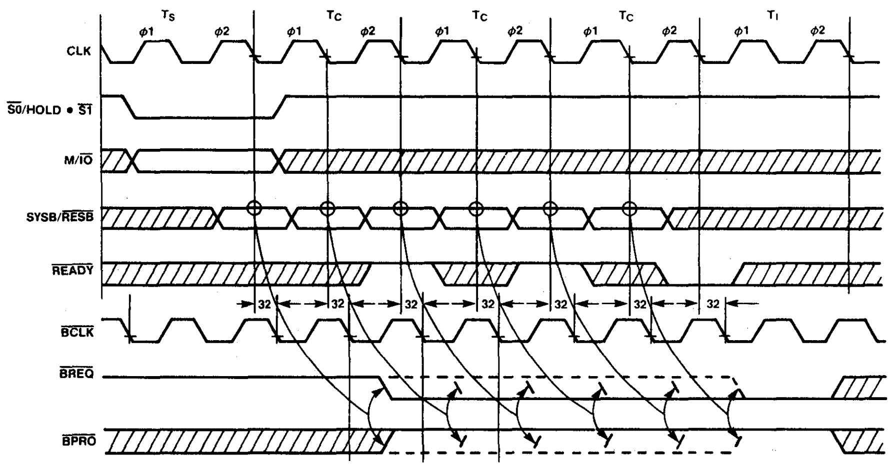


Figure 20. $\overline{BPRN}$ to $\overline{BPRO}$ Timing Relationship

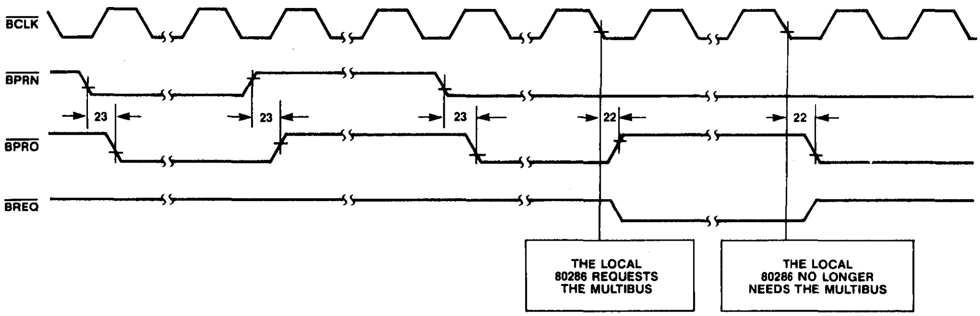


Figure 21. 80286 $\overline{LOCK}$ and 82289 $\overline{LLOCK}$ Relationship

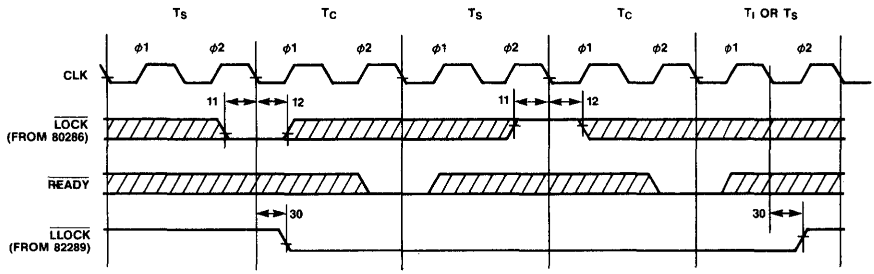
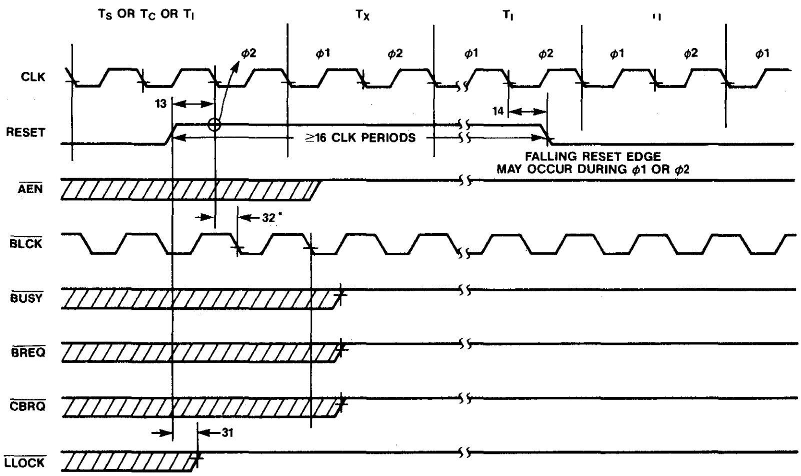


Figure 22. RESET Active Pulse



* FOR 82289 TEST PURPOSES ONLY

Figure 23. $\overline{INIT}$ Active Pulse

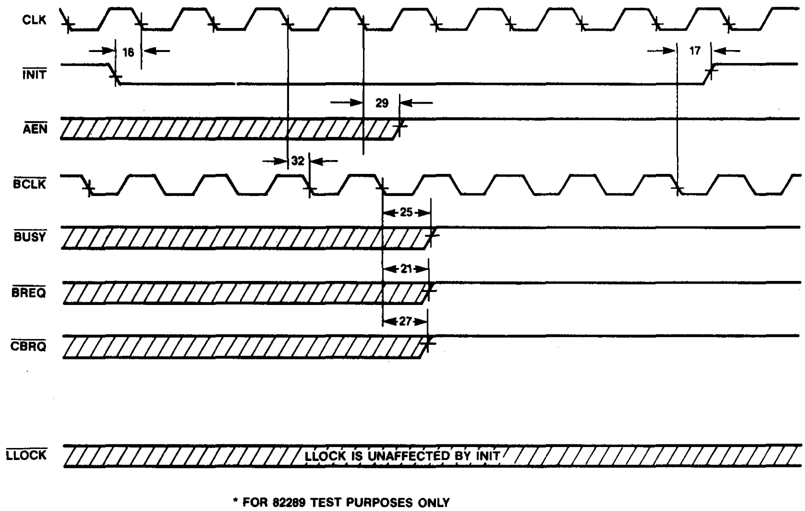
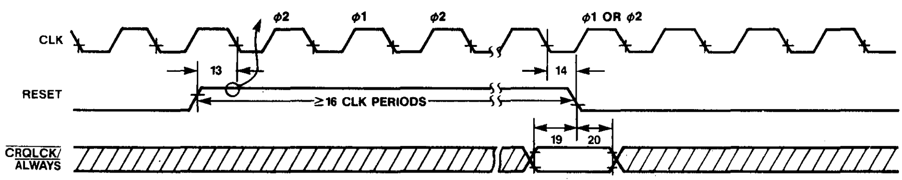
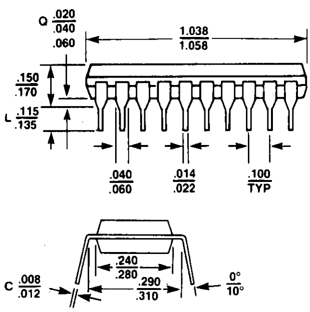


Figure 24. Programming the Always-Release/Common-Bus-Request-Release Option

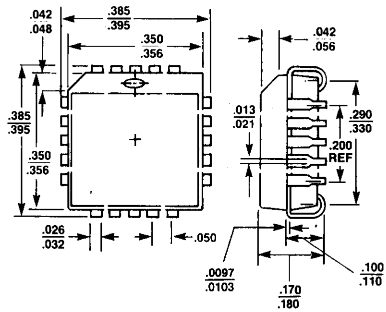


PACKAGE DIMENSIONS

20-pin DIP



20-pin PLCC



ALL DIMENSIONS IN INCHES

ORDERING INFORMATION AND PRODUCT CODE

KS 82C289 X X X

- **SAMSUNG SEMICONDUCTOR** — KS
- **Part Number** — 82C289
- **Speed**
  - -8.0 8.0MHz
  - -10.0 10.0MHz
  - -12.5 12.5MHz
  - -16.0 16.0MHz
- **Temperature**
  - C — Commercial (0°C to +70°C)
  - I — Industrial (-40°C to +85°C)
- **Packaging**
  - P — Plastic DIP
  - L — Plastic Leaded Chip Carrier (PLCC)

SAMSUNG products are designated by a Product Code. When ordering, please refer to products by their full code. For unusual, and/or specific packaging or processing requirements not covered by the standard product line, please contact the SAMSUNG MOS Product Group.

KS84C21/C22

DYNAMIC RAM CONTROLLERS

FEATURES

- Direct drive for 256K, 1Mbit and 4Mbit DRAMs
- Page, nibble and static column accesses
- Interleaved or non-interleaved accesses to maximize system performance
- Programmable or mask-programmed versions
- Programmable refresh operations
- Staggered and burst refresh
- Refresh operations virtually transparent to the CPU
- Programmable wait states
- Byte operation with four independent $\overline{CAS}$ outputs
- Easy interface to all major microprocessors
- Built in delay line
- Synchronous and asynchronous operation
- On-chip capacitive load drivers
- Can be used with 25MHz clock
- CMOS technology for low power consumption
- TTL-compatible inputs
- 68-pin PLCC package (KS84C21)
- 84-pin PLCC package (KS84C22)

PRODUCT OVERVIEW

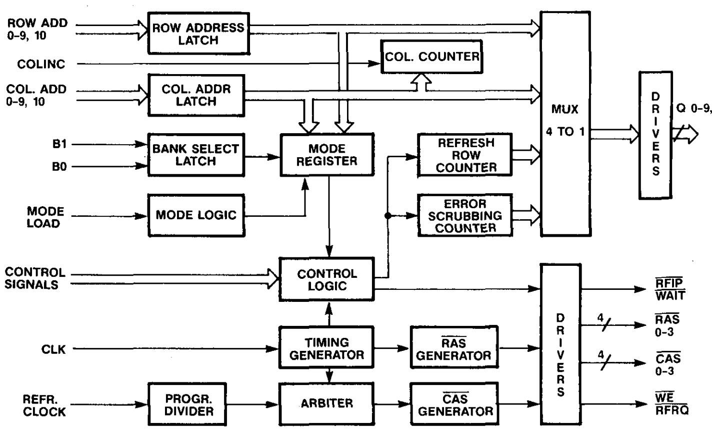
The Samsung KS84C21 and KS84C22 are high performance dynamic RAM (DRAM) controllers. They simplify the interface between the microprocessor and the DRAM array, while also significantly reducing the required design time. The KS84C21 supports the 256K DRAM and the 1MBit DRAM, while the KS84C22 supports the 256K DRAM, 1MBit DRAM and 4MBit DRAM.

Both devices are available in either externally programmable or masked programmable versions. The externally programmable version is an economic and flexible design solution for small-scale applications and prototyping. A 23-bit programmable Mode Register allows the selection of various options and features, including synchronous or asynchronous operation; interleaved or non-interleaved operation; burst or non-burst access; insertion of Wait States into the CPU cycle; a variety of refresh options; as well as the ability to fine tune the control signals.

A mask-programmed version of the chip offers the same Mode Register options. However, the chip is programmed at the factory to customer specifications. This version offers maximum system reliability and eliminates the need for external logic.

Both chips have a drive capability of 500pF, sufficient to drive memory arrays of up to 88 DRAMs under worst case conditions. Figure 1 shows a block diagram of the chips.

Figure 1. KS84C21/C22 Block Diagram



INTERFACE SPECIFICATIONS

The Dynamic Ram Controller is available in two packages. The KS84C21, shown in Figure 2 is a 68-pin device and supports the 256K DRAM and 1Mbit DRAM. The KS84C22, shown in Figure 3 is an 84-pin device designed for use with the 256K DRAM 1 and 4Mbit DRAM.

Figure 2. Pin Configuration of the KS84C21 DRAM Controller

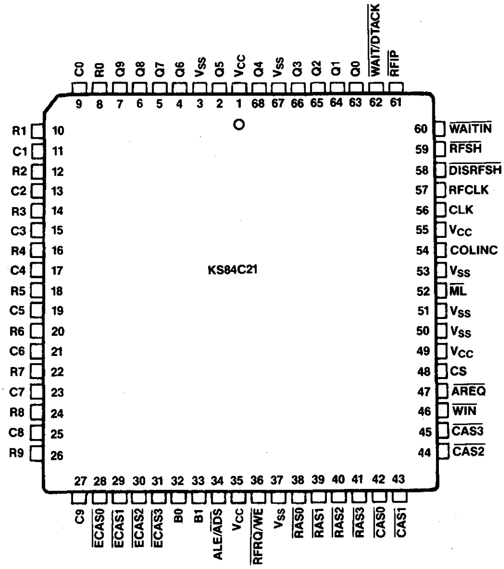
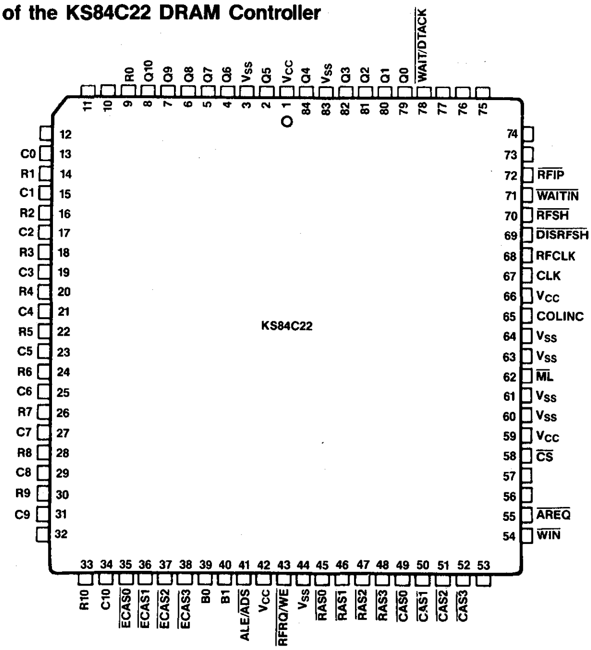


Figure 3. Pin Configuration of the KS84C22 DRAM Controller



3

Table 1 shows detailed pin allocations for the KS84C21, while Table 2 shows the KS84C22. Table 3 provides the input/output signal definitions.

Note on Conventions:
A bar over the signal name is used to denote an active low signal ($\overline{\text{ADS}}$). Active high signals are shown with no bar (ALE).

Table 1. KS84C21 Pin Allocations

Pin No.	Signal Abbrev.	Signal Name
1	V_{CC}	V_{CC}
2	Q5	Multiplexed Address 5
3	V_{SS}	V_{SS}
4	Q6	Multiplexed Address 6
5	Q7	Multiplexed Address 7
6	Q8	Multiplexed Address 8
7	Q9	Multiplexed Address 9
8	R0	Row Address 0
9	C0	Column Address 0
10	R1	Row Address 1
11	C1	Column Address 1
12	R2	Row Address 2
13	C2	Column Address 2
14	R3	Row Address 3
15	C3	Column Address 3
16	R4	Row Address 4
17	C4	Column Address 4
18	R5	Row Address 5
19	C5	Column Address 5
20	R6	Row Address 6
21	C6	Column Address 6
22	R7	Row Address 7
23	C7	Column Address 7
24	R8	Row Address 8
25	C8	Column Address 8
26	R9	Row Address 9
27	C9	Column Address 9
28	$\overline{\text{ECAS0}}$	Enable $\overline{\text{CAS0}}$
29	$\overline{\text{ECAS1}}$	Enable $\overline{\text{CAS1}}$
30	$\overline{\text{ECAS2}}$	Enable $\overline{\text{CAS2}}$
31	$\overline{\text{ECAS3}}$	Enable $\overline{\text{CAS3}}$
32	B0	Bank Select 0
33	B1	Bank Select 1
34	ALE/$\overline{\text{ADS}}$	Address Latch Enable/ Address Strobe
35	V_{CC}	V_{CC}
36	$\overline{\text{RFRQ}}$/WE	Refresh Request/Write Enable
37	V_{SS}	V_{SS}
38	$\overline{\text{RAS0}}$	Row Address Strobe 0
39	$\overline{\text{RAS1}}$	Row Address Strobe 1
40	$\overline{\text{RAS2}}$	Row Address Strobe 2
41	$\overline{\text{RAS3}}$	Row Address Strobe 3
42	$\overline{\text{CAS0}}$	Column Address Strobe 0
43	$\overline{\text{CAS1}}$	Column Address Strobe 1
44	$\overline{\text{CAS2}}$	Column Address Strobe 2
45	$\overline{\text{CAS3}}$	Column Address Strobe 3
46	$\overline{\text{WIN}}$	Write Enable Input
47	$\overline{\text{AREQ}}$	Access Request
48	$\overline{\text{CS}}$	Chip Select
49	V_{CC}	V_{CC}
50	V_{SS}	V_{SS}
51	V_{SS}	V_{SS}
52	$\overline{\text{ML}}$	Mode Load
53	V_{SS}	V_{SS}
54	COLINC	Column Increment
55	V_{CC}	V_{CC}
56	CLK	Clock
57	RFCLK	Refresh Clock
58	$\overline{\text{DISRFSH}}$	Disable Internal Refresh
59	$\overline{\text{RFSH}}$	External Refresh Request
60	$\overline{\text{WAITIN}}$	Add Wait State
61	$\overline{\text{RFIP}}$	Refresh in Progress
62	$\overline{\text{WAIT/DTACK}}$	Wait/Data Transfer Acknowledge
63	Q0	Multiplexed Address 0
64	Q1	Multiplexed Address 1
65	Q2	Multiplexed Address 2
66	Q3	Multiplexed Address 3
67	V_{SS}	V_{SS}
68	Q4	Multiplexed Address 4

Table 2. KS84C22 Pin Allocations

Pin No.	Signal Abbrev.	Signal Name
1	V_{CC}	V_{CC}
2	Q5	Multiplexed Address 5
3	V_{SS}	V_{SS}
4	Q6	Multiplexed Address 6
5	Q7	Multiplexed Address 7
6	Q8	Multiplexed Address 8
7	Q9	Multiplexed Address 9
8	Q10	Multiplexed Address 10
9	R0	Row Address 0
10	—	N.C.
11	—	N.C.
12	—	N.C.
13	C0	Column Address 0
14	R1	Row Address 1
15	C1	Column Address 1
16	R2	Row Address 2
17	C2	Column Address 2
18	R3	Row Address 3
19	C3	Column Address 3
20	R4	Row Address 4
21	C4	Column Address 4
22	R5	Row Address 5
23	C5	Column Address 5
24	R6	Row Address 6
25	C6	Column Address 6
26	R7	Row Address 7
27	C7	Column Address 7
28	R8	Row Address 8
29	C8	Column Address 8
30	R9	Row Address 9
31	C9	Column Address 9
32	—	N.C.
33	R10	Row Address 10
34	C10	Column Address 10
35	$\overline{\text{ECAS0}}$	Enable $\overline{\text{CAS0}}$
36	$\overline{\text{ECAS1}}$	Enable $\overline{\text{CAS1}}$
37	$\overline{\text{ECAS2}}$	Enable $\overline{\text{CAS2}}$
38	$\overline{\text{ECAS3}}$	Enable $\overline{\text{CAS3}}$
39	B0	Bank Select 0
40	B1	Bank Select 1
41	ALE/$\overline{\text{ADS}}$	Address Latch Enable/ Address Strobe
42	V_{CC}	V_{CC}
43	$\overline{\text{RFRQ/WE}}$	Refresh Request/Write Enable
44	V_{SS}	V_{SS}
45	$\overline{\text{RAS0}}$	Row Address Strobe 0
46	$\overline{\text{RAS1}}$	Row Address Strobe 1
47	$\overline{\text{RAS2}}$	Row Address Strobe 2
48	$\overline{\text{RAS3}}$	Row Address Strobe 3
49	$\overline{\text{CAS0}}$	Column Address Strobe 0
50	$\overline{\text{CAS1}}$	Column Address Strobe 1
51	$\overline{\text{CAS2}}$	Column Address Strobe 2
52	$\overline{\text{CAS3}}$	Column Address Strobe 3
53	—	N.C.
54	$\overline{\text{WIN}}$	Write Enable Input
55	$\overline{\text{AREQ}}$	Access Request
56	—	N.C.
57	—	N.C.
58	$\overline{\text{CS}}$	Chip Select
59	V_{CC}	V_{CC}
60	V_{SS}	V_{SS}
61	V_{SS}	V_{SS}
62	$\overline{\text{ML}}$	Mode Load
63	V_{SS}	V_{SS}
64	V_{SS}	V_{SS}
65	COLINC	Column Increment
66	V_{CC}	V_{CC}
67	CLK	Clock
68	RFCLK	Refresh Clock
69	$\overline{\text{DISRFSH}}$	Disable Internal Refresh
70	$\overline{\text{RFSH}}$	External Refresh Request
71	$\overline{\text{WAITIN}}$	Add Wait State
72	$\overline{\text{RFIP}}$	Refresh in Progress
73	—	N.C.
74	—	N.C.
75	—	N.C.
76	—	N.C.
77	—	N.C.
78	$\overline{\text{WAIT/DTACK}}$	Wait/Data Transfer Acknowledge
79	Q0	Multiplexed Address 0
80	Q1	Multiplexed Address 1
81	Q2	Multiplexed Address 2
82	Q3	Multiplexed Address 3
83	V_{SS}	V_{SS}
84	Q4	Multiplexed Address 4

Table 3. Interface Signal Definitions

Note: I indicates an input signal. O indicates an output signal. Timing notations (t12) etc. are referenced to the timing diagrams at the end of the product description.

Symbol	Type	Description
ADS/ALE	I	**Address Strobe/Address Latch Enable:** This input latches row, column and bank addresses, and initiates DRAM access. Addresses are strobed independently of CS, however CS must be low to initiate an access. While ADS or ALE is high, the on-chip address latches are transparent to the input. In Mode 0: This input functions as address latch enable ALE. In Mode 1: This input is active low, and functions as address strobe signal. The falling edge of ADS also starts an access, if CS is low for the set-up time t12. (Mode is selected by Bit B1 in the Mode Register. See PROGRAMMING THE KS84C21/C22.)
AREQ	I	**Access Request:** This input terminates an access. In non-interleave mode: it brings RAS high. In interleave mode: it brings CAS and RAS high.
B0, B1	I	**Bank Select:** These inputs are bank addresses, and allow one of up to four memory banks to be selected. Selection depends upon how C4, C5 and C6 in the Mode Register are set.
C0-9, 10	I	**Column Address Inputs:** These column address bits are usually connected to the high order address bits of the microprocessor. They select columns in the DRAM cell configuration.
CAS0-3	O	**Column Address Strobe:** These inputs strobe the column address. They go low after the programmed Column Address Set-up time of 0 or 10ns.
CLK	I	**Clock:** This is the system clock. It is used for bus arbitration and timing purposes. Synchronous access requests must be synchronized with the system clock. The duty cycle is significant if 1/2 Wait State is programmed.
CS	I	**Chip Select:** The CS input must be low to enable a DRAM access. Row, column and bank address are strobed independently of CS. There is a pre-access setup time. In Mode 0 this is the rising edge of CLK, and in Mode 1 the falling edge of ADS.
COLINC/ EXTDRF	I	**Column Increment/Extend Refresh:** This input has two functions. During a DRAM access, toggling COLINC increments the latched column address, which can be used to access incremental memory locations within a row. During refresh, EXTDRF extends a refresh cycle, to allow a read-modify-write cycle to be performed in a system with error correction. See ERROR SCRUBBING.
DISRFSH	I	**Disable Internal Refresh:** When low, this input disables Internal Refresh.
ECAS0-3	I	**Enable CAS0-3:** These inputs are used to enable or disable individual CAS outputs, or delay CAS from going low. They are useful when accessing bytes, nibbles or pages. ECAS0 also programs output WE (RFRQ), and sets the trailing edge of CAS.

Table 3. Interface Signal Definitions (Continued)

Symbol	Type	Description
$\overline{ML}$	I	**Mode Load:** This input latches the row, column, $\overline{ECAS0}$, and bank address inputs into the Mode Register.
Q0-9, 10	O	**Address Outputs:** These outputs are the multiplexed address bits (R0-10, C0-10). They access the memory for read, write and refresh operations. The output load may be as high as 500pF.
R0-9, 10	I	**Row Address Inputs:** These address inputs are usually connected to the low order address bits of the microprocessor. They select rows in the DRAM cell configuration.
$\overline{RAS0-3}$	O	**Row Address Strobe:** These row address strobe signals are used to strobe the row addresses into the DRAM.
RFCLK	I	**Refresh Clock:** This input determines the timing of the refresh cycles for the DRAMs. It should be a multiple of 2MHz. It is divided according to bits C0, 1, 2, and C3 in the Mode Register, so that the refresh cycles occur at 15μs or 13μs intervals.
$\overline{RFIP}$	O	**Refresh in Progress:** This output indicates that a refresh cycle is in progress. $\overline{RFIP}$ goes low one CLK cycle prior to the start of a refresh cycle.
$\overline{RFSH}$	I	**External Refresh Request:** Refresh cycles can be requested externally by driving the $\overline{RFSH}$ signal low.
$\overline{WAITIN}$	I	**Add Wait State:** If this input is low, one or two extra Wait States will be added to the access cycle at an external event, e.g. memory read.
$\overline{WAIT/DTACK}$	O	**Wait/Data Transfer Acknowledge:** This output inserts Wait States into CPU access cycles. The output is controlled by bits R2, R3, R4, R5 and R7, in the Mode Register.
$\overline{WE/RFRQ}$	O	**Write Enable/Refresh Request:** After Power up reset and in interleave mode, this output functions as refresh request. In non-interleave mode it can be programmed to function as the $\overline{WE}$ output if $\overline{ECAS0}$ is low in the Mode Register.
$\overline{WIN}$	I	**Write Enable Input:** This input controls the $\overline{WE}$ output, and delays $\overline{CAS}$, if programmed to do so by bit C9 in the Mode Register.

KS84C21/22 OPERATION

Introduction

The KS84C21/22 support both synchronous and asynchronous operations; interleaved or non-interleaved accesses; burst and non-burst accesses, and a variety of refresh operations. They generate all the signals required to control these various functions, by means of the Mode Register. (See PROGRAMMING THE KS84C21/22.) Timing characteristics for typical operations are shown under AC SWITCHING CHARACTERISTICS.

Reset

Power Up Reset

The KS84C21/22 on-chip power-up reset logic generates a reset pulse:

- At power up;
- If V_{CC} falls well below +3.0V, and reaches V_{CC} min. (Short spikes below the minimum V_{CC} will not reset the chip. However, correct functionality is guaranteed only within the operating conditions.)

When the chip is reset, all internal flip-flops, counters, and the Mode register are reset, and the output lines are inactive: $\overline{RAS0-3}$, $\overline{CAS0-3}$, $\overline{WAIT}$ ($\overline{DACK}$), $\overline{RFIP}$, $\overline{WE}$ ($\overline{RFRQ}$) are high, while Q0-9, 10 are low. Note that there are no tri-state buffers on any of the outputs.

The chip does not need any time to synchronize after power up, it is operable after 200 microseconds, as required by most DRAMs.

After power-up reset, the Mode Register must be reprogrammed in the programmable version of the chip.

External Reset

The Mode Load signal ($\overline{ML}$) can also be used to reset the chip. When $\overline{ML}$ is driven low, all counters and flip-flops are reset, and the Mode Register is enabled to receive the mode bit inputs.

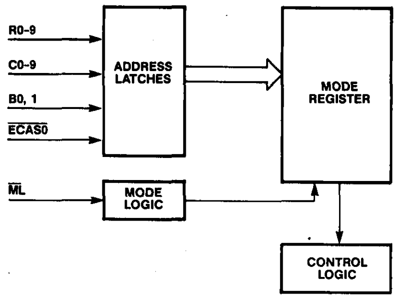
Programming the KS84C21/22

The KS84C21/22 has a Mode Register that can be programmed by the user, or mask-programmed at the factory. The outputs from the register control the internal program modes.

Mode Register

Figure 4 shows data flow to and from the Mode Register.

Figure 4. Mode Register Data Flow



The Mode Register receives inputs from the CPU on the address lines: Row addresses R0-9, Column address C0-9, and Bank addresses B0, B1 and $\overline{ECAS0}$. These bits are loaded into the Register when Mode Load ($\overline{ML}$) goes low. Alternatively, the Mode Register may be programmed by initiating a 'dummy' access, as shown in the Mode Load Timing Characteristics (Figure 11, AC Switching Characteristics). $\overline{ML}$, $\overline{CS}$ and $\overline{AREQ}$ are asserted, the addresses are loaded into the Mode Register on the falling edge of $\overline{AREQ}$, while $\overline{ML}$ and $\overline{CS}$ are low, or when $\overline{ML}$ goes high (whichever occurs first).

It is necessary to program the chip after power up, and before using it in normal operation. The inputs to the register are encoded to control a variety of functions, as shown in Table 4. Note that inputs R10 and C10 of the KS84C22 do not program the Mode Register.

Table 4. Programming the Mode Register

ADDRESS LATCH

B0

B0 allows the user to decide whether address inputs should be latched by $\overline{ADS}$/ALE, or whether the address latches should be permanently transparent and merely allow passage of the address inputs.

B0	
0	Address bits latched.
1	Address latches transparent.

ACCESS MODES

B1

B1 allows the user to select either synchronous or asynchronous access modes.

In Mode 0 (synchronous), access is controlled by the system clock, and the access $\overline{RAS}$ is initiated on the rising edge of the first clock input after ALE goes high. $\overline{AREQ}$ is used to hold $\overline{RAS}$ low during access.

In Mode 1 (asynchronous), the leading edge of $\overline{ADS}$ initiates access immediately, and the trailing edge of $\overline{AREQ}$ terminates $\overline{RAS}$.

B1	
0	Access Mode 0 (synchronous)
1	Access Mode 1 (asynchronous)

ENABLE COLUMN ADDRESS STROBE

$\overline{ECAS0}$

Controls the $\overline{CAS}$ outputs. Only one $\overline{ECAS}$ Mode Register.

$\overline{ECAS0}$	
0	$\overline{CASn}$ outputs are negated with $\overline{AREQ}$ in non-interleave mode. $\overline{WE}$ output is selected.
1	$\overline{CASn}$ outputs can be held low until the rising edge of CLK, after $\overline{RAS}$ is deasserted in non-interleave mode. $\overline{RFRQ}$ is selected.

$\overline{RAS}$ LOW AND $\overline{RAS}$ PRECHARGE TIME

R0, R1

These bits control the period of time that $\overline{RAS}$ is low during refresh operations, and also determine the guaranteed $\overline{RAS}$ precharge time. The time interval shown (T) is equivalent to one Clock (CLK) cycle.

R0	R1	$\overline{RAS}$ Low Time	$\overline{RAS}$ Precharge Time
0	0	2T	1T
0	1	2T	2T
1	0	3T	2T
1	1	4T	3T

Table 4. Programming the Mode Register (Continued)

WAIT OR DTACK GENERATION FOR NON-BURST MODE ACCESSES

R2, R3, R7

These bits control the WAIT or DTACK generation modes for R7 non-burst accesses. Bit R7 is set to select either WAIT or DTACK type of output. The time interval shown (T) is equal to one Clock cycle.

R7	R2	R3	WAIT High from Access RAS Low. Non-delayed Access	WAIT High from Access RAS Low, After Delayed Access	DTACK Low from RAS Low
0	0	0	No wait states	0T	—
0	0	1	No wait states	1/2T	—
0	1	0	1/2T	1/2T	—
0	1	1	1T	1T	—
1	0	0	—	—	0T
1	0	1	—	—	1/2T
1	1	0	—	—	1T
1	1	1	—	—	1-1/2T

WAIT OR DTACK GENERATION FOR BURST MODE ACCESSES

R4, R5

R4 and R5 Control WAIT or DTACK generation modes during burst mode accesses.

R4	R5	Condition	
0	0	No wait states.	WAIT stays high and DTACK stays low from previous access.
0	1	1/2T.	WAIT goes high on the falling edge of the next CLK.
1	0	1T.	WAIT goes high on the rising edge of the next CLK. DTACK goes low one click cycle after CAS.
1	1	0T.	WAIT(DTACK) follows CAS.

ADDS WAIT STATE

R6

R6 adds wait states to the current access if WAITIN is low.

R6	Condition
0	Hold WAIT low (DTACK high) for one extra clock period.
1	Hold WAIT low (DTACK high) for two extra clock periods.

3

Table 4. Programming the Mode Register (Continued)

INTERLEAVING	
R8	R8 Determines whether the DRAM is accessed in interleaved or non-interleaved mode. In interleaved mode, the row addresses are multiplexed to the DRAM controller address outputs, after the column addresses have been held for a sufficient time (35ns minimum) after $\overline{CAS}$ has gone low. In non-interleaved mode, the column addresses are held on the DRAM controller address outputs until $\overline{CAS}$ goes high.
STAGGERED REFRESH OPERATIONS	
R9	R9 determines whether the refresh operation is standard, or staggered. During a standard refresh cycle, all $\overline{RAS}$ outputs will be asserted and deasserted at the same time. In staggered refresh operations, the $\overline{RAS}$ outputs will go low in sequence, at one clock intervals. One or two $\overline{RAS}$ outputs are selected at a time, depending upon the $\overline{RAS}/\overline{CAS}$ configuration selected by the setting of C4-C6. There is no error scrubbing during this type of refresh.
RFCLK DIVIDER	
C0, C1, C2	These bits allow the user to select the divider for the refresh clock input (RFCLK), from which the internal REFRESH clock is generated. Select divider such that the result is an approximately 2MHz clock (REFRESH).

R8	
0	Interleaved mode
1	Non-interleaved mode

R9	
0	Standard refresh
1	Staggered refresh

C0	C1	C2	
0	0	0	Divide by 10
0	0	1	Divide by 6
0	1	0	Divide by 8
0	1	1	Divide by 4
1	0	0	Divide by 9
1	0	1	Divide by 5
1	1	0	Divide by 7
1	1	1	Divide by 3

Table 4. Programming the Mode Register (Continued)

REFRESH CLOCK DIVIDER

C3

C3 allows the user to divide the internal refresh clock (REFRESH), to get the required refresh cycle time.

C3	
0	Divide by 30. Divides the internal REFRESH clock (usually 2MHz) by 30, to produce a refresh clock period every 15 microseconds.
1	Divide by 26. Divides the internal REFRESH clock (usually 2MHz) by 26, to produce a refresh clock period every 13 microseconds.

RAS AND CAS CONFIGURATIONS

C4, C5, C6

These bits, in conjunction with B0 and B1 control the RAS and CAS configurations. There are four and four CAS outputs, that can be grouped so that each RAS and CAS will drive one fourth of the array, regardless of whether the array is arranged in 1, 2 or 4 banks. The setting of these bits also determines whether error scrubbing and interleaving can be supported.

<table>
<tr><th>C4</th><th>C5</th><th>C6</th><th>RAS and CAS Configuration Modes</th><th>Error Scrubbing</th><th>Support Interleaving</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>RAS0-3 are brought low during an access. CAS0-3 are all selected during an access but only those enabled by the corresponding ECAS can go low. B0 and B1 are not used.</td><td>Yes</td><td>No</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>RAS groups are selected by B1. B0 is not used. All CAS outputs are selected, making this mode useful for byte writing via ECAS0-3 inputs and the CAS0-3 outputs.
<table><tr><th>B1</th><th>B0</th><th></th></tr><tr><td>0</td><td>—</td><td>RAS0, 1</td></tr><tr><td>1</td><td>—</td><td>RAS2,3</td></tr></table></td><td>No</td><td>No</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>RAS, CAS pairs selected by B0, A particular CAS cannot go low unless its ECAS is also low.
<table><tr><th>B1</th><th>B0</th><th></th></tr><tr><td>0</td><td>0</td><td>RAS0 and CAS0</td></tr><tr><td>0</td><td>1</td><td>RAS1 and CAS1</td></tr><tr><td>1</td><td>0</td><td>RAS2 and CAS2</td></tr><tr><td>1</td><td>1</td><td>RAS3 and CAS3</td></tr></table></td><td>Yes</td><td>Yes</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>RASn is selected by B0 and B1. CAS outputs are selected, making this mode useful for byte writing via ECAS0-3 inputs and the CAS0-3 outputs.
<table><tr><th>B1</th><th>B0</th><th></th></tr><tr><td>0</td><td>0</td><td>RAS0</td></tr><tr><td>0</td><td>1</td><td>RAS1</td></tr><tr><td>1</td><td>0</td><td>RAS2</td></tr><tr><td>1</td><td>1</td><td>RAS3</td></tr></table></td><td>No</td><td>No</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>RAS, CAS groups selected by B1. A particular CAS cannot go low unless its ECAS is also low.
<table><tr><th>B1</th><th>B0</th><th></th></tr><tr><td>0</td><td>—</td><td>RAS0, 1 and CAS0, 1</td></tr><tr><td>1</td><td>—</td><td>RAS2, 3 and CAS2, 3</td></tr></table></td><td>Yes</td><td>Yes</td></tr>
</table>

Table 4. Programming the Mode Register (Continued)

RAS AND CAS CONFIGURATIONS (Continued)

C4	C5	C6	RAS and CAS Configuration Modes	Error Scrubbing	Support Interleaving
1	0	1	RAS, CAS groups are selected by B1. A particular CAS cannot go low unless its ECAS is also low. B1 | B0 | 0 | — | RAS0, 1 and CAS0, 1 1 | — | RAS2, 3 and CAS2, 3	No	Yes
1	1	0	RAS0-3 and CAS0-3 are all selected during an access. This mode is useful for byte writing via ECAS0-3 inputs and the CAS0-3 outputs. B0 and B1 are not used.	No	No
1	1	1	RASn and CASn are selected by B0 and B1. A particular CAS cannot go low unless its ECAS is also low. B1 | B0 | 0 | 0 | RAS0 and CAS0 0 | 1 | RAS1 and CAS1 1 | 0 | RAS2 and CAS2 1 | 1 | RAS3 and CAS3	No	Yes

COLUMN ADDRESS SETUP TIME SELECTION

C7 — C7 allows the user to select a minimum guaranteed setup time (t_{ASC}) for the column address inputs.

C7	
0	Selects 10ns setup time.
1	Selects 0ns setup time.

ROW ADDRESS HOLD TIME SELECTION

C8 — C8 allows the user to select a minimum guaranteed hold time (t_{RAH}) for the row address inputs.

C8	
0	Selects 25ns hold time.
1	Selects 15ns hold time.

DELAY CAS DURING WRITE ACCESSES

C9 — C9 allows the user to delay CAS during write operations. If no delay is selected, CAS is treated in the same way for read and write operations. If delay is selected, CAS is delayed for one rising clock edge after RAS goes low.

C9	
0	No delay.
1	Delay selected.

Standard Access Operations

The versatile KS84C21/C22 chips support a variety of DRAM operations. They enable read and write accesses, in synchronous or asynchronous mode, with or without interleaving, and in burst or non-burst mode. Typical operations are illustrated in the timing diagrams at the end of this Product Description.

Operating Features

DRAM performance is optimized under the control of the KS84C21/C22, as a function of the special operating features designed into the chips. This section describes some of the features that enhance DRAM performance.

Controlling Precharge Time

The precharge time of the DRAM, or the time the chip takes to stabilize between accesses, negatively impacts the overall access speed of the memory devices. Since the DRAM performance is generally trailing CPU throughput time, the DRAM controller can play an important role in improving overall system performance.

$\overline{RAS}$ Low and $\overline{RAS}$ Precharge Time. RAS precharge time can be programmed using bits R0 and R1 in the Mode Register. The precharge time is guaranteed during access and refresh. $\overline{RAS}$ low and $\overline{RAS}$ precharge times are counted by the rising edges of the CLK input. Each bank of memory devices has its own precharge counter. This is an important feature, since the KS84C21/C22 allows memory interleaving of 2 or 4 memory banks.

$\overline{AREQ}$ must go high at tC22 with respect to the rising edge of the CLK input, to be counted as 1T of the programmed precharge time. (This means that 1T can be somewhat less than one clock period.)

The KS84C21/C22 inserts Wait States as required, to keep the CPU and DRAM interactions in step. The system designer is responsible, however, for making sure that the appropriate numbers of Wait States are inserted to keep $\overline{RAS}$ low for the period of time required by the DRAM specification.

$\overline{CAS}$ Precharge Time. The $\overline{ECASn}$ input controls $\overline{CAS}$ precharge time during a burst access. The $\overline{CASn}$ output is a direct function of the $\overline{ECASn}$ input. The KS84C21/C22 does not monitor precharge time t_{CP} or t_{NCP} in a page or nibble access.

Access Features

The KS84C21/C22 enables a number of types of DRAM access, that either enhance DRAM performance, or increase the DRAM's flexibility in specific applications.

Static Column Access. With this type of access, a specific memory row is accessed, and the column addresses to that row are toggled, enabling sequential accesses, without invoking a succession of $\overline{RAS}$ and $\overline{CAS}$ signals. The input addresses can be either latched or fall-through, as programmed by bit B0 in the Mode Register. This feature does not support random row accesses.

Page Access. For such applications as frame buffer, or printer buffer, the KS84C21/C22 support fast page accesses, in which a specific row is accessed, and incremental column addresses within that row are accessed sequentially. The built in column counter provides the column address. If the row changes, a new access must be initiated with $\overline{ADS}$ or ALE. This feature does not support random row accesses.

Memory Interleaving. Performance is similarly enhanced if consecutive accesses are made to different memory banks by hiding the precharge time in the access of subsequent access cycle. The KS84C21/C22 supports access to up to 88 DRAMs, arranged in up to four banks, each containing 16 memory devices for data and 6 for error correction. The bank address bits, B0 and B1 are the least significant bits, as seen by the CPU. The KS84C21/C22 ensures that the DRAM will be precharged for the programmed number of CLK cycles by inserting Wait States. The precharge counter, as programmed by R0 and R1, keeps track of the CLK inputs, and after reaching the programmed number, the rising edge of the next CLK input is used to complete the current cycle. The precharge counter starts with the rising edge of the first CLK input (which is counted as 1T) that occurs after the low-to-high transition of $\overline{AREQ}$. There is a required setup time to the rising edge of CLK of tC22.

Delay $\overline{CAS}$

An early write cycle to a DRAM is useful if the input data is not stable at the falling edge of $\overline{WE}$, or if bidirectional data buffers are used. With this sort of access, $\overline{WE}$ goes low before $\overline{CAS}$ is low. The column address bits and data are stored in the DRAM latches on the falling edge of $\overline{CAS}$. The data output buffer of the DRAM is tri-stated during the entire $\overline{RAS}$ cycle.

To achieve an early write cycle, the CAS output of the KS84C21/C22 can be delayed one CLK cycle, if bit C9 of the Mode Register is set appropriately. CAS will go low tC24 after the rising edge of CLK. If CAS has been delayed in this way, and requires further delay, this can be done by holding ECASn high, which prevents CAS from going low.

Conversely, a late write access may be required, in which WE is asserted after CAS. In this case, the column address bits are latched into the DRAMs on the falling edge of CAS and the input data is latched on the falling edge of WE.

Wait States

Wait states are required when a relatively slow DRAM is operating with a fast CPU. The KS84C21/C22 generates the WAIT signal, and sends it back to the CPU instructing it to insert a Wait. This means that the CPU will not look for data prematurely, and during a Refresh operation, an access is deferred. Bit R7 of the Mode Register must be set to '0' to instigate this feature.

If the Wait state is not selected, the KS84C21/C22 generates a handshaking signal, DTACK, which is returned to the CPU to acknowledge transfer of data.

Refresh Operations

The KS84C21/22 provide a number of refresh options, as described below.

Automatic Internal Refresh

Internal refresh is generated by an internal refresh counter, which keeps track of the refresh intervals, and also supplies the row address bits required to refresh the memory area. (Internal refresh is a RAS-only operation.) The refresh period is selected by bits C0, C1, C2 and C3 of the Mode Register.

The refresh period for most DRAMs is 15 microseconds. This means that the one megabit DRAM has to be refreshed every eight milliseconds, during which time, 512 rows must be accessed. This calls for a 9-bit refresh counter. The KS84C21 has a 10-bit counter, and the C22 has an 11-bit counter. The extra bits are used for error scrubbing over the whole address range.

If a refresh is requested by the on-chip Refresh counter, while an access is in progress, that access is finished before the refresh cycle is initiated. The next access is deferred until the refresh cycle is complete. The wait logic automatically inserts Wait States.

Internal refresh is possible in both interleaved and non-interleaved modes.

Automatic Internal Staggered Refresh

Staggered refresh, during which the RAS signals are staggered at one CLK intervals, can be selected by appropriately setting bit R9 in the Mode Register. This type of cycle allows the memory area to be refreshed in two or four refresh operations that are interspersed with regular memory accesses. Staggering refresh operations reduces the switching current.

External Controlled Refresh

Refresh operations can be controlled externally and can be either 'all RAS' or staggered. As for internal refresh, the row address bits are supplied by the on-chip refresh counter.

Internal refresh must be disabled by driving DISRFSH low. RFSH must go low at setup time tR1.

Refresh Request Divider

The refresh request divider (derived from the programmable divider asserts RFRQ externally, if internal or external refresh has been selected by DISRFSH.

Clearing the Refresh Counter (Row Address)

The refresh counter is cleared by driving DISRFSH high and RFSH low, with a setup time of tR1 to the rising edge of CLK. This procedure does not invoke a refresh of the DRAM.

Error Scrubbing

In a system with error correction, transparent error scrubbing is one method of increasing data integrity. A full access is performed during refresh, during which data and ECC bits are continuously updated and checked, and random bit errors corrected. The error scrubbing option is selected by appropriately setting bits C4, C5 and C6 of the Mode Register.

When the KS84C21/22 are programmed for error scrubbing, a complete memory access is performed during the refresh cycle. The 12- or 13-bit internal scrubbing counter provides the column address bits, and the 10- or 11-bit refresh counter provides the row address bits. Error scrubbing is done by word, not by byte.

If the error correction circuitry detects an error, the error is corrected by writing the corrected word to the DRAM by means of the read-modify-write operation. (The data is read and checked during the read portion, and modified/corrected data is written back during the write portion.)

To enable this type of cycle, EXTDRF must be asserted while $\overline{RAS}$ is low. $\overline{RAS}$ and $\overline{CAS}$ remain low until the rising edge of the next CLK, after EXTDRF has gone low again.

Although the KS84C21/22 control the error scrubbing, they do not provide the error correction circuitry.

Access Modes

The KS84C21/22 supports both synchronous and asynchronous operations. The user can select the mode most suited to the microprocessor with which the DRAM is interfacing, by means of bit B1 in the Mode Register.

Mode 0 — Synchronous Access

Mode 0 is selected when B1 = 0. To initiate a Mode 0 operation, ALE must pulse high t02 before the rising edge of the clock input (CLK). Provided that the chip select signal ($\overline{CS}$) has been established at t01 before the rising edge of the next CLK input, access will start on the rising edge of that CLK.

Since ALE is high, the address latch is transparent to the address inputs, and, if the chip is programmed in Address Latch Mode (B0 = 0), the latch stores the address bits that were present one setup time (t06) before the high-to-low transition of ALE. If the chip is not in Latch Mode (B0 = 1), the address inputs have to meet the setup time of t05 to the rising edge of CLK, to make sure that the row address bits are on the Q output when row address strobe ($\overline{RAS}$) is asserted.

Mode 1 — Asynchronous Access

Mode 1 is selected when B1 = 1. To initiate a Mode 1 operation, $\overline{CS}$ must be low for t12 before $\overline{ADS}$ goes low. If the chip is programmed in Address Latch Mode, the address latch, which is transparent to address inputs while $\overline{ADS}$ is high, stores the address that was present one set up time t14 before the high-to-low transition of the $\overline{ADS}$ signal.

Interleaving

The KS84C21/22 support both interleaved and non-interleaved memory operation. Interleaving is controlled by the R8 input to the Mode Register.

Interleaving

With R8 set at 0, the chip supports interleaved accessing of the DRAM. This is a way of reducing access cycle time. In interleaved mode, access cycles (read or write) are overlapped, so that before an access cycle is completed in one memory bank location, another access may be started in a different memory bank. Since the precharge time of most DRAMs is between 80 and 100 nanoseconds (about the same length as t_{RAS}), interleaving can save up to 50% of cycle time.

Memory accesses can only be overlapped in physically separated banks of memory, and may occur during precharge time.

Interleaving can take place in either Mode 0 or Mode 1.

Non-Interleaving

When R8 is set at 1, the chip does not support interleaving. The address lines from the microprocessor are connected to the Row (R), Column (C), and Bank (B) inputs of the KS84C21. B0 and B1 (bank address bits) may be connected to the most significant or the least significant address bits.

Access starts in Mode 0 if ALE pulses high t02 before the edge of the CLK input. In 1, access starts when CS remains low for t12 before the falling edge of $\overline{ADS}$. In both cases, access is terminated when $\overline{AREQ}$ goes high, terminating $\overline{RAS}$. $\overline{CAS}$ goes high or stays low until the rising edge of the next CLK, as programmed by $\overline{ECAS0}$

DC ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

DC Supply Voltage 7V
Temperature Under Bias .... 0°C + 70°C
Storage Temperature .... -65°C to 150°C
All Input and Output Voltage ..... V_{SS} - 0.5V to +7V
Power Dissipation at 25MHz 0.6W
E.S.D. 2000V

Note: If the device is used beyond the maximum rating, permanent damage may occur. Operation should be limited to those conditions specified under DC Electrical Characteristics.

DC Electrical Characteristics (T_A = 0°C to +70°C, V_{CC} = 4.5V to 5.5V, V_{SS} = 0V)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input High Voltage	Tested with limited Test pattern	2.0		V_{CC}+0.5	V
V_{IL}	Input Low Voltage	Tested with limited Test pattern	-0.5		0.8	V
V_{OH1}	Q and $\overline{WE}$ Outputs	I_{OH} = -10mA	2.4			V
V_{OL1}	Q and $\overline{WE}$ Outputs	I_{OL} = 10mA			0.5	V
V_{OH2}	All outputs except Q and $\overline{WE}$	I_{OL} = -3mA	2.4			V
V_{OL2}	All outputs except Q and $\overline{WE}$	I_{OL} = 3mA			0.5	V
I_{IN}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}			±10	μA
I_{ILML}	$\overline{ML}$ Input Current	V_{IN} = V_{SS}			200	μA
I_{CC1}	Quiescent Current	CLK at 25MHz Inputs Inactive			15	mA
I_{CC2}	Supply Current	Inputs Active (I load = 0)			2.5	mA/MHz
C_{IN}	Input Capacitance	f_{IN} at 1MHz		5	10	pF

AC SWITCHING CHARACTERISTICS

Figure 5 shows a typical test circuit, while Figure 6 shows the output drive levels. Figures 7 through 14 provide switching characteristics for a number of typical KS84C21/C22 operations:

- Figure 7. Mode 0 Interleave
- Figure 8. Mode 0 Wait State, Non-Interleave
- Figure 9. Mode 1 Interleave, Address Latch
- Figure 10. Burst Access, Page Mode
- Figure 11. Non-Interleave, Delay $\overline{CAS}$
- Figure 12. Mode Load
- Figure 13. CLK, RFCLK Timing
- Figure 14. Internal Refresh
- Figure 15. Refresh and Extend Refresh
- Figure 16. Staggered Refresh

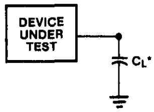
Unless otherwise stated V_{CC} = 4.5V to 5.5V, 0 < T_A < 70°C

Load Capacitance: Q0-Q9, Q10 — C_L = 500pF
$\overline{WE}$ — C_L = 700pF
$\overline{RAS0-3}$, $\overline{CAS0-3}$ — C_L = 175pF
All other Outputs — C_L = 50pF

All minimum and maximum values are measured in nanoseconds.

CAPACITIVE LOAD SWITCHING

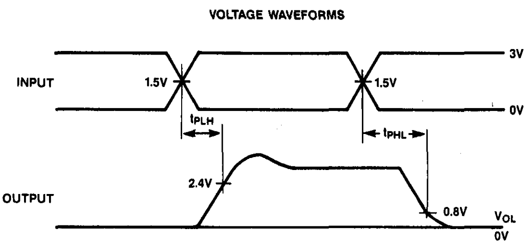
Figure 5. Switching Test Circuit



*t_{pd} SPECIFIED AT C_L = 500pF ALL Q OUTPUTS
C_L = 175pF RAS AND CAS OUTPUTS
C_L = 700pF $\overline{WE}$ OUTPUT

TYPICAL SWITCHING CHARACTERISTICS

Figure 6a. Output Drive Levels



AC Testing inputs are driven at 3.0V for a logic "1" and 0.0V for a logic "0". Timing measurements are made at 2.4V for a logic "1" and 0.8V for a logic "0" at the outputs.

Figure 6b. Simplified Output Driver Schematic

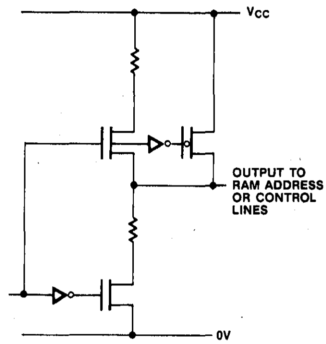
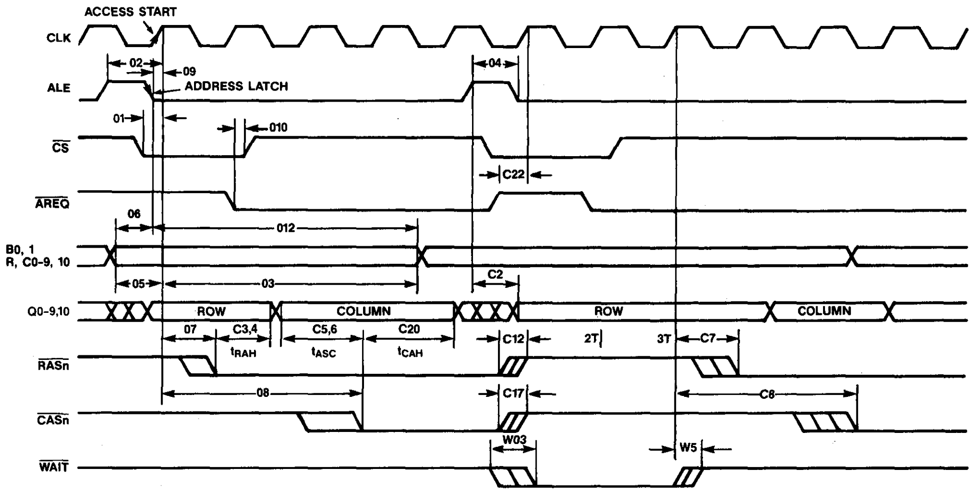


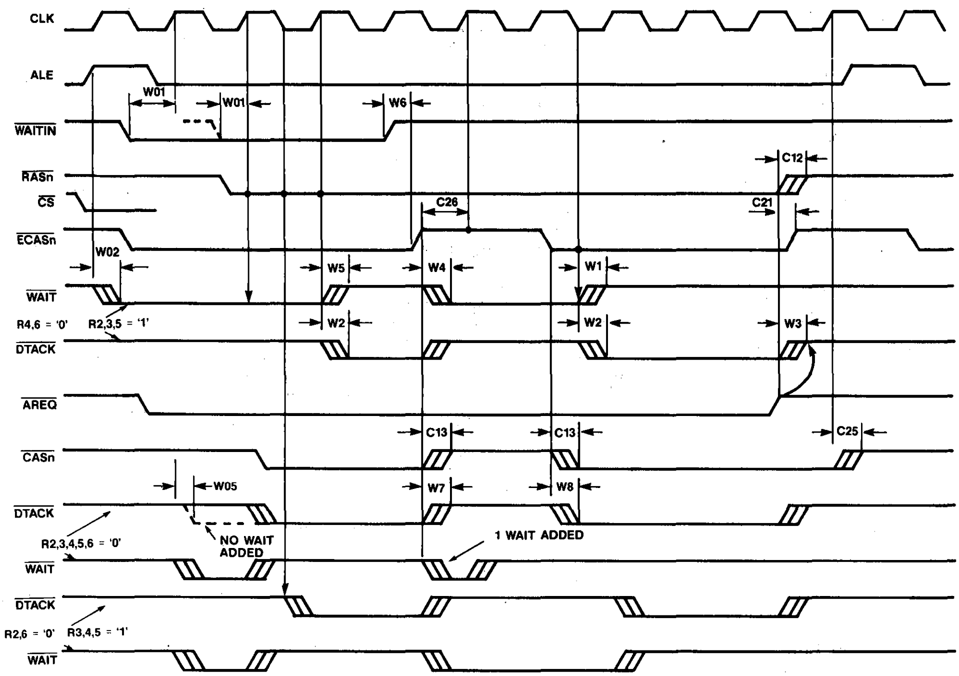
Figure 7. Mode 0 Interleave



No.	Parameter	Min	Max
01	$\overline{CS}$ Low to CLK Rising Edge	10	
02	ALE High to CLK Rising Edge	15	1T
03	Address Hold Time from CLK Rising Edge not using the on-Chip Address Latch	t08	
04	ALE Pulse Width	15	
05	Address Set-up to CLK Rising Edge not using the On-Chip Address Latch	20	
06	Address Set-up to ALE Falling Edge using the On-Chip Address Latch	3	
07	CLK Rising Edge to $\overline{RAS}$ Low		35
08	CLK Rising Edge to $\overline{CAS}$ Low (non-delayed access)		
a	t_{RAH} = 15ns, t_{ASC} = 0ns		85
b	t_{RAH} = 15ns, t_{ASC} = 10ns		95
c	t_{RAH} = 25ns, t_{ASC} = 0ns		95
d	t_{RAH} = 25ns, t_{ASC} = 10ns		105
09	ALE Low to CLK Rising Edge Setup	15	
010	$\overline{CS}$ Low while $\overline{AREQ}$ Low	0	
012	Address Hold Time from ALE falling edge using the On-Chip Address Latch	10	

No.	Parameter	Min	Max
C2	Address to Q output		35
C3	Row Address Hold Time, t_{RAH} = 15ns	15	
C4	Row Address Hold Time, t_{RAH} = 25ns	25	
C5	Column Address Set-up Time t_{ASC} = 0ns	0	
C6	Column Address Set-up Time t_{ASC} = 10ns	10	
C7	CLK Rising Edge to $\overline{RAS}$ active after delayed access		35
C8	CLK Rising Edge to $\overline{CAS}$ active after delayed access		
a	t_{RAH} = 15ns, t_{ASC} = 0ns		85
b	t_{RAH} = 15ns, t_{ASC} = 10ns		95
c	t_{RAH} = 25ns, t_{ASC} = 0ns		95
d	t_{RAH} = 25ns, t_{ASC} = 10ns		105
C12	$\overline{AREQ}$ High to $\overline{RAS}$ High	35	
C17	$\overline{AREQ}$ High to $\overline{CASn}$ High	25	
C20	Column Address Hold Time in Interleave	35	
C22	$\overline{AREQ}$ High to CLK Rising Edge to recognized as 1T of $\overline{RAS}$ precharge	15	1T
W03	$\overline{CS}$ Low to $\overline{WAIT}$ Low if No Wait State programmed		25
W5	CLK Rising Edge to $\overline{WAIT}$ High		25
	CLK High to $\overline{DTACK}$ Low 0T Programmed		35

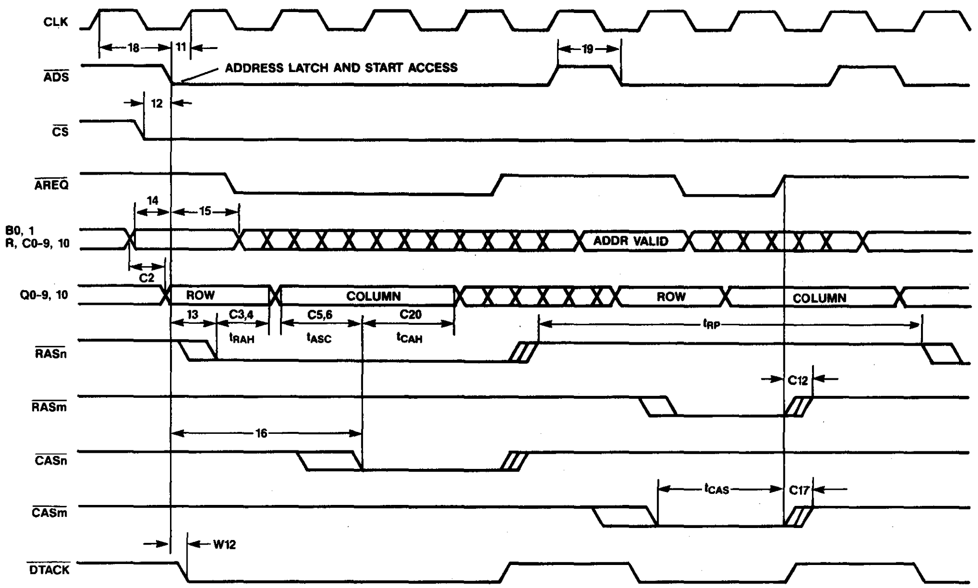
Figure 8. Mode 0, Wait State, Non-Interleave



No.	Parameter	Min	Max
C12	AREQ High to RAS High		35
C13	ECASn High to CASn High or ECASn Low to CASn Low		25
C21	AREQ Rising Edge to ECAS Rising Edge in order not to start a Wait State	20	
C25	CLK Rising Edge to CASn High if ECASn low at AREQ Rising Edge (if Delay Programmed by ECAS0)		30
C26	ECAS Low Set-up to CLK Rising Edge during burst access	20	

No.	Parameter	Min	Max
W01	WAITIN Low to CLK Rising Edge to Add Wait State (s) if no Wait State is programmed	5	
W02	ALE Rising Edge to WAIT Low (CS must be Low)		25
W1	CLK to WAIT High		30
W2	CLK to DTACK Low		30
W3	AREQ Rising Edge to DTACK High		25
W4	ECAS Rising Edge to WAIT Low		25
W5	CLK Rising Edge to WAIT High		25
	CLK High to DTACK Low 0T Programmed		35
W6	WAITIN Low to ECAS Rising Edge to Add Wait State(s)	5	
W7	ECAS High to DTACK High during burst access		35
W8	ECAS low to DTACK Low during Burst Access (0T programmed)		35

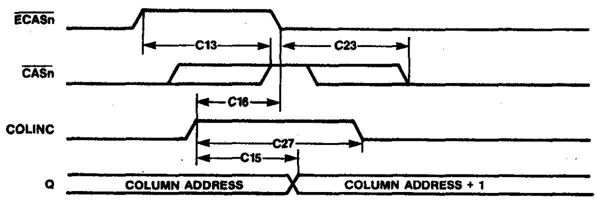
Figure 9. Mode 1, Interleave, Address Latch



No.	Parameter	Min	Max
C2	Address to Q output		35
C3	Row Address Hold Time, t_{RAH} = 15ns	15	
C4	Row Address Hold Time, t_{RAH} = 25ns	25	
C5	Column Address Set-up Time t_{ASC} = 0ns	0	
C6	Column Address Set-up Time t_{ASC} = 10ns	10	
C12	AREQ High to RAS High		35
C17	AREQ High to CAS High		25
C20	Column Address Hold Time in Interleave	35	
W12	ADS Low to DTACK Low OT from RAS Programmed R2, 3 = '0', R7 = '1'		40

No.	Parameter	Min	Max
11a	ADS Low to CLK Rising Edge	7	
11b	ADS Low to CLK, to guarantee WAIT DTACK output	25	
12	CS to ADS Low Set-up Time	5	
13	ADS Falling Edge to RAS Low during an Access		35
14a	Address Set-up to ADS Falling Edge using the On-Chip Address Latch	10	
14b	Address Set-up to ADS Falling Edge not using the On-Chip Address Latch	10	
15a	Address Hold after ADS Falling Edge using the On-Chip Address Latch	8	
15b	Address Hold after ADS Falling Edge not using the On-Chip Address Latch	t16	
16	ADS Low to CAS Low C9 = '0' (not delayed access)		
a	t_{RAH} = 15ns, t_{ASC} = 0ns		85
b	t_{RAH} = 15ns, t_{ASC} = 10ns		95
c	t_{RAH} = 25ns, t_{ASC} = 0ns		95
d	t_{RAH} = 25ns, t_{ASC} = 10ns		105
18	ADS held High from CLK Rising Edge	3	
19	ADS Pulse Width	10	

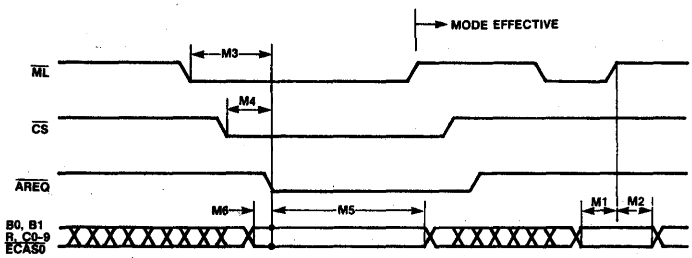
Figure 10. Burst Access — Page Mode



No.	Parameter	Min	Max
C13	$\overline{\text{ECASn}}$ High to $\overline{\text{CASn}}$ High		25
C15	COLINC Rising Edge to Column Address Output		35

No.	Parameter	Min	Max
C16	COLINC High Set-up to $\overline{\text{ECASn}}$ Low	15	
C23	$\overline{\text{ECASn}}$ Low to $\overline{\text{CAS}}$ Low		25
C27	COLINC Pulse Width	20	

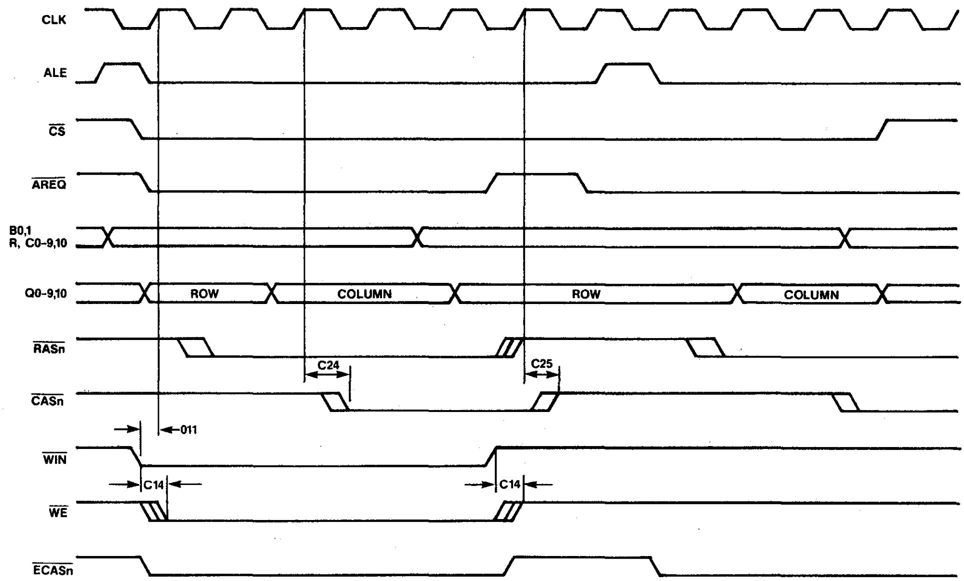
Figure 11. Mode Load



No.	Parameter	Min	Max
M1	Mode Address Set-up Time	5	
M2	Mode Address Hold Time	5	
M3	$\overline{\text{ML}}$ asserted to $\overline{\text{AREQ}}$ asserted	10	

No.	Parameter	Min	Max
M4	$\overline{\text{CS}}$ asserted to $\overline{\text{AREQ}}$ asserted	5	
M5	Mode Address Hold Time from $\overline{\text{AREQ}}$ Low	30	
M6	Mode Address Set-up Time to $\overline{\text{AREQ}}$ Low	0	

Figure 12. Non-Interleave — Delay $\overline{CAS}$



No.	Parameter	Min	Max
011	$\overline{WIN}$ low to CLK Rising Edge to delay $\overline{CAS}$ (C9 = '1')	5	
C14	$\overline{WIN}$ to $\overline{WE}$		40
C24	CLK Rising Edge to $\overline{CAS}$ Low if delayed by $\overline{WIN}$		30
C25	CLK Rising Edge to $\overline{CASn}$ High if $\overline{ECASn}$ Low at $\overline{AREQ}$ (if delay programmed by $\overline{ECAS0}$)		30

No.	Parameter	Min	Max
C18	CLK High	15	
C18a	CLK Low	15	
C19	CLK Period	40	
C28	RFCLK High	15	
C28a	RFCLK Low	15	
C29	RFCLK Period	40	

Figure 13. CLK, RFCLK Timing

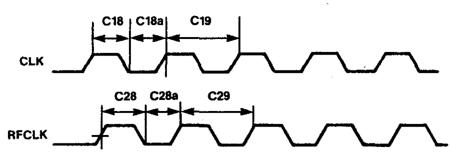
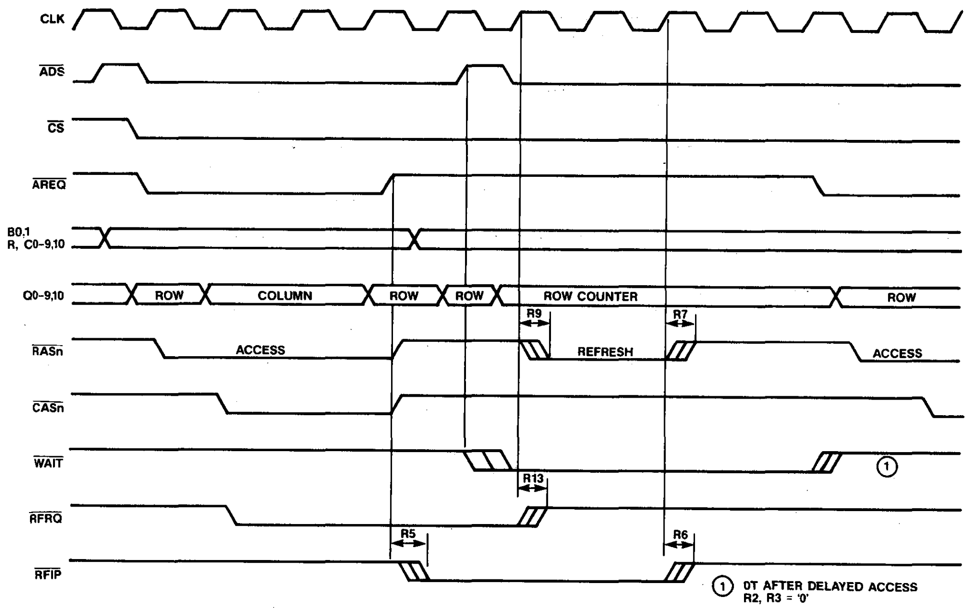
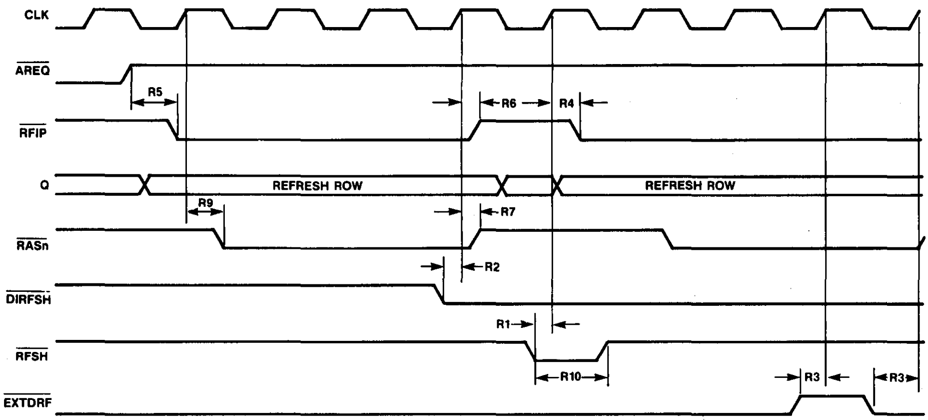


Figure 14. Internal Refresh — Interleave Access



No.	Parameter	Min	Max
R5	AREQ High to RFIP Low for Pending Refresh Burst Access		35
R6	CLK Rising Edge to RFIP High for Pending Refresh Ending		35
R7	CLK Rising Edge to Refresh RAS Ending		30
R9	CLK Rising Edge to Refresh RAS Starting		35
R13	CLK Rising Edge to RFRQ High		35

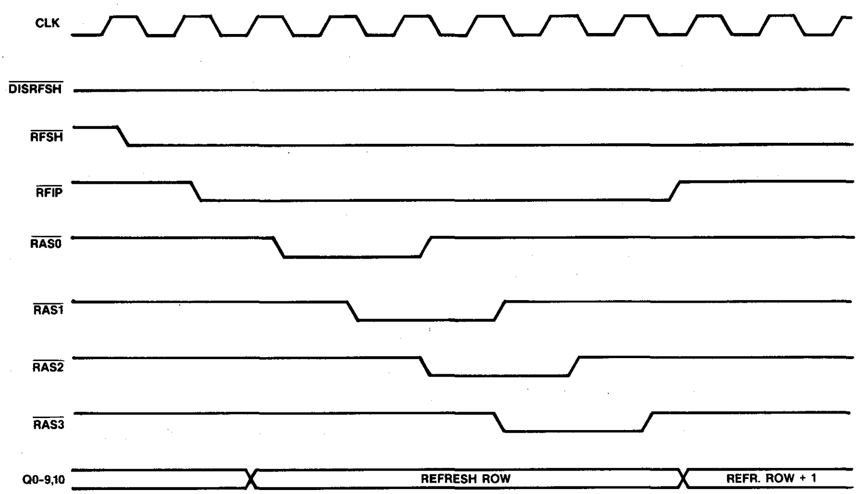
Figure 15. Refresh and Extended Refresh



No.	Parameter	Min	Max
R1	$\overline{\text{RFSH}}$ Low Set-up to CLK Rising Edge	5	
R2	DISRFSH Low Set-up to CLK Rising Edge	15	
R3	EXTDRF Set-up to CLK Rising Edge	12	
R4	CLK Rising Edge to $\overline{\text{RFIP}}$ Low		30
R5	$\overline{\text{AREQ}}$ High to $\overline{\text{RFIP}}$ Low for Pending Refresh Burst Access		35

No.	Parameter	Min	Max
R6	CLK Rising Edge to $\overline{\text{RFIP}}$ High for Pending Refresh Ending		35
R7	CLK Rising Edge to Refresh $\overline{\text{RAS}}$ Ending		30
R9	CLK Rising Edge to Refresh $\overline{\text{RAS}}$ Starting		35
R10	$\overline{\text{RFSH}}$ Low Pulse Width	15	

Figure 16. Staggered Refresh



NOTES ON TIMING CHARACTERISTICS

This section provides notes on timing characteristics for the following operations:

- Interleaving (Figures 7, 9 and 14)
- Two consecutive accesses to the same bank
- Refresh (Figures 14, 15 and 16)
- Wait States (Figure 8)

Interleaving

Relevant Mode Bits

R8	Interleave/non-interleave mode
C4, 5, 6	Select Interleave 2, 4, 5, or 7
B0	Address latch mode
B1	Access Modes
C7	Column Address Setup Time
C8	Row Address Hold Time
R0, 1	RAS Precharge Time

External Signal Inputs

CS — This input enables the access cycle.
Mode 0: It must be low for t01 before the rising edge of CLK. CS must stay low until AREQ goes low.
Mode 1: It must be low t12 before the falling edge of ADS.

ADS — Mode 1: This input latches the address during asynchronous accesses. The falling edge must occur t11 before the rising edge of CLK. It may go high after AREQ was low for one CLK period. The address of the R, C and B inputs is latched at the falling edge of ADS, if bit B0 in the Mode Register is '0'. While ADS is high, the address latches are transparent to the input.

ALE — Mode 0: This input latches the address during synchronous accesses. The rising edge must occur t02 before the rising edge of the next CLK input which starts an access. This is also true if the on-chip address latch is programmed in fall-through mode (bit B0 in the Mode Register is '1').

AREQ — This input ends the active time of RAS and CAS. It may go low with ADS or some time later. AREQ has to be high tC22 before the rising edge of CLK in order to be recognized as 1T of precharge time.

RASn and CASn go high at the rising edge of AREQ, independently of ADS. Example: If RAS3 followed by RAS1 has been invoked, RAS3 goes high with the first rising edge of AREQ and RAS1 with the second.

RAS Precharge time: If two consecutive access cycles address the same bank, i.e. the two least significant bits do not change, the precharge time t_{RP} is met by invoking Wait States.

ECASn — ECASn must be toggled to invoke a burst access while RASn is low.

CAS precharge time: The CAS precharge time during burst access must be controlled by the ECAS inputs. KS84C21/22 do not monitor the duration of CAS.

R, C B0, B1 — Mode 0: Address inputs must be stable t05 before CLK goes high if the address latches are fall through, and t06 if the address bits are latched. The address hold time is t03 or t12.

Mode 1: Address inputs must be stable for a setup time of t14a and t14b before ADS goes low. The address hold time is t15a and t15b for latched and unlatched address bits.

Note: To meet the address hold time requirements, the KS84C21/22 guarantee that the column address is turned on for 35ns. If an access is initiated before the column address is turned on, the column address may change, since the address latches are transparent while ADS or ALE is high.

External Signal Inputs *(Continued)*

B0, B1 — These two inputs should be connected to the two least significant address bits. B0 and B1 select one of the memory banks, depending upon the setting of bits C4, C5 and C6 in the Mode Register. Set-up and hold times are as described for the address inputs.

Signal outputs

Q-Row — The Q outputs are the multiplexed address outputs. The row address is on the Q-outputs after the propagation delay time tC2. The row address appears after a Column Address Hold time of 35ns minimum (interleave mode only).

$\overline{\text{RASn}}$ — The row address is guaranteed to be stable when $\overline{\text{RAS}}$ goes low. $\overline{\text{RASn}}$ stays low as long as $\overline{\text{AREQ}}$ is low and then stays high for the programmed number of CLK cycles. If required, Wait States are requested by the output $\overline{\text{WAIT}}$ or $\overline{\text{DTACK}}$.

$\overline{\text{CASn}}$ — This output goes low after t16, guaranteeing the programmed Column Address Set-up time of 0ns or 10ns and the Row Address Hold time of 15ns or 25ns.

Q-Coln — After the Row Address Hold time has elapsed, the column address is multiplexed to the Q outputs. After the Column Address Hold time of min. 35ns, the row address will again be on the output.

$\overline{\text{WE}}/\overline{\text{RFRQ}}$ — This output signal is asserted when an internal or external refresh is requested. In interleave mode, the $\overline{\text{WE}}$ input to the DRAMs must be controlled by external logic.

Two Consecutive Accesses to the Same Bank

External Signal Inputs

$\overline{\text{AREQ}}$ — $\overline{\text{AREQ}}$ must go high to end the access in progress, before a pending access can be executed.

$\overline{\text{ADS}}$/ALE — An access may be started while $\overline{\text{AREQ}}$ is high or low. This means that $\overline{\text{ADS}}$ or ALE may go low while $\overline{\text{CAS}}$ is active.

Signal Outputs

$\overline{\text{WAIT}}$ *or* $\overline{\text{DTACK}}$ — This output is asserted when the same bank is accessed in two consecutive cycles, and/or the $\overline{\text{RASn}}$ precharge time for the current access is less than the programmed precharge time. The $\overline{\text{WAIT}}$ output if programmed, is asserted immediately when the KS84C21/C22 detects that the bank did not change and the DRAM was not precharged.

$\overline{\text{RASn}}$ — These outputs go high with the rising edge of $\overline{\text{AREQ}}$, and remain high for the number of CLK cycles programmed by R0 and R1 in the Mode Register. After the precharge time has elapsed, a pending access is executed on the rising edge of the CLK that ended the precharge time. These conditions are true for both Mode 0 and Mode 1.

Refresh

Relevant Mode Bits

R0, R1	$\overline{\text{RAS}}$ low time during refresh and RAS precharge time.
R9	Staggered refresh
C0-3	Refresh clock divider
C4-6	Select 0, 2, 4 is error scrubbing during refresh

External Signal Inputs

$\overline{\text{ECAS0}}$ — If $\overline{\text{ECAS0}}$ is set low in the Mode Register, the output $\overline{\text{WE}}/\overline{\text{RFRQ}}$ becomes $\overline{\text{WE}}$. If $\overline{\text{ECAS0}}$ is high at this time, $\overline{\text{WE}}/\overline{\text{RFRQ}}$ will function as refresh request. However, in interleave mode, this output is always $\overline{\text{RFRQ}}$.

***External Signal Inputs** (Continued)*

$\overline{\text{DISRFSH}}$	When high, this signal enables internal refresh, and when low, externally controlled refresh. External refresh can also be invoked by the $\overline{\text{RFSH}}$ input.
$\overline{\text{RFSH}}$	Must stay high for internally controlled refresh cycles. If $\overline{\text{DISRFSH}}$ is low, the $\overline{\text{RFSH}}$ input controls the number of refresh cycles performed, depending on how long it stays low. One refresh cycle is performed if $\overline{\text{RFSH}}$ is low for a minimum of one CLK period, and then goes high tR1 before the rising edge of the CLK input that ends the refresh operation. The Refresh Counter can be cleared with $\overline{\text{DISRFSH}}$ high and $\overline{\text{RFSH}}$ low with the set-up time t21 to CLK rising edge.
COLINC/ EXTDRF	If error scrubbing has been chosen and this input goes high while $\overline{\text{RAS}}$ is low, the refresh cycle in progress is extended to allow a read-modify-write cycle for error correction. $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ remain low until the rising edge of the next CLK input after EXTDRF has gone low again.

Signal Outputs

$\overline{\text{RFIP}}$	This signal goes low one CLK period before $\overline{\text{RAS}}$ goes low, and goes high on the rising edge of the CLK that ends the $\overline{\text{RAS}}$ active cycle.
$\overline{\text{WAIT/DTACK}}$	If an access is requested during the refresh period, this access is deferred by inserting Wait States until refresh is complete.
$\overline{\text{WE}}$ or $\overline{\text{RFRQ}}$	This output becomes $\overline{\text{RFRQ}}$ in interleave mode. If $\overline{\text{RFRQ}}$ programmed to do so by $\overline{\text{ECAS0}}$, it becomes $\overline{\text{RFRQ}}$ in non-interleave mode. $\overline{\text{RFRQ}}$ goes low when an internal refresh request occurs, and goes high when the refresh $\overline{\text{RAS}}$ is sserted. $\overline{\text{RFRQ}}$ is activated regardless of internally or externally controlled refresh.
$\overline{\text{RASn}}$	This signal goes low after the precharge time of the access in progress, to start the refresh operation. It is toggled high and low for the number of CLK cycles programmed by R0 and R1 in the Mode Register. All $\overline{\text{RAS}}$ inputs go low at the same time, or are staggered at one CLK intervals Figure 16) if a staggered refresh is programmed by Mode bit R9. The refresh counter (controlled either internally or externally) is incremented at every refresh, on the rising edge of $\overline{\text{RAS3}}$.

Wait States

Relevant Mode Bits

R2, R3	Wait during non-burst access
R4, R5	Add Wait State(s) to the current access if $\overline{\text{WAITIN}}$ is low.
R7	Select $\overline{\text{WAIT}}$ or $\overline{\text{DTACK}}$.

External Signal Inputs

ALE	Mode 0: $\overline{\text{WAIT}}$ goes low after the rising edge of ALE, if $\overline{\text{CS}}$ is low. If $\overline{\text{CS}}$ is high when ALE goes high, then the $\overline{\text{WAIT}}$ output will not be asserted until $\overline{\text{CS}}$ enables the access.
$\overline{\text{ADS}}$	Mode 1: Wait State starts if an access is initiated by $\overline{\text{ADS}}$ going low, provided that $\overline{\text{CS}}$ is low at set up time t12.
$\overline{\text{AREQ}}$	If this input goes high, $\overline{\text{DTACK}}$ goes high after a maximum interval of tW3.
$\overline{\text{ECASn}}$	During a non-burst access, $\overline{\text{ECAS}}$ inputs are normally low, unless $\overline{\text{CASn}}$ is delayed from going low. During burst access, the rising edge of $\overline{\text{ECASn}}$ starts a Wait State while $\overline{\text{AREQ}}$ is low. The Wait State is terminated as programmed by R4 and R5 in the Mode Register. $\overline{\text{ECASn}}$ must stay low tC21 after $\overline{\text{AREQ}}$ goes high. This ensures that no further Wait State is inserted.

External Signal Inputs *(Continued)*

$\overline{\text{WAITIN}}$ Keeping this signal low allows Wait States to be inserted at particular external events, such as read instructions, or into a portion of memory that requires additional Wait States. $\overline{\text{WAITIN}}$ can be deasserted one CLK period before $\overline{\text{WAIT}}$ ends and $\overline{\text{DTACK}}$ starts. The active time of $\overline{\text{WAIT}}$ or $\overline{\text{DTACK}}$ is prolonged by one or two CLK cycles. $\overline{\text{WAITIN}}$ must be low for a setup time of tW01 in Mode 0, and tW11 in Mode 1, and must stay low for a minimum of one CLK period before the Wait State ends.

Signal Outputs

$\overline{\text{WAIT}}/\overline{\text{DTACK}}$ This output is either $\overline{\text{WAIT}}$ or $\overline{\text{DTACK}}$, depending on the setting of R7 in the Mode Register. $\overline{\text{WAIT}}$ goes low and $\overline{\text{DTACK}}$ stays high for the programmed number of Wait States. Wait States are inserted if necessary to meet the $\overline{\text{RAS}}$ precharge time, or to delay access.

There is a precharge counter for every bank. If the $\overline{\text{RAS}}$ precharge time has not elapsed at the expected number of CLK cycles, $\overline{\text{WAIT}}$ output goes low, or $\overline{\text{DTACK}}$ stays high, to instruct the CPU to insert Wait States until the precharge time has elapsed.

Wait During Non-Burst Access

The first access of any memory cycle is always a non-burst access.

$\overline{\text{WAIT}}$ Mode 0: $\overline{\text{WAIT}}$ goes low after tW02 and stays low for the programmed number of clock periods after $\overline{\text{RAS}}$ goes low. $\overline{\text{CS}}$ must meet the set-up time before the rising edge of CLK. $\overline{\text{WAIT}}$ is delayed from going low until $\overline{\text{CS}}$ goes low. It stays high if zero Waits states are programmed. If $\overline{\text{WAITIN}}$ goes low at tW01 before the rising edge of CLK, one or two extra Wait States are inserted, depending upon the setting of R6 in the Mode Register.

Mode 1: $\overline{\text{WAIT}}$ goes low after the '$\overline{\text{CS}}$ set up time to $\overline{\text{ADS}}$ low' of tW13, and stays low for the programmed number of Wait States after $\overline{\text{RAS}}$ goes low. It stays high if zero Wait States are programmed. If $\overline{\text{WAITIN}}$ goes low tW11 before the falling edge of $\overline{\text{ADS}}$, one or two extra Wait States are inserted. $\overline{\text{WAIT}}$ does not go low when $\overline{\text{ADS}}$ goes low, if an access does not start (that is if $\overline{\text{CS}}$ is high.)

$\overline{\text{DTACK}}$ Mode 0: $\overline{\text{DTACK}}$ stays high for the programmed number of clock cycles of $\overline{\text{RAS}}$ goes low. It switches to high a maximum interval of tW3 after $\overline{\text{AREQ}}$ goes high. If $\overline{\text{WAITIN}}$ goes low tW01 before the rising edge of the CLK which starts the access, $\overline{\text{DTACK}}$ stays high for one or two extra CLK cycles, depending upon the setting of bit R6 in the Mode Register.

Mode 1: $\overline{\text{DTACK}}$ stays high for the programmed number of CLK cycles after $\overline{\text{RAS}}$ goes low. It goes high tW3 after $\overline{\text{AREQ}}$ goes high. If $\overline{\text{WAITIN}}$ goes low tW11 before the rising edge of CLK, $\overline{\text{DTACK}}$ will stay high for one or two additional CLK cycles, depending upon the setting of bit R6 in the Mode Register.

PACKAGE DIMENSIONS

The Samsung KS84CXX DRAM Controllers are available in two packages. The KS84C21 68-Pin PLCC package is shown in Figure 17, while the 84-Pin version is shown in Figure 18.

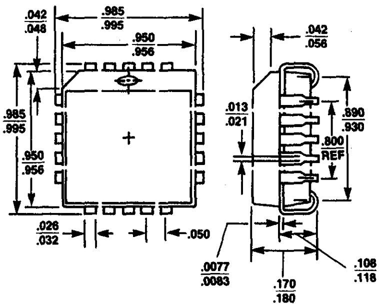


Figure 17. 68-Pin PLCC Package

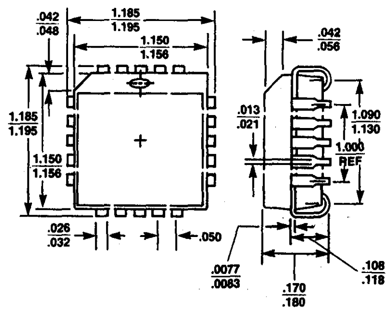


Figure 18. 84-Pin PLCC Package

ORDERING INFORMATION AND PRODUCT CODE

KS 84CXX XX X X

- **KS** — **SAMSUNG SEMICONDUCTOR**
- **84CXX** — **Part Number**: 84C21, 84C22
- **XX** — **Speed**: -25 25MHz
- **X** — **Temperature**: C — Commercial (0°C to +70°C)
- **X** — **Packaging**: L — Plastic Leaded Chip Carrier (PLCC)

SAMSUNG products are designated by a Product Code. When ordering, please refer to products by their full code. For unusual, and/or specific packaging or processing requirements not covered by the standard product line, please contact the SAMSUNG MOS Products Group.

KS84C31/32

ENHANCED DYNAMIC RAM CONTROLLERS
Preliminary

FEATURES

- 33MHz operation
- Direct drive for 256K, 1Mbit and 4Mbit DRAMs
- No wait state operation with 66 MHz 80386 or similar CPU's
- 68030/68040 interface, fast cache fill mode
- Page, nibble and static column accesses
- Page switch detection
- Interleaved or non-interleaved accesses
- Fast Nibble access
- Programmable or mask-programmed versions
- Programmable refresh operations
- Staggered and burst refresh
- Refresh operations virtually transparent to the CPU
- Programmable wait states
- Byte operation with four independent CAS outputs
- Easy interface to all major microprocessors
- Built in delay line
- Synchronous and asynchronous operation
- On-chip capacitive load drivers
- CMOS technology for low power consumption
- TTL-compatible inputs
- 68-pin PLCC package (KS84C31)
- 84-pin PLCC package (KS84C32)

PRODUCT OVERVIEW

The Samsung KS84C31 and KS84C32 are high performance dynamic RAM (DRAM) controllers. They simplify the interface between the microprocessor and the DRAM array, while also significantly reducing the required design time. The KS84C31 supports the 256K DRAM and the 1MBit DRAM, while the KS84C32 supports the 256K DRAM, 1MBit DRAM and 4MBit DRAM.

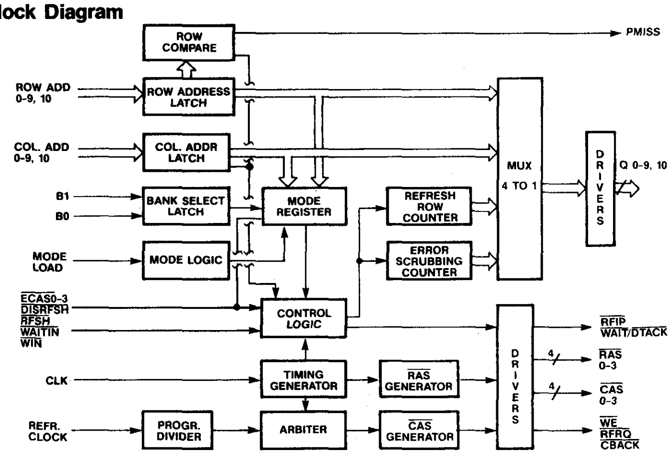
Both devices are functionally enhanced versions of their 84C21/22 counterparts. They are available in either externally programmable or masked programmable versions. The externally programmable version is an economic and flexible design solution for small-scale applications and prototyping. A 26-bit programmable Mode Register allows the selection of various options and features, including synchronous or asynchronous operation; interleaved or non-interleaved operation; burst or non-burst access; insertion of Wait States into the CPU cycle; a variety of refresh options; as well as the ability to fine tune the control signals. Two CPU's namely the 68030 and 68040 are directly supported.

A mask-programmed version of the chip offers the same Mode Register options. However, the chip is programmed at the factory to customer specifications. This version offers maximum system reliability and eliminates the need for external logic.

Both chips have a drive capability of 380 pF, sufficient to drive large memory arrays. Several hundred DRAMs may be driven if damping resistors are used to control ground bounce.

Figure 1 shows a block diagram of the chips.

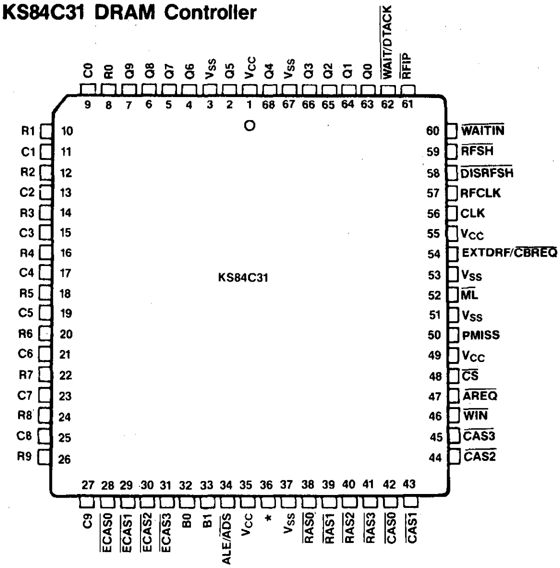
Figure 1. KS84C31/32 Block Diagram



INTERFACE SPECIFICATIONS

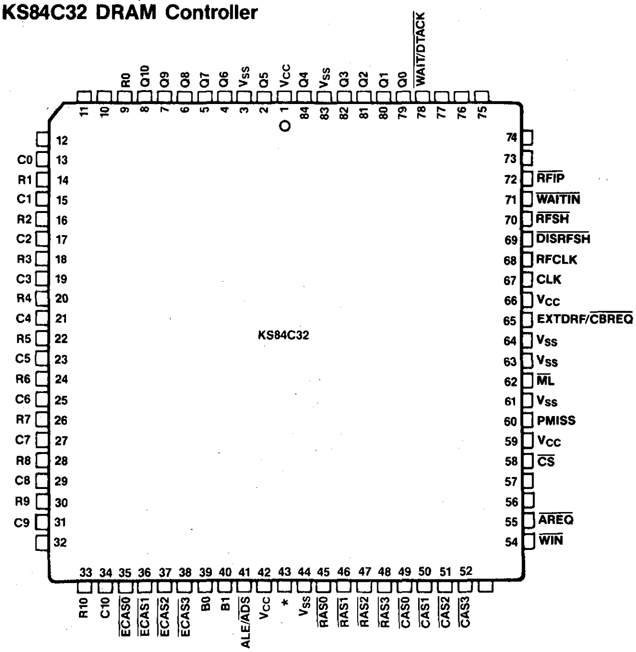
The Dynamic Ram Controller is available in two packages. The KS84C31, shown in Figure 2 is a 68-pin device and supports the 256K DRAM and 1Mbit DRAM. The KS84C32, shown in Figure 3 is an 84-pin device designed for use with the 256K DRAM 1 and 4Mbit DRAM.

Figure 2a. Pin Configuration of the KS84C31 DRAM Controller



*36	WE	Non-interleave
*43	RFRQ	Interleave
	CBACK	68030 mode

Figure 2b. Pin Configuration of the KS84C32 DRAM Controller



3

Figure 3. Logic Symbol

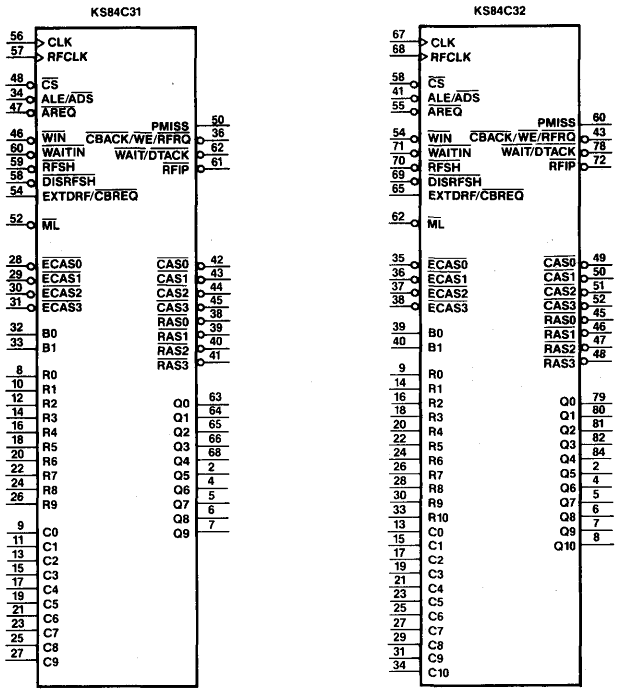


Table 1 shows detailed pin allocations for the KS84C31, while Table 2 shows the KS84C32. Table 3 provides the input/output signal definitions.

Note on Conventions:
A bar over the signal name is used to denote an active low signal ($\overline{ADS}$). Active high signals are shown with no bar (ALE).

Table 1. KS84C31 Pin Allocations

Pin No.	Signal Abbrev.	Signal Name
1	V_{CC}	V_{CC}
2	Q5	Multiplexed Address 5
3	V_{SS}	V_{SS}
4	Q6	Multiplexed Address 6
5	Q7	Multiplexed Address 7
6	Q8	Multiplexed Address 8
7	Q9	Multiplexed Address 9
8	R0	Row Address 0
9	C0	Column Address 0
10	R1	Row Address 1
11	C1	Column Address 1
12	R2	Row Address 2
13	C2	Column Address 2
14	R3	Row Address 3
15	C3	Column Address 3
16	R4	Row Address 4
17	C4	Column Address 4
18	R5	Row Address 5
19	C5	Column Address 5
20	R6	Row Address 6
21	C6	Column Address 6
22	R7	Row Address 7
23	C7	Column Address 7
24	R8	Row Address 8
25	C8	Column Address 8
26	R9	Row Address 9
27	C9	Column Address 9
28	$\overline{ECAS0}$	Enable $\overline{CAS0}$
29	$\overline{ECAS1}$	Enable $\overline{CAS1}$
30	$\overline{ECAS2}$	Enable $\overline{CAS2}$
31	$\overline{ECAS3}$	Enable $\overline{CAS3}$
32	B0	Bank Select 0
33	B1	Bank Select 1
34	ALE/$\overline{ADS}$	Address Latch Enable/ Address Strobe
35	V_{CC}	V_{CC}
36	$\overline{RFRQ/WE}$	Refresh Request/Write Enable
	$\overline{CBACK}$	Cache Burst Acknowledge
37	V_{SS}	V_{SS}
38	$\overline{RAS0}$	Row Address Strobe 0
39	$\overline{RAS1}$	Row Address Strobe 1
40	$\overline{RAS2}$	Row Address Strobe 2
41	$\overline{RAS3}$	Row Address Strobe 3
42	$\overline{CAS0}$	Column Address Strobe 0
43	$\overline{CAS1}$	Column Address Strobe 1
44	$\overline{CAS2}$	Column Address Strobe 2
45	$\overline{CAS3}$	Column Address Strobe 3
46	$\overline{WIN}$	Write Enable Input
47	$\overline{AREQ}$	Access Request
48	$\overline{CS}$	Chip Select
49	V_{CC}	V_{CC}
50	PMISS	Page Miss
51	V_{SS}	V_{SS}
52	$\overline{ML}$	Mode Load
53	V_{SS}	V_{SS}
54	$\overline{EXTDRF}$	Extend Refresh
	$\overline{CBREQ}$	Cache Brust Request
55	V_{CC}	V_{CC}
56	CLK	Clock
57	RFCLK	Refresh Clock
58	$\overline{DISRFSH}$	Disable Internal Refresh
59	$\overline{RFSH}$	External Refresh Request
60	$\overline{WAITIN}$	Add Wait State
61	$\overline{RFIP}$	Refresh in Progress
62	$\overline{WAIT/DTACK}$	Wait/Data Transfer Acknowledge
63	Q0	Multiplexed Address 0
64	Q1	Multiplexed Address 1
65	Q2	Multiplexed Address 2
66	Q3	Multiplexed Address 3
67	V_{SS}	V_{SS}
68	Q4	Multiplexed Address 4

Table 2. KS84C32 Pin Allocations

Pin No.	Signal Abbrev.	Signal Name
1	V_{CC}	V_{CC}
2	Q5	Multiplexed Address 5
3	V_{SS}	V_{SS}
4	Q6	Multiplexed Address 6
5	Q7	Multiplexed Address 7
6	Q8	Multiplexed Address 8
7	Q9	Multiplexed Address 9
8	Q10	Multiplexed Address 10
9	R0	Row Address 0
10	—	N.C.
11	—	N.C.
12	—	N.C.
13	C0	Column Address 0
14	R1	Row Address 1
15	C1	Column Address 1
16	R2	Row Address 2
17	C2	Column Address 2
18	R3	Row Address 3
19	C3	Column Address 3
20	R4	Row Address 4
21	C4	Column Address 4
22	R5	Row Address 5
23	C5	Column Address 5
24	R6	Row Address 6
25	C6	Column Address 6
26	R7	Row Address 7
27	C7	Column Address 7
28	R8	Row Address 8
29	C8	Column Address 8
30	R9	Row Address 9
31	C9	Column Address 9
32	—	N.C.
33	R10	Row Address 10
34	C10	Column Address 10
35	$\overline{ECAS0}$	Enable $\overline{CAS0}$
36	$\overline{ECAS1}$	Enable $\overline{CAS1}$
37	$\overline{ECAS2}$	Enable $\overline{CAS2}$
38	$\overline{ECAS3}$	Enable $\overline{CAS3}$
39	B0	Bank Select 0
40	B1	Bank Select 1
41	ALE/$\overline{ADS}$	Address Latch Enable/ Address Strobe
42	V_{CC}	V_{CC}
43	$\overline{RFRQ/WE}$	Refresh Request/Write Enable
	$\overline{CBACK}$	Cache Burst Acknowledge
44	V_{SS}	V_{SS}
45	$\overline{RAS0}$	Row Address Strobe 0
46	$\overline{RAS1}$	Row Address Strobe 1
47	$\overline{RAS2}$	Row Address Strobe 2
48	$\overline{RAS3}$	Row Address Strobe 3
49	$\overline{CAS0}$	Column Address Strobe 0
50	$\overline{CAS1}$	Column Address Strobe 1
51	$\overline{CAS2}$	Column Address Strobe 2
52	$\overline{CAS3}$	Column Address Strobe 3
53	—	N.C.
54	$\overline{WIN}$	Write Enable Input
55	$\overline{AREQ}$	Access Request
56	—	N.C.
57	—	N.C.
58	$\overline{CS}$	Chip Select
59	V_{CC}	V_{CC}
60	PMISS	Page Miss
61	V_{SS}	V_{SS}
62	$\overline{ML}$	Mode Load
63	V_{SS}	V_{SS}
64	V_{SS}	V_{SS}
65	EXTDRF	Extend Refresh
	$\overline{CBREQ}$	Cache Burst Request
66	V_{CC}	V_{CC}
67	CLK	Clock
68	RFCLK	Refresh Clock
69	$\overline{DISRFSH}$	Disable Internal Refresh
70	$\overline{RFSH}$	External Refresh Request
71	$\overline{WAITIN}$	Add Wait State
72	$\overline{RFIP}$	Refresh in Progress
73	—	N.C.
74	—	N.C.
75	—	N.C.
76	—	N.C.
77	—	N.C.
78	$\overline{WAIT/DTACK}$	Wait/Data Transfer Acknowledge
79	Q0	Multiplexed Address 0
80	Q1	Multiplexed Address 1
81	Q2	Multiplexed Address 2
82	Q3	Multiplexed Address 3
83	V_{SS}	V_{SS}
84	Q4	Multiplexed Address 4

3

Table 3. Interface Signal Definitions

Note: I indicates an input signal. O indicates an output signal. Timing notations (t_{12}) etc. are referenced to the timing diagrams at the end of the product description.

Symbol	Type	Description
$\overline{ADS}$/ALE	I	**Address Strobe/Address Latch Enable:** This input latches row, column and bank addresses, and initiates DRAM access. $\overline{CS}$ must be low to initiate an access. $\overline{ADS}$/ALE must be invoked for every access burst or non-burst but only for the first access in 68030 or nibble mode. In Mode 0: This input functions as address latch enable ALE. In Mode 1: This input is active low, and functions as address strobe signal. The falling edge of $\overline{ADS}$ also starts an access, if $\overline{CS}$ is low for the set-up time t_{12}. (Mode is selected by Bit B1 in the Mode Register. See PROGRAMMING THE KS84C31/32.)
$\overline{AREQ}$	I	**Access Request:** This input terminates an access. In non-interleave mode: it brings $\overline{RAS}$ high. In interleave mode: it brings $\overline{CAS}$ and $\overline{RAS}$ high.
B0, B1	I	**Bank Select:** These inputs are bank addresses, and allow one of up to four memory banks to be selected. Selection depends upon how C4, C5 and C6 in the Mode Register are set.
C0-9, 10	I	**Column Address Inputs:** These column address bits are usually connected to the high order address bits of the microprocessor. They select columns in the DRAM cell configuration. C0–C9 are also used to program the Mode Register.
$\overline{CAS0\text{-}3}$	O	**Column Address Strobe:** These inputs strobe the column address. They go low after the programmed Column Address Set-up time of 0 or 10ns. In 68030 and Nibble Mode $\overline{CAS}$s are switched for the burst access at the rising/falling edge of CLK.
CLK	I	**Clock:** This is the system clock. It is used for bus arbitration and timing purposes. Synchronous access requests must be synchronized with the system clock. The duty cycle is significant if 1/2 Wait State is programmed and in Nibble Mode.
$\overline{CS}$	I	**Chip Select:** The $\overline{CS}$ input must be low to enable a DRAM access and to strobe Row column and Bank address. There is a pre-access setup time. In Mode 0 this is the rising edge of CLK, and in Mode 1 the falling edge of $\overline{ADS}$. $\overline{CS}$ must enable every access in non-interleaving, interleaving or page access. It has to enable only the first non-burst access in 68030 and Nibble Mode.
EXTDRF	I	**Extend Refresh:** During refresh, EXTDRF extends a refresh cycle, to allow a read-modify-write cycle to be performed in a system with error correction. See ERROR SCRUBBING.
$\overline{CBREQ}$	I	**Cache Burst Request:** This input is compatible to the $\overline{CBREQ}$ output of the 68030 if $\overline{ECAS1}$ in the Mode Register is set to '1' (68030 Mode).
$\overline{DISRFSH}$	I	**Disable Internal Refresh:** When low, this input disables Internal Refresh.
$\overline{ECAS0\text{-}3}$	I	**Enable $\overline{CAS0\text{-}3}$:** These inputs are used to enable or disable individual $\overline{CAS}$ outputs, or delay $\overline{CAS}$ from going low. They are useful when accessing bytes, nibbles or pages. $\overline{ECAS0\text{-}3}$ also programs output $\overline{WE}$ ($\overline{RFRQ}$), sets the trailing edge of $\overline{CAS}$, and selects 68030 and Nibble Mode. See PROGRAMMING THE KS84C31/32.

Table 3. Interface Signal Definitions (Continued)

Symbol	Type	Description
ML	I	**Mode Load:** This input latches the row, column, ECAS0-3, and bank address inputs into the Mode Register.
Q0-9, 10	O	**Address Outputs:** These outputs are the multiplexed address bits (R0-10, C0-10). They access the memory for read, write and refresh operations. The output load may be as high as 380pF.
R0-9, 10	I	**Row Address Inputs:** These address inputs are usually connected to the low order address bits of the microprocessor. They select rows in the DRAM cell configuration.
RAS0-3	O	**Row Address Strobe:** These row address strobe signals are used to strobe the row addresses into the DRAM.
RFCLK	I	**Refresh Clock:** This input determines the timing of the refresh cycles for the DRAMs. It should be a multiple of 2MHz. It is divided according to bits C0, 1, 2, and C3 in the Mode Register, so that the refresh cycles occur at 15μs or 13μs intervals.
RFIP	O	**Refresh in Progress:** This output indicates that a refresh cycle is in progress. RFIP goes low one CLK cycle prior to the start of a refresh cycle.
RFSH	I	**External Refresh Request:** Refresh cycles can be requested externally by driving the RFSH signal low.
WAITIN	I	**Add Wait State:** If this input is low, one or two extra Wait States will be added to the access cycle at an external event, e.g. memory read.
WAIT/DTACK	O	**Wait/Data Transfer Acknowledge:** This output inserts Wait States into CPU access cycles. The output is controlled by bits R2, R3, R4, R5 and R7, in the Mode Register.
WE/RFRQ	O	**Write Enable/Refresh Request:** After Power up reset and in interleave mode, this output functions as refresh request. In non-interleave mode it can be programmed to function as the WE output if ECAS0 is low in the Mode Register.
CBACK	O	**Cache Burst Acknowledge:** This output is compatible with the CBACK input of the 68030 if ECAS1 in the Mode Register is set to '1'.
PMISS	O	**Page Miss:** If Page Mode is programmed this output goes high if a page change has been detected or when a refresh request has occurred for the 5th time. It stays high until the page address has been latched into the DRAMs. This signal is asserted during the precharge period and can be used to add wait states for non-burst access.
WIN	I	**Write Enable Input:** This input controls the WE output, and delays CAS, if programmed to do so by bit C9 in the Mode Register.

KS84C31/32 OPERATION

Introduction

The KS84C31/32 are Enhanced Dynamic Ram Controllers (also called EDRC in the following) that are built on the proven KS84C21/22 architecture with some upgrades that improves the access to dynamic RAMs by cutting the access time and make it suitable for cache applications. The additional features supported are a page access to random pages (static column or standard page access) and fast nibble access. The 68030 is supported by a 68030 mode. Other CPUs or cache controllers can utilize the fast nibble access mode by a specially build in Nibble Mode.

Reset

Power Up Reset

The KS84C231/32 on-chip power-up reset logic generates a reset pulse:

- At power up;
- If V_{CC} falls well below +3.0V, and reaches V_{CC} min. (Short spikes below the minimum V_{CC} will not reset the chip. However, correct functionality is guaranteed only within the operating conditions.)

When the chip is reset, all internal flip-flops, counters, and the Mode register are reset, and the output lines are inactive: RAS0-3, CAS0-3, WAIT (DTACK), RFIP, WE (RFRQ/CBACK) and PMISS are high, while Q0-9, 10 are low. Note that there are no tri-state buffers on any of the outputs.

The chip does not need any time to synchronize after power up, it is operable after 200 microseconds, as required by most DRAMs.

After power-up reset, the Mode Register must be reprogrammed in the programmable version of the chip.

External Reset

The Mode Load signal (ML) can also be used to reset the chip. When ML is driven low, all counters and flip-flops are reset, and the Mode Register is enabled to receive the mode bit inputs.

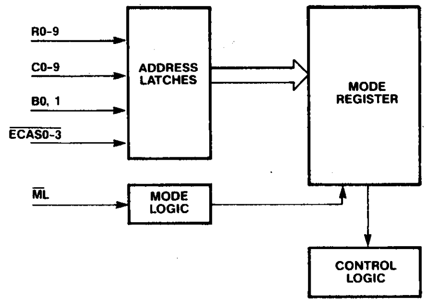
Programming the KS84C31/32

The KS84C31/32 has a Mode Register that can be programmed by the user, or mask-programmed at the factory. The outputs from the register control the internal program modes.

Mode Register

Figure 4 shows data flow to and from the Mode Register.

Figure 4. Mode Register Data Flow



The Mode Register receives inputs from the CPU on the address lines: Row addresses R0-9, Column address C0-9, and Bank addresses B0, B1 and ECAS0-3. These bits are loaded into the Register when Mode Load (ML) goes low. Alternatively, the Mode Register may be programmed by initiating a 'dummy' access, as shown in the Mode Load Timing Characteristics (Figure 11, AC Switching Characteristics). ML, CS and AREQ are asserted, the addresses are loaded into the Mode Register on the falling edge of AREQ, while ML and CS are low, or when ML goes high (whichever occurs first).

It is necessary to program the chip after power up, and before using it in normal operation. The inputs to the register are encoded to control a variety of functions, as shown in Table 4. Note that inputs R10 and C10 of the KS84C32 do not program the Mode Register.

Table 4. Programming the Mode Register

RAS LOW AND RAS PRECHARGE TIME

R0, R1 — These bits control the period of time that RAS is low during refresh operations, and also determine the guaranteed RAS precharge time. The time interval shown (T) is equivalent to one Clock (CLK) cycle.

R0	R1	RAS Low Time	RAS Precharge Time
0	0	2T	1T
0	1	2T	2T
1	0	3T	2T
1	1	4T	3T

WAIT OR DTACK GENERATION FOR NON-BURST MODE ACCESSES

R2, R3, R7 — These bits control the WAIT or DTACK generation modes for R7 non-burst accesses. Bit R7 is set to select either WAIT or DTACK type of output. The time interval shown (T) is equal to one rising clock while ½T means a falling clock edge.

R7	R2	R3	WAIT High from Access RAS Low. Non-delayed Access	WAIT High from Access RAS Low, After Delayed Access	DTACK Low from RAS Low
0	0	0	No wait states	0T	—
0	0	1	No wait states	1/2T	—
0	1	0	1/2T	1/2T	—
0	1	1	1T	1T	—
1	0	0	—	—	0T
1	0	1	—	—	1/2T
1	1	0	—	—	1T
1	1	1	—	—	1-1/2T

WAIT OR DTACK GENERATION FOR BURST MODE ACCESSES

R4, R5 — R4 and R5 Control WAIT or DTACK generation modes during burst mode accesses. T is counted from burst access start.

R4	R5	Condition	
0	0	No wait states.	WAIT stays high and DTACK stays low from previous access. ½T or 1T wait states must be programmed for Nibble or 68030 Mode.
0	1	1/2T.	WAIT goes high on the falling edge of the next CLK after CAS goes low or access start.
1	0	1T.	WAIT goes high on the rising edge of the next CLK after CAS goes low. DTACK goes low one CLK cycle after CAS or access start.
1	1	0T.	WAIT(DTACK) follows CAS.

Table 4. Programming the Mode Register (Continued)

ADDS WAIT STATE

R6

R6 adds wait states to the current access if WAITIN is low.

R6	Condition
0	Hold WAIT low (DTACK high) for one extra clock period.
1	Hold WAIT low (DTACK high) for two extra clock periods.

INTERLEAVING

R8

R8 Determines whether the DRAM is accessed in interleaved or non-interleaved mode.

In interleaved mode, the row addresses are multiplexed to the DRAM controller address outputs, after the column addresses have been held for a sufficient time (25ns minimum) after CAS has gone low.

In non-interleaved mode, the column addresses are held on the DRAM controller address outputs until CAS goes high.

R8	
0	Interleaved mode
1	Non-interleaved mode

STAGGERED REFRESH OPERATIONS

R9

R9 determines whether the refresh operation is standard, or staggered.

During a standard refresh cycle, all RAS outputs will be asserted and deasserted at the same time.

In staggered refresh operations, the RAS outputs will go low in sequence, at one clock intervals. One or two RAS outputs are selected at a time, depending upon the RAS/CAS configuration selected by the setting of C4-C6. There is no error scrubbing during this type of refresh.

R9	
0	Standard refresh
1	Staggered refresh

RFCLK DIVIDER

C0, C1, C2

These bits allow the user to select the divider for the refresh clock input (RFCLK), from which the internal REFRESH clock is generated. Select divider such that the result is an approximately 2MHz clock (REFRESH).

C0	C1	C2	
0	0	0	Divide by 10
0	0	1	Divide by 6
0	1	0	Divide by 8
0	1	1	Divide by 4
1	0	0	Divide by 9
1	0	1	Divide by 5
1	1	0	Divide by 7
1	1	1	Divide by 3

Table 4. Programming the Mode Register (Continued)

REFRESH CLOCK DIVIDER

C3

C3 allows the user to divide the internal refresh clock (REFRESH), to get the required refresh cycle time.

C3	
0	Divide by 30. Divides the internal REFRESH clock (usually 2MHz) by 30, to produce a refresh clock period every 15 microseconds.
1	Divide by 26. Divides the internal REFRESH clock (usually 2MHz) by 26, to produce a refresh clock period every 13 microseconds.

RAS AND CAS CONFIGURATIONS

C4, C5, C6

These bits, in conjunction with B0 and B1 control the RAS and CAS configurations. There are four and four CAS outputs, that can be grouped so that each RAS and CAS will drive one fourth of the array, regardless of whether the array is arranged in 1, 2 or 4 banks. The setting of these bits also determines whether error scrubbing and interleaving can be supported.

C4	C5	C6	RAS and CAS Configuration Modes	Error Scrubbing	Support Interleaving
0	0	0	RAS0-3 are brought low during an access. CAS0-3 are all selected during an access but only those enabled by the corresponding ECAS can go low. B0 and B1 are not used.	Yes	No
0	0	1	RAS groups are selected by B1. B0 is not used. All CAS outputs are selected, making this mode useful for byte writing via ECAS0-3 inputs and the CAS0-3 outputs. B1 / B0: 0 / — : RAS0, 1 1 / — : RAS2,3	No	No
0	1	0	RAS, CAS pairs selected by B0 and B1. A particular CAS cannot go low unless its ECAS is also low. B1 / B0: 0 / 0 : RAS0 and CAS0 0 / 1 : RAS1 and CAS1 1 / 0 : RAS2 and CAS2 1 / 1 : RAS3 and CAS3	Yes	Yes
0	1	1	RASn is selected by B0 and B1. CAS outputs are selected with the corresponding ECAS input, making this mode useful for byte writing via ECAS0-3 inputs and the CAS0-3 outputs. B1 / B0: 0 / 0 : RAS0 0 / 1 : RAS1 1 / 0 : RAS2 1 / 1 : RAS3	No	No
1	0	0	RAS, CAS groups selected by B1. A particular CAS cannot go low unless its ECAS is also low. B1 / B0: 0 / — : RAS0, 1 and CAS0, 1 1 / — : RAS2, 3 and CAS2, 3	Yes	Yes

Table 4. Programming the Mode Register (Continued)

RAS AND CAS CONFIGURATIONS (Continued)

<table>
<tr><th>C4</th><th>C5</th><th>C6</th><th>RAS and CAS Configuration Modes</th><th>Error Scrubbing</th><th>Support Interleaving</th></tr>
<tr><td>1</td><td>0</td><td>1</td><td>RAS, CAS groups are selected by B1. A particular CAS cannot go low unless its ECAS is also low.<table><tr><th>B1</th><th>B0</th><th></th></tr><tr><td>0</td><td>—</td><td>RAS0, 1 and CAS0, 1</td></tr><tr><td>1</td><td>—</td><td>RAS2, 3 and CAS2, 3</td></tr></table></td><td>No</td><td>Yes</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>RAS0-3 and CAS0-3 are all selected during an access. This mode is useful for byte writing via ECAS0-3 inputs and the CAS0-3 outputs. B0 and B1 are not used.</td><td>No</td><td>No</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>RASn and CASn are selected by B0 and B1. A particular CAS cannot go low unless its ECAS is also low.<table><tr><th>B1</th><th>B0</th><th></th></tr><tr><td>0</td><td>0</td><td>RAS0 and CAS0</td></tr><tr><td>0</td><td>1</td><td>RAS1 and CAS1</td></tr><tr><td>1</td><td>0</td><td>RAS2 and CAS2</td></tr><tr><td>1</td><td>1</td><td>RAS3 and CAS3</td></tr></table></td><td>No</td><td>Yes</td></tr>
</table>

COLUMN ADDRESS SETUP TIME SELECTION

C7

C7 allows the user to select a minimum guaranteed setup time (t_{ASC}) for the column address inputs.

C7	
0	Selects 10ns setup time.
1	Selects 0ns setup time.

ROW ADDRESS HOLD TIME SELECTION

C8

C8 allows the user to select a minimum guaranteed hold time (t_{RAH}) for the row address inputs.

C8	
0	Selects 20ns hold time.
1	Selects 12ns hold time.

DELAY CAS DURING WRITE ACCESSES

C9

C9 allows the user to delay CAS during write operations. If no delay is selected, CAS is treated in the same way for read and write operations. If delay is selected, CAS is delayed for one rising clock edge after RAS goes low.

C9	
0	No delay.
1	Delay selected.

Table 4. Programming the Mode Register (Continued)

ADDRESS LATCH	
B0	B0 allows the user to decide whether address inputs should be latched by $\overline{ADS}$/ALE, or whether the address latches should be permanently transparent and merely allow passage of the address inputs. **B0** — 0: Address bits latched. 1: Address latches transparent. Note: If $\overline{ECAS2}$ is set to '1' (Page Mode) in the Mode Register, then the Row Address is always latched independent of B0. For static column operation, B0 can be set to '1' or '0'.
ACCESS MODES	
B1	B1 allows the user to select either synchronous or asynchronous access modes. In Mode 0 (synchronous), access is controlled by the system clock, and the access $\overline{RAS}$ is initiated on the rising edge of the first clock input after ALE goes high. $\overline{AREQ}$ is used to hold $\overline{RAS}$ low during access. In Mode 1 (asynchronous), the leading edge of $\overline{ADS}$ initiates access immediately, and the rising edge of $\overline{AREQ}$ terminates $\overline{RAS}$. **B1** — 0: Access Mode 0 (synchronous). 1: Access Mode 1 (asynchronous)

PROGRAMMING THE KS84C31/32

User Selection	INTERNAL PROGRAMMING MODES
$\overline{\text{ECAS0}}$	**$\overline{\text{CAS}}$ DELAY**
0	$\overline{\text{CAS}}$ outputs are negated when $\overline{\text{AREQ}}$ goes high.
1	$\overline{\text{CAS}}$ outputs stay low till the next rising edge of CLK after $\overline{\text{RAS}}$ is deasserted by $\overline{\text{AREQ}}$.
$\overline{\text{ECAS1}}$	**68030 MODE**
0	Non 68030 mode (default)
1	**68030 Mode:** This mode supports the fast synchronous cache fill of the 68030. The handshake signals $\overline{\text{CBREQ}}$ and $\overline{\text{CBACK}}$ on pin 54 and 36 (pin 65 and 43 on KS84C32) can be connected with the corresponding 68030 signals.
$\overline{\text{ECAS2}}$	**PAGE MODE**
0	Non Page Mode (default)
1	**Page Mode/Static Column Mode:** Non Interleave. The Row Address is strobed according the setting of B0 of the Mode Register into the Row Address Latch. If the address is different from the previous one then the output signal PMISS is asserted when an access is requested. Individual $\overline{\text{CAS}}$s can be select by the corresponding $\overline{\text{ECAS}}$ inputs. See Page Mode.
$\overline{\text{ECAS3}}$	**NIBBLE MODE**
0	Non nibble mode (default)
1	**Nibble Mode:** In this mode up to 4 access cycles can be performed without precharging the rows. $\overline{\text{CAS}}$ stay low for min one clock period during the nibble access after $\overline{\text{DTACK}}$ did go low. $\overline{\text{CAS}}$ stays high ½T period for the $\overline{\text{CAS}}$ precharge time. $\overline{\text{AREQ}}$ going high ends the burst access at any time. An individual $\overline{\text{CAS}}$ output can be disabled with the corresponding $\overline{\text{ECAS}}$ input for byte access.

Access Modes

The KS84C31/32 supports both synchronous and asynchronous operations. The user can select the mode most suited to the microprocessor with which the DRAM is interfacing, by means of bit B1 in the Mode Register.

Mode 0 — Synchronous Access

Mode 0 is selected when B1 = 0. To initiate a Mode 0 operation, ALE must pulse high t_{02} before the rising edge of the clock input (CLK). Provided that the chip select signal ($\overline{\text{CS}}$) has been established at t_{01} before the rising edge of the next CLK input, access will start on the rising edge of that CLK. The Address register will be reloaded only if there is an access started with $\overline{\text{CS}}$ low before the rising edge of CLK.

Since ALE is high, the address latch is transparent to the address inputs, and, if the chip is programmed in Address Latch Mode (B0 = 0), the latch stores the address bits that were present one setup time (t_{06}) before the high-to-low transition of ALE. If the chip is not in Latch Mode (B0 = 1), the address inputs have to meet the setup time of t_{05} to the rising edge of CLK, to make sure that the row address bits are on the Q output when row address strobe ($\overline{\text{RAS}}$) is asserted.

Mode 1 — Asynchronous Access

Mode 1 is selected when B1 = 1. To initiate a Mode 1 operation, $\overline{\text{CS}}$ must be low for t_{12} before $\overline{\text{ADS}}$ goes low. If the chip is programmed in Address Latch Mode, the address latch stores the address that was present one set up time t_{14} before the high-to-low transition of the $\overline{\text{ADS}}$ signal. In order to latch the R/C/B inputs into the address latches, $\overline{\text{CS}}$ must be low. The address is strobed with the start of an access at the falling edge of $\overline{\text{ADS}}$. The address latches are transparent while $\overline{\text{ADS}}$ is high.

Access Features

The KS84C31/32 features a number of different access methods to DRAMs that improve either the cycle time or the RAS/CAS access time. The data throughput and therefore the CPU performance can be greatly enhanced by utilizing these features.

The KS84C31/32 support both interleaved and non-interleaved memory operation. Interleaving is controlled by the R8 input to the Mode Register.

Non-Interleaving

When R8 is set at 1, the chip does not support interleaving. The address lines from the microprocessor are connected to the Row (R), Column (C), and Bank (B) inputs of the KS84C31. B0 and B1 (bank address bits) may be connected to the most significant or the least significant address bits.

Access starts in Mode 0 if ALE pulses high t_{02} before the edge of the CLK input. In 1, access starts when CS remains low for t_{12} before the falling edge of ADS. In both cases, access is terminated when AREQ goes high, terminating RAS. CAS goes high or stays low until the rising edge of the next CLK, as programmed by ECAS0.

Interleaving

With R8 set at 0, the chip supports interleaved accessing of the DRAM. This is a way of reducing access cycle time. In interleaved mode, access cycles (read or write) are overlapped, so that before an access cycle is completed in one memory bank location, another access may be started in a different memory bank. Since the precharge time of most DRAMs is between 80 and 100 nanoseconds (about the same length as t_{RAS}), interleaving can save up to 50% of cycle time.

Memory accesses can only be overlapped in physically separated banks of memory, and may occur during precharge time.

Interleaving can take place in either Mode 0 or Mode 1.

Performance is enhanced if consecutive accesses are made to different memory banks by hiding the precharge time in the access of subsequent access cycles. The KS84C31/32 supports access to up to 88 DRAMs, arranged in up to four banks, each containing 16 memory devices for data and 6 for error correction. The bank address bits, B0 and B1 are the least significant bits, as seen by the CPU. The KS84C31/32 ensures that the DRAM will be precharged for the programmed number of CLK cycles by inserting Wait States. The precharge counter, as programmed by R0 and R1, keeps track of the CLK input, and after reaching the programmed number, the rising edge of the CLK input is used to complete the current cycle. The precharge counter starts with the rising edge of the first CLK input (which is counted as 1T) that occurs after the low-to-high transition of AREQ. There is a required setup time to the rising edge of CLK of t_{C22}.

Static Column Access

In order to perform a static column access to a DRAM, the KS84C31/32 has to be programmed for Page Mode operation. The row address will be latched and compared with the row address of the previous address and validated at the time of the access start which is either the rising edge of CLK after ALE goes high (access mode 0) or the falling edge of ADS (access mode 1). The Column Address Latch can be in fall through or latch mode. A change of the row address will assert the output PMISS (page miss) and the current access cycle will be terminated. After the DRAM has been precharged, the pending access will be executed by asserting the RASn and CASn outputs. A full RAS/CAS access by deasserting AREQ must be invoked after maximum 100μs according to the DRAM specs for maximum RAS pulse width. (See Forced Refresh).

ECAS inputs must also be low in order to enable the CAS outputs. Wait states for the burst access are counted from the time the access starts.

Page Access

The conventional page access works similar to the static column access with the difference that the columns have to be precharged by bringing CAS high. As with static column operation, the KS84C31/32 has to be programmed for Page Mode operation. A CASn output must be deasserted by an ECASn input. The column address latch becomes transparent while ADS/ALE is high not when ECAS goes high. ECAS can be connected to the ALE signal. CASn will be asserted by the ECASn input. In case of a page miss or after the 5th internal refresh request, PMISS will be asserted and the access should be terminated by feeding PMISS back to AREQ input.

A wait state during the burst access is terminated with the falling edge (1/2T) or the rising edge (1T) of CLK after the access starts. That means ECAS has no influence on the wait state termination except if 0T is programmed. In this instance DTACK follows CAS.

Forced Refresh

The RAS pulse width t_{RASC} of most DRAMs is limited to 100 μs. The KS84C31/32 will force a refresh after the 5th internal refresh request which should be every 75μs. PMISS will be asserted allowing to terminate the RAS cycle. The page access has to be terminated by forcing AREQ high which in turn will bring RAS, CAS and DTACK high, (WAIT output low). The deferred 5 refresh cycles will be performed in a burst refresh to ensure that the refresh period will not be exceeded. PMISS is high until a page address has been strobed into the DRAMs.

68030 Mode

The KS84C31/32 can be interfaced with a 68030 CPU with minimum interface logic requirement if the Mode Register ECAS1 has been loaded with '1' (default is '0'). The interface provided takes advantage of the fast nibble mode access for filling the cache of the 68030 which is a synchronous operation terminated with STERM. STERM can be connected to DTACK output of the KS84C31/32. CBREQ (Cache Burst Request) and CBACK (Cache Burst Acknowledge) of the 68030 can be connected to the corresponding signals of the EDRC.

Note: If 68030 mode is programmed then Error Scrubbing is not supported.

An access is initiated by loading the address A2–A22(24) into the address latch of the KS84C31/32. A0 and A1 together with SIZ0 and SIZ1 determine the byte selected. (See Figure 16, 17).

The first access is a non burst access and is initiated with ADS which can be connected to AS of the 68030. RAS and CAS are asserted based on the internal delay line. If CBREQ is asserted, the KS84C31/32 responds by acknowledging the request with CBACK at the time DTACK is going low. If the CPU scans a low on STERM input (which is connected to DTACK output) at the rising edge of CLK, it will latch the data at the next falling edge of CLK. At this falling edge, CAS will go high.

Burst Access:

The CAS precharge time is 1/2T of the CLK. The CAS low time depends on the programmed state of R4 and R5. If 1T of wait state is programmed, DTACK will be high until the next rising edge of CLK after CAS goes low. If 1/2 is programmed then DTACK ends with the falling edge which accounts for 1T. t_{NCP} is always a 1/2 clock cycle. After DTACK goes Low, the DRC counts one rising edge of CLK. At this time DTACK will be deasserted. At the next falling CLK edge, and CAS will be deasserted again. There is a minimum hold time of CLK to CAS high in order to assure sufficient data hold time.

This sequence continues until CBREQ goes high. The last nibble access is determined by the signal CBREQ. If this signal goes high, CBACK will be negated and one more nibble access will be performed. The RAS output is negated at AREQ rising edge which can be AS of the CPU. AREQ can terminate the nibble access at any time.

DTACK follows CAS if 0T is programmed. (R4 = 1, R5 = 1). The Mode setting, No wait state R4 = 0, R5 = 0 is not allowed. A minimum of 1/2T or 1T must be programmed.

Asynchronous operation of the 68030 is also supported. In this mode, the 68030 operates like a 68020 and the KS84C31/32 should be programmed either in interleave non-interleave or page mode.

Nibble Mode

One of the fastest possible access modes is the nibble access that allows access to up to 4 memory locations without having to supply the column address and with only one RAS precharge period. This type of access, though very fast, is not used commonly. The reason for that is the interface overhead required to generate the proper timing for the nibble access and the availability of nibble mode DRAMs. With the advent of cache controller and CPUs with cache memory on chip, the nibble access is the preferred method to fill the cache. One example is the 68040 which works best with nibble access and is shown in Figure 18, 19).

The first access which is a non burst access is started with ADS or CLK according to the setting of mode bit B1. The RAS/CAS arbitration is controlled by the on chip delay line. Wait states are programmed by R2 and R3. CAS stays low until the next rising edge of CLK after DTACK did acknowledge the access. The data should be scanned at the rising or falling edge of CLK (the 68040 will scan data on the rising edge). DTACK goes high with the falling edge of CLK.

Burst Access:

A burst access is initiated by CAS going high and CAS will stay high for a half clock period. DTACK stays high for the programmed number of wait states start counting with CAS falling edge. DTACK will stay low until the next falling edge. The CPU will sample data at the next rising clock edge. At this edge CAS will be deasserted which ends the nibble access. There is a minimum CAS hold time built in in order to guarantee sufficient data hold time.

If 0T is programmed (R4 = 1, R5 = 1), DTACK follows CAS and CAS is controlled by ECAS input.

The mode setting R4 = 0, R5 = 0 may not be used in nibble mode. This is due to the CAS low time is being measured from DTACK going low. Since no wait state are programmed, DTACK would go low only for the non-burst access and CAS would go high immediately.

The CAS precharge time also can be expanded by disabling CAS from going low with the corresponding ECAS input or a particular CAS can be disabled for byte access.

The burst can be terminated at any time by AREQ. If this input is going high, all RASs will go high and stay high minimal the programmed precharge time. CASs also will be deasserted but can be delayed from going high till the next rising edge of CLK to guarantee sufficient data hold time (program ECAS0 to '1').

CS has to be low with a setup hold time to the first access. During consecutive nibble access cycles, CS may be high.

Delay CAS

An early write cycle to a DRAM is useful if the input data is not stable at the falling edge of WE, or if bidirectional data buffers are used. With this sort of access, WE goes low before CAS is low. The column address bits and data are stored in the DRAM latches on the falling edge of CAS. The data output buffer of the DRAM is tri-stated during the entire RAS cycle.

To achieve an early write cycle, the CAS output of the KS84C31/32 can be delayed one CLK cycle, if bit C9 of the Mode Register is set appropriately. CAS will go low t_{C24} after the rising edge of CLK. If CAS has been delayed in this way, and requires further delay, this can be done by holding ECASn high, which prevents CAS from going low.

Conversely, a late write access may be required, in which WE is asserted after CAS. In this case, the column address bits are latched into the DRAMs on the falling edge of CAS and the input data is latched on the falling edge of WE.

Standard Access Operations

The versatile KS84C31/32 chips support a variety of DRAM operations. They enable read and write accesses, in synchronous or asynchronous mode, with or without interleaving, and in burst or non-burst mode. Typical operations are illustrated in the timing diagrams at the end of this Product Description.

Operating Features

DRAM performance is optimized under the control of the KS84C31/32, as a function of the special operating features designed into the chips. This section describes some of the features that enhance DRAM performance.

Controlling Precharge Time

The precharge time of the DRAM, or the time the chip takes to restore the data between accesses, negatively impacts the overall access speed of the memory devices. Since the DRAM performance is generally trailing CPU throughput time, the DRAM controller can play an important role in improving overall system performance.

RAS Low and RAS Precharge Time. RAS precharge time can be programmed using bits R0 and R1 in the Mode Register. The precharge time is guaranteed during access and refresh. RAS low and RAS precharge times are counted by the rising edges of the CLK input. Each bank of memory devices has its own precharge counter. This is an important feature, since the KS84C31/32 allows memory interleaving of 2 or 4 memory banks.

AREQ must go high at t_{C22} with respect to the rising edge of the CLK input, to be counted as 1T of the programmed precharge time. (This means that 1T can be somewhat less than one clock period.)

The KS84C31/32 inserts Wait States as required, to keep the CPU and DRAM interactions in step. The system designer is responsible, however, for making sure that the appropriate numbers of Wait States are inserted to keep RAS low for the period of time required by the DRAM specification.

CAS Precharge Time. The ECASn input controls CAS precharge time during a burst access. The CASn output is a direct function of the ECASn input.

In 68030 and Nibble Mode, the CAS precharge time is dependent on the CLK input. Individual CASs can be enabled/disabled by the corresponding ECAS input.

Wait States

Wait states are required when a relatively slow DRAM is operating with a fast CPU. The KS84C31/32 generates the WAIT signal, and sends it back to the CPU instructing it to insert a Wait State. This means that the CPU will not look for data prematurely, and during a Refresh operation, an access is deferred. Bit R7 of the Mode Register must be set to '0' to instigate this feature.

If the Wait state is not selected, the KS84C31/32 generates a handshaking signal, DTACK, which is returned to the CPU to acknowledge transfer of data.

Wait states are counted in terms of CLK cycles. 1T of wait state means DTACK goes low with the rising edge of CLK after RAS started the DRAM access by a high/low transition, or in case of page mode after the burst access started. ECAS has influence on the WAIT (DTACK) output only if 0T (R4, 5 = '1') is programmed. DTACK will be high (WAIT low) until the page compare is completed and no page miss has been detected. WAIT is not asserted if there is no access to the DRAM.

3

Refresh Operations

The KS84C31/32 provide a number of refresh options, as described below.

Automatic Internal Refresh

Internal refresh is generated by an internal refresh counter, which keeps track of the refresh intervals, and also supplies the row address bits required to refresh the memory area. (Internal refresh is a $\overline{RAS}$-only operation.) The refresh period is selected by bits C0, C1, C2 and C3 of the Mode Register.

The refresh period for most DRAMs is 15 microseconds. This means that the one megabit DRAM has to be refreshed every eight milliseconds, during which time, 512 rows must be accessed. This calls for a 9-bit refresh counter. The KS84C31 has a 10-bit counter, and the KS84C32 has an 11-bit counter. The extra bits are used for error scrubbing over the whole address range.

If a refresh is requested by the on-chip Refresh counter, while an access is in progress, that access is finished before the refresh cycle is initiated. The next access is deferred until the refresh cycle is complete. The wait logic automatically inserts Wait States.

Internal refresh is possible in both interleaved and non-interleaved modes.

Forced Refresh

The $\overline{RAS}$ pulse width t_{RASC} of most DRAMs is limited to 100 μs. The KS84C31/32 will force a refresh after the 5th internal refresh request which should be every 75μs. PMISS will be asserted allowing to terminate the $\overline{RAS}$ cycle by feeding this output back to the $\overline{AREQ}$ input. The page access has to be terminated by forcing $\overline{AREQ}$ high which in turn will bring $\overline{RAS}$, $\overline{CAS}$ and $\overline{DTACK}$ high. ($\overline{WAIT}$ output low). The deferred 5 refresh cycles will be performed in a burst refresh to ensure that the refresh period will not be exceeded. PMISS is high until a page address has been strobed into the DRAM.

Automatic Internal Staggered Refresh

Staggered refresh, during which the $\overline{RAS}$ signals are staggered at one CLK intervals, can be selected by appropriately setting bit R9 in the Mode Register. This type of cycle allows the memory area to be refreshed in two or four refresh operations that are interspersed with regular memory accesses. Staggering refresh operations reduces the switching current.

External Controlled Refresh

Refresh operations can be controlled externally and can be either staggered or non-staggered. As for internal refresh, the row address bits are supplied by the on-chip refresh counter. External refresh is a $\overline{RAS}$ only refresh.

Internal refresh must be disabled by driving $\overline{DISRFSH}$ low. $\overline{RFSH}$ must go low at setup time t_{R1}.

Refresh Request Divider

The refresh request divider (derived from the programmable divider asserts $\overline{RFRQ}$, if internal or external refresh has been selected by $\overline{DISRFSH}$.

Clearing the Refresh Counter (Row Address)

The refresh counter is cleared by driving $\overline{DISRFSH}$ high and $\overline{RFSH}$ low, with a setup time of t_{R1} to the rising edge of CLK. This procedure does not invoke a refresh of the DRAM.

Error Scrubbing

In a system with error correction, transparent error scrubbing is one method of increasing data integrity. A full access is performed during refresh, during which data and ECC bits are continuously updated and checked, and random bit errors corrected. The error scrubbing option is selected by appropriately setting bits C4, C5 and C6 of the Mode Register.

When the KS84C31/32 are programmed for error scrubbing, a complete memory access is performed during the refresh cycle. The 12- or 13-bit internal scrubbing counter provides the column address bits, and the 10- or 11-bit refresh counter provides the row address bits. Error scrubbing is done by word, not by byte.

If the error correction circuitry detects an error, the error is corrected by writing the corrected word to the DRAM by means of the read-modify-write operation. (The data is read and checked during the read portion, and modified/corrected data is written back during the write portion.)

To enable this type of cycle, $\overline{EXTDRF}$ must be asserted while $\overline{RAS}$ is low. $\overline{RAS}$ and $\overline{CAS}$ remain low until the rising edge of the next CLK, after EXTDRF has gone low again.

Although the KS84C31/32 control the error scrubbing, they do not provide the error correction circuitry.

DC ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

DC Supply Voltage 7V
Temperature Under Bias .... 0°C + 70°C
Storage Temperature .... -65°C to 150°C
All Input and Output Voltage ..... V_{SS} - 0.5V to +7V
Power Dissipation at 33MHz 0.6W
E.S.D. 4000V

Note: If the device is used beyond the maximum rating, permanent damage may occur. Operation should be limited to those conditions specified under DC Electrical Characteristics.

DC Electrical Characteristics (T_A = 0°C to +70°C, V_{CC} = 4.5V to 5.5V, V_{SS} = 0V)

3

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input High Voltage	Tested with limited Test pattern	2.0		V_{CC}+0.5	V
V_{IL}	Input Low Voltage	Tested with limited Test pattern	-0.5		0.8	V
V_{OH1}	Q and $\overline{WE}$ Outputs	I_{OH} = -10mA	2.4			V
V_{OL1}	Q and $\overline{WE}$ Outputs	I_{OL} = 10mA			0.5	V
V_{OH2}	All outputs except Q and $\overline{WE}$	I_{OL} = -3mA	2.4			V
V_{OL2}	All outputs except Q and $\overline{WE}$	I_{OL} = 3mA			0.5	V
I_{IN}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}			±10	μA
I_{ILML}	$\overline{ML}$ Input Current	V_{IN} = V_{SS}			200	μA
I_{CC1}	Quiescent Current	CLK at 33MHz Inputs Inactive			20	mA
I_{CC2}	Supply Current	Inputs Active (I load = 0)			2.5	mA/MHz
C_{IN}	Input Capacitance	f_{IN} at 1MHz		5	10	pF

AC SWITCHING CHARACTERISTICS

Figure 5 shows a typical test circuit, while Figure 6 shows the output drive levels. Figures 7 through 14 provide switching characteristics for a number of typical KS84C31/32 operations:

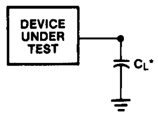
Unless otherwise stated V_{CC} = 4.5V to 5.5V, 0 < T_A < 70°C

Load Capacitance: Q0-Q9, Q10 — C_L = 380pF
$\overline{WE}$ — C_L = 500pF
$\overline{RAS0-3}$, $\overline{CAS0-3}$ — C_L = 125pF
All other Outputs — C_L = 50pF

All minimum and maximum values are measured in nanoseconds.

CAPACITIVE LOAD SWITCHING

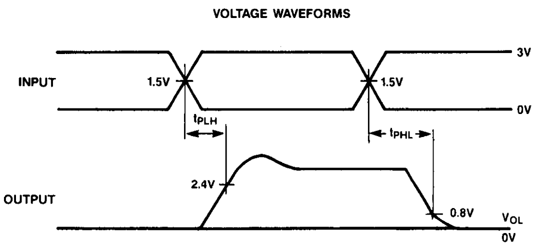
Figure 5. Switching Test Circuit



*t_{PD} SPECIFIED AT C_L = 380pF ALL Q OUTPUTS
C_L = 125pF ALL BUT Q AND PMISS OUTPUT
C_L = 500pF WE OUTPUTS
C_L = 50pF PMISS OUTPUTS

TYPICAL SWITCHING CHARACTERISTICS

Figure 6a. Output Drive Levels



AC Testing inputs are driven at 3.0V for a logic "1" and 0.0V for a logic "0". Timing measurements are made at 2.4V for a logic "1" and 0.8V for a logic "0" at the outputs.

Figure 6b. Simplified Output Driver Schematic

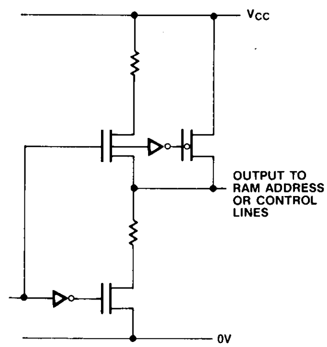
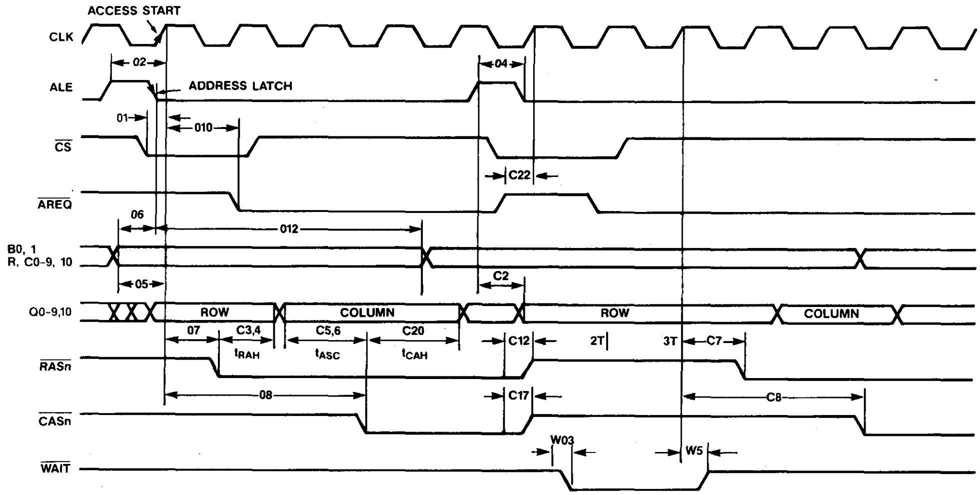


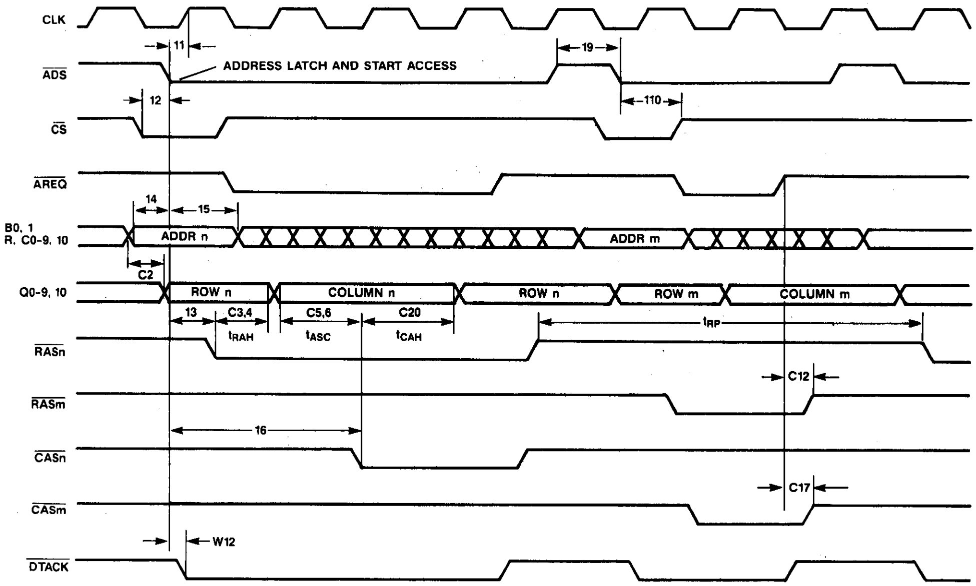
Figure 7. Mode 0 Interleave



No.	Parameter	-25 Min	-25 Max	-33 Min	-33 Max
01	$\overline{CS}$ Low to CLK Rising Edge	10		5	
02	ALE High to CLK Rising Edge	15		10	
04	ALE Pulse Width	15		10	
05a	Address Set-up to CLK Rising Edge using the On-Chip Address Latch	10		10	
05b	Address Set-up to CLK Rising Edge not using the On-Chip Address Latch	20		20	
06	Address Set-up to ALE Falling Edge using the On-Chip Address Latch	10		10	
07	CLK Rising Edge to $\overline{RAS}$ Low		35		30
08	CLK Rising Edge to $\overline{CAS}$ Low (non-delayed access)				
a	t_{RAH} = 12ns, t_{ASC} = 0ns		85		80
b	t_{RAH} = 12ns, t_{ASC} = 10ns		95		90
c	t_{RAH} = 30ns, t_{ASC} = 0ns		95		90
d	t_{RAH} = 30ns, t_{ASC} = 10ns		105		100
010	$\overline{CS}$ Low after access start	10		10	
012	Address Hold Time from ALE falling edge using the On-Chip Address Latch	20	15		

No.	Parameter	-25 Min	-25 Max	-33 Min	-33 Max
C3	Row Address Hold Time, t_{RAH} = 12ns	12		11	
C4	Row Address Hold Time, t_{RAH} = 20ns	20		20	
C5	Column Address Set-up Time t_{ASC} = 0ns	0		0	
C6	Column Address Set-up Time t_{ASC} = 10ns	10		10	
C7	CLK Rising Edge to $\overline{RAS}$ active after delayed access		35		30
C8	CLK Rising Edge to $\overline{CAS}$ active after delayed access				
a	t_{RAH} = 12ns, t_{ASC} = 0ns		85		80
b	t_{RAH} = 12ns, t_{ASC} = 10ns		95		90
c	t_{RAH} = 20ns, t_{ASC} = 0ns		95		90
d	t_{RAH} = 20ns, t_{ASC} = 10ns		105		100
C12	$\overline{AREQ}$ High to $\overline{RAS}$ High		35		30
C17	$\overline{AREQ}$ High to $\overline{CAS}$ High		35		30
C20	Column Address Hold Time in Interleave	25	40	25	40
C22	$\overline{AREQ}$ High to CLK Rising Edge to recognized as 1T of $\overline{RAS}$ precharge	15		10	
W03	CLK Rising Edge to $\overline{WAIT}$ Low		30		25
W5	CLK Rising Edge to $\overline{WAIT}$ High		30		25
W05	CLK High to $\overline{DTACK}$ Low 0T Programmed		35		30

Figure 8. Mode 1, Interleave, Address Latch

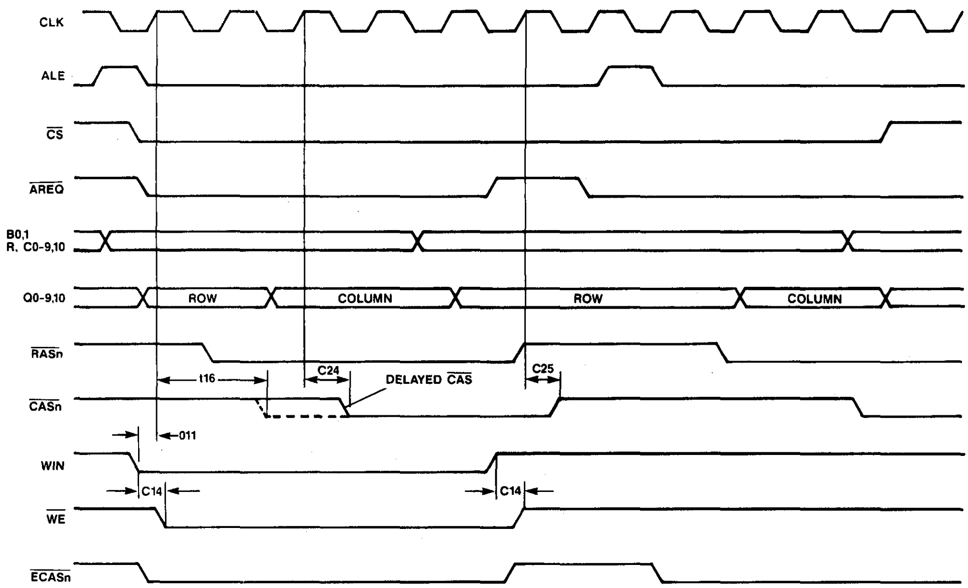


No.	Parameter	-25 Min	-25 Max	-33 Min	-33 Max
C2	Address to Q output		35		30
C3	Row Address Hold Time t_{RAH} = 12ns	15		12	
C4	Row Address Hold Time t_{RAH} = 20ns	25		20	
C5	Column Address Set-up Time t_{ASC} = 0ns	0		0	
C6	Column Address Set-up Time t_{ASC} = 10ns	10		10	
C12	AREQ High to RAS High		35		30
C17	AREQ High to CAS High				
C20	Column Address Hold Time in Interleave	25	40	25	40
W12	ADS Low to DTACK Low 0T from RAS Programmed R2, 3 = '0', R7 = '1'		40		30

No.	Parameter	-25 Min	-25 Max	-33 Min	-33 Max
11	ADS Low to CLK, to guarantee WAIT DTACK output	25		15	
12	CS to ADS Low Set-up Time	5		5	
13	ADS Falling Edge to RAS Low during an Access		35		35
14a	Address Set-up to ADS Falling Edge using the On-Chip Address Latch	10		10	
14b	Address Set-up to ADS Falling Edge not using the On-Chip Address Latch	10		10	
15	Address Hold after ADS Falling Edge using the On-Chip Address Latch	8		8	
16	ADS Low to CAS Low C9 = '0' (not delayed access)				
a	t_{RAH} = 12ns, t_{ASC} = 0ns		85		
b	t_{RAH} = 12ns, t_{ASC} = 10ns		95		
c	t_{RAH} = 20ns, t_{ASC} = 0ns		95		
d	t_{RAH} = 20ns, t_{ASC} = 10ns		105		
19	ADS High Pulse Width	10			
110	CS Low after access start	10			

3

Figure 9. Non-Interleave — Delay CAS



No.	Parameter	-25 Min	-25 Max	-33 Min	-33 Max
011	WIN low to CLK Rising Edge to delay CAS (C9 = '1')	5		5	
C14	WIN to WE		40		33
C24	CLK Rising Edge to CAS Low if delayed by WIN		30		30
C25	CLK Rising Edge to CASn High if ECASn Low at AREQ (if delay programmed by ECAS0)		30		30

No.	Parameter	-25 Min	-25 Max	-33 Min	-33 Max
C18	CLK High	15		13	
C18a	CLK Low	15		13	
C19	CLK Period	40		33	
C28	RFCLK High	15		15	
C28a	RFCLK Low	15		15	
C29	RFCLK Period	40		40	

Figure 10. CLK, RFCLK Timing

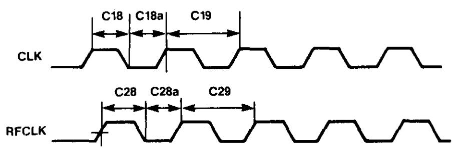


Figure 11. KS84C31/32 Static Column Operation Mode 1

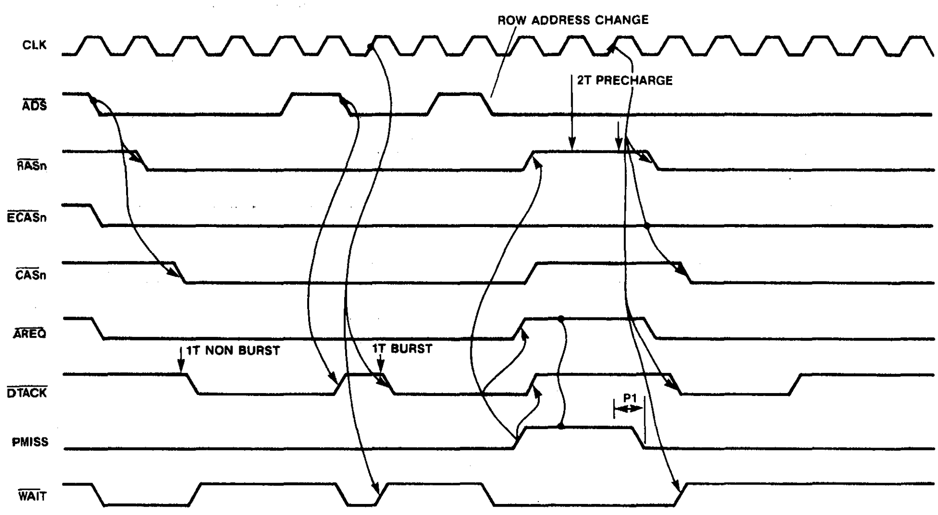


Figure 12. KS84C31/32 Page Mode Operation Mode 1

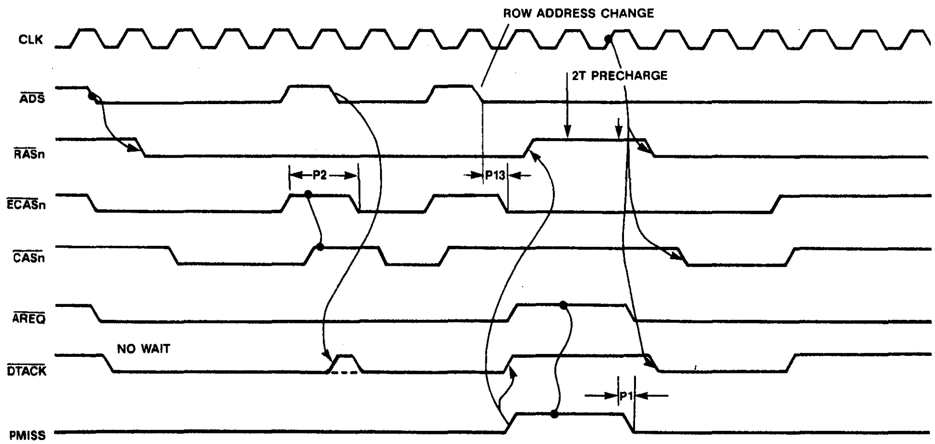
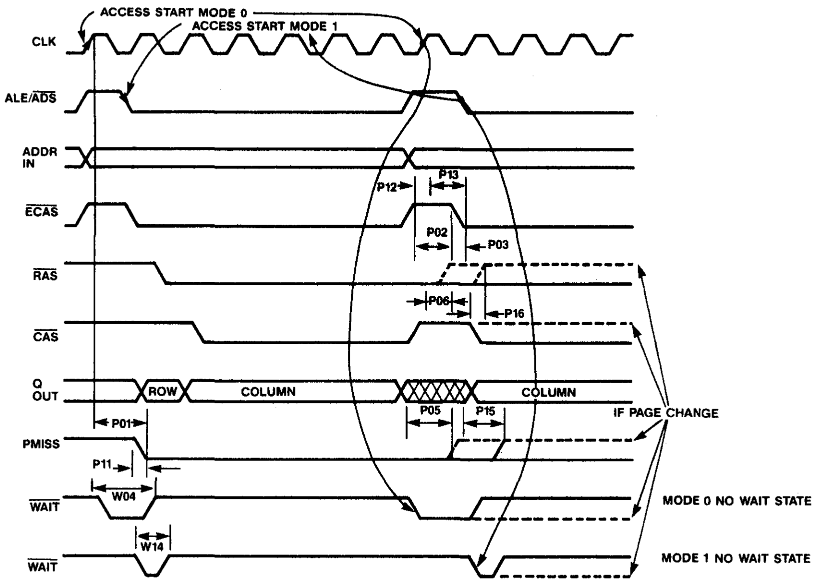


Figure 13. KS84C31/32 Page Mode Operation



Mode 0:

No.	Parameter	-25 Min	-25 Max	-33 Min	-33 Max
P01	Burst access start to PMISS low (50pF load)		30		25
P02	$\overline{\text{ECASn}}$ high setup to access start	10		10	
P03	$\overline{\text{ECASn}}$ hold from access start	20		20	
P04	Access start to $\overline{\text{CAS}}$ low if page hit ($\overline{\text{ECAS}}$ hold = 0ns)	25		25	
P05	PMISS high from access start (50pF load)		15		15
P06	$\overline{\text{RAS}}$ high from access start if page miss		35		30

Mode 1:

No.	Parameter	-25 Min	-25 Max	-33 Min	-33 Max
P11	Burst access start to PMISS low (50pF load)		30		25
P12	$\overline{\text{ECASn}}$ high setup to access start	10		10	
P13	$\overline{\text{ECASn}}$ hold from access start	20		20	
P14	$\overline{\text{ADS}}$ low to $\overline{\text{CAS}}$ low if page hit ($\overline{\text{ECAS}}$ hold = 0ns)		25		25
P15	PMISS high from access start (50pF load)		15		15
P16	$\overline{\text{RAS}}$ high from access start if page miss		35		30

Mode 0 and 1:

No.	Parameter	-25 Min	-25 Max	-33 Min	-33 Max
P1	PMISS low from deferred access start (50pF load)		15		15
P2	$\overline{\text{ECAS}}$ high width	15		15	

Figure 14. KS84C31/32 Simplified Logic for Page Mode

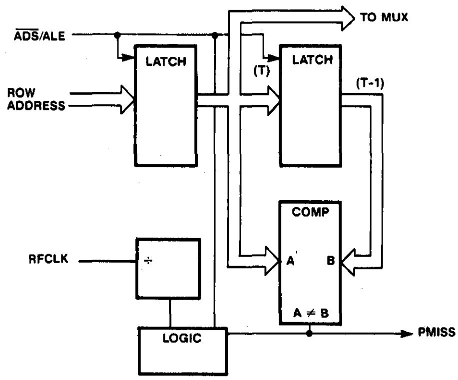


Figure 15. Page Mode Interface with 68020

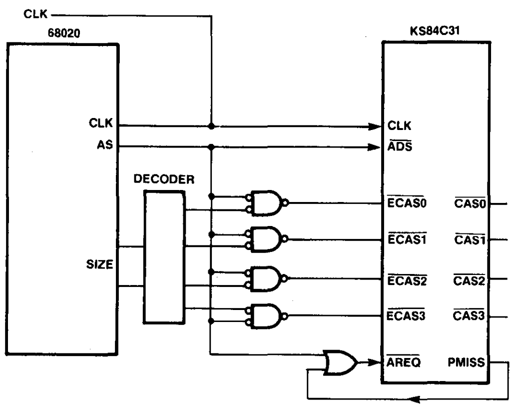
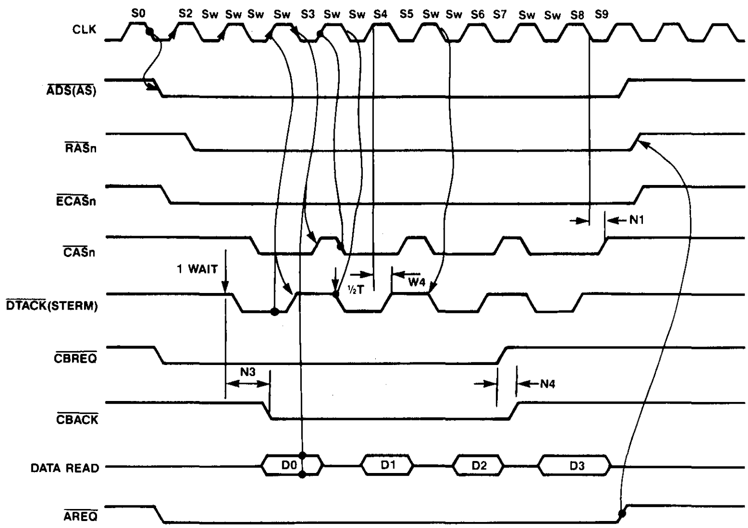


Figure 16. 68030 Cache Fill Operation, Nibble Mode Access with 68030 Wait States Mode 1



Nibble Mode A.C. Parameter

No.	Parameter	-25 Min	-25 Max	-33 Min	-33 Max
N1	CLK to $\overline{CAS}$ high	5	20	4	15
N2	CLK to $\overline{CAS}$ low		20		15
N3	CLK to $\overline{CBACK}$ low		18		14
N4	CLK to $\overline{CBACK}$ high		18		14
W4	CLK to $\overline{DTACK}$ high		30		25

Figure 17. 68030 — KS84C31/32 Interface

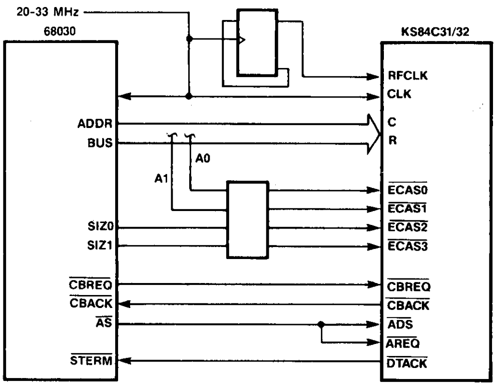


Figure 18. 68040 or Similar CPU or Cache Interface KS84C31/32 Interface Timing with Nibble Mode Burst Access

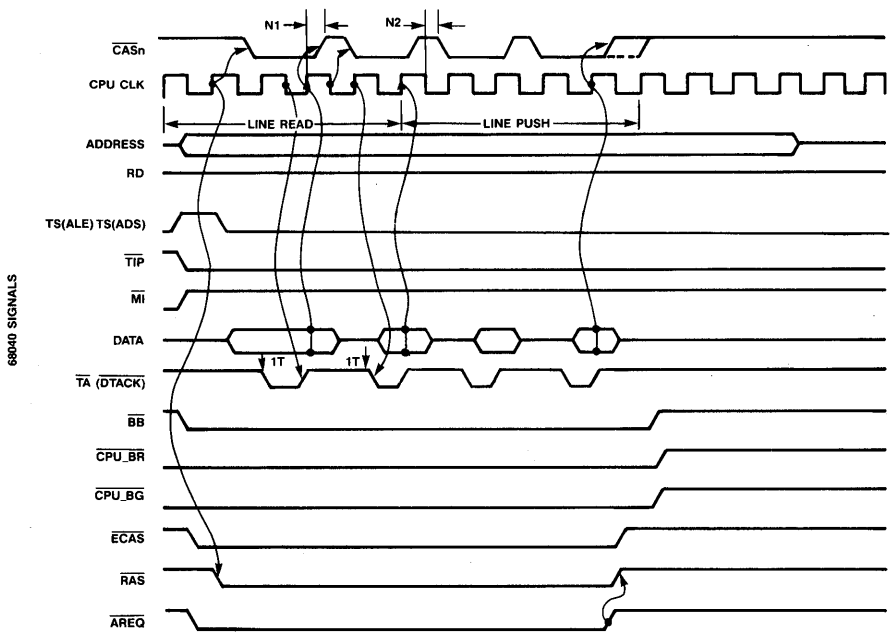
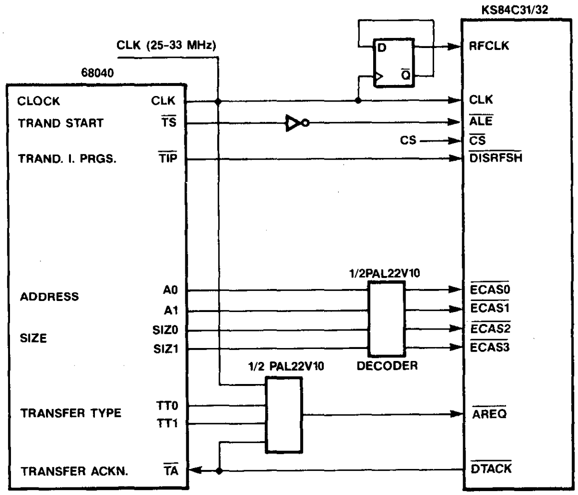
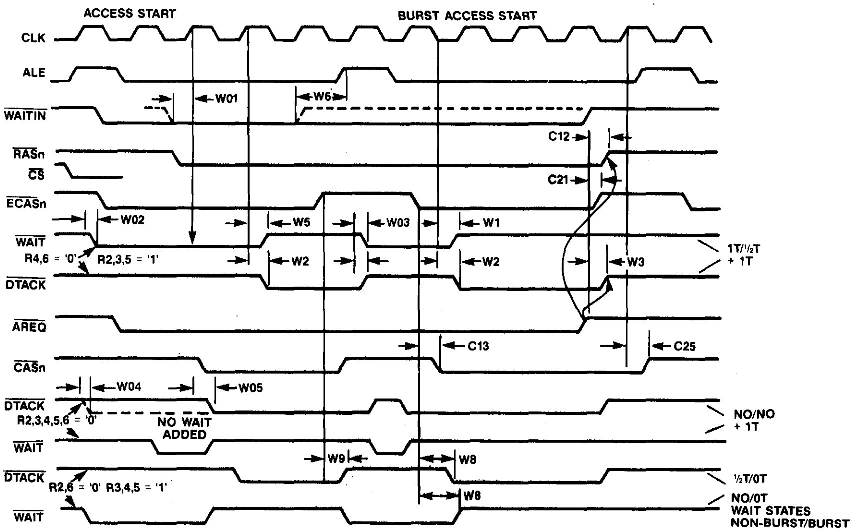


Figure 19. 68040 — KS84C31/32 Interface



3

Figure 20. Mode 0, Wait State, Non-Interleave with Burst Access



No.	Parameter	-25 Min	-25 Max	-33 Min	-33 Max
C12	AREQ High to RAS High		35		
C13	ECASn High to CASn High		25		
	ECASn Low to CASn Low		·		
C21	AREQ Rising Edge to ECAS Rising Edge in order not to start a Wait State	20			
C25	CLK Rising Edge to CASn High if ECASn low at AREQ Rising Edge (if Delay Programmed by ECAS0)		30		

Mode 1:

No.	Parameter	-25 Min	-25 Max	-33 Min	-33 Max
W11	WAITIN Low to ADS Low to Add Wait State(s) if No Wait State is Programmed	5		5	
W12	ADS Low to DTACK Low 0T from RAS Programmed R2, 3 = '0', R7 = '1'		40		30
W13	ADS falling edge to WAIT Low (CS must be Low)		30		25
W14	ADS Falling Edge to WAIT Low delayed access		35		25
W15	CLK High to DTACK High delayed access		35		25

No.	Parameter	-25 Min	-25 Max	-33 Min	-33 Max
W01	WAITIN Low to CLK Rising Edge to Add Wait State (s) if no Wait State is programmed	5			5
W02	CLK Rising Edge to WAIT Low (CS must be Low)		25		20
W03	CLK Rising Edge to WAIT Low (DTACK High)		30		25
W04	CLK to DTACK Low if no wait state programmed		30		25
W05	CLK High to DTACK Low 0T Programmed		35		25
W1	CLK falling edge to WAIT High		30		25
W2	CLK rising or falling edge to DTACK Low		30		25
W3	AREQ/ALE/ADS to DTACK High		30		25
W5	CLK Rising Edge to WAIT High		30		25
W6	WAITIN Low to Access Start to Add Wait State(s)	5		5	
W7	ALE/ADS High to DTACK High (WAIT Low) during Burst Access (not 0T programmed)		35		25
W8	CAS Low to DTACK Low (WAIT High) during Burst Access (0T programmed)		35		25
W9	ECAS High to DTACK High if 0T programmed)				

Figure 21. Wait State with $\overline{CS}$

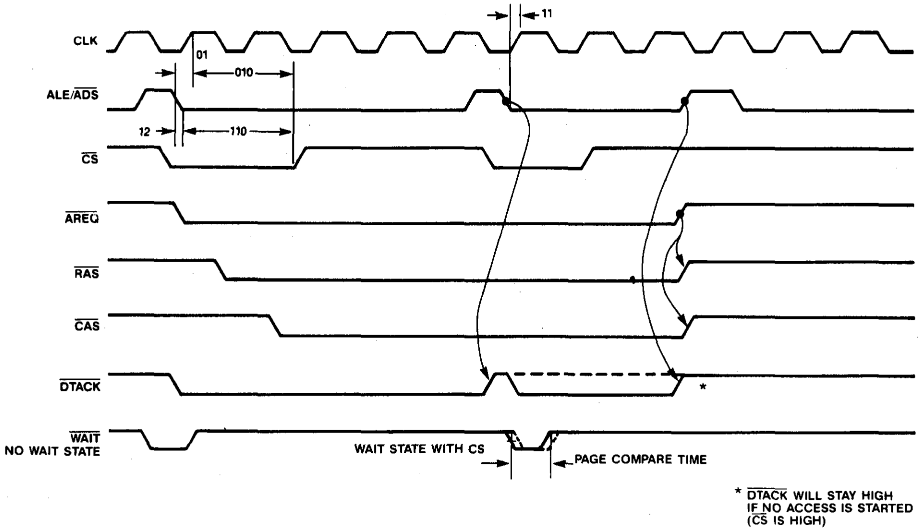
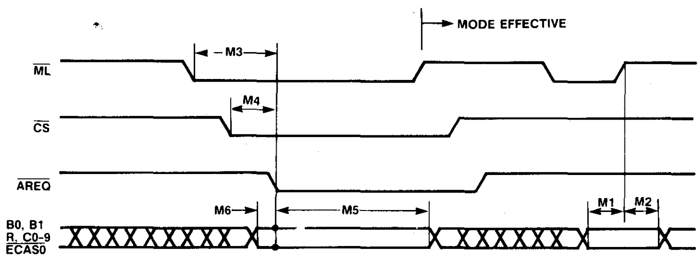


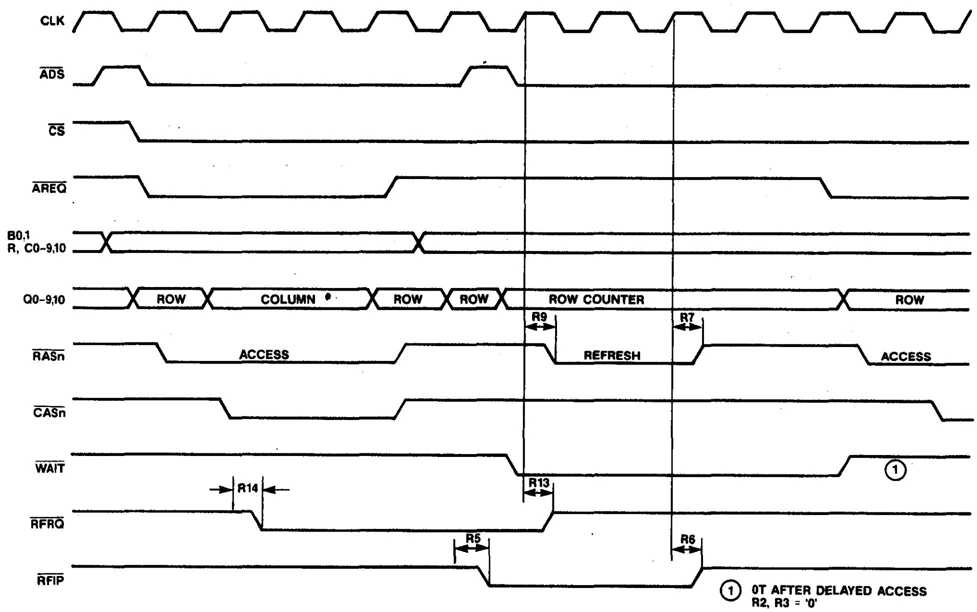
Figure 22. Mode Load



No.	Parameter	-25 Min	-25 Max	-33 Min	-33 Max
M1	Mode Address Set-up Time	5		5	
M2	Mode Address Hold Time	5		5	
M3	$\overline{ML}$ asserted to $\overline{AREQ}$ asserted	10		10	

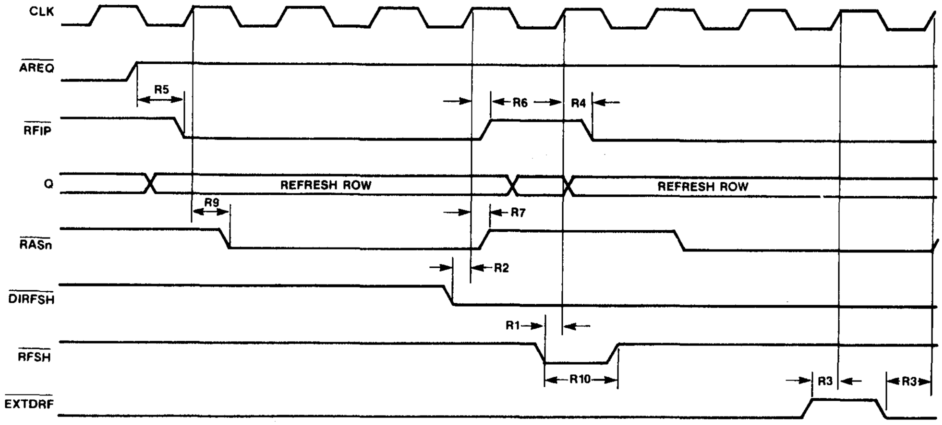
No.	Parameter	-25 Min	-25 Max	-33 Min	-33 Max
M4	$\overline{CS}$ asserted to $\overline{AREQ}$ asserted	5		5	
M5	Mode Address Hold Time from $\overline{AREQ}$ Low	30		30	
M6	Mode Address Set-up Time to $\overline{AREQ}$ Low	0		0	

Figure 23. Internal Refresh — Interleave Access



No.	Parameter	-25 Min	-25 Max	-33 Min	-33 Max
R5	CLK High to RFIP Low		35		35
R6	CLK Rising Edge to RFIP High for Pending Refresh Ending		35		35
R7	CLK Rising Edge to Refresh RAS Ending		30		30
R9	CLK Rising Edge to Refresh RAS Starting		35		35
R13	CLK Rising Edge to RFRQ High		35		35
R14	CLK Rising Edge to RFRQ Low		35		35

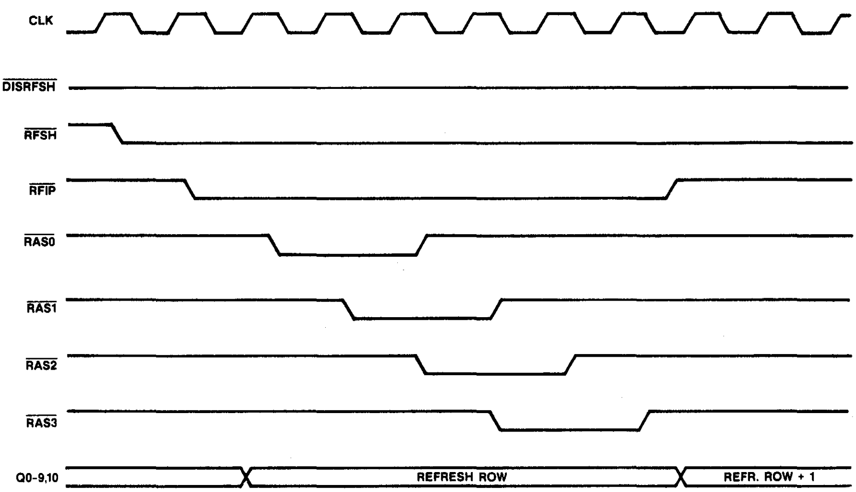
Figure 24. Refresh and Extended Refresh



No.	Parameter	-25		-33	
		Min	Max	Min	Max
R1	RFSH Low Set-up to CLK Rising Edge	5		5	
R2	DISRFSH Low Set-up to CLK Rising Edge	15		15	
R3	EXTDRF Set-up to CLK Rising Edge	12		12	
R4	CLK Rising Edge to RFIP Low		30		30
R5	AREQ High to RFIP Low		35		35

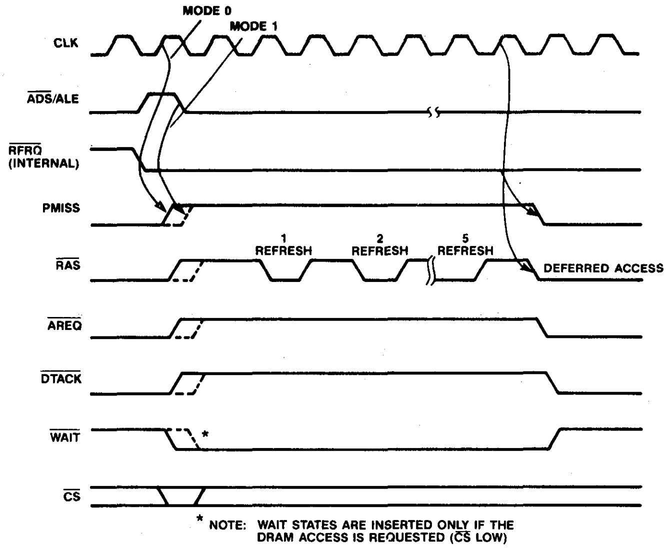
No.	Parameter	-25		-33	
		Min	Max	Min	Max
R6	CLK Rising Edge to RFIP High		35		35
R7	CLK Rising Edge to Refresh RAS Ending		30		30
R9	CLK Rising Edge to Refresh RAS Starting		35		35
R10	RFSH Low Pulse Width	15		15	

Figure 25. Staggered Refresh



3

Figure 26. Page Mode Forced Refresh



APPENDIX

Commonalities and Differences between the KS84C21/22 and the KS84C31/32.

Pin Compatibility

The KS84C31/32 are fully pin for pin compatible with the KS84C21/22.

Functional Compatibility

Besides the differences described below which are all upgrades to the KS84C21/22, there is only one feature that is left off and that is the column increment feature. The EDRC supports access to random pages and random column if page mode is programmed. The column increment counter would be of no great benefit.

Mode Register

The Mode Register is expanded by 3 bits (ECAS1, ECAS2 and ECAS3) to select the 68030 mode, the page mode operation and the Nibble Mode, respectively.

Page Mode

The EDRC supports page access to random columns within a page. If the page of consecutive access cycles is different from each other, the EDRC will set the output PMISS to indicate that there is a page miss. CAS outputs are asserted deasserted by the corresponding ECAS inputs, however, CAS will be delayed from going low in case of a page miss. CAS, RAS and WE will be deasserted when a page miss is detected.

Static Column

The EDRC supports the faster static column access. The address latch will latch the Row address. The column address latch can either be in "fall through" or "latch" mode.

Interleave Mode

Interleaving of memory cycles is possible only in non-page mode operation. Interleaving is also disabled in 68030 and Nibble mode.

68030

The EDRC supports the fast cache fill mode of the 68030. Up to four 32 bit words can be fetched by nibble access cycles. The handshake signals provided by the 68030 are compatible with the corresponding I/O lines provided by the EDRC. These 2 handshake signals CBREQ and CBACK are multiplexed with signals RFRQ (refresh request output) and the EXTDRF (extend refresh input).

Nibble Mode

The EDRC easily interfaces with the 68040 and other controller that can utilize the fast nibble type access.

The CAS outputs are switched in this mode during the burst access cycles by the CLK input. Individual CASs can be disabled by the appropriate ECAS input. A burst lasts four access cycles but can be terminated at any time with the AREQ input going high.

Operating Frequency

The maximum operating frequency is 33 MHz on the CLK input and 20 MHz on the RFCLK input.

Wait State Timing

The assertion of the WAIT(DTACK) output has been changed slightly. A wait state starts always when the access starts which is in mode 0 the rising edge of CLK after ALE goes high and in mode 1 at the falling edge of ADS provided that CS setup time is sufficient.

A wait state starts when an access has been requested that is CS is asserted. In 68030 and Nibble Mode, CS has to be asserted only for the non-burst access.

Column Address Hold Time During Interleaving

The column address hold time is reduced to min 25 ns and the max time is 40 ns. This allows starting a consecutive access earlier with the cycle.

Row Address Hold Time

The Row Address hold time has been reduced to 12 and 20 ns respectively.

PMISS Output: This output has been added to signal that a page miss has been detected. This signal should be fed back to the AREQ input if the page mode option is selected. It also can be used to add wait states during a non-burst or burst access.

Summary of AC Parameters

The leading digit indicates the following area where the specifications refer:

0	Mode 0	N	Nibble Mode
1	Mode 1	P	Page Mode
C	Common	R	Refresh
M	Mode Load	W	Wait

No.	Parameter	-25 Min	-25 Max	-33 Min	-33 Max
01	CS Low to CLK Rising Edge	10		5	
02	ALE High to CLK Rising Edge	15		10	
04	ALE Pulse Width	15		10	
05a	Address Set-up to CLK Rising Edge using the On-Chip Address Latch	10		10	
05b	Address Set-up to CLK Rising Edge not using the On-Chip Address Latch	20		20	
06	Address Set-up to ALE Falling Edge using the On-Chip Address Latch	10		10	
07	CLK Rising Edge to RAS Low		35		30
08	CLK Rising Edge to CAS Low (non-delayed access)				
a	t_{RAH} = 12ns, t_{ASC} = 0ns		85		80
b	t_{RAH} = 12ns, t_{ASC} = 10ns		95		90
c	t_{RAH} = 20ns, t_{ASC} = 0ns		95		90
d	t_{RAH} = 20ns, t_{ASC} = 10ns		105		100
010	CS Low after access start	10		10	
011	WIN low to CLK Rising Edge to delay CAS (C9 = '1')	5		5	
012	Address Hold Time from ALE falling edge using the On-Chip Address Latch	20		15	
11	ADS Low to CLK, to guarantee WAIT DTACK output	25		15	
12	CS to ADS Low Set-up Time	5		5	
13	ADS Falling Edge to RAS Low during an Access		35		35
14a	Address Set-up to ADS Falling Edge using the On-Chip Address Latch	10		10	
14b	Address Set-up to ADS Falling Edge not using the On-Chip Address Latch	10		10	
15	Address Hold after ADS Falling Edge using the On-Chip Address Latch	8		8	

No.	Parameter	-25 Min	-25 Max	-33 Min	-33 Max
16	ADS Low to CAS Low C9 = '0' (not delayed access)				
a	t_{RAH} = 12ns, t_{ASC} = 0ns		85		
b	t_{RAH} = 12ns, t_{ASC} = 10ns		95		
c	t_{RAH} = 20ns, t_{ASC} = 0ns		95		
d	t_{RAH} = 20ns, t_{ASC} = 10ns		105		
19	ADS High Pulse Width	10			
110	CS Low after access start	10			
C2	Address to Q output		35		30
C3	Row Address Hold Time, t_{RAH} = 12ns	12		11	
C4	Row Address Hold Time, t_{RAH} = 20ns	20		20	
C5	Column Address Set-up Time t_{ASC} = 0ns	0		0	
C6	Column Address Set-up Time t_{ASC} = 10ns	10		10	
C7	CLK Rising Edge to RAS active after delayed access		35		30
C8	CLK Rising Edge to CAS active after delayed access				
a	t_{RAH} = 12ns, t_{ASC} = 0ns		85		80
b	t_{RAH} = 12ns, t_{ASC} = 10ns		95		90
c	t_{RAH} = 20ns, t_{ASC} = 0ns		95		90
d	t_{RAH} = 20ns, t_{ASC} = 10ns		105		100
C12	AREQ High to RAS High		35		30
C13	ECASn High to CASn High		25		
	ECASn Low to CASn Low				
C14	WIN to WE		40		33
C17	AREQ High to CAS High		35		30
C18	CLK High	15		13	
C18a	CLK Low	15		13	
C19	CLK Period	40		33	
C20	Column Address Hold Time in Interleave	25	40	25	40
C21	AREQ Rising Edge to ECAS Rising Edge in order not to start a Wait State	20			

		-25		-33	
No.	**Parameter**	**Min**	**Max**	**Min**	**Max**
C22	AREQ High to CLK Rising Edge to recognized as 1T of RAS precharge	15		10	
C24	CLK Rising Edge to CAS Low if delayed by WIN		30		30
C25	CLK Rising Edge to CASn High if ECASn Low at AREQ (if delay programmed by ECAS0)		30		30
C28	RFCLK High	15		15	
C28a	RFCLK Low	15		15	
C29	RFCLK Period	40		40	
M1	Mode Address Set-up Time	5		5	
M2	Mode Address Hold Time	5		5	
M3	ML asserted to AREQ asserted	10		10	
M4	CS asserted to AREQ asserted	5		5	
M5	Mode Address Hold Time from AREQ Low	30		30	
M6	Mode Address Set-up Time to AREQ Low	0		0	
N1	CLK to CAS high	5	20	4	15
N2	CLK to CAS low		20		15
N3	CLK to CBACK low		18		14
N4	CLK to CBACK high		18		14
P01	Burst access start to PMISS low (50pF load)		30		25
P02	ECASn high setup to access start	10		10	
P03	ECASn hold from access start	20		20	
P04	Access start to CAS low if page hit (ECAS hold = 0 ns)	25		25	
P05	PMISS high from access start (50pF load)		15		15
P06	RAS high from access start if page miss		35		30
P1	PMISS low from deferred access start (50pF load)		15		15
P2	ECAS high width	15		15	
P11	Burst access start to PMISS low (50pF load)		30		25

		-25		-33	
No.	**Parameter**	**Min**	**Max**	**Min**	**Max**
P12	ECASn high setup to access start	10		10	
P13	ECASn hold from access start	20		20	
P14	ADS low to CAS low if page hit (ECAS hold = 0 ns)		25		25
P15	PMISS high from access start (50pF load)		15		15
P16	RAS high from access start if page miss		35		30
R1	RFSH Low Set-up to CLK Rising Edge	5		5	
R2	DISRFSH Low Set-up to CLK Rising Edge	15		15	
R3	EXTDRF Set-up to CLK Rising Edge	12		12	
R4	CLK Rising Edge to RFIP Low		30		30
R5	AREQ High to RFIP Low		35		35
R6	CLK Rising Edge to RFIP High		35		35
R7	CLK Rising Edge to Refresh RAS Ending		30		30
R9	CLK Rising Edge to Refresh RAS Starting		35		35
R10	RFSH Low Pulse Width	15		15	
R13	CLK Rising Edge to RFRQ High		35		35
R14	CLK Rising Edge to RFRQ Low		35		35
W01	WAITIN Low to CLK Rising Edge to Add Wait State (s) if no Wait State is programmed	5			5
W02	CLK Rising Edge to WAIT Low (CS must be Low)		25		20
W03	CLK Rising Edge to WAIT Low (DTACK High)		30		25
W04	CLK to DTACK Low if no wait state programmed		30		25
W05	CLK High to DTACK Low 0T Programmed		35		25
W1	CLK falling edge to WAIT High		30		25
W2	CLK rising or falling edge to DTACK Low		30		25
W3	AREQ/ALE/ADS to DTACK High		30		25

No.	Parameter	-25 Min	-25 Max	-33 Min	-33 Max
W4	CLK to $\overline{DTACK}$ High		30		25
W5	CLK Rising Edge to $\overline{WAIT}$ High		30		25
W6	$\overline{WAITIN}$ Low to Access Start to Add Wait State(s)	5		5	
W7	ALE/$\overline{ADS}$ High to $\overline{DTACK}$ High ($\overline{WAIT}$ Low) during Burst Access (not 0T programmed)		35		25
W8	$\overline{CAS}$ low to $\overline{DTACK}$ Low ($\overline{WAIT}$ High) during Burst Access (0T programmed)		35		25
W9	$\overline{ECAS}$ high to $\overline{DTACK}$ high if 0T programmed				

No.	Parameter	-25 Min	-25 Max	-33 Min	-33 Max
W11	$\overline{WAITIN}$ Low to $\overline{ADS}$ Low to Add Wait State(s) if No Wait State is Programmed	5		5	
W12	$\overline{ADS}$ Low to $\overline{DTACK}$ Low 0T from $\overline{RAS}$ Programmed R2, 3 = '0', R7 = '1'		40		30
W13	$\overline{ADS}$ falling edge to $\overline{WAIT}$ Low ($\overline{CS}$ must be Low)		30		25
W14	$\overline{ADS}$ Falling Edge to $\overline{WAIT}$ Low delayed access		35		25
W15	CLK High to $\overline{DTACK}$ High delayed access		35		25

PACKAGE DIMENSIONS

The Samsung KS84CXX DRAM Controllers are available in two packages. The KS84C31 68-Pin PLCC package is shown in Figure 27, while the 84-Pin version is shown in Figure 28.

Figure 27. 68-Pin PLCC Package

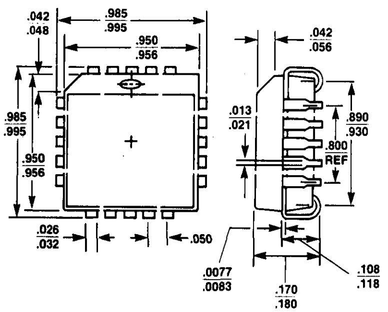
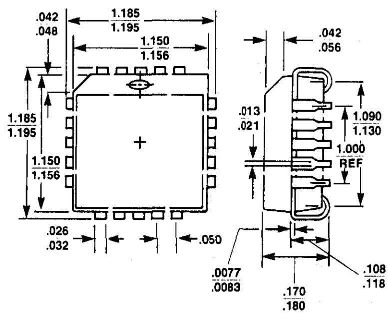


Figure 28. 84-Pin PLCC Package



ORDERING INFORMATION AND PRODUCT CODE

KS 84CXX XX X X

- **KS** — **SAMSUNG SEMICONDUCTOR**
- **84CXX** — **Part Number**
  - 84C31
  - 84C32
- **XX** — **Speed**
  - -33 33MHz
- **X** — **Temperature**
  - C — Commercial (0°C to +70°C)
- **X** — **Packaging**
  - L — Plastic Leaded Chip Carrier (PLCC)

SAMSUNG products are designated by a Product Code. When ordering, please refer to products by their full code. For unusual, and/or specific packaging or processing requirements not covered by the standard product line, please contact the SAMSUNG MOS Product Group.

KS85C30

SERIAL COMMUNICATION CONTROLLER

Preliminary

PRODUCT FEATURES

- 6, 8, and 10 MHz operation
- Low power CMOS
- Pin compatible to NMOS versions
- High speed - 2.5M bit/sec channels
- Two independent, full-duplex channels, each with separate crystal oscillator, baud rate generator and Digital PLL
- Multi-protocol operation, programmable for NRZ, NRZI or FM data encoding
- Asynchronous mode with programmable clock factor
- Synchronous mode with internal or external character synchronization
- Break detection and generation
- Parity, overrun, and framing error detection
- Local loopback and auto echo modes
- Supports T1 digital trunk
- Enhanced DMA support

PRODUCT OVERVIEW

The KS85C30 CMOS Serial Communications Controller (SCC) is an enhanced CMOS version of the industry standard NMOS SCC. It is a dual channel, multi-protocol data communications peripheral that easily interfaces to CPU's with non-multiplexed address/data buses. The programming flexibility of the internal registers allows the SCC to be configured to satisfy a wide variety of serial communication applications. The many on-chip features such as baud rate generators, digital phase locked loops, and crystal oscillators dramatically reduce the need for external logic. Additional features including a 10 X 19-bit status FIFO and 14-bit byte counter were added to support high speed SDLC transers using DMA controllers.

The SCC handles asynchronous formats, synchronous byte-oriented protocols such as IBM Bisync, and synchronous bit-oriented protocols such as HDLC and IBM SDLC. This versatile device supports virtually any serial data transfer application (cassette, diskette, tape drives etc.). The advanced CMOS process offers lower power consumption, higher performance, and superior noise immunity.

The device can generate and check CRC codes in any synchronous mode and can be programmed to check data integrity in various modes. The SCC also has facilities for modem controls in both channels. In applications where these controls are not needed the modem controls can be used for general-purposes I/O. The daisy-chain interrupt hierarchy is also supported.

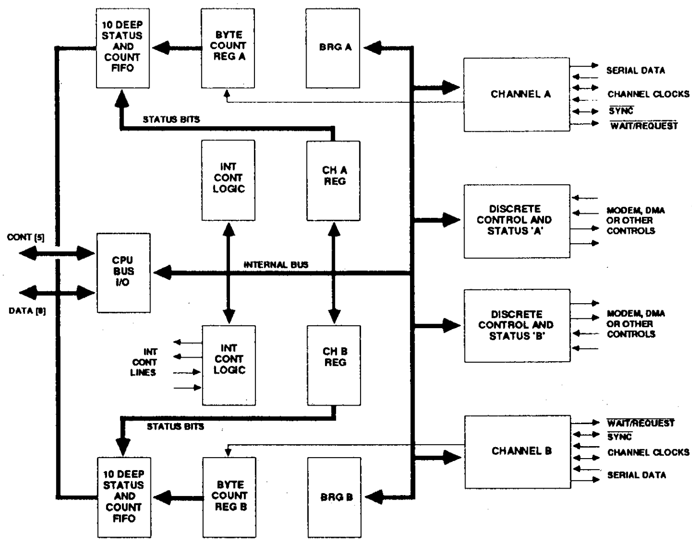


Figure 1 : KS85C30 BLOCK DIAGRAM

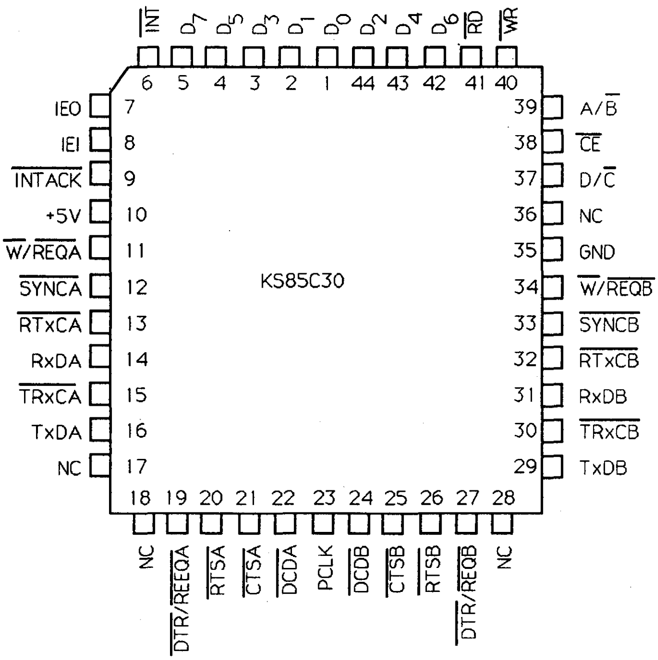


Figure 2a: 44-PIN PLCC CONFIGURATION

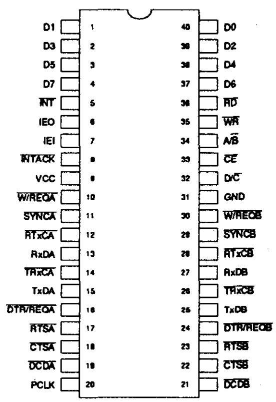


Figure 2b: 40-PIN DIP CONFIGURATION

TABLE 1a: 40-Pin DIP Pin Assignment

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
1	D_1	8	$\overline{\text{INTACK}}$	15	TxDA	22	$\overline{\text{CTSB}}$	29	$\overline{\text{SYNCB}}$	36	$\overline{\text{RD}}$
2	D_3	9	V_{CC}	16	$\overline{\text{DTR/REQA}}$	23	$\overline{\text{RTSB}}$	30	W/REQA	37	D_6
3	D_5	10	$\overline{\text{W/REQA}}$	17	$\overline{\text{RTSA}}$	24	$\overline{\text{DTR/REQB}}$	31	GND	38	D_4
4	D_7	11	$\overline{\text{SYNCA}}$	18	$\overline{\text{CTSA}}$	25	TxDB	32	D/$\overline{\text{C}}$	39	D_2
5	$\overline{\text{INT}}$	12	$\overline{\text{RTxCA}}$	19	$\overline{\text{DCDA}}$	26	$\overline{\text{TRxCB}}$	33	$\overline{\text{CE}}$	40	D_0
6	IEO	13	RxDA	20	PCLK	27	RxDB	34	A/$\overline{\text{B}}$		
7	IEI	14	$\overline{\text{TRxCA}}$	21	$\overline{\text{DCDB}}$	28	$\overline{\text{RTxCB}}$	35	$\overline{\text{WR}}$		

Table 1b: 44-Pin PLCC Pin Assignment

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
1	D_0	9	$\overline{\text{INTACK}}$	17	NC	25	$\overline{\text{CTSB}}$	33	$\overline{\text{SYNCB}}$	41	$\overline{\text{RD}}$
2	D_1	10	+5V	18	NC	2	$\overline{\text{RTSB}}$	34	$\overline{\text{W/REQB}}$	42	D_4
3	D_3	11	$\overline{\text{W/REQA}}$	19	$\overline{\text{DTR/REQA}}$	27	$\overline{\text{DTR/REQB}}$	35	GND	43	D_4
4	D_5	12	$\overline{\text{SYNCA}}$	20	$\overline{\text{RTSA}}$	28	NC	36	NC	44	D_2
5	D_7	13	$\overline{\text{RTxCA}}$	21	$\overline{\text{CTSA}}$	29	TxDB	37	D/$\overline{\text{C}}$		
6	$\overline{\text{INT}}$	14	RxDA	22	$\overline{\text{DCDA}}$	30	$\overline{\text{TRxCB}}$	38	$\overline{\text{CE}}$		
7	IEO	15	$\overline{\text{TRxCA}}$	23	PCLK	31	RxDB	39	A/$\overline{\text{B}}$		
8	IEI	16	TxDA	24	$\overline{\text{DCDB}}$	32	$\overline{\text{RTxCB}}$	40	$\overline{\text{WR}}$		

Table 1 c: PIN DESCRIPTIONS

Symbol	Type	Name and Function
A/$\overline{B}$	I	**Channel A/Channel B :** This signal selects the channel in which the read or write operation occurs.
$\overline{CE}$	I	**Chip Enable:** This signal selects the SCC for a read or write operation.
$\overline{CTSA}$, $\overline{CTSB}$	I	**Clear To Send:** If these pins are programmed as Auto Enables, a Low on the inputs enables the respective transmitters. If not programmed as Auto Enables, they may be used as general-purpose inputs. Both inputs are Schmitt-trigger buffered to accommodate slow rise-time signals. The SCC detects pulses on these pins and can interrupt the CPU on both logic level transitions.
D_0 - D_7	I/O	**Data Bus (3-state):** These lines carry data and commands to and from the SCC.
D/$\overline{C}$	I	**Data/Control Select:** This signal defines the type of information transferred to or from the SCC. A High means data is transferred; a Low indicates a command.
$\overline{DCDA}$, $\overline{DCDB}$	I	**Data Carrier Detect:** These pins function as receiver enables if they are programmed for Auto Enables; otherwise they may be used as general-purpose input pins. Both pins are Schmitt-trigger buffered to accommodate slow rise-time signals. The SCC detects pulses on these pins and can interrupt the CPU on both logic level transitions.
$\overline{DTR}$/$\overline{REQA}$ DTR/REQB	O	**Data Terminal Ready/Request:** These outputs follow the state programmed into the DTR bit. They can also be used as general-purpose outputs or as Request lines for a DMA controller.
IEI	I	**Interrupt Enable In:** IEI is used with IEO to form an interrupt daisy-chain when there is more than one interrupt driven device. A High IEI indicates that no other higher priority device has an interrupt under service or is requesting an interrupt.
IEO	O	**Interrupt Enable Out:** IEO is High only if IEI is High and the CPU is not servicing an SCC interrupt or the SCC is not requesting an interrupt (Interrupt Acknowledge cycle only). IEO is connected to the next lower priority device's IEI input and this inhibits interrupts from lower priority devices.
$\overline{INT}$	O	**Interrupt Request:** This signal is activated when the SCC requests an interrupt.
$\overline{INTACK}$ PCLK	I I	**Interrupt Acknowledge:** This signal indicates an active Interrupt Acknowledge cycle. During this cycle, the SCC interrupt daisy chain settles. When $\overline{RD}$ becomes active, the SCC places an interrupt vector on the data bus (if IEI is High). INTACK is latched by the rising edge of PCLK. **Clock:** This is the master SCC clock used to synchronize internal signals. PCLK is a TTL level signal..PCLK is not required to have any phase relationship with the master system clock.
$\overline{RD}$	I	**Read:** This signal indicates a read operation and when the SCC is selected, enables the SCC's bus drivers. During the Interrupt Acknowledge cycle, this signal gates the interrupt vector onto the bus if the SCC is the highest priority device requesting an interrupt.
$\overline{RTSA}$, $\overline{RTSB}$	O	**Request to Send:** When the Request To Send (RTS) bit in Write Register 5 (Figure 10)is set, the RTS signal goes Low. When the RTS bit is reset in Asynchronous mode and Auto Enable is on, the signal goes High after the transmitter is empty. In Synchronous mode or in Asynchronous mode with Auto Enable off, the RTS pin strictly follows the state of the RTS bit. Both pins can be used as general-purpose outputs.

3

Table 1 c: PIN DESCRIPTIONS con't

Symbol	Type	Name and Function
$\overline{RTxCA}$, $\overline{RTxCB}$	I	**Receive/Transmit Clocks:** These pins can be programmed in several different modes of operation. In each channel $\overline{RTxC}$ may supply the receive clock, the transmit clock, the clock for the baud rate generator, or the clock for the Digital Phase-Locked Loop. These pins can also be programmed for use with the respective $\overline{SYNC}$ pins as a crystal oscillator. The receive clock may be 1, 16, 32, or 64 times the data rate in Asynchronous modes.
RxDA, RxDB	I	**Receive Data:** These inputs signals receive serial data at standard TTL levels.
$\overline{SYNCA}$, $\overline{SYNCB}$	I/O	**Synchronization:** These pins can act either as inputs, outputs, or part of the crystal oscillator circuit. In the Asynchronous Receive mode (crystal oscillator option not selected), these pins are inputs similar to CTS and $\overline{DCD}$. In this mode, transitions on these lines affect the state of the Synchronous/Hunt status bits in Read Register 0 (Figure 9) but have no other function. In external Synchronization mode with the crystal oscillator not selected, these lines also act as inputs. In this mode, $\overline{SYNC}$ must be driven Low two receive clock cycles after the last bit in the synchronous character is received. Character assembly begins on the rising edge of the receive clock immediately preceding the activation of $\overline{SYNC}$. In the Internal Synchronization mode (Monosync and Bisync) with the crystal oscillator not selected, these pins act as outputs and are active only during the part of the receive clock cycle in which synchronous characters are recognized. The synchronous condition is not latched, so these outputs are active each time a synchronization pattern is recognized (regardless of character boundaries). In SDLC mode, these pins act as outputs and are valid on receipt of a flag.
$\overline{TRxCA}$, $\overline{TRxCB}$	I/O	**Transmit/Receive Clocks:** These pins can be programmed in several different modes of operation. TRxC may supply the receive clock or the transmit clock in the input mode or supply the output of the Digital Phase-Locked Loop, the crystal oscillator, the baud rate generator, or the transmit clock in the output mode.
TxDA, TxDB	O	**Transmit Data:** These output signals transmit serial data at standard TTL levels.
V_{DD}		**Power:** 5V ± 5% DC Supply
V_{SS}		**Ground:** 0V
$\overline{WR}$	I	**Write:** When the SCC is selected, this signal indicates a write operation. The coincidence of $\overline{RD}$ and $\overline{WR}$ is interpreted as a reset.
$\overline{W/REQA}$ W/REQB	O	**Wait/Request:** Open-drain when programmed for a Wait function, driven High or Low when programmed for a Request function. These dual-purpose outputs may be programmed as Request lines for a DMA controller or as Wait lines to synchronize the CPU to the SCC data rate. The reset state is Wait.

OPERATIONAL DESCRIPTION

The functional capabilities of the SCC can be described from two different points of view; as a data communications device, it transmits and receives data in a wide variety of data communications protocols; as a microprocessor peripheral, the SCC offers valuable features such as vectored interrupts, polling, and simple handshake capability.

Data Communications Capabilities

The SCC provides two independent full-duplex channels programmable for use in any common Asynchronous or Synchronous data communication protocol. Figure 3 and the following description briefly detail these protocols.

Asynchronous Modes

Transmission and reception can be accomplished independently on each channel with five to eight bits per character, plus optional even or odd parity. The transmitters can supply one, one-and-one-half, or two stop bits per character and can provide a break output at any time. The receiver break-detection logic interrupts the CPU both at the start and at the end of a received break. Reception is protected from spikes by transient spike-rejection mechanism that checks the signal one-half a bit time after Low level is detected on the receive data input. If the Low does not persist (as in the case of transient), the character assembly process does not start.

Framing errors and overrun errors are detected and buffered together with partial character on which they occur. Vectored interrupts allow fast servicing or error conditions using dedicated routines. Furthermore, a built-in checking process avoids the interpretation of a framing error as a new start bit: a framing error results in the addition of one-half a bit time to the point at which the search for the next start bit begins.

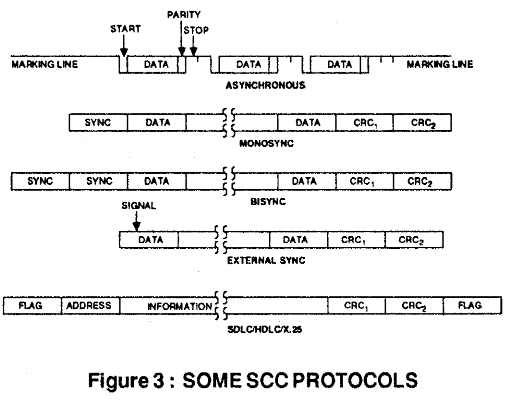


Figure 3 : SOME SCC PROTOCOLS

The SCC does not require symmetric transmit and receive clock signals, thus allowing use of a wide variety of clock sources. The transmitter and receiver can handle data at a rate of 1, 1/16, 1/32, or 1/64 of the clock inputs. In Asynchronous modes, SYNC may be programmed as an input used for functions such as monitoring a ring indicator.

Synchronous Modes

The SCC supports both byte-oriented and bit-oriented synchronous communication. Synchronous byte-oriented protocols can be handled in several modes, allowing character synchronization with a 6-bit or 8-bit synchronous character (Monosync), any 12-bit synchronization pattern (Bisync), or with an external synchronous signal. Leading sync characters can be removed without interrupting the CPU.

Five- or 7-bit synchronous characters are detected with 8- or 16-bit patterns in the SCC by overlapping the larger pattern across multiple incoming synchronous characters as shown in Figure 4.

CRC checking for Synchronous byte-oriented modes is delayed by one character time so that the CPU may disable CRC checking on specific characters. This permits the implementation of protocols such as IBM Bysinc.

Both CRC-16 ($X^{16} + X^{15} + X^2 + 1$) and CCITT ($X^{16} + X^{12} + X^5 + 1$) error checking polynomials are supported. Either polynomial may be selected in all Synchronous modes. Users may preset the CRC generator and checker to all 1s or all 0s. The SCC also provides a feature that automatically transmits CRC data when no other data is available for transmission. This allows for high speed transmissions under DMA control, with no need for CPU intervention at the end of a message. When there is no data or CRC to send in Synchronous modes, the transmitter inserts 6-, 8-, or 16-bit synchronous characters, regardless of the programmed character length.

The SCC supports Synchronous bit-oriented protocols, such as SDLC and HDLC, by performing automatic flag sending, zero insertion, and CRC generation. A special command can be used to abort a frame in transmission. At the end of a message, the SCC automatically transmits the CRC and trailing flag when the transmitter underruns. The transmitter may also be programmed to send an idle line consisting of continuous flag characters or a steady marking condition.

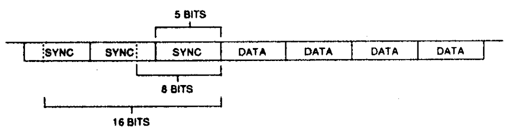


Figure 4 : DETECTING 5- OR 7-BIT SYNCHRONOUS CHARACTERS

If a transmit under run occurs in the middle of a message, as external/status interrupt warns the CPU of this status change so that an abort may be issued. The SCC may also be programmed to send an abort itself in case of an underrun, relieving the CPU of this task. One to eight bits per character can be sent, allowing reception of a message with no prior information about the character structure in the information field of a frame.

The receiver automatically acquires synchronization on the leading flag of a frame in SDLC or HDLC and provides a synchronization signal on the SYNC pin (an interrupt can also be programmed). The receiver can be programmed to search for frames addressed by a single byte (or four bits within a byte) of a user-selected address or to a global broadcast address. In this mode, frames not matching either the user-selected or broadcast address are ignored. The number of address bytes can be extended under software control. For receiving data, an interrupt on the first received character, or an interrupt on every character, or on special condition only (end-of-frame) can be selected. The receiver automatically deletes all 0s inserted by the transmitter during character assembly. CRC is also calculated and is automatically checked to validate frame transmission. At the end of transmission, the status of a received frame is available in the status registers. In SDLC mode, the SCC must be programmed to use the SDLC CRC polynomial, but the generator and checker may be preset to all 1s or all 0s. The CRC is inverted before transmission and the receiver checks against the bit pattern 0001110100001111.

NRZ, NRZI or FM coding may be used in any 1x mode. The parity options available in Asynchronous modes are available in Synchronous modes.

The SCC can be conveniently used under DMA control to provide high speed reception or transmission. In reception, for example the SCC can interrupt the CPU when the first character of a message is received. The CPU then enables the DMA to transfer the message to memory. The SCC then issues an end-of-frame interrupt and the CPU can check the status of the received message. Thus, the CPU is freed for other service while the message is being received. The CPU may also enable the DMA first and have the SCC interrupt only on end-of-frame. This procedure allows all data to be transferred via the DMA.

SDLC Loop Mode

The SCC supports SDLC Loop mode in addition to normal SDLC. In an SDLC Loop, there is a primary controller station that manages the message traffic flow on the loop and any number of secondary stations. In SDLC Loop mode, the SCC performs the functions of a secondary station while an SCC operating in regular SDLC mode can act as a controller (Figure 5).

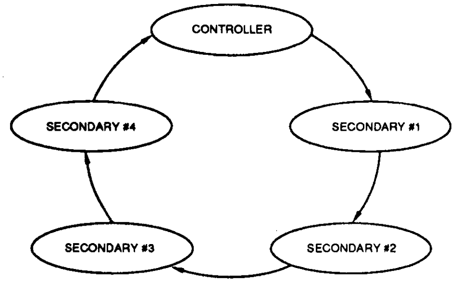


Figure 5 : AN SDLC LOOP

A secondary station in an SDLC Loop is always listening to the messages being sent around the loop, and in fact must pass these messages to the rest of the loop by re-transmitting them with one-bit-time delay. The secondary station can place its own message on the loop only at specific times. The controller signals that secondary stations may transmit messages by sending a special character, called an EOP (End of Poll), around the loop. The EOP character is the bit pattern 11111110. Because of zero insertion during messages, this bit pattern is unique and easily recognized.

When a secondary station has a message to transmit and recognizes an EOP on the line, it changes the last binary 1 of the EOP to a 0 before transmission. This has the effect of turning the EOP into a flag sequence. The secondary station now places its message on the loop and terminates the message with an EOP. Any secondary stations further down the loop with messages to transmit can then append their messages to the message of the first secondary station by the same process. Any secondary stations without messages to send merely echo the incoming messages and are prohibited from placing message son the loop (except upon recognizing an EOP).

SDLC Loop mode is a programmable option in the SCC. NRZ, NRZI, and FM coding may all be used in SDLC Loop mode.

Baud Rate Generator

Each channel in the SCC contains a programmable baud rate generator. Each generator consists of two 8-bit time constant registers that form a 16-bit time constant, a 16-bit down counter, and a flip-flop on the output producing a square wave. On startup, the flip-flop on the output is set in a High state, the value in the time constant register is loaded into the counter, and the counter starts counting down. The output of the baud rate generator toggle upon reaching 0, the value in the time constant register is loaded into the counter, and the process is repeated. The time constant may be changed at any time, but the new value does not take effect until the next load of the counter.

The output of the baud rate generator may be used as either the transmit clock, the receive clock, or both. It can also drive the Digital Phase-Locked Loop (see next section).

If the receive clock or transmit clock is not programmed to come from the TRxC pin, the output of the baud rate generator may be echoed out via the TRxC pin.

The following formula relates the time constant to the baud rate where PCLK or RTxC is the baud rate generator input frequency in Hz. The clock mode is 1, 16, 32, or 64 as selected in Write Register 4, bits D6 and D7. Synchronous operation modes should select 1 and Asynchronous should select 16, 32, or 64.

$$\text{Time Constant} = \frac{\text{PCLK or RTxC Frequency}}{2(\text{Baud Rate})(\text{Clock Mode})} - 2$$

Digital Phase-Locked Loop

The SCC contains a Digital Phase-Locked Loop (DPLL) to recover clock information from a data stream with NRZI or FM encoding. The DPLL is driven by a clock that is nominally 32 (NRZI) or 16 (FM) times the data rate. The DPLL uses this clock, along with the data stream, to construct a clock for the data. This clock may then be used as the SCC receive clock, the transmit clock, or both.

For NRZI encoding, the DPLL counts the 32x clock to create nominal bit times. As the 32x clock is counted, the DPLL is searching the incoming data stream for edges (either 1 to 0 or 0 to 1). Whenever an edge is detected, the DPLL makes a count adjustment (during the next counting cycle), producing a terminal count closer to the center of the bit cell.

For FM encoding, the DPLL still counts from 0 to 31, but with a cycle corresponding to two bit times. When the DPLL is locked, the clock edges in the data stream should occur between counts 15 and 16 and between counts 31 and 0. The DPLL looks for edges only during a time centred on the 15 and 16 counting transition.

The 32x clock for the DPLL can be programmed to come from either the RTxC input or the output of the baud rate generator. The DPLL output may be programmed to be echoed out of the SCC via the TRxC pin (if this pin is not being used as an input).

Data Encoding

The SCC may be programmed to encode and decode the serial data in four different ways (Figure 6). In NRZ encoding, a 1 is represented by a High level and a 0 is represented by a Low level. In NRZI encoding, a 1 is represented by no change in level and a 0 is represented by a change in level. In FM1 (more properly, bi-phase mark), a transition occurs at the beginning of every bit cell. A 1 is represented by an additional transition at the center of the bit cell and a 0 is represented by no additional transition at the center of the bit cell. In FM0 (bi-phase space), a transition occurs at the beginning a every bit cell. A 0 is represented by an additional transition at the center of the bit cell, and a 1 is represented by no additional transition at the center of the bit cell. In addition to these four methods, the SCC can be used to decode Manchester (bi-phase level) data by using the DPLL in the FM mode and programming the receiver for NRZ data. Manchester encoding always produces a transition at the center of the bit cell. If the transition is 0 to 1, the bit is a 0. If the transition is 1 to 0, the bit is a 1.

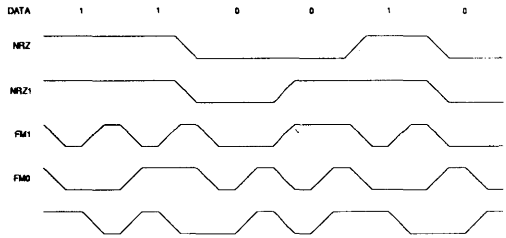


Figure 6 : DATA ENCODING METHODS

Auto Echo and Local Loopback

The SCC is capable of automatically echoing everything it receives. This feature is useful mainly in Asynchronous modes, but works in Synchronous and SDLC modes as well. In Auto Echo mode, TxD is RxD. Auto Echo mode can be used with NRZI or FM encoding with no additional delay, because the data stream is not decoded before re-transmission. In Auto Echo mode, the CTS input is ignored as a transmitter enable (although transitions on this input can still cause interrupts if programmed to do so). In this mode, the transmitter is actually bypassed and the programmer is responsible for disabling transmitter interrupts and WAIT/REQUEST on transmit.

The SCC is also capable of local loopback. In this mode TxD is RxD, just as in Auto Echo mode. However, in Local Loopback mode, the internal transmit data is tied to the internal receive data and RxD is ignored (except to be echoed out via TxD). The CTS and DCD inputs are also ignored as transmit and receive enables. However, transitions on these inputs can still cause interrupts. Local Loopback works in Asynchronous, Synchronous and SDLC modes with NRZ, NRZI or FM coding of the data stream.

I/O Peripheral Interface Capabilities

The SCC offers the choice of Polling, Interrupt (vectored or nonvectored), and Block Transfer modes to transfer data, status, and control information to and from the CPU. The Block Transfer mode can be implemented under CPU or DMA control.

Polling

All interrupts are disabled. Three status registers in the SCC are automatically updated whenever any function is performed. For example, end-of-frame in DSLC mode sets a bit in one of these status registers. The idea behind polling is for the CPU to periodically read a status register until the register contents indicate the need for date to be transferred. Only one register needs to be read; depending on its contents, the CPU either writes data, reads data, or continues. Two bits in the register indicate the need for data transfer. An alternative is a poll of the Interrupt Pending register to determine the source of an interrupt. The status for both channels resides in one register.

Interrupts

When an SCC responds to an Interrupt Acknowledge signal (INTACK) from the CPU, an interrupt vector may be placed on the data bus. This vector is written in WR2 and may be read in RR2A or RR2B (Figures 9 and 10).

To speed interrupt response time, the SCC can modify three bits in this vector to indicate status. If the vector is read in Channel A, status is never included; if it is read in Channel B, status is always included.

Each of the six sources of interrupts in the SCC (Transmit, Receive, and External/Status interrupts in both channels) has three bits associated with the interrupt source: Interrupt Pending (IP), Interrupt Under Service (IUS), and Interrupt Enable (IE). Operation the IE bit is straightforward. If the IE bit is set for a given interrupt source, then that source can request interrupts. The exception is when the MIE (Master Interrupt Enable) bit in WR9 is reset and no interrupts may be requested. The IE bits are write only.

The other two bits are related to the interrupt priority chain (Figure 7). As a microprocessor peripheral, the SCC may request an interrupt only when no higher priority device is requesting one, e.g., when IEI is High. If the device in question requests an interrupt, it pulls down INT. The CPU then responds with INTACK, and the interrupting device places the vector on the data bus.

In the SCC, the IP bit signals a need for interrupt servicing. When an IP bit is 1 and the IEI input is High, the INT output is pulled Low, requesting an interrupt. In the SCC, if the IE bit is not set by enabling interrupts, then the IP for that source can never be set. The IP bits are readable in RR3A.

The IUS bits signal that an interrupt request is being serviced. If an IUS is set, all interrupt sources of lower priority in the SCC and external to the SCC are prevented from requesting interrupts. The internal interrupt sources are inhibited by the state of the internal daisy chain, while lower priority devices are inhibited by the IEO output of the SCC being pulled Low and propagated to subsequent peripherals. An IUS bit is set during an Interrupt Acknowledge cycle if there are no higher priority devices requesting interrupts.

There are three types of interrupts: Transmit, Receive, and External/Status. Each interrupt type is enabled under program control with Channel A having higher priority than Channel B, and with Receiver, Transmit and External/Status interrupts prioritized in that order within each channel. When the Transmit interrupt is enable, the CPU is interrupted when the transmit buffer becomes empty. (This implies that the transmitter must have had a data character written into it so that it can become empty.) When enabled, the received can interrupt the CPU in one of three ways:

- Interrupt on First Receive Character or Special Receive Condition.
- Interrupt on All Receive Characters or Special Receive Condition.
- Interrupt on Special Receive Condition Only.

Interrupt on First Character or Special Condition and Interrupt on Special Condition Only are typically used with the Block Transfer mode. A Special Receive Condition is one of the following: receiver overrun, framing error in Asynchronous mode, end-of-frame in SDLC mode and, optionally, a parity error. The Special Receive Condition interrupt is different from an ordinary receive character

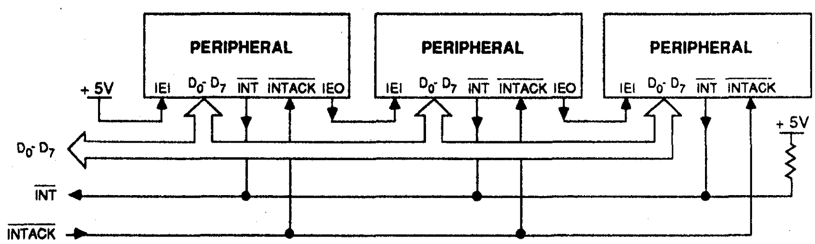


Figure 7 : INTERRUPT SCHEDULE

available interrupt only in the status placed in the vector during the Interrupt Acknowledge cycle. In (Interrupt on First Receive Character, an interrupt can occur from Special Receive Conditions any time after the first receive character interrupt.

The main function of the External/Status interrupt is to monitor the signal transitions of the CTs, DCD, and SYNC pins; however, an External/Status interrupt is also caused by a Transmit Underrun condition, or a zero count in the baud rate generator, or by the detection of a Break (Asynchronous mode), Abort (SDLC mode) or EOP (SDLC Loop mode) sequence in the data stream. The interrupt caused by the Abort or EOP has a special feature allowing the SCC to interrupt when the Abort or EOP sequence is detected or terminated. This feature facilitates the proper termination of the current message, correct initialization of the next message, and the accurate timing of the Abort condition in external logic in SDLC mode. In SDLC Loop mode, this feature allows secondary stations to recognize the wishes of the primary station to regain control of the loop during a poll sequence.

CPU/DMA Block Transfer

The SCC provides a Block Transfer mode to accommodate CPU block transfer functions and DMA controllers. The Block Transfer mode uses the WAIT/REQUEST output in conjunction with the Wait/Request bits in WR1. The WAIT/REQUEST output can be defined under software control as a WAIT line in the CPU Block Transfer mode or as a REQUEST line in the DMA Block Transfer mode.

To a DMA controller, the SCC $\overline{\text{REQUEST}}$ output indicates that the SCC is not ready to transfer data to or from memory. To the CPU, the WAIT line indicates that the SCC is not ready to transfer data, thereby requesting that the CPU extend the I/O cycle. The $\overline{\text{DTR}}/\overline{\text{REQUEST}}$ line allows full-duplex operation under DMA control.

ARCHITECTURE

The SCC internal structure includes two full-duplex channels, two baud rate generators, internal control and interrupt logic, and a bus interface to a nonmultiplexed bus. Associated with each channel are a number of read and write registers for mode control and status information, as well as logic necessary to interface to modems or other external devices (Figure 1).

The logic for both channels provides formats, synchronization, and validation for data transferred to and from the channel interface. The modem control inputs are monitored by the control logic under program control. All of the modem control signals are general-purpose in nature and can optionally but used for functions other than modem control.

The register set for each channel includes ten control (write) registers, two sync-character (write) registers, and four status (read) registers. In addition, each baud rate generator has two (read/write) registers for holding the time constant that determines the baud rate. Finally, associated with the interrupt logic is a write register for the interrupt vector accessible through either channel, a write only Master Interrupt Control register and three read registers: one containing the vector with status information (Channel B only), one containing the vector without status (Channel A only), and one containing the Interrupt Pending bits (Channel A only).

The registers for each channel are designated as follows:

WRO-WR15 — Write Registers 0 through 15.

RR0-RR3, RR10, RR12, RR15 — Read Registers 0 through 3, 10, 12, 13, 15.

Table 9 lists the functions assigned to each read or write register. The SCC contains only one WR2 and WR9, but they can be accessed by either channel. All other registers are paired (one for each channel).

Data Path

The transmit and receive data path illustrated in (Figure 8) is identical for both channels. The receiver has three 80-bit buffer registers in a FIFO arrangement, in addition to the 8-bit receive shift register. This scheme creates additional time for the CPU to service an interrupt at the beginning of a block of high speed data. Incoming data is routed through one of several paths (data or CRC) depending on the selected mode (the character length in Asynchronous modes also determines the data path).

The transmitter has an 8-bit Transmit Data buffer register loaded from the internal data bus and a 20 bit Transmit Shift register than can be loaded either from the synchronous character registers or from the Transmit Data register. Depending on the operational mode, outgoing data is routed through one of four main paths before it is transmitted from the Transmit Data output (TxD).

Table 2 : READ AND WRITE REGISTER FUNCTIONS

Register	Function
Read	
RR0	Transmit/Receive buffer status and External status
RR1	Special Receive Condition status
RR2	Modified Interrupt vector (Channel B only) Unmodified Interrupt vector (Channel A only)
RR3	Interrupt Pending bits (Channel A only)
RR8	Receive Buffer
RR10	Miscellaneous status
RR12	Lower byte of baud rate generator time constant
RR13	Upper byte of baud rate generator time constant
RR15	External/Status Interrupt information
Write	
WR0	CRC initialize, initialization commands for the various modes, Register Pointers
WR1	Transmit/Receive interrupt and data transfer mode definition
WR2	Interrupt vector (accessed through either channel)
WR3	Receive parameters and control
WR4	Transmit/Receive miscellaneous parameters and modes
WR5	Transmit parameters and controls
WR6	Sync characters or SDLC address field
WR7	Sync characters or SDLC flag
WR8	Transmit buffer
WR9	Master interrupt control and reset (accessed through either channel)
WR10	Miscellaneous transmitter/receiver control bits
WR11	Clock mode control
WR12	Lower byte of baud rate generator time constant
WR13	Upper byte of baud rate generator time constant
WR14	Miscellaneous control bits
WR15	External/Status interrupt control

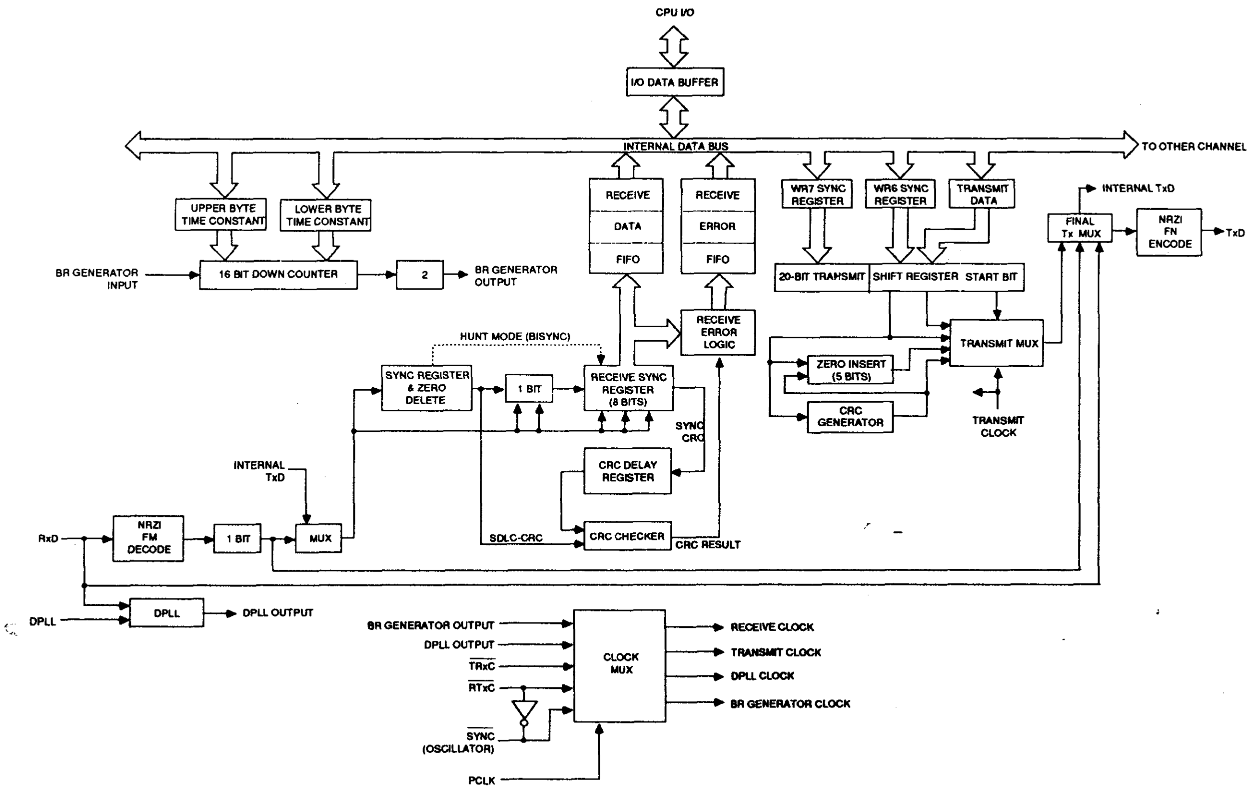


Figure 8 : DATA PATH

PROGRAMMING

The SCC contains write registers in each channel that are programmed by the system separately to configure the functional personality of the channels.

In the SCC, register addressing is direct for the data registers only, which are selected by a High on the D/C pin. In all other cases (with the exception of WR0 and RR0)), programming the write registers requires two write operations and reading the read registers requires both a write and read operation. The first write is to WR0 and contains three bits that point to the selected register. The second write is the actual control word for the selected register, and if the second operation is read, the selected read register is accessed.

All of the registers in the SCC, including the data registers, may be accessed in this fashion. The pointer bits are automatically cleared after the read or write operation so that WR0 (or RR0) is addressed again.

The system program first issues a series of commands to initialize the basic mode of operation. This is followed by other commands to qualify conditions within the selected mode. For example, the Asynchronous mode, character length, clock rate, number of stop bits, even or odd parity might be set first. Then the interrupt mode would be set, and finally, receiver or transmitter enable.

Read Registers

The SCC contains eight read registers (actually nine, counting the receive buffer (RR8) in each channel). Four of these may be read to obtain status information (RR0, RR1, and RR15). Two registers (RR12 and RR13) may be read to learn the baud rate generator time constant. RR2 contains either the unmodified interrupt vector (Channel A) or the vector modified by status information (Channel B). RR3 contains the Interrupt Pending (IP) bits (Channel A). Figure 9 shows the formats for each read register.

The status bits of RR0 and RR1 are grouped to simplify status monitoring; e.g., when the interrupt vector indicates a Special Receive Condition interrupt, all the appropriate error bits can be read from a single register (RR1)

READ REGISTER 0

Bit	Function
D_0	Rx CHARACTER AVAILABLE
D_1	ZERO COUNT
D_2	Tx BUFFER EMPTY
D_3	DCD
D_4	SYNC/HUNT
D_5	CTS
D_6	Tx UNDERRUN/EOM
D_7	BREAK/ABORT

READ REGISTER 10

Bit	Function
D_0	0
D_1	ON LOOP
D_2	0
D_3	0
D_4	LOOP SENDING
D_5	0
D_6	TWO CLOCKS MISSING
D_7	ONE CLOCK MISSING

READ REGISTER 1

Bit	Function
D_0	ALL SENT
D_1	RESIDUE CODE 2
D_2	RESIDUE CODE 1
D_3	RESIDUE CODE 0
D_4	PARITY ERROR
D_5	Rx OVERRUN ERROR
D_6	CRC/FRAMING ERROR
D_7	END OF FRAME (SDLC)

READ REGISTER 12

Bit	Function
D_0	TC_0
D_1	TC_1
D_2	TC_2
D_3	TC_3
D_4	TC_4
D_5	TC_5
D_6	TC_6
D_7	TC_7

TC_0–TC_7: LOWER BYTE OF TIME CONSTANT

READ REGISTER 2

Bit	Function
D_0	V_0
D_1	V_1
D_2	V_2
D_3	V_3
D_4	V_4
D_5	V_5
D_6	V_6
D_7	V_7

V_0–V_7: INTERUPT VECTOR*

*Modified in B channel

READ REGISTER 13

Bit	Function
D_0	TC_8
D_1	TC_9
D_2	TC_{10}
D_3	TC_{11}
D_4	TC_{12}
D_5	TC_{13}
D_6	TC_{14}
D_7	TC_{15}

TC_8–TC_{15}: UPPER BYTE OF TIME CONSTANT

READ REGISTER 3

Bit	Function
D_0	CHANNEL B EXT/STAT IP*
D_1	CHANNEL B Tx IP*
D_2	CHANNEL B Rx IP*
D_3	CHANNEL A EXT/STAT IP*
D_4	CHANNEL A Tx IP*
D_5	CHANNEL A Rx IP*
D_6	0
D_7	0

*Always 0 in B channel

READ REGISTER 15

Bit	Function
D_0	0
D_1	ZERO COUNT IE
D_2	0
D_3	DCD IE
D_4	SYNC/HUNT IE
D_5	CTS IE
D_6	Tx UNDERRUN/EOM IE
D_7	BREAK/ABORT IE

Figure 9 : READ REGISTER BIT FUNCTIONS

Write Registers

The SCC contains 13 write registers (14 counting WR8, the transmit buffer) in each channel. These write registers are programmed separately to configure the functional "personality" of the channels. In addition, there are two registers (WR2 and WR9) shared by the two channels that may be accessed through either of them. WR2 contains the interrupt vector for both channels, while WR9 contains the interrupt control bits. Figure 10 shows the format of each write register.

WRITE REGISTER 0

D_2	D_1	D_0	
0	0	0	REGISTER 0
0	0	1	REGISTER 1
0	1	0	REGISTER 2
0	1	1	REGISTER 3
1	0	0	REGISTER 4
1	0	1	REGISTER 5
1	1	0	REGISTER 6
1	1	1	REGISTER 7
0	0	0	REGISTER 8 (WITH POINT HIGH COMMAND)
0	0	1	REGISTER 9 (WITH POINT HIGH COMMAND)
0	1	0	REGISTER 10 (WITH POINT HIGH COMMAND)
0	1	1	REGISTER 11 (WITH POINT HIGH COMMAND)
1	0	0	REGISTER 12 (WITH POINT HIGH COMMAND)
1	0	1	REGISTER 13 (WITH POINT HIGH COMMAND)
1	1	0	REGISTER 14 (WITH POINT HIGH COMMAND)
1	1	1	REGISTER 15 (WITH POINT HIGH COMMAND)

D_5	D_4	D_3	
0	0	0	NULL CODE
0	0	1	POINT HIGH
0	1	0	RESET EXT/STAT INTERRUPTS
0	1	1	SEND ABORT (SDLC)
1	0	0	ENABLE INT ON NEXT Rx CHARACTER
1	0	1	RESET TxINT PENDING
1	1	0	ERROR RESET
1	1	1	RESET HIGHEST IUS

D_7	D_6	
0	0	NULL CODE
0	1	RESET Rx CRC CHECKER
1	0	RESET Tx CRC GENERATOR
1	1	RESET Tx UNDERRUN/EOM LATCH

WRITE REGISTER 1

Bit	Function
D_0	EXT INT ENABLE
D_1	Tx INT ENABLE
D_2	PARITY IS SPECIAL CONDITION
D_5	WAIT/DMA REQUEST ON RECEIVE/TRANSMIT
D_6	WAIT/DMA REQUEST FUNCTION
D_7	WAIT/DMA REQUEST ENABLE

D_4	D_3	
0	0	Rx INT DISABLE
0	1	Rx INT ON FIRST CHARACTER OR SPECIAL CONDITION
1	0	INT ON ALL Rx CHARACTERS OR SPECIAL CONDITION
1	1	Rx INT ON SPECIAL CONDITION ONLY

WRITE REGISTER 2

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
V_7	V_6	V_5	V_4	V_3	V_2	V_1	V_0

V_0–V_7: INTERRUPT VECTOR

WRITE REGISTER 3

Bit	Function
D_0	Rx ENABLE
D_1	SYNC CHARACTER LOAD INHIBIT
D_2	ADDRESS SEARCH MODE (SDLC)
D_3	Rx CRC ENABLE
D_4	ENTER HUNT MODE
D_5	AUTO ENABLES

D_7	D_6	
0	0	Rx 5 BITS/CHARACTER
0	1	Rx 7 BITS/CHARACTER
1	0	Rx 6 BITS/CHARACTER
1	1	Rx 8 BITS/CHARACTER

WRITE REGISTER 4

Bit	Function
D_0	PARITY ENABLE
D_1	PARITY EVEN/ODD

D_3	D_2	
0	0	SYNC MODES ENABLE
0	1	1 STOP BIT/CHARACTER
1	0	1½ STOP BITS/CHARACTER
1	1	2 STOP BITS/CHARACTER

D_5	D_4	
0	0	8 BIT SYNC CHARACTER
0	1	16 BIT SYNC CHARACTER
1	0	SDLC MODE (01111110 FLAG)
1	1	EXTERNAL SYNC MODE

D_7	D_6	
0	0	X1 CLOCK MODE
0	1	X 16 CLOCK MODE
1	0	X32 CLOCK MODE
1	1	X64 CLOCK MODE

WRITE REGISTER 5

Bit	Function
D_0	Tx CRC ENABLE
D_1	RTS
D_2	SDLC/CRC-16
D_3	Tx ENABLE
D_4	SEND BREAK
D_7	DTR

D_6	D_5	
0	0	Tx 5 BITS (OR LESS)/CHARACTER
0	1	Tx 7 BITS/CHARACTER
1	0	Tx 6 BITS/CHARACTER
1	1	Tx 8 BITS/CHARACTER

WRITE REGISTER 6

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
$SYNC_7$	$SYNC_6$	$SYNC_5$	$SYNC_4$	$SYNC_3$	$SYNC_2$	$SYNC_1$	$SYNC_0$	MONOSYNC, 8 BITS
$SYNC_1$	$SYNC_0$	$SYNC_5$	$SYNC_4$	$SYNC_3$	$SYNC_2$	$SYNC_1$	$SYNC_0$	MONOSYNC, 6 BITS
$SYNC_7$	$SYNC_6$	$SYNC_5$	$SYNC_4$	$SYNC_3$	$SYNC_2$	$SYNC_1$	$SYNC_0$	BISYNC, 16 BITS
$SYNC_3$	$SYNC_2$	$SYNC_1$	$SYNC_0$	1	1	1	1	BISYNC, 12 BITS
ADR_7	ADR_6	ADR_5	ADR_4	ADR_3	ADR_2	ADR_1	ADR_0	SDLC
ADR_7	ADR_6	ADR_5	ADR_4	X	X	X	X	SDLC (ADDRESS RANGE)

Figure 10 : WRITE REGISTER BIT FUNCTIONS

3

WRITE REGISTER 7

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
$SYNC_7$	$SYNC_6$	$SYNC_5$	$SYNC_4$	$SYNC_3$	$SYNC_2$	$SYNC_1$	$SYNC_0$	MONOSYNC, 8 BITS
$SYNC_5$	$SYNC_4$	$SYNC_3$	$SYNC_2$	$SYNC_1$	$SYNC_0$	X	X	MONOSYNC, 6 BITS
$SYNC_{15}$	$SYNC_{14}$	$SYNC_{13}$	$SYNC_{12}$	$SYNC_{11}$	$SYNC_{10}$	$SYNC_9$	$SYNC_8$	BISYNC, 16 BITS
$SYNC_{11}$	$SYNC_{10}$	$SYNC_9$	$SYNC_8$	$SYNC_7$	$SYNC_6$	$SYNC_5$	$SYNC_4$	BISYNC, 12 BITS
0	1	1	1	1	1	1	0	SDLC

WRITE REGISTER 9

Bit	Function
D_0	VIS
D_1	NV
D_2	DLC
D_3	MIE
D_4	STATUS HIGH/STATUS LOW
D_5	0

D_7	D_6	
0	0	NO RESET
0	1	CHANNEL RESET B
1	0	CHANNEL RESET A
1	1	FORCE HARDWARE RESET

WRITE REGISTER 10

Bit	Function
D_0	6 BIT/$\overline{8\ BIT}$ SYNC
D_1	LOOP MODE
D_2	ABORT/$\overline{FLAG}$ ON UNDERRUN
D_3	MARK/$\overline{FLAG}$ IDLE
D_4	GO ACTIVE ON POLL

D_6	D_5	
0	0	NRZ
0	1	NRZ1
1	0	FM1 (TRANSITION = 1)
1	1	FM0 (TRANSITION = 0)

D_7: CRC PRESET I/$\overline{O}$

WRITE REGISTER 11

D_1	D_0	
0	0	$\overline{TRxC}$ OUT = XTAL OUTPUT
0	1	$\overline{TRxC}$ OUT = TRANSMIT CLOCK
1	0	$\overline{TRxC}$ OUT = BR GENERATOR OUTPUT
1	1	$\overline{TRxC}$ OUT = DPLL OUTPUT

D_2: $\overline{TRxC}$ O/I

D_4	D_3	
0	0	TRANSMIT CLOCK = $\overline{RTxC}$ PIN
0	1	TRANSMIT CLOCK = $\overline{TRxC}$ PIN
1	0	TRANSMIT CLOCK = BR GENERATOR OUTPUT
1	1	TRANSMIT CLOCK = DPLL OUTPUT

D_6	D_5	
0	0	RECEIVE CLOCK = $\overline{RTxC}$ PIN
0	1	RECEIVE CLOCK = $\overline{TRxC}$ PIN
1	0	RECEIVE CLOCK = BR GENERATOR OUTPUT
1	1	RECEIVE CLOCK = DPLL OUTPUT

D_7: $\overline{RTxC}$ XTAL/$\overline{NO\ XTAL}$

WRITE REGISTER 12

Bit	Function
D_0	TC_0
D_1	TC_1
D_2	TC_2
D_3	TC_3
D_4	TC_4
D_5	TC_5
D_6	TC_6
D_7	TC_7

LOWER BYTE OF TIME CONSTANT

WRITE REGISTER 13

Bit	Function
D_0	TC_8
D_1	TC_9
D_2	TC_{10}
D_3	TC_{11}
D_4	TC_{12}
D_5	TC_{13}
D_6	TC_{14}
D_7	TC_{15}

UPPER BYTE OF TIME CONSTANT

WRITE REGISTER 14

Bit	Function
D_0	BR GENERATOR ENABLE
D_1	BR GENERATOR SOURCE
D_2	DTR/REQUEST FUNCTION
D_3	AUTO ECHO
D_4	LOCAL LOOPBACK

D_7	D_6	D_5	
0	0	0	NULL COMMAND
0	1	1	ENTER SEARCH MODE
0	1	0	RESET MISSING CLOCK
0	1	1	DISABLE DPLL
1	0	0	SET SOURCE = BR GENERATOR
1	0	1	SET SOURCE = $\overline{RTxC}$
1	1	0	SET FM MODE
1	1	1	SET NRZ1 MODE

WRITE REGISTER 15

Bit	Function
D_0	0
D_1	ZERO COUNT IE
D_2	FIFO ENABLE
D_3	DCD IE
D_4	SYNC/HUNT IE
D_5	CTS IE
D_6	Tx UNDERRUN/EOM IE
D_7	BREAK/ABORT IE

Figure 10 : WRITE REGISTER BIT FUNCTIONS con't

FIFO

FIFO Enhancements

When used with a DMA controller, the Z85C30 FIFO enhancement maximizes the SCC's ability to receive high speed back-to-back SDLC messages while minimizing frame overruns due to CPU latencies in responding to interrupts.

Additional logic was added to the industry standard NMOS SCC consisting of a 10 deep by 19 bit status FIFO, 14-bit receive byte counter, and control logic as shown in Figure 16. The 10 x 19 bit status FIFO is separate from the existing three byte receive data FIFO.

When the enhancement is enabled, the status in read register 1 (RR1) and byte count for the SDLC frame will be stored in the 10 x 19 bit status FIFO. This allows the DMA controller to transfer the next frame into memory while the CPU verifies the message was properly received.

Summarizing the operation, data is received, assembled, loaded into the three byte receive FIFO before being transferred to memory by the DMA controller. When a flag is received at the end of an SDLC frame, the frame byte count from the 14-bit counter and five status bits are loaded into the status FIFO for verification by the CPU. The CRC checker is automatically reset in preparation for the next frame which can begin immediately. Since the byte count and status are saved for each frame, the message integrity can be verified at a later time. Status information for up to 10 frames can be stored before a status FIFO overrun could occur.

FIFO Detail

For a better understanding of details of the FIFO operation, refer to the block diagram contained in Figure 11.

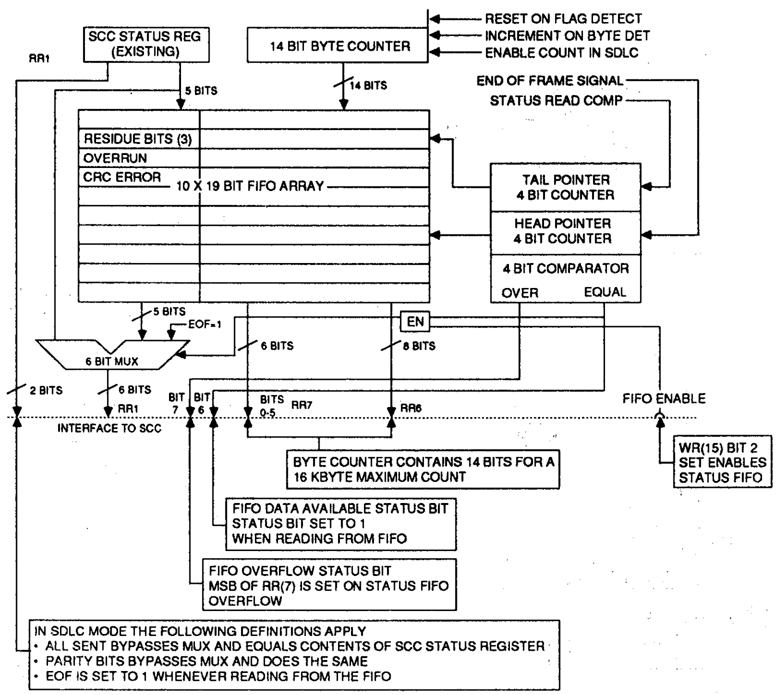


Figure 11 : SCC STATUS REGISTER MODIFICATIONS

Enable/Disable

This FIFO is implemented so that it is enabled when WR15 bit 2 is set and the SCC is in the SDLC/HDLC mode, otherwise the status register contents bypass the FIFO and go directly to the bus interface (the FIFO pointer logic is reset either when disabled or via a channel or power-on reset). When the FIFO mode is disabled, the SCC is completely downward-compatible with the NMOS 8530. The FIFO mode is disabled on power-up (WR15 bit 2 is set to 0 on reset). The effects of backward compatibility on the register set are that RR4 is an image of RR0, RR5 is an image of RR1, RR6 is an image of RR2 and RR7 is an image of RR3. For the details of the added registers, refer to Figure 18. The status of the FIFO Enable signal can be obtained by reading RR15 bit 2. If the FIFO is enabled, the bit will be set to 1; otherwise, it will be reset.

Read Operation

When WR15 bit 2 is set and the FIFO is not empty, the next read to any of status register RR1 or the additional registers RR6 and RR6 will actually be from the FIFO. Reading status register RR1 causes one location of the FIFO to be emptied, so status should be read after reading the byte count, otherwise the count will be incorrect. Before the FIFO underflows, it is disabled. In this case, the multiplexer is switched to allow status to read directly from the status register, and reads from RR7 and RR6 will contain bits that are undefined. Bit 6 of RR7 (FIFO Data Available) can be used to determine if status data is coming from the FIFO or directly from the status register, since it is set to 1 whenever the FIFO is not empty.

Since not all status bits must be stored in the FIFO, the All Sent, Parity, and EOF bits will bypass the FIFO. The status bits sent through the FIFO will be Residue Bits (3), Overrun, and CRC Error.

The sequence for proper operation of the byte count and FIFO logic is to read the registers in the following order: RR7, RR6 and RR1 (reading RR6 is optional). Additional logic prevents the FIFO from being emptied by multiple reads from RR1. The read from RR7 latches trhe FIFO empty/full status bit (bit 6) and steers the status multiplexer to read from the SCC megacell instead of the status FIFO (since the status FIFO is empty). The read from RR1 allows an entry to be read from the FIFO (if the FIFO was empty, logic is added to prevent a FIFO underflow condition).

Write Operation

When the end of an SDLC frame (EOF) has been received and the FIFO is enabled, the contents of the status and byte-count registers are loaded into the FIFO. The EOF signal is used to increment the FIFO. If the FIFO overflows, the MSB of RR7 (FIFO Overflow) is set to indicate the overflow. This bit and the FIFO control logic is reset by disabling and re-enabling the FIFO control bit (WR15 bit 2). For details of FIFO control timing uring an SDLC frame, refer to Figure 12.

Byte Counter Detail

The 14-bit byte counter allows for packets up to 16K bytes to be received. For a better understanding of its operation refer to Figures 11 and 12.

Enable

The byte counter is enabled in the SDLC/HDLC mode.

Reset

The byte counter is reset whenever an SDLC flag character is received. The reset is timed so that the contens of the byte counter are successfully written into the FIFO.

Increment

The byte counter is incremented by writes to the data FIFO. The counter represents the number of bytes received by the SCC, rather than the number of bytes transferred from the SCC. (These counts may differ by up to the number of bytes in the receive data FIFO contained in the SCC).

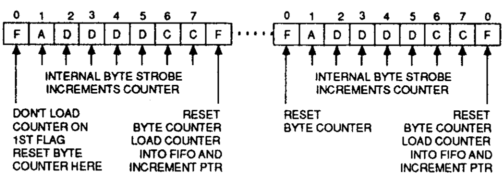


Figure 12 : SDLC BYTE COUNTING DETAIL

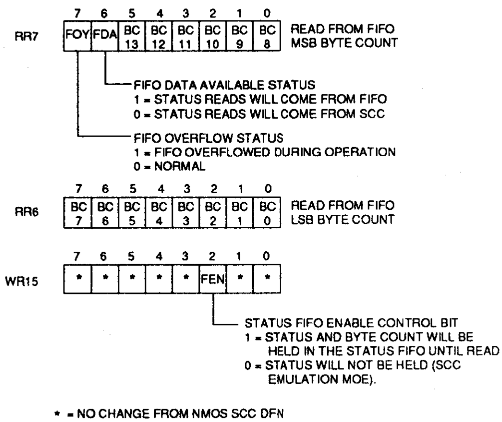


Figure 13 : SCC ADDITIONAL REGISTERS

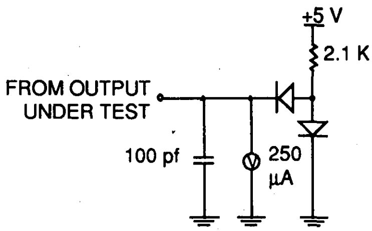


Figure 14: STANDARD TEST LOAD

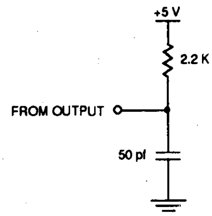


Figure 15: OPEN-DRAIN TEST LOAD

Table 3 : CAPACITANCE ($T_A = 25\,°C$, $V_{DD} = 5V \pm 5\%$, $V_{SS} = 0V$)

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
C_{IN}	Input /Capacitance	Unmeasured pins		10	pF
C_{OUT}	Output Capacitance	Returned to V_{SS}		15	pF
$C_{I/O}$	Bidirectional Capacitance			20	pF

f = 1 MHz, over specified temperature range.

Table 4 : RECOMMENDED OPERATING CONDITIONS

DC Supply Voltage		+4.75V to +5.25V
Operating Temperature Range	Commercial	0 °C to 70 °C

Table 5 : ABSOLUTE MAXIMUM RATINGS

Voltages on all pins with respect to V_{DD}	-0.3V to +7.0V
Power Dissipation (PD_{MAX})	165 mW
Operating Temperature (T_{OPT})	0 °C to 70 °C
Storage Temperature (T_{STG})	-65 °C TO +150 °C

Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 6 : DC CHARACTERISTICS (T_A - 0 °C to 70 °C, $V_{DD} = 5V \pm 10\%$)

Symbol	Paraneter	Test Conditions	Limits		Units
			Min	Max	
I_{CC1}	I_{CC}Supply Current	Clk = 10 MHz		30	mA
I_{IL}	Input Leakage Current	$0.4 \leq V_{IN} \leq +2.4V$		±10.0	µA
I_{OL}	Output Leakage Current	$0.4 \leq V_{OUT} \leq +2.4V$		±10.0	µA
V_{IH}	Input High Voltage		2.2	$V_{CC} + 0.3$	V
V_{IL}	Input Low Voltage		-0.3	0.8	V
V_{OHI}	Output High Voltage	I_{OH}=-1.6mA	2.4		V
V_{OH2}	Output High Voltage	I_{OH}=-250µA	V_{CC}- 0.8		V
V_{OL}	Output Low Voltage	I_{OL}=+2.0mA		0.4	V

Table 7 : AC CHARACTERISTICS (T_A = 0 °C to 70 °C, V_{DD} = 5V ± 5%)

Symbol	Parameter	Test Conditions	Limits 6 MHz Min	6 MHz Max	8MHz Min	8MHz Max	10MHz Min	10MHz Max	Units
TcPC	PCLK Cycle Time		165	2000	125	2000	100	2000	ns
TdA(DR)	Address Required Valid to Read Data Valid Delay			280		220		180	ns
TdIAi(RD)	$\overline{\text{INTACK}}$ to $\overline{\text{RD}}$ ↓ (Acknowledge) Delay	Note 5	200		150		125		ns
TdIEI(IEO)	IEI to IEO Delay Time			100		95		90	ns
TdPC(IEO)	PCLK ↑ to IEO Delay			250		200		175	ns
TdPC(INT)	PCLK ↓ to $\overline{\text{INT}}$ Valid Delay	Note 4		500		500		500	ns
TdRDA(DR)	$\overline{\text{RD}}$ ↓ (Acknowledge) to Read Data Valid Delay			180		140		120	ns
TdRDA(INT)	$\overline{\text{RD}}$ ↓ to $\overline{\text{INT}}$ Inactive Delay	Note 4		500		500		500	ns
TdRD(DRA)	$\overline{\text{RD}}$ ↓ to Read Data Active Delay		0		0		0		ns
TdRD(DRz)	$\overline{\text{RD}}$ ↑ to Read Data Float Delay	Note 2		45		40		35	ns
TdRDf(DR)	$\overline{\text{RD}}$ ↓ to Read Data Valid Delay			180		140		120	ns
TdRDf(REQ)	$\overline{\text{RD}}$ ↓ to $\overline{\text{W/REQ}}$ Not Valid Delay			200		170		160	ns
TdRDr(DR)	$\overline{\text{RD}}$ ↑ to Read Data Not Valid Delay		0		0		0		ns
TdRDr(REQ)	$\overline{\text{RD}}$ ↑ to $\overline{\text{DTR/REQ}}$ Not Valid Delay			4TcPC		4TcPC		4TcPC	ns
TdRD(W)	$\overline{\text{RD}}$ ↓ Wait Valid Delay	Note 4		200		170		160	ns
TdRD(WRQ)	$\overline{\text{RD}}$ ↑ to $\overline{\text{WR}}$ ↓ Delay for No Reset		15		15		15		ns
TdWR(REQ)	$\overline{\text{WR}}$ ↓ to $\overline{\text{W/REQ}}$ Not Valid Delay			200		170		160	ns
TdWRQ(RD)	$\overline{\text{WR}}$ ↑ to $\overline{\text{RD}}$ ↓ Delay for No Reset		30		15		15		ns
TdWRr(REQ)	$\overline{\text{WR}}$ ↓ $\overline{\text{DTR/REQ}}$ Not Valid Delay			4TcPC		4TcPC		4TcPC	ns
TdWR(W)	$\overline{\text{WR}}$ ↓ to Wait Valid Delay	Note 4		200		170		160	ns
TfPC	PCLK Fall Time			10		10		10	ns
ThA(RD)	Address to $\overline{\text{RD}}$ ↑ Hold Time		0		0		0		ns
ThA(WR)	Address to $\overline{\text{WR}}$ ↑ Hold Time		0		0		0		ns
ThCE(RD)	$\overline{\text{CE}}$ to $\overline{\text{RD}}$ ↑ Hold Time	Note 1	0		0		0		ns
ThCE(WR)	$\overline{\text{CE}}$ to $\overline{\text{WR}}$ ↑ Hold Time		0		0		0		ns
ThDW(WR)	Write Data to $\overline{\text{WR}}$ ↑ Hold Time		20		20		20		ns
ThIA(PC)	$\overline{\text{INTACK}}$ to PCLK ↑ Hold Time		100		40		30		ns
ThIA(RD)	$\overline{\text{INTACK}}$ to $\overline{\text{RD}}$ ↑ Hold Time		0		0		0		ns
ThIA(WR)	$\overline{\text{INTACK}}$ to $\overline{\text{WR}}$ ↑ Hold Time		0		0		0		ns
ThIEI(RDA)	IEI to $\overline{\text{RD}}$ ↑ (Acknowledge) Hold Time		0		0		0		ns
Trc	Valid Access Recovery Time	Note 3	4TcPC		4TcPC		4TcPC		ns
TrPC	PCLK Rise Time			10		10		10	ns
TsA(RD)	Address to $\overline{\text{RD}}$ ↓ Setup Time		80		70		50		ns
TsA(WR)	Address to $\overline{\text{WR}}$ ↓ Setup Time		80		70		50		ns
TsCEh(RD)	$\overline{\text{CE}}$ High to $\overline{\text{RD}}$ ↓ Setup Time	Note 1	70		60		50		ns
TsCEh(WR)	$\overline{\text{CE}}$ High to $\overline{\text{WR}}$ ↓ Setup Time		70		60		50		ns

3

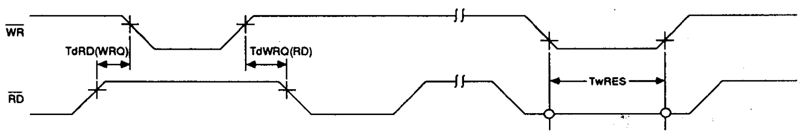
Table 7: AC CHARACTERISTICS con't

Symbol	Parameter	Test Conditions	Limits						Units
			6 MHz		8MHz		10MHz		
			Min	Max	Min	Max	Min	Max	
TsCEI(RD)	$\overline{CE}$ Low to $\overline{RD}$ ↓ Setup Time	Note 1	0		0		0		ns
TsCEI(WR)	$\overline{CE}$ Low to $\overline{WR}$ ↓ Setup Time		0		0		0		ns
TsDW(WR)	Write Data to $\overline{WR}$ ↓ Setup Time		10		10		10		ns
TsIAi(RD)	$\overline{INTACK}$ to $\overline{RD}$ ↓ Setup Time	Note 1	160		145		130		ns
TsIAi(WR)	$\overline{INTACK}$ to $\overline{WR}$ ↓ Setup Time	Note 1	160		145		130		ns
TsIA(PC)	$\overline{INTACK}$ to PCLK ↑ Setup Time		20		20		20		ns
TsIEI(RDA)	IEI to $\overline{RD}$ ↓ (Acknowledge) Setup Time		100		95		95		ns
TwPCh	PCLK High Width		70	1000	50	1000	40	1000	ns
TwPCl	PCLK Low Width		70	1000	50	1000	40	1000	ns
TwRDA	$\overline{RD}$ (Acknowledge) Width		200		150		125		ns
TwRDl	$\overline{RD}$ Low Width	Note 1	200		150		125		ns
TwRES	$\overline{WR}$ and $\overline{RD}$ Coincident Low for Reset		200		150		100		ns
TwWRl	$\overline{WR}$ Low Width		200		150		125		ns

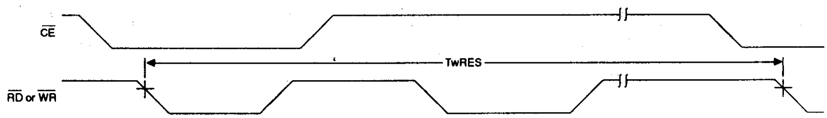
Notes: 1. Parameter does not apply to Interrupt Acknowledge transactions.
2. Float delay is defined as the time required for a ± 0.5V change at the output with a maximum dc load and minimum ac load.
3. Parameter applies only between transactions involving the SCC.
4. Open-drain output, measured with open-drain test load.
5. Parameter is system dependent. For any SCC in the daisy chain, TdIAi(RD) must be greater than the sum of TdPC(IEO) for the highest priority device in the daisy chain, TsIEI(RDA) for the SCC, and TdIEIf(IEO) for each device separating them in the daisy chain.

Figure 16 : TIMING DIAGRAMS

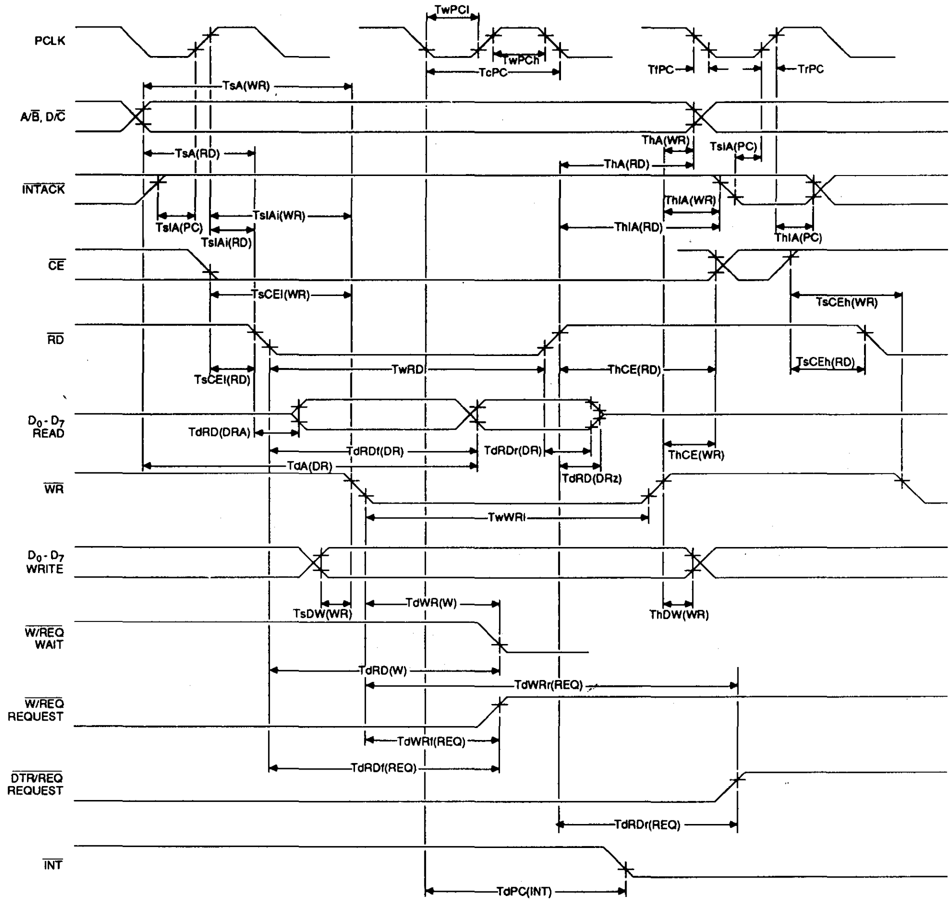
a) Reset Timing



b) Cycle Timing

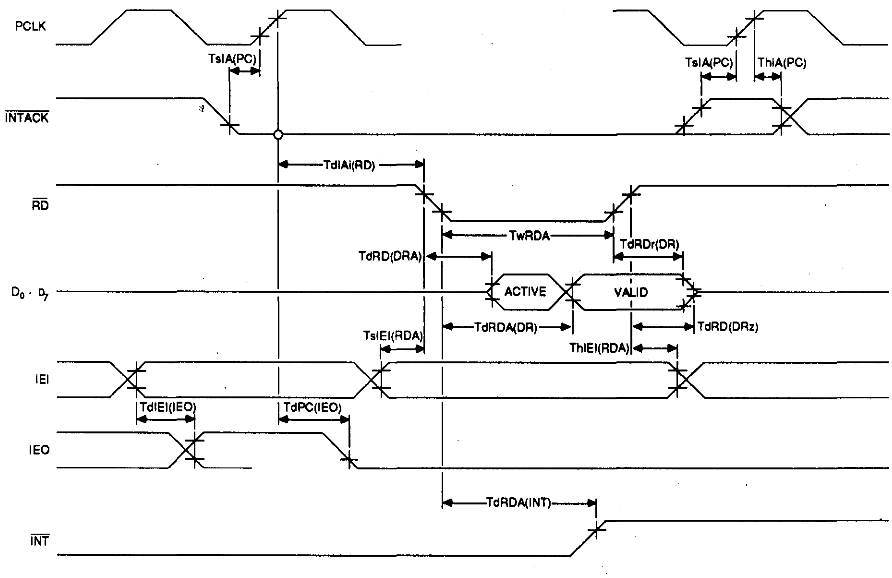


c) Read and Write Timing



Note: Addresses on A/B̄ and D/C̄ and the status on INTACK must remain stable throughout the cycle. If CE falls after RD or WR falls, or if it rises before RD or WR rises, the effective RD or WR is shortened. Data must be valid before the falling edge of WR.

d) Interrupt Acknowledge Timing



Note: Between the time INTACK goes Low and the falling edge of RD, the internal and external IEI/IEO daisy chains settle. If there is an interrupt pending in the SCC and IEI is High when RD falls, the Acknowledge cycle is intended for the SCC. In this case, the SCC may be programmed to respond to RD Low by placing its interrupt vector on D_0-D_7 and it then sets the appropriate Interrupt-Under-Service latch internally.

Table 8 : AC CHARACTERISTICS, GENERAL TIMING (T_A - 0 °C to 70 °C, V_{DD} = 5V ± 5%)

Symbol	Parameter	Test Conditions	Limits 6 MHz Min	6 MHz Max	8MHz Min	8MHz Max	10MHz Min	10MHz Max	Units
TcRTX	$\overline{RTxC}$ Cycle Time (RxD, TxD)	Notes 6,7	640		500		400		ns
TcRTXX	Crystal Oscillator Period	Note 3	165	1000	125	1000	100	1000	ns
TcTRX	$\overline{TRxC}$ Cycle Time	Notes 6, 7	640		500		400		ns
TdPC(REQ)	PCLK ↓ to $\overline{W/REQ}$ Valid Delay			250		250		250	ns
TdPC(W)	PCLK ↓ to Wait Inactive Delay			350		350		350	ns
TdTXCf(TXD)	$\overline{TxC}$ ↓ to TxD Delay (X1 Mode)	Note 2		230		200		150	ns
TdTxCr(TXD)	$\overline{TxC}$ ↑ to TxD Delay (X1 Mode)	Notes 2, 5		230		200		150	ns
TdTXD(TRX)	TxD to $\overline{TRxC}$ Delay (Send Clock Echo)			200		200		200	ns
ThRXD(RXCf)	RxD to $\overline{RxC}$ ↓ Hold Time (X1 Mode)	Notes 1, 5	150		150		150		ns
ThRXD(RXCr)	RxD to $\overline{RxC}$ ↑ Hold Time (X1 Mode)	Note 1	150		150		150		ns
ThSY(RXC)	$\overline{SYNC}$ to $\overline{RxC}$ ↑ Hold Time		5TcPC		5TcPC		5TcPC		ns
TsRXC(PC)	$\overline{RxC}$ ↑ to PCLK ↑ Setup Time (PCLK ÷ 4 case only)	Notes 1, 4	70	TwPCL	60	TwPCL	40	TwPCL	ns
TsRXD(RXCf)	RxD to $\overline{RxC}$ ↓ Setup Time (X1 Mode)	Notes 1, 5	0		0		0		ns
TsRXD(RXCr)	RxD to $\overline{RxC}$ ↑ Setup Time (X1 Mode)	Note 1	0		0		0		ns
TsSY(RXC)	$\overline{SYNC}$ to $\overline{RxC}$ ↑ Setup Time	Note 1	-200		-200		-200		ns
TsTXC(PC)	$\overline{TxC}$ ↓ to PCLK ↑ Setup Time	Notes 2, 4	0		0		0		ns
TwEXT	$\overline{DCD}$ or $\overline{CTS}$ Pulse Width		200		200		200		ns
TwRTXh	$\overline{RTxC}$ High Width	Note 6	180		150		150		ns
TwRTXl	$\overline{RTxC}$ Low Width	Note 6	180		150		150		ns
TwSY	$\overline{SYNC}$ Pulse Width		200		200		200		ns
TwTRXh	$\overline{TRxC}$ High Width	Note 6	180		150		150		ns
TwTRXl	$\overline{TRxC}$ Low Width	Note 6	180		150		150		ns

Notes:
1. $\overline{RxC}$ is $\overline{RTxC}$ or $\overline{TRxC}$, whichever is supplying the receive clock.
2. $\overline{TxC}$ is $\overline{TRxC}$ or $\overline{RTxC}$, whichever is supplying the transmit clock.
3. Both $\overline{RTxC}$ and $\overline{SYNC}$ have 30 pf capacitors to ground connected to them.
4. Parameter applies only if the data rate is one-fourth the PCLK rate. In all other cases, no phase relationship between RxC and PCLK or $\overline{TxC}$ and PCLK is required.
5. Parameter applies only to FM encoding/decoding.
6. Parameter applies only for transmitter and receiver; DPLL and baud rate generator timing requirements are identical to case PCLK requirements.
7. The maximum receive or transmit data is 1/4 PCLK.

Figure 17 : GENERAL TIMING

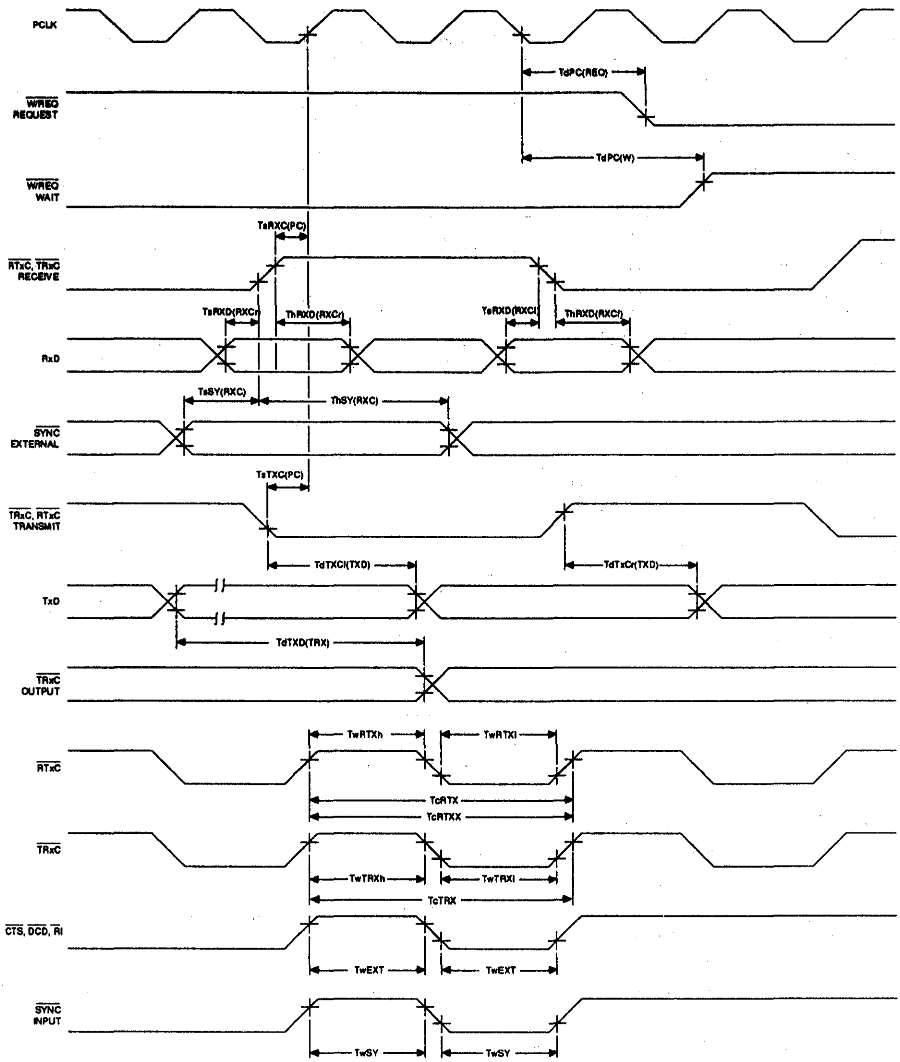
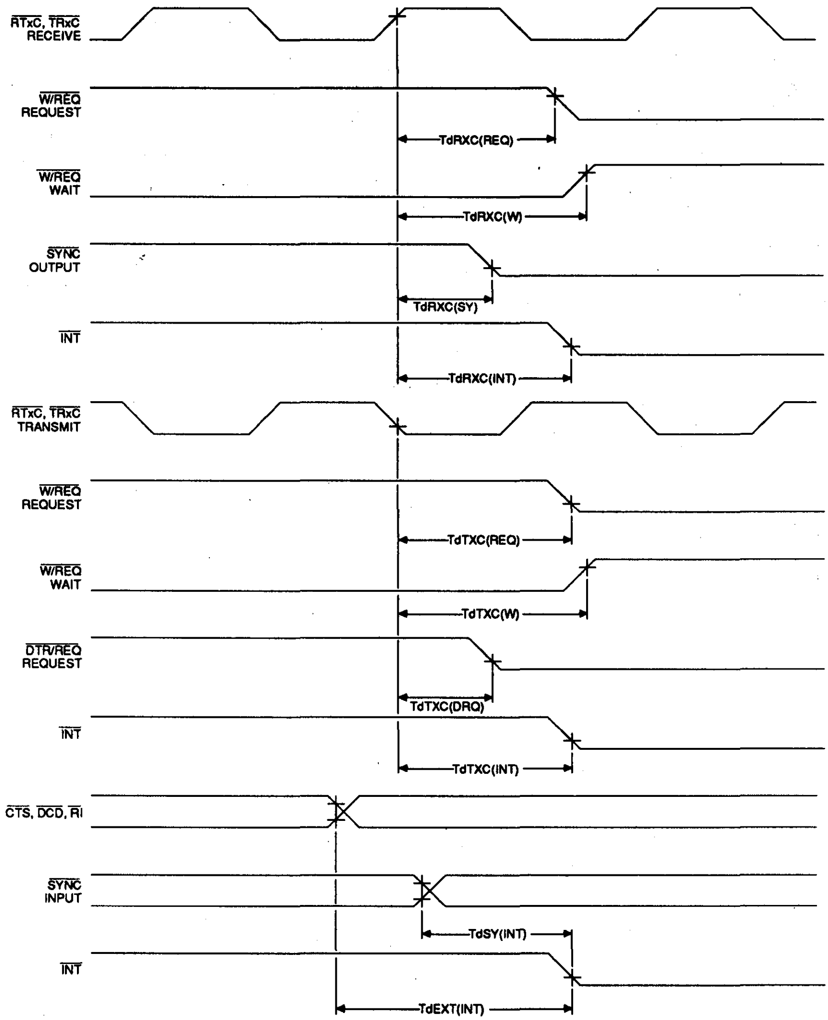


Table 9 : AC CHARACTERISTICS, SYSTEM TIMING (T_A - 0 °C to 70 °C, V_{DD} = 5V ± 5%)

Symbol	Parameter	Test Conditions	Limits						Units
			6 MHz		8MHz		10MHz		
			Min	Max	Min	Max	Min	Max	
TdEXT(INT)	$\overline{DCD}$ or $\overline{CTS}$ Transition to $\overline{INT}$ Valid Delay	Note 1	2	6	2	6	2	6	TcPC
TdRXC(INT)	$\overline{RxC}$ $\uparrow$ to $\overline{INT}$ Valid Delay	Notes 1, 2	10	16	10	16	10	16	TcPC
TdRXC(REQ)	$\overline{RxC}$ $\uparrow$ to $\overline{W/REQ}$ Valid Delay	Note 2	8	12	8	12	8	12	TcPC
TdRXC(SY)	$\overline{RxC}$ $\uparrow$ to $\overline{SYNC}$ Valid Delay	Note 2	4	7	4	7	4	7	TcPC
TdRXC(W)	$\overline{RxC}$ $\uparrow$ to Wai' Inactive Delay	Notes 1, 2	8	14	8	14	8	14	TcPC
TdSY(INT)	$\overline{SYNC}$ Transition to $\overline{INT}$ Valid Delay	Note 1	2	6	2	6	2	6	TcPC
TdTXC(DRQ)	TxC $\downarrow$ to DTR/REQ Valid Delay	Note 3	4	7	4	7	4	7	TcPC
TdTXC(INT)	$\overline{TxC}$ $\downarrow$ to $\overline{INT}$ Valid Delay	Notes 1, 3	6	10	6	10	6	10	TcPC
TdTXC(REQ)	$\overline{TxC}$ $\downarrow$ to $\overline{W/REQ}$ Valid Delay	Note 3	5	8	5	8	5	8	TcPC
TdTXC(W)	$\overline{TxC}$ $\downarrow$ to Wait Inactive Delay	Notes 1, 3	5	11	5	11	5	11	TcPC

Notes: 1.Open-drain output, measured with open-drain test load.
2. $\overline{RxC}$ is $\overline{RTxC}$ or $\overline{TRxC}$, whichever is supplying the receive clock.
3. $\overline{TxC}$ is $\overline{TRxC}$ or $\overline{RTxC}$, whichever is supplying the transmit clock.

Figure 18 : SYSTEM TIMING



3

PACKAGE DIMENSIONS

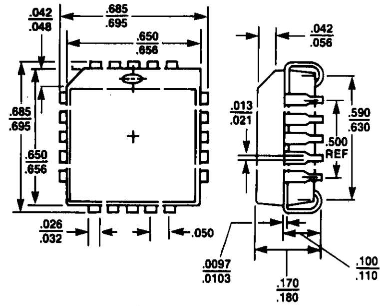
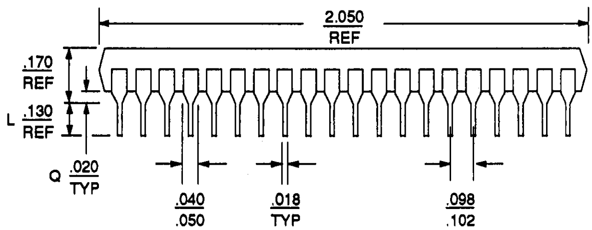
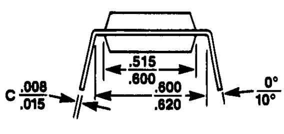


Figure 19 : 44-Pin PLCC





ALL DIMENSIONS IN INCHES

Figure 20 : 40-Pin DIP

ORDERING INFORMATION and PRODUCT CODE

KS 85C30 – X X X

Samsung Semiconductor, Inc. (KS)

Part Number (85C30)

Speed
- -6 6 MHz
- -8 8 MHz
- -10 10 MHz

Temperature
- C - Commercial (0 °C to + 70 °C)

Packaging
- P - Plastic DIP
- L - Plastic Leaded Chip Carrier (PLCC)

Samsung products are designated by a Product Code. When ordering, refer to products by their full code. For unusual, and/or specific packaging or processing requirements not covered by the standard product line, please contact Samsung Microprocessor Marketing.

SALES OFFICES 4

SAMSUNG SEMICONDUCTOR SALES OFFICES - U.S.A.

CALIFORNIA		ILLINOIS	MASSACHUSETTS	TEXAS
22837 Ventura Blvd. Suite 305 Woodland Hills, CA 91367 (818) 346-6416 FAX: (818) 346-6621	2700 Augustine Drive Suite 198 Santa Clara, CA 95054 (408) 727-7433 FAX: (408) 727-5071	901 Warrenville Road Suite 120 Lisle, IL 60532-1359 (312) 852-2011 FAX:(312) 852-3096	20 Burlington Mall Road Suite 205 Burlington, MA 01803 (617) 273-4888 FAX:(617)273-9363	15851 Dallas Parkway Suite 745 Dallas, TX 75248-3307 (214) 239-0754 FAX:(214) 392-4624

SAMSUNG SEMICONDUCTOR REPRESENTATIVES

U.S.A. and CANADA

ARIZONA

HAAS & ASSOC. INC.
77441 East Butherus Drive
Suite 300
Scottsdale,AZ 85260
TEL: (602) 998-7195
FAX: (602) 998-7869

CALIFORNIA

QUEST REP INC.
9444 Farnham St.
Suite 107
San Diego,CA 92123
TEL: (619) 565-8797
FAX: (619) 565-8990

SYNPAC
3945 Freedom Circle
Suite 650
Santa Clara,CA 95054
TEL: (408) 988-6988
FAX: (408) 988-5041

WESTAR REP COMPANY
2472 Chambers Road
Suite 100
Tustin, CA 92680
TEL:(714) 832-3325
FAX: (714) 832-7894

WESTAR REP COMPANY
25202 Crenshaw Blvd.
Suite 217
Torrance, CA 90505
TEL: (213) 539-2156
FAX: (213) 539-2564

CANADA

TERRIER ELEC.
145 The West Mall
Etobicoke, Ontario, Canada
M9C 1C2
TEL: (416) 622-7558
FAX: (416) 626-1035

TERRIER ELEC.
3700 Gilmore Way, 106A
Burnaby, B.C., Canada
V5G 4M1
TEL: (604) 433-0159
FAX: (604) 430-0144

TERRIER ELEC.
6600 Transcanadienne
Suite 750-17
Pointe Claire, Quebec, Canada
H9R 452
TEL: (514) 695-4421
FAX: (514) 695-3295

COLORADO

CANDAL INC.
7500 West Mississippi Ave.
Suite A-2
Lakewood, CO 80226
TEL: (303) 935-7128
FAX: (303) 935-7310

CONNECTICUT

PHOENIX SALES
257 Main Street
Torrington,CT 06790
TEL: (203) 496-7709
FAX: (203) 496-0912

FLORIDA

MEC
700 W. Hillsboro Blvd.
Bldg. 4, Suite 204
Deerfield Beach, FL 33441
TEL: (305) 426-8944
FAX: (305) 426-8799

MEC
511 Carriage Road
Indian Harbour Beach, FL 32937
TEL: (407) 332-7158
(407) 773-1100
FAX: (407) 830-5436

MEC
830 North Atlantic Blvd.
Suite B401
Cocoa Beach, FL 32931
TEL: (407) 799-0820
FAX: (407) 799-0923

MEC
1001 45th, N.E.
St. Petersburg, FL 33703
TEL: (813) 522-3433
FAX: (813) 522-3993

ILLINOIS

IRI
8430 Gross Point Road
Skokie,IL 60076
TEL: (312) 967-8430
FAX: (312) 967-5903

INDIANA

STB & ASSOC. INC.
3003 E. 96th St.
Suite102
Indianapolis,IN 46240
TEL: (317) 844-9227
FAX: (317) 844-1904

MARYLAND

ADVANCED TECH SALES
809 Hammonds Ferry Rd.
Suite D
Linthicum,MD 21090
TEL: (301) 789-9360
FAX: (301) 789-9364

MASSACHUSETTS

NEW TECH SOLUTIONS, INC.
111 South Bedford Street
Suite 102
Burlington, MA 01803
TEL: (617) 229-8888
FAX: (617) 229-1614

MICHIGAN

JENSEN C.B.
2145 Crooks Rd.
Troy,MI 48084
TEL: (313) 643-0506
FAX: (313) 643-4735

MINNESOTA

IRI
1120 East 80th Street
Bloomington, MN 55420
TEL: (612) 854-1120
FAX: (612) 854-8312

NEW JERSEY

NECCO
2460 Lemoine Avenue
Ft. Lee,NJ 07024
TEL: (201) 461-2789
FAX: (201) 461-3857

NEW MEXICO

S.W. SALES, INC.
7137 Settlement Way, N.W.
Albuquerque, NM 87120
TEL: (505) 899-9005

NEW YORK

T-SQUARE
6443 Ridings Road
Syracuse, NY 13206
TEL: (315) 463-8592
FAX: (315) 463-0355

T-SQUARE
7353 Victor-Pittsford Road
Victor, NY 14564
TEL: (716) 924-9101
FAX: (716) 924-4946

NORTH CAROLINA

GODWIN & ASSOC.
1100 Logger Ct.
Suite B 102
Raleigh, NC 27609
TEL: (919) 878-8000
FAX: (919) 878-3923

GODWIN & ASSOCIATES
2812 Oak Leigh Drive
Charlotte, NC 28213
TEL: (704)549-8500
FAX: (704) 549-9792

OHIO

BAILEY, J.N. & ASSOC.
129 W. Main Street
New Lebanon,OH 45345
TEL: (513) 687-1325
FAX: (513) 687-2930

BAILEY, J.N. & ASSOC.
2679 Indianola Avenue
Columbus,OH 43202
TEL: (614) 262-7274
FAX: (614) 262-0384

BAILEY, J.N. & ASSOC.
1667 Devonshire Drive
Brunswick,OH 44212
TEL: (216) 273-3798
FAX: (216) 225-1461

OREGON

EARL & BROWN CO.
9735 S.W. Sunshine Ct.
Suite500
Beaverton,OR 97005
TEL: (503) 643-5500
FAX: (503) 644-9230

PENNSYLVANIA

RIVCO JANUARY INC.
RJI Building
78 South Trooper Road
Norristown,PA 19403
TEL: (215) 631-1414
FAX: (215) 631-1640

PUERTO RICO

DIGIT-TECH
P.O. Boz 1945
Calle Cruz #2
Bajos, San German 00753
TEL: (809) 892-4260
FAX: (809) 892-3366

TEXAS

S.W. SALES INC.
2267 Trawood, Bldg. E3
El Paso, TX 79935
TEL: (915) 594-8259
FAX: (915) 592-0288

VIELOCK ASSOC.
720 E. Park Blvd.
Suite102
Plano,TX 75074
TEL: (214) 881-1940
FAX: (214) 423-8556

VIELOCK ASSOC.
9600 Great Hills Trail
Suite150-W
Austin,TX 78759
TEL: (512) 345-8498
FAX: (512) 346-4037

UTAH

ANDERSON & ASSOC.
270 South Main, #108
Bountiful, UT 84010
TEL: (801) 292-8991
FAX: (801) 298-1503

VIRGINIA

ADVANCED TECHNOLOGY SALES, INC.
406 Grinell Drive
Richmond, VA 23236
TEL: (804) 320-8756
FAX: (804) 320-8761

WASHINGTON

EARL & BROWN CO.
2447-A 152nd Ave. N.E.
Redmond,WA 98052
TEL: (206) 885-5064
FAX: (206) 885-2262

WISCONSIN

IRI
631 Mayfair
Milwaukée, WI 53226
TEL: (414) 259-0965
FAX: (414) 259-0326

SAMSUNG SEMICONDUCTOR SALES OFFICES-EUROPE

SAMSUNG SEMICONDUCTOR EUROPE GmbH Mergenthaler Allee 38-40 D6236 Eschborn (West Germany) Tel: 06196/9009-0 Fax: 0196/9009-89	**PARIS** Centre d'Affaires La Boursidiere RN 186, Bat. Bourgogne, BP 202 F-92357 Le Plessis-Robinson (France) Tel: 1/40 94 07 00 Fax: 1/40 94 02 16	**MILANO** Viale G. Matteotti, 26 I-20095 Cusano Milanino (Italy) Tel: 2/61 32 888 Fax: 2/61 92 279	**MÜNCHEN** Carl-Zeiss-Ring 4, D-8045 Ismaning (West Germany) Tel: 089/96 48 30 + 089/96 48 38 Fax:

SAMSUNG SEMICONDUCTOR REPRESENTATIVES

EUROPE

AUSTRIA

SATRON HANDELSGES. MBH
Hoffmeistergasse 8-10/1/5
A-1120 Wien
TEL: 0043-222-87 30 20
FAX: 0043-222-83 35 83
TLX: 047-753 11 85 1

BELGIUM

C & S ELECTRONICS NV
Heembeekstraat 111
D1100
TEL: 0032-2-7 25 09 00
FAX: 0032-2-7 25 08 13
TLX: 046-25820

DENMARK

MER-EL
Ved Klaedebo 18
DK-2907 Horshiom
TEL: 0046-157 100
FAX: 045-257 22 99
TLX: 37360 MEDEL DK

FINLAND

INSTRUMENTARIUM ELEKTRONIIKKA
P.O. Box 64, Vitikka 1
SF-02631-ESPOO
Helsinki
TEL: 00358-0-5 28 43 20
FAX: 00308-0-502 10 73
TLX: 057-12 44 26

FRANCE

ASIA MOS (OMNITECH ELCCTRONIQUE)
Ratiment Evolic 1 165,
Boulevard De Vaimy
F-92705 Colombes
TEL: 0033-1-47 60 12 47
FAX: 0033-1-47 60 15 82
TLX: 042-61 38 90

SONEL-ROHE (SCAIB)
6, Rue Le Corbusier
Silic 424
F-94583 Rungis Cedex
TEL: 0033-1-46 86 81 70
FAX: 0033-1-45 60 55 49
TLX: 042-20 69 52

GERMANY (WEST)

SILCOM ELECTRONICS VERTRIEBS GmbH
Neusser Str. 336-338
D-4050 Monchengladbach
TEL: (49)-0-2161-6 07 52
FAX: (49)-0-2161-65 16 38
TLX: 85 21 89

TERMOTROL GmbH
Pilotystr. 4
D-8000 Munchen 22
TEL: (49)-0-89-23 0 52 52
FAX: (49)-0-89-23 0352 98
TLX: 17898453

ING. THEO HENSKES GmbH
Laatzener Str. 19
Postfach 72 12 26
D 3000 Hannover 72
TEL: (49)-0-511-86 50 75
FAX: (49)-0-511-87 60 04
TLX: 92 35 09

ASTRONIC GmbH
Grunwalder Weg 30
D-8024 Deisenhofen
TEL: (49)-0-89-61 30 303
FAX: (49)-0-89-61 31 66 8
TLX: 5 21 61 87

MSC-MICROCOMPUTERS SYSTEMS COMPONENTS VERTRIEBS GmbH
Industriestrabe 16
Postfach 1380
D-7513 Stutensee 3
TEL: (49)-0-7249-70 75
FAX: (49)-0-7249 79 93
TLX: 17 72 49 11

SAMSUNG SEMICONDUCTOR REPRESENTATIVES

MICRONETICS GmbH
Wail Dur Stadtor Str. 45 — TEL: (49)-0-7159-60 19
D-7253 Renningen 1 — FAX: (49)-0-7 159 51 19
TLX: 72 47 08

ITALY

DIS. EL. SPA
Via Aia Di Stura 71/18 — TEL: 0039-1-12201522/25
I-10148 Torino — FAX: 0039-1-12 16 59 15
TLX: 043-21 51 18

MOXEL S.R.L.
Via C. Frova, 34 — TEL: 0039-2-61 29 05 21
I-2092 Cinisello Balsamo — FAX: 0039-2-6 17 25 82
TLX: 043-35 20 45

NETHERLANDS

MALCHUS BV HANDEIMIJ.
Fokkerstraat 511-513 — TEL: 0031-10-4 27 77 77
Postbus 48 — FAX: 0031-10-4 15 48 67
NL-3125 BD Schiedam — TLX: 044-2 15 98

NORWAY

SEMI DEVICES A/S
Asenveien 1 — TEL: 0047-9-87 65 60
N-1400 Ski

PORTUGAL

NIPOSOM-J. NABAIS LTD.
R. Casimiro Freire 9A — TEL: 00351-1-89-66 10
P-1900 Lisboa — FAX: 00351-80 95 17
TLX: 0404-1 40 28

SPAIN

SEMITRONIC S.A.
C/Maria Lombillo, 14 — TEL: 0034-1-320 21 60 61
E 28077 Madrid — FAX: 0034-1-320 21 98

SEMICONDUCTORES S.A.
Ronda General Mitre — TEL: 0034-3-2 17 23 40
240 Bjs — FAX: 0034-3-2 17 65 98
E-08006 Barcelona — TLX: 052-9 77 87

SWEDEN

MIKO KOMPONENT AB
Seqersbwagen 3 — TEL: 0046-753-89 08 0
P.O. Box 2001 — FAX: 0046-753-75 34 0
S-14502 Norsborg — TLX: 054-150 23

SWITZERLAND

PANATEL AG
Grundstr. 20 — TEL: 0041-42 64 30 30
CH-6343 Rotkreuz — FAX: 0041-42 64 30 35
TLX: 045-86 87 63

UNITED KINGDOM

KORD DISTRIBUTION LTD.
Watchmoor Road. Camberley — TEL: 0276 685741
Surrey GU153AQ. — TLX: 859919 KORDIS G.

BYTECH LTD.
2 The Western Centre, — TEL: Sales 0344 482211
Western Road, — Account/Admin 0344 424222
Bracknell Berkshire
RG121RW — TLX: 848215

ITT MULTI COMPONENTS
346 Edinburgh Avenue — TEL: 0753 824212
Slough SL1 4TU — FAX: 0753 824160
TLX: 849804

NELTRONIC LIMITED
John F. Kennedy Road, — TEL: (01) 503560
Naas Road, Oublin 12, — FAX: (01) 552789
Ireland — TLX: 93556 NELT EI

SAMSUNG SEMICONDUCTOR REPRESENTATIVES

ASIA

HONG KONG

AV. CONCEPT LTD.
Rm. 802-804, Tower A,
Hunghom Comm, Centre,
37-39 Ma Tau Wai Road
Hunghom, Kln, H.K.
TEL: 3-629325
FAX: 3-7643108
TLX: 52362 ADVCC HX

PROTECH COMPONENTS LTD.
Flat 3, 10/F., Wing Shing Ind. Bldg., 26Ng Fong Street, San Po Kong, Kowloon, Hong Kong
TEL: 3-3522181
FAX: 3-3523759
TLX: 38396 PTLD HX

TAIWAN

YOSUN INDUSTRIAL COPR.
Min-Sheng Commercial Bldg., 10F No. 481 Min-Sheng East Rd., Taipei, Taiwan, R.O.C.
TEL: 011-886-2-501-0770~9
FAX: 001-886-2-503-1278
TLX: 26777 YOSUNIND

KENTOP ELECTRONCIS CO., LTD.
3/F, Nbr 22., Sec-2, Chung Cheng Rd., Shin-Lin, Taipei, Taiwan, R.O.C.
TEL: 001-886-2-832-5800/5802
FAX: 001-886-2-832-5521

KINREX CORP
2nd. Fl., 514-3
Tun Hwa S.Rd.,
Taipei, Taiwan, R.O.C.
TEL: 001-886-2-700-4686~9
FAX: 001-886-2-704-2482
TLX: 20402 KINREX

JAPAN

ADO ELECTRONIC INDUSTRIAL CO., LTD.
7th Fl., Sasage Bldg., 4-6 Sotokanda 2-Chome Chiyoda-ku, Tokyo 101, Japan
TEL: 03-257-1618
FAX: 03-257-1579

INTERCOMPO INC.
Ihi Bldg., 1-6-7, Shibuya, Shibuya-ku, Tokyo 150 Japan
TEL: 03-406-5612
FAX: 04-409-4834

CHEMI-CON INTERNATIONAL COPR.
Mitauya Toranomon Bldg., 22-14, Toranomon 1 Chome Minato-ku, Tokyo 105, Japan
TEL: 03-508-2841
FAX: 03-504-0566

TOMEN ELECTRONICS COPR.
1-1, Uschisaiwai-cho 2 Chome Chiyoda-ku, Tokyo, 100
TEL: 03-506-3473
FAX: 03-506-3497

DIA SEMICON SYSTEMS INC.
Wacore 64 1-37-8, Sangenjaya, Setagaya-ku, Tokyo 154 Japan
TEL: 03-487-0386
FAX: 03-487-8088

RIKEI CORP.
Nichimen Bldg., 2-2-2, Nakanoshima, Kita-ku, Osaka 530 Japan
TEL: 06-201-2081
FAX: 06-222-1185

SINGAPORE

GEMINI ELECTRONICS PTE LTD.
100, Upper Cross Street #09-08 OG Bldg. Singapore 0105
TEL: 65-5351777
FAX: 65-5350348
TLX: RS 42819

INDIA

COMPONENTS AND SYSTEMS MARKETING ASSOCIATES (INDIA) PVT. LTD.
100, Dadasaheb Phalke Road, Dadar, Bombay 400 014
TEL: 4114585
FAX: 4112546
TLX: 001-4605 PDT IN

TURKEY

ELEKTRO SAN. VE TIC. KOLL. STI.
Hasanpasa, Ahmet Rasim Sok No. 16 Kadiköy istanbul-Turkey
TEL: 337-2245
FAX: 336-8814
TLX: 29569 elts tr

THAILAND

VUTIPONG TRADING LTD., PART.
51-53 Pahurat Rd. (Banmoh) Bangkok 10200 THAILAND
TEL: 221-9699 3641
223-4608
FAX: 224-0861
TLX: 87470 Vutipong TH

SAMSUNG SEMICONDUCTOR REPRESENTATIVES

KOREA

NAEWAE ELECTRIC CO., LTD.

#751-33, Daelim-dong	TEL: 646-9101-9
Youngdeungpo-ku,	FAX: 844-3001
Seoul, Korea	C.P.O. Box 1409
Cable: "ELECONAEWAE"	Sewoon Store: 277-0767
Seoul	Pusan Branch:
	(051) 808-7425
	Youngsan: 701-7341-5

SAMSUNG LIGHT-ELECTRONICS CO., LTD.

4th Fl. Room 2-3, Electroncis	TEL: 718-0045,
Main Bldg., #16-9,	718-9531-5
Hankangro-3ka, Yongsan-ku,	FAX: 718-9536
Seoul, Korea	

NEW CASTLE SEMICONDUTOR CO., LTD.

4th Fl. Room 10-11, Elec-	TEL: 718-8531-4
tronics Main Bldg., #16-9,	FAX: 718-8535
Hankangro-3ka, Yongsan-ku,	
Seoul, Korea	

HANKOOK SEMICON-DUCTOR

#1054-9, Namhyung-dong,	TEL: 588-2981-4
Kwanak-ku, Seoul, Korea	FAX: 588-2980

SEG YUNG INTERISE CORP.

#21-301, Suninbldg, 16-1,	TEL: 701-6811-6,
Hankangro-2ka, Yongsan. ku,	701-6781-4
Seoul, Korea	FAX: 701-6785

SAMSUNG SEMICONDUCTOR DISTRIBUTORS

ALABAMA

HAMMOND (205) 830-4764
4411-B Evangel Circle, N.W.
Huntsville, AL 35816

ARIZONA

ADDED VALUE (602) 951-9788
7741 East Gray Road
Suite #9
Scottsdale, AZ 85260

CYPRESS/RPS (602) 966-2256
2164 E. Broadway Road #310-8
Tempe, AZ 85282

CALIFORNIA

ADDED VALUE (209) 734-8861
3320 East Mineral King
Unit D
Visalia, CA 93291

ADDED VALUE (714) 259-8258
1582 Parkway Loop
Unit G
Tustin, CA 92680

ADDED VALUE (619) 558-8890
6397 Nancy Ridge Road
San Diego, CA 92121

ADDED VALUE (818) 889-2861
31194 La Baya Drive, #100
Westlake Village, CA 91362

ALL AMERICAN (800) 669-8300
369 Van Ness Way #701
Torrance, CA 90501

BELL MICRO PRODUCTS (714) 963-0667
18350 Mt. Langley
Fountain Valley, CA 92708

BELL MICRO PRODUCTS (408) 434-1150
550 Sycamore Drive
Milpitas, CA 95035

CYPRESS/RPS (714) 521-5230
6230 Descanso Avenue
Buena Park, CA 90620

CYPRESS/RPS (619) 535-0011
10054 Mesa Ridge Ct
Suite118
San Diego, CA 92121

CYPRESS/RPS (408) 980-8400
2175 Martin Avenue
Santa Clara, Ca 95050

CYPRESS/RPS (818) 710-7780
21550 Oxnard, #420
Woodland Hills, CA 91367

JACO (805) 495-9998
2260 Townsgate Road
Westlake Village, CA 91361

JACO (408) 432-9290
2880 ZANKER ROAD
SUITE 202
SAN JOSE, CA 95134

JACO (714) 837-8966
23-441 South Pointe Drive
Laguna Hills,, CA 92653

MICRO GENESIS (408) 727-5050
2880 Lakeside Drive
Santa Clara, CA 95054

CANADA

ELECTRONIC WHOLESALERS
1935 Avenue De L'Eglise (514) 769-8861
Montreal,Quebec,Canada
H4E 1H2

PETERSON,C.M (519) 434-3204
220 Adelaide Street North
London,Ontario,Canada
N6B 3H4

SAYNOR VARAH (416) 445-2340
99 Scarsdale Road
Don Mills, Ontario, Canada
M3B 2R4

SAYNOR VARAH (604) 273-2911
1-13511 Crestwood Place
Richmond, B.C., Canada
V6V 2G5

WESTBURNE IND.ENT.,LTD.
300 Steeprock Drive (416) 635-2950
Downsview,Ontario,Canada
M3J 2W9

COLORADO

ADDED VALUE (303) 422-1701
4090 Youngfield
Wheat Ridge, CO 80033

CYPRESS/RPS (303) 792-5829
12503 E. Euclid Drive
Englewood, CO 80111

CONNECTICUT

ALMO ELECTRONICS (203) 288-6556
31 Village Lane
Wallingford, CT 06492

JACO (203) 235-1422
384 Pratt Street
Meriden, CT 06450

4

JV (203) 469-2321
690 Main Street
East Haven, CT 06512

FLORIDA

ALL AMERICAN (305) 621-8282
16251 N.W. 54th Avenue
Miami, FL 33014

HAMMOND (407) 973-7103
6600 N.W. 21st. Avenue
Fort Lauderdale, FL 33309

HAMMOND (407) 849-6060
1230 W. Central Blvd
Orlando, FL 32802

MICRO GENESIS (407) 869-9989
2170 W. State Road 434 #324
Longwood, FL 32779

GEORGIA

HAMMOND (404) 449-1996
5680 Oakbrook Parkway
#160
Norcross, GA 30093

QUALITY COMPONENTS (404) 449-9508
6145 Northbelt Parkway
Suite B
Norcross, GA 30071

ILLINOIS

GOOLD (312) 860-7171
101 Leland Court
Bensenville, IL 60106

QPS (312) 884-6620
101 Commerce Dr. #A
Schaumburg, IL 60173

INDIANA

ALTEX (317) 848-1323
12744 N. Meridian
Carmel, IN 46032

CHELSEA INDUSTRIES (317) 253-9065
8465 Keystone Crossing, #115
Indianapolis, IN 46240

MARYLAND

ALL AMERICAN (301) 251-1205
1136 Taft Street
Rockville, MD 20853

ALMO ELECTRONICS (301) 953-2566
8309B Sherwick Court
Jessup, MD 20794

GENERAL RADIO SUPPLY (301) 995-6744
6935L Oakland Mills Road
Columbia, MD 21045

JACO (301) 995-6620
Rivers Center
10270 Old Columbia Road
Columbia, MD 21046

MASSACHUSETS

ALMO ELECTRONICS (617) 821-1450
60 Shawmut Avenue
Canton, MA 02021

GERBER (617) 329-2400
128 Carnegie Row
Norwood,MA 02062

JACO (617) 273-1860
222 Andover Street
Wilmington,MA 01887

MICHIGAN

CALDER (616) 698-7400
4245 Brockton Drive
Grand Rapids, MI 49508

CHELSEA INDUSTRIES (313) 525-1155
34443 Schoolcraft
Livonia, MI 48150

MINNESOTA

ALL AMERICAN (612) 944-2151
11409 Valley View Road
Eden Prairie, MN 55344

CYPRESS/RPS (612) 934-2104
7650 Executive Drive
Eden Prairie, MN 55344

VOYAGER (612) 571-7766
5201 East River Road
Fridley, MN 55421

MISSOURI

CHELSEA INDUSTRIES (314) 997-7709
2555 Metro Blvd
Maryland Heights, MO 63043

NEW JERSEY

ALMO ELECTRONICS (201) 613-0200
12 Connerty Court
East Brunswick, NJ 08816

GENERAL RADIO SUPPLY (609) 964-8560
600 Penn St. @ Bridge Plaza
Camden, NJ 08102

JACO (201) 942-4000
Ottilio Office Complex
555 Preakness Avenue
Totowa, NJ 07512

SAMSUNG SEMICONDUCTOR DISTRIBUTORS
(Continued)

NEW YORK

ALL AMERICAN (516) 981-3935
33 Commack Loop
Ronkonkoma, NY 11779

CAM/RPC (716) 427-9999
2975 Brighton Henrietta TL Road
Rochester, NY 14623

JACO (516)-273-5500
145 Oser Avenue
Hauppauge, NY 11788

MICRO GENESIS (516) 472-6000
90-10 Colin Drive
Holbook, NY 11741

NORTH CAROLINA

QUALITY COMPONENTS (919) 467-4897
3029-105 Stonybrook Drive
Raleigh, NC 27604

DIXIE (704) 377-5413
2220 South Tryon Street
Charlotte, NC 28234

HAMMOND (919) 275-6391
2923 Pacific Avenue
Greensboro, NC 27420

RESCO/RALEIGH (919) 781-5700
Hwy. 70 West & Resco Court
Raleigh, NC 27612

OHIO

CAM/RPC (216) 461-4700
749 Miner Road
Cleveland, OH 44143

CAM/RPC (614) 888-7777
15 Bishop Drive #104
Westerville, OH 43081

CAM/RPC (513) 433-5551
7973-B Washington Woods Drive
Centerville, OH 45459

CHELSEA INDUSTRIES (513) 891-3905
10979 Reed Hartman Highway
#133
Cincinnati, OH 45242

CHELSEA INDUSTRIES (216) 893-0721
1360 Tomahawk
Maumee, OH 43537

SCHUSTER (513) 489-1400
11320 Grooms Road
Cincinnati, OH 45242

SCHUSTER (216) 425-8134
2057D East Aurora Road
Twinsburg, OH 44087

OKLAHOMA

QUALITY COMPONENTS (918) 664-8812
3158 S. 108th East Avenue
Suite 274
Tulsa, OK 74146

OREGON

CYPRESS/RPS (503) 641-2233
15075 S.Koll Parkway
Suite D
Beaverton, OR 97006

PENNSYLVANIA

ALMO ELECTRONICS (215) 698-4003
9815 Roosevelt Blvd.
Philadelphia, PA 19114

CAM/RPC (412) 782-3770
620 Alpha Drive
Pittsburgh, PA 15238

ALMO ELECTRONICS (412) 776-9090
220 Executive Drive
Mars, PA 16046

SOUTH CAROLINA

DIXIE (803) 297-1435
4909 Pelham Road
Greenville, SC 29606

DIXIE (803) 779-5332
1900 Barnwell Street
Columbia, SC 29201

HAMMOND (803) 233-4121
1035 Lowndes Hill Rd.
Greenville, SC 29607

TEXAS

ADDED VALUE (214) 404-1144
4470 Spring Valley Road
Dallas, TX 75244

ADDED VALUE (512) 454-8845
6448 Highway 290 East
#A103
Austin, TX 78723

ALL AMERICAN (214) 231-5300
1819 Firman Drive, #127
Richardson, TX 75081

CYPRESS/RPS (214) 869-1435
2156 W. Northwest Highway
Dallas, TX 75220

SAMSUNG SEMICONDUCTOR DISTRIBUTORS
(Continued)

JACO (214) 235-9575
1209 Glenville Drive
Richardson, TX 75080

MICRO GENESIS (214) 644-5055
9221 LBJ Freeway, #220
Dallas, TX 75243

OMNIPRO (214) 233-0500
4141 Billy Mitchell
Dallas, TX 75244

QUALITY COMPONENTS (214) 733-4300
4257 Kellway Circle
Addison, TX 75244

QUALITY COMPONENTS (713) 240-2255
1005 Industrial Blvd.
Sugar Land, TX 77478

QUALITY COMPONENTS (512) 835-0220
2120-M Braker Lane
Austin, TX 78758

UTAH

ADDED VALUE (801) 975-9500
1836 Parkway Blvd.
West Valley City, UT 84119

VIRGINIA

VIRGINIA ELEC. (804) 296-4184
715 Henry Avenue
Charlottesville, VA 22901

WASHINGTON

CYPRESS/RPS (206) 483-1144
22125 17th Avenue
Suite114
Bothell, WA 98021

JACO (206) 881-9700
15014 N.E. 40th Street
Bldg. "O", Unit 202
Redmond, WA 98052

PRIEBE (206) 881-2363
14807 N.E. 40th
Redmond, WA 98052

WISCONSIN

MARSH (414) 475-6000
1563 S. 101st. Street
Milwaukee, WI 53214

NOTES

NOTES

SAMSUNG
Electronics

Semiconductor Business

HEAD OFFICE:
8/10FL. SAMSUNG MAIN BLDG.
250, 2-KA, TAEPYUNG-RO,
CHUNG-KU, SEOUL, KOREA
C.P.O. BOX 8233
TELEX: KORSST K27970
TEL: (SEOUL) 751-2114
FAX: 753-0967

BUCHEON PLANT:
82-3, DODANG-DONG,
BUCHEON, KYUNGKI-DO, KOREA
C.P.O. BOX 5779 SEOUL 100
TELEX: KORSEM K28390
TEL: (SEOUL) 741-0066, 662-0066
FAX: 741-4273

KIHEUNG PLANT:
SAN #24 NONGSUH-RI, KIHEUNG-MYUN
YONGIN-GUN, KYUNGKI-DO, KOREA
C.P.O. BOX 37 SUWON
TELEX: KORSST K23813
TEL: (SEOUL) 741-0620/7
FAX: 741-0628

GUMI BRANCH:
259, GONDAN-DONG, GUMI,
KYUNGSANGBUK-DO, KOREA
TELEX: SSTGUMI K54371
TEL: (GUMI) 2-2570
FAX: (GUMI) 52-7942

SAMSUNG SEMICONDUCTOR INC.:
3725 NORTH FIRST STREET
SANJOSE, CA 95134-1708, USA
TEL: (408) 434-5400
TELEX: 339544
FAX: (408) 434-5650

HONG KONG BRANCH:
24FL. TOWER 1 ADMIRALTY CENTER
18 HARCOURT ROAD HONG KONG
TEL: 5-8626900
TELEX: 80303 SSTC HX
FAX: 5-8661343

TAIWAN OFFICE:
RM B. 4FL, NO 581
TUN-HWA S, RD, TAPIEI, TAIWAN
TEL: (2) 706-6025/7
FAX: (2) 706-6028

SAMSUNG ELECTRONICS JAPAN CO., LTD.
6F. SUDAMACHI BERDE BLDG.
2-3, KANDA-SUDAMACHI
CHIYODA-KU, TOKYO 101, JAPAN
TELEX: 2225206 SECJPN J
TEL: (03) 258-9506
FAX: (03) 258-9695

SAMSUNG SEMICONDUCTOR EUROPE GMBH:
MERGENTHALER ALLEE 38-40
D-6236 ESCHBORN, W/G
TEL: 0-6196-90090
FAX: 0-6196-900989
TELEX: 4072678 SSED

SAMSUNG (U.K.) LTD.:
SAMSUNG HOUSE 3 RIVERBANK WAY
GREAT WEST ROAD BRENTFORD
MIDDLESEX TW8 9RE
TEL: 862-9312 (EXT) 304
862-9323 (EXT) 292
FAX: 862-0096, 862-0097
TELEX: 25823

PRINTED IN KOREA
JULY, 1989