'77

MITSUBISHI LSI DATA BOOK

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PREFACE

This data book is prepared to provide reference information on Mitsubishi microprocessors, IC memories and LSIs for peripheral circuits.

Mitsubishi has recently completed the development of a new concept in digital computer design. MELPS 8 (Mitsubishi Electric LSI Processor Series 8) is the family name of 8-bit parallel CPU, IC memories and LSIs for their peripheral circuits incorporating these new concepts. The design and manufacture include proprietary technology developed over many years of experience as a leader in the electronics industry.

The MELPS 8 family has been developed with the total system in mind. This has resulted in a form of computer architecture with a built-in high degree of system modularity that will accommodate a large variety of I/O controllers and other commercial applications. A powerful application-oriented instruction set has been incorporated. Most important, however, this approach of total design provides the user the opportunity to substantially reduce system costs while simultaneously expanding operational capabilities.

The MELPS 8 microprocessor M58710S is an 8-bit parallel central processing unit fabricated on a single chip using an N-channel silicon-gate process. While the latest state-of-the-art technology is used in this CPU, it is still compatible with the Intel 8080A in pin configuration, electrical characteristics, timing and software. A description and the specifications of the M58710S microprocessor are included in this data book. The user will find it easy to substitute this CPU in present systems and future systems being developed.

Mitsubishi's new MELPS 8 family represents more than just a continuing commitment to total coordinated hardware and software design. Because it is a full commitment to provide users with cost-effective hardware and a full range of software, the users can easily take full advantage of the powerful MELPS 8 family.

Software must be evaluated along with the hardware when selecting a microprocessor. Savings a user may anticipate if he selects cheap hardware will soon disappear when the cost of developing an application program is added. A full range of software has been developed to assist users in implementing their applications. This includes such aids as simulators, cross compilers, assemblers, cross assemblers and a full subroutine library. The software support has even been extended to automatic design programs to assist in the development of special mask-ROMs made to customers' specifications.

Mitsubishi Electric is a billion dollar high-technology corporation operating world-wide to supply a broad range of products for industries such as communications, information processing, automatic control and aerospace. We pioneered the development of microelectronic devices. Since the introduction of our first MOS ICs in 1968, we have been producing a wide variety of products such as MOS LSIs for desk-top calculators, C-MOS LSIs for wrist watches and 16-digit P-channel silicon gate microprocessors for electric cash registers. Mitsubishi has played a significant role in the evolution of microprocessors for almost a decade.

Microelectronic technology has made giant strides since the introduction of the Intel 8080A. The performance of current devices has improved by magnitudes while the cost is a fraction of that of earlier devices. Manufacturing controls have been developed to increase the reliability of newer devices. The MELPS 8 is an industry leader in performance, reliability and cost because of advanced system architecture, manufacturing experience and quality control. A user would be well advised to consider Mitsubishi for their future needs of microelectronic devices.

Koji Suzaki, Mgr.
Semiconductor Marketing Div.,
Mitsubishi Electric Corp.

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INDEX BY FUNCTION

Type	Alternative designation	Circuit function and organization	Application notes	Structure	Ambient operating temp. Ta (°C)
Microprocessors					
M58710S	8080A	8-Bit Parallel CPU	78 instructions	N, Si	0 ~ 70
Static RAMs					
M58531P		256-Bit (256 × 1) Static RAM		P, Si	−10~75
M58721P ★ M58721S ★★	2101A-4	1024-Bit (256 × 4) Static RAM		N, Si, ED	0 ~ 70
M58722P ★ M58722S ★★	2111A-4	1024-Bit (256 × 4) Static RAM		N, Si, ED	0 ~ 70
M58723P ★ M58723S ★★	2112A-4	1024-Bit (256 × 4) Static RAM		N, Si, ED	0 ~ 70
M58751P ★ M58751S	2102A-4	1024-Bit (1024 × 1) Static RAM		N, Si, ED	0 ~ 70
Dynamic RAMs					
M58533P		1024-Bit (256 × 1) Dynamic RAM		P, Si	0 ~ 70
M58755S-1 ★	2107B	4096-Bit (4096 × 1) Dynamic RAM		N, Si	0 ~ 70
M58755S-2 ★	2107B	4096-Bit (4096 × 1) Dynamic RAM		N, Si	0 ~ 70
M58755S-3 ★	2107B	4096-Bit (4096 × 1) Dynamic RAM		N, Si	0 ~ 70
M58756K ★★ M58756S ★	2104	4096-Bit (4096 × 1) Dynamic RAM		Ni, Si	0 ~ 70
Mask ROMs					
M58730-XXXS		8192-Bit (1024 × 8) Mask-Programmable ROM	Custom product	N, Si	0 ~ 70
M58730-001S		8192-Bit (1024 × 8) Mask-Programmed ROM	Subroutine 1 : integer arithmetic operations	N, Si	0 ~ 70
M58731-XXXP ★★ M58731-XXXS ★	8316	16384-Bit (2048 × 8) Mask-Programmable ROM	Custom product	N, Si, ED	0 ~ 70
M58731-001S ★		1638-Bit (2048 × 8) Mask-Programmed ROM	MELPS 8 basic operating monitor BOM-B	N, Si, ED	0 ~ 70
Field Programmable ROMs					
M58563S ★	1702A	2048-Bit (256 × 8 or 512 × 4) Erasable and Electrically Reprogrammable ROM	512 × 4-bit organization is also possible. Electrical programming, ultraviolet erasing	P, Si, FA	0 ~ 70
M58563S-1 ★	1702A	2048-Bit (256 × 8 or 512 × 4) Erasable and Electrically Reprogrammable ROM	512 × 4-bit organization is also possible. Electrical programming, ultraviolet erasing	P, Si, FA	0 ~ 70
M58651S ★★	2401	4096-Bit (1024 × 4) Electrically Alterable ROM	Electrical programming and erasing	P, Al	0 ~ 70
M54700K ★ M54700P ★ M54700S	6300	1024-Bit (256 × 4) Field Programmable ROM	Ni-Cr fuse programming	B	0 ~ 75
M54730K ★ M54730P ★ M54730S	6330	256-Bit (32 × 8) Field Programmable ROM with Open Collector Outputs	Ni-Cr fuse programming	B	0 ~ 75
Shift Registers					
M58502P		1024-Bit (256 × 4) Dynamic Shift Register		P, Si	−10~75
M58503P		1024-Bit (512 × 2) Dynamic Shift Register		P, Si	−10~75
M58504P		1024-Bit (1024 × 1) Dynamic Shift Register		P, Si	−10~75
LSIs for Peripheral Circuits					
M58609-XXS		Keyboard Encoder	for reed switch, 88 keys, 4 mode shifts 9-bit output	P, Al	−20~75
M58609-04S		Keyboard Encoder (JIS code standard product)		P, Al	−20~75
M58620-XXXS		Keyboard Encoder	for solid-state switch, 91 keys, 4 mode shifts, 10-bit output	P, Al	−20~75
M58620-001S		Keyboard Encoder (JIS code standard product)		P, Al	−20~75
M58740P ★★ M58740S ★	8255	Programmable Peripheral Interface	I/O port for CPU M58710S. 24 I/O pins	N, Si, ED	0 ~75
M54550P ★	8244	Clock Generator and Driver for CPU M58710S	CPU M58710S	B	0 ~75
M54551K ★	8228	System Controller and Bus Driver for CPU M58710S	Bidirectional bus driver for data bus isolation	B, S	0 ~75
M54552P	8212	8-Bit Input/Output Port with Three-State Outputs		B, S	0 ~75

Note 1 ★=New product: ★★=Under development

2 N=N-channel, P=P-channel; Si=Silicon gate, Al=Aluminum gate, ED=Enhancement depletion mode, FA=FAMOS; B=Bipolar S=Schottkey

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Supply voltage				Clock voltage	Electrical characteristics					Package outline	Interchangeable products		Page
V_{DD}	V_{CC}	V_{SS} GND	V_{BB}	$V\phi$	Typ pwr dissipation (mW)	Max access time (ns)	Max cycle time (ns)	Max frequency (MHz)	TTL compatibility		Mfr.	Type	
12V±5%	5V±5%	0V	−5V±5%	V_{DD}±1.0V	780	—	—	2	YES	40S1	INTEL	C8080	4−2
—	−9V±5%	5V±5%	—	—	360	1,500	1,500	—	YES	16P1	INTEL	P1101A	5−3
—	5V±5%	0V	—	—	150	450	450	—	YES	22P1 22S1	INTEL	P2101A-4 C2101A-4	5−27
—	5V±5%	0V	—	—	150	450	450	—	YES	18P1 18S1	INTEL	P2111A-4 C2111A-4	5−31
—	5V±5%	0V	—	—	150	450	450	—	YES	16P1 16S1	INTEL	P2112A-4 C2112A-4	5−35
—	5V±5%	0V	—	—	100	450	450	—	YES	16P1 16S1	INTEL	P2102A-4 C2102A-4	5−13
	0V	16V±5%	V_{SS}+3.5V ±0.5V	16V±5%	270	300	580	—	NO	18P1	INTEL	P1103	5−7
12V±10%	5V±10%	0V	−5V±10%	V_{DD}±1V	300	200	400	—	YES	22S1	INTEL TI	C2107B TMS4060-2	5−17
12V±10%	5V±10%	0V	−5V±10%	V_{DD}±1V	240	270	470	—	YES	22S1	INTEL TI	C2107B-4 TMS4060	5−17
12V±10%	5V±10%	0V	−5V±10%	V_{DD}±1V	350	150	320	—	YES	22S1	INTEL TI	C2107B TMS4060-2	5−17
12V±10%	5V±10%	0V	−5V±10%	2.4V	450	300	425	—	YES	16K1 16S1	INTEL MOSTEK	C2104 4096	5−41
12V±5%	5V±5%	0V	−5V±5%	—	250	850	—	—	YES	24S1	INTEL	C8308	6−3
12V±5%	5V±5%	0V	−5V±5%	—	250	850	—	—	YES	24S1	—	—	6−8
—	5V±5%	0V	—	—	200	850	—	—	YES	24P1 24S1	INTEL	P8316A C8316A	6−9
—	5V±5%	0V	—	—	200	850	—	—	YES	24S1	—	—	6−14
−9V±5%	−9V±5%	5V±5%	Vss	—	300	1,000	1,000	—	YES	24S10	INTEL	C1702A	6−15
−9V±5%	−9V±5%	5V±5%	Vss	—	300	1,500	1,500	—	YES	24S10	INTEL	C1702A-6	6−15
—	−14V±1V	5V±5%	—	$-14V^{+1}_{-5}V$	80	2,000	2,000	—	YES	24S1	NCR	2401	6−20
—	5V±5%	0V	—	—	450	60	60	—	YES	16K1 16P1 16S1	MMI	6300J 6300N 6300	6−26
—	5V±5%	0V	—	—	450	50	50	—	YES	16K1 16P1 16S1	MMI	6330J 6330N 6330	6−31
—	−5V±5%	5V±5%	—	−11V±1V	15	—	—	3†	YES	16P1	INTEL	P1402A	7−3
—	−5V±5%	5V±5%	—	−11V±1V	15	—	—	3†	YES	16P1	—	—	7−3
—	−5V±5%	5V±5%	—	−11V±1V	15	—	—	3†	YES	16P1	—	—	7−3
−12V±1V	0V	5V±10%	—	—	70	—	—	0.1	YES	40B1	GI	AY-5-2376	8−3
−12V±1V	0V	5V±10%	—	—	70	—	—	0.1	YES	40B1	—	—	8−7
−12V±10%	0V	5V±10%	—	—	350	—	—	—	YES	40B1	—	—	8−9
−12V±10%	0V	5V±10%	—	—	350	—	—	—	YES	40B1	—	—	8−14
—	5V±5%	0V	—	—	200	—	—	—	YES	40P1 40S1	INTEL	P8255 C8255	8−17
—	5V±5%	0V	—	—	450	—	—	—	YES	16P1	INTEL	P8224	8−21
—	5V±5%	0V	—	—	550	—	—	—	YES	28K1	INTEL	D8228	8−25
—	5V±5%	0V	—	—	450	25 *	—	—	YES	24P1	INTEL	P8212	8−29

* : Propagation delay time †: Data frequency

INDEX BY TYPE DESIGNATION

Type	Structure	Function	Circuit function	Page
M54550P	B, S	I/O	Clock Generator and Driver for CPU M58710S	8 −21
M54551K	B, S	I/O	System Controller and Bus Driver for CPU M58710S	8 −25
M54552P	B, S	I/O	8-Bit Input/Output Port with Three-State Output	8 −29
M54700P M54700K M54700S	B	PROM	1024-Bit (256 ×4) Field Programmable ROM	6 −26
M54730P M54730K M54730S	B	PROM	256-Bit (32 ×8) Field Programmable ROM with Open Collector Outputs	6 −31
M58502P	P, Si	S/R	1024-Bit (256 ×4) Dynamic Shift Register	7 − 3
M58503P	P, Si	S/R	1024-Bit (512 ×2) Dynamic Shift Register	7 − 3
M58504P	P, Si	S/R	1024-Bit (1024 ×1) Dynamic Shift Register	7 − 3
M58531P	P, Si	RAM	256-Bit (256 ×1) Static RAM	5 − 3
M58533P	P, Si	RAM	1024-Bit (256 ×1) Dynamic RAM	5 − 7
M58563S	P, Si, FA	PROM	2048-Bit (256 ×8 or 512 ×4) Erasable and Electrically Reprogrammable ROM	6 −15
M58563S-1	P, Si, FA	PROM	2048-Bit (256 ×8 or 512 ×4) Erasable and Electrically Reprogrammable ROM	6 −15
M58651S	P, Al	PROM	4096-Bit (1024 ×4) Electrically Alterable ROM	6 −20
M58609-04S	P, Al	I/O	Keyboard Encoder (JIS Code Standard Product)	8 − 7
M58609-XXS	P, Al	I/O	Keyboard Encoder	8 − 3
M58620-001S	P, Al	I/O	Keyboard Encoder (JIS Code Standard Product)	8 −14
M58620-XXXS	P, Al	I/O	Keyboard Encoder	8 − 9
M58710S	N, Si	CPU	8-Bit Parallel CPU	4 − 2
M58721P M58721S	N, Si, ED	RAM	1024-Bit (256 ×4) Static RAM	5 −27
M58722P M58722S	N, Si, ED	RAM	1024-Bit (256 ×4) Static RAM	5 −31
M58723P M58723S	N, Si, ED	RAM	1024-Bit (256 ×4) Static RAM	5 −35
M58730-001S	N, Si	ROM	8192-Bit (1024 ×8) Mask-Programmed ROM	6 − 8
M58730-XXXS	N, Si	ROM	8192-Bit (1024 ×8) Mask-Programmable ROM	6 − 3
M58731-001S	N, Si, ED	ROM	16384-Bit (2048 ×8) Mask-Programmed ROM	6 −14
M58731-XXXP M58731-XXXS	N, Si, ED	ROM	16384-Bit (2048 ×8) Mask-Programmable ROM	6 − 9
M58740P M58740S	N, Si, ED	I/O	Programmable Peripheral Interface	8 −17
M58751P M58751S	N, Si, ED	RAM	1024-Bit (1024 ×1) Static RAM	5 −13
M58755S-1	N, Si	RAM	4096-Bit (4096 ×1) Dynamic RAM	5 −17
M58755S-2	N, Si	RAM	4096-Bit (4096 ×1) Dynamic RAM	5 −17
M58755S-3	N, Si	RAM	4096-Bit (4096 ×1) Dynamic RAM	5 −17
M58756K M58756S	N, Si	RAM	4096-Bit (4096 ×1) Dynamic RAM	5 −41

1

Words	Bits/word			
	1	2	4	8
32				PROMs M54730P/M54730S/ M54730K
256	RAMs M58531P		RAMs M58721P／M58721S M58722P／M58722S M58723P／M58723S PROMs M54700P/M54700S/ M54700K S/Rs M58502P	PROMs M58563S M58563S-1
512		S/Rs M58503P	PROMs M58563S M58563S-1	
1024	RAMs M58751P/M58751S M58533P S/Rs M58504P		EAROMs M58651S	ROMs M58730-XXXS M58730-001S
2048				ROMs M58731-XXXP/ M58731-XXXS M58731-001S
4096	RAMs M58755S-1 M58755S-2 M58755S-3 M58756K M58756S			

GUIDE TO INTERCHANGEABILITIES

Function	Mitsubishi Electric	Circuit organization	Advanced Micro Devices	American Microsystems	Electronic Arrays
CPU	M58710S	8-bit parallel	AM9080A		
Static RAMs	M58531P	256× 1 bit			
	M58721P	256× 4 bit			
	M58721S	256× 4 bit			
	M58722P	256× 4 bit			
	M58722S	256× 4 bit			
	M58723P	256× 4 bit			
	M58723S	256× 4 bit			
	M58751P	1024× 1 bit			
	M58751S	1024× 1 bit		S3102	
Dynamic RAMs	M58533P	1024× 1 bit		S2103	
	M58755S-1	4096× 1 bit		S4021-1	
	M58755S-2	4096× 1 bit			
	M58755S-3	4096× 1 bit		S4021-4	μPD411D-3
	M58756K	4096× 1 bit			
	M58756S	4096× 1 bit		S4096-3	
Mask ROMs	M58730-XXXS	1024× 8 bit			
	M58730-001S	1024× 8 bit			
	M58731-XXXP	2048× 8 bit			
	M58731-XXXS	2048× 8 bit			
	M58731-001S	2048× 8 bit			
Field Programmable ROMs	M58563S	256× 8 or 512× 4 bit FAMOS			
	M58563S-1	256× 8 or 512× 4 bit FAMOS			
	M58651S	1024× 4 bit EAROM			
Fusible PROMs	M54700K	256× 4 bit			
	M54700P	256× 4 bit			
	M54700S	256× 4 bit			
	M54740K	32× 8 bit			
	M54730P	32× 8 bit			
	M54730S	32× 8 bit			
Dynamic Shift Registers	M58502P	256× 4 bit	AM1402A		
	M58503P	512× 2 bit	AM1403A		
	M58504P	1024× 1 bit	AM1404A		
I/O divices	M58609-XXS	Keyboard encoder			
	M58609-04S	Keyboard encoder			
	M58620-XXXS	Keyboard encoder			
	M58620-001S	Keyboard encoder			
	M54550P	Clock generator/driver			
	M54551K	System controller/bus driver			
	M54552P	8-bit I/O port	AM8212		
	M58740P	Programmable periph. interface			
	M58740S	Programmable periph. interface			

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Fairchild Semiconductor	Fujitsu	Hitachi	Intel	Intersil	Monolithic Memories	Mostek
			C8080			
			C1101A	IM7501		MK4007P
		HM45102	P2101A-4			
	MB8101		C2101A-4			
			P2111A-4			
	MB8111		C2111A-4			
			P21112A-4			
	MB8112		C2112A-4			
			P2102A-4	IM7552-1CPE		MK4102P-1
			C2102A-4	IM7552-1CDE		
3524-5	MB8103	HM3503	C1103			MK4006-6P
	MB8107		C2107B			
			C2107B-4			
	MB8108		C2107B			
			D2104			
F4096DC	MB8214		C2104			MK4096
			C8308			
			P8316A			
			C8316A			
	MB8513		C1702A			
			C1702A-6			
					6300N	
					6300	
					6330N	
					6330	
			C1402	IM7702		
				IM7703		
				IM7704		
			P8224			
			D8228			
	MB471		P8212			
			P8255			
			C8255			

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GUIDE TO INTERCHANGEABILITIES

Function	Mitsubishi Electric	Circuit organization	Motorola Semiconductor Products	National Semiconductor	Nippon Electric
CPU	M58710S	8-bit parallel		INS8080A	μPD8080A
Static RAMs	M58531P	256× 1 bit		MM1101AN	μPD402D
	M58721P	256× 4 bit			
	M58721S	256× 4 bit			μPD2101
	M58722P	256× 4 bit			
	M58722S	256× 4 bit			μPD2111
	M58723P	256× 4 bit			
	M58723S	256× 4 bit			
	M58751P	1024× 1 bit			
	M58751S	1024× 1 bit			
Dynamic RAMs	M58533P	1024× 1 bit		MM1103D	μPD404D
	M58755S-1	4096× 1 bit			μPD411D
	M58755S-2	4096× 1 bit	6606L		
	M58755S-3	4096× 1 bit			μPD411D-3
	M58756K	4096× 1 bit			
	M58756S	4096× 1 bit	6604		μPD414D
Mask ROMs	M58730-XXXS	1024× 8 bit			
	M58730-001S	1024× 8 bit			
	M58731-XXXP	2048× 8 bit			
	M58731-XXXS	2048× 8 bit			
	M58731-001S	2048× 8 bit			
Field Programmable ROMs	M58563S	256× 8 or 512× 4 bit FAMOS		MM1702A	
	M58563S-1	256× 8 or 512× 4 bit FAMOS			
	M58651S	1024× 4 bit EAROM			
Fusible PROMs	M54700K	256× 4 bit			
	M54700P	256× 4 bit			
	M54700S	256× 4 bit			
	M54740K	32× 8 bit			
	M54730P	32× 8 bit			
	M54730S	32× 8 bit			
Dynamic Shift Registers	M58502P	256× 4 bit		MM1402A	
	M58503P	512× 2 bit		MM1403A	
	M58504P	1024× 1 bit		MM1404A	
I/O divices	M58609-XXS	Keyboard encoder			
	M58609-04S	Keyboard encoder			
	M58620-XXXS	Keyboard encoder			
	M58620-001S	Keyboard encoder			
	M54550P	Clock generator/driver			μPB8224D
	M54551K	System controller/bus driver			μPB8228D
	M54552P	8-bit I/O port			μPB8212D
	M58740P	Programmable periph. interface			
	M58740S	Programmable periph. interface			μPD8255C

GUIDE TO INTERCHANGEABILITIES

Texas Instruments	Toshiba	Signetics	General Instrument
TMS8080			
	T3374		RA9-1101A
TMS4039			
TMS4042			
TMS4043			
TMS4033	T3382	2602	
		1103	RA9-1103D
TMS4060-2			
TMS4060			
TMS4060-2			
TMS4096			
TMS4700			
			ER2401
		2502	
		2503	
		2504	
			AY-5-2376

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ORDERING INFORMATION AND PACKAGE OUTLINES

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ORDERING INFORMATION

FUNCTION CODE

Mitsubishi integrated circuits may be ordered using a simplified alphanumeric type-code which defines the function of the ICs and the package style.

Example: M 5 87 55 S – 1

- M: Mitsubishi integrated circuit prefix
- Temperature range
  - 5: Standard industrial/commercial (0 to 75°C or −20 to 85°C).
  - 9: High reliability (military)
- Series designation using 1 or 2 alpha-numeric characters.
  - 1 ~ 19: Linear circuit
  - 3: TTL
  - 32 ~ 33: TTL (equivalent to Texas Instruments' SN74 series)
  - 41 ~ 47: TTL
  - 84: CMOS
  - 85: P-channel silicon gate MOS
  - 86: P-channel aluminum gate MOS
  - 87: N-channel silicon gate MOS
  - 9: DTL
  - S32~S33: Schottky TTL (equivalent to Texas Instruments' SN74S series)
- Circuit function identification code using 2 digits.
- Package style
  - B: Resin-sealed ceramic dual in-line (DIL)
  - K: Glass-sealed ceramic dual in-line (DIL)
  - P: Molded plastic dual in-line (DIL)
  - S: Metal-sealed ceramic dual in-line (DIL)
- Electrical characteristic identification code using 1 digit.

PACKAGE CODE

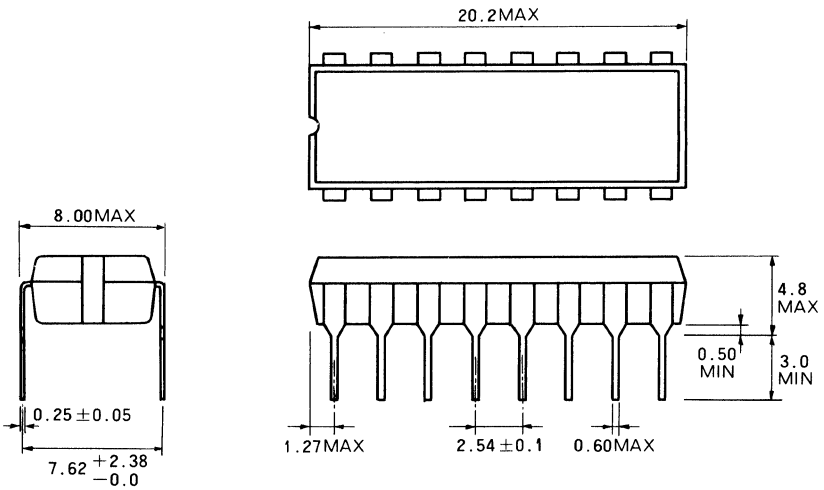
Package style may be specified by using the following simplified alphanumeric code.

Example: 24 P 1

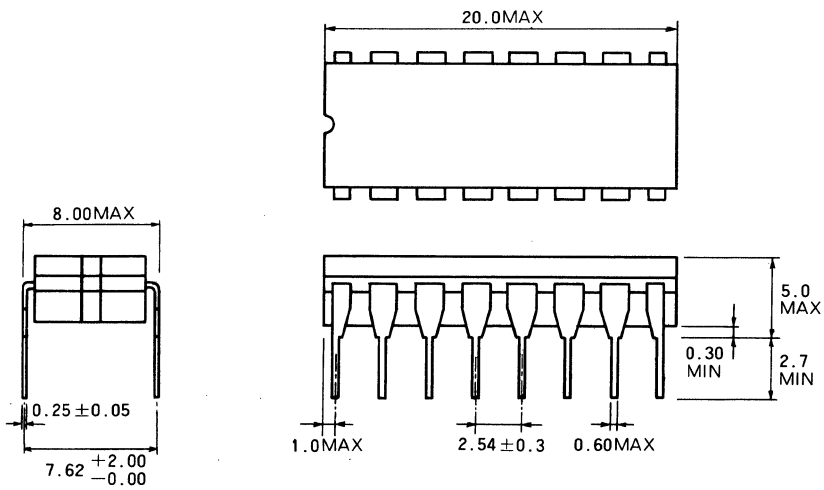
- Number of pins
- Package structure
  - B: Resin-sealed ceramic
  - K: Glass-sealed ceramic
  - P: Molded plastic
  - S: Metal-sealed ceramic
- Package outline
  - 1: DIL without fin
  - 10: DIL without fin and with quartz lid

2

TYPE 16P1 16-PIN MOLDED PLASTIC DIL

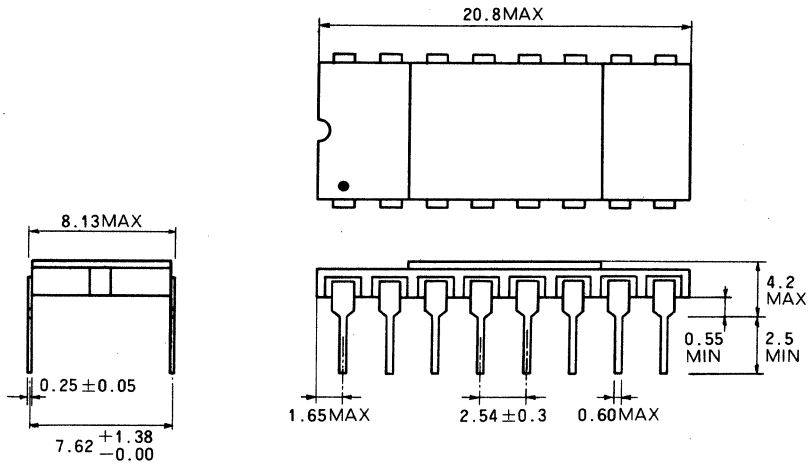


TYPE 16K1 16-PIN GLASS-SEALED CERAMIC DIL

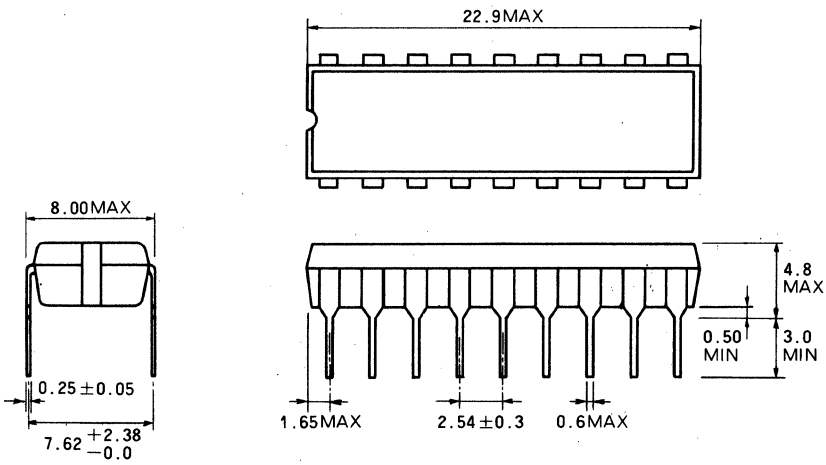


PACKAGE OUTLINES

TYPE 16S1 16-PIN METAL-SEALED CERAMIC DIL



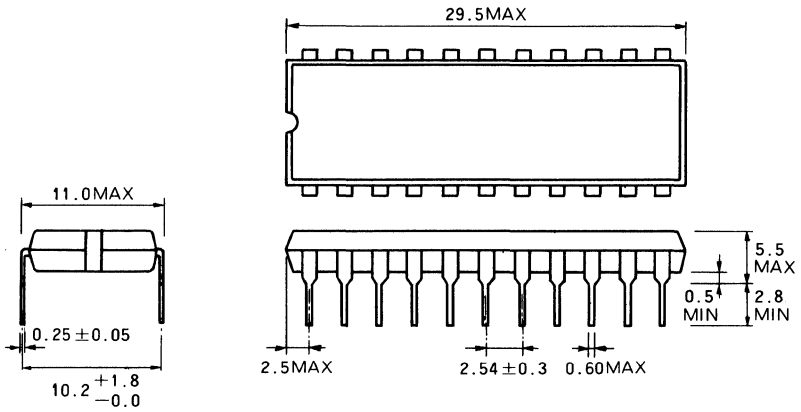
TYPE 18P1 18-PIN MOLDED PLASTIC DIL



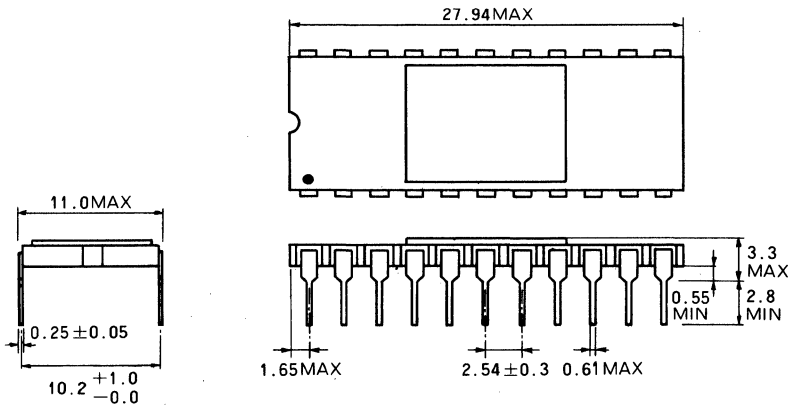
MITSUBISHI ELECTRIC

2

TYPE 22P1 22-PIN MOLDED PLASTIC DIL

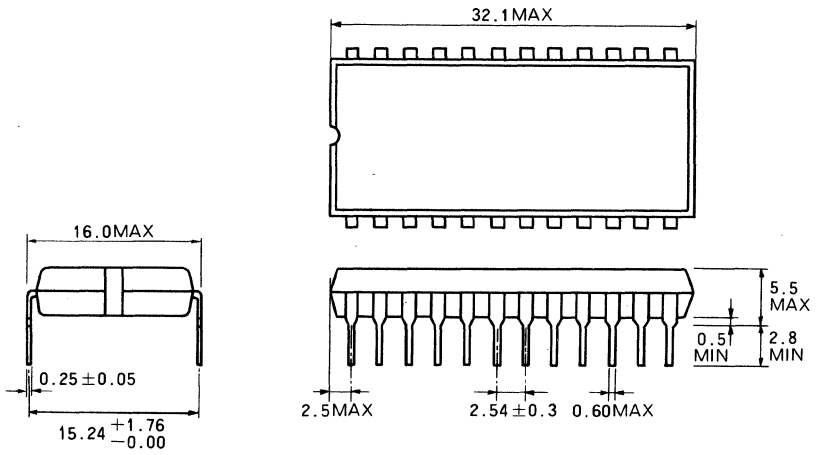


TYPE 22S1 22-PIN METAL-SEALED CERAMIC DIL

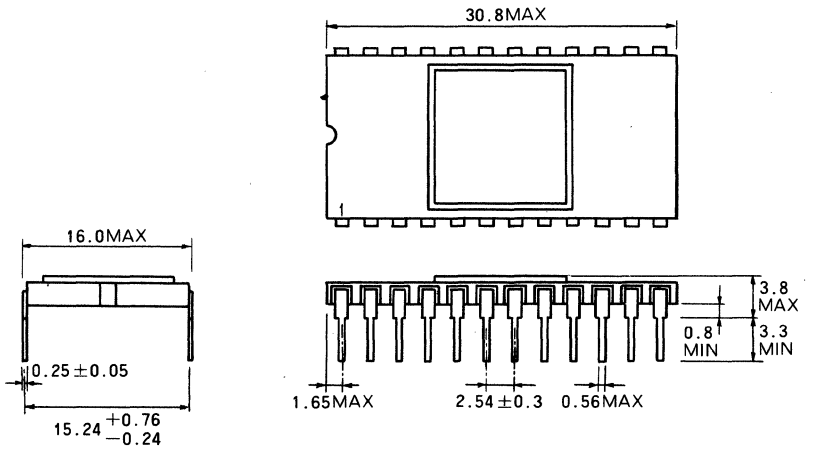


PACKAGE OUTLINES

TYPE 24P1 24-PIN MOLDED PLASTIC DIL



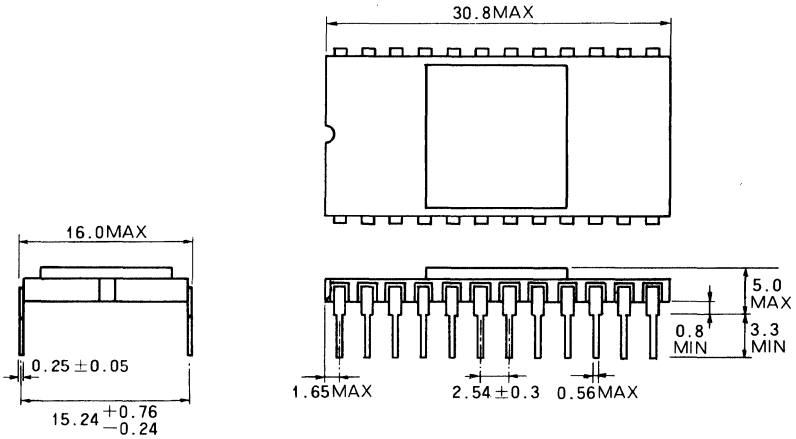
TYPE 24S1 24-PIN METAL-SEALED CERAMIC DIL



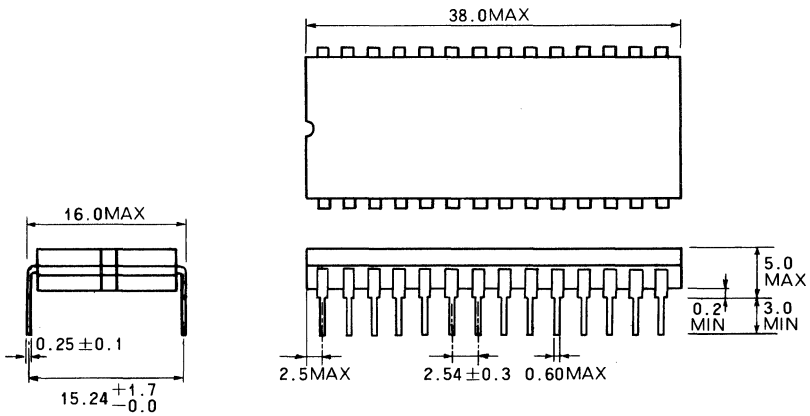
MITSUBISHI ELECTRIC

2

TYPE 24S10 24-PIN METAL-SEALED CERAMIC DIL WITH QUARTZ LID

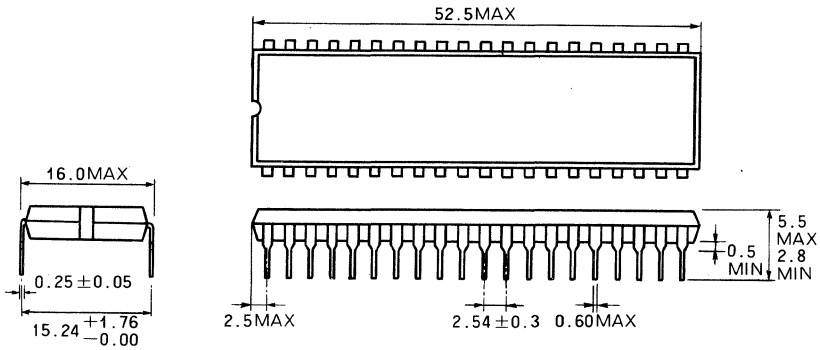


TYPE 28K1 28-PIN GLASS-SEALED CERAMIC DIL

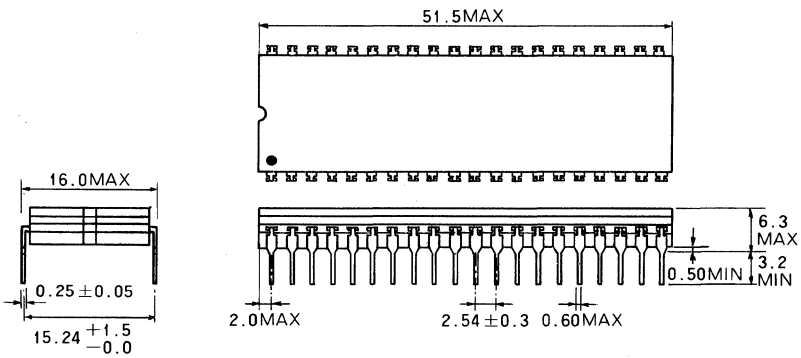


PACKAGE OUTLINES

TYPE 40P1 40-PIN MOLDED PLASTIC DIL



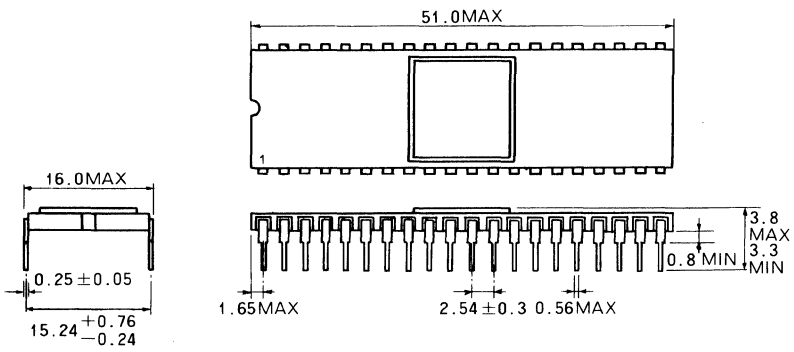
TYPE 40B1 40-PIN RESIN-SEALED CERAMIC DIL



MITSUBISHI ELECTRIC

2

TYPE 40S1 40-PIN METAL-SEALED CERAMIC DIL



GENERAL INFORMATION

3

TERMINOLOGY

GENERAL

Semiconductor A material with resistivity usually in the range between metals and insulators, in which the electrical charge carrier concentration increases with increasing temperature range.

Extrinsic semiconductor A semiconductor with charge carrier concentration dependent upon impurities or other imperfections.

N-type semiconductor An extrinsic semiconductor in which the conduction electron density exceeds the mobile hole density.

P-type semiconductor An extrinsic semiconductor in which the mobile hole density exceeds the conduction electron density.

Junction A region of transition between semiconducting regions of different electrical properties.

PN junction A junction between P- and N-type semiconductor materials.

Depletion layer A region in which the mobile charge carrier density is insufficient to neutralize the net fixed charge density of donors and acceptors.

Breakdown (of a reverse-biased PN junction) A phenomenon, the initiation of which is observed as a transition from a state of dynamic resistance to a state of substantially lower dynamic resistance for increasing the magnitude of a reverse current.

Semiconductor device A device whose essential characteristics are due to the flow of charge carriers within a semiconductor.

Reverse voltage The voltage across a junction or a diode when biased in the direction corresponding to the higher resistance.

Breakdown voltage The reverse voltage at which the reverse current through a junction becomes greater than a specified value.

Case temperature The temperature measured at a specified point on the case of a semiconductor device.

Storage temperature The temperature at which a semiconductor device is stored without any voltage applied.

INTEGRATED CIRCUITS

Microelectronics The concept of the construction and use of highly miniaturized electronic circuits.

Microcircuit A microelectronic device, having a high equivalent circuit-element and/or component density, which is considered as a single unit.

Note: A microcircuit may be a microassembly or an integrated (micro) circuit.

Integrated circuit A circuit in which a number of circuit elements are inseparably associated and electrically interconnected, so that, for the purpose of specification, testing, commerce and maintenance, it is considered indivisible.

Note: For this definition, a circuit element does not have an envelope or external connection and is not specified or sold as a separate item.

Integrated microcircuit A microcircuit in which a number of circuit elements are inseparably associated and electrically interconnected, so that, for the purpose of specification, testing, commerce and maintenance, it is considered indivisible.

Note 1: For this definition, a circuit element does not have an envelope or external connection and is not specified or sold as a separate item.

2: Where no misunderstanding is possible, the term 'integrated microcircuit' may be abbreviated to 'integrated circuit

3: Further qualifying terms may be used to describe the technique used in the manufacture of a specific integrated microcircuit.

Examples of the use of qualifying terms are:

semiconductor monolithic integrated circuit,
semiconductor multichip integrated circuit,
thin film integrated circuit,
thick film integrated circuit,
hybrid integrated circuit.

Microassembly A microcircuit consisting of various components and/or integrated microcircuits which are constructed separately and which can be tested before being assembled and packaged.

Note 1: For this definition, a component has external connections and possibly an envelope as well and it also can be specified and sold as a separate item.

2: Further qualifying terms may be used to describe the form of the components and/or the assembly techniques used in the construction of a specific microassembly.

Examples of use of qualifying terms are:

semiconductor multichip microassembly.
discrete component microassembly.

Integrated electronics The art and technology of the design, fabrication and use of integrated circuits.

Worst-case conditions (for a single characteristic) The values of the applied conditions which individually are chosen from within a specified range and together produce the most unfavorable value for a considered characteristic.

Note: Worst-case conditions for different characteristics may be different.

DIGITAL INTEGRATED CIRCUITS

Digital signal The variation with time of a physical quantity that is used for the transmission of information or for information processing, and that has a finite number of nonoverlapping ranges of values.

Note 1: The physical quantity may be voltage, or current, or impedance, etc.

2: For convenience, each range of values can be represented by a single value—e.g., the nominal value.

Binary signal A digital signal with only two possible ranges of values.

Note: For convenience, each range of values can be represented by a single value.—e.g., the nominal value.

Low range (of a binary signal) The range of least positive (most negative) levels of a binary signal.

Note: This range is often denoted by 'L-range,' and any level in the range by 'L-level.'

High range (of a binary signal) The range of most positive (least negative) levels of a binary signal.

Note: This range is often denoted by 'H-range,' and any level in the range by 'H-level.'

Digital circuit A circuit which is designed to operate by means of digital signals at the input(s) and at the output(s).

Note 1: In this definition, it is understood that 'inputs' and 'outputs' exclude static power supplies.

2: In some digital circuits—e.g., certain types of astable circuits—the inputs need not exist.

Binary circuit A digital circuit designed to operate with binary signals.

Note: The pairs of ranges of values of the binary signals may be different at different terminals.

Input configuration (input pattern) (of a binary circuit) A combination of the L-levels and H-levels at the input terminals at a given instant.

Output configuration (output pattern) (of a binary circuit) A combination of the L-levels and H-levels at the output terminals at a given instant.

Note: When there is no possibility of ambiguity, the output configuration (output pattern) may be represented by the level (expressed as L-level or H-level) of the signal at a stated output terminal of the circuit (the reference output terminal).

Input terminal A terminal by means of which an applied signal may modify the output configuration (output pattern) of the circuit—either directly or indirectly—by modifying the ways in which the circuit reacts to signals at other terminals.

Combinatorial (digital) circuit A digital circuit in which there exists one, and only one, combination of the digital signals at the outputs for each possible combination of digital signals at the inputs.

Sequential (digital) circuit A digital circuit in which there exists at least one combination of the digital signals at the inputs for which there is more than one corresponding combination of the digital signals at the outputs.

Note: These combinations at the outputs are determined by previous history—e.g., as a result of internal memory or delay.

Elementary combinatorial circuit A binary combinatorial (digital) circuit which has only one output terminal, and in which the output signal accepts the value occurring only once in the function if, and only if, the signals applied to all the input terminals are either all in the H-range or all in the L-range.

Note 1: Because the output signal value (occurring only once in the function table) can lie either in the H-range or in the L-range, there are four types of elementary combinatorial circuits.

According to the assignment of the signal values L and H to the binary values 0 and 1 of Boolean algebra, the following logic operations can be realized by means of the four types of elementary combinatorial circuits: AND, OR, NAND, NOR.

2: Nonelementary combinatorial circuits can be formed by combining elementary combinatorial circuits or by combining elementary combinatorial circuits with inverters.

Function table A representation of the necessary or possible relations between the values of the digital signals at the inputs and the outputs of a digital circuit, these values of the digital signals being indicated either by using electrical values directly or by stating the electrical significance of the symbols—e.g., L and H for binary circuits. Generally, every column indicates the values of the digital signals at an input or at an output of the digital circuit; every row indicates the combination of values of the digital signals at the input(s) and the resulting values of the digital signals at the output(s); whenever the value of the digital signal at an output is not determined, it should be indicated by a question mark; whenever the value of a digital signal at an input has no influence, it should be indicated by the symbol L/H or X.

Truth table (for a relation between digital variables) A representation of the logic relationship between one or more independent digital variables and one or more dependent digital variables, by means of a table which, for each possible combination of the values of the independent variables, gives the appropriate values of the dependent variables.

Note: The distinction between 'function table' and 'truth table' is fundamentally necessary, because the same digital circuit may fulfill several different logic operations, according to the arbitrary assignment of the values of the digital variables to the values of the digital electrical quantities.

Input loading factor (of a bipolar digital circuit) A factor which indicates the ratio of the input current of a specified input terminal of a digital circuit to the input current of a particular circuit which is chosen as a reference load.

Note: The reference load should preferably be chosen in such a way that the input loading factor becomes an integer.

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Output loading capability (of a bipolar digital circuit) A factor which indicates the ratio of the maximum output current of a specified output terminal of a digital circuit to the input current of a particular circuit which is chosen as a reference load.

Note: The reference load should preferably be chosen in such a way that the output loading capability becomes an integer.

Excitation An input configuration (input pattern), or change in input configuration (input pattern), that can: cause the circuit to change its output configuration (output pattern), either directly, or in conjunction with an already existing state of preparedness; or put the circuit in a state of preparedness; or either cancel or modify an already existing state of preparedness.

Note 1: The repetition or reiteration of a given excitation will not necessarily produce the same effect.

2: In some cases, an excitation can also maintain an output configuration (output pattern) which it could have produced.

Expander circuit An auxiliary circuit which can be used to expand the number of inputs of equal influence of an associated circuit without modifying the function of the associated circuit.

Binary inverter A binary circuit which has only one input terminal and one output terminal, and in which a signal value L (or H) at the input produces a signal value H (or L) at the output.

Function (sequential) matrix A table having several inputs which gives the possible output configurations for each input configuration(s) and from which the output configuration(s) resulting from a transition from each individual input configuration to any other input configuration can be read directly.

Note: Where appropriate, a function (sequential) matrix may be completed by additional data or details concerning time conditions—e.g., transition times for the input levels, delay time, duration of the input configuration to produce a desired new output configuration.

SEQUENTIAL CIRCUITS

Master-slave arrangement An arrangement of two bistable circuits such that one of them, called the 'slave,' reproduces the output configuration of the other circuit, called the 'master.' The transfer of information from the master to the slave is produced by means of an appropriate signal.

Register An arrangement of bistable circuits by means of which information may be accepted, stored and restituted.

Note: The register may form part of another memory and is of a specified capacity.

Shift Register A register that, by means of an appropriate control signal, can transfer information between consecutive bistable circuits with the sequence being preserved.

Counter A sequential circuit for storing numbers that permits such numbers to be incremented or decremented by a defined constant, including unity.

TIME INTERVALS BETWEEN INPUT SIGNALS

Setup time (t_{su}) (of a digital circuit) The time interval between the application of a signal which is maintained at a specified input terminal and a consecutive active transition at another specified input terminal.

Note 1: The setup time is measured between the instants at which the magnitudes of the two signals pass through specified values within the transition of the signal levels.

2: The setup time is the actual time between two events and may be insufficient to accomplish the setup. A minimum value is specified which is the shortest interval for which correct operation of the digital circuit is guaranteed.

3: The setup time may have a negative value, in which case the minimum limit for which correct operation of the digital circuit is guaranteed defines the longest interval between the active transition and the application of the other signal

Hold time (t_h) (of a digital circuit) The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.

Note 1: The hold time is measured between the instants at which the magnitudes of the two signals pass through specified values within the transitions of the signal levels.

2: The hold time is the actual time between two events and may be insufficient to accomplish the intended result.
A minimum value is specified which is the shortest interval for which correct operation of the digital circuit is guaranteed.

3: The hold time may have a negative value, in which case the minimum limit for which correct operation of the digital circuit is guaranteed defines the longest interval between the change of the signal and the active transition.

Resolution time (t_{res}) (of a digital circuit) The time interval between the cessation of one input pulse and the commencement of the next input pulse applied to the same input terminal.

Note 1: The resolution time is measured between the instants at which the magnitude of the input signal passes through specified values within the transitions of the signal levels.

2: The resolution time is the actual time between two pulses and may be insufficient to ensure that both pulses are recognized. A minimum value is specified which is the shortest interval for which correct operation of the digital circuit is guaranteed.

SWITCHING TIMES OF BINARY CIRCUITS

High-level to low-level (low-level to high-level) propagation time (t_{PHL} and t_{PLH}) The time interval between specified reference points on the input and on the output pulses, when the output is going to the low (high) level and when the device is driven and loaded by typical devices of stated type.

Note: The mean value between the upper limit of the input low range and the lower limit of the input high range is generally used as the specified reference level.

High-level to low-level (low-level to high-level) delay time (t_{DHL} and t_{DLH}) The time interval between specified reference points on the input and on the output pulses, when the output is going to the low (high) level and when the device is driven and loaded by specified networks.

High-level to low-level (low-level to high-level) transition time (t_{THL} and t_{TLH}) The time interval between specified reference points on the edge of the output pulse when the output is going to the low (high) level and when a specified input signal is applied through a specified network and the output is loaded by another specified network.

INTEGRATED CIRCUIT MEMORIES

Memory cell (memory element) The smallest subdivision of a memory into which a unit of data has been or can be entered, in which it is or can be stored, and from which it can be retrieved.

Integrated circuit memory An integrated circuit consisting of memory cells (elements) and usually including associated circuits such as those for address selection, amplifiers, etc.

Read-only memory (ROM) A memory intended to be read only.

Note: Unless otherwise specified, the term 'read-only memory' implies that the content is unalterable, and defined by its structure.

Fixed-programmed read-only memory A read-only memory in which the data contents of each cell (element) are determined during manufacture and are thereafter unalterable.

Mask-programmed read-only memory A fixed-programmed read-only memory in which the data contents of each cell (element) are determined during manufacture by the use of a mask.

Field-programmable read-only memory A read-only memory that, after being manufactured, can have the data content of each memory cell (element) altered.

Programmable read-only memory (PROM) A read-only memory that can have the data content of each memory cell (element) altered once only.

Reprogrammable read-only memory A read-only memory that can have the data content of each memory cell (element) altered more than once.

Read/write memory A memory in which each cell (element) may be selected by applying appropriate electrical input signals, and in which the stored data may be either: a) sensed at appropriate output terminals; or b) changed in response to other similar electrical input signals.

Static read/write memory A memory in which the data are retained in the absence of control signals.

Note 1: The words 'read/write' may be omitted from the term when no misunderstanding will result.
2: A static memory may use dynamic addressing or sensing circuits.

Dynamic read/write memory A memory in which the cells (elements) require the repetitive application of control signals in order to retain the data stored.

Note 1: The words 'read/write' may be omitted from the term when no misunderstanding will result.
2: Such repetitive application of the control signals is normally called a refresh operation.
3: A dynamic memory may use static addressing or sensing circuits.
4: This definition applies whether the control signals are generated inside or outside the integrated circuit.

Volatile memory A memory whose data content is lost when the power supply is disconnected.

Random-access memory (RAM) A memory that permits access to any of its address locations in any desired sequence.

MICROPROCESSOR INTEGRATED CIRCUITS

Microprocessor integrated circuit An integrated circuit capable of:

1. Accepting coded instructions at one or more terminals.
2. Carrying out, in accordance with the instructions received, all of:
   a. the acceptance of coded data for processing and/or storage;
   b. arithmetic and logical operations on the input data together with any relevant data stored in the microprocessor integrated circuit;
   c. the delivery of coded data.
3. Accepting and/or delivering signals controlling and/or describing the operation or state of the microprocessor integrated circuit.

Note: The instructions may be fed in, built in, or held in an internal store.

Note: The definitions of terms described here are extracted from IEC publication 147-0. Some of the terms for integrated circuit memories and microprocessors are under consideration.

FOR DIGITAL INTEGRATED CIRCUITS

Symbol	Parameter—definition
C_i	Input capacitance
C_o	Output capacitance
$C_{i/o}$	Input/output terminal capacitance
$C_{i(\phi)}$	Input capacitance of clock input
f	Frequency
$f(\phi)$	Clock frequency
I	Current—the current into an integrated circuit terminal is defined as a positive value and the current out of a terminal is defined as a negative value
I_{BB}	Supply current from V_{BB}
$I_{BB(AV)}$	Average supply current from V_{BB}
I_{CC}	Supply current from V_{CC}
$I_{CC(AV)}$	Average supply current from V_{CC}
$I_{CC(PD)}$	Power-down supply current from V_{CC}
I_{DD}	Supply current from V_{DD}
$I_{DD(AV)}$	Average supply current from V_{DD}
I_{GG}	Supply current from V_{GG}
$I_{GG(AV)}$	Average supply current from V_{GG}
I_I	Input current
I_{IH}	High-level input current—the value of the input current when V_{OH} is applied to the input considered
I_{IL}	Low-level input current—the value of the input current when V_{OL} is applied to the input considered
I_{OH}	High-level output current—the value of the output current when V_{OH} is applied to the output considered
I_{OL}	Low-level output current—the value of the output current when V_{OL} is applied to the output considered
I_{OZ}	Off-state (high-impedance-state) output current—the current into an output having a three-state capability with input conditions so applied that it will establish, according to the product specification, the off (high-impedance) state at the output
I_{OZH}	Off-state (high-impedance-state) output current, with high-level voltage applied to the output
I_{OZL}	Off-state (high-impedance-state) output current, with low-level voltage applied to the output
I_{OS}	Short-circuit output current
I_{SS}	V_{SS} supply current
P_d	Power dissipation
R_I	Input resistance
R_L	External load resistance
R_{OFF}	Off-state output resistance
R_{ON}	On-state output resistance
t_a	Access time—the time interval between the application of a specified input pulse during a read cycle and the availability of valid data signals at an output
$t_{a(AD)}$	Address access time—the time interval between the application of an address input pulse and the availability of valid data signals at an output
$t_{a(CE)}$	Chip enable access time
$t_{a(CS)}$	Chip select access time
t_c	Cycle time
$t_{c(REF)}$	Refresh cycle time—the time interval between successive signals that are intended to restore the level in a dynamic memory cell to its original level
$t_{c(RD)}$	Read cycle time—the time interval between the start of a read cycle and the start of the next cycle
$t_{c(RMW)}$	Read-modify-write cycle time—the time interval between the start of a cycle in which the memory is read and new data are entered, and the start of the next cycle
$t_{c(WR)}$	Write cycle time—the time interval between the start of a write cycle and the start of the next cycle
$t_{dv(AD)}$	Data valid time with respect to address—the time interval following an initial change of address during which data stored at the initial address continues to be valid at the output
$t_{dv(CE)}$	Data valid time with respect to chip enable—the time interval following chip enable during which output data continues to be valid
$t_{dv(CS)}$	Data valid time with respect to chip select—the time interval following chip select during which output data continues to be valid
t_d	Delay time—the time between the specified reference points on two pulses
$t_{d(\phi)}$	Delay time between clock pulses—e.g., symbology: delay time, clock 1 to clock 2 or clock 2 to clock 1
t_{DHL}	High-level to low-level delay time—the time interval between specified reference points on the input and on the output pulses, when the output is going to
t_{DLH}	Low-level to high-level delay time—the low (high) level and when the device is driven and loaded by specified networks
t_f	Fall time
t_h	Hold time—the time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal
$t_{h(AD)}$	Address hold time
$t_{h(CE)}$	Chip enable hold time
$t_{h(CS)}$	Chip select hold time
$t_{h(DA)}$	Data hold time

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Symbol	Parameter—definition
$t_{h(RD)}$	Read hold time
$t_{h(WR)}$	Write hold time
t_{PHL}	High-level to low-level propagation time—the time interval between specified reference points on the input and on the output pulses when the output is
t_{PLH}	Low-level to high-level propagation time—the going to the low (high) level and when the device is driven and loaded by typical devices of stated type
t_r	Rise time
t_{su}	Setup time—the time interval between the application of a signal which is maintained at a specified input terminal and a consecutive active transition at another specified input terminal
$t_{su(AD)}$	Address setup time
$t_{su(AD\text{-}WR)}$	Address setup time with respect to write
$t_{su(CE\text{-}P)}$	Chip enable setup time with respect to precharge
$t_{su(CS)}$	Chip select setup time
$t_{su(CS\text{-}WR)}$	Chip select setup time with respect to write
$t_{su(DA)}$	Data setup time
$t_{su(P\text{-}CE)}$	Precharge setup time with respect to chip enable
$t_{su(RD)}$	Read setup time
$t_{su(WR)}$	Write setup time
t_{THL}	High-level to low-level transition time—the time interval between specified reference points on the edge of the output pulse when the output is going to
t_{TLH}	Low-level to high-level transition time—the low (high) level and when a specified input signal is applied through a specified network and the output is loaded by another specified network
t_w	Pulse width—the time interval between specified reference points on the leading and trailing edges of the waveforms
$t_{w(CE)}$	Chip enable pulse width
$t_{w(CEH)}$	Chip enable high pulse width
$t_{w(CEL)}$	Chip enable low pulse width
$t_{w(CS)}$	Chip select pulse width
$t_{w(RD)}$	Read pulse width
$t_{w(WR)}$	Write pulse width
$t_{w(\phi)}$	Clock pulse width
t_{wr}	Write recovery time—the time interval between the termination of a write pulse and the initiation of a new cycle
T_a	Ambient temperature
T_{opr}	Operating temperature
T_{stg}	Storage temperature
V_{BB}	V_{BB} supply voltage
V_{CC}	V_{CC} supply voltage
V_{DD}	V_{DD} supply voltage
V_{GG}	V_{GG} supply voltage
V_I	Input voltage
V_{IH}	High-level input voltage—the value of the permitted high-state voltage at the input
V_{IL}	Low-level input voltage—the value of the permitted low-state voltage range at the input
V_O	Output voltage
V_{OH}	High-level output voltage—the value of the guaranteed high-state voltage range at the output
V_{OL}	Low-level output voltage—the value of the guaranteed low-state voltage range at the output

Note: The symbols shown here are, with some exceptions, extracted from IEC publication 148.

QUALITY ASSURANCE AND RELIABILITY TESTING

1. PLANNING

In recent years, advances in integrated circuits have been rapid, with increasing density and speed accompanied by decreasing cost. Because of these advances, it is now practical and economically justifiable to use these devices in systems of greater complexity and in which they were previously considered too expensive. All of these advances add up to increased demand.

We at Mitsubishi foresaw this increased demand and organized our production facilities to meet it. We also realized that simply increasing production to meet the demand was not enough and that positive steps would have to be taken to assure the reliability of our products.

This realization resulted in development of our Quality Assurance System. The system has resulted in improved productus, and Mitsubishi is able to supply its customers' needs with ICs of high reliability and stable quality. This system is the key to future planning for improved design, production and quality assurance.

2. QUALITY ASSURANCE SYSTEM

The Quality Assurance System imposes quality controls on Mitsubishi products from the initial conception of a new product to the final delivery of the product to the customer. A diagram of the total system is shown in Fig. 1. For ease of understanding, the system is divided into three stages.

2.1 Quality Assurance in the Design Stage

The characteristics of the bread-board devices are carefully checked to assure that all specifications are met. Standard integrated circuits and high-quality discrete components are used. During the design stage, extensive use is made of a sophisticated CAD program, which is updated to always include the latest state-of-the-art techniques.

2.2 Quality Assurance in the Limited-Manufacturing Stage

Rigid controls are maintained on the environment, incoming material and manufacturing equipment such as tools and test equipment. The products and materials used are subjected to stringent tests and inspections as they are manufactured. Wafer production is closely monitored.

Finally, a tough quality assurance test and inspection is made before the product is released for delivery to a customer. This final test includes a complete visual inspection, and electrical characteristics tests. A sampling technique is used to conduct tests under severe operating conditions to assure that the products meet reliability specifications. Pictures of some of the test equipment used are shown in Figs. 2 ~ 5.

2.3 Quality Assurance in the Full Production Stage

Full production of a product is not started until it has been confirmed that it can be manufactured to meet quality and reliability specifications. The controls, tests and inspection procedures developed in §2.2 are continued. The closest monitoring assures that they are complied with.

3. RELIABILITY CONTROL

3.1 Reliability Tests

The newly established Reliability Center for Electronic Components of Japan has established a qualification system for electronic components. Reliability test methods and procedures are developed to mainly meet MIL-STD-883 and EIAJ-IC-121 specifications. Details of typical tests used on Mitsubishi ICs are shown in Table 1.

Table 1 Typical reliability test items and conditions

Group	Item	Test condition
1	High temperature operating life	Maximum operating ambient temperature 1000h
	High temperature storage life	Maximum storage temperature 1000h
	Humidity (steady state) life	65°C 95%RH 500h
2	Soldering heat	260°C 10s
	Thermal shock	0~100°C 15 cycles, 10min/cycle
	Temperature cycle	Minimum to maximum storage temperature, 10 cycles of 1h/cycle
3	Soldering	230°C, 5s, use rosin flux
	Lead integrity	Tension: 340g 30s Bending stress: 225g, ±30°, 3 times
	Vibration	20G, X, Y, Z each direction, 4 times 100~2000Hz—4 min/cycle
	Dropping	75cm, 3 times, wood plate, Y_1 direction
	Constant acceleration	20000G, Y_1 direction, 1 min

3.2 Failure Analysis

Devices that have failed during reliability or acceleration tests are analyzed to determine the cause of failure. This information is fed back to the process engineering section and manufacturing section so that improvements can be made to increase reliability. A summary of failure analysis procedures is shown in Table 2.

Table 2 Summary of failure analysis procedures

Step	Description
1. External examination	O Inspection of leads, plating, soldering and welding O Inspection of materials, sealing and package marking O Visual inspection of other items of the specifications O Use of stereo microscopes, metallurgical microscopes, X-ray photographic equipment, fine leakage and gross leakage testers in the examination
2. Electrical tests	O Checking for open circuits, short circuits and parametric degradation by electrical parameter measurement O Observation of characteristics by a synchroscope or a curve tracer and checking of important physical characteristics by electrical characteristics O Stress tests such as environmental or life tests, if required
3. Internal examination	O Removal of the cover of the device, the optical inspection of the internal structure of the device O Checking of the silicon chip surface O Measurement of electrical characteristics by probes, if applicable O Use of SEM, XMA and infrared microscanner if required
4. Chip analysis	O Use of metallurgical analysis techniques to supplement analysis of the internal examination O Slicing for cross-sectional inspection O Analysis of oxide film defects O Analysis of diffusion defects

QUALITY ASSURANCE AND RELIABILITY TESTING

Fig. 1 Quality assurance system

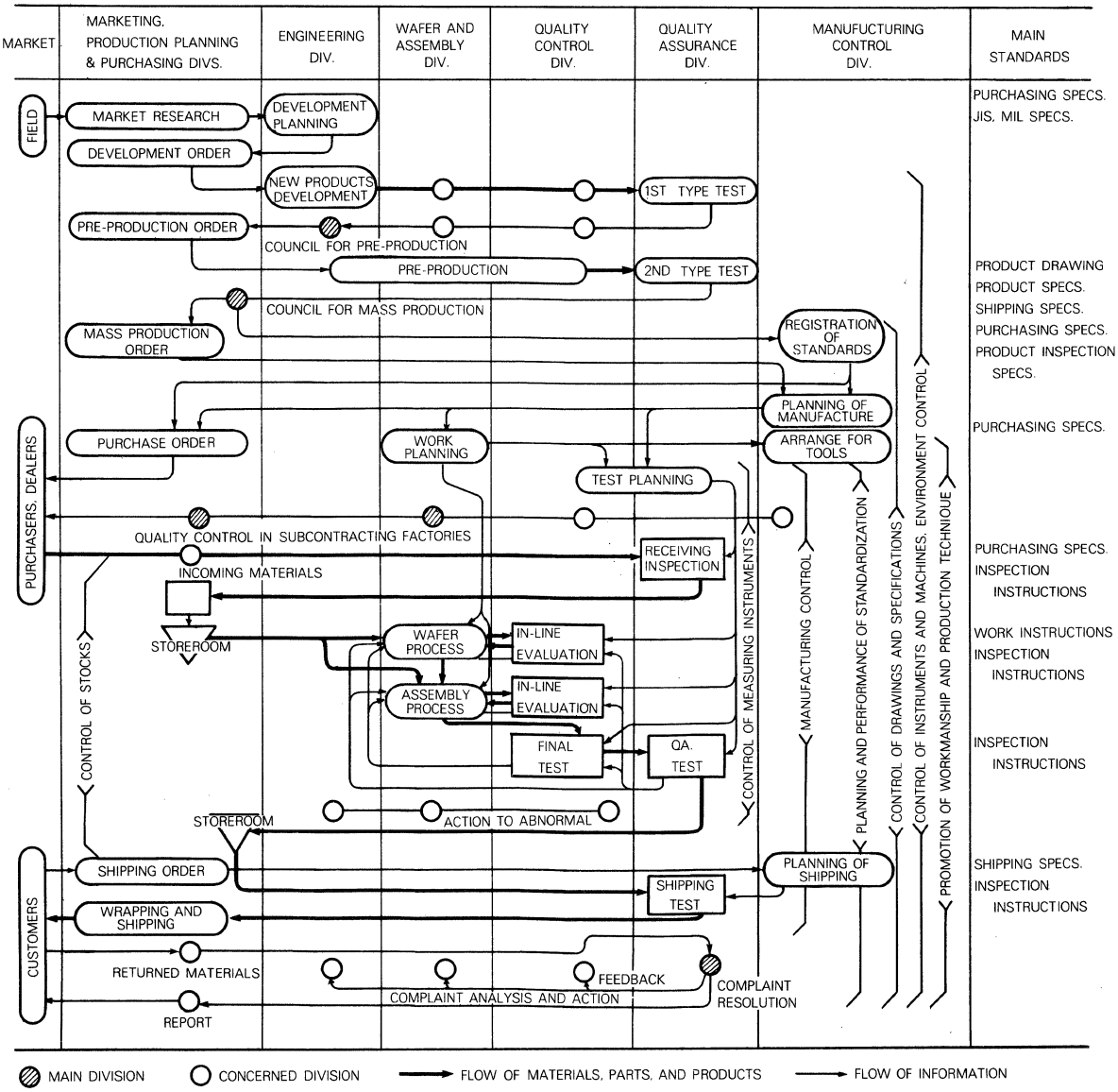


Fig. 2 Large-scale test system for LSIs

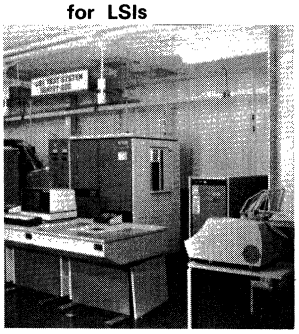


Fig. 3. Monitored temperature cycling tester

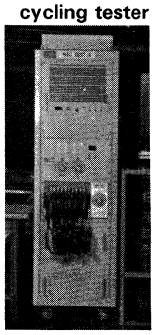


Fig. 4 Helium leakage tester

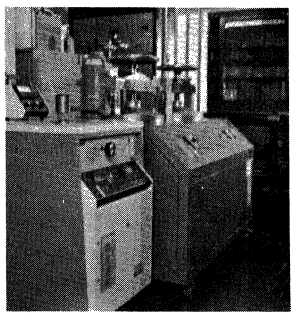
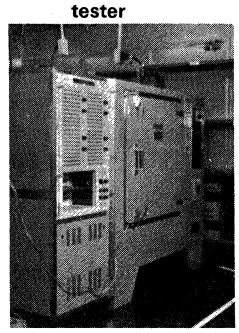


Fig. 5 Operating life tester



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4. TYPICAL RESULTS OF RELIABILITY TESTS AND FAILURE ANALYSES

4.1 Results of Reliability Test

Formerly, sufficient reliability for memory MOS LSIs was obtained by using metal-sealed ceramic packages, but with the development of high reliability plastic molding technology, production has been shifted to plastic molded memory MOS LSIs.

The following tests were performed:

1. Operating life test: Durability is tested at high temperature under operating state conditions by applying clock pulse inputs as shown in Fig. 6.
2. DC biased test: Durability is tested at high temperature biasing DC voltage, as shown in Fig. 7.
3. High temperature storage: The durability of devices stored at high temperatures is tested.

Typical results of memory MOS LSI life tests are shown in Table 3. The failure rate computed from this reliability data using an appropriate acceleration factor is 0.1 FIT or less (1 FIT=10^{-9}/hour) per bit, about the same as, or less than, for core memories.

Fig. 6 Operating life test procedure (for M58755 4K-bit dynamic RAM)

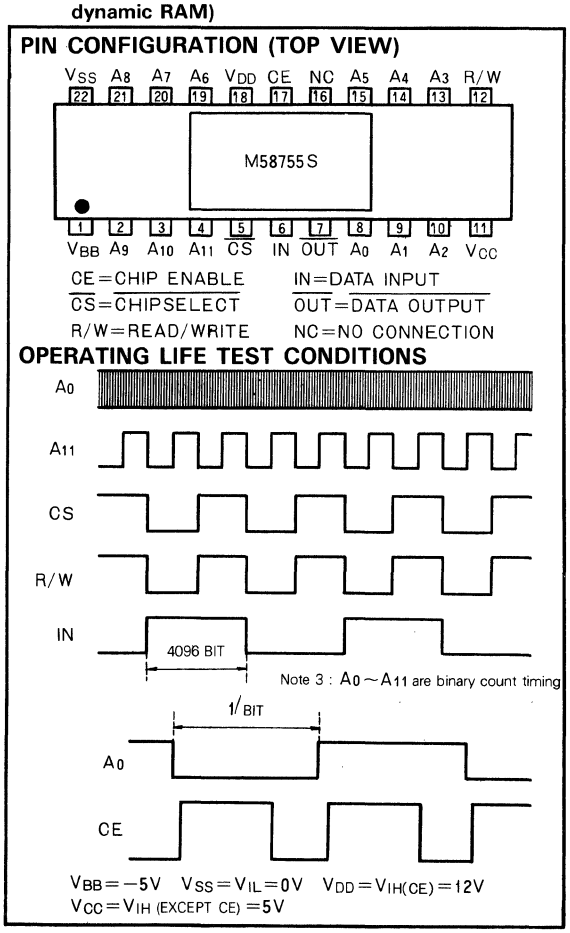


Fig. 7 DC biased test procedure (for M58751 1K-bit static RAM)

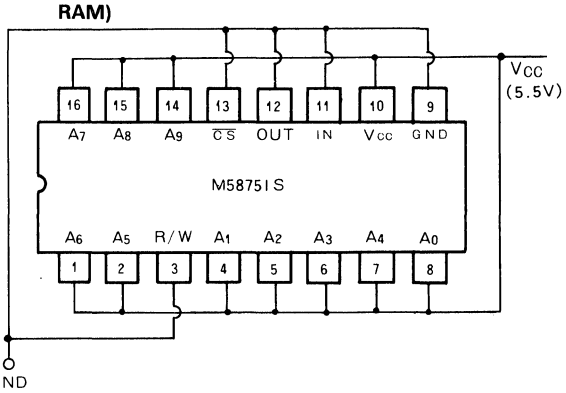


Table 3 Typical results of memory MOS LSI life tests

Type number	Package	Test	Temp. °C	No. of samples	Component hours	No. of failures	Remarks
M58533S	28-pin metal-sealed ceramic DIL	Operating life	55°C	38	114,000	0	
			80°C	20	20,000	0	
			125°C	15	15,000	0	
		DC biased	80°C	20	20,000	0	
			125°C	15	20,000	0	
		High temp. stg.	150°C	38	15,000	0	
M58533P	28-pin plastic molded DIL	Operating life	80°C	20	20,000	0	Functional
			125°C	55	74,000	1	failure
		DC biased	80°C	20	20,000	0	
			125°C	40	60,000	0	
		High temp. stg.	150°C	30	30,000	0	
M58531P	16-pin plastic molded DIL	Operating life	80°C	20	20,000	0	
			125°C	20	20,000	0	
		DC biased	80°C	20	20,000	0	
			125°C	20	20,000	0	
		High temp. stg.	150°C	50	50,000	0	
M58751P	16-pin plastic molded DIL	Operating life	80°C	40	80,000	0	
			125°C	120	160,000	0	
		DC biased	125°C	40	80,000	0	
		High temp. stg.	150°C	5	5,000	0	
			200°C	5	5,000	0	
M58755S	22-pin ceramic DIL	Operating life	80°C	39	88,000	0	Functional
			125°C	149	271,000	1	failure (at 240h)
		DC biased	125°C	66	137,000	0	
					Total	2	

4.2 Typical Results of Failure Analyses

Accelerated testing under conditions more severe than normal operating conditions is used to observe failures of moisture resistance, of wire bonding, of surge voltage destruction and of vapor-deposited aluminum interconnection. Typical results are shown below.

4.2.1. Failure in Moisture Resistance

An example of the results of steam pressure testing, performed to evaluate the moisture resistance of a plastic molded package, is shown in Fig. 8. The vapor-deposited aluminum interconnection was corroded due to moisture penetration.

4.2.2. Failure of Wire Bonding

An example of a failure during the monitored temperature cycling test for evaluating the reliability of the wire bonding of the inner leads of the IC is shown in Fig. 9. The cause of this failure may have been the opening of the inner lead bonding because of a difference in thermal expansion coefficients of metal and resin producing a stress on the inner lead.

4.2.3. Failure Due to Surge Voltage

Many integrated circuits fail in the field due to a surge voltage. Surge voltage marginal tests have been performed to reproduce this failure for analysis of the destruction.

Examples of failures during this test are shown in Figs. 10 ~ 13. Figs. 10 and 11 indicate the existence of a bridge that was confirmed by an X-ray microanalyzer. Figs. 12 and 13 indicate the existence of a hot spot that was confirmed by an infrared microscanner.

4.2.4. Failure of Vapor-Deposited Interconnections

Fig. 14 shows an open-circuit vapor-deposited aluminum interconnection, at a high current density region, caused by the operating life test. This test is performed as a step stress test to investigate IC degradation and failure by temperature and voltage. This phenomenon is due to aluminum electromigration, which is observed when high-current loads are applied to a vapor-deposited aluminum interconnection.

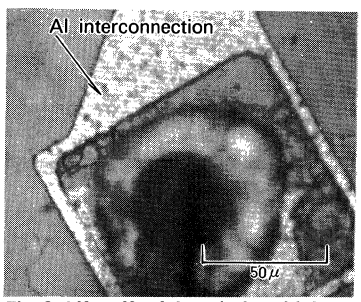


Fig. 8 Corrosion of vapor-deposited aluminum interconnection, analyzed by metallurgical microscope

5. CONCLUSION

Mitsubishi Electric's Quality Assurance System is being expanded to provide stronger emphasis on the following points:

1. Establishment of quality and reliability levels that satisfy customers' requirements.
2. Expansion of the reliability tests of wafers and assembly processes for better evaluation, and standardization of circuit and design rules.
3. Establishment of procedures for speeding up the introduction of new technology and improved methods that raise reliability and to improve the accelerated life tests for better failure analysis.
4. Establishment of a system for collecting data on failures in the field, which will then be analyzed to develop improved methods for increasing reliability.

We welcome and appreciate the cooperation of our customers in developing design specifications, establishing quality levels, controlling incoming inspections, developing assembly and adjusting processes and collecting field data. Mitsubishi is anxious to work with its customers to develop ICs of increased reliability that meet their requirements.

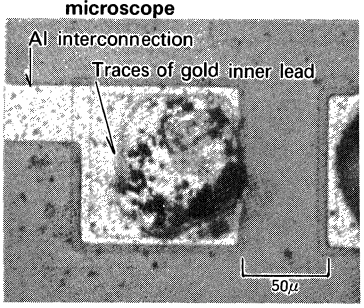


Fig. 9 Lift off of bonded gold inner lead, analyzed by metallurgical microscope

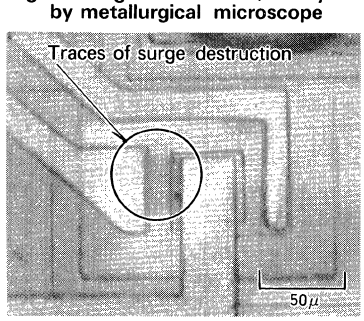


Fig. 10 Surge destruction, analyzed by metallurgical microscope

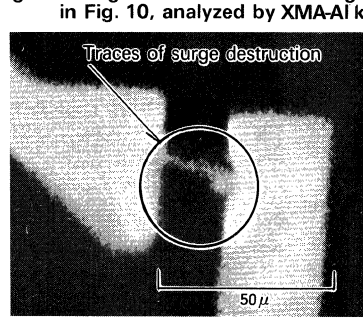


Fig. 11 Enlargement of aluminum bridge in Fig. 10, analyzed by XMA-Al kα

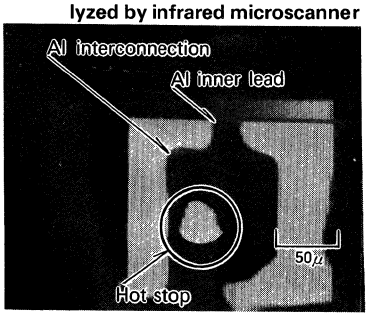


Fig. 12 Hot spot at bonding head, analyzed by infrared microscanner

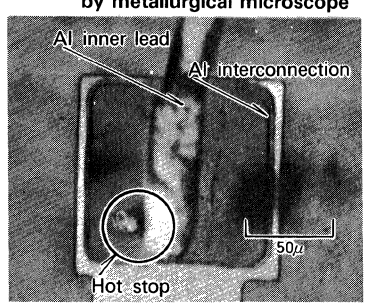


Fig. 13 Junction in Fig. 12 after removal of aluminum, analyzed by metallurgical microscope

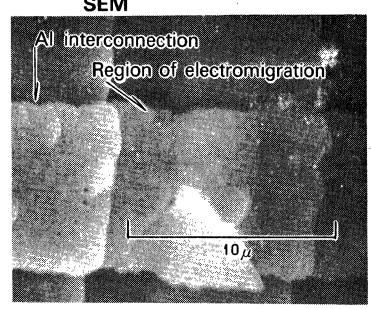


Fig. 14 Electromigration of aluminum interconnection, analyzed by SEM

PRECAUTIONS IN HANDLING MOS ICs

A MOS transistor has a very thin oxide insulator under the gate electrode on the silicon substrate. It is operated by altering the conductance (g_m) between source and drain to control mobile charges in the channel formed by the applied gate voltage.

If a high voltage were applied to a gate terminal, the insulator-film under the gate electrode could be destroyed, and all Mitsubishi MOS IC/LSIs contain internal protection circuits at each input terminal to prevent this. It is inherently necessary to apply reverse bias to the P-N junctions of a MOS IC/LSI.

Under certain conditions, however, it may be impossible to completely avoid destruction of the thin insulator-film due to the application of unexpectedly high voltage or thermal destruction due to excessive current from a forward biased P-N junction. The following recommendations should be followed in handling MOS devices.

1. KEEPING VOLTAGE AND CURRENT TO EACH TERMINAL BELOW MAXIMUM RATINGS

1. The recommended ranges of operating conditions provide adequate safety margins. Operating within these limits will assure maximum equipment performance and quality.
2. Forward bias should not be applied to any terminal since excessive current may cause thermal destruction.
3. Output terminals should not be connected directly to the power supply. Short-circuiting of a terminal to a power supply having low impedance may cause burn-out of the internal leads or thermal destruction due to excessive current.

2. KEEPING ALL TERMINALS AT THE SAME POTENTIAL DURING TRANSPORT AND STORAGE

When MOS IC/LSIs are not in use, both input and output terminals can be in a very high impedance state so that they are easily subjected to electrostatic induction from AC fields of the surrounding space or from charged objects in their vicinity. For this reason, MOS IC/LSIs should be protected from electrostatic charges while being transported and stored by conductive rubber-foam, aluminum foil, shielded boxes or other protective precautions.

3. KEEPING ELECTRICAL EQUIPMENT, WORK TABLES AND OPERATING PERSONNEL AT THE SAME POTENTIAL

1. All electric equipment, work table surfaces and operating personnel should be grounded. Work tables should be covered with copper or aluminum plates of good conductivity, and grounded. One method of grounding personnel, after making sure that there is no potential difference with electrical equipment, is by the use of a wristwatch metallic ring, etc. attached around the wrist and grounded in series with a 1M Ω resistor. Be sure that the grounding meets national regulations on personnel safety.
2. Current leakage from electric equipment must be prevented not only for personnel safety, but also to avert the destruction of MOS IC/LSIs, as described above. Items such as testers, curve-tracers and synchroscopes must be checked for current leakage before being grounded.

4. PRECAUTIONS FOR MOUNTING OF MOS IC/LSIs

1. The printed wiring lines to input and output terminals of MOS IC/LSIs should not be close to or parallel to high-voltage or high-power signal lines. Turning power on while the device is short-circuited, either by a solder bridge made during assembly or by a probe during adjusting and testing, may cause maximum ratings to be exceeded, which may result in the destruction of the device.
2. When input/output, or input and/or output, terminals of a MOS IC/LSIs (now open-circuits) are connected, we must consider the possibility of current leakage and take precautions similar to §2 above. To reduce such undesirable trouble, it is recommended that an interface circuit be inserted at the input or output terminal, or a resistor with a resistance that does not exceed the output driving capability of the MOS IC/LSI be inserted between the power supply and the ground.
3. A filter circuit should be inserted in the AC power supply line to absorb surges which can frequently be strong enough to destroy a MOS IC/LSI.
4. Terminal connections should be made as described in the catalog while being careful to meet specifications.
5. Ungrounded metal plates should not be placed near input or output terminals of any MOS IC/LSIs, since destruction of the insulation may result if they become electrostatically charged.
6. Equipment cases should provide shielding from electrostatic charges for more reliable operation. When a plastic case is used, it is desirable to coat the inside of the case with conductive paint and to ground it. This is considered necessary even for battery-operated equipment.

MICROPROCESSORS

4

M58710S

Alternative Designation 8080A

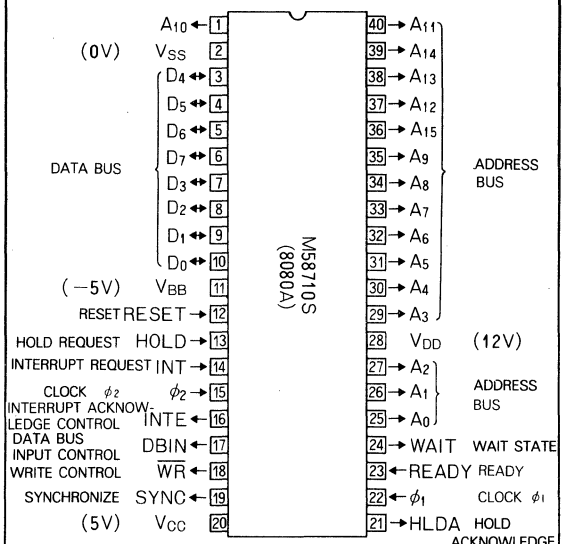
8-BIT PARALLEL CPU

The M58710S is an 8-bit parallel central processing unit (CPU) fabricated on a single chip using a high-speed N-channel silicon-gate MOS process, in a ceramic DIL package.

FEATURES

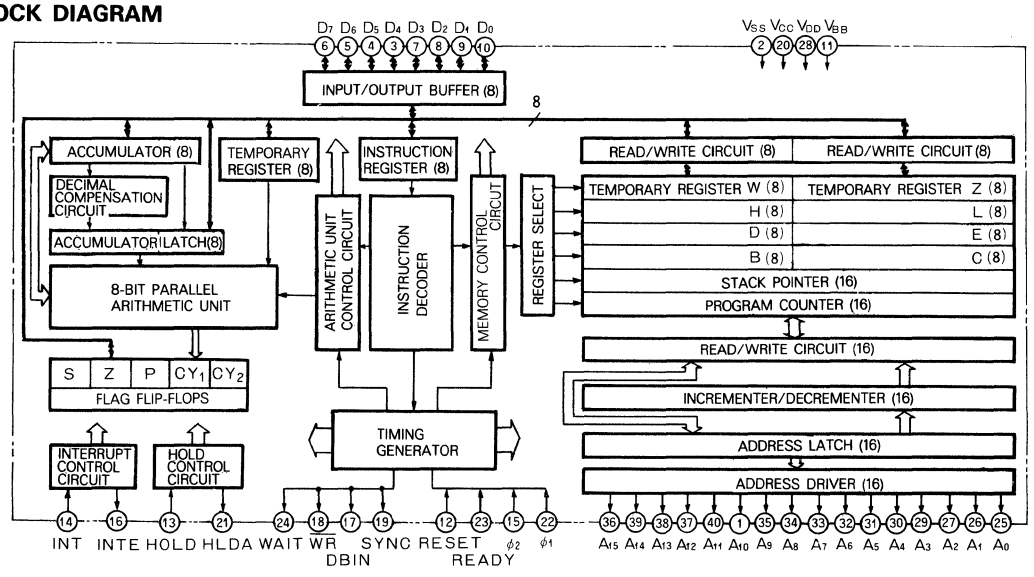
- Basic machine instructions: 78
- Execution time (at clock frequency 2MHz): 2μs
- Directly accessible memory capacity: 65536 bytes
- Number of input/output ports: 256 each
- Multi-level interruption
- Direct memory access (DMA) operation
- All outputs are fully TTL-compatible; I_{OL} = 1.9mA
- Unlimited subroutine nesting
- Interchangeable with the Intel's 8080A in pin-to-pin connections and machine instructions.

PIN CONFIGURATION (TOP VIEW)



Outline 40S1

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

PIN DESCRIPTIONS

Pin	Name	Input or output	Function significance
A_0 ⌇ A_{15}	Address bus	Out	Provides the address signal to external memory up to 65536 bytes or denotes the I/O device number for up to 256 input and 256 output devices. Address terminals are three-state, and remain in the floating state during the HLT instruction execute cycle. T_{WH} or in the hold state.
D_0 ⌇ D_7	Data bus	In/Out	Provides bidirectional transfer of instructions and data between CPU and the external memory or the I/O ports. Status signals are also transferred. When $\overline{WR}$ is low, data goes to memory or output ports. When DBIN is high, the data is received by the CPU. The status signals are sent on the data bus, synchronizing with SYNC. Like the address bus; the data bus maintains the floating state during the HLT instruction execute cycle (T_{WH}) and in the hold state.
SYNC	Synchronizing signal	Out	Indicates the beginning of machine cycles M_1 through M_5. The status signals for each cycle are sent out on the data bus while SYNC is active, and are latched in the external registers during SYNC.
DBIN	Data bus input control signal	Out	Indicates to the external circuits that the data bus is in the input mode, in which the CPU receives instructions or data from memory or input ports. The CPU receives instructions or data on the data bus when DBIN is high.
READY	Ready signal	In	Indicates to the CPU that data from memory or input/output ports is valid on the data bus. When the READY signal is not high in the T_2 state, the CPU will enter a waiting state (T_W) and the WAIT signal goes high. When READY is high, its state advances from T_2 or T_W to T_3. This READY signal is used to synchronize the CPU with slower memory or input/output ports.
WAIT	Wait state signal	Out	Indicates that the CPU has entered a waiting state. When the WAIT signal is high, the CPU is in a waiting state (T_W) and the output on the address bus and the data bus is kept stable.
$\overline{WR}$	Write control signal	Out	Indicates timing of a data write-in operation to memory or output ports. When $\overline{WR}$ is low, data on the data bus is valid; when the WAIT signalis high, it is kept low.
HOLD	Hold request signal	In	When READY is high, the CPU enters the hold state provided that: • the CPU is in the HLD instruction execute state (T_{WH}). • the CPU is in the T_2 or T_W state and the READY signal is high. When the CPU is in the hold state, the data bus and the address bus will be in the floating state, and will be used with the memory or input/output ports regardless of CPU operation.
HLDA	Hold acknowledge signal	Out	When high, indicates that the CPU is in the hold state and the address bus and the data bus will be in the floating state.
INTE	Interrupt enable control signal	Out	When high, indicates that an interruption will be accepted by the CPU. It is set to high by instruction EI and is reset to low by instruction DI. It is automatically reset to low at state T_1 of machine cycle M_1 when an interrupt is accepted, and is also reset by the RESET signal.
INT	Interrupt request signal	In	Indicates to the CPU M58710S that an interrupt is being requested. When the INT is high, the interrupt request will be accepted by the CPU unless HLDA is high or INTE is low. If INT is accepted, INTE will go low and status information INTA will be transferred to the data bus as an interrupt request signal.
RESET	Reset signal	In	When high, the program counter is reset to '0' and instruction NOP is set to the instruction register. INTE is reset to low, and the CPU will not accept interrupts. While RESET is high, the address bus and the data bus remain in the floating state; when RESET goes low, the program will start at location 0. The data registers, accumulator, stack pointer and flag flip-flops are not reset by this signal. No synchronization is necessary for the RESET signal, but the high level must be kept for a minimum of 3 clock cycles.

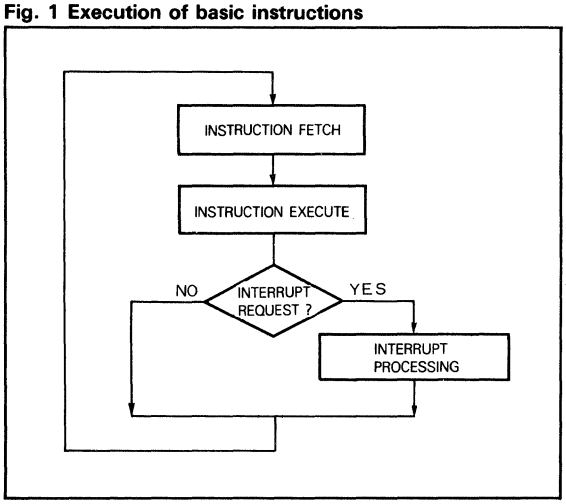
8-BIT PARALLEL CPU

BASIC TIMING

Execution of instructions proceeds in two stages: 1) fetch, and 2) analyze and execute.

Fig. 1 shows the consecutive relationship between stages 1 and 2, after which it is determined whether or not there has been an interrupt request. If there has not, the next instruction is fetched immediately; if there has, it is fetched after completing the necessary interrupt processing. One cycle of this loop completes the execution of one instruction.

Fig. 1 Execution of basic instructions



There are five machine cycles (M_1, M_2, M_3, M_4 and M_5) and the fetching, analysis, and execution of a single instruction requires from 1 to 5 machine cycles.

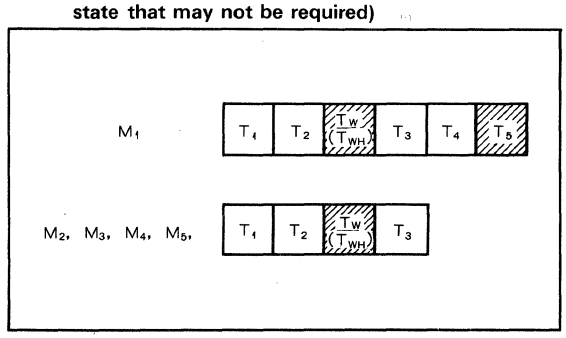
Each cycle consists of from three to five states (T_1, T_2, T_3, T_4 and T_5), the actual number depending upon the instruction being executed. The duration of one state is defined by successive low-to-high transitions of the ϕ_1 clock. (500ns at a clock frequency of 2MHz).

There is also another state T_W, situated between T_2 and T_3 (see Fig. 2) and controlled by the external signals READY and HOLD, and instruction HLT. The duration of T_W is an integral multiple of the clock cycle.

The first machine cycle (M_1) in every instruction cycle is a fetch cycle, and the address for memory read is sent on the address bus. M_1 is composed of states $T_1 \sim T_4$ or $T_1 \sim T_5$, as shown in Fig. 2. Machine cycles M_2, M_3, M_4 and M_5 are usually composed of three states ($T_1 \sim T_3$), with the exception of the instruction XTHL, which requires five states: $T_1 \sim T_5$.

When the clock period is 500ns and there is no T_W, M_1 requires 2μs or 2.5μs, and the other machine cycles require 1.5μs to execute an instruction. When T_W exists, the execution time increases accordingly. Since the minimum instruction cycle requires four states ($T_1 \sim T_4$) of machine cycle M_1, the minimum instruction execution time is 2μs.

Fig. 2 Machine cycle states (hatched blocks indicate a state that may not be required)

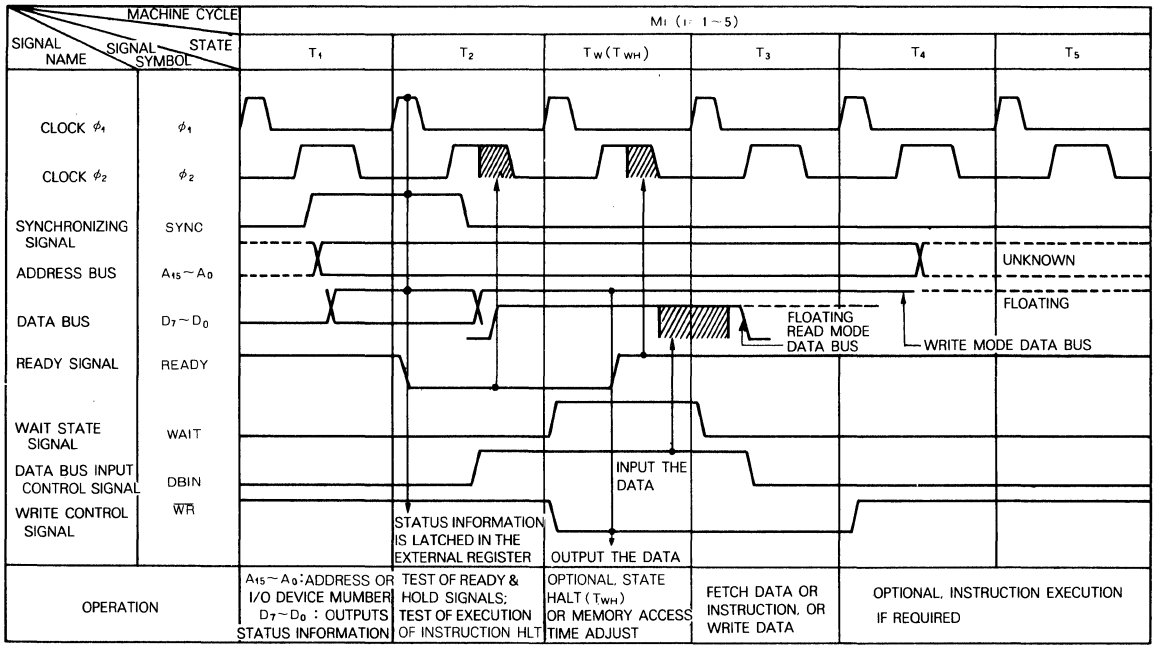


INTERRUPT

When an interruption is requested, the decision whether to accept it or not is taken after the instruction in progress is completed; that is, during the last state of the last machine cycle.

When interrupt is requested and the CPU is in the interrupt-enable state (signal INTE is high), the CPU accepts the interrupt and begins a special interrupt machine cycle M_1 in which the program counter is not incremented and the CPU sends out status information INTA (the interrup acknowledge signal). During state T_3 of special interrupt machine cycle M_1, the external interrupt control circuit sends the interrupt instruction corresponding to interrupt factors on the data bus, and the CPU fetches and executes this instruction. This instruction is a special one-byte call (instruction RST) or a special three-byte call (instruction CALL) which facilitates the processing of interrupts.

Fig. 3 Basic instruction cycle



- Besides the states shown in Fig.3, there is a state T_H, in which the CPU stays in the hold state after the machine cycle.
- States T_W, T_4 and T_5 are optional.
- Hatched portions indicate periods during which input data should be kept stable.
- The address data is valid during the period designated by solid lines.
- The period of T_W depends on the condition of the READY signal.

Table 1 Status information

Data bus	Signal symbol	Status information designation	Function
D_0	INTA	Interrupt acknowledge	Goes high when the CPU accepts the interrupt request signal from the INT terminal.
D_1	$\overline{WO}$	Write mode	Goes high when the current machine cycle is in a read mode, and falls when in a write (output) mode.
D_2	STACK	Stack	Goes high when the address bus holds the pushdown stack address from the stack pointer.
D_3	HLTA	HLT instruction acknowledge	Goes high when the CPU executes the HLT instruction and maintains the halt state.
D_4	OUT	Output instruction acknowledge	Goes high when the address bus contains the address of an output device and the data bus contains the output data. (The address of an output device is contained simultaneously in the upper 8 bits and the lower 8 bits of the address bus.)
D_5	M_1	M_1 status	Goes high when the CPU is in the fetch cycle for the first byte of an instruction.
D_6	INP	Input instruction acknowledge	Goes high when the address bus contains the address of an input device and the data bus receives the input data. (The address of an output device is contained simultaneously in the upper 8 bits and the lower 8 bits of the address bus).
D_7	MEMR	Memory read	Goes high when the data bus is used for memory read data.

STATUS INFORMATION

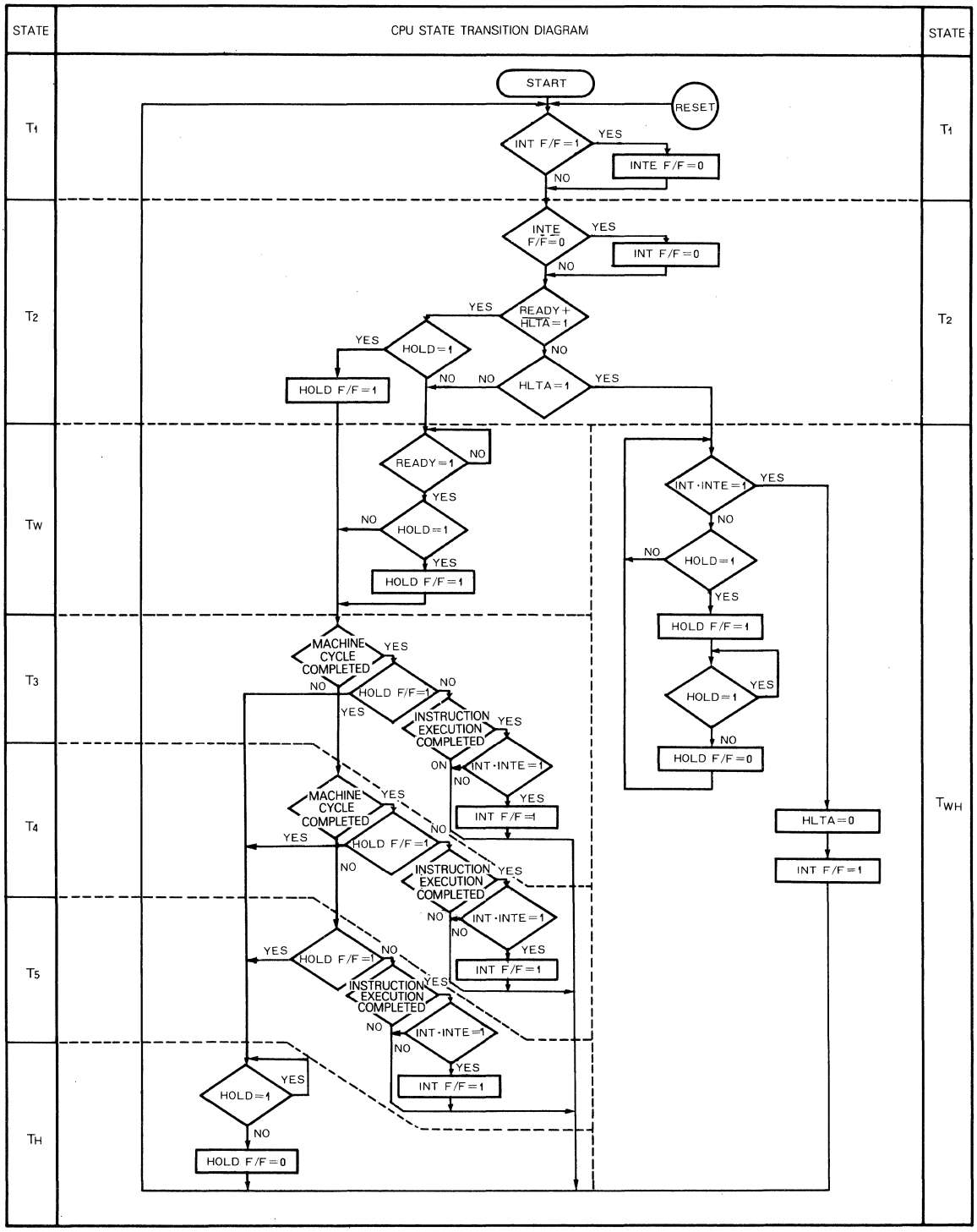
The M58710S sends out 8 bits of status information on data bus (D_7~D_0) at the first state of each machine cycle ($M_i \cdot T_1$) synchronizing with signal SYNC·ϕ_1. Table 1 gives the functions of the status information that will be sent out on the data bus.

Table 2 Status

Status information / Mode No.		1	2	3	4	5	6	7	8	9	10
Data bus bit	Status signal name	Instruction fetch	Memory read	Stack read	Input read	Interrupt acknowl.	Halt acknowledge	Interrupt acknowl. while halt	Memory write	Stack write	Output write
D_0	INTA	0	0	0	0	1	0	1	0	0	0
D_1	$\overline{WO}$	1	1	1	1	1	1	1	0	0	0
D_2	STACK	0	0	1	0	0	0	0	0	1	0
D_3	HLTA	0	0	0	0	0	1	1	0	0	0
D_4	OUT	0	0	0	0	0	0	0	0	0	1
D_5	M_1	1	0	0	0	1	0	1	0	0	0
D_6	INP	0	0	0	1	0	0	0	0	0	0
D_7	MEMR	1	1	1	0	0	1	0	0	0	0

8-BIT PARALLEL CPU

CPU STATE TRANSITION DIAGRAM



MITSUBISHI ELECTRIC

INSTRUCTION CODE LIST

$D_3 \sim D_0$ \ $D_7 \sim D_4$	Hexadecimal notation	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0000	0	NOP	(NOP)	(NOP)	(NOP)	MOV B, B	MOV D, B	MOV H, B	MOV M, B	ADD B	SUB B	ANA B	ORA B	RNZ	RNC	RPO	RP
0001	1	LXI B	LXI D	LXI H	LXI SP	MOV B, C	MOV D, C	MOV H, C	MOV M, C	ADD C	SUB C	ANA C	ORA C	POP B	POP D	POP H	POP PSW
0010	2	STAX B	STAX D	SHLD	STA	MOV B, D	MOV D, D	MOV H, D	MOV M, D	ADD D	SUB D	ANA D	ORA D	JNZ	JNC	JPO	JP
0011	3	INX B	INX D	INX H	INX SP	MOV B, E	MOV D, E	MOV H, E	MOV M, E	ADD E	SUB E	ANA E	ORA E	JMP	OUT	XTHL	DI
0100	4	INR B	INR D	INR H	INR M	MOV B, H	MOV D, H	MOV H, H	MOV M, H	ADD H	SUB H	ANA H	ORA H	CNZ	CNC	CPO	CP
0101	5	DCR B	DCR D	DCR H	DCR M	MOV B, L	MOV D, L	MOV H, L	MOV M, L	ADD L	SUB L	ANA L	ORA L	PUSH B	PUSH D	PUSH H	PUSH PSW
0110	6	MVI B	MVI D	MVI H	MVI M	MOV B, M	MOV D, M	MOV H, M	HLT	ADD M	SUB M	ANA M	ORA M	ADI	SUI	ANI	ORI
0111	7	RLC	RAL	DAA	STC	MOV B, A	MOV D, A	MOV H, A	MOV M, A	ADD A	SUB A	ANA A	ORA A	RST 0	RST 2	RST 4	RST 6
1000	8	(NOP)	(NOP)	(NOP)	(NOP)	MOV C, B	MOV E, B	MOV L, B	MOV A, B	ADC B	SBB B	XRA B	CMP B	RZ	RC	RPE	RM
1001	9	DAD B	DAD D	DAD H	DAD SP	MOV C, C	MOV E, C	MOV L, C	MOV A, C	ADC C	SBB C	XRA C	CMP C	RET	(RET)	PCHL	SPHL
1010	A	LDAX B	LDAX D	LHLD	LDA	MOV C, D	MOV E, D	MOV L, D	MOV A, D	ADC D	SBB D	XRA D	CMP D	JZ	JC	JPE	JM
1011	B	DCX B	DCX D	DCX H	DCX SP	MOV C, E	MOV E, E	MOV L, E	MOV A, E	ADC E	SBB E	XRA E	CMP E	(JMP)	IN	XCHG	EI
1100	C	INR C	INR E	INR L	INR A	MOV C, H	MOV E, H	MOV L, H	MOV A, H	ADC H	SBB H	XRA H	CMP H	CZ	CC	CPE	CM
1101	D	DCR C	DCR E	DCR L	DCR A	MOV C, L	MOV E, L	MOV L, L	MOV A, L	ADC L	SBB L	XRA L	CMP L	CALL	(CALL)	(CALL)	(CALL)
1110	E	MVI C	MVI E	MVI L	MVI A	MOV C, M	MOV E, M	MOV L, M	MOV A, M	ADC M	SBB M	XRA M	CMP M	ACI	SBI	XRI	CPI
1111	F	RRC	RAR	CMA	CMC	MOV C, A	MOV E, A	MOV L, A	MOV A, A	ADC A	SBB A	XRA A	CMP A	RST 1	RST 3	RST 5	RST 7

This list shows the machine codes and corresponding machine instructions. $D_3 \sim D_0$ indicate the lower 4 bits of the machine code and $D_7 \sim D_4$ indicate the upper 4 bits. Hexadecimal numbers are also used to indicate this code. The instruction may consist of one, two, or three bytes, but only the first byte is listed.

indicates a three-byte instruction.

indicates a two-byte instruction.

( ) is not a formal instruction, but if this code is accessed, the instruction in parentheses may be executed. This is not, however, guaranteed.

8-BIT PARALLEL CPU

MACHINE INSTRUCTIONS

Item: Instr. class	Mnemonic	Instruction code: D_7D_6	$D_5D_4D_3$	$D_2D_1D_0$	16mal notatn	No. of states	No. of bytes	No. of cycles	Functions	Flags: S	Z	P	CY_2	CY_1	Address bus: Contents	Mach. cycle *	Data bus: Contents	I/O	Mach. cycle †
Data transfer	**MOV r1, r2**	0 1	D D D	S S S		5	1	1	$(r_1) \leftarrow (r_2)$	X	X	X	X	X					
	MOV M, r	0 1	1 1 0	S S S		7	1	2	$(M) \leftarrow (r)$ Where, M = (H) (L)	X	X	X	X	X	M	M_4	(r)	O	M_4
	MOV r, M	0 1	D D D	1 1 0		7	1	2	$(r) \leftarrow (M)$ Where, M = (H) (L)	X	X	X	X	X	M	M_4	(M)	I	M_4
	MVI r, n	0 0	D D D	1 1 0		7	2	2	$(r) \leftarrow n$	X	X	X	X	X			⟨B_2⟩	I	M_4
			⟨B_2⟩																
	MVI M, n	0 0	1 1 0	1 1 0	3 6	10	2	3	$(M) \leftarrow n$ Where, M = (H) (L)	X	X	X	X	X	M	M_5	⟨B_2⟩	I	M_5
			⟨B_2⟩																
	LXI B, m	0 0	0 0 0	0 0 1	0 1	10	3	3	$(C) \leftarrow$ ⟨B_2⟩	X	X	X	X	X			⟨B_2⟩	I	M_2
			⟨B_2⟩						$(B) \leftarrow$ ⟨B_3⟩ Where, m = ⟨B_3⟩ ⟨B_2⟩								⟨B_3⟩	I	M_3
			⟨B_3⟩																
	LXI D, m	0 0	0 1 0	0 0 1	1 1	10	3	3	$(E) \leftarrow$ ⟨B_2⟩	X	X	X	X	X			⟨B_2⟩	I	M_2
			⟨B_2⟩						$(D) \leftarrow$ ⟨B_3⟩ Where, m = ⟨B_3⟩ ⟨B_2⟩								⟨B_3⟩	I	M_3
			⟨B_3⟩																
	LXI H, m	0 0	1 0 0	0 0 1	2 1	10	3	3	$(L) \leftarrow$ ⟨B_2⟩	X	X	X	X	X			⟨B_2⟩	I	M_2
			⟨B_2⟩						$(H) \leftarrow$ ⟨B_3⟩ Where, m = ⟨B_3⟩ ⟨B_2⟩								⟨B_3⟩	I	M_3
			⟨B_3⟩																
	LXI SP, m	0 0	1 1 0	0 0 1	3 1	10	3	3	$(SP) \leftarrow m$	X	X	X	X	X			⟨B_2⟩	I	M_2
			⟨B_2⟩														⟨B_3⟩	I	M_3
			⟨B_3⟩																
	SPHL	1 1	1 1 1	0 0 1	F 9	5	1	1	$(SP) \leftarrow (H)(L)$	X	X	X	X	X					
	STAX B	0 0	0 0 0	0 1 0	0 2	7	1	2	$((B)(C)) \leftarrow (A)$	X	X	X	X	X	(B) (C)	M_4	(A)	O	M_4
	STAX D	0 0	0 1 0	0 1 0	1 2	7	1	2	$((D)(E)) \leftarrow (A)$	X	X	X	X	X	(D) (E)	M_4	(A)	O	M_4
	LDAX B	0 0	0 0 1	0 1 0	0 A	7	1	2	$(A) \leftarrow ((B)(C))$	X	X	X	X	X	(B) (C)	M_4	((B) (C))	I	M_4
	LDAX D	0 0	0 1 1	0 1 0	1 A	7	1	2	$(A) \leftarrow ((D)(E))$	X	X	X	X	X	(D) (E)	M_4	((D) (E))	I	M_4
	STA m	0 0	1 1 0	0 1 0	3 2	13	3	4	$(m) \leftarrow (A)$	X	X	X	X	X	m	M_4	(A)	O	M_4
			⟨B_2⟩																
			⟨B_3⟩																
	LDA m	0 0	1 1 1	0 1 0	3 A	13	3	4	$(A) \leftarrow (m)$	X	X	X	X	X	m	M_4	(m)	I	M_4
			⟨B_2⟩																
			⟨B_3⟩																
	SHLD m	0 0	1 0 0	0 1 0	2 2	16	3	5	$(m) \leftarrow (L)$	X	X	X	X	X	m	M_4	(L)	O	M_4
			⟨B_2⟩						$(m+1) \leftarrow (H)$						m + 1	M_5	(H)	O	M_5
			⟨B_3⟩																
	LHLD m	0 0	1 0 1	0 1 0	2 A	16	3	5	$(L) \leftarrow (m)$	X	X	X	X	X	m	M_4	(m)	I	M_4
			⟨B_2⟩						$(H) \leftarrow (m+1)$						m+1	M_5	(m + 1)	I	M_5
			⟨B_3⟩																
	XCHG	1 1	1 0 1	0 1 1	E B	4	1	1	$(H)(L) \leftrightarrow (D)(E)$	X	X	X	X	X					
	XTHL	1 1	1 0 0	0 1 1	E 3	18	1	5	$(H)(L) \leftrightarrow ((SP)+1)((SP))$	X	X	X	X	X	(SP)	M_2	((SP))	I	M_2
															(SP)+1	M_3	((SP)+1)	I	M_3
Arithmetic, logical, compare	**ADD r**	1 0	0 0 0	S S S		4	1	1	$(A) \leftarrow (A) + (r)$	O	O	O	O	O					
	ADD M	1 0	0 0 0	1 1 0	8 6	7	1	2	$(A) \leftarrow (A) + (M)$ Where, M = (H) (L)	O	O	O	O	O	M	M_4	(M)	I	M_4
	ADI n	1 1	0 0 0	1 1 0	C 6	7	2	2	$(A) \leftarrow (A) + n$	O	O	O	O	O			⟨B_2⟩	I	M_4
			⟨B_2⟩																
	ADC r	1 0	0 0 1	S S S		4	1	1	$(A) \leftarrow (A) + (r) + (CY_2)$	O	O	O	O	O					
	ADC M	1 0	0 0 1	1 1 0	8 E	7	1	2	$(A) \leftarrow (A) + (M) + (CY_2)$ Where, M = (H) (L)	O	O	O	O	O	M	M_4	(M)	I	M_4
	ACI n	1 1	0 0 1	1 1 0	C E	7	2	2	$(A) \leftarrow (A) + n + (CY_2)$	O	O	O	O	O			⟨B_2⟩	I	M_4
			⟨B_2⟩																
	DAD B	0 0	0 0 1	0 0 1	0 9	10	1	3	$(H)(L) \leftarrow (H)(L) + (B)(C)$	X	X	X	O	X					
	DAD D	0 0	0 1 1	0 0 1	1 9	10	1	3	$(H)(L) \leftarrow (H)(L) + (D)(E)$	X	X	X	O	X					
	DAD H	0 0	1 0 1	0 0 1	2 9	10	1	3	$(H)(L) \leftarrow (H)(L) + (H)(L)$	X	X	X	O	X					
	DAD SP	0 0	1 1 1	0 0 1	3 9	10	1	3	$(H)(L) \leftarrow (H)(L) + (SP)$	X	X	X	O	X					
	SUB r	1 0	0 1 0	S S S		4	1	1	$(A) \leftarrow (A) - (r)$	O	O	O	O	O					
	SUB M	1 0	0 1 0	1 1 0	9 6	7	1	2	$(A) \leftarrow (A) - (M)$ Where, M = (H) (L)	O	O	O	O	O	M	M_4	(M)	I	M_4
	SUI n	1 1	0 1 0	1 1 0	D 6	7	2	2	$(A) \leftarrow (A) - n$	O	O	O	O	O			⟨B_2⟩	I	M_4
			⟨B_2⟩																
	SBB r	1 0	0 1 1	S S S		4	1	1	$(A) \leftarrow (A) - (r) - (CY_2)$	O	O	O	O	O					
	SBB M	1 0	0 1 1	1 1 0	9 E	7	1	2	$(A) \leftarrow (A) - (M) - (CY_2)$ Where, M = (H) (L)	O	O	O	O	O	M	M_4	(M)	I	M_4
	SBI n	1 1	0 1 1	1 1 0	D E	7	2	2	$(A) \leftarrow (A) - n - (CY_2)$	O	O	O	O	O			⟨B_2⟩	I	M_4
			⟨B_2⟩																
	ANA r	1 0	1 0 0	S S S		4	1	1	$(A) \leftarrow (A) \wedge (r)$	O	O	O	0	O					
	ANA M	1 0	1 0 0	1 1 0	A 6	7	1	2	$(A) \leftarrow (A) \wedge (M)$ Where, M = (H) (L)	O	O	O	0	O	M	M_4	(M)	I	M_4
	ANI n	1 1	1 0 0	1 1 0	E 6	7	2	2	$(A) \leftarrow (A) \wedge n$	O	O	O	0	O			⟨B_2⟩	I	M_4
			⟨B_2⟩																
	XRA r	1 0	1 0 1	S S S		4	1	1	$(A) \leftarrow (A) \forall (r)$	O	O	O	0	0					
	XRA M	1 0	1 0 1	1 1 0	A E	7	1	2	$(A) \leftarrow (A) \forall (M)$ Where, M = (H) (L)	O	O	O	0	0	M	M_4	(M)	I	M_4
	XRI n	1 1	1 0 1	1 1 0	E E	7	2	2	$(A) \leftarrow (A) \forall n$	O	O	O	0	0			⟨B_2⟩	I	M_4
			⟨B_2⟩																
	ORA r	1 0	1 1 0	S S S		4	1	1	$(A) \leftarrow (A) \vee (r)$	O	O	O	0	0					
	ORA M	1 0	1 1 0	1 1 0	B 6	7	1	2	$(A) \leftarrow (A) \vee (M)$ Where, M = (H) (L)	O	O	O	0	0	M	M_4	(M)	I	M_4
	ORI n	1 1	1 1 0	1 1 0	F 6	7	2	2	$(A) \leftarrow (A) \vee n$	O	O	O	0	0			⟨B_2⟩	I	M_4
			⟨B_2⟩																
	CMP r	1 0	1 1 1	S S S		4	1	1	$(A) - (r)$	O	O	O	O	O					
	CMP M	1 0	1 1 1	1 1 0	B E	7	1	2	$(A) - (M)$ Compare; Where, M = (H) (L)	O	O	O	O	O	M	M_4	(M)	I	M_4
	CPI n	1 1	1 1 1	1 1 0	F E	7	2	2	$(A) - n$	O	O	O	O	O			⟨B_2⟩	I	M_4
			⟨B_2⟩																
Register increment/decrement	**INR r**	0 0	D D D	1 0 0		5	1	1	$(r) \leftarrow (r) + 1$	O	O	O	X	O					
	INR M	0 0	1 1 0	1 0 0	3 4	10	1	3	$(M) \leftarrow (M) + 1$ Where, M = (H) (L)	O	O	O	X	O	M	M_4	(M)	I	M_4
	DCR r	0 0	D D D	1 0 1		5	1	1	$(r) \leftarrow (r) - 1$	O	O	O	X	O					
	DCR M	0 0	1 1 0	1 0 1	3 5	10	1	3	$(M) \leftarrow (M) - 1$ Where, M = (H) (L)	O	O	O	X	O	M	M_4	(M)	I	M_4
	INX B	0 0	0 0 0	0 1 1	0 3	5	1	1	$(B)(C) \leftarrow (B)(C) + 1$	X	X	X	X	X					
	INX D	0 0	0 1 0	0 1 1	1 3	5	1	1	$(D)(E) \leftarrow (D)(E) + 1$	X	X	X	X	X					
	INX H	0 0	1 0 0	0 1 1	2 3	5	1	1	$(H)(L) \leftarrow (H)(L) + 1$	X	X	X	X	X					
	INX SP	0 0	1 1 0	0 1 1	3 3	5	1	1	$(SP) \leftarrow (SP) + 1$	X	X	X	X	X					
	DCX B	0 0	0 0 1	0 1 1	0 B	5	1	1	$(B)(C) \leftarrow (B)(C) - 1$	X	X	X	X	X					
	DCX D	0 0	0 1 1	0 1 1	1 B	5	1	1	$(D)(E) \leftarrow (D)(E) - 1$	X	X	X	X	X					
	DCX H	0 0	1 0 1	0 1 1	2 B	5	1	1	$(H)(L) \leftarrow (H)(L) - 1$	X	X	X	X	X					
	DCX SP	0 0	1 1 1	0 1 1	3 B	5	1	1	$(SP) \leftarrow (SP) - 1$	X	X	X	X	X					
Rotate & shift contents of accumulator	**RLC**	0 0	0 0 0	1 1 1	0 7	4	1	1	Left shift CY_2 ← A_7 A_6 ····· A_1 A_0 ←	X	X	X	O	X					
	RRC	0 0	0 0 1	1 1 1	0 F	4	1	1	Right shift CY_2 → A_7 A_6 ····· A_1 A_0 →	X	X	X	O	X					
	RAL	0 0	0 1 0	1 1 1	1 7	4	1	1	Left shift CY_2 ← A_7 A_6 ····· A_1 A_0 ←	X	X	X	O	X					
	RAR	0 0	0 1 1	1 1 1	1 F	4	1	1	Right shift CY_2 → A_7 A_6 ····· A_1 A_0 →	X	X	X	O	X					
Accumu. compen.	**CMA**	0 0	1 0 1	1 1 1	2 F	4	1	1	$(A) \leftarrow \overline{(A)}$	X	X	X	X	X					
	DAA	0 0	1 0 0	1 1 1	2 7	4	1	1	Results of binary addition are adjusted to BCD	O	O	O	O	O					
Carry set	**STC**	0 0	1 1 0	1 1 1	3 7	4	1	1	$(CY_2) \leftarrow 1$	X	X	X	1	X					
	CMC	0 0	1 1 1	1 1 1	3 F	4	1	1	$(CY_2) \leftarrow \overline{(CY_2)}$	X	X	X	O	X					

*: State is T_1. †: State is T_2.

MITSUBISHI ELECTRIC

Instr. class	Mnemonic	Instruction code D7 D6 D5 D4 D3 D2 D1 D0	16-mal notatn	No. of states	No. of bytes	No. of cycles	Functions	Flags S Z P CY2 CY1	Address bus Contents	Address bus Mach. cycle*	Data bus Contents	Data bus I/O	Data bus Mach. cycle**
Jump	JMP m	1 1 0 0 0 0 1 1 <B2> <B3>	C3	10	3	3	(PC)←m	X X X X X			<B2> <B3>	I I	M2 M3
	PCHL	1 1 1 0 1 0 0 1	E9	5	1	1	(PC)←(H)(L)	X X X X X					
	JC m	1 1 0 1 1 0 1 0 <B2> <B3>	DA	10	3	3	(CY2) = 1	X X X X X	If condition is true.				
	JNC m	1 1 0 1 0 0 1 0 <B2> <B3>	D2	10	3	3	(CY2) = 0 If condition is true (PC)←m	X X X X X					
	JZ m	1 1 0 0 1 0 1 0 <B2> <B3>	CA	10	3	3	(Z) = 1	X X X X X			<B2> <B3>	I I	M2 M3
	JNZ m	1 1 0 0 0 0 1 0 <B2> <B3>	C2	10	3	3	(Z) ≠ 0	X X X X X					
	JP m	1 1 1 1 0 0 1 0 <B2> <B3>	F2	10	3	3	(S) = 0 If condition is false (PC)←(PC) + 3	X X X X X	If condition is false.				
	JM m	1 1 1 1 1 0 1 0 <B2> <B3>	FA	10	3	3	(S) = 1	X X X X X					
	JPE m	1 1 1 0 1 0 1 0 <B2> <B3>	EA	10	3	3	(P) = 1	X X X X X					
	JPO m	1 1 1 0 0 0 1 0 <B2> <B3>	E2	10	3	3	(P) = 0	X X X X X					
Subroutine call	CALL m	1 1 0 0 1 1 0 1 <B2> <B3>	CD	17	3	5	((SP)−1)((SP)−2)←(PC)+3, (PC)←m (SP) ← (SP)−2	X X X X X	(SP)−1 (SP)−2	M4 M5	<B2> <B3> ((PC)+3)15−8 ((PC)+3)7−0	I I O O	M2 M3 M4 M5
	RST n	1 1 A A A 1 1 1		11	1	3	((SP)−1)((SP)−2)←(PC)+1, (PC)←n×8, (SP) ← (SP)−2 Where 0≤n≤7	X X X X X	(SP)−1 (SP) 2	M4 M5	((PC)+1)15−8 ((PC)+1)7−0	O O	M4 M5
	CC m	1 1 0 1 1 1 0 0 <B2> <B3>	DC	17/11	3	5/3	(CY2) = 1	X X X X X	If condition is true.				
	CNC m	1 1 0 1 0 1 0 0 <B2> <B3>	D4	17/11	3	5/3	(CY2) = 0	X X X X X					
	CZ m	1 1 0 0 1 1 0 0 <B2> <B3>	CC	17/11	3	5/3	(Z) = 1 ((SP)−1)((SP)−2)←(PC)+3 (PC)←m	X X X X X	(SP)−1	M4	<B2> <B3> ((PC)+3)15−8	I I O	M2 M3 M4
	CNZ m	1 1 0 0 0 1 0 0 <B2> <B3>	C4	17/11	3	5/3	(Z) = 0 (SP)←(SP)−2	X X X X X	(SP)−2	M5	((PC)+3)7−0	O	M5
	CP m	1 1 1 1 0 1 0 0 <B2> <B3>	F4	17/11	3	5/3	(S) = 0	X X X X X					
	CM m	1 1 1 1 1 1 0 0 <B2> <B3>	FC	17/11	3	5/3	(S) = 1 If condition is false (PC)←(PC) + 3	X X X X X					
	CPE m	1 1 1 0 1 1 0 0 <B2> <B3>	EC	17/11	3	5/3	(P) = 1	X X X X X					
	CPO m	1 1 1 0 0 1 0 0 <B2> <B3>	E4	17/11	3	5/3	(P) = 0	X X X X X					
Return	RET	1 1 0 0 1 0 0 1	C9	10	1	3	(PC) ←((SP)+1)((SP)), (SP)←(SP)+2	X X X X X	(SP) (SP)+1	M4 M5	((SP)) ((SP)+1)	I I	M4 M5
	RC	1 1 0 1 1 0 0 0	D8	11/5	1	3/1	(CY2) = 1 If condition is true	X X X X X	If condition is true.				
	RNC	1 1 0 1 0 0 0 0	D0	11/5	1	3/1	(CY2) ≠ 0	X X X X X					
	RZ	1 1 0 0 1 0 0 0	C8	11/5	1	3/1	(Z) = 1 (PC)←((SP)+1)((SP))	X X X X X	(SP)	M4	((SP))	I	M4
	RNZ	1 1 0 0 0 0 0 0	C0	11/5	1	3/1	(Z) = 0 (SP)←(SP)+2	X X X X X	(SP)+1	M5	((SP)+1)	I	M5
	RP	1 1 1 1 0 0 0 0	F0	11/5	1	3/1	(S) = 0	X X X X X					
	RM	1 1 1 1 1 0 0 0	F8	11/5	1	3/1	(S) = 1 If condition is false	X X X X X	If condition is false.				
	RPE	1 1 1 0 1 0 0 0	E8	11/5	1	3/1	(P) = 1 (PC)←((PC)+1	X X X X X					
	RPO	1 1 1 0 0 0 0 0	E0	11/5	1	3/1	(P) = 0	X X X X X					
Input/output control	IN n	1 1 0 1 1 0 1 1 <B2>	DB	10	2	3	(A) ← (Input buffer) ← (Input device of number n) (Input data)	X X X X X	<B2> B2>	M5	<B2> (Input data)	I	M4 M5
	OUT n	1 1 0 1 0 0 1 1 <B2>	D3	10	2	3	(Output device of number n) ←(A)	X X X X X	<B2> <B2>	M5	<B2> (A)	O O	M4 M5
Interrupt control	EI	1 1 1 1 1 0 1 1	FB	4	1	1	(INTE)←1	X X X X X					
	DI	1 1 1 1 0 0 1 1	F3	4	1	1	(INTE)←0	X X X X X					
Stack control	PUSH PSW	1 1 1 1 0 1 0 1	F5	11	1	3	((SP)−1)←(A), ((SP)−2)←(F) (SP) ←(SP)−2	X X X X X	(SP) 1 (SP)−2	M4 M5	(A) (F)	O O	M4 M5
	PUSH B	1 1 0 0 0 1 0 1	C5	11	1	3	((SP)−1)←(B), ((SP)−2)←(C) (SP) ←(SP)−2	X X X X X	(SP)−1 (SP)−2	M4 M5	(B) (C)	O O	M4 M5
	PUSH D	1 1 0 1 0 1 0 1	D5	11	1	3	((SP)−1)←(D), ((SP)−2)←(E) (SP) ←(SP)−2	X X X X X	(SP)−1 (SP)−2	M4 M5	(D) (E)	O O	M4 M5
	PUSH H	1 1 1 0 0 1 0 1	E5	11	1	3	((SP)−1)←(H), ((SP)−2)←(L) (SP) ←(SP)−2	X X X X X	(SP)−1 (SP)−2	M4 M5	(H) (L)	O O	M4 M5
	POP PSW	1 1 1 1 0 0 0 1	F1	10	1	3	(F) ←((SP)), (A) ←((SP)+1) (SP) ←(SP)+2	O O O O O	(SP) (SP)+1	M4 M5	((SP)) ((SP)+1)	I I	M4 M5
	POP B	1 1 0 0 0 0 0 1	C1	10	1	3	(C) ←((SP)), (B) ←((SP)+1) (SP) ←(SP)+2	X X X X X	(SP) (SP)+1	M4 M5	((SP)) ((SP)+1)	I I	M4 M5
	POP D	1 1 0 1 0 0 0 1	D1	10	1	3	(E) ←((SP)), (D) ←((SP)+1) (SP) ←(SP)+2	X X X X X	(SP) (SP)+1	M4 M5	((SP)) ((SP)+1)	I I	M4 M5
	POP H	1 1 1 0 0 0 0 1	E1	10	1	3	(L) ←((SP)), (H) ←((SP)+1) (SP) ←(SP)+2	X X X X X	(SP) (SP)+1	M4 M5	((SP)) ((SP)+1)	I I	M4 M5
Others	HLT	0 1 1 1 0 1 1 0	76	7	1	1	(PC) ←(PC)+1	X X X X X					
	NOP	0 0 0 0 0 0 0 0	00	4	1	1	(PC) ←(PC)+1	X X X X X					

*: State is T1. **: State is T2.

Symbol	Meaning
r	Register
m,	Two-byte data
n	One-byte data
<B2>	Second byte of instruction
<B3>	Third byte of instruction
AAA	Binary representation for RST instruction n
F	8-bit data from the most to the least significant bit S, Z, 0, CY1, 0, P, 1, CY2
PC	Program counter
SP	Stack pointer

Symbol	Meaning
SSS or DDD	Bit pattern designating register or memory.

Register or memory	SSS or DDD
B	0 0 0
C	0 0 1
D	0 1 0
E	0 1 1
H	1 0 0
L	1 0 1
M	1 1 0
A	1 1 1

Where, M=(H)(L)

Symbol	Meaning
←	Data is transferred in direction shown
( )	Contents of register or memory location
∨	Inclusive OR
∨	Exclusive OR
∧	Logical AND
—	1's complement
X	Content of flag is not changed after execution
O	Content of flag is set or reset after execution
I	Input mode
O	Output mode

8-BIT PARALLEL CPU

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{DD}	Supply voltage	With respect to V_{BB} (substrate)	−0.3～20	V
V_{CC}	Supply voltage		−0.3～20	V
V_{SS}	Supply voltage		−0.3～20	V
V_I	Input voltage		−0.3～20	V
Pd	Maximum power dissipation	Ta = 25°C	1500	mW
Topr	Operating free-air temperature		0～70	°C
Tstg	Storage temperature		−65～150	°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{BB}	Supply voltage	−4.75	−5	−5.25	V
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{DD}	Supply voltage	11.4	12	12.6	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	3.3		V_{CC}+1	V
V_{IL}	Low-level input voltage	−1		0.8	V
$V_{IH(\phi)}$	High-level clock input voltage	9		V_{DD}+1	V
$V_{IL(\phi)}$	Low-level clock input voltage	−1		0.8	V
Topr	Operating free-air temperature	0		70	°C

ELECTRICAL CHARACTERISTICS (Ta = 0～70°C, V_{DD} = 12V ± 5%, V_{CC} = 5V ± 5%, V_{BB} = −5V ± 5%, V_{SS} = 0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{OL}	Low-level output voltage	I_{OL} = 1.9mA, All output			0.45	V
V_{OH}	High-level output voltage	I_{OH} = −150μA	3.7			V
I_{BB}	V_{BB} supply current	Operating at $t_{c(\phi)}$ = 480ns, Ta = 25°C (Note 2)		−0.01	−1	mA
I_{CC}	V_{CC} supply current			60	75	mA
I_{DD}	V_{DD} supply current			40	70	mA
I_I	Input current, except clock and data bus	$0 \leqq V_I \leqq V_{CC}$			±10	μA
$I_{I(\phi)}$	Clock input current	$0 \leqq V_{I(\phi)} \leqq V_{DD}$			±10	μA
$I_{I(DB)}$	Input current, data bus (Note 3)	$0 \leqq V_{I(DB)} \leqq V_{IL}$ $V_{IL} \leqq V_{I(DB)} \leqq V_{CC}$			10 −100	μA
$I_{I(HOLD)}$	Input current during hold, address or data bus	At hold state 0.45V $\leqq V_O \leqq V_{CC}$			10 −100 −2	μA μA mA
$C_{i(\phi_1)}$	Input capacitance, clock input (ϕ_1)	$V_{(\phi_1)}$ = 0V, f = 1MHz, 25mVr.m.s		20	25	pF
$C_{i(\phi_2)}$	Input capacitance, clock input (ϕ_2)	$V_{(\phi_2)}$ = 0V		15	20	pF
C_i	Input capacitance, any input except clock	V_I = 0V		5	10	pF
C_o	Output capacitance	V_O = 0V		5	20	pF

Note 1 : Current flowing into an IC is positive; out is negative.

2 : $t_{c(\phi)} = t_{d(\phi_{1H}\cdot\phi_2)} + t_{r(\phi_2)} + t_{w(\phi_2)} + t_{f(\phi_2)} + t_{d(\phi_2\cdot\phi_1)} + t_{r(\phi_1)}$

3 : Active pull-up resistors will be switched on to the data bus when DBIN is high and data input voltage is more positive than V_{IH} min.

TIMING REQUIREMENTS ($Ta = 0 \sim 70°C$, $V_{DD} = 12V \pm 5\%$, $V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, $V_{SS} = 0V$, unless otherwise noted)

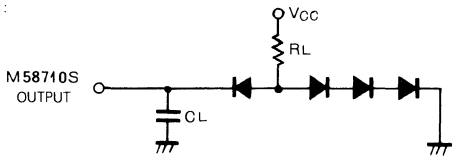
Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
$t_{c(\phi)}$	Clock cycle time (Note 4)	480		2000	ns
$t_{r(\phi)}$	Clock rise time	0		50	ns
$t_{f(\phi)}$	Clock fall time	0		50	ns
$t_{w(\phi 1)}$	Clock 1 pulse width	60			ns
$t_{w(\phi 2)}$	Clock 2 pulse width	220			ns
$t_{d(\phi 1L-\phi 2)}$	Delay time, clock 1 to clock 2	0			ns
$t_{d(\phi 2-\phi 1)}$	Delay time, clock 2 to clock 1	70			ns
$t_{d(\phi 1H-\phi 2)}$	Delay time, clock 1 high to clock 2	80			ns
$t_{su(DA-\phi 1)}$	Data setup time with respect to clock 1	30			ns
$t_{su(DA-\phi 2)}$	Data setup time with respect to clock 2	150			ns
$t_{su(HOLD)}$	Hold setup time	140			ns
$t_{su(INT)}$	Interrupt setup time	120			ns
$t_{su(RDY)}$	Ready setup time	120			ns
$t_{h(DA)}$	Data hold time	$t_{PD(DBI)}$			ns
$t_{h(HOLD)}$	Hold input hold time	0			ns
$t_{h(INT)}$	Interrupt hold time	0			ns
$t_{h(RDY)}$	Ready hold time	0			ns

Note 4 : $t_{c(\phi)} = t_{d(\phi 1L-\phi 2)} + t_{r(\phi 2)} + t_{w(\phi 2)} + t_{r(\phi 2)} + t_{d(\phi 2-\phi 1)} + t_{r(\phi 1)}$

SWITCHING CHARACTERISTICS ($Ta = 0 \sim 70°C$, $V_{DD} = 12V \pm 5\%$, $V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted)

Symbol	Parameter	Test conditions (Note 5)	Limits			Unit
			Min	Typ	Max	
$t_{PD(AD)}$	Propagation delay time, clock 2 to address outputs	$R_L = 2.1k\Omega$, $C_L = 100pF$			200	ns
$t_{PD(DA)}$	Propagation delay time, clock 2 to data bus	$R_L = 2.1k\Omega$, $C_L = 100pF$			220	ns
$t_{PD(CONT)}$	Propagation delay time, clocks to control outputs	$R_L = 2.1k\Omega$, $C_L = 50pF$			120	ns
$t_{PD(DBI)}$	Propagation delay time, clock 2 to DBIN output	$R_L = 2.1k\Omega$, $C_L = 50pF$	25		140	ns
$t_{PD(INT)}$	Propagation delay time, clock 2 to INTE output	$R_L = 2.1k\Omega$, $C_L = 50pF$			200	ns
$t_{PD(DI)}$	Time for data bus to enter input mode				$t_{PD(DBI)}$	ns
t_{PXZ}	Disable time to high-impedance state during hold address output and data bus				120	ns
$t_{d(\overline{WR}-AD)}$	Delay time, write signal to address output	$R_L = 2.1k\Omega$, $C_L = 100pF$	$t_{d(\phi 1H-\phi 2)}$			ns
$t_{d(AD-\overline{WR})}$	Delay time, address output to write signal	$R_L = 2.1k\Omega$, $C_L = 100pF$	Note 6			ns
$t_{d(\overline{WR}-DA)}$	Delay time, write signal to data output	$R_L = 2.1k\Omega$, $C_L = 100pF$	$t_{d(\phi 1H-\phi 2)}$			ns
$t_{d(DA-\overline{WR})}$	Delay time, data output to write signal	$R_L = 2.1k\Omega$, $C_L = 100pF$	Note 7			ns

Note 5 : Load circuit :

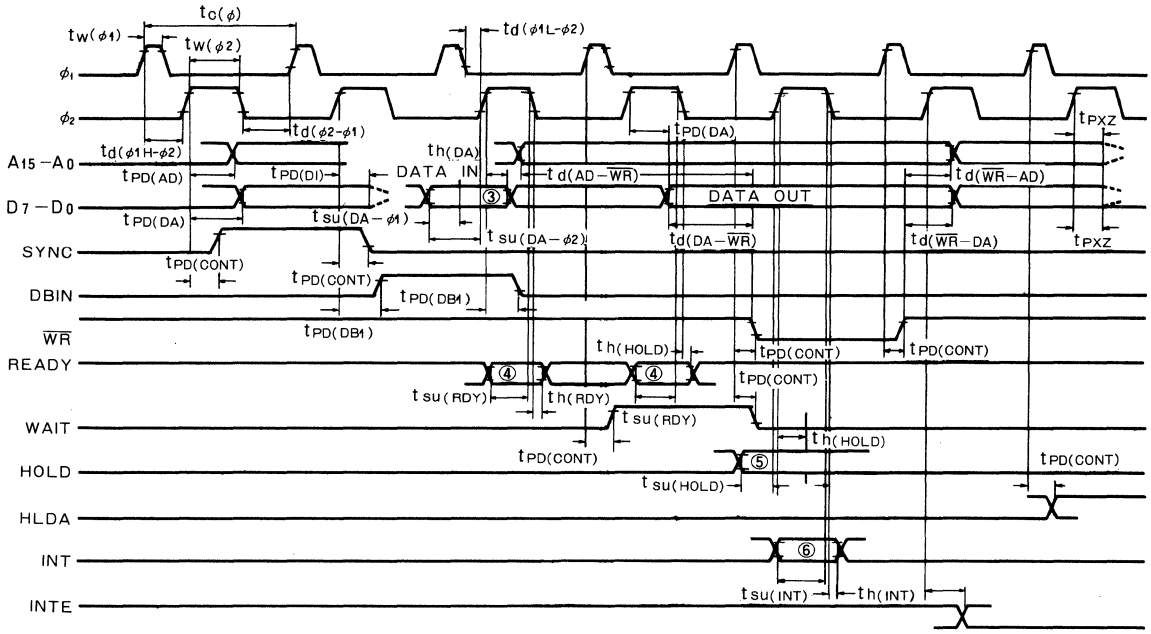


6 : $t_{d(AD-\overline{WR})} = 2t_{c(\phi)} - t_{d(\phi 1H-\phi 2)} - t_{r(\phi)} - 140ns$

7 : $t_{d(DA-\overline{WR})} = t_{c(\phi)} - t_{c(\phi 1H-\phi 2)} - t_{r(\phi)} - 170ns$

8-BIT PARALLEL CPU

TIMING DIAGRAM



Note 1 : This timing diagram shows timing relationships only, it does not represent any specific machine cycle.

2 : Time measurements are made at the following reference voltages: Clock voltage H = 8.0V, L = 1.0V; input voltage, H = 3.3V, L = 0.8V; output voltage, H = 2.0V, L = 0.8V

3 : Data on the data bus must be stable for this period in the input mode. Requirements $t_{su(DA-\phi1)}$, $t_{su(DA-\phi2)}$, $t_{h(DA)}$ must be satisfied.

4 : The ready signal must be stable for this period during state T_2 or T_W. External synchronization is required.

5 : The hold signal must be stable for this period during state T_2 or T_W when entering the hold mode and during states T_3, T_4, T_5, T_{WH} and T_H when in the hold mode. External synchronization is not required.

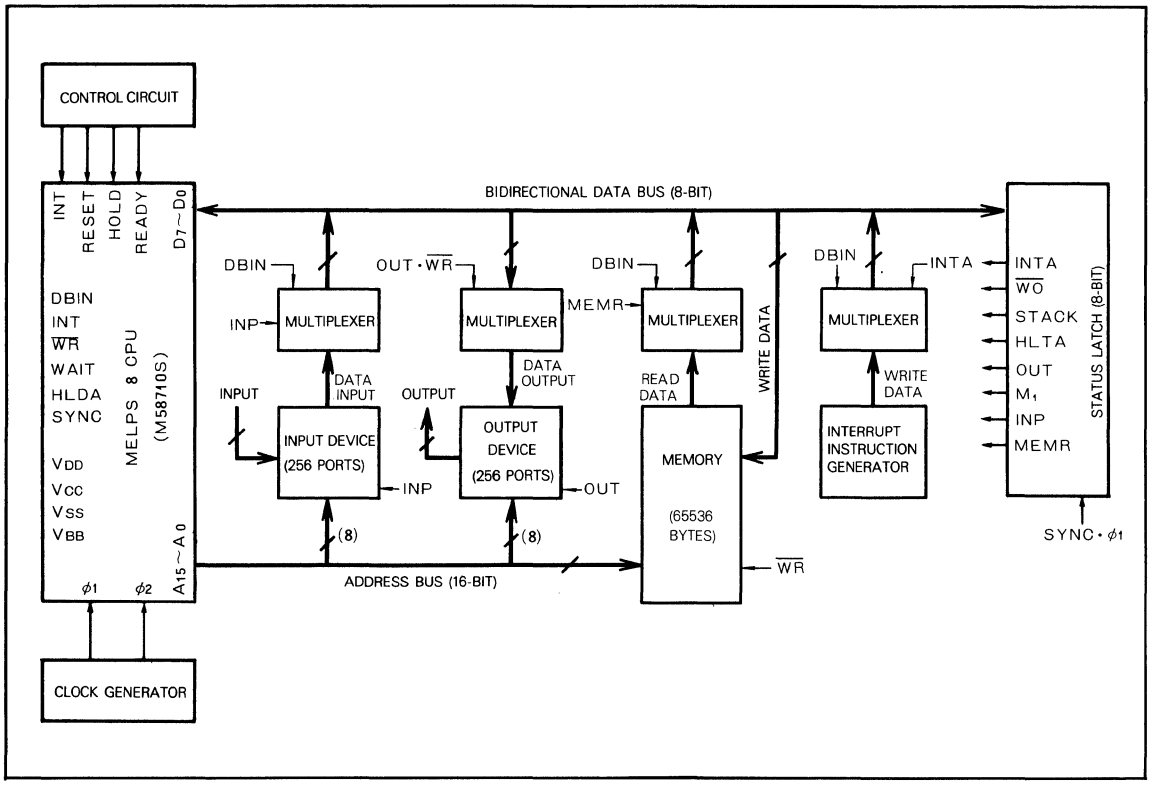
6 : The interrupt signal INT must be stable for the period immediately before the last state of any instruction in order to be recognized on the following machine cycle M_1. External synchronization is not required.

APPLICATIONS

A Basic System Using the M58710S

The configuration of a system using the M58710S will depend on the functions of the system. A typical basic system is shown in Fig. 1, and a summary of its operation is as follows:

Fig. 1 An example of a basic system using the M58710S



1. After the CPU receives the two phase clocks ϕ_1 and ϕ_2 from the clock generator and the external reset signal, the address bus provides the address to memory location zero.
2. At the same time the CPU sends out status signals, which are latched temporarily in the status latch (flip-flops in which status information is latched). The status signals alert external circuits as to the state of the machine cycle that the CPU is ready to execute. When the CPU calls for data or instructions to be read from memory, status signal MEMR is applied to the multiplexer, and the 8-bit data from memory is read into the CPU through the bidirectional data bus across the multiplexer.
3. The 8-bit data coming from memory is decoded as an instruction. If it is a register-reference-arithmetic instruction, it is executed in the CPU; if it is a move-to-memory instruction, the CPU outputs the memory location to the address bus and data to be written on the data bus in the next machine cycle (Note 1). The memory write in operation is executed by write control signal WR.
4. During input and output operation, the CPU outputs the I/O device number to the address bus, outputs a status signal (INP in the input mode; OUT in the output mode) and executes the read/write operation to the I/O devices using the bidirectional data bus.
5. If there is a signal from terminal INT to the CPU, the CPU is in the interrupt enable state, and it sends out status information INTA (Note 2), and an interrupt instruction is sent to the CPU from the interrupt instruction generator across the multiplexer. By executing this interrupt instruction, the CPU can jump to the interrupt processing subroutine.

Note 1 : Each instruction may have five machine cycles. For register-to-register transfer or arithmetic instruction, instruction fetching and execution are carried out by machine cycle M_1 but memory access instructions, or 2-byte or 3-byte instructions require more than one machine cycle.

2 : The interrupt acknowledge signal goes high when the CPU accepts an interrupt request (INT) signal.

Push-Down Stack Operation

The M58710S has a last-in first-out stack. This stack has a pointer that maintains the address of the next available stack location in memory and can be initialized to use any position of memory. Since the stack pointer has a 16-bit register, it can locate any stack location up to 65536 bytes according to memory capacity. An example of the interrupt request is shown in Fig. 2 and the operation of the stack pointer in Fig. 3.
plained as follows:

Fig. 2 Processing an interrupt request

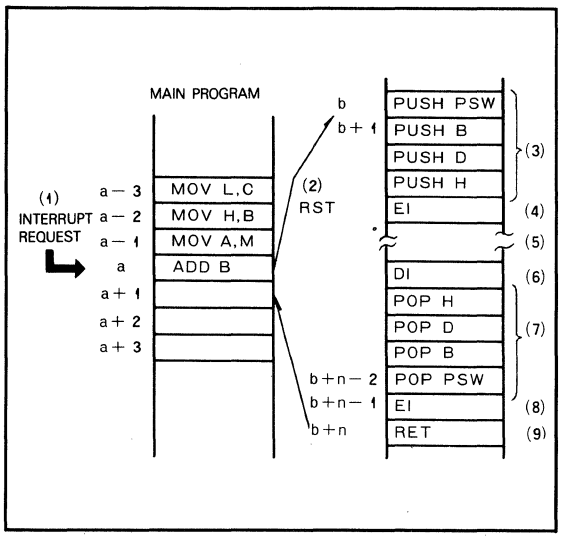


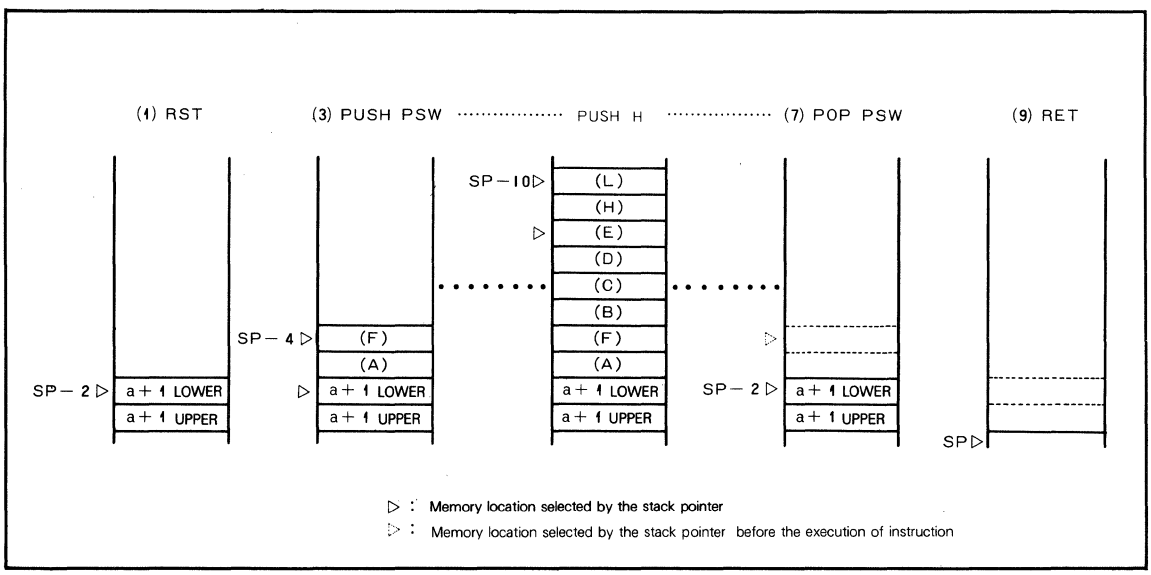
Fig. 2 is explained as follows:

1. An external interrupt request occurs when the CPU executes the instruction stored at location a in the main program.
2. Instruction RST is fetched, the content of the program counter is incremented and pushed onto the push-down stack. Then the CPU jumps to the first location b of the interrupt operation program.
3. The contents of the register are pushed onto the stack. F (in Fig. 3) indicates 8-bit data of flag flip-flops including CY_2, CY_1, Z, P and S. These are, from the most to the least significant bit, S, Z, 0, CY_1, 0, P, 1, CY_2.
4. Instruction EI is executed, enabling the CPU to accept the next interrupt request.
5. The interrupt operation is carried out.
6. The CPU enters the interrupt disable state.
7. The contents of registers are popped off the stack.
8. Instruction EI is executed, enabling the CPU to accept the interrupt request after return to the main program.
9. The content of the program counter is returned to location a+1 of the main program.

The operation of the push-down stack shown in Fig. 2 is described in Fig. 3, where SP indicates the content of the stack pointer before the interrupt is requested. Instruction LXI SP should be used to initialize the stack pointer.
the stack pointer.

The content of the stack pointer is SP-4 at (3), but at (9), after the execution of instruction RET, it returns to the initial state, and the content of the stack point is SP.

Fig. 3 Operation of the push-down stack



RANDOM-ACCESS MEMORIES

5

256-BIT (256-WORD BY 1-BIT) STATIC RANDOM-ACCESS MEMORY

DESCRIPTION

The M58531P is a 256-word by 1-bit P-channel silicon-gate MOS static RAM, designed for applications where ease of use is the important design object. Both inputs and outputs are fully compatible with TTL.

FEATURES

- Fast access time: 850ns (typ) 1,500ns (max)
- Low standby power: 0.7mW/bit (typ)
- Low operating power: 1.4mW/bit (typ)
- All inputs/outputs are fully compatible with TTL
- Three-state output and OR-tie capability
- Easy memory expansion by chip select signal
- Interchangeable with Intel's 1101A in pin configuration and electrical characteristics

APPLICATION

- Small-capacity memory systems

FUNCTION

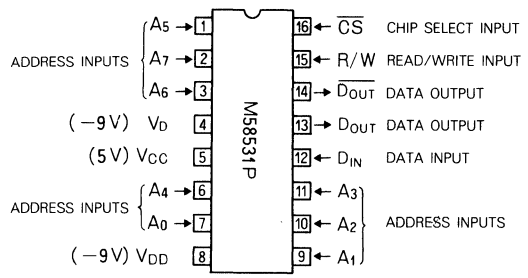
Static design eliminates external clocks and refresh circuitry. All inputs and outputs are fully compatible with TTL.

In the write mode, address signals $A_0 \sim A_7$ are used to select storage locations, and when signal R/W remains high the data of signal D_{IN} are writeen.

In the read mode, address signals $A_0 \sim A_7$ are used to select storage locations, and when signal R/W remains low the data of the selected location is read out to the D_{OUT} terminals.

When signal $\overline{CS}$ is high, the chip is deselected, disabling both read and write operations and enabling the OR-tie with other output terminals since the outputs are in the floating (high-impedance) state.

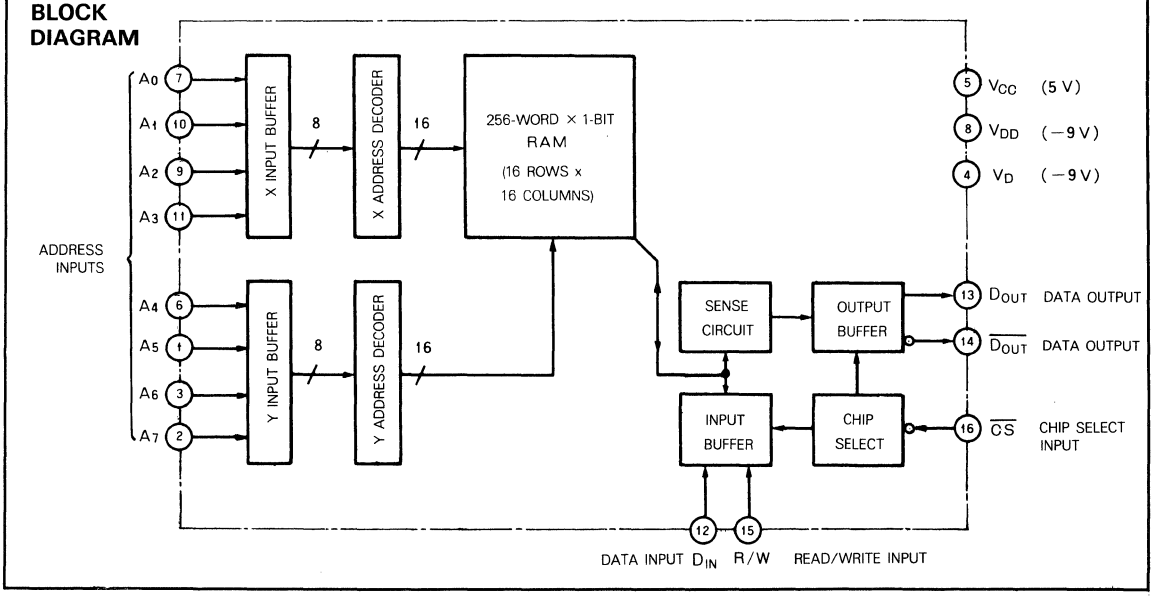
PIN CONFIGURATION (TOP VIEW)



Outline 16P1

The M58531P has two power supply terminals, V_{DD} for the memory cell part in which the data is stored, and V_D for the read/write control circuit. Power dissipation is low since, during standby, current is supplied only to the memory cell part for data storage, and read/write operation is not performed.

BLOCK DIAGRAM



256-BIT (256-WORD BY 1-BIT) STATIC RANDOM-ACCESS MEMORY

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{DD}	Supply voltage	With respect to V_{CC}	0.3～−20	V
V_D	Supply voltage		0.3～−20	V
V_I	Input voltage		0.3～−20	V
V_O	Output voltage		0.3～−20	V
Pd	Power dissipation	Ta=25°C	700	mW
Topr	Operating free-air temperature range		−10～75	°C
Tstg	Storage temperature range		−40～125	°C

RECOMMENDED OPERATING CONDITIONS (Ta=−10～75°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{DD}	Supply voltage	−9.45	−9	−8.55	V
V_D	Supply voltage	−9.45	−9	−8.55	V
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IL}	Low-level input voltage	V_{CC}-15		Vcc-4.5	V
V_{IH}	High-level input voltage	V_{CC}-2		Vcc+0.3	V

ELECTRICAL CHARACTERISTICS (Ta=−10～75°C, V_{CC}=5V±5%, V_{DD}=−9V±5%, V_D=−9V±5%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		Vcc−2		Vcc+0.3	V
V_{IL}	Low-level input voltage		Vcc−15		Vcc−4.5	V
V_{OH}	High-level output voltage	I_{OH}=−100μA	3.5	4.9		V
V_{OL}	Low-level output voltage	I_{OL}=2mA			0.45	V
I_I	Input current	V_I-V_{CC}=−15V			−1	μA
I_{OZ}	Off-state input current	V_O-V_{CC}=−5V, $V_{I(CS)}=V_{CC}-2V$			−1	μA
I_{OH}	High-level output current	V_D=0V		−2	−7	mA
I_{OL}	Low-level output current	V_O=0.45V	2			mA
I_{DD}	Supply current from V_{DD}	I_O=0mA Ta=25°C		−13	−19	mA
I_D	Supply current from V_D	I_O=0mA Ta=25°C		−12	−18	mA
C_i	Input capacitance	$V_I=V_{CC}$ f=1MHz, Ta=25°C		7	10	pF
Co	Output capacitance	$V_O=V_{CC}$ f=1MHz, Ta=25°C		7	10	pF
$C_{(V_D)}$	Capacitance, V_D power supply	$V_D=V_{CC}$ f=1MHz, Ta=25°C		20	35	pF

Note 1 : Current flowing into an IC is positive; out is negative.

SWITCHING CHARACTERISTICS (Ta=−10～75°C, V_{CC}=5V±5%, V_{DD}=−9V±5%, V_D=−9V±5%, unless otherwise noted)

Read Cycle

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{C(RD)}$	Read cycle time	(Note 3)	1.5			μs
$t_{su(\overline{CS})}$	Chip select setup time				1.2 (Note 2)	μs
$t_{a(AD)}$	Address access time			0.85	1.5	μs

Note 2 : Maximum value of $t_{su(\overline{CS})}$ measured at minimum read cycle (1.5μs)

256-BIT (256-WORD BY 1-BIT) STATIC RANDOM-ACCESS MEMORY

Write Cycle

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{c(WR)}$	Write cycle time	(Note 3)	0.8			μs
$t_{su(WR)}$	Write setup time		0.3			μs
$t_{w(WR)}$	Write pulse width		0.4			μs
$t_{su(DA)}$	Data setup time		0.3			μs
$t_{h(DA)}$	Data hold time		0.1			μs

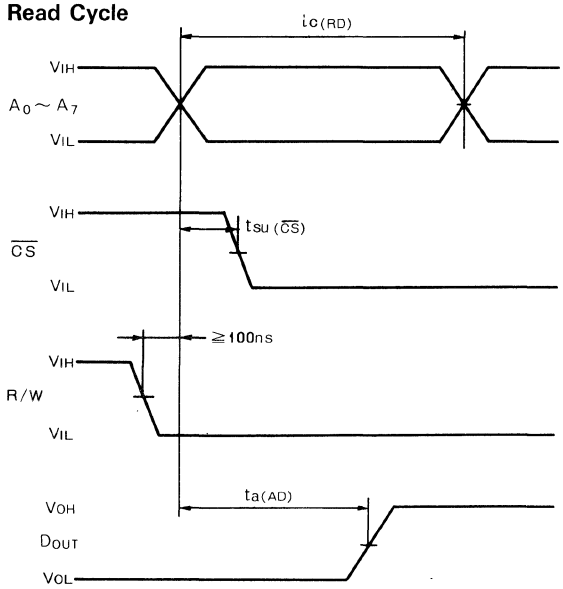
Chip Select and Deselect

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{w(\overline{CS})}$	Chip select pulse width	(Note 3)	0.4			μs
$t_{a(\overline{CS})}$	Chip select access time			0.2	0.3	μs
$t_{dv(\overline{CS})}$	Data valid time with respect to chip select			0.1	0.3	μs

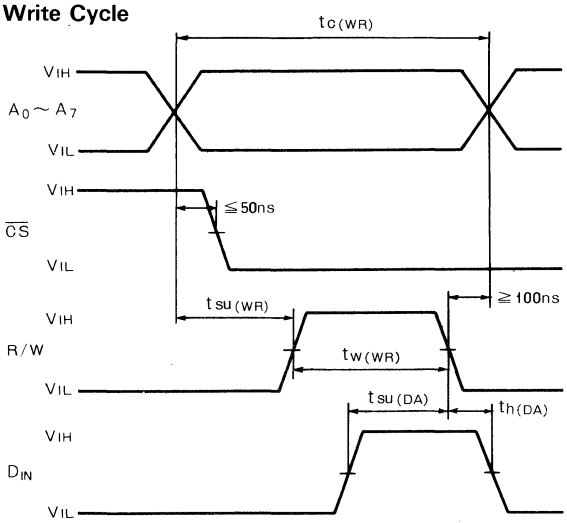
Note 3 : Input voltage waveform has an amplitude of 0~5V and $t_r = t_f = 10$ns Output load is one TTL gate and a 20pF capacitance. Unless otherwise noted, the reference points are the 1.5V level of the output of a TTL gate ($t_{PD} \leqq 10$ns)

TIMING DIAGRAMS

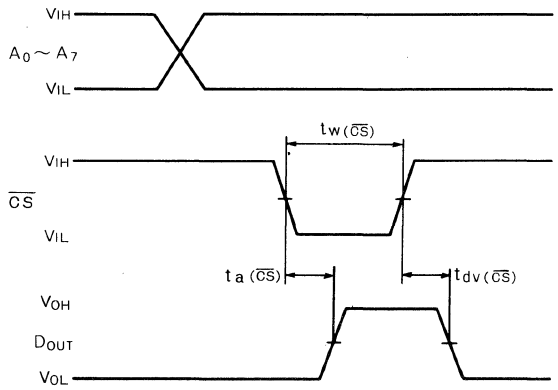
Read Cycle



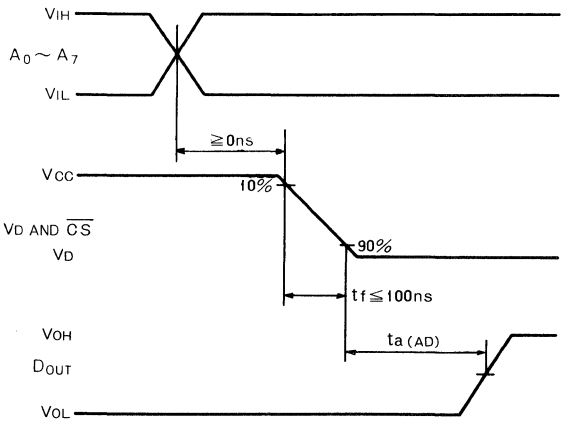
Write Cycle



Chip Select and Deselect



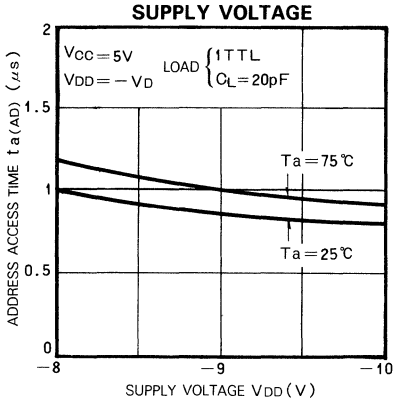
VD Power Supply Switching



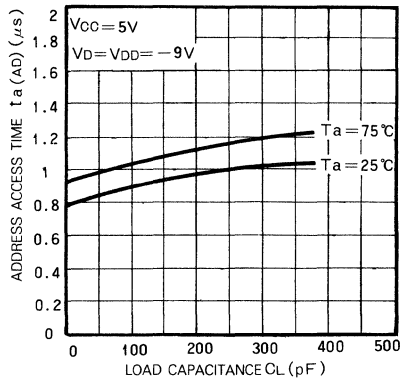
256-BIT (256-WORD BY 1-BIT) STATIC RANDOM-ACCESS MEMORY

TYPICAL CHARACTERISTICS

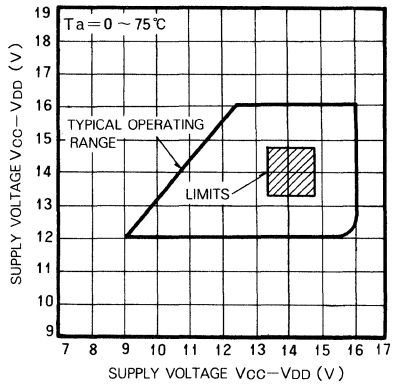
ADDRESS ACCESS TIME VS. SUPPLY VOLTAGE



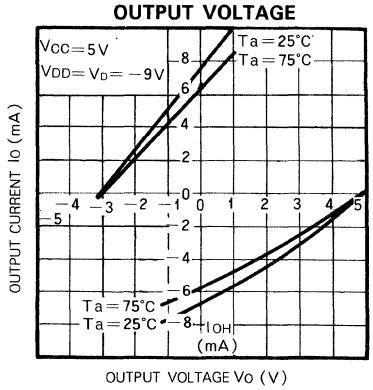
ADDRESS ACCESS TIME VS. LOAD CAPACITANCE



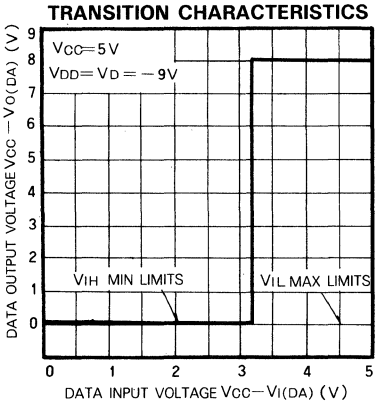
SUPPLY VOLTAGE OPERATING RANGE



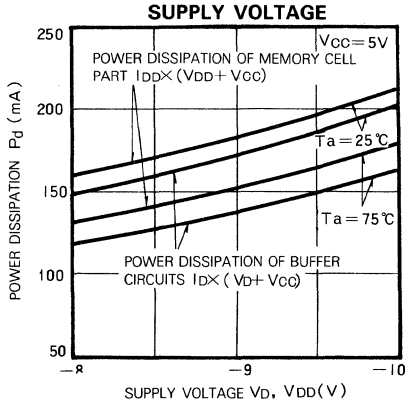
OUTPUT CURRENT VS. OUTPUT VOLTAGE



DATA TERMINAL INPUT/OUTPUT TRANSITION CHARACTERISTICS



POWER DISSIPATION VS. SUPPLY VOLTAGE



MITSUBISHI ELECTRIC

1024-BIT (1024-WORD BY 1-BIT) DYNAMIC RANDOM-ACCESS MEMORY

DESCRIPTION

The M58533P is a 1024-word by 1-bit P-channel silicon-gate MOS RAM, designed for applications where utilization of the high-speed low-power characteristics peculiar to dynamic circuitry is the important design object.

FEATURES

- Fast access time: 300ns (max) (Ta = 0~70°C)
- Fast cycle time: 580ns (min) (Ta = 0~70°C)
- Refresh interval: 2ms (max) (Ta = 0~70°C)
- Low standby power: 50μW/bit (typ)
- Low operating power: 0.25mW/bit (typ)
- Output terminal has OR-tie capability
- Easy memory expansion by chip enable input
- Interchangeable with Intel's 1103 in pin configuration and electrical characteristics

APPLICATION

- Main memory of computers
- Memory for Chinese-character printer

FUNCTION

The M58533P has the following four function cycles:

READ—when an address is designated by address signals A_0~A_9 and R/W is turned high, data in the designated address is read out to the output.

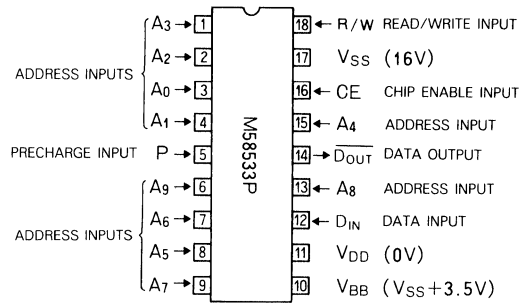
WRITE—when an address is designated by address signals A_0~A_9 and the low-level write pulse is applied to the R/W terminal, data input during that time is written.

READ/WRITE (READ-MODIFY-WRITE)—In the write cycle, if data that is read out from the output terminals is treated as effective data during the period before the write pulse is applied, both read and write operations are performed in one cycle.

REFRESH—This cycle periodically refreshes the dynamically memorized data, and it is performed by designating the address of A_0~A_4 in the read cycle.

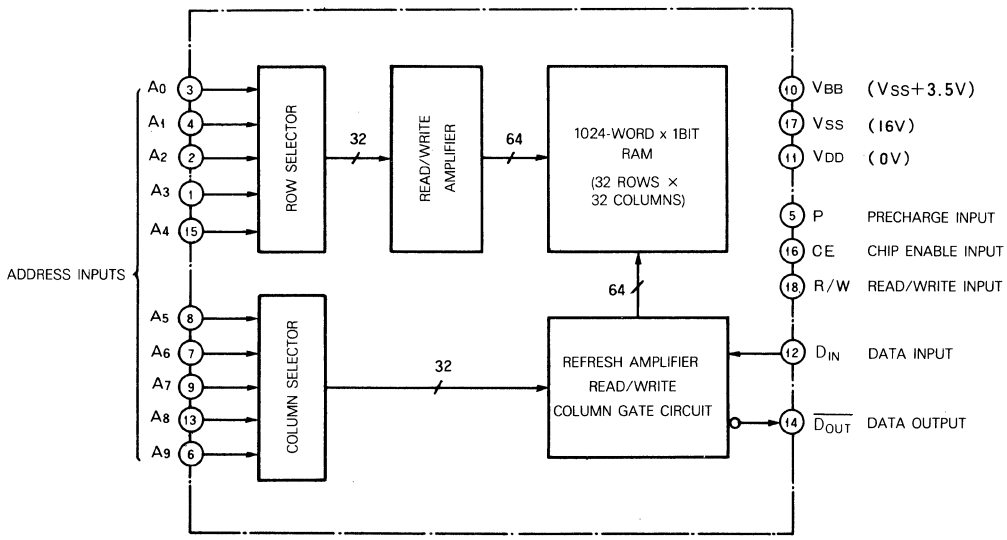
The output can go to the floating (high-impedance) state when chip enable goes high, and the output can then be OR-tied.

PIN CONFIGURATION (TOP VIEW)



Outline 18P1

BLOCK DIAGRAM



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1024-BIT (1024-WORD BY 1-BIT) DYNAMIC RANDOM-ACCESS MEMORY

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{DD}	Supply voltage	With respect to V_{BB}	0.3～－25	V
V_{SS}	Supply voltage		0.3～－25	V
V_I	Input voltage		0.3～－25	V
V_O	Output voltage		0.3～－25	V
Pd	Power dissipation	Ta＝25°C	700	mW
Topr	Operating free-air temperature range		0～70	°C
Tstg	Storage temperature range		－40～125	°C

RECOMMENDED OPERATING CONDITIONS (Ta＝0～70°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Nom	Max	
V_{SS}	Supply voltage		15.2	16	16.8	V
$V_{BB}-V_{SS}$	Supply voltage		3	3.5	4	V
V_{DD}	Supply voltage	GND		0		V
V_{IH}	High-level input voltage		$V_{SS}-1$		$V_{SS}+1$	V
V_{IL}	Low-level input voltage		$V_{SS}-17$		$V_{SS}-15$	V
R_L	Load resistance	Between $\overline{D_{OUT}}$ and V_{DD}	0.1		1	kΩ

ELECTRICAL CHARACTERISTICS (Ta＝0～70°C, V_{SS}＝16V±5%, $V_{BB}-V_{SS}$＝3V～4V, V_{DD}＝0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage, all inputs		$V_{SS}-1$		$V_{SS}+1$	V
$V_{IL(P,CE,R/W)}$	Low-level input voltage, P, CE and R/W		$V_{SS}-17$		$V_{SS}-15$	V
$V_{IL(AD,DA)}$	Low-level input voltage, AD and DA		$V_{SS}-17$		$V_{SS}-14.5$	V
I_I	Input leakage current, all inputs	V_I＝0V			－1	μA
I_{OH}	High-level output current	V_O＝0V	－500	－800	－4000	μA
I_{OL}	Low-level output current				－1	μA
I_{BB}	Supply current from V_{BB}				100	μA
I_{DD1}	Supply current from V_{DD}	$V_{I(AD)}$＝$V_{I(P)}$＝0V, $V_{I(CE)}$＝V_{SS}, Ta＝25°C		－37	－56	mA
I_{DD2}	Supply current from V_{DD}	$V_{I(AD)}$＝$V_{I(P)}$＝$V_{I(CE)}$＝0V, Ta＝25°C		－38	－59	mA
I_{DD3}	Supply current from V_{DD}	$V_{I(P)}$＝V_{SS}, $V_{I(CE)}$＝0V, Ta＝25°C		－5.6	－11	mA
I_{DD4}	Supply current from V_{DD}	$V_{I(P)}$＝V_{SS}, $V_{I(CE)}$＝V_{SS}, Ta＝25°C		－3	－4	mA
$I_{DD(AV)}$	Average supply current from V_{DD}	tc＝580ns, $t_{W(P)}$＝190ns, Ta＝25°C		－17	－25	mA
$C_{i(A_0-A_9)}$	Input capacitance, AD	V_I＝V_{SS}, V_i＝25mVrms, f＝1MHz		5	7	pF
$C_{i(P,CE)}$	Input capacitance, P and CE			15	18	pF
$C_{i(R/W)}$	Input capacitance, R/W			11	15	pF
$C_{i(DA)}$	Input capacitance, DA			3	5	pF
$C_{O(DA)}$	Output capacitance	V_O＝V_{DD}, V_o＝25mVrms, f＝1MHz		2	3	pF

Note 1 : Current flowing into an IC is positive; out is negative.

2 : Output voltage is defined as follows: $V_{OH}=V_{DD}-R_L \cdot I_{OH}$, $V_{OL}=V_{DD}-R_L \cdot I_{OL}$

1024-BIT (1024-WORD BY 1-BIT) DYNAMIC RANDOM-ACCESS MEMORY

TIMING REQUIREMENTS (For Read, Write, or Read-Modify-Write Cycle)

($Ta = 0 \sim 70°C$, $V_{SS} = 16V \pm 5\%$, $V_{BB} - V_{SS} = 3 \sim 4V$, $V_{DD} = 0V$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{c(REF)}$	Refresh cycle time	See timing diagram for read, write and read-modify-write cycles			2	ms
$t_{su(AD-CE)}$	Address setup time with respect to chip enable		115			ns
$t_{su(CE-AD)}$	Chip enable setup time with respect to address		20			ns
$t_{su(P-CE)}$	Precharge setup time with respect to chip enable		125			ns
$t_{d(PL-CEL)}$	Delay time, precharge low to chip enable low				75	ns
$t_{d(PH-CEH)}$	Delay time, precharge high to chip enable high				140	ns
$t_{su(CE-P)}$	Chip enable setup time with respect to precharge		85			ns

SWITCHING CHARACTERISTICS ($Ta = 0 \sim 70°C$, $V_{SS} = 16V \pm 5\%$, $V_{BB} - V_{SS} = 3V \sim 4V$, $V_{DD} = 0V$, unless otherwise noted)

Read Cycle

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{c(RD)}$	Read cycle time	See timing diagram for read cycle $tr = tf = 20ns$, $C_L = 100pF$ $R_{LOAD} = 100\Omega$, $V_{REF} = 40mV$	480			ns
$t_{h(CE)}$	Chip enable hold time		165		500	ns
$t_{a(P,LH)}$	Precharge low-to-high access time				120	ns
$t_{a(AD)}$	Address access time		300			ns
$t_{a(P,HL)}$	Precharge high-to-low access time		310			ns

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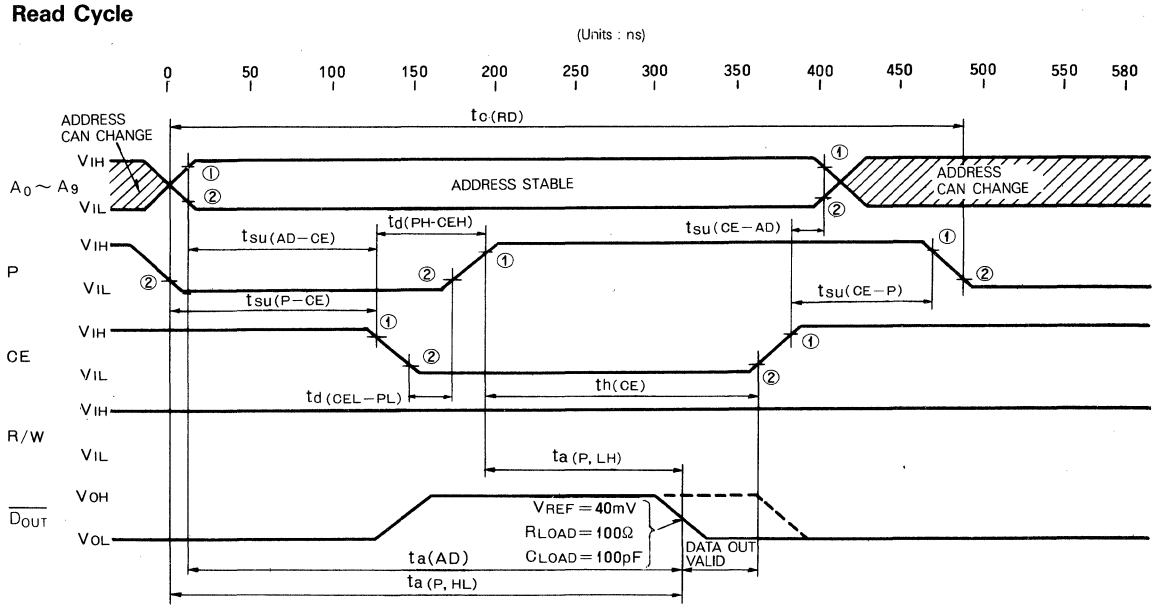
Write or Read-Modify-Write Cycle

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{c(WR)}$	Write-cycle time	See timing diagram for read, write and read-modify-write cycle. $C_L = 100pF$ $R_L = 100\Omega$ $V_{REF} = 40mV$ $tr = tf = 20ns$	580			ns
$t_{c(RMW)}$	Read-modify-write cycle time		580			ns
$t_{su(P-WR)}$	Precharge setup time with respect to write		165			ns
$t_{w(WR)}$	Write pulse width		50			ns
$t_{su(WRHL)}$	Write setup time with respect to high-to-low output		80			ns
$t_{su(DA)}$	Data setup time		105			ns
$t_{h(DA)}$	Data hold time		10			ns
$t_{a(P,LH)}$	Precharge low-to-high access time				120	ns
$t_{su(WRLH)}$	Write setup time with respect to low-to-high output		0			ns

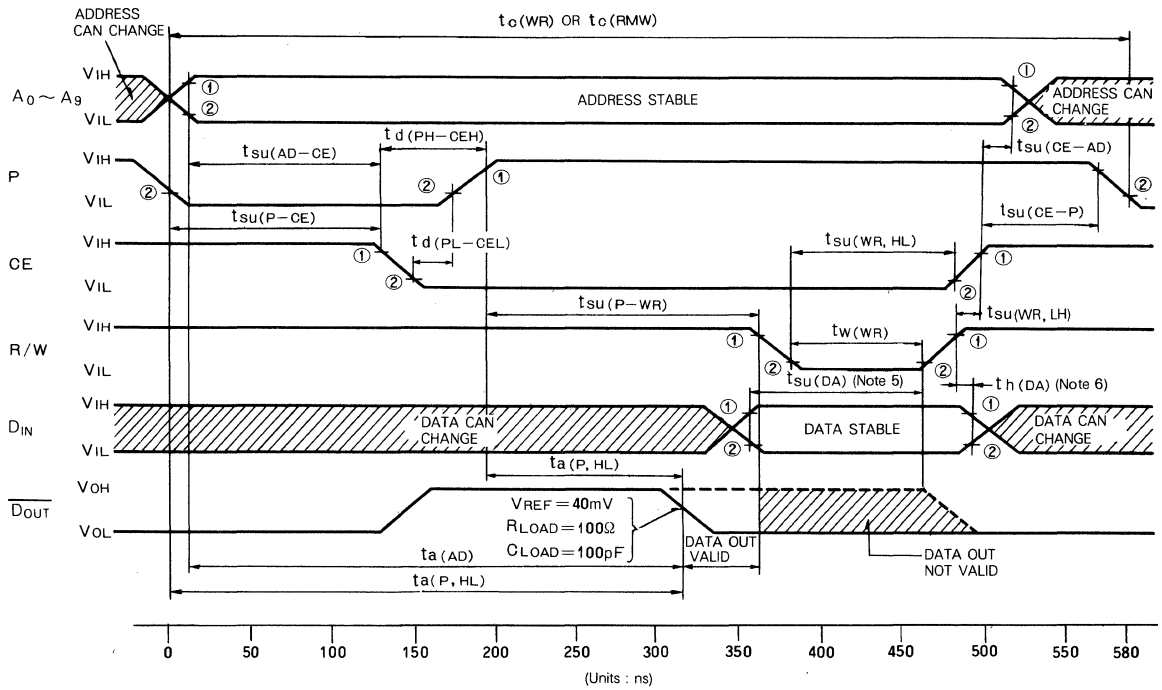
1024-BIT (1024-WORD BY 1-BIT) DYNAMIC RANDOM-ACCESS MEMORY

TIMING DIAGRAMS

Read Cycle



Write or Read-Modify-Write Cycle



Note 3 : The reference level of point ① is $V_{SS}-2V$, and point ② is $V_{DD}+2V$.

4 : t_T is defined as the transition time between point ① and point ②.

5 : $t_{su(DA)}$ is referenced to point ② of the rising edge of CE or R/W .

6 : $t_{h(DA)}$ is referenced to point ① of the rising edge of CE or R/W .

7 : $t_{a(AD)}=t_{su(AD-CE)}min+t_{d(PL-CEL)}+t_{a(P,LH)}max+2t_T$

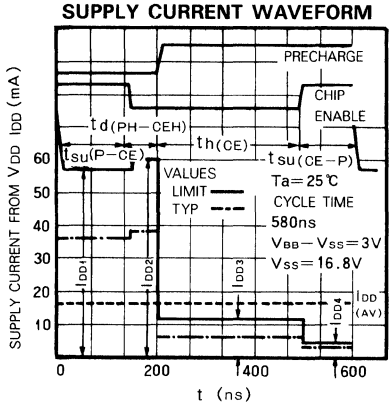
8 : $t_{a(P,HL)}=t_{su(P-CE)}min+t_{d(PL-CEL)}+t_{a(P,LH)}max+2t_T$

MITSUBISHI ELECTRIC

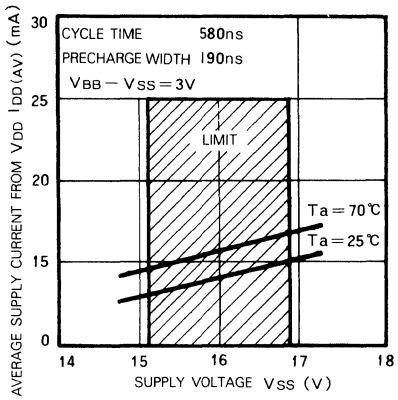
1024-BIT (1024-WORD BY 1-BIT) DYNAMIC RANDOM-ACCESS MEMORY

TYPICAL CHARACTERISTICS

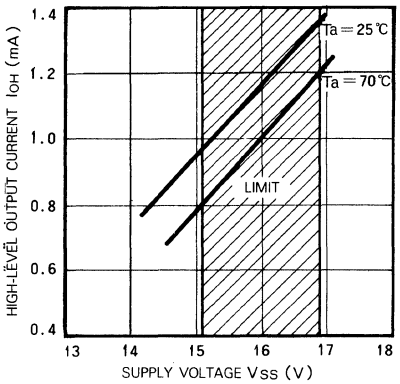
SUPPLY CURRENT WAVEFORM



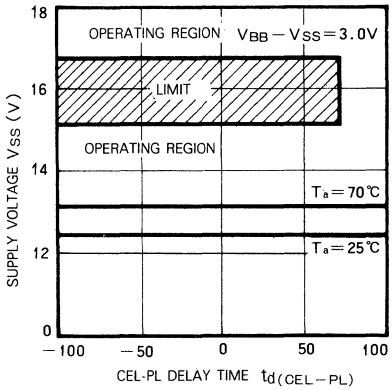
AVERAGE SUPPLY CURRENT FROM VDD VS. SUPPLY VOLTAGE VSS



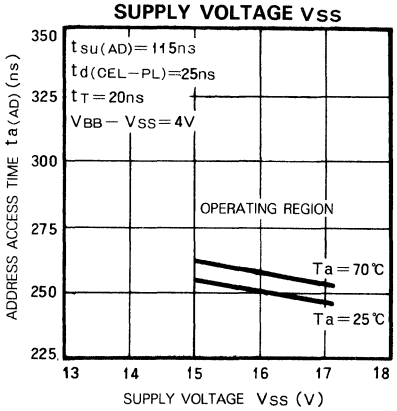
HIGH-LEVEL OUTPUT CURRENT VS. SUPPLY VOLTAGE VSS



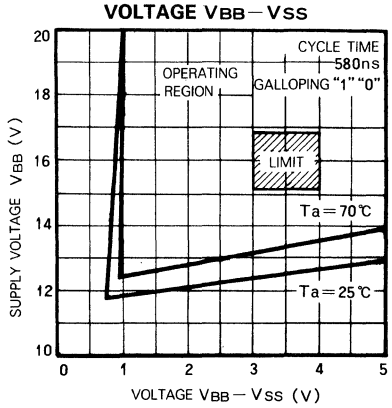
SUPPLY VOLTAGE VS. CEL-PL DELAY TIME



ADDRESS ACCESS TIME VS. SUPPLY VOLTAGE VSS



SUPPLY VOLTAGE VS. VOLTAGE VBB−VSS



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M58751P, M58751S

Alternative Designation 2102A

1024-BIT (1024-WORD BY 1-BIT) STATIC RANDOM-ACCESS MEMORY

DESCRIPTION

The M58751P and M58751S are 1024-word by 1-bit N-channel silicon-gate MOS static RAMs, designed for applications where ease of use is the important design object. Both operate by a single 5V power supply, as does TTL, and all inputs and output are directly compatible with TTL.

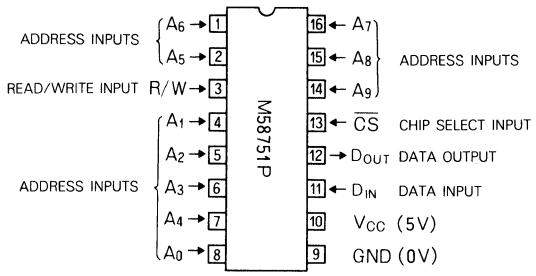
FEATURES

- Fast access time: 450ns (max)
- Low power dissipation: 100μW/bit (typ)
- Single 5V power supply
- Data holding at 1.5V supply voltage is possible
- Requires no external clock or refreshing
- All inputs and output are directly compatible with TTL
- Three-state output and OR-tie capability
- Easy memory expansion by chip select input
- Both M58751P and M58751S are interchangeable with Intel's 2102A-4 in pin configuration and electrical characteristics

APPLICATION

- Small-capacity memory systems

PIN CONFIGURATION (TOP VIEW)



Outline 16P1 (M58751P)
16S1 (M58751S)

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FUNCTION

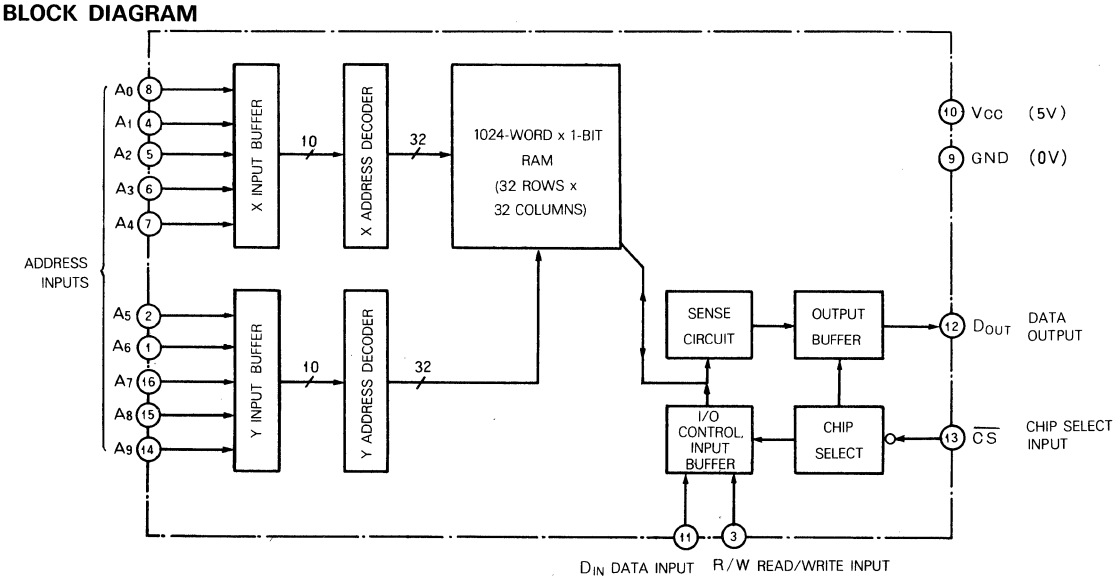
Static design makes the M58751P and M58751S convenient to use as they require no external clocks or refreshing, and all inputs and output are directly compatible with TTL.

During writing operation, when a location is designated by address signals A_0~A_9 and R/W goes low, D_{IN} at that time is written; during reading operation, when a location is designated by address signals A_0~A_9 and R/W goes high, data of the designated address is taken from the D_{OUT} terminal.

When $\overline{CS}$ is high, the chip is in the non-selectable state, disabling both reading and writing operations of the device. In this case the output is in the floating (high impedance) state enabling OR-tie to other outputs.

The memory data is held when supply voltage drops to 1.5V, enabling battery back-up operation during power stoppages and low-power operation during standby.

BLOCK DIAGRAM



M58751P, M58751S

Alternative Designation 2102A

1024-BIT (1024-WORD BY 1-BIT) STATIC RANDOM-ACCESS MEMORY

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Conditions	Limits	Unit
V_{CC}	Supply voltage		With respect to GND	−0.3～7	V
V_I	Input voltage			−0.3～7	V
V_O	Output voltage			−0.3～7	V
P_d	Power dissipation	M58751P	Ta＝25°C	700	mW
		M58751S		1000	mW
T_{opr}	Operating free-air temperature range			0～70	°C
T_{stg}	Storage temperature range	M58751P		−40～125	°C
		M58751S		−65～150	°C

RECOMMENDED OPERATING CONDITIONS (Ta＝0～70°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	V
V_{IL}	Low-level input voltage	0		0.65	V
V_{IH}	High-level input voltage	2.2		V_{CC}	V

ELECTRICAL CHARACTERISTICS (Ta＝0～70°C, V_{CC}＝5V±5%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2.2		Vcc	V
V_{IL}	Low-level input voltage		0		0.65	V
V_{OH}	High-level output voltage	I_{OH}＝−200μA	2.4			V
V_{OL}	Low-level output voltage	I_{OL}＝2.1mA			0.4	V
I_I	Input current	V_I＝0～5.25V			10	μA
I_{OZH}	Off-state high-level output current	$V_I(\overline{CS})$＝2.2V, V_O＝2.4V～V_{CC}			10	μA
I_{OZL}	Off-state low-level output current	$V_I(\overline{CS})$＝2.2V, V_O＝0.4V			−10	μA
I_{CC}	Supply current from V_{CC}	V_I＝5.25 (all inputs), output open		20	40	mA
Ci	Input capacitance, all inputs	V_I＝GND, V_i＝25mV$_{rms}$, f＝1MHz		3	5	pF
Co	Output capacitance	V_O＝GND, V_o＝25mV$_{rms}$, f＝1MHz		7	10	pF

POWER-DOWN CHARACTERISTICS (Ta＝0～70°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$V_{CC(PD)}$	Power-down supply voltage		1.5			V
$V_I(\overline{CS})$	Power-down chip select voltage	2.2V≦$V_{CC(PD)}$≦V_{CC}	2.2			V
		1.5V≦$V_{CC(PD)}$≦2.2V	$V_{CC(PD)}$			V
$I_{CC(PD1)}$	Power-down supply current	V_{CC}＝1.5V, all inputs＝1.5V		13	25	mA
$I_{CC(PD2)}$	Power-down supply current	V_{CC}＝2.0V, all inputs＝2.0V		15	30	mA

Note : Current flowing into an IC is positive ; out is negative.

1024-BIT (1024-WORD BY 1-BIT) STATIC RANDOM-ACCESS MEMORY

SWITCHING CHARACTERISTICS (Ta=0~70°C, Vcc=5V±5%, unless otherwise noted)

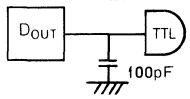
Read Cycle

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{c(RD)}$	Read cycle time	Input pulse V_{IH}=2.2V	450			ns
$t_{a(AD)}$	Address access time	V_{IL}=0.65V			450	ns
$t_{a(\overline{CS})}$	Chip select access time	tr=tf=20ns			230	ns
$t_{dv(AD)}$	Data valid time with respect to address	Reference level 1.5V	40			ns
$t_{dv(\overline{CS})}$	Data valid time with respect to chip select	Load=1TTL, C_L=100pF	0			ns

TIMING REQUIREMENTS (Ta=0~70°C, Vcc=5V±5%, unless otherwise noted)

Write Cycle

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{c(WR)}$	Write cycle time	Input pulse V_{IH}=2.2V	450			ns
$t_{su(AD)}$	Address setup time	V_{IL}=0.65V	20			ns
$t_{w(WR)}$	Write pulse width	tr=tf=20ns	300			ns
$t_{h(DA)}$	Data hold time	Reference level =1.5V	50			ns
$t_{su(DA)}$	Data setup time	Load=1TTL, C_L=100pF	300			ns
t_{WR}	Write recovery time		0			ns
$t_{su(\overline{CS})}$	Chip select setup time		300			ns

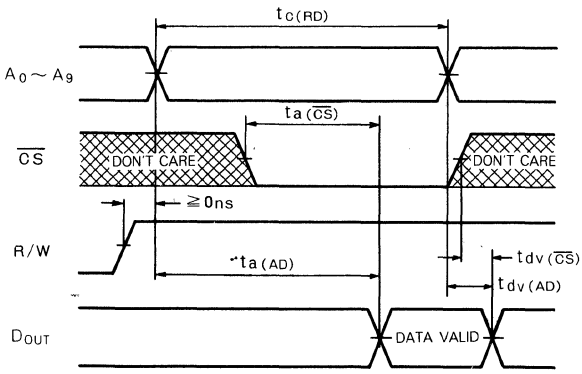


Power-Down Operation

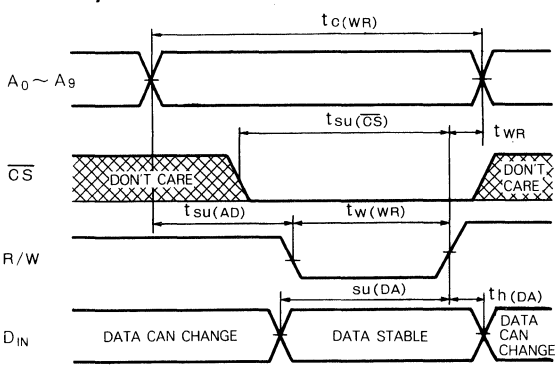
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(PD)}$	Power-down setup time		0			ns
$t_{R(PD)}$	Power-down recovery time		$t_{c(RD)}$			ns

TIMING DIAGRAMS

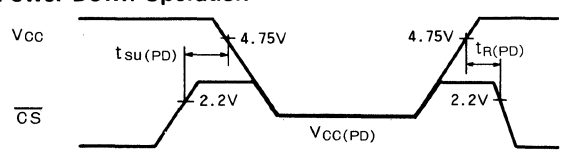
Read Cycle



Write Cycle



Power-Down Operation



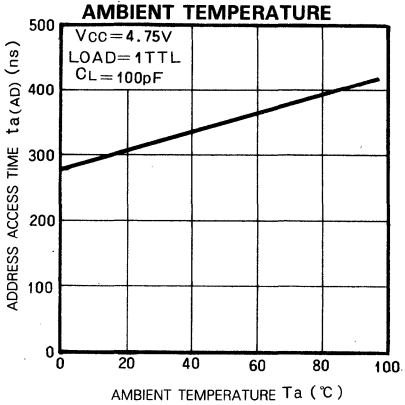
M58751P, M58751S

Alternative Designation 2102A

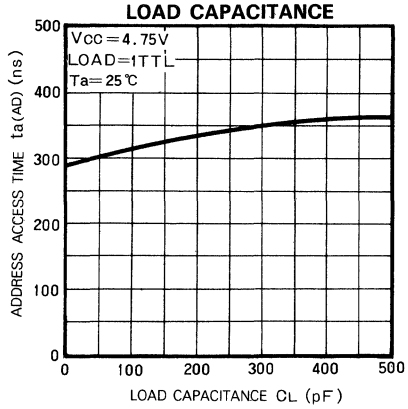
1024-BIT (1024-WORD BY 1-BIT) STATIC RANDOM-ACCESS MEMORY

TYPICAL CHARACTERISTICS

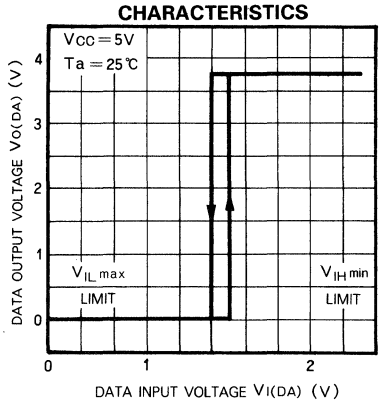
ADDRESS ACCESS TIME VS. AMBIENT TEMPERATURE



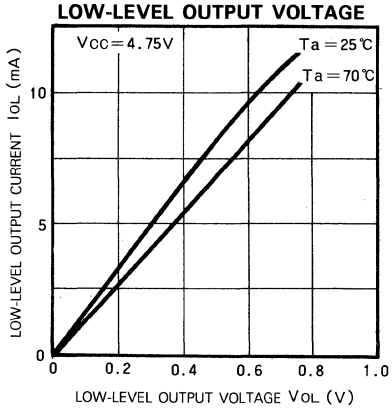
ADDRESS ACCESS TIME VS. LOAD CAPACITANCE



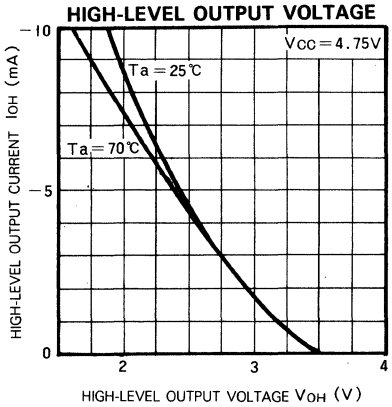
DATA INPUT-OUTPUT TRANSFER CHARACTERISTICS



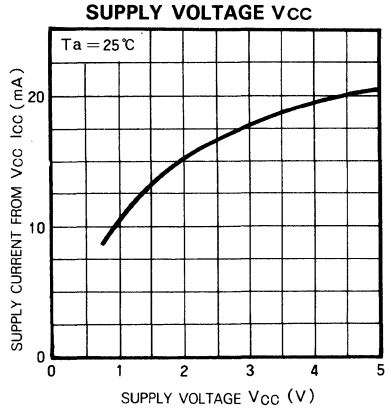
LOW-LEVEL OUTPUT CURRENT VS. LOW-LEVEL OUTPUT VOLTAGE



HIGH-LEVEL OUTPUT CURRENT VS. HIGH-LEVEL OUTPUT VOLTAGE



SUPPLY CURRENT FROM Vcc VS. SUPPLY VOLTAGE Vcc



M58755S-1, M58755S-2, M58755S-3

Alternative Designation 2107B

4096-BIT (4096-WORD BY 1-BIT) DYNAMIC RANDOM-ACCESS MEMORY

DESCRIPTION

The M58755S series consists of three 4096-word by 1-bit dynamic RAMs, fabricated with the N-channel silicon-gate MOS process. These RAMs are designed for large-capacity memory systems where high speed, low power dissipation and low cost are important design objects.

FEATURES

Symbol	M58755S−1	M58755S−2	M58755S−3
Access time (max)	200ns	270ns	150ns
Cycle time (min)	400ns	470ns	320ns
Minimum cycle power dissipation (typ)	300mW	240mW	350mW

- Low standby power: 0.03μW/bit (typ)
- Voltage range for all power supplies (V_{DD}, V_{CC}, V_{BB}): ±10%
- Refresh interval: 2ms (Ta = 0~70°C)
- Refresh addresses: A_0, A_1, A_2, A_3, A_4, A_5
- All input terminals except CE are directly TTL compatible
- Memory expansion is enabled by chip select input
- Output can be in the floating (high-impedance) state when $\overline{CS}$ is high or CE is low.
- Interchangeable with Intel's 2107B and TI's TMS4060

APPLICATION

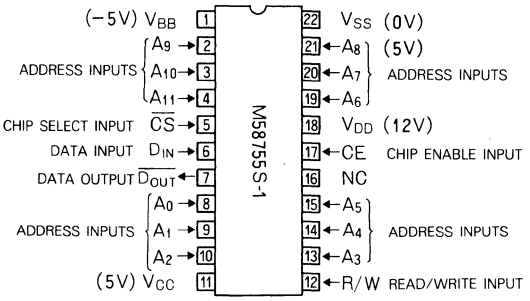
- Main memory unit for computers

FUNCTION

A location is designated by address signals A_0~A_{11}, and reading from and writing to that location is controlled by R/W. When $\overline{CS}$ is high, the chip is in the non-selectable state, disabling both read and write operations.

The devices are dynamic RAMs, and must be refreshed every 2ms to hold data stored in the memory cells. Refreshing is performed by reading sequentially the 64 locations designated by the 6 address signals A_0~A_5.

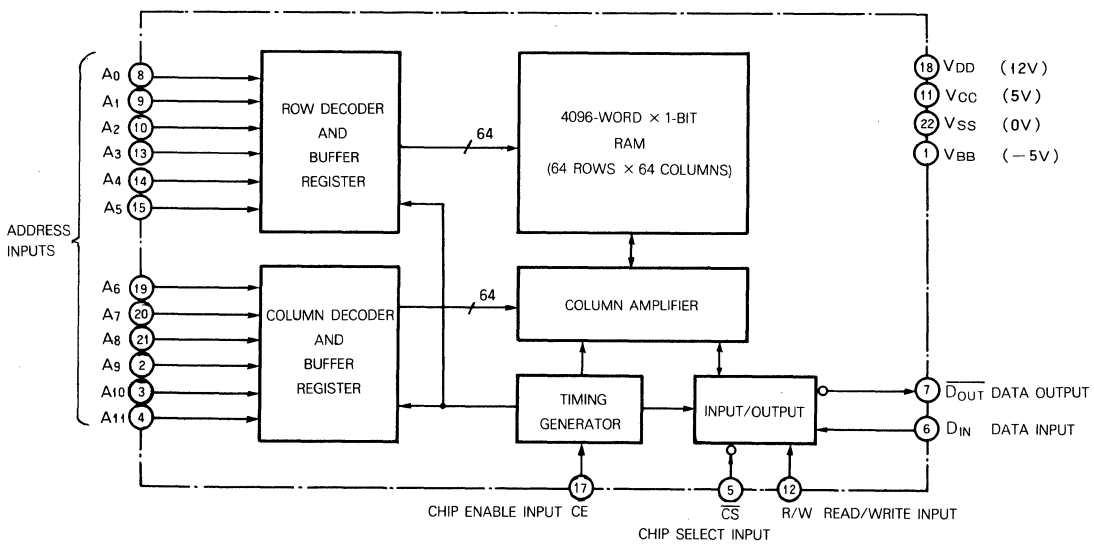
PIN CONFIGURATION (TOP VIEW)



NC= NO CONNECTION

Outline 22S1

BLOCK DIAGRAM



M58755S-1, M58755S-2, M58755S-3

Alternative Designation 2107B

4096-BIT (4096-WORD BY 1-BIT) DYNAMIC RANDOM ACCESS MEMORY

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{DD}	Supply voltage	With respect to V_{BB} (substrate)	−0.3～20	V
V_{CC}	Supply voltage		−0.3～20	V
V_{SS}	Supply voltage		−0.3～20	V
V_I	Input voltage		−0.3～20	V
V_O	Output voltage		−0.3～20	V
P_d	Power dissipation	Ta＝25°C	1000	mW
T_{opr}	Operating free-air temperature range		0～70	°C
T_{stg}	Storage temperature range		−55～150	°C

RECOMMENDED OPERATING CONDITIONS (Ta＝0～70°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{DD}	Supply voltage	10.8	12	13.2	V
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{BB}	Supply voltage	−4.5	−5	−5.5	V
$V_{IH(CE)}$	High-level chip enable input voltage	V_{DD}−1		V_{DD}+1	V
V_{IH}	High-level input voltage, all inputs except chip enable	2.4		V_{CC}+1	V
$V_{IL(CE)}$	Low-level chip enable input voltage	−1		1	V
V_{IL}	Low-level input voltage, all inputs except chip enable	−1		0.6	V

ELECTRICAL CHARACTERISTICS

(Ta＝0～70°C, V_{DD}＝12V±10%, V_{CC}＝5V±10%, V_{SS}＝0V, V_{BB}＝−5V±10%, unless otherwise noted)

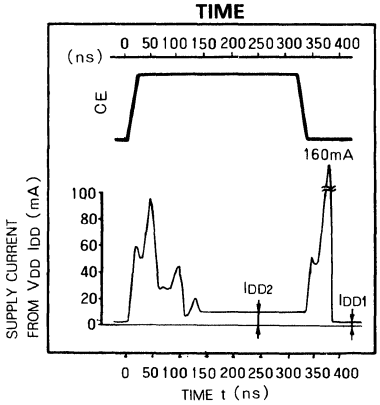
Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
$V_{IH(CE)}$	High-level chip enable input voltage			V_{DD}−1		V_{DD}+1	V
V_{IH}	High-level input voltage, all inputs except chip enable			2.4		V_{CC}+1	V
$V_{IL(CE)}$	Low-level chip enable input voltage			−1		1	V
V_{IL}	Low-level input voltage, all inputs except chip enable			−1		0.6	V
$I_{I(CE)}$	Input current, chip enable input		V_I＝V_{DD}+1V		0.01	2	μA
I_I	Input current, all inputs except chip enable		V_I＝6.5V		0.01	10	μA
V_{OH}	High-level output voltage		I_{OH}＝−2mA	2.4		V_{CC}	V
V_{OL}	Low-level output voltage		I_{OL}＝2mA	0		0.45	V
I_{OZ}	Off-state output current		V_{OZ}＝0～V_{CC}	−10		10	μA
I_{DD1}	Supply current from V_{DD}		$V_{IL(CE)}$＝−1V～0.6V		10	200	μA
I_{DD2}	Supply current from V_{DD}		$V_{IH(CE)}$＝V_{IH}, $V_{IL(\overline{CS})}$＝V_{IL}		10	25	mA
I_{CC}	Supply current from V_{CC}		$V_{IL(CE)}$＝V_{IL} or $V_{IH(\overline{CS})}$＝V_{IH}		0.01	10	μA
I_{BB}	Supply current from V_{BB}				0.01	100	μA
$I_{DD(AV)}$	Average supply current from V_{DD}	M58755S−1	$t_{w(CE)}$＝230ns, t_C＝400ns		25	40	mA
		M58755S−2	$t_{w(CE)}$＝300ns, t_C＝470ns		20	35	mA
		M58755S−3	$t_{w(CE)}$＝180ns, t_C＝310ns		29	45	mA
$C_{i(CE)}$	Input capacitance, chip enable input		V_{IL}＝V_{SS}, V_{BB}＝−5V, f＝1MHz		17	25	pF
C_i	Input capacitance, all inputs except chip enable		V_{IL}＝V_{SS}, V_{BB}＝−5V, f＝1MHz		5	7	pF
C_o	Output capacitance		V_{OL}＝V_{SS}, V_{BB}＝−5V, f＝1MHz		5	7	pF

Note 1 : Current flowing into an IC is positive; out is negative.

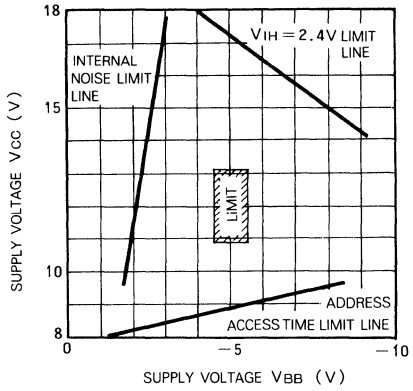
4096-BIT (4096-WORD BY 1-BIT) DYNAMIC RANDOM-ACCESS MEMORY

TYPICAL CHARACTERISTICS (M58755S-1)

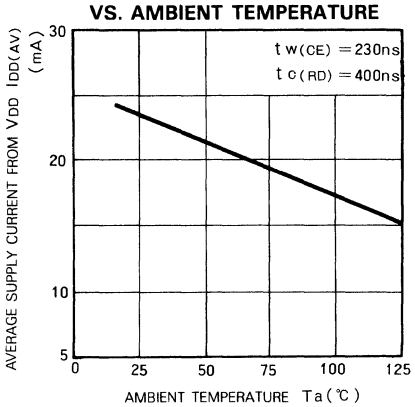
SUPPLY CURRENT FROM V_{DD} VS. TIME



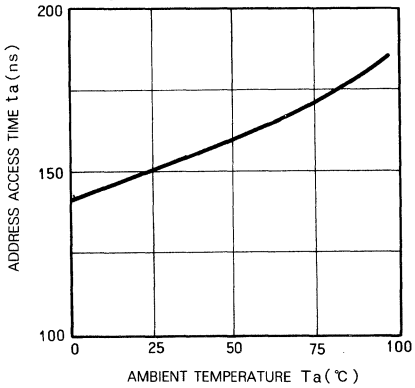
V_{DD} VS. V_{BB} OPERATING REGION



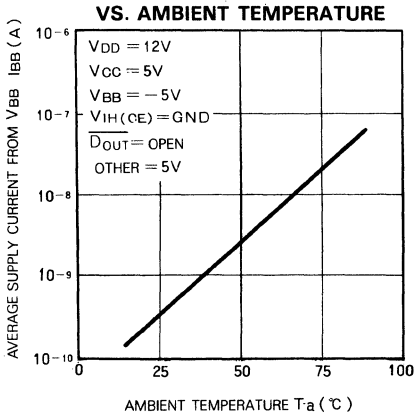
AVERAGE SUPPLY CURRENT FROM V_{DD} VS. AMBIENT TEMPERATURE



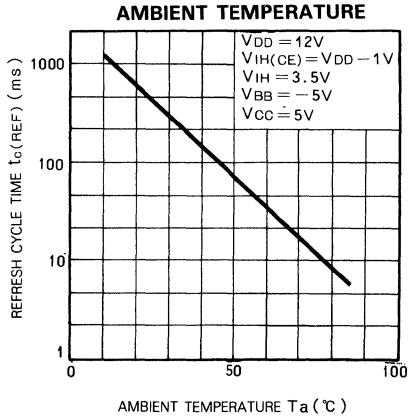
ADDRESS ACCESS TIME VS. AMBIENT TEMPERATURE



AVERAGE SUPPLY CURRENT FROM V_{BB} VS. AMBIENT TEMPERATURE



REFRESH CYCLE TIME VS. AMBIENT TEMPERATURE



5

4096-BIT (4096-WORD BY 1-BIT) DYNAMIC RANDOM-ACCESS MEMORY

TIMING REQUIREMENTS M58755S-1 ($Ta=0\sim70°C$, $V_{DD}=12V\pm10\%$, $V_{CC}=5V\pm10\%$, $V_{SS}=0V$, $V_{BB}=-5V\pm10\%$, unless otherwise noted)

Read, Write or Read-Modify-Write Cycle

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{c(REF)}$	Refresh cycle time				2	ms
$t_{w(CEL)}$	Chip enable low pulse width		130			ns
$t_{r(CE)}$	Chip enable pulse rise time				40	ns
$t_{f(CE)}$	Chip enable pulse fall time				40	ns
$t_{su(AD)}$	Address setup time		0			ns
$t_{su(\overline{CS})}$	Chip select setup time		0			ns
$t_{h(AD)}$	Address hold time		100			ns
$t_{h(\overline{CS})}$	Chip select hold time		100			ns

Read Cycle

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{c(RD)}$	Read cycle time	$t_r=t_f=20ns$	400			ns
$t_{w(CEH)}$	Chip enable high pulse width		230		4000	ns
$t_{su(RD)}$	Read setup time		−10			ns
$t_{h(RD)}$	Read hold time		0			ns

Write or Read-Modify-Write Cycle

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{c(WR)}$	Write cycle time	$t_r=t_f=20ns$	400			ns
$t_{c(RMW)}$	Read-modify-write cycle time		520			ns
$t_{w(CEH)}$	Chip enable high pulse width,write cycle		230		4000	ns
$t_{w(CEH)}$	Chip enable high pulse width, read-modify-write cycle		350		4000	ns
$t_{su(RD)}$	Read setup time		−10			ns
$t_{h(RD)}$	Read hold time		180			ns
$t_{su(WR)}$	Write setup time		150			ns
$t_{w(WR)}$	Write pulse width		50			ns
$t_{d(WR)}$	Write delay time		150			ns
$t_{su(DA)}$	Data setup time		0			ns
$t_{h(DA)}$	Data hold time		0			ns

SWITCHING CHARACTERISTICS ($Ta=0\sim70°C$, $V_{DD}=12V\pm10\%$, $V_{CC}=5V\pm10\%$, $V_{SS}=0V$, $V_{BB}=-5V\pm10\%$, unless otherwise noted)

Read Cycle

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{a(CE)}$	Chip enable access time	$C_L=50pF$, Load=1 TTL, $V_{REF}=2.0V$			180	ns
$t_{a(AD)}$	Address access time	$t_{su(AD)}=0ns$, $t_r=t_f=20ns$			200	ns
$t_{dv(CE)}$	Data valid time with respect to chip enable		0			ns

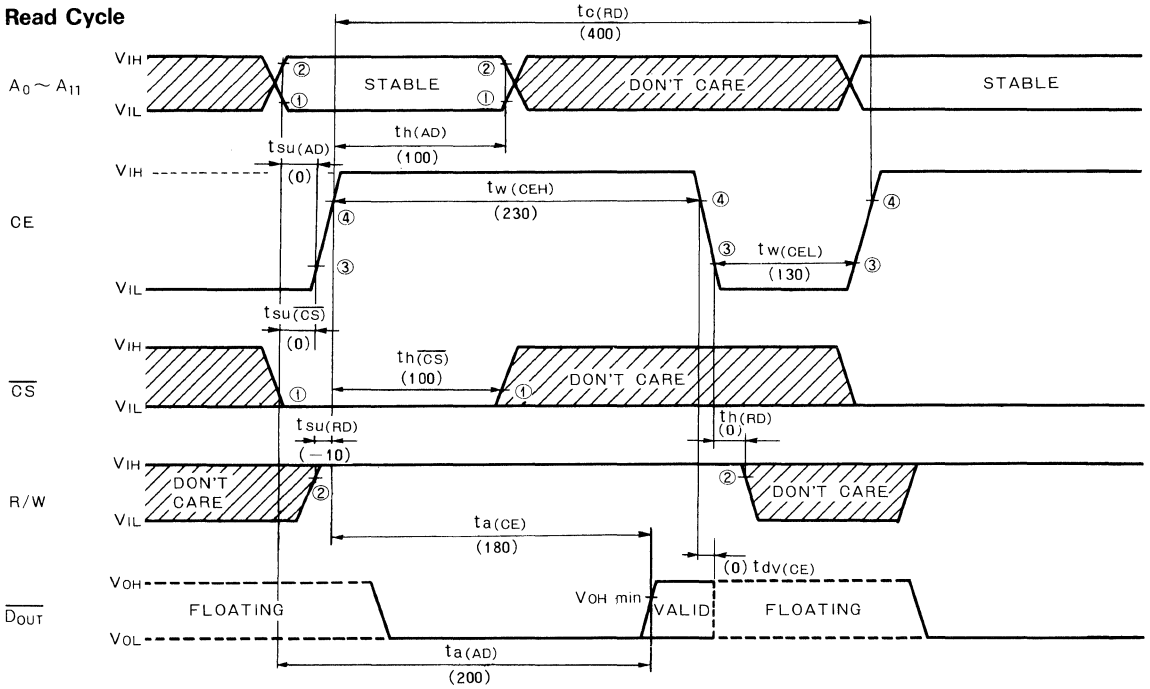
Read-Modify-Write Cycle

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{a(CE)}$	Chip enable access time	$C_L=50pF$, Load=1 TTL, $V_{REF}=2.0V$			180	ns
$t_{a(AD)}$	Address access time	$t_{su(AD)}=0ns$, $t_r=t_f=20ns$			200	ns
$t_{dv(CE)}$	Data valid time with respect to chip enable		0			ns

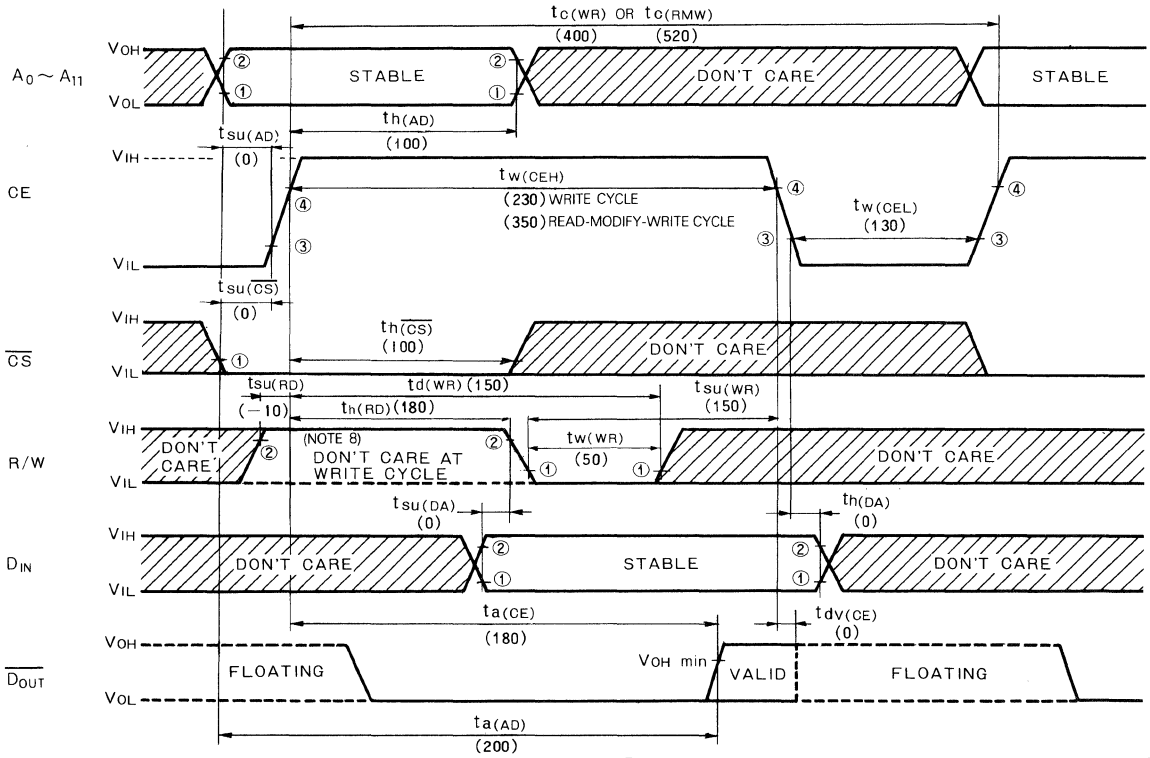
4096-BIT (4096-WORD BY 1-BIT) DYNAMIC RANDOM ACCESS MEMORY

TIMING DIAGRAMS

Read Cycle



Write or Read-Modify-Write Cycle



Note 4 : Hatching indicates the state is unknown or changing.

5 : V_{SS}+0.6V is the reference level for point ①, and V_{SS}+2.4V for point ②.

6 : V_{SS}+2.0V is the reference level for point ③, and V_{DD} −2.0V for point ④.

7 : The transition time (t_T) of the CE Pulse is defined as the transition time from ③ to ④ and from ④ to ③.

8 : The level of the dotted line should be kept high during read-modify-write cycle.

9 : Numbers in parentheses ( ) indicate the minimum timing value in ns.

4096-BIT (4096-WORD BY 1-BIT) DYNAMIC RANDOM-ACCESS MEMORY

TIMING REQUIREMENTS M58755S-2 ($Ta=0\sim70°C$, $V_{DD}=12V\pm10\%$, $V_{CC}=5V\pm10\%$, $V_{SS}=0V$, $V_{BB}=-5V\pm10\%$, unless otherwise noted)

Read, Write or Read-Modify-Write Cycle

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{c(REF)}$	Refresh cycle time				2	ms
$t_{w(CEL)}$	Chip enable low pulse width		130			ns
$t_{r(CE)}$	Chip enable pulse rise time				40	ns
$t_{f(CE)}$	Chip enable pulse fall time				40	ns
$t_{su(AD)}$	Address setup time		0			ns
$t_{su(\overline{CS})}$	Chip select setup time		0			ns
$t_{h(AD)}$	Address hold time		100			ns
$t_{h(\overline{CS})}$	Chip select hold time		100			ns

Read Cycle

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{c(RD)}$	Read cycle time	$t_r=t_f=20ns$	470			ns
$t_{w(CEH)}$	Chip enable high pulse width		300		4000	ns
$t_{su(RD)}$	Read setup time		−10			ns
$t_{h(RD)}$	Read hold time		0			ns

Write or Read-Modify-Write Cycle

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{c(WR)}$	Write cycle time	$t_r=t_f=20ns$	470			ns
$t_{c(RMW)}$	Read-modify-write cycle time		590			ns
$t_{w(CEH)}$	Chip enable high pulse width, write cycle		300		4000	ns
$t_{w(CEH)}$	Chip enable high pulse width, read-modify-write cycle		420		4000	ns
$t_{su(RD)}$	Read setup time		−10			ns
$t_{h(RD)}$	Read hold time		250			ns
$t_{su(WR)}$	Write setup time		150			ns
$t_{w(WR)}$	Write pulse width		50			ns
$t_{d(WR)}$	Write delay time		150			ns
$t_{su(DA)}$	Data setup time		0			ns
$t_{h(DA)}$	Data hold time		0			ns

SWITCHING CHARACTERISTICS ($Ta=0\sim70°C$, $V_{DD}=12V\pm10\%$, $V_{CC}=5V\pm10\%$, $V_{SS}=0V$, $V_{BB}=-5V\pm10\%$, unless otherwise noted)

Read Cycle

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{a(CE)}$	Chip enable access time	$C_L=50pF$, Load=1 TTL, $V_{REF}=2.0V$			250	ns
$t_{a(AD)}$	Address access time	$t_{su(AD)}=0ns$, $t_r=t_f=20ns$			270	ns
$t_{dv(CE)}$	Data valid time with respect to chip enable		0			ns

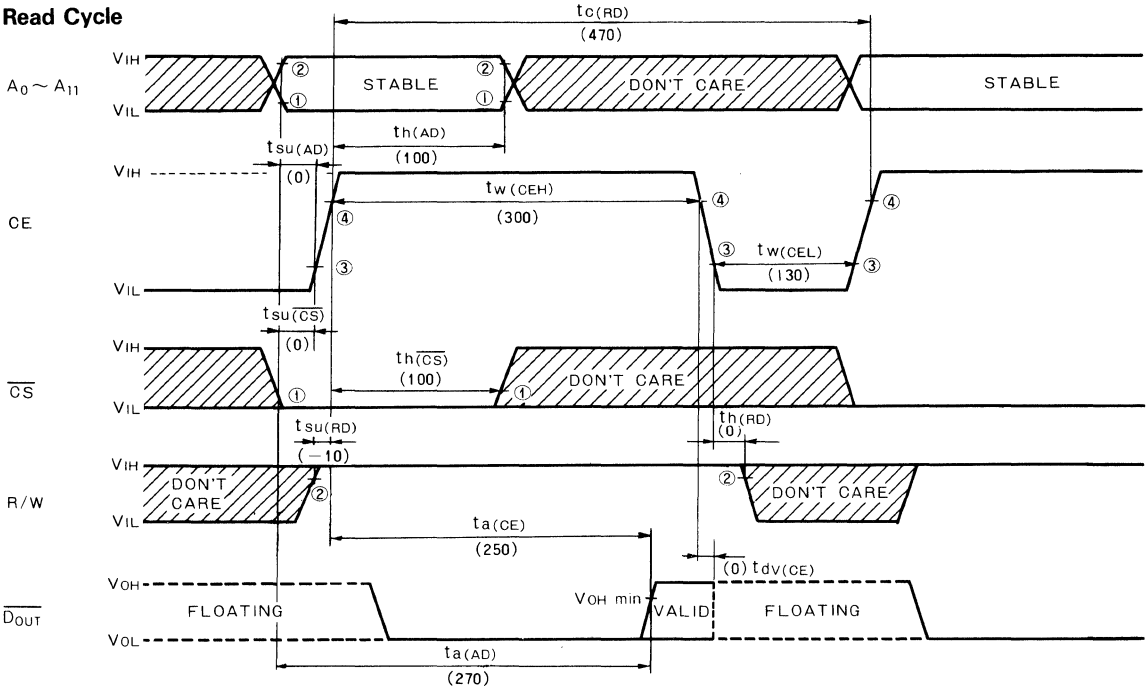
Read-Modify-Write Cycle

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{a(CE)}$	Chip enable access time	$C_L=50pF$, Load=1 TTL, $V_{REF}=2.0V$			250	ns
$t_{a(AD)}$	Address access time	$t_{su(AD)}=0ns$, $t_r=t_f=20ns$			270	ns
$t_{dv(CE)}$	Data valid time with respect to chip enable		0			ns

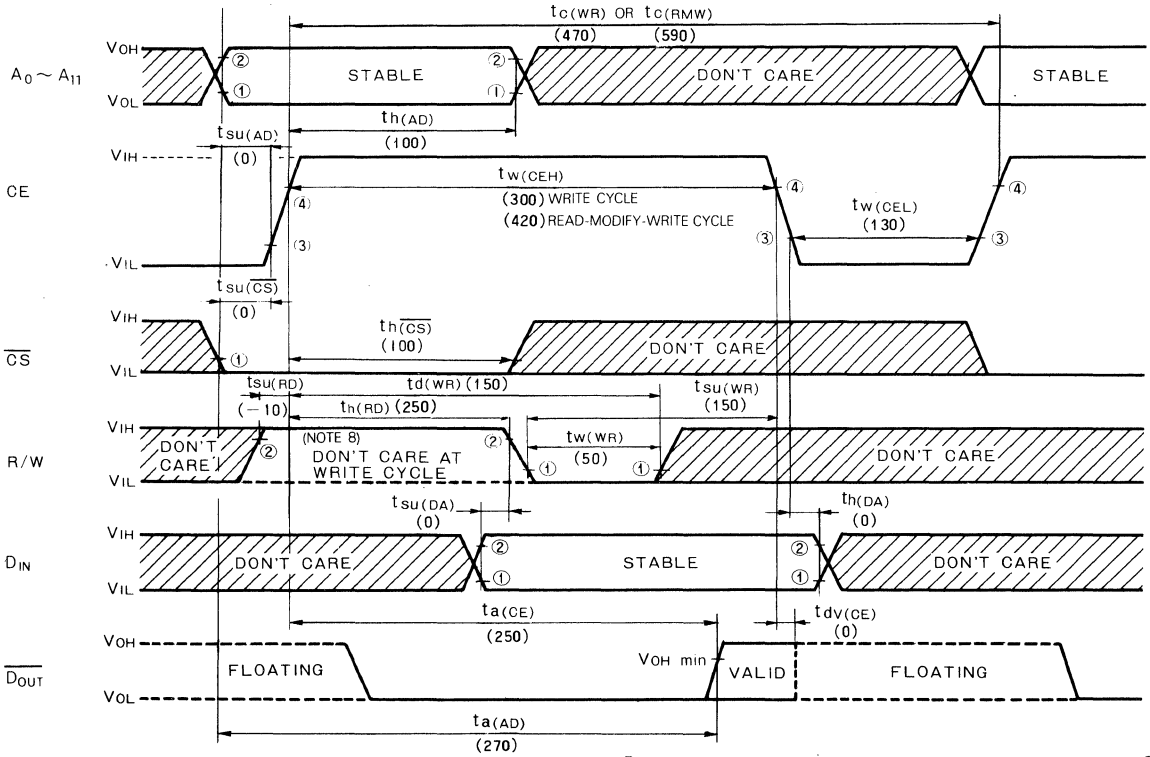
4096-BIT (4096-WORD BY 1-BIT) DYNAMIC RANDOM-ACCESS MEMORY

TIMING DIAGRAMS

Read Cycle



Write or Read-Modify-Write Cycle



Note 4 : Hatching indicates the state is unknown or changing.

5 : Vss+0.6V is the reference level for point ①, and Vss+2.4V for point ②.

6 : Vss+2.0V is the reference level for point ③, and V_{DD} −2.0V for point ④.

7 : The transition time (t_T) of the CE Pulse is defined as the transition time from ③ to ④ and from ④ to ③.

8 : The level of the dotted line should be kept high during read-modify-write cycle.

9 : Numbers in parentheses ( ) indicate the minimum timing value in ns.

4096-BIT (4096-WORD BY 1-BIT) DYNAMIC RANDOM-ACCESS MEMORY

TIMING REQUIREMENTS M58755S-3 ($Ta=0\sim70°C$, $V_{DD}=12V\pm10\%$, $V_{CC}=5V\pm10\%$, $V_{SS}=0V$, $V_{BB}=-5V\pm10\%$, unless otherwise noted)

Read, Write or Read-Modify-Write Cycle

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{c(REF)}$	Refresh cycle time				2	ms
$t_{w(CEL)}$	Chip enable low pulse width		130			ns
$t_{r(CE)}$	Chip enable pulse rise time				40	ns
$t_{f(CE)}$	Chip enable pulse fall time				40	ns
$t_{su(AD)}$	Address setup time		0			ns
$t_{su(\overline{CS})}$	Chip select setup time		0			ns
$t_{h(AD)}$	Address hold time		100			ns
$t_{h(\overline{CS})}$	Chip select hold time		100			ns

Read Cycle

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{c(RD)}$	Read cycle time	$t_r=t_f=20ns$	320			ns
$t_{w(CEH)}$	Chip enable high pulse width		180		4000	ns
$t_{su(RD)}$	Read setup time		−10			ns
$t_{h(RD)}$	Read hold time		0			ns

Write or Read-Modify-Write Cycle

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{c(WR)}$	Write cycle time	$t_r=t_f=20ns$	320			ns
$t_{c(RMW)}$	Read-modify-write cycle time		470			ns
$t_{w(CEH)}$	Chip enable high pulse width, write cycle		180		4000	ns
$t_{w(CEH)}$	Chip enable high pulse width, read-modify-write cycle		300		4000	ns
$t_{su(RD)}$	Read setup time		−10			ns
$t_{h(RD)}$	Read hold time		150			ns
$t_{su(WR)}$	Write setup time		150			ns
$t_{w(WR)}$	Write pulse width		50			ns
$t_{d(WR)}$	Write delay time		150			ns
$t_{su(DA)}$	Data setup time		0			ns
$t_{h(DA)}$	Data hold time		0			ns

SWITCHING CHARACTERISTICS ($Ta=0\sim70°C$, $V_{DD}=12V\pm10\%$, $V_{CC}=5V\pm10\%$, $V_{SS}=0V$, $V_{BB}=-5V\pm10\%$, unless otherwise noted)

Read Cycle

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{a(CE)}$	Chip enable access time	$C_L=50pF$, Load=1 TTL, $V_{REF}=2.0V$			130	ns
$t_{a(AD)}$	Address access time	$t_{su(AD)}=0ns$, $t_r=t_f=20ns$			150	ns
$t_{dv(CE)}$	Data valid time with respect to chip ennable		0			ns

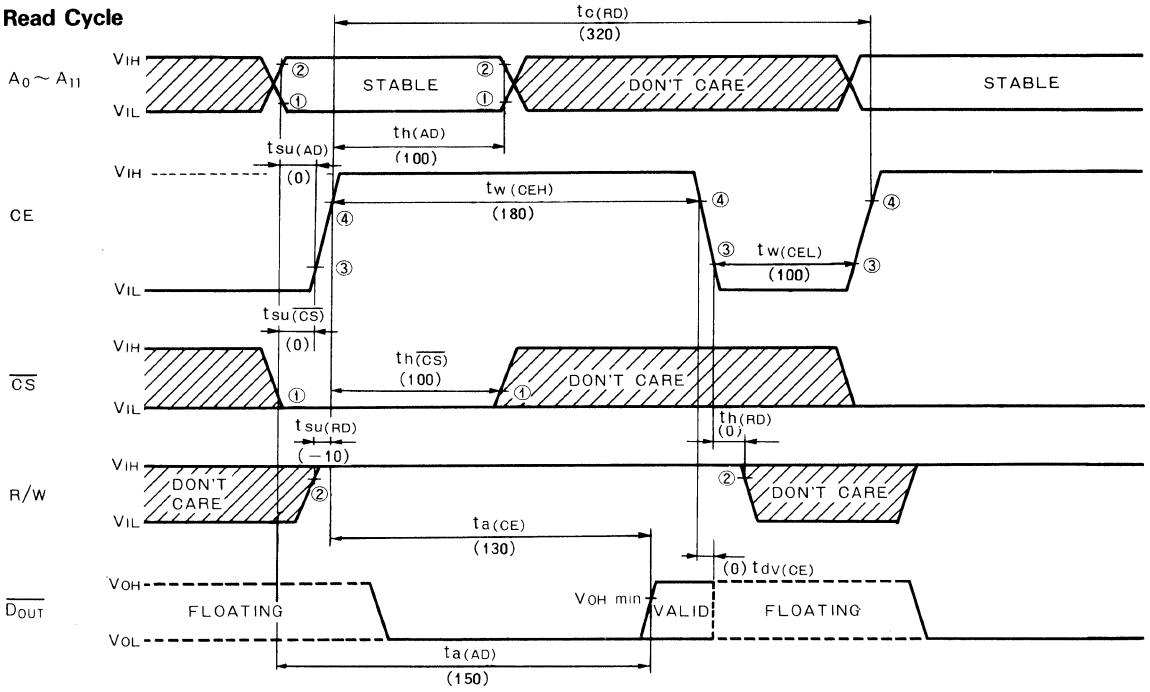
Read-Modify-Write Cycle

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{a(CE)}$	Chip enable access time	$C_L=50pF$, Load=1 TTL, $V_{REF}=2.0V$			130	ns
$t_{a(AD)}$	Address access time	$t_{su(AD)}=0ns$, $t_r=t_f=20ns$			150	ns
$t_{dv(CE)}$	Data valid time with respect to chip enable		0			ns

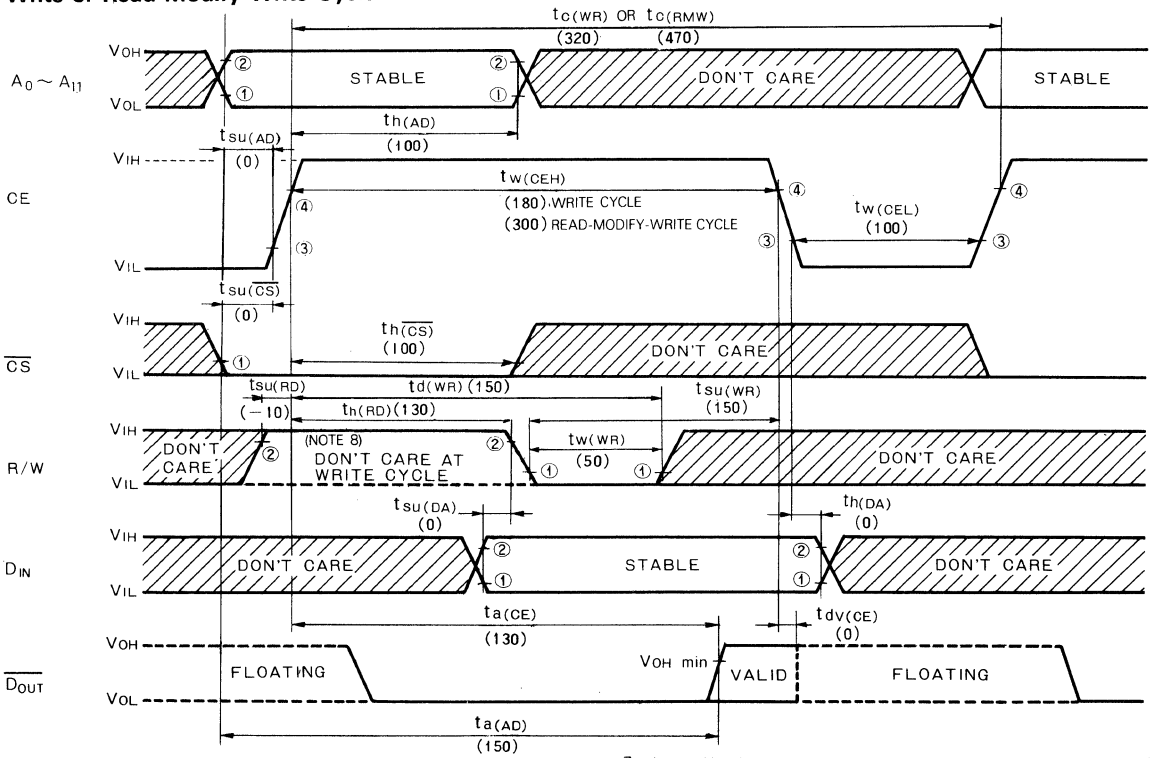
4096-BIT (4096-WORD BY 1-BIT) DYNAMIC RANDOM-ACCESS MEMORY

TIMING DIAGRAMS

Read Cycle



Write or Read-Modify-Write Cycle



Note 4 : Hatching indicates the state is unknown or changing.

5 : Vss+0.6V is the reference level for point ①, and Vss+2.4V for point ②.

6 : Vss+2.0V is the reference level for point ③, and V_{DD} −2.0V for point ④.

7 : The transition time (t_T) of the CE Pulse is defined as the transition time from ③ to ④ and from ④ to ③.

8 : The level of the dotted line should be kept high during read-modify-write cycle.

9 : Numbers in parentheses ( ) indicate the minimum timing value in ns.

M58755S-1, M58755S-2, M58755S-3

Alternative Designation 2107B

4096-BIT (4096-WORD BY 1-BIT) DYNAMIC RANDOM-ACCESS MEMORY

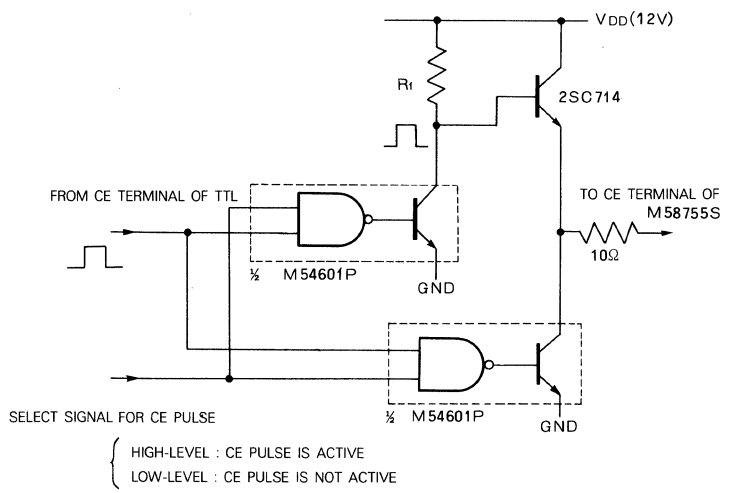
APPLICATION

Method of Refreshing

Since 64 memory cells designated by the X address can be refreshed in 1 cycle, (either read, write or read-modify-write), a read operation for all 64 addresses selected by the 6 address signals $A_0 \sim A_5$ must be performed within 2ms to refresh all 4096 memory cells. If the chip is refreshed during a write cycle or a read-modify-write cycle, then signal $\overline{CS}$ must be kept low; during a read cycle, $\overline{CS}$ can be either high or low. If a read operation is executed when the chip is in the non-designated state with $\overline{CS}$ high, refreshing can be performed with the output terminal $\overline{D_{OUT}}$ in the floating (high-impedance) state. Thus all the M58755Ss used in the memory system can be refreshed in only 64 cycles.

Recommended Driver Circuit for Chip Enable Pulse

COMPONENTS : M54601P · · · · · · · 1
2SC714 · · · · · · · · · 1
RESISTORS · · · · · 2



Note 1 : R_1 is determined according to a required rise time of the CE pulse. For example, when C_L capacitance load for the CE pulse is 300pF, R_1 is set at 300Ω ($\frac{1}{2}$W) ; then, rise time $t_r = 30$ns; fall time $t_f = 30$ns; $t_{PHL} = 20$ns; $t_{PLH} = 20$ns.

2 : One M54601P dual peripheral positive AND driver circuit should be used for each CE driver circuit.

M58721P, M58721S

Alternative Designation 2101A

1024-BIT (256-WORD BY 4-BIT) STATIC RANDOM-ACCESS MEMORY

DESCRIPTION

The M58721P and M58721S are 256-word by 4-bit static RAMs, fabricated with the N-channel silicon-gate MOS process and designed for simple interfacing. They operate by a single 5V supply, as does TTL, and are directly TTL-compatible.

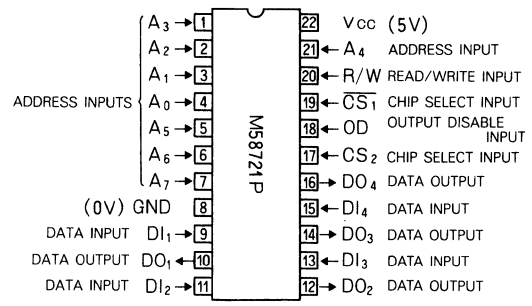
FEATURES

- Fast access time: 450ns (max)
- Low power dissipation: 150μW/bit (typ)
- Single 5V supply voltage
- Data holding at 1.5V supply voltage (optional)
- No clocks or refreshing required
- All inputs and outputs are directly TTL-compatible
- All outputs are three-state, with OR-tie capability
- Simple memory expansion by chip select input
- Separate data inputs and outputs
- Interchangeable with Intel's 2101A-4 in pin configuration and electrical characteristics.

APPLICATION

- Small-capacity memory units

PIN CONFIGURATION (TOP VIEW)



Outline 22P1 (M58721P)
22S1 (M58721S)

FUNCTION

The M58721P and M58721S have 256-word by 4-bit organization and provide separate data input and output terminals. During a write cycle, when a location is designated by address signals $A_0 \sim A_7$ and signal R/W goes low, the data of the IN signal at that time is written.

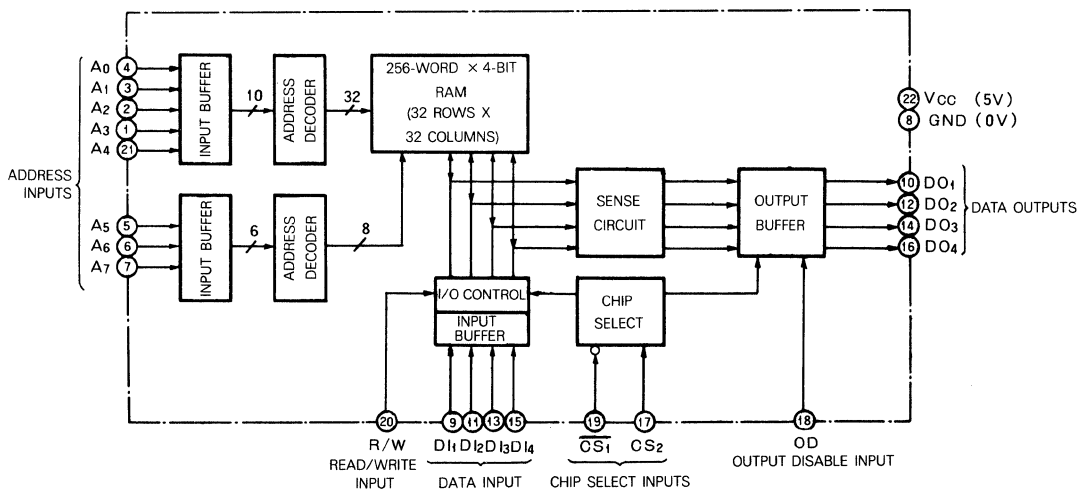
During a read cycle, when a location is designated by address signals $A_0 \sim A_7$ and R/W goes high, data of the designated address is taken from the DO terminal.

When signal $\overline{CS_1}$ is high or CS_2 is low, the chip is in the non-selectable state, disabling both reading and writing. In this case the output is in the floating (high-impedance) state useful for OR-ties with other output terminals.

When signal OD is high, the output is in the floating state, so that OD is used as an input/output select control signal for common input/output operation.

The memory data can be held at a supply voltage of 1.5V, enabling battery back-up operation during power failure and power-down operation in the standby mode.

BLOCK DIAGRAM



M58721P, M58721S

Alternative Designation 2101A

1024-BIT (256-WORD BY 4-BIT) STATIC RANDOM-ACCESS MEMORY

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Conditions	Limits	Unit
V_{CC}	Supply voltage		With respect to GND	−0.3～7	V
V_I	Input voltage			−0.3～7	V
V_O	Output voltage			−0.3～7	V
Pd	Maximum power dissipation	M58721P	Ta=25°C	700	mW
		M58721S		1000	mW
Topr	Operating free-air ambient temperature			0～70	°C
Tstg	Storage temperature	M58721P		−40～125	°C
		M58721S		−65～150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0～10°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IL}	Low-level input voltage	0		0.8	V
V_{IH}	High-level input voltage	2.2		V_{CC}	V

ELECTRICAL CHARACTERISTICS (Ta=0～70°C, V_{CC}=5V±5%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2.2		V_{CC}	V
V_{IL}	Low-level input voltage		0		0.8	V
V_{OH}	High-level output voltage	I_{OH}=−200μA	2.4			V
V_{OL}	Low-level output voltage	I_{OL}=3.5mA			0.45	V
I_I	Input current	V_I=0～5.25V			10	μA
I_{OZH}	Off-state high-level output current	$V_{I(\overline{CS_1})}$=2.2V, V_O=2.4V～V_{CC}			10	μA
I_{OZL}	Off-state low-level output current	$V_{I(\overline{CS_1})}$=2.2V, V_O=0.4V			−10	μA
I_{CC}	Supply current from V_{CC}	V_I=5.25V (all inputs), output open		30	60	mA
C_i	Input capacitance, all inputs	V_I=GND, f=1MHz, 25mVrms		3	5	pF
C_o	Output capacitance	V_O=GND, f=1MHz, 25mVrms		8	12	pF

Note 1 : Current flowing into an IC is positive; out is negative.

TIMING REQUIREMENTS (For Write Cycle) (Ta=0～70°C, V_{CC}=5V±5%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{c(WR)}$	Write cycle time	Input pulse V_{IH}=2.2V	350			ns
$t_{w(WR)}$	Write pulse width	V_{IL}=0.8V	250			ns
$t_{su(AD)}$	Address setup time with respect to write	t_r=t_f=20ns	20			ns
t_{wr}	Write recovery time		0			ns
$t_{su(OD)}$	Output disable setup time with respect to data in	Reference level=1.5V	100			ns
$t_{su(DA)}$	Data setup time	Load=2TTL, C_L=100pF	170			ns
$t_{h(DA)}$	Data hold time		0			ns
$t_{su(CS)}$	Chip select setup time		250			ns

SWITCHING CHARACTERISTICS (For Read Cycle) (Ta=0～70°C, V_{CC}=5V±5%, unless otherwise noted)

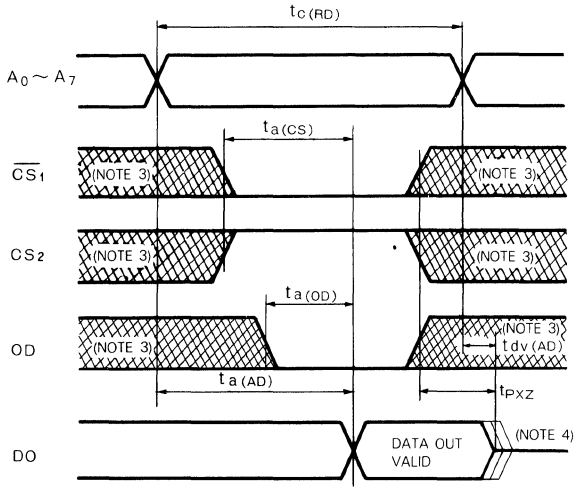
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{c(RD)}$	Read cycle time	Input pulse V_{IH}=2.2V	450			ns
$t_{a(AD)}$	Address access time	V_{IL}=0.8V			450	ns
$t_{a(CS)}$	Chip select access time	t_r=t_f=20ns			180	ns
$t_{a(OD)}$	Output disable access time				150	ns
t_{PXZ}	Output disable time (Note 2)	Reference level=1.5V			100	ns
$t_{dv(AD)}$	Data valid time with respect to address	LOAD=2TTL, C_L=100pF	40			ns

Note 2 : t_{PXZ} is with respect to $\overline{CS_1}$, CS_2, or OD, whichever occurs first.

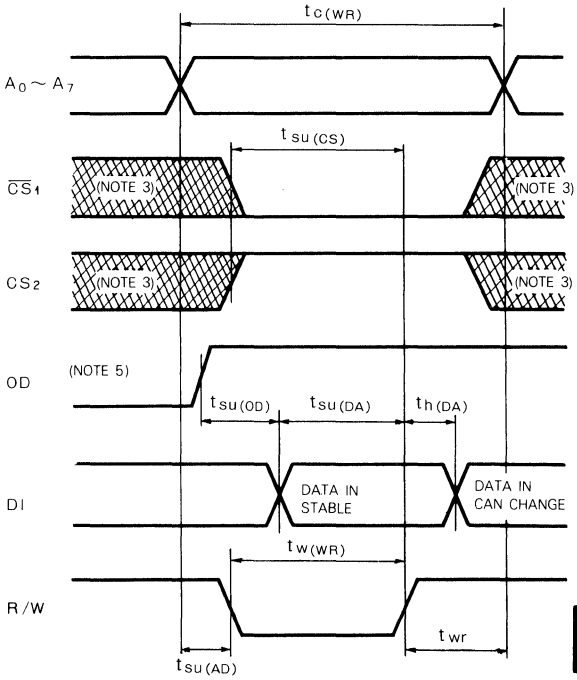
1024-BIT (256-WORD BY 4-BIT) STATIC RANDOM-ACCESS MEMORY

TIMING DIAGRAMS

Read Cycle



Write Cycle



Note 3 : Hatching indicates the state is unknown.

4 : Indicates that during this period the data out is invalid for this definition of $t_{dv(AD)}$ and is in the floating state for this definition of t_{PXZ}.

5 : OD may be kept low for the full cycle except during common input/output operation.

POWER-DOWN OPERATION (OPTIONAL) These characteristics are guaranted only under custom specifications.

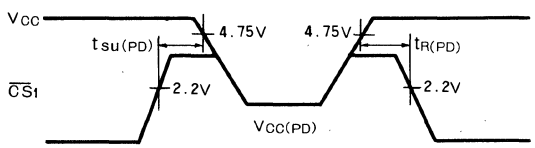
Electrical Characteristics (T_a=0~70°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$V_{CC(PD)}$	Power-down supply voltage		1.5			V
$V_{I(\overline{CS1})}$	Power-down chip select input voltage	2.2V≦$V_{CC(PD)}$≦V_{CC}	2.2			V
		1.5V≦$V_{CC(PD)}$≦2.2V	$V_{CC(PD)}$			V
$I_{CC(PD1)}$	Power-down supply current from V_{CC}	V_{CC}=1.5V, all inputs=1.5V		15	30	mA
$I_{CC(PD2)}$	Power-down supply current from V_{CC}	V_{CC}=2.0V, all inputs=2.0V		20	40	mA

Timing Requirements (T_a=0~70°C, V_{CC}=5V±5%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(PD)}$	Power-down setup time		0			ns
$t_{R(PD)}$	Power-down recovery time		$t_{c(RD)}$			ns

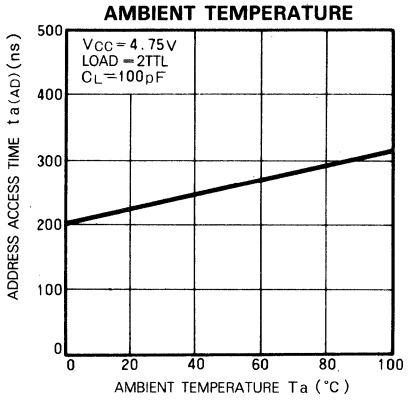
Timing Diagram



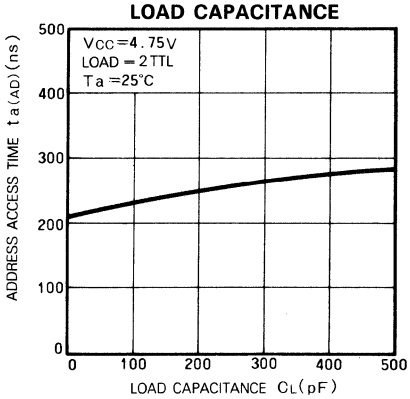
1024-BIT (256-WORD BY 4-BIT) STATIC RANDOM-ACCESS MEMORY

TYPICAL CHARACTERISTICS

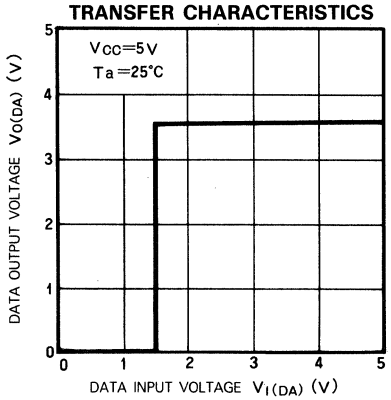
ADDRESS ACCESS TIME VS. AMBIENT TEMPERATURE



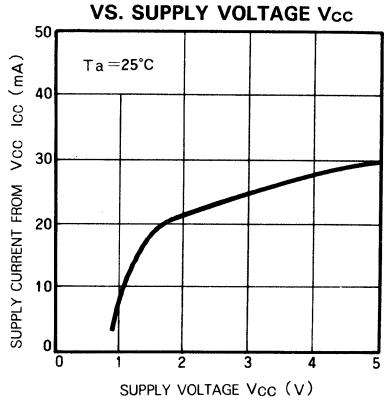
ADDRESS ACCESS TIME VS. LOAD CAPACITANCE



DATA INPUT/OUTPUT TRANSFER CHARACTERISTICS



SUPPLY CURRENT FROM V_{CC} VS. SUPPLY VOLTAGE V_{CC}



M58722P, M58722S

Alternative Designation 2111A

1024-BIT (256-WORD BY 4-BIT) STATIC RANDOM-ACCESS MEMORY

DESCRIPTION

The M58722P and M58722S are 256-word by 4-bit static RAMs, fabricated with the N-channel silicon-gate MOS process and designed for simple interfacing. They operate on a single 5V supply, as does TTL, and are directly TTL-compatible.

The input and output terminals are common, and an OD terminal is provided.

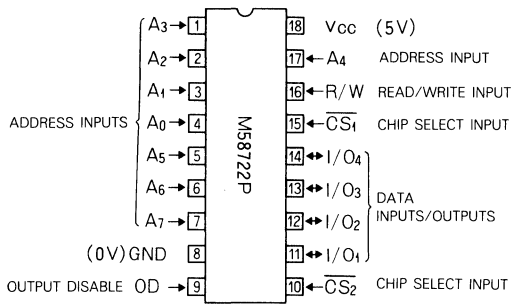
FEATURES

- Fast access time: 450ns (max)
- Low power dissipation: 150μW/bit (typ)
- Single 5V power supply
- Data holding at 1.5V supply voltage (optional)
- No clocks or refreshing required
- All inputs and outputs are directly TTL-compatible
- All outputs are three-state, with OR-tie capability
- Simple memory expansion by chip select input
- Common data inputs and outputs
- Interchangeable with Intel's 2111A-4 in pin configuration and electrical characteristics

APPLICATION

- Small-capacity memory units

PIN CONFIGURATION (TOP VIEW)



Outline 18P1 (M58722P)
18S1 (M58722S)

FUNCTION

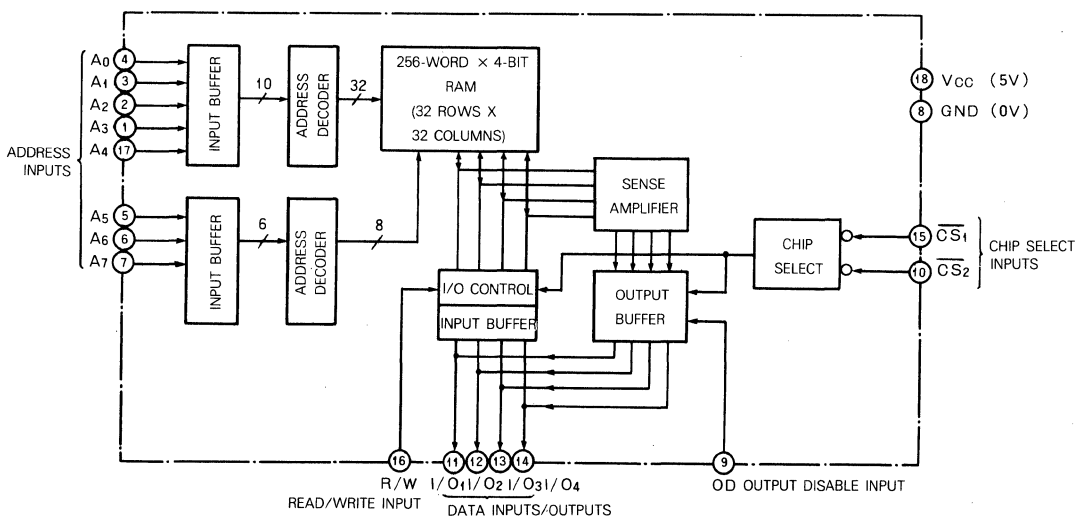
The M58722P and M58722S have 256-word by 4-bit organization and provide common data input and output terminals. During a write cycle, when a location is designated by address signals $A_0 \sim A_7$, the OD signal is kept high to keep the I/O terminals in the input mode, signal R/W goes low, and the data of the IN signal at that time is written.

During a read cycle, when a location is designated by address signals $A_0 \sim A_7$, the OD signal is kept low to keep the I/O terminals in the output mode, signal R/W goes high, and the data of the designated address is taken from the I/O terminals.

When signal $\overline{CS}_1$ or $\overline{CS}_2$ is high, the chip is in the non-selectable state, disabling both reading and writing. In this case the output is in the floating (high-impedance) state, useful for OR-ties with other output terminals.

The memory data can be held at a supply voltage of 1.5V, enabling battery back-up operation during power failure and power-down operation in the standby mode.

BLOCK DIAGRAM



M58722P, M58722S

Alternative Designation 2111A

1024-BIT (256-WORD BY 4-BIT) STATIC RANDOM-ACCESS MEMORY

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Conditions	Limits	Unit
V_{CC}	Supply voltage		With respect to GND	−0.3～7	V
V_I	Input voltage			−0.3～7	V
V_O	Output voltage			−0.3～7	V
Pd	Maximum power dissipation	M58722P	Ta＝25°C	700	mW
		M58722S		1000	mW
Topr	Operating free-air ambient temperature			0～70	°C
Tstg	Storage temperature	M58722P		−40～125	°C
		M58722S		−65～150	°C

RECOMMENDED OPERATING CONDITIONS (Ta＝0～10°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IL}	Low-level input voltage	0		0.8	V
V_{IH}	High-level input voltage	2.2		V_{CC}	V

ELECTRICAL CHARACTERISTICS (Ta＝0～70°C, V_{CC}＝5V±5%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2.2		V_{CC}	V
V_{IL}	Low-level input voltage		0		0.8	V
V_{OH}	High-level output voltage	I_{OH}=−200μA	2.4			V
V_{OL}	Low-level output voltage	I_{OL}=3.5mA			0.45	V
I_I	Input current	V_I= 0 ～5.25V			10	μA
I_{OZH}	Off-state high-level output current	$V_{I(\overline{CS_1})}$=2.2V, V_O=2.4V～V_{CC}			10	μA
I_{OZL}	Off-state low-level output current	$V_{I(\overline{CS_1})}$=2.2V, V_O=0.4V			−10	μA
I_{CC}	Supply current from V_{CC}	V_I=5.25V (all inputs), output open		30	60	mA
C_i	Input capacitance, all inputs	V_I=GND, f=1MHz, 25mVrms		3	5	pF
C_o	Output capacitance	V_O=GND, f=1MHz, 25mVrms		8	12	pF

Note 1 : Current flowing into an IC is positive; out is negative.

TIMING REQUIREMENTS (For Write Cycle) (Ta＝0～70°C, V_{CC}＝5V±5%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{c(WR)}$	Write cycle time	Input pulse V_{IH}=2.2V	350			ns
$t_{w(WR)}$	Write pulse width	V_{IL}=0.8V	250			ns
$t_{su(AD)}$	Address setup time with respect to write	t_r=t_f=20ns	20			ns
t_{wr}	Write recovery time		0			ns
$t_{su(OD)}$	Output disable setup time with respect to data in	Reference level＝1.5V	100			ns
$t_{su(DA)}$	Data setup time	Load＝2TTL, C_L=100pF	170			ns
$t_{h(DA)}$	Data hold time		0			ns
$t_{su(CS)}$	Chip select setup time		250			ns

SWITCHING CHARACTERISTICS (For Read Cycle) (Ta＝0～70°C, V_{CC}＝5V±5%, unless otherwise noted)

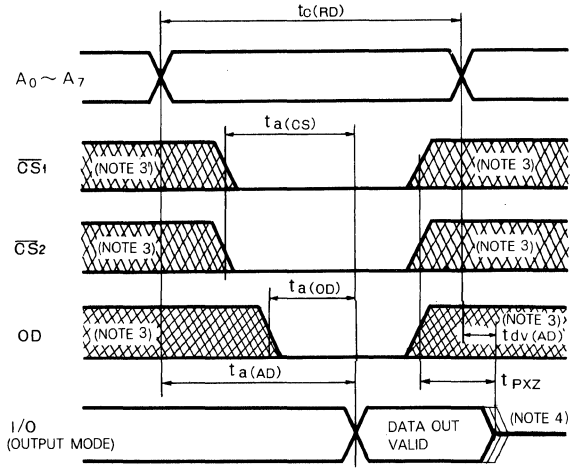
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{c(RD)}$	Read cycle time	Input pulse V_{IH}=2.2V	450			ns
$t_{a(AD)}$	Address access time	V_{IL}=0.8V			450	ns
$t_{a(\overline{CS})}$	Chip select access time	t_r=t_f=20ns			180	ns
$t_{a(OD)}$	Output disable access time				150	ns
t_{PXZ}	Output disable time (Note 2)	Reference level＝1.5V			100	ns
$t_{dv(AD)}$	Data valid time with respect to address	LOAD＝2TTL, C_L=100pF	40			ns

Note 2 : t_{PXZ} is with respect to $\overline{CS_1}$, $\overline{CS_2}$, or OD, whichever occurs first.

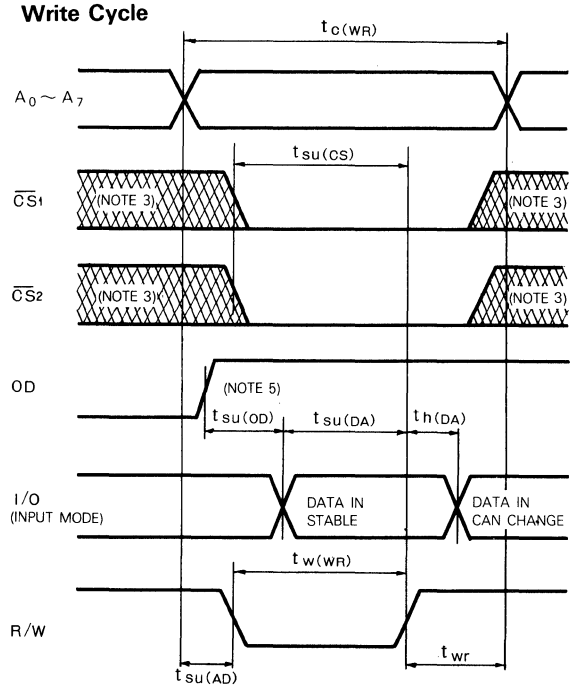
1024-BIT (256-WORD BY 4-BIT) STATIC RANDOM-ACCESS MEMORY

TIMING DIAGRAM

Read Cycle



Write Cycle



Note 3 : Hatching indicates the state is unknown.

4 : Indicates that during this period the data out is invalid for this definition of $t_{dv(AD)}$ and is in the floating state for this definition of t_{PXZ}.

5 : The input signals from the external circuits should not be applied to the I/O terminals, for during this period they are in output mode.

POWER-DOWN OPERATION (OPTIONAL) **These characteristics are guaranted only under custom specifications.**

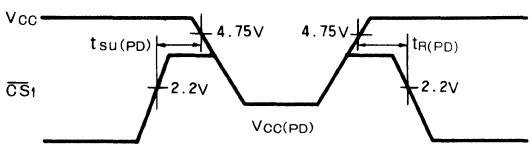
Electrical Characteristics (T_a = 0 ~ 70°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$V_{CC(PD)}$	Power-down supply voltage		1.5			V
V_I ($\overline{CS1}$)	Power-down chip select input voltage	2.2V ≦ $V_{CC(PD)}$ ≦ V_{CC}	2.2			V
		1.5V ≦ $V_{CC(PD)}$ ≦ 2.2V	$V_{CC(PD)}$			V
$I_{CC(PD1)}$	Power-down supply current from V_{CC}	V_{CC} = 1.5V, all inputs = 1.5V		15	30	mA
$I_{CC(PD2)}$	Power-down supply current from V_{CC}	V_{CC} = 2.0V, all inputs = 2.0V		20	40	mA

Timing Requirements (T_a = 0 ~ 70°C, V_{CC} = 5V ±5%, unless otherwise noted)

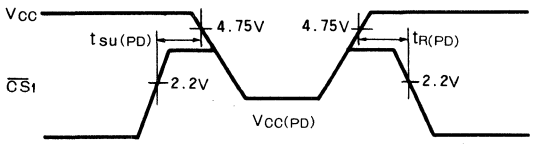
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(PD)}$	Power-down setup time		0			ns
$t_{R(PD)}$	Power-down recovery time		$t_{c(RD)}$			ns

Timing Diagram



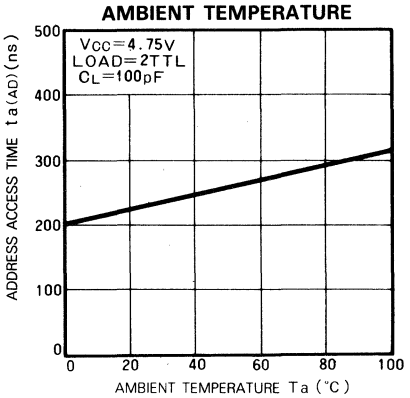
1024-BIT (256-WORD BY 4-BIT) STATIC RANDOM-ACCESS MEMORY

Timing Diagram

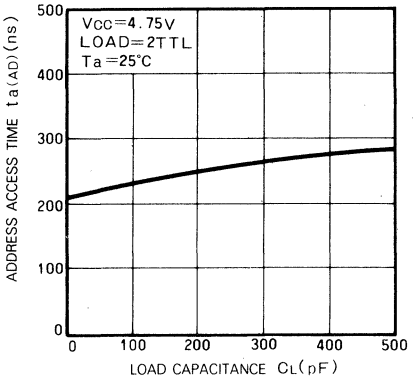


TYPICAL CHARACTERISTICS

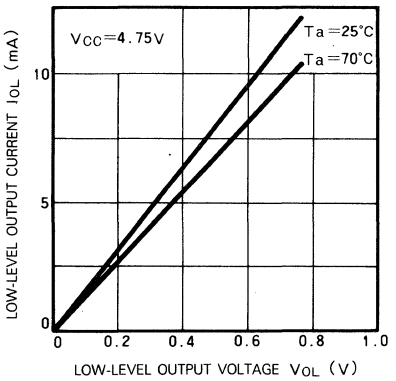
ADDRESS ACCESS TIME VS. AMBIENT TEMPERATURE



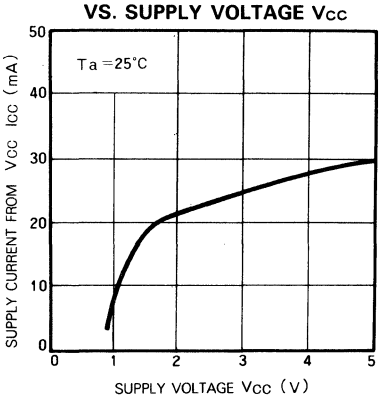
ADDRESS ACCESS TIME VS. LOAD CAPACITANCE



LOW-LEVEL OUTPUT CURRENT VS. LOW-LEVEL OUTPUT VOLTAGE



SUPPLY CURRENT FROM Vcc VS. SUPPLY VOLTAGE Vcc



M58723P, M58723S

Alternative Designation 2112A

1024-BIT (256-WORD BY 4-BIT) STATIC RANDOM-ACCESS MEMORY

DESCRIPTION

The M58723P and M58723S are 256-word by 4-bit static RAMs fabricated with the N-channel silicon-gate MOS process and designed for simple interfacing. They operate from a single 5V supply, as does TTL, and are directly TTL-compatible.

The input and output terminals are common.

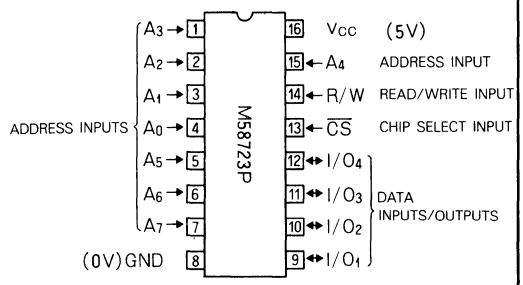
FEATURES

- Fast access time: 450ns (max)
- Low power dissipation: 150μW/bit (typ)
- Single 5V supply voltage
- Data holding at 1.5V supply voltage (optional)
- Requires no clocks or refreshing
- All inputs and outputs are directly TTL-compatible
- All outputs are three-state, with OR-tie capability
- Simple memory expansion by chip select input
- Common data inputs and outputs
- Interchangeable with Intel's 2112A-4 in pin configuration and electrical characteristics.

APPLICATION

- Small-capacity memory units

PIN CONFIGURATION (TOP VIEW)



Output 16P1 (M58723P)
16S1 (M58723S)

FUNCTION

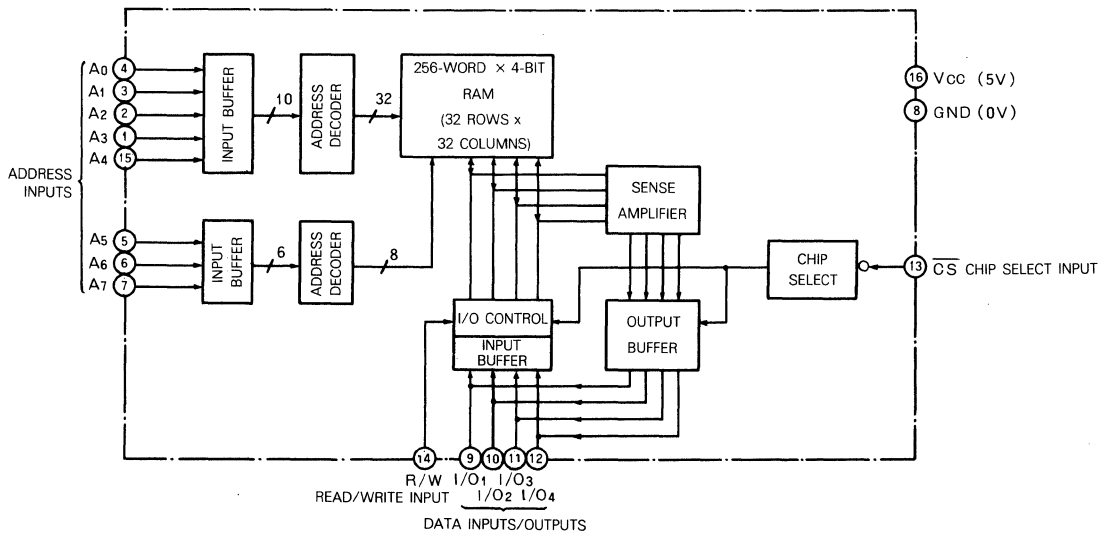
The M58723P and M58723S have 256-word by 4-bit organization and provide common data input and output terminals. During a write cycle, when a location is designated by address signals A_0~A_7 and signal R/W goes low, the data of the I/O signal at that time is written.

During a read cycle, when a location is designated by address signal A_0~A_7 and R/W goes high, data of the designated address is taken from the I/O terminals.

When signal $\overline{CS}$ is high, the chip is in the non-selectable state, disabling both reading and writing. In this case the output is in the floating (high-impedance) state, useful for OR-ties with other output terminals.

The memory data can be held at a supply voltage of 1.5V, enabling battery back-up operation during power failure and power-down operation in the standby mode.

BLOCK DIAGRAM



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M58723P, M58723S

Alternative Designation 2112A

1024-BIT (256-WORD BY 4-BIT) STATIC RANDOM-ACCESS MEMORY

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Conditions	Limits	Unit
V_{CC}	Supply voltage		With respect to GND	−0.3～7	V
V_I	Input voltage			−0.3～7	V
V_O	Output voltage			−0.3～7	V
Pd	Maximum power dissipation	M58723P	Ta＝25°C	700	mW
		M58723S		1000	mW
Topr	Operating free-air ambient temperature			0～70	°C
Tstg	Storage temperature	M58723P		−40～125	°C
		M58723S		−65～150	°C

RECOMMENDED OPERATING CONDITIONS (Ta＝0～70°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IL}	Low-level input voltage	0		0.8	V
V_{IH}	High-level input voltage	2.2		V_{CC}	V

ELECTRICAL CHARACTERISTICS (Ta＝0～70°C, V_{CC}＝5V±5%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2.2		V_{CC}	V
V_{IL}	Low-level input voltage		0		0.8	V
V_{OH}	High-level output voltage	I_{OH}＝−200μA	2.4			V
V_{OL}	Low-level output voltage	I_{OL}＝3.5mA			0.45	V
I_I	Input current	V_I＝0～5.25V			10	μA
I_{OZH}	Off-state high-level output current	$V_{I(\overline{CS})}$＝2.2V, V_O＝2.4V～V_{CC}			10	μA
I_{OZL}	Off-state low-level output current	$V_{I(\overline{CS})}$＝2.2V, V_O＝0.4V			−10	μA
I_{CC}	Supply current from V_{CC}	V_I＝5.25V (all inputs), output open		30	60	mA
C_i	Input capacitance, all inputs	V_I＝GND, f＝1MHz, 25mVrms		3	5	pF
C_o	Output capacitance	V_O＝GND, f＝1MHz, 25mVrms		8	12	pF

Note : Current flowing into an IC is positive; out is negative.

TIMING REQUIREMENTS (Ta＝0～70°C, Vcc＝5V±5%, unless otherwise noted)

Write Cycle 1

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{c(WR)1}$	Write cycle time	Input pulse	350			ns
$t_{su(AD)1}$	Address setup time with respect to write pulse	V_{IH}＝2.2V	20			ns
$t_{w(WR)1}$	Write pulse width	V_{IL}＝0.8V	250			ns
t_{wr1}	Write recovery time	t_r＝t_f＝20ns	0			ns
$t_{su(DA)1}$	Data setup time	Reference level＝1.5V	170			ns
$t_{h(DA)1}$	Data hold time	Load＝2TTL, C_L＝100pF	0			ns
$t_{h(\overline{CS})1}$	Chip select hold time		0			ns
$t_{su(WR)1}$	Write pulse setup time with respect to chip select		0			ns
$t_{su(\overline{CS})1}$	Chip select setup time		170			ns

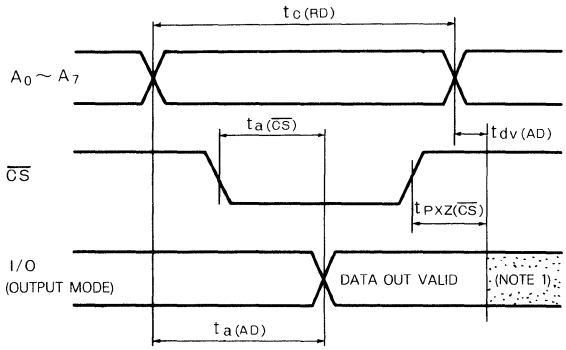
Write Cycle 2

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{c(WR)2}$	Write cycle time	Input pulse	350			ns
$t_{su(AD)2}$	Address setup time with respect to write pulse	$V_{IH}=2.2V$	20			ns
$t_{w(WR)2}$	Write pulse width	$V_{IL}=0.8V$	250			ns
t_{wr2}	Write recovery time	$t_r=t_f=20ns$	0			ns
$t_{su(DA)2}$	Data setup time	Reference level=1.5V	170			ns
$t_{h(DA)2}$	Data hold time	Load = 2TTL, $C_L=100pF$	0			ns
$t_{h(\overline{CS})2}$	Chip select hold time		0			ns
$t_{su(\overline{CS})2}$	Chip select setup time		0			ns
$t_{PXZ(WR)2}$	Output disable time with respect to write pulse				80	ns

SWITCHING CHARACTERISTICS (For Read Cycle) ($Ta=0\sim70°C$, $V_{CC}=5V\pm5\%$, unless otherwise noted)

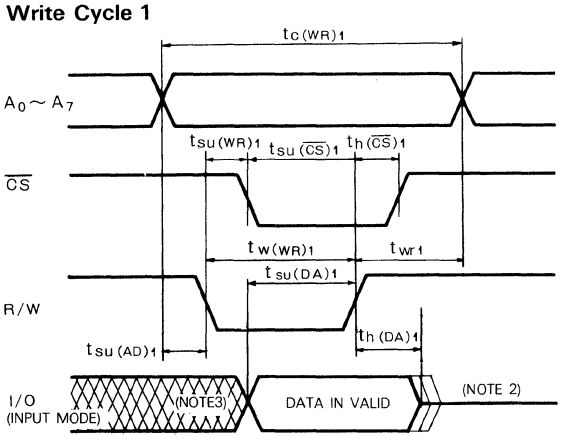
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{c(RD)}$	Read cycle time	Input pulse	450			ns
$t_{a(AD)}$	Address access time	$V_{IH}=2.2V$, $V_{IL}=0.8V$			450	ns
$t_{a(\overline{CS})}$	Chip select access time	$t_r=t_f=20ns$			180	ns
$t_{PXZ(\overline{CS})}$	Output disable time with respect to chip select	Reference level 1.5V			100	ns
$t_{dv(AD)}$	Data valid time with respect to address	Load = 2TTL, $C_L=100pF$	40			ns

TIMING DIAGRAMS
Read Cycle

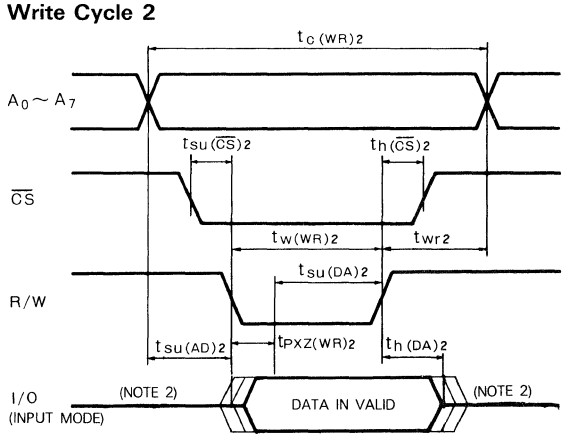


Note 1 : In this period, the data out is valid for a definition of $t_{dv(AD)}$ and is in the floating state for a definition of $t_{PXZ(\overline{CS})}$

Write Cycle 1



Write Cycle 2



Note 2 : The input signals from the external circuits should not be applied to the I/O terminals (keeping them three-state) for during this period the I/O terminals are in the output mode.

3.: The input signals from the external circuits can be applied to the I/O terminals since the signal $\overline{CS}$ is delayed in relation to signal R/W.

1024-BIT (256-WORD BY 4-BIT) STATIC RANDOM-ACCESS MEMORY

POWER-DOWN OPERATION (OPTIONAL) These characteristics are guaranted only under custom specifications.

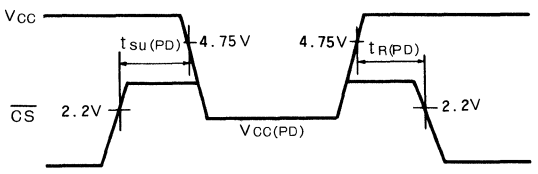
Electrical Characteristics (T_a = 0 ~ 70°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$V_{CC(PD)}$	Power-down supply voltage		1.5			V
$V_I(\overline{CS})$	Power-down chip select input voltage	2.2V ≦ $V_{CC(PD)}$ ≦ V_{CC}	2.2			V
		1.5V ≦ $V_{CC(PD)}$ ≦ 2.2V	$V_{CC(PD)}$			V
$I_{CC(PD1)}$	Power-down supply current from V_{CC}	V_{CC} = 1.5V, all inputs = 1.5V		15	30	mA
$I_{CC(PD2)}$	Power-down supply current from V_{CC}	V_{CC} = 2.0V, all inputs = 2.0V		20	40	mA

Timing Requirements (T_a = 0 ~ 70°C, V_{CC} = 5V ±5%, unless otherwise noted)

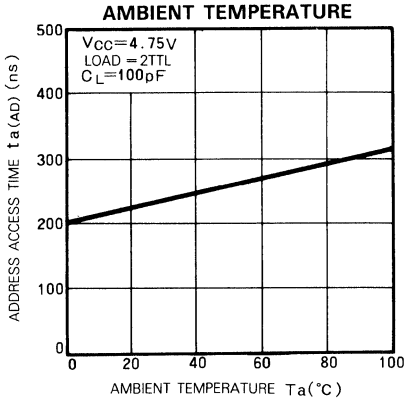
Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
$t_{su(PD)}$	Power-down setup time	0			ns
$t_{R(PD)}$	Power-down recovery time	$t_{c(RD)}$			ns

Timing Diagram

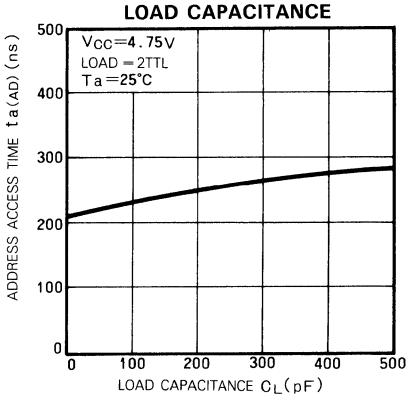


TYPICAL CHARACTERISTICS

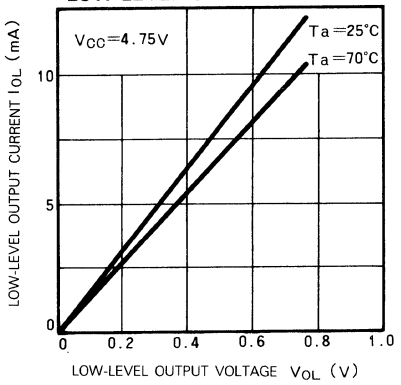
ADDRESS ACCESS TIME VS. AMBIENT TEMPERATURE



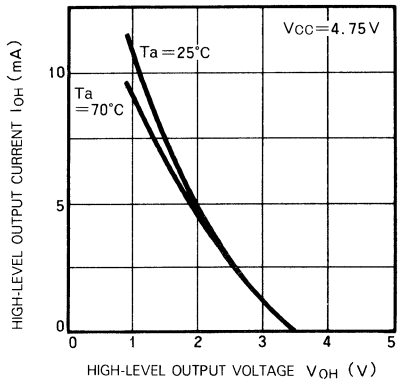
ADDRESS ACCESS TIME VS. LOAD CAPACITANCE



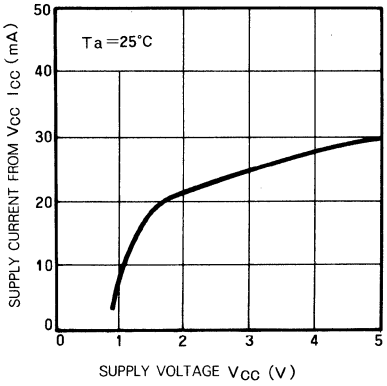
LOW-LEVEL OUTPUT CURRENT VS. LOW-LEVEL OUTPUT VOLTAGE



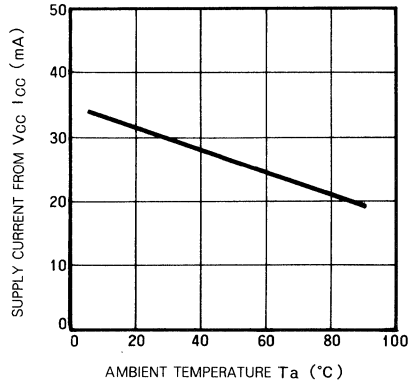
HIGH-LEVEL OUTPUT CURRENT VS. HIGH-LEVEL OUTPUT VOLTAGE



SUPPLY CURRENT FROM Vcc VS. SUPPLY VOLTAGE Vcc



SUPPLY CURRENT FROM Vcc VS. AMBIENT TEMPERATURE



M58756K, M58756S

Alternative Designation 2104

4096-BIT (4096-WORD BY 1-BIT) DYNAMIC RANDOM-ACCESS MEMORY

DESCRIPTION

The M58756S and M58756K are 4096-word by 1-bit dynamic RAMs, fabricated with the N-channel silicon-gate MOS process. As it is composed of a dynamic circuit, it requires refreshing every 2ms.

FEATURES

- Fast access time: 300ns (max)
- Fast read cycle time: 425ns (min)
- Refresh interval: 2ms (max)
- Low standby power dissipation: 3μW/bit (typ)
- Low operating power dissipation: 130μW/bit (typ)
- All inputs are directly TTL-compatible
- All outputs are three-state and directly TTL-compatible; data can be latched, effective until the next cycle
- Easy memory expansion by chip select signal ($\overline{CS}$)
- Interchangeable with Intel's 2104 in pin configuration and electrical characteristics

APPLICATION

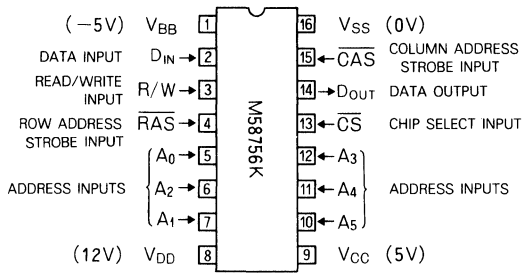
- Main, memory systems for computers

FUNCTION

Being dynamic RAMs, the M58756S and M58756K must be refreshed every 2ms to hold data stored in the memory cells. Refresh must be performed by reading sequentially the 64 locations designated by the 6 address signals A_0~A_5 and clock signal RAS.

The output terminals of the M58756S and M58756K are kept in the floating (high-impedance) state by clock signal $\overline{CAS}$, after which the data is read out from the output terminal during a read cycle.

PIN CONFIGURATION (TOP VIEW)



Outline 16K1 (M58756K)
16S1 (M58756S)

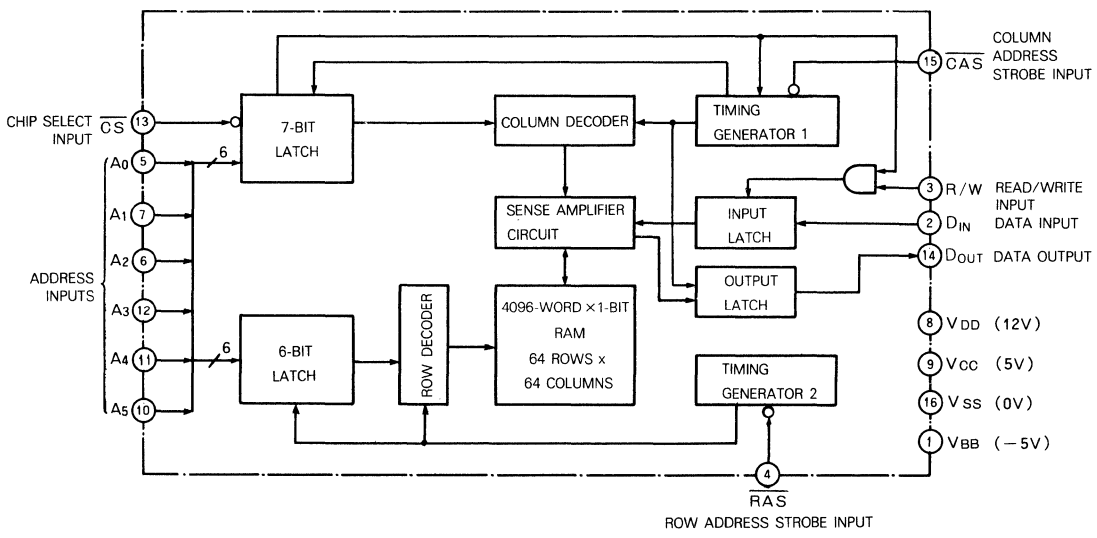
SUMMARY OF OPERATIONS

Input				Output *	Refresh	Operations
$\overline{RAS}$	$\overline{CAS}$	$\overline{CS}$	R/W			
A	A	A	A	(Valid data)—Open—High-level	Can	Write cycle
A	A	A	I	(Valid data)—Open—(Valid data)	Can	Read cycle
A	A	I	DC	(Valid data)—Open—Open	Can	Refresh
I	A	DC	DC	(Valid data)—Open—Open	Can't	Standby Output open
I	I	DC	DC	(Valid data)—(Valid data) —(Valid data)	Can't	Standby

* Previous cycle—between cycles—actual cycle

A : Operating states I: Nonoperating DC: Don't care

BLOCK DIAGRAM



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M58756K, M58756S

Alternative Designation 2104

4096-BIT (4096-WORD BY 1-BIT) DYNAMIC RANDOM-ACCESS MEMORY

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{DD}	Supply voltage	With respect to V_{BB}	−0.3～ 20	V
V_{CC}	Supply voltage		−0.3～ 20	V
V_{SS}	Supply voltage		−0.3～ 20	V
V_I	Input voltage		−0.3～ 20	V
V_O	Output voltage		−0.3～ 20	V
P_d	Maximum power dissipation	Ta=25°C	1000	mW
Topr	Operating free-air ambient temperature		0～70	°C
Tstg	Storage temperature		−55～150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0～70°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{DD}	Supply voltage	10.8	12	13.2	V
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{BB}	Supply voltage	−4.5	−5	−5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage	−1.0		0.6	V

ELECTRICAL CHARACTERISTICS (Ta=0～70°C, V_{DD}=12V±10%, V_{CC}=5V±10%, V_{SS}=0V, V_{BB}=−5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2.4		6.5	V
V_{IL}	Low-level input voltage		−1.0		0.6	V
V_{OH}	High-level output voltage	I_{OH}=−5.0mA	2.4		V_{CC}	V
V_{OL}	Low-level output voltage	I_{OL}=2.0mA	0		0.4	V
I_I	Input current	V_I=−1.0～6.5V			10	μA
I_{OZ}	Off-state output current	$V_{I(\overline{CS})}$=2.4V			10	μA
I_{DD1}	Supply current from V_{DD}, when chip deselected	$V_{I(\overline{CAS})}$, $V_{I(\overline{RAS})}$=V_{IH}		1	2	mA
I_{DD2}	Supply current from V_{DD}, when chip selected			1	2	mA
$I_{DD(AV)}$	Averge supply current from V_{DD}	t_C=425ns, $t_{W(\overline{RAS}H)}$=125ns, Ta=25°C		43	56	mA
I_{CC}	Supply current from V_{CC}	V_O= no load			10	μA
I_{BB}	Supply current from V_{BB}				75	μA
$C_{i(AD)}$	Input capacitance, address terminals	V_I=V_{SS}, V_{BB}=−5V, f=1MHz, V_i=25mVrms			10	pF
$C_{i(DA)}$	Input capacitance, data input terminals				7	pF
$C_{i(R/W)}$	Input capacitance, R/W terminal				7	pF
$C_{i(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ terminal				7	pF
$C_{i(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ terminal				7	pF
$C_{i(\overline{CS})}$	Input capacitance, $\overline{CS}$ terminal				7	pF
C_O	Output capacitance	V_O=V_{SS}, V_{BB}=−5V, f=1MHz, V_i=25mVrms			8	pF

Note 1 : Current flowing into an IC is positive; out is negative.

4096-BIT (4096-WORD BY 1-BIT) DYNAMIC RANDOM-ACCESS MEMORY

TIMING REQUIREMENTS (For Read, Write or Read-Modify-Write Cycle)

($Ta = 0 \sim 70°C$, $V_{DD} = 12V \pm 10\%$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, $V_{BB} = -5V \pm 10\%$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
$t_{c(REF)}$	Refresh cycle time				2	ms
$t_{w(\overline{RAS}H)}$	$\overline{RAS}$ high pulse width		125			ns
$t_{d(\overline{RAS}\text{-}\overline{CAS})}$	Delay time between $\overline{RAS}$ and $\overline{CAS}$		90		2000	ns
$t_{su(RA\text{-}\overline{RAS})}$	Row address setup time with respect to $\overline{RAS}$		0			ns
$t_{su(CA\text{-}\overline{CAS})}$	Column address setup time with respect to $\overline{CAS}$		0			ns
$t_{su(\overline{CS}\text{-}\overline{CAS})}$	Chip select setup time with respect to $\overline{CAS}$		0			ns
$t_{h(\overline{RAS}\text{-}RA)}$	Row address hold time with respect to $\overline{RAS}$		50			ns
$t_{h(\overline{CAS}\text{-}CA)}$	Column address hold time with respect to $\overline{CAS}$		50			ns
$t_{h(\overline{CAS}\text{-}\overline{CS})}$	Chip select hold time with respect to $\overline{CAS}$		50			ns
$t_{su(\overline{CAS}\text{-}\overline{RAS})}$	$\overline{CAS}$ setup time with respect to $\overline{RAS}$		−50		50	ns
t_{PXZ}	Output invalid time from $\overline{CAS}$		0		80	ns
t_T	Transition time		5		50	ns

SWITCHING CHARACTERISTICS ($Ta = 0 \sim 70°C$, $V_{DD} = 12V \pm 10\%$, V_{CC} $5V \pm 10\%$, $V_{SS} = 0V$, $V_{BB} = -5V \pm 10\%$, unless otherwise noted)

Read Cycle

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{c(RD)}$	Read cycle time		425			ns
$t_{w(\overline{CAS}L)}$	$\overline{CAS}$ low pulse width		200		10000	ns
$t_{w(\overline{RAS}L)}$	$\overline{RAS}$ low pulse width		300		32000	ns
$t_{h(\overline{CAS}\text{-}\overline{RAS})}$	$\overline{RAS}$ hold time with respect to $\overline{CAS}$		200			ns
$t_{h(\overline{CAS}\text{-}RD)}$	Read hold time with respect to $\overline{CAS}$		80			ns
$t_{su(RD\text{-}\overline{CAS})}$	Read setup time with respect to $\overline{CAS}$		0			ns
$t_{h(\overline{RAS}\text{-}\overline{CAS})}$	$\overline{CAS}$ hold time with respect to $\overline{RAS}$		300			ns
$t_{a(\overline{CAS})}$	$\overline{CAS}$ access time	$C_L = 50pF$, Load = 1TTL			200	ns
$t_{a(\overline{RAS})}$	$\overline{RAS}$ access time	$C_L = 50pF$, Load = 1TTL (Note 7)			300	ns

Write Cycle

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{c(WR)}$	Write cycle time		425			ns
$t_{w(\overline{CAS}L)}$	$\overline{CAS}$ low pulse width		200		10000	ns
$t_{w(\overline{RAS}L)}$	$\overline{RAS}$ low pulse width		300		32000	ns
$t_{h(\overline{CAS}\text{-}\overline{RAS})}$	$\overline{RAS}$ hold time with respect to $\overline{CAS}$		200			ns
$t_{su(WR\text{-}\overline{CAS})}$	Write setup time with respect to $\overline{CAS}$		200			ns
$t_{h(\overline{CAS}\text{-}WR)}$	Write hold time with respect to $\overline{CAS}$		130			ns
$t_{w(WR)}$	Write pulse width		200			ns
$t_{su(DA\text{-}\overline{CAS})}$	Data setup time with respect to $\overline{CAS}$		0			ns
$t_{h(\overline{CAS}\text{-}DA)}$	Data hold time with respect to $\overline{CAS}$		130			ns
$t_{h(\overline{RAS}\text{-}\overline{CAS})}$	$\overline{CAS}$ hold time with respect to $\overline{RAS}$		300			ns

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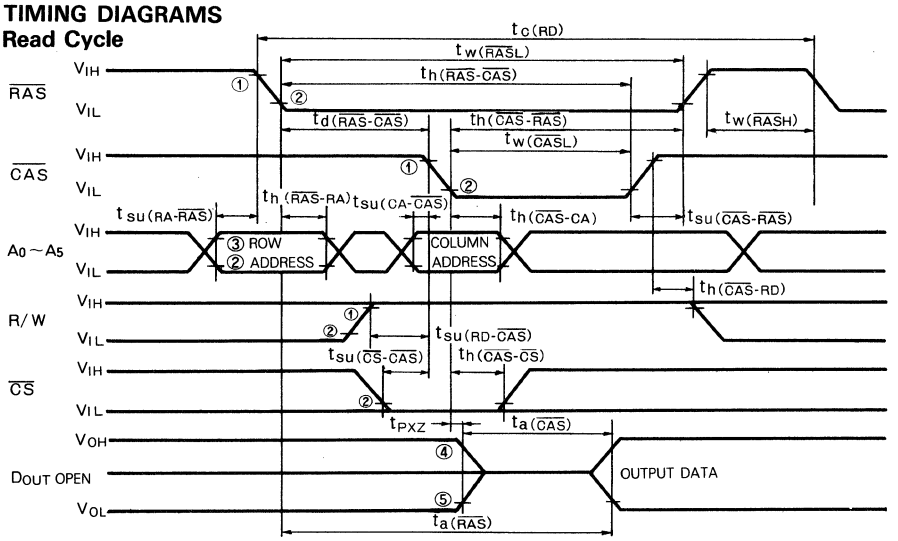
4096-BIT (4096-WORD BY 1-BIT) DYNAMIC RANDOM-ACCESS MEMORY

Read-Modify-Write Cycle

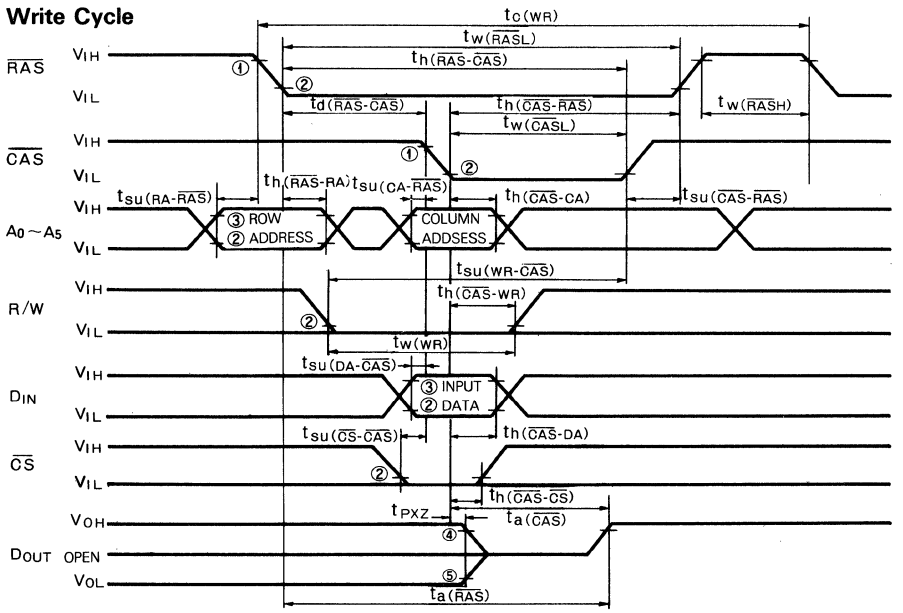
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{c(RMW)}$	Read-modify-write cycle time		595			ns
$t_{w(\overline{CAS}L)}$	$\overline{CAS}$ low pulse width		320		10000	ns
$t_{w(\overline{RAS}L)}$	$\overline{RAS}$ low pulse width		450		32000	ns
$t_{su(WR-\overline{RAS})}$	Write setup time with respect to $\overline{RAS}$		200			ns
$t_{su(WR-\overline{CAS})}$	Write setup time with respect to $\overline{CAS}$		200			ns
$t_{w(WR)}$	Write pulse width		200			ns
$t_{su(RD-\overline{CAS})}$	Read setup time with respect to $\overline{CAS}$		0			ns
t_{MOD}	Modify time		0			ns
$t_{su(DA-WR)}$	Data setup time with respect to write		0			ns
$t_{h(WR-DA)}$	Data hold time with respect to write		170			ns

TIMING DIAGRAMS

Read Cycle



Write Cycle



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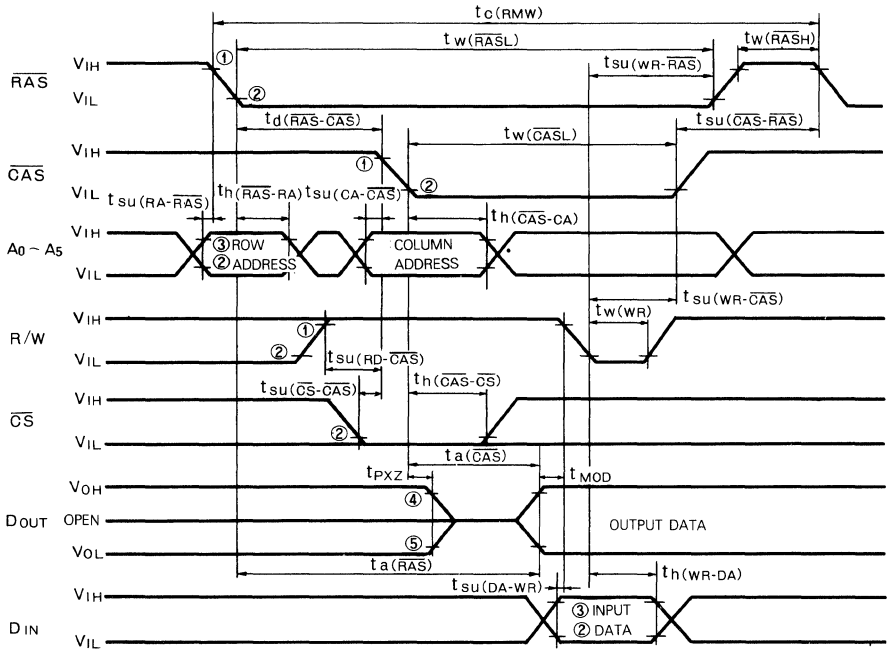
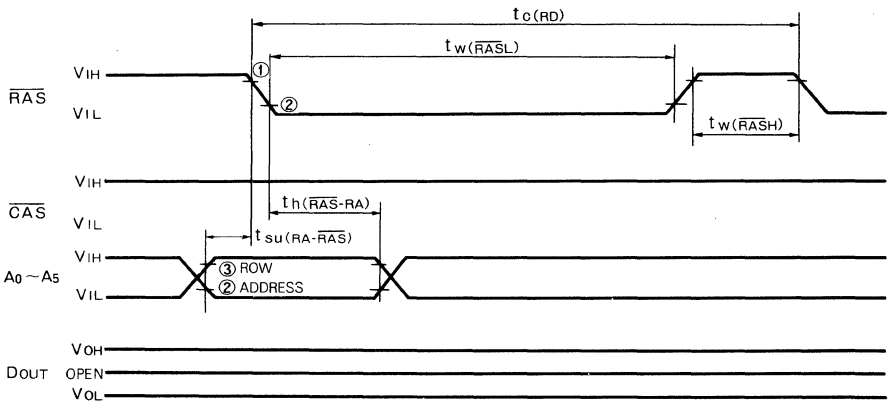
Read-Modify-Write Cycle



RAS Only Refresh Cycle



Note 3 : Reference level for ①, ③ and ④ is 2.4V.

4 : Reference level for ② is 0.6V.

5 : Reference level for ⑤ is 0.4V.

6 : Both rise time t_r and fall time t_f should be less than 10ns.

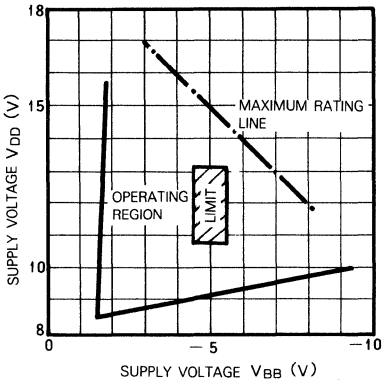
7 : $t_{a(\overline{RAS})max.} = t_{d(\overline{RAS}\text{-}\overline{CAS})min.} + t_T + t_{a(\overline{CAS})max.}$ when $t_{d(\overline{RAS}\text{-}\overline{CAS})} > t_{d(\overline{RAS}\text{-}\overline{CAS})min.}$, $t_{a(\overline{RAS})}$ increases by the amount of increase of $t_{d(\overline{RAS}\text{-}\overline{CAS})}$

5

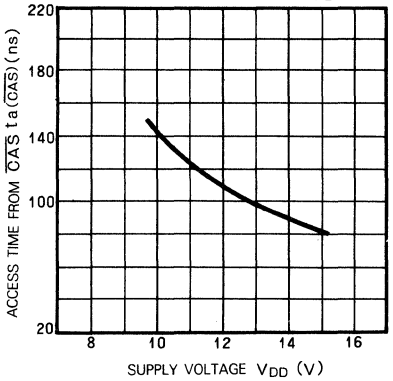
4096-BIT (4096-WORD BY 1-BIT) DYNAMIC RANDOM-ACCESS MEMORY

TYPICAL CHARACTERISTICS

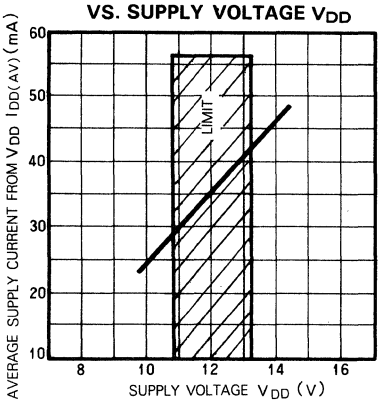
V_{DD} VS. V_{BB} OPERATING REGION



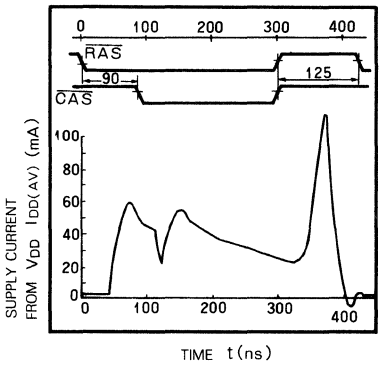
ACCESS TIME FROM $\overline{CAS}$ VS. SUPPLY VOLTAGE V_{DD}



AVERGE SUPPLY CURRENT FROM V_{DD} VS. SUPPLY VOLTAGE V_{DD}



SUPPLY CURRENT FROM V_{DD} VS. TIME



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READ-ONLY MEMORIES

6

DEVELOPMENT OF CUSTOM MASK ROMs

DESCRIPTION

Mitsubishi can provide the following mask ROMs made to a customer's specifications.

M58730-XXXS	1024-word by 8-bit mask ROM
M58731-XXXS	2048-word by 8-bit mask ROM
M58609-XXS	Keyboard encoder
M58620-XXXS	Keyboard encoder

An automatic mask design program has been developed to assure production of mask ROMs without errors, rapidly, in accordance with the specifications of the customer. On the basis of data supplied by the customer, the program automatically generates the following:

1. The plotter instructions for automatic mask production.
2. A check list for verifying that the customer's specifications have been met.
3. A test program to assure that the production ROMs meet specifications.

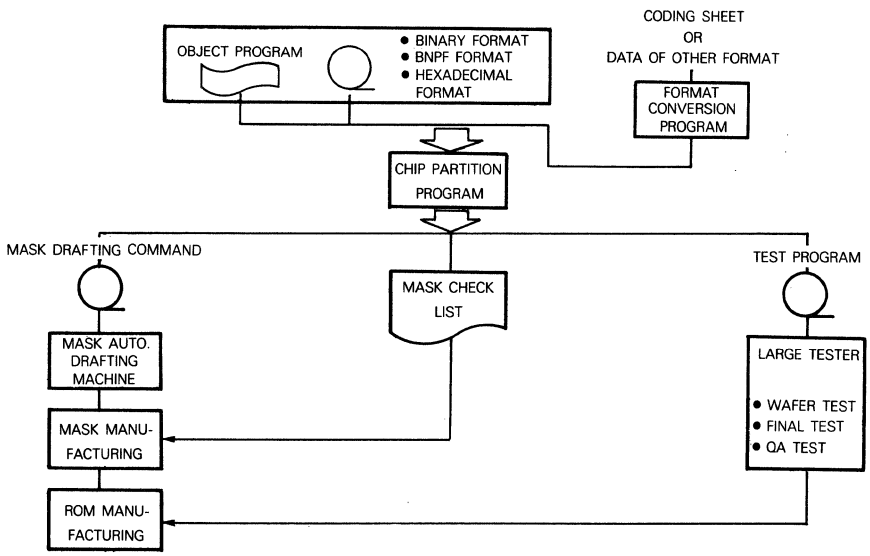
1. M58730-XXXS and M58731-XXXS Mask ROMs

The object program for mask encoding can be in MELPS 8 binary, hexadecimal or BNPF form. The object program format is the same as the produced by a MELPS 8 cross assembler or a PL/Iμ cross compiler. The standard medium used for transmitting an object program is paper tape; however, magnetic tape may also be used.

2. M58609-XXS and M58620-XXXS Keyboard Encoders

Submit the character codes, corresponding to each key, on the coding sheet in octal form.

MASK ROM AUTOMATIC DESIGN PROGRAM



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M58730-XXXS

Alternative Designation 8308

8192-BIT (1024-WORD BY 8-BIT) MASK-PROGRAMMABLE ROM

DESCRIPTION

The M58730-XXXS is an 8192-bit static MOS mask-programmable read-only memory organized as 1024 words of 8 bits. It is fabricated using N-channel silicon-gate MOS technology, and is designed for fixed-memory applications such as program storage with an M58710S 8-bit parallel CPU. The inputs and outputs are TTL-compatible. Programming is performed by Mitsubishi in accordance with the customer's specifications by changing a single mask during the manufacturing cycle.

The XXX in the type code stands for a 3-digit decimal number which is assigned by Mitsubishi to identify the customer's specifications to which the ROM has been programmed.

FEATURES

- Fast access time: 850ns (max.)
- Two chip select inputs ($\overline{CS_1}$, CS_2) for easy memory expansion
- Three-state output; OR-tie capability
- Inputs and outputs are TTL-compatible.
- Input protection circuits for all inputs
- Pins compatible with Intel's 8308

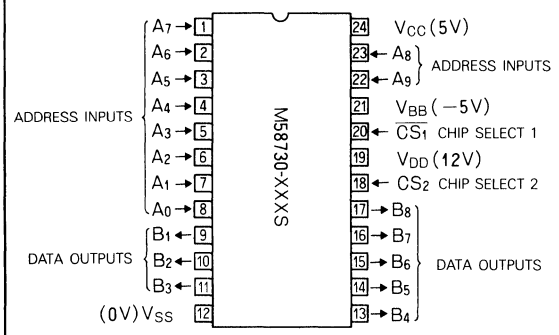
APPLICATION

- Microcomputer memories

FUNCTION

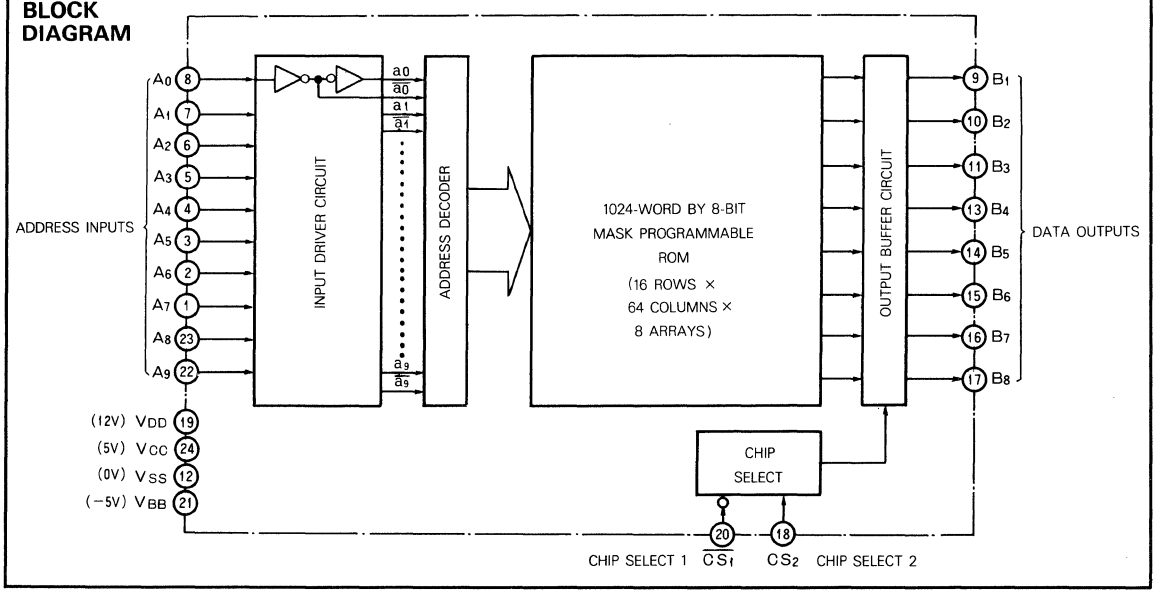
Address inputs A_0~A_9 are decoded to select one of the 1024 words, and the contents of that address are read out to data outputs B_1~B_8. Chip select 1 ($\overline{CS_1}$) and chip select 2 (CS_2) are used to connect two or more M58730-XXXS ROMs. When $\overline{CS_1}$ is high or CS_2 is low, all outputs are disabled and will assume a floating (high-impedance) states.

PIN CONFIGURATION (TOP VIEW)



Outline 24S1

BLOCK DIAGRAM



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8192-BIT (1024-WORD BY 8-BIT) MASK-PROGRAMMABLE ROM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{DD}	Supply voltage	With respect to V_{BB}	−0.3～20	V
V_{CC}	Supply voltage		−0.3～20	V
V_{SS}	Supply voltage		−0.3～20	V
V_I	Input voltage		−0.3～20	V
Pd	Power dissipation	Ta＝25°C	1.0	W
Topr	Operating free-air temperature		0－70	°C
Tstg	Storage temperature		−65～150	°C

RECOMMENDED OPERATING CONDITIONS (Ta＝0～70°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{DD}	Supply voltage	11.4	12	12.6	V
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{SS}	Supply voltage		0		V
V_{BB}	Supply voltage	−4.75	−5	−5.25	V
V_{IH}	High-level input voltage	3.3		$V_{CC}+1$	V
V_{IL}	Low-level input voltage	$V_{SS}-1$		0.8	V

ELECTRICAL CHARACTERISTICS (Ta＝0～70°C, V_{DD}＝12V±5%, V_{CC}＝5V±5%, V_{SS}＝0V, V_{BB}＝−5V±5%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{OH}	High-level output voltage	I_{OH}＝−100μA	$V_{CC}-1$			V
V_{OL}	Low-level output voltage	I_{OL}＝1.9mA			0.45	V
I_I	Input current	V_I＝0V～V_{CC}			±10	μA
I_{OZ}	Off-state output current	V_O＝0V～V_{CC} ($\overline{CS_1}$ and CS_2 are in a floating condition. see Timing Diagram)			10 −100	μA
I_{DD}	V_{DD} supply current				60	mA
I_{CC}	V_{CC} supply current	Output open			100	μA
I_{BB}	V_{BB} supply current			−0.01	−1	mA
C_I	Input capacitance	Ta＝25°C, V_I＝0V, 1MHz, 25mVrms V_{DD}＝V_{CC}＝V_{SS}＝0V (Note 2)			10	pF
C_O	Output capacitance	Ta＝25°C, V_I＝0V, 1MHz, 25mVrms V_{DD}＝V_{CC}＝V_{SS}＝0V (Note 2)			10	pF

Note 1 : The current flowing into an IC is positive; out is negative. The maximum and minimum are defined by absolute values.

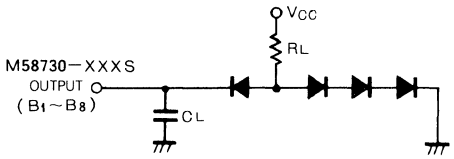
2 : All terminals other than the test terminal are connected to V_{SS} during measurement of input and output capacitance.

8192-BIT (1024-WORD BY 8-BIT) MASK-PROGRAMMABLE ROM

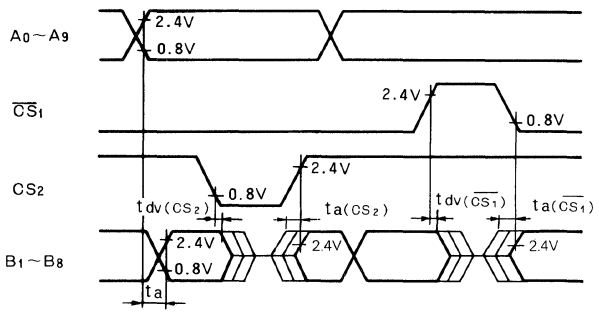
SWITCHING CHARACTERISTICS ($Ta = 0 \sim 70°C$, $V_{DD} = 12V \pm 5\%$, $V_{CC} = 5V \pm 5\%$, $V_{SS} = 0V$, $V_{BB} = -5V \pm 5\%$, unless otherwise noted).

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
ta	Access time	$C_L = 100pF$, $R_L = 2.1k\Omega$ (Note 3)		400	850	ns
$ta(\overline{CS_1})$	Chip select access time			100	300	ns
$ta(CS_2)$	Chip select Access time			100	300	ns
$tdv(\overline{CS_1})$	Data valid time with respect to $\overline{CS_1}$			100	300	ns
$tdv(CS_2)$	Data valid time with respect to CS_2			100	300	ns

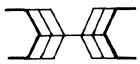
Note 3 : Load circuit diagram:



TIMING DIAGRAM



Chip select 1 $\overline{CS_1}$	Chip select 2 CS_2	Data output $B_1 \sim B_8$
L	L	Z
H	L	Z
L	H	O
H	H	Z

Note 1 :  THE CENTER LINE INDICATES A FLOATING (HIGH-IMPEDANCE) STATE

2 : H indicates high-level inputs; L indicates low-level inputs.

3 : Z indicates floating (off) state

4 : O indicates that outputs are enabled.

5 : Rise time $t_r \leqq 20ns$,
Fall time $t_f \leqq 20ns$.

6

M58730-XXXS

Alternative Designation 8308

8192-BIT (1024-WORD BY 8-BIT) MASK-PROGRAMMABLE ROM

ORDERING INFORMATION

This information covers the M58730-XXXS ROM and the object program required for the automatic mask design program. An automatic mask design program has been developed that accepts a customer's specifications and then automatically generates the following:

1. The plotter instructions for automatic mask production.
2. A check list for verifying that the customer's specifications have been met.
3. A test program to assure that the production ROMs meet specifications.

The object program for the automatic mask design program may be supplied in MELPS 8 binary, hexadecimal or BNPF form. The format of the data is the same as the output from a MELPS 8 cross assembler or a PL/Iμ cross compiler. It accepts either standard punched paper tape or magnetic tape as the input medium.

A separate tape should be produced for each object program. The tape along with a printout of the truth table, for confirmation, should accompany each order.

1. Object Program Format

- Object program addresses are absolute.
- The data can be in either MELPS 8 binary, hexadecimal or BNPF form.
- The output tape from a MELPS 8 cross assembler, or PL/Iμ cross compiler can be used.
- The hexadecimal and BNPF formats are Intel-compatible.
- The character code can be ASCII or ISO, with or without parity.

2. Object Program Medium

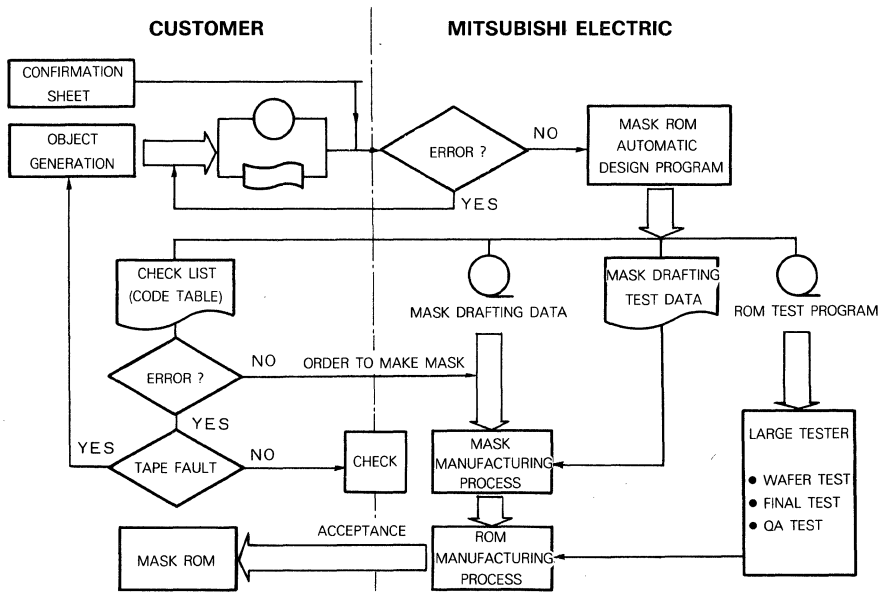
- Paper tape: 8-level, 25.4mm (1 inch) wide
- Magnetic tape: 9-track, 800 BPI, odd parity

3. Items for Confirmation

- The format of the object program
- Type number of the M58730-XXXS (including the 3-digit number represented by XXX)
- A truth table printout of memory state

Note : Details for preparation of the object program tape and confirmation material are given in § 4 following.

MASK ROM DEVELOPMENT FLOW CHART



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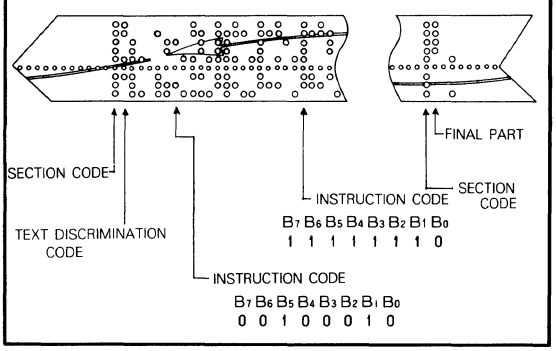
4. Object Program Preparation and Format

1. MELPS 8 Binary

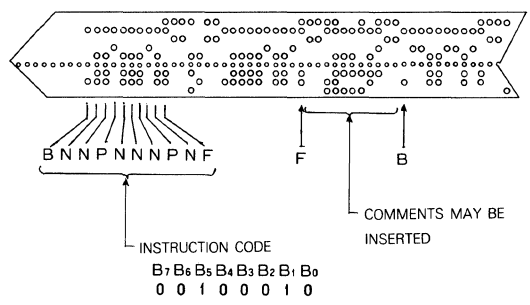
Example of MELPS 8 binary paper tape



- A separate tape should be prepared for each object program. Two copies of the tape should be supplied.
- The final part code should be inserted at the end of each tape.
- The first address of the ROM should be indicated.
- The region outside the range from the first address to the first address + 1024 is ignored.
- The ROM addresses may be non-sequential in the object program.
- The unused area within a chip will be filled with '1's. If '1's are not suitable, appropriate digits should be indicated.
- It should be indicated whether the area to be programmed is the ROM only, the RAM only, or both.
- All parts except the text and final part are ignored.
- The levels of bit code '1' and '0' should be specified as low or high.
- At least 50 frames of sprocket holes should be punched at the start and the end of the tape.

2. BNPF

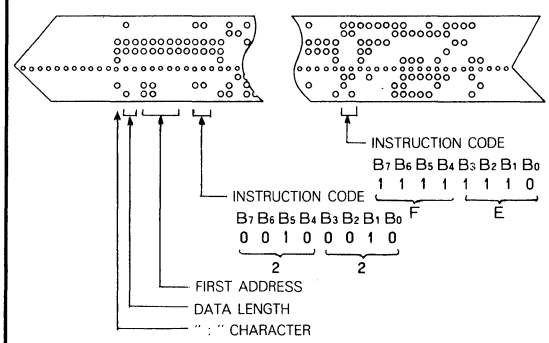
Example of BNPF paper tape



- This format is Intel-compatible.
- A separate tape should be prepared for each object program. Two copies of the tape should be supplied.
- The unused area within a chip should be filled with appropriate codes.
- When less than 1024 bytes are used, the unused area should be filled with appropriate codes, or a '$' character may be inserted at the end of the used area. In the latter case, the remaining area is filled with 'L's.
- Comments, not containing any 'B' or '$' characters, may be inserted between the 'F' and 'B'.
- The character code is ASCII or ISO, with or without parity.
- The address is incremented in sequence by the data string.
- The magnitude of the bits between the 'B' and 'F' is defined as from high order to low order.
- At least 50 frames of sprocket holes should be punched at the start and the end of the tape.
- The levels of 'P' and 'N' should be specified as either low or high.

3. Hexadecimal

Example of hexadecimal paper tape



- This format is Intel-compatible.
- A separate tape should be prepared for each object program. Two copies of the tape should be supplied.
- A record of data length zero is considered the end of one chip's data.
- The first address of the ROM should be indicated.
- The region outside the range from the first address to the first address + 1024 is ignored.
- The ROM addresses may be non-sequential in the object program.
- The unused area within a chip will be filled with '0's. If '0's are not suitable, appropriate digits should be indicated.
- The character code is ASCII or ISO code with or without parity.
- The levels of bit codes '1' and '0' should be specified as either low or high.
- At least 50 frames of sprocket holes should be punched at the start and the end of the tape.

6

M58730-001S

8192-BIT (1024-WORD BY 8-BIT) MASK-PROGRAMMED ROM SUBROUTINE 1 INTEGER ARITHMETIC OPERATIONS

DESCRIPTION

- The M58730-001S is an M58730-XXXS that has been developed for use with an M58710S CPU.
- It includes 18 subroutines for an M58710S 8-bit parallel CPU.
- It can perform integer arithmetic operations, logical operations and shift operations with 16-bit or 32-bit data.

UNIT OF INFORMATION

The basic unit of an M58710S is 8 bits, but with subroutines it has two operand lengths.

- Single word length:

An operand consisting of 2 bytes (16 bits). In binary form it is capable of expressing numbers from -2^{15} to $2^{15}-1$.

- Double word length:

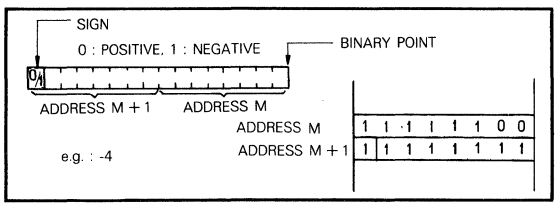
An operand consisting of 4 bytes (32 bits). In decimal form it is equivalent to 7 decimal digits. In binary form it is capable of expressing numbers from -2^{31} to $2^{31}-1$.

NUMERICAL EXPRESSIONS

1. Binary Numbers

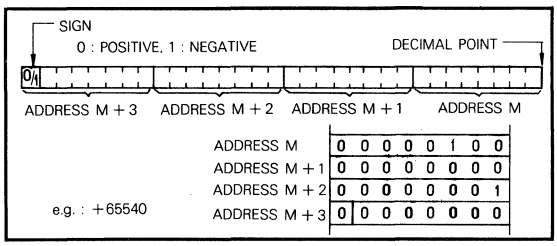
1. Single Word Length (2 Bytes)

This binary number consists of 16 bits. Negative numbers are in 2's complement form. It is capable of expressing numbers from -2^{15} to $2^{15}-1$.



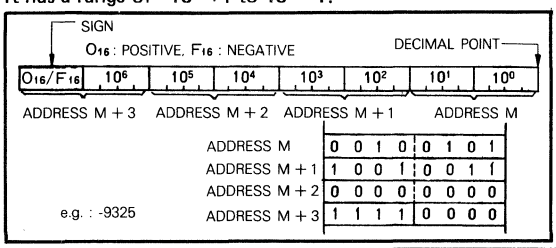
2. Double Word Length (4 bytes)

This binary number consists of 32 bits. Negative numbers are in 2's complement form. It is capable of expressing numbers from -2^{31} to $2^{31}-1$.

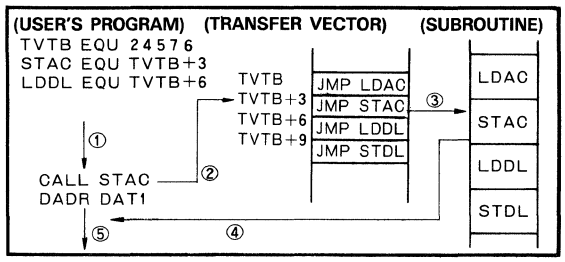


2. Double Word Length Decimal Numbers

This decimal number consists of 32 bits. The numerical portion is seven digits and the sign is the most significant digit. It has a range of -10^7+1 to 10^7-1.



SUBROUTINE REFERENCE



Note : The processing order is ①, ②, ③, ④, ⑤. A transfer vector is used to set the entry address of each subroutine.

SUBROUTINE FUNCTIONS

- Load pseudo accumulator

The pseudo accumulator is loaded with the specified single word (2 bytes) or double word (4 bytes) data.

- Store pseudo accumulator

The contents of the pseudo accumulator, single word (2 bytes) or double word (4 bytes) data, is stored in the address location specified.

- Shift pseudo accumulator

The contents of the pseudo accumulator, 32 bits (2 words) of data, are shifted right or left n positions.

- Arithmetic right shift of pseudo accumulator

The contents of the pseudo accumulator, 32 bits (2 words) of data, are arithmetically shifted right n positions.

- Logical operations

The specified single word (2 bytes) data is logically inclusive ORed, ANDed or exclusive ORed to the contents of the pseudo accumulator, and the result retained in the pseudo accumulator.

- Binary integer add or subtract

The specified single word (2 bytes) or double word (4 bytes) binary data is binarily added to or subtracted from the contents of the pseudo accumulator, and the result is retained in the pseudo accumulator.

- Decimal integer add or subtract

The specified double word (4 bytes) decimal data is decimally added to or subtracted from the contents of the pseudo accumulator, and the result is retained in the pseudo accumulator.

- Binary integer multiply

The single word (2 bytes) data in the pseudo accumulator is multiplied by a specified single word (2 bytes) data, and the result is retained in the pseudo accumulator.

- Binary integer divide

The double word (4 bytes) data in the pseudo accumulator is divided by a specified single word (2 bytes) data, and the result is retained in the pseudo accumulator.

RESERVED MEMORY LOCATIONS

Memory locations 6000_{16} to $63FF_{16}$ are reserved by ROM. In addition, a 50-byte RAM region, locations $3FCE_{16}$ to $3FFF_{16}$, is reserved for executing the ROM programs.

M58731-XXXP, M58731-XXXS

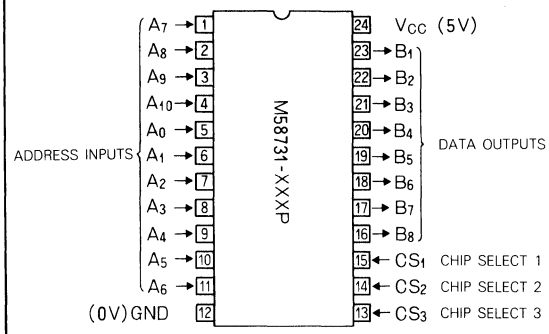
Alternative Designation 8316A

16384-BIT (2048-WORD BY 8-BIT) MASK-PROGRAMMABLE ROM

DESCRIPTION

The M58731-XXXP, S are 16,384-bit parallel output, static read-only memories organized as 2048 words of 8 bits. They are fabricated using N-channel silicon-gate ED-MOS technology. They have a single supply voltage. The inputs and outputs interface with TTL circuits without additional circuits. The M58731-XXXP, S are designed for high-density fixed-memory applications such as program storage for an M58710S 8-bit parallel CPU. Programming is performed by Mitsubishi in accordance with the customer's specifications by changing a single mask during the manufacturing cycle.

PIN CONFIGURATION (TOP VIEW)



Outline 24P1 (M58731-XXXP)
24S1 (M58731-XXXS)

FEATURES

- 2048-word by 8-bit organization
- Single 5V power supply
- Low power dissipation: 31.4μW/bit (max.)
- Read access time: 850ns (max.)
- Three programmable chip select inputs (CS_1, CS_2, CS_3) for easy memory expansion
- Three-state output for OR-ties
- All inputs and outputs are TTL-compatible
- Input protection circuits at all inputs
- Electrical characteristics and pins are compatible with Intel's 8316A.

APPLICATION

- High-density microcomputer memories

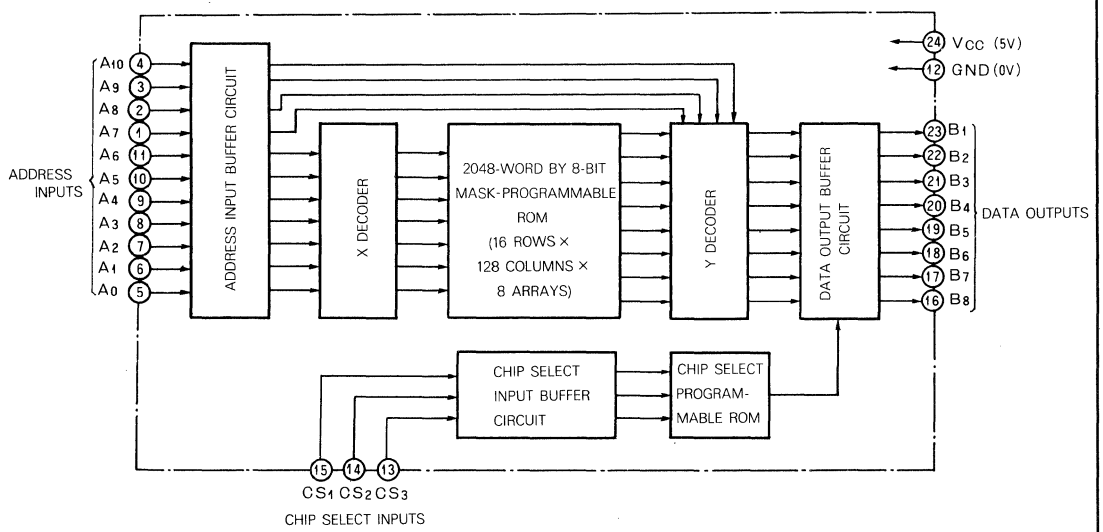
FUNCTION

When any of the 2048 addresses are selected by positive-logic input signals (A_0~A_{10}), the contents of that address in the ROM are read out to the data outputs (B_1~B_8). A_0 is the least-significant bit and A_{10} is the most-significant bit of the address. The three chip select inputs are programmable during the masking process, and any combination of active high-level and active low-level may be used for chip selection. When a chip is selected, the contents of the ROM are read out; and under other conditions, the data outputs (B_1~B_8) are in the floating (high-impedance) state.

The XXX in the type code stands for a 3-digit decimal number which is assigned by Mitsubishi to identify the customer's specifications to which the ROM has been programmed.

6

BLOCK DIAGRAM



M58731-XXXP, M58731-XXXS

Alternative Designation 8316A

16384-BIT (2048-WORD BY 8-BIT) MASK-PROGRAMMABLE ROM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Conditions	Limits	Unit
V_{CC}	Supply voltage		With respect to GND	−0.5～7.0	V
V_I	Input voltage			−0.5～7.0	V
V_O	Output voltage			−0.5～7.0	V
P_d	Power dissipation	M58731-XXXP	Ta＝25°C	500	mW
		M58731-XXXS		1000	mW
Topr	Operating free-air temperature range			0～70	°C
Tstg	Storage temperature range	M58731-XXXP		−40～125	°C
		M58731-XXXS		−65～150	°C

RECOMMENDED OPERATING CONDITIONS (Ta＝0～70°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	V
GND			0		V
V_{IH}	High-level input voltage	2.0		V_{CC}+1.0	V
V_{IL}	Low-level input voltage	−0.5		0.8	V

ELECTRICAL CHARACTERISTICS (Ta＝0～70°C, V_{CC}＝5V±5%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{OH}	High-level output voltage	I_{OH}＝−100μA	2.2			V
V_{OL}	Low-level output voltage	I_{OL}＝2.0mA			0.45	V
I_{CC}	Supply current from V_{CC}	All inputs＝5.25V, output open		40	98	mA
I_I	Input current	V_I＝0V～V_{CC}			10	μA
I_{OZ}	Off-state input current	Floating state, V_I＝0.45V～V_{CC}	−20		10	μA
C_i	Input capacitance	0V except test terminal, 1MHz, Ta＝25°C		4	10	pF
C_O	Output capacitance			8	15	pF

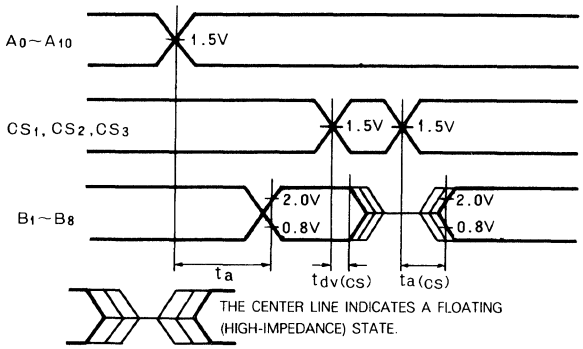
Note 1 : Current flowing into an IC is positive; out is negative.

16384-BIT (2048-WORD BY 8-BIT) MASK-PROGRAMMABLE ROM

SWITCHING CHARACTERISTICS (Ta = 0 ~ 70°C, V_{CC} = 5V ± 5%, unless otherwise noted)

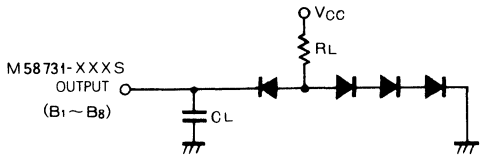
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_a	Access time	C_L = 100pF R_L = 2.1kΩ (Note 2)		400	850	ns
$t_{a(CS)}$	Chip select access time				300	ns
$t_{dv(CS)}$	Data valid time with respect to chip select		0		300	ns

TIMING DIAGRAM



Input pulse level 0.8 ~ 2.0V
Input pulse rise time t_r (10% ~ 90%) 20ns
Input pulse fall time t_f (10% ~ 90%) 20ns
Referance voltage at timing measurement
Input 1.5V
Output 0.8 ~ 2.0V

Note 2 : Load circuit diagram :



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M58731-XXXS

Alternative Designation 8316A

16384-BIT (2048-WORD BY 8-BIT) MASK-PROGRAMMABLE ROM

ORDERING INFORMATION

This information covers the M58731-XXXS ROM and the object program required for the automatic mask design program. An automatic mask design program has been developed that accepts a customer's specifications and then automatically generates the following:

1. The plotter instructions for automatic mask production.
2. A check list for verifying that the customer's specifications have been met.
3. A test program to assure that the production ROMs meet specifications.

The object program for the automatic mask design program may be supplied in MELPS 8 binary, hexadecimal or BNPF form. The format of the data is the same as the output from a MELPS 8 cross assembler or a PL/Iμ cross compiler. It accepts either standard punched paper tape or magnetic tape as the input medium.

A separate tape should be produced for each object program. The tape along with a printout of the truth table, for confirmation, should accompany each order.

1. Object Program Format

- Object program addresses are absolute.
- The data can be in either MELPS 8 binary, hexadecimal or BNPF form.
- The output tape from a MELPS 8 cross assembler, or PL/Iμ cross compiler can be used.
- The hexadecimal and BNPF formats are Intel-compatible.
- The character code can be ASCII or ISO, with or without parity.

2. Object Program Medium

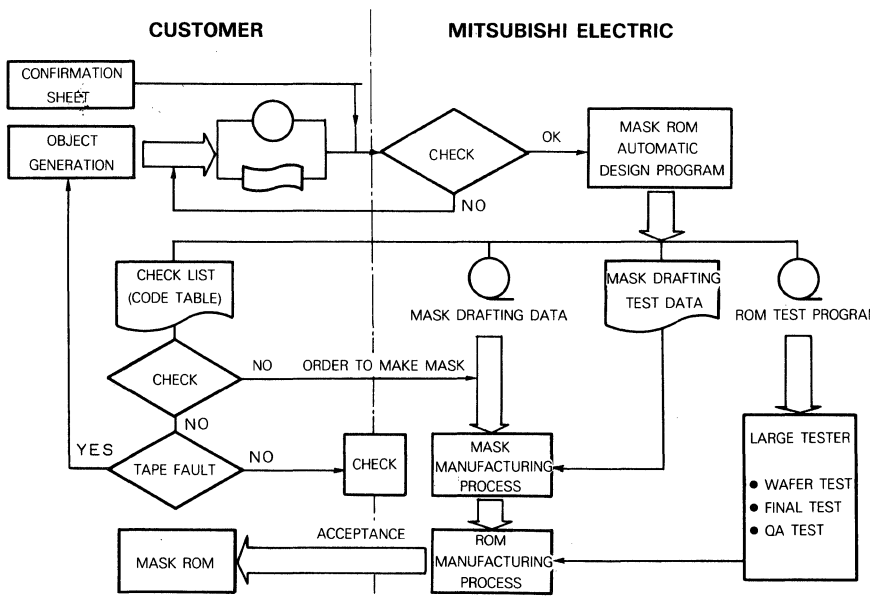
- Paper tape: 8-level, 25.4mm (1 inch) wide
- Magnetic tape: 9-track, 800 BPI, odd parity

3. Items for Confirmation

- The format of the object program
- Type number of the M58731-XXXS (including the 3-digit number represented by XXX)
- The active logic level of the chip select CS_1, CS_2 and CS_3
- A truth table printout of memory state

Note : Details for preparation of the object program tape and confirmation material are given in § 4 following.

MASK ROM DEVELOPMENT FLOW CHART



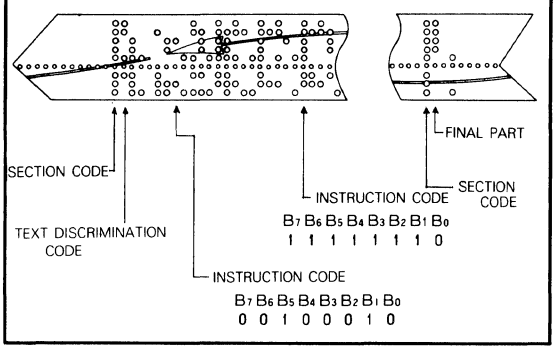
MITSUBISHI ELECTRIC

16384-BIT (2048-WORD BY 8-BIT) MASK-PROGRAMMABLE ROM

4. Object Program Preparation and Format

1. MELPS 8 Binary

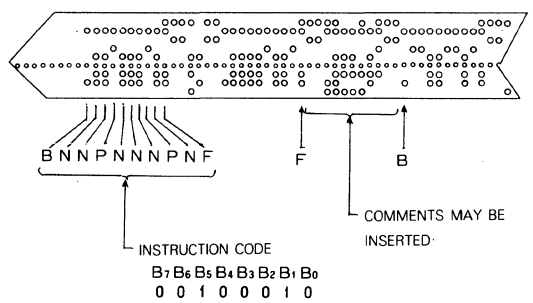
Example of MELPS 8 binary paper tape



- A separate tape should be prepared for each object program. Two copies of the tape should be supplied.
- The final part code should be inserted at the end of each tape.
- The first address of the ROM should be indicated.
- The region outside the range from the frist address to the first address + 2048 is ignored.
- The ROM addresses may be non-sequential in the object program.
- The unused area within a chip will be filled with '1's. If '1's are not suitable, appropriate digits should be indicated
- It should be indicated whether the area to be programmed is the ROM only, the RAM only, or both.
- All parts except the text and final part are ignored.
- The levels of bit code '1' and '0' should be specified as low or high.
- At least 50 frames of sprocket holes should be punched at the start and the end of the tape.

2. BNPF

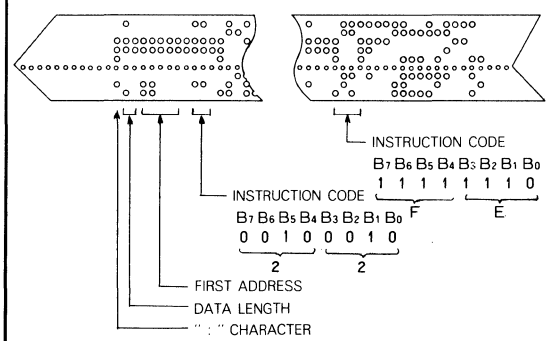
Example of BNPF paper tape



- This format is Intel-compatible.
- A separate tape should be prepared for each object program. Two copies of the tape should be supplied.
- The unused area within a chip should be filled with appropriate codes.
- When less than 2048 bytes are used, the unused area should be filled with appropriate codes, or a '$' character may be inserted at the end of the used area. In the latter case, the remaining area is filled with 'L's.
- Comments, not containing any 'B' or '$' characters, may be inserted between the 'F' and 'B'.
- The character code is ASCII or ISO, with or without parity.
- The address is incremented in sequence by the data string.
- The magnitude of the bits between the 'B' and 'F' is defined as from high order to low order.
- At least 50 frames of sprocket holes should be punched at the start and the end of the tape.
- The levels of 'P' and 'N' should be specified as either low or high.

3. Hexadecimal

Example of hexadecimal paper tape



- This format is Intel-compatible.
- A separate tape should be prepared for each object program. Two copies of the tape should be supplied.
- A record of data length zero is considered the end of one chip's data.
- The first address of the ROM should be indicated.
- The region outside the range from the first address to the first address + 2048 is ignored.
- The ROM addresses may be non-sequential in the object program.
- The unused area within a chip will be filled with '0's. If '0's are not suitable, appropriate digits should be indicated.
- The character code is ASCII or ISO code with or without parity.
- The levels of bit codes '1' and '0' should be specified as either low or high.
- At least 50 frames of sprocket holes should be punched at the start and the end of the tape.

6

M58731-001S

16384-BIT (2048-WORD BY 8-BIT) MASK-PROGRAMMED ROM, MELPS 8 BASIC OPERATING MONITOR BOM-B

DESCRIPTION

The M58731-001S is an M58731-XXXS that has been developed for use with an M58710S CPU. It contains the basic operating monitor BOM-B for an M58710S CPU. BOM-B is a monitor program that controls the execution and debugging of user's programs and is contained in 2K bytes of memory.

FEATURES

- A standard mask ROM useful for microcomputer control and program debugging
- Three macroinstructions and nine monitor commands
- User's monitor commands are easily added
- The BOM-B program cannot be destroyed by a user's program

FUNCTION

The BOM-B has 9 monitor commands and 3 macroinstructions as shown in Table 1. They are used for the following functions:

1. Controlling program execution
2. Loading programs
3. Punching memory
4. Debugging programs
5. Controlling input and output

Start of Execution of BOM-B Program

The execution is started at address 6800_{16}. The following message is printed out and then a monitor command can be typed in: **MELPS8 BOM-B A01**

//

Conditions for Hardware

1. Reserved Memory Locations
   Memory locations 6800_{16} to $6FFF_{16}$ are reserved. In addition a 78-byte RAM region, locations $3FCE_{16}$ to $3FFF_{16}$, is reserved for executing the ROM programs.
2. Input/Output Device Number
   PTR, for keyboard input $7B_{16}$ (IN 7B#)
   PTP, for print output $7B_{16}$ (OUT 7B#)
   Status input $3B_{16}$ (IN 3B#)
   Where the status bits are defined as follows:

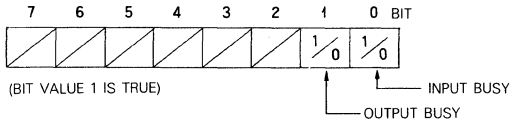


Table 1 A list of the 9 monitor commands and the 3 macroinstructions for BOM-B

Names of monitor commands or macroinstructions		Function	Monitor command input format or calling sequence	Parameter
Command	G	Go to program execution	//G para 1(4) _ [para2(4)] CR LF	para 1(4): Start address para 2(4): Change start address
	R	Program restart	//R CR LF	—
	L	MELPS 8 binary loader	//L CR LF	—
	H	MELPS 8 hexadecimal loader	//H CR LF	—
	T	MELPS 8 binary punch text block of memory data	//T para 1(4), para2(4) CR LF	para 1(4): First address para 2(4): End address
	E	MELPS 8 binary punch end block	//E [para 1(4)] CR LF	para 1(4): Start address
	P	Print hexadecimal text block of memory data	//P para 1(4), para2(4) CR LF	para 1(4): First address para 2(4): End address
	S	Substitute memory	//S para 1(4) CR LF	para 1(4): Change address
	M	Print and modify register data	//M CR LF	—
Macroinstruction	EXIT	Exit the end of a program	CALL 6806 #	
	PAUSE	Pause program execution	CALL 6803 #	
	EXIO	Execution input/output control	CALL 6EBC # ---------- Execute EXIO macroinstruction. DADR DCB1 ---------- First address of data control block (DCB). DCB1 DEF I OD --- IOD for PTR is 52 #, for PTP is 50 #, for KEYBOARD is 4B #, for PRINT is 44 #. DADR DA --- Set the first address of input/output data area. DADR DL --- Set the data length of input/output data. DA: Input/output data store memory (DL bytes)	

Note 1: Para n(m) : A hexadecimal number (0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F) of the nth parameter in one command (of an operator's input or a monitor's print-out), which has a valid length of 1 to m. If the length exceeds m, the least-significant digits are valid.
2 : _____ (underline) : Indicates an input by an operator.
3 : [ ] : The parameter may be omitted.
4 : # : Indicates a hexadecimal number in assembler language.

M58563S, M58563S-1

Alternative Designation 1702A

2048-BIT (256-WORD BY 8-BIT OR 512-WORD BY 4-BIT) ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM

DESCRIPTION

The M58563S are FAMOS (floating-gate avalanche-injection MOS) ultraviolet-light erasable and electrically reprogrammable 2048-bit ROMs. They incorporate P-channel silicon-gate MOS technology, are designed for microcomputer system applications, and have direct TTL compatibility for all inputs and outputs, without extra interface circuits.

Static circuity is adopted and the device is interchangeable with Intel's 1702A.

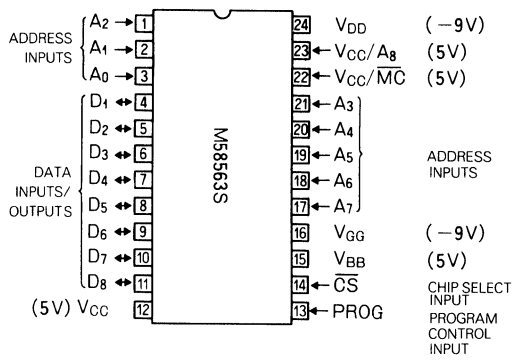
FEATURES

- Full-decoded 256-word by 8-bit organization; 512-word by 4-bit organization is also available for reading.
- Easy memory expansion by chip-select ($\overline{CS}$) input.
- All inputs and outputs are directly TTL-compatible and have OR-tie capability. All outputs are 3-state.
- Access time:
  M58563S: 1μs (max)
  M58563S-1: 1.5μs (max)
- No clocks required; the circuitry is entirely static.
- Interchangeable with Intel's 1702A.

APPLICATION

- Computers and peripheral equipment

PIN CONFIGURATION (TOP VIEW)



Outline 24S10

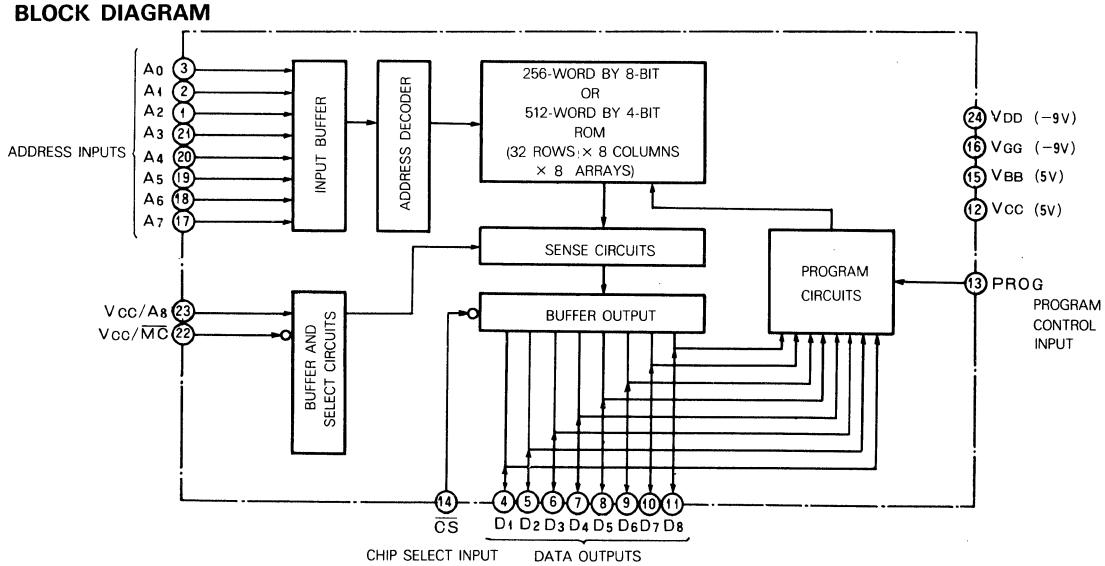
FUNCTION

In the 256-word by 8-bit organization mode, V_{CC} to pins 22 ($V_{CC}/\overline{MC}$) and 23 (V_{CC}/A_8), low-level input to the chip-enable terminal $\overline{CS}$ and address signals to the address inputs (A_0~A_7) make the data contents of the designated address location available at the data outputs (D_1~D_8). Applying low-level input to pin 22, using pin 23 as an address input, and connecting the output terminals in pairs (D_1, D_2), (D_3, D_4), (D_5, D_6) and (D_7, D_8), gives the 512-word by 4-bit organization. In this case, if V_{CC}/A_8 is kept at low level, the contents of D_1, D_3, D_5, and D_7 are available at the data-output terminals. If V_{CC}/A_8 is kept at high level, the contents of D_2, D_4, D_6, D_8 are available at the data-output terminals.

Programming is performed individually at any bit location, by applying input patterns to D_1~D_8 at the specified timing, address inputs to A_0~A_7 and the program-control signal to terminal PROG.

6

BLOCK DIAGRAM



M58563S, M58563S-1

Alternative Designation 1702A

2048-BIT (256-WORD BY 8-BIT OR 512-WORD BY 4-BIT) ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM

ABSOLUTE MAXIMUM RATINGS Note 1

Symbol	Parameter	Conditions	Limits	Unit
V_{I1}	Input voltage, read input	With respect to V_{CC} (substrate)	0.3～−20	V
V_{I2}	Input voltage, write input		0.3～−48	V
Topr	Operating free-air temperature		0～70	°C
Tstg	Storage temperature		−65～125	°C

Note 1 : Stresses above those listed above may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or at any other conditions above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods affects device reliability.

READ OPERATION

Recommended Operating Conditions (Ta = 0～70°C , unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Nom	Max	
V_{DD}	Supply voltage		−8.55	−9.0	−9.45	V
V_{GG}	Supply voltage		−8.55	−9.0	−9.45	V
V_{CC}	Supply voltage		4.75	5.0	5.25	V
V_{BB}	Supply voltage (Note 2)		4.75	5.0	5.25	V
V_{IL1}	Low-level input voltage, for TTL interface		−1.0		0.65	V
V_{IL2}	Low-level input voltage, for MOS interface		V_{DD}		$V_{CC}-6$	V
V_{IH}	High-level input voltage		$V_{CC}-2$		$V_{CC}+0.3$	V

Note 2 : V_{BB} should be connected to the same power supply as V_{CC}.

Electrical Characteristics ($Ta = 0～70°C$, $V_{CC} = 5V \pm 5\%$, $V_{DD} = -9V \pm 5\%$, $V_{GG} = -9V \pm 5\%$, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
I_{IL}	Low-level input current, address, chip-select input		$V_{IL} = 0V$			1	μA
I_{OZ}	Off-state output current		$V_{IL} = 0V$, $\overline{CS} = V_{CC}-2V$			1	μA
I_{DD0}	V_{DD} supply current	M58563S	$V_{GG} = V_{CC}$, $\overline{CS} = V_{CC}-2V$		2.4	6	mA
		M58563S-1	$I_{OL} = 0mA$, $Ta = 25°C$		2.0	5	mA
I_{DD1}	V_{DD} supply current	M58563S	$\overline{CS} = V_{CC}-2V$		24	42	mA
		M58563S-1	$I_{OL} = 0mA$, $Ta = 25°C$		20	35	mA
I_{DD2}	V_{DD} supply current	M58563S	$\overline{CS} = 0V$, $I_{OL} = 0mA$, $Ta = 25°C$		15	30	mA
		M58563S-1			12.5	25	mA
I_{DD3}	V_{DD} supply current	M58563S	$\overline{CS} = V_{CC}-2V$, $I_{OL} = 0mA$, $Ta = 0°C$		30		mA
		M58563S-1			25		mA
I_{OS1}	Output clamp current	M58563S	$V_O = -1.0V$, $Ta = 0°C$		6		mA
		M58563S-1			5		mA
I_{OS2}	Output clamp current	M58563S	$V_O = -1.0V$, $Ta = 25°C$		4.8	9.6	mA
		M58563S-1			4	8	mA
I_{GG}	V_{GG} supply current					1	μA
I_{OL}	Low-level output current		$V_O = 0.45V$	1.6	4		mA
I_{OH}	High-level output current		$V_O = 0V$	−2			mA
V_{OL}	Low-level output voltage		$I_{OL} = 1.6mA$		−3	0.45	V
V_{OH}	High-level output voltage		$I_{OH} = -100\mu A$	3.5	4.5		V
C_i	Input capacitance		f = 1MHz		8	10	pF
C_i (V_{GG})	Input capacitance, V_{GG} input					30	pF
C_o	Output capacitance				10	15	pF

2048-BIT (256-WORD BY 8-BIT OR 512-WORD BY 4-BIT) ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM

Timing Requirements ($Ta = 0 \sim 70°C$, $V_{CC} = 5V \pm 5\%$, $V_{DD} = -9V \pm 5\%$, $V_{GG} = -9V \pm 5\%$, unless otherwise noted)

Symbol	Parameter		Conditions	Limits			Unit
				Min	Typ	Max	
f_r	Repetition frequency	M58563S				1.0	MHz
		M58563S-1				0.66	MHz
$t_{su(AD-CS)}$	Address setup time with respect to chip select	M58563S				100	ns
		M58563S-1				600	ns
$t_{su(AD-VGG)}$	Address setup time with respect to clocked V_{GG} (Note 1)			1			μs

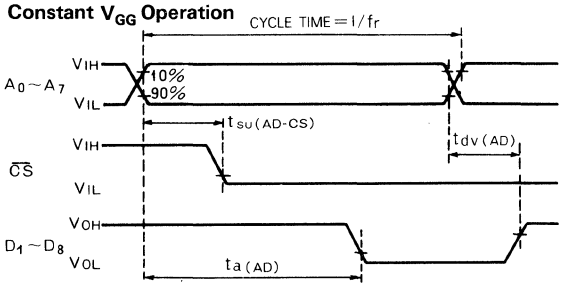
Switching Characteristics ($Ta = 0 \sim 70°C$, $V_{CC} = 5V \pm 5\%$, $V_{DD} = -9V \pm 5\%$, $V_{GG} = -9V \pm 5\%$, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
$t_{a(AD)}$	Address access time	M58563S				1	μs
		M58563S-1				1.5	μs
$t_{dv(AD)}$	Data valid time with respect to address					100	ns
$t_{a(CS)}$	Chip select access time		$V_{IH} = 4V$, $V_{IL} = 0V$			900	ns
$t_{dv(CSLH)}$	Data valid time with respect to chip select low-to high-level		t_r, $t_f \leqq 50ns$			300	ns
$t_{a(\overline{MC})}$	Mode change access time		Output load 50pF			400	ns
$t_{a(A8)}$	Address A_8 access time					600	ns
$t_{dv(VGGLH)}$	Data valid time with respect to clocked V_{GG} low-to-high-level (Note 1)					5	μs

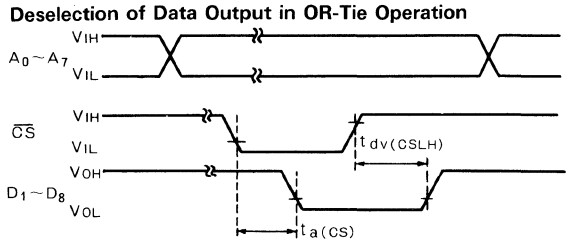
Note 1 : Power-down option.

Timing Diagrams

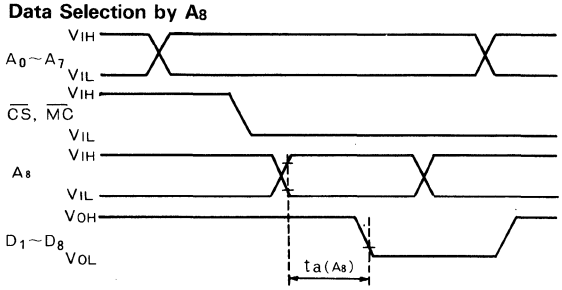
Constant V_{GG} Operation



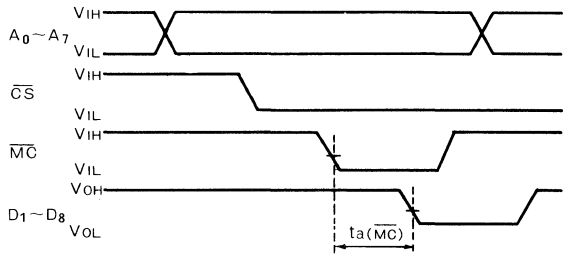
Deselection of Data Output in OR-Tie Operation



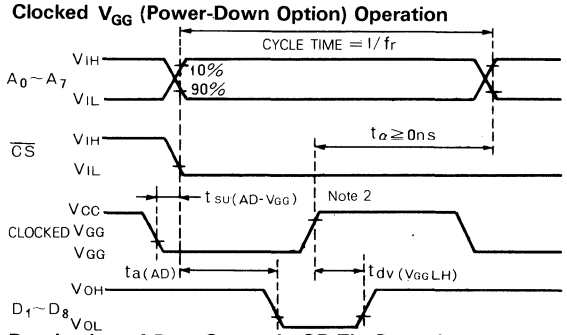
Data Selection by A_8



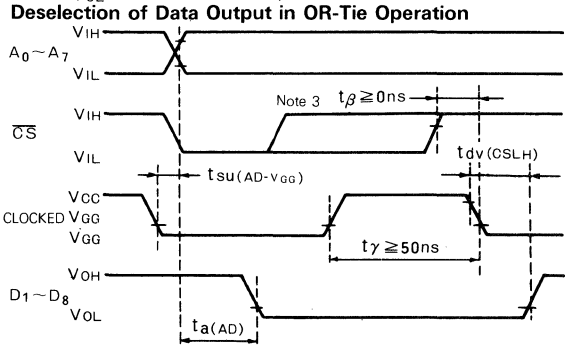
Data Selection by $\overline{MC}$



Clocked V_{GG} (Power-Down Option) Operation



Deselection of Data Output in OR-Tie Operation



Note 2 : The output will be retained for $t_{dv(VGGLH)}$ even if clocked V_{GG} is at V_{CC} level.

3 : If $\overline{CS}$ makes a transition from V_{IL} to V_{IH} while clocked V_{GG} is at V_{GG} level, then deselection of output occurs at $t_{dv(CSLH)}$

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M58563S, M58563S-1

Alternative Designation 1702A

2048-BIT (256-WORD BY 8-BIT OR 512-WORD BY 4-BIT) ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM

PROGRAM OPERATION

Recommended Operating Conditions ($T_a = 25°C$, $V_{CC} = 0V$, $V_{BB} = 12V \pm 10\%$, $V_{CC}/\overline{M_C} = V_{CC}/A_8 = \overline{CS} = 0V$, unless otherwise noted)

Symbol	Prameter	Limits			Unit
		Min	Nom	Max	
$V_{IH(P)}$	High-level input voltage			0.3	V
$V_{IL1(P)}$	Low-level input voltage, data input	−46		−48	V
$V_{IL2(P)}$	Low-level input voltage, address input	−25		−48	V
$V_{IL3(P)}$	Low-level input voltage, V_{DD}, program input	−46		−48	V
$V_{IL4(P)}$	Low-level input voltage, V_{GG} input	−30		−40	V

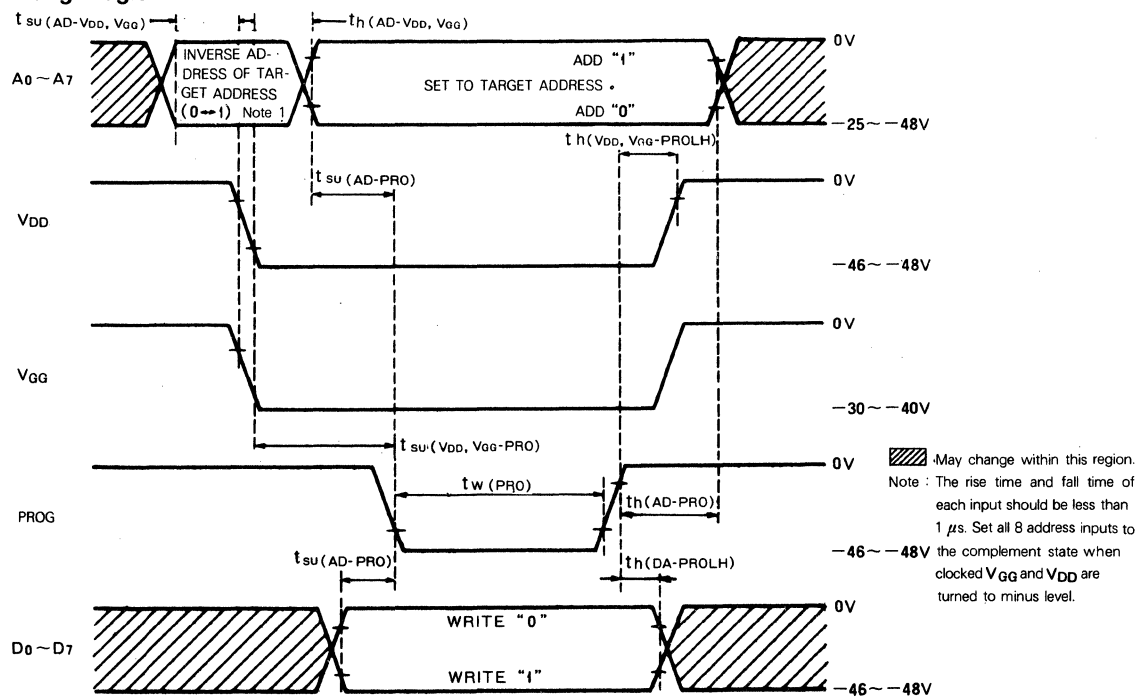
Electrical Characteristics ($T_a = 25°C$, $V_{CC} = 0V$, $V_{BB} = 12V \pm 10\%$, $V_{CC}/\overline{MC} = V_{CC}/A_8 = \overline{CS} = 0V$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$I_{IL1(P)}$	Low-level input current, address, data input	$\|V_{IL}\| \leqq 48V$			10	mA
$I_{IL2(P)}$	Low-level input current, program, V_{GG} input	$\|V_{IL}\| \leqq 48V$			10	mA
$I_{BB(P)}$	Supply current, V_{BB} input			0.5		mA
$I_{DDM(P)}$	Supply current, V_{DD} peak maximum current	$V_{GG} = -35V$, $V_{DD} = V_{IL2(P)} = -48V$		200		mA

Timing Requirements ($T_a = 25°C$, $V_{BB} = 12V \pm 10\%$, $\overline{CS} = V_{CC}/\overline{MC} = V_{CC}/A_8 = 0V$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
	Duty cycle V_{GG}, V_{DD}				20	%
$t_{w(PRO)}$	Programming pulse width	$V_{DD} = V_{IL3(P)} = -48V$, $V_{GG} = -35V$		1	3	ms
$t_{su(DA\text{-}PRO)}$	Data setup time with respect to program		25			μs
$t_{h(DA\text{-}PROLH)}$	Data hold time w/ respect to program low-to-high-level		10			μs
$t_{su(V_{DD},V_{GG}\text{-}PRO)}$	V_{DD}, V_{GG} setup time with respect to program		100			μs
$t_{h(V_{DD},V_{GG}\text{-}PROLH)}$	V_{DD}, V_{GG} time w/ respect to program low-to-high-level		10		100	μs
$t_{su(AD\text{-}V_{DD},V_{GG})}$	Address setup time with respect to V_{DD}, V_{GG}		25			μs
$t_{h(AD\text{-}V_{DD},V_{GG})}$	Address hold time with respect to V_{DD}, V_{GG}		25			μs
$t_{su(AD\text{-}PRO)}$	Address setup time with respect to program		10			μs
$t_{h(AD\text{-}PRO)}$	Address hold time with respect to program		10			μs

Timing Diagram



PROGRAMMING PROCEDURE

Before programming, find the number of pulses that are necessary to complete programming, verifying the output after application of a single programming pulse.

To program, apply 3 to 5 times this number of programming pulses.

ERASING PROCEDURE

The M58563S/S-1 can be erased by exposure to high-intensity short-wave ultraviolet rays at a wave length of 2537Å through the transparent quartz lid provided.

The recommended exposure is approximately 5Ws/cm^2. Mitsubishi Electric's Model GL-10 short-wave ultraviolet sterilizing lamp can erase either device in 10 to 20 minutes at a distance of 2cm. If the energy of the lamp used is unknown, find the total time (t_E) required to erase all bits and use a short-wave ultraviolet light exposure time of 4 to 6 times this value.

HANDLING PRECAUTIONS FOR FAMOS DEVICES

In addition to general handling precautions for MOS devices, the following points apply to FAMOS devices.

1. When programming, the programming voltage and duty cycle should be carefully held within the specified values. Exceeding the voltage and duty cycle may result in thermal destruction of the device.
2. Before erasing, clean the surface of the quartz lid to completely remove oily impurities, which may impede irradiation and affect the erasing characteristics. Also, scratches on the lid surface may act as refractors, and prevent erasing of some bits.
3. The electrical characteristics may be slightly affected by light entering through the transparent lid. Although in normal operation the programmed information would probably not be erased, to assure reliability it is desirable to cover the lid with opaque tape. Also, avoid programming in a brightly lit location.

M58651S

Alternative Designation 2401

4096-BIT (1024-WORD BY 4-BIT) ELECTRICALLY ALTERABLE ROM

DESCRIPTION

The M58651S is a fully decoded electrically erasable and reprogrammable ROM organized as 1024 words of 4 bits. This ROM is fabricated using P-channel MNOS technology. Data is stored by selectively applying negative writing pulses that tunnel electrons through the gate insulation onto the SiO_2-Si_3N_4 interface of the MNOS memory transistors. Data is erased by applying a negative pulse to the erase substrate of the device.

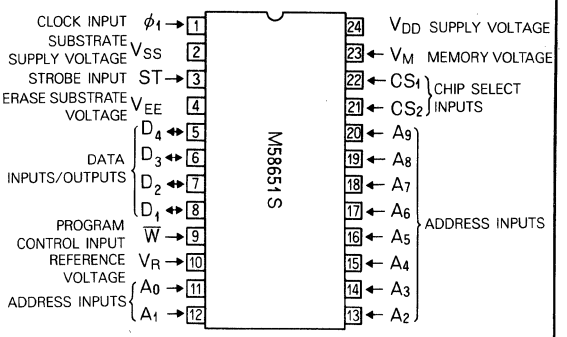
FEATURES

- Fully decoded memory with 1024 words of 4 bits
- Two chip select inputs for easy memory expansion
- Electrically reprogrammable: 10^6 times (min)
- Access time: 3μs (max)
- Program time: 20ms/4 bits
- Simultaneous erasure of all data: 100ms
- Minimum data retention: 2×10^{11} read accesses per word (min) between refreshing
- Power-off nonvolatile data storage life: 10 years (min)
- Three-state outputs
- Interchangeable with NCR's 2401 in pin connections and electrical characteristics

APPLICATION

- Read-only memories which require frequent and quick reprogramming, such as prototypes or field programmed microcomputer systems

PIN CONFIGURATION (TOP VIEW)



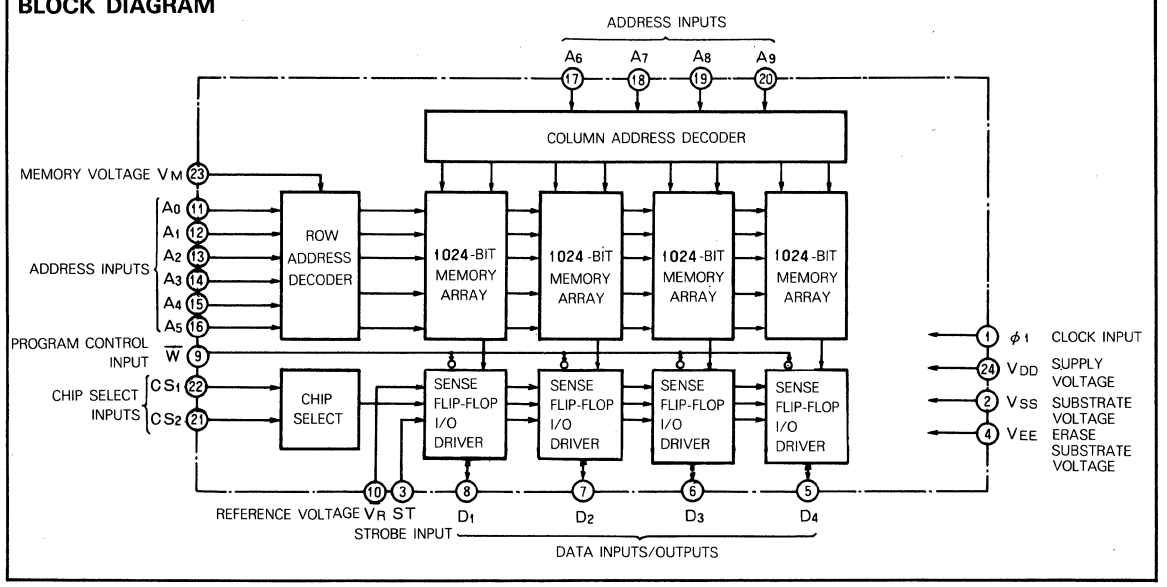
Outline 24S1

FUNCTION

The following voltages should be applied to each terminal for erase, program or read operations of memory. (V_{SS} = 0V is applicable.)

Symbol	Parameter	Erase mode	Program mode	Read mode
V_{DD}	Supply voltage	V_{SS}	V_{SS}-28V	V_{SS}−19V
V_{SS}	Substrate supply voltage	5 V	5 V	5 V
V_M	Memory voltage	V_{SS}	V_{DD}	V_{SS}−10V
V_R	Reference voltage	V_{SS}	V_{SS}	V_{DD}
V_{EE}	Erase substrate voltage	V_{SS}−28V	V_{SS}	V_{SS}
$\overline{W}$	Program control input	V_{SS}−28V	V_{DD}	V_{SS}

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

4096-BIT (1024-WORD BY 4-BIT) ELECTRICALLY ALTERABLE ROM

FUNCTIONAL OPERATIONS

Erasing

Data is erased by applying a $V_{SS}-28V$ 100ms pulse to the erase substrate voltage V_{EE}. All bits are electrically erased simultaneously.

Programming

Apply a low-level input to the program control terminal $\overline{W}$, and V_{DD} voltage to the memory voltage terminal V_M. Data is stored by selectively applying program pulses as designated by the address signals $A_0 \sim A_9$. At this time from 100 to 300 pulses of approximately 100μs pulse width should be applied to the clock ϕ_1 input.

Data is stored, theoretically, by selectively applying negative programming pulses that tunnel electrons through the gate insulation onto the SiO_2-Si_3N_4 interface of the MNOS memory transistors.

When the programming voltage is removed, the charge trapped on the interface has changed the state from 0 to 1 (a '1' is stored).

Data to be programmed is supplied through input terminals $D_1 \sim D_4$.

The programming time is 20ms/4 bits. With pull-up resistors, address inputs $A_0 \sim A_9$ and data inputs $D_1 \sim D_4$ are TTL-compatible.

Read Operation

Data is read selectively by applying a $V_{SS}-10V$ to the memory voltage terminal V_M from the input/output terminals $D_1 \sim D_4$ (operating now as output terminals.) Two modes can be used for read operations. In the strobed mode, the strobe input is used to sample and hold the output data. In the nonstrobed mode, the strobe terminal should be maintained as $V_{SS}-24\pm1V$ throughout the entire read cycle.

The access time is less than 3μs in the nonstrobed mode.

Strobed data may be accessed a minimum of 2×10^{11} times without refreshing and is nonvolatile in excess of ten years in the power-off state and at an ambient temperature of 70°C.

Chip Select

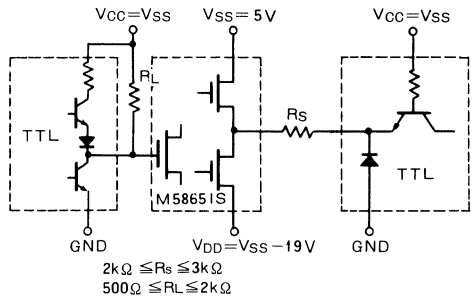
Both chip select inputs CS_1 and CS_2 must be at V_{SS} level to enable the data at the output terminals to be programmed into memory. These chip select inputs allow easy memory expansion, and with pull-up resistors are TTL-compatible.

Electrically Reprogrammable

Memory can be erased and rewritten up to 10^6 times.

INTERFACES

With TTL



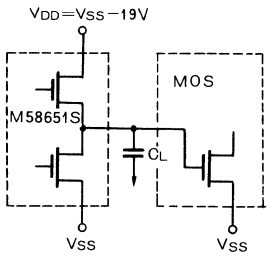
TTL-compatible terminals

Data input/output terminals ($D_1 \sim D_4$)

Address input terminals ($A_0 \sim A_9$)

Chip select input terminals (CS_1, CS_2)

With MOS



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M58651S

Alternative Designation 2401

4096-BIT (1024-WORD BY 4-BIT) ELECTRICALLY ALTERABLE ROM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{DD}	Supply voltage	With respect to V_{SS}	0.3～−30	V
V_M	Memory voltage		0.3～−30	V
V_R	Reference voltage		0.3～−30	V
V_{EE}	Erase substrate voltage		0.3～−30	V
V_I	Input voltage		0.3～−30	V
V_O	Output voltage		0.3～−30	V
Topr	Operating free-air temperature range		0～70	°C
Tstg	Storage temperature range		−65～150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0～70°C, unless otherwise noted)

Symbol	Parameter	Limits									Unit
		Erase mode			Program mode			Read mode			
		Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V_{DD}	Supply voltage	4.75	V_{SS}	$V_{SS}+0.3$	$V_{SS}-29$	$V_{SS}-28$	$V_{SS}-27$	$V_{SS}-20$	$V_{SS}-19$	$V_{SS}-18$	V
V_{SS}	Substrate supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V_M	Memory voltage		V_{SS}			V_{DD}		$V_{SS}-10.5$	$V_{SS}-10$	$V_{SS}-9.5$	V
V_R	Reference voltage		V_{SS}		V_{SS}	V_{SS}	V_{SS}		V_{DD}		V
V_{EEH}	High-level erase substrate voltage	$V_{SS}-0.4$	V_{SS}	$V_{SS}+0.3$	$V_{SS}-0.4$	V_{SS}	$V_{SS}+0.3$	$V_{SS}-0.4$	V_{SS}	$V_{SS}+0.3$	V
V_{EEL}	Low-level erase substrate voltage	$V_{SS}-29$	$V_{SS}-28$	$V_{SS}-27$	$V_{SS}-0.4$	V_{SS}	$V_{SS}+0.3$	$V_{SS}-0.4$	V_{SS}	$V_{SS}+0.3$	V
$V_{IH}(\overline{W})$	High-level program input voltage	$V_{SS}-29$	V_{SS}	$V_{SS}+0.3$	$V_{SS}-1.5$	V_{SS}	$V_{SS}+0.3$	$V_{SS}-1.5$	V_{SS}	$V_{SS}+0.3$	V
$V_{IL}(\overline{W})$	Low-level program input voltage	$V_{SS}-29$		$V_{SS}-4.4$	$V_{SS}-29$		$V_{SS}-4.4$	$V_{SS}-1.5$	V_{SS}	$V_{SS}+0.3$	V
$V_{IH}(\phi_I)$	High-level clock input voltage		V_{SS}		$V_{SS}-0.8$	V_{SS}	$V_{SS}+0.3$	$V_{SS}-0.8$	V_{SS}	$V_{SS}+0.3$	V
$V_{IL}(\phi_I)$	Low-level clock input voltage		V_{SS}			V_{DD}		$V_{SS}-25$	$V_{SS}-24$	$V_{SS}-23$	V
$V_{IH(ST)}$	High-level strobe input voltage		V_{SS}			V_{DD}		$V_{SS}-0.8$	V_{SS}	$V_{SS}+0.3$	V
$V_{IL(ST)}$	Low-level strobe input voltage		V_{SS}			V_{DD}		$V_{SS}-25$	$V_{SS}-24$	$V_{SS}-23$	V
$V_{IH(AD,CS)}$	High-level address, chip select input voltage		Don't care		$V_{SS}-1.5$	V_{SS}	$V_{SS}+0.3$	$V_{SS}-1.5$	V_{SS}	$V_{SS}+0.3$	V
$V_{IL(AD,CS)}$	Low-level address, chip select input voltage		Don't care		V_{DD}		$V_{SS}-4.4$	V_{DD}		$V_{SS}-4.4$	V
$V_{IH(DA)}$	High-level data input voltage		Don't care		$V_{SS}-1.5$	V_{SS}	$V_{SS}+0.3$				V
$V_{IL(DA)}$	Low-level data input voltage		Don't care		V_{DD}		$V_{SS}-4.4$				V

Note 1 : Can be used even when $V_{SS}=0V$

ELECTRICAL CHARACTERISTICS (Ta=0～70°C, V_{SS}=GND, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_I	Input leakage current (except pins 1,2,4,5,6,7,8,23,24)	$V_I=-15V(V_{I(\phi1)}=V_{DD}=-20V$, all other pins = GND)			−2	μA
$I_{I(\phi_I)}$	Clock input leakage current	$V_{I(\phi_I)}=-29V$ ($V_{DD}=-29V$, $V_{I(\overline{W})}=V_{I(ST)}=-25V$, all other pins = GND)			−200	μA
$I_{I(V_M)}$	Memory voltage leakage current	$V_{I(V_M)}=-29V$ ($V_{DD}=-29V$, $V_{I(\overline{W})}=V_{I(ST)}=-25V$, all other pins = GND)			−200	μA
I_O	Output leakage current	$V_O=-15V$ (chip deselected)			−10	μA
$I_{I(VEE)}$	Erase substrate leakage current	$V_{EE}=-28V$ ($V_{I(\overline{W})}=V_{I(ST)}=-25V$)			−1	mA
I_{DD1}	Supply current from V_{DD} (read mode)	$V_{DD}=-19V$ (no load)		−8.5	−12	mA
I_{DD2}	Supply current from V_{DD} (program mode)	$V_{DD}=-28V$ (no load)		−18	−25	mA
V_{OH}	High-level output voltage	C_L=100pF	$V_{SS}-1.5$			V
V_{OL}	Low-level output voltage	C_L=100pF			$V_{SS}-10$	V
t_S	Unpowered nonvolatile data storage time		10			year
$C_{i(AD,CS)}$	Address, chip select input capacitance			6	10	pF
$C_{i(W)}$	Program input capacitance			10	20	pF
$C_{i(ST)}$	Strobe input capacitance			10	15	pF
$C_{i(\phi_I)}$	Clock input capacitance			40	50	pF
$C_{i(VEE)}$	Erase substrate input capacitance			600	700	pF
$C_{i/o(DA)}$	Data input/output capacitance			6	10	pF

Note 2 : Current flowing into an IC is positive; out is negative.

3 : Characteristics are shown at MOS load.

4096-BIT (1024-WORD BY 4-BIT) ELECTRICALLY ALTERABLE ROM

TIMING REQUIREMENTS

For Erase (Ta = 0 ~ 70°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{w(V_{EE})}$	VEE erase pulse width		100		1,000	ms
t_r	VEE rise time		0.01		1.0	ms
t_f	VEE fall time		0.01		1.0	μs
$t_{h(V_{EE}-\overline{W})}$	Erase pulse hold time with respect to program		10			μs
$t_{su(V_{EE}-\overline{W})}$	Erase pulse setup time with respect to program		10			μs

For Programming (Ta = 0 ~ 70°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$N_{\phi W}$	Number of one word programming clock pulses	$t_{W(\phi 1)}$ = 100μs ±10%, 5μs min dead interval	100	200	300	pulses
$t_{h(\phi 1-\overline{W})}$	Clock $\phi 1$ hold time with respect to program		1,000			ns
$t_{h(\phi 1-AD,CS)}$	Clock $\phi 1$ hold time with respect to address, chip select		1,000			ns
$t_{su(\phi 1-AD,CS)}$	Clock $\phi 1$ setup time with respect to address, chip select		0			μs
$t_{su(DA-\phi 1)}$	Data input setup time with respect to clock $\phi 1$		0			μs
$t_{h(DA-\phi 1)}$	Data input hold time with respect to clock $\phi 1$		0			μs

Read Cycle, For Nonstrobed Operation (Ta = 0 ~ 70°C, $V_{I(ST)}$ = V_{SS} −24 ±1 V, unless otherwise noted)

Symbol	Prameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{w(\phi 1)}$	Clock $\phi 1$ pulse width	$t_{r(\phi 1)}$, $t_{f(\phi 1)}$ ≦ 50ns	850		2,000	ns
$t_{h(\phi 1-AD)}$	Clock $\phi 1$ hold time with respect to address		400			ns
$t_{h(AD-\phi 1)}$	Address hold time with respect to clock $\phi 1$		0			μs

Read Cycle, For Strobed Operation (Ta = 0 ~ 70°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{w(\phi 1)}$	Clock $\phi 1$ pulse width	$t_{r(\phi 1)}$, $t_{f(\phi 1)}$ ≦ 50ns	850		2,000	ns
$t_{h(\phi 1-AD)}$	Clock $\phi 1$ hold time with respect to address		400			ns
$t_{h(ST-\phi 1)}$	Stobe hold time with respect to clock $\phi 1$		1.5			μs
$t_{w(ST)}$	Strobe pulse width	$t_{r(ST)}$, $t_{f(ST)}$ ≦ 50ns	850			ns

SWITCHING CHARACTERISTICS

For Erasing and Programming (Ta = 0 ~ 70°C unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
N_W	Number of times word may be rewritten				10^6	times

Read Cycle For Nonstrobed Operation (Ta = 0 ~ 70°C, $V_{I(ST)}$ = V_{SS} −24 ±1 V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{a(AD)}$	Address access time				3	μs
$t_{a(\phi 1)}$	Clock $\phi 1$ access time				1,750	ns
$t_{dv(\phi 1HL)}$	Data valid time with respect to clock $\phi 1$ high-to-low-level input				300	ns
N_{RA}	Number of read accesses per word between refreshings		2×10^{11}			times

Read Cycle For Strobed Operation (Ta = 0 ~ 70°C, unless otherwise noted)

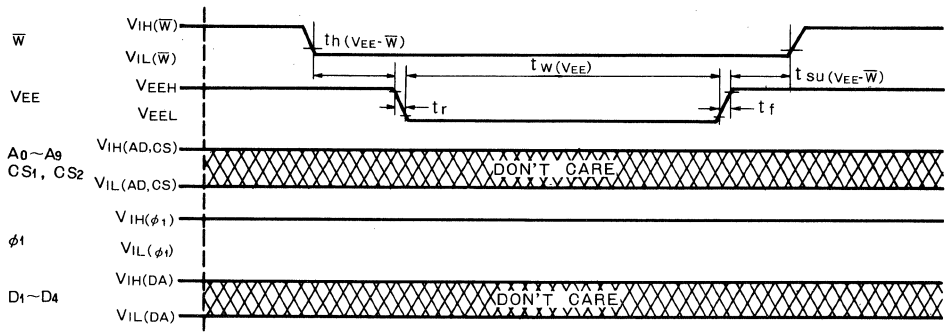
Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
$t_{a(ST)}$	Strobe access time			2.25	μs
$t_{dv(STHL)}$	Data valid time with respect to strobe high-to-low-level input			300	ns
N_{RA}	Number of read accesses per word between refreshings	2×10^{11}			times

6

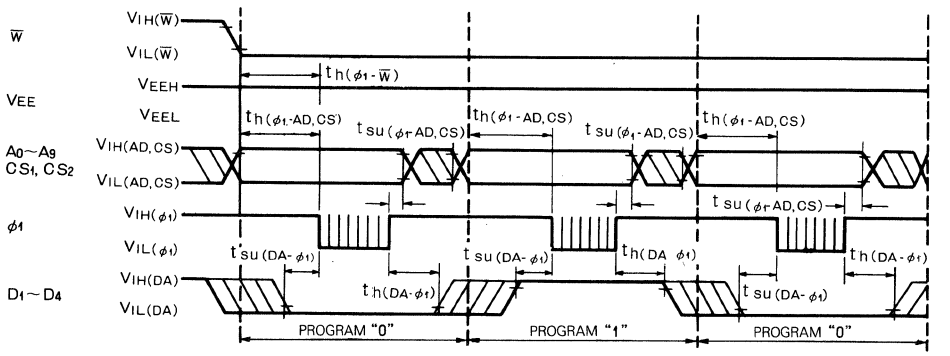
4096-BIT (1024-WORD BY 4-BIT) ELECTRICALLY ALTERABLE ROM

TIMING DIAGRAMS

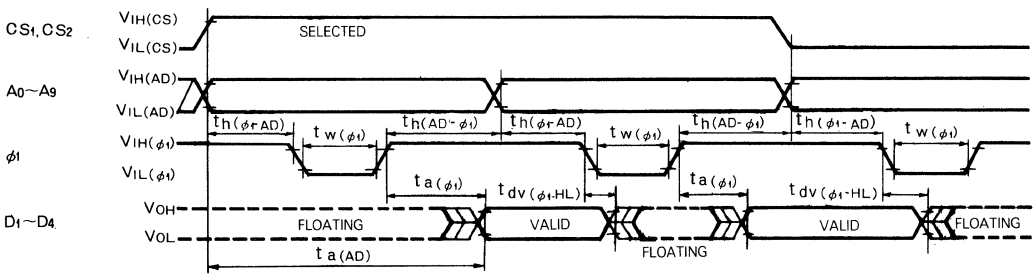
Erasing



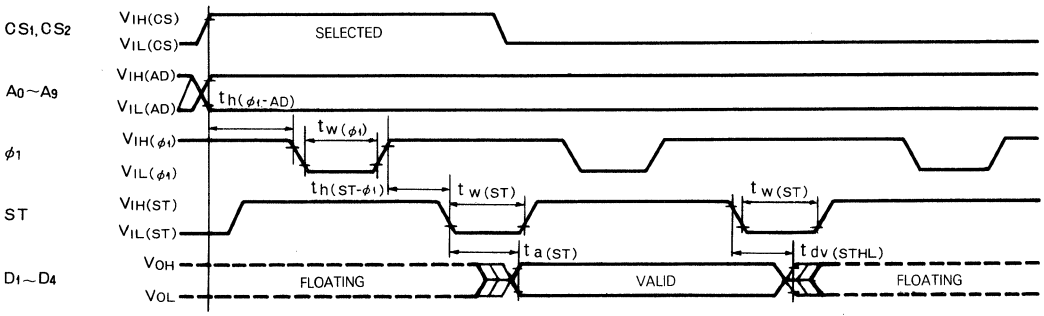
Programming



Read Cycle for Nonstrobed Operation



Read Cycle for Strobed Operation



MITSUBISHI ELECTRIC

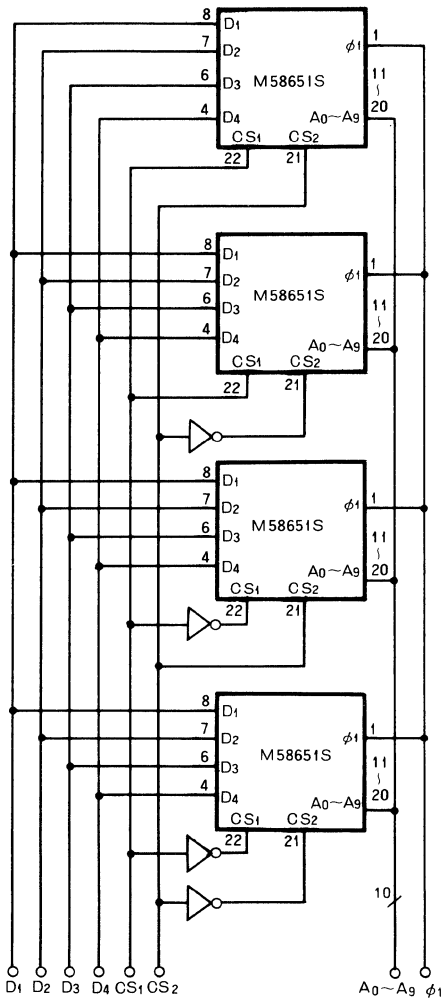
4096-BIT (1024-WORD BY 4-BIT) ELECTRICALLY ALTERABLE ROM

APPLICATION

Chip Select Circuit

Both chip selects CS_1 and CS_2 must be low to keep the data outputs $D_1 \sim D_4$ in the floating (high-impedance) state. These chip select inputs allow easy memory expansion. An example of a multichip memory with 4096 words of 4 bits is shown below.

Fig. 1 Expansion of number of words



M54700K, M54700P, M54700S

Alternative Designation 6300

1024-BIT (256-WORD BY 4-BIT) FIELD PROGRAMMABLE ROM

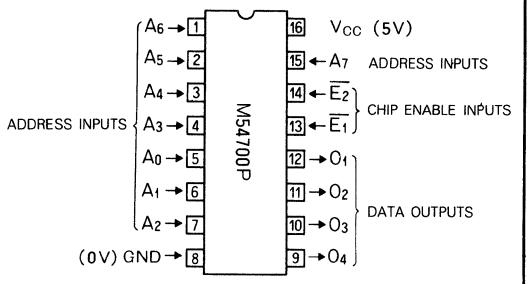
DESCRIPTION

The memory cells of the M54700K, P, S are a matrix of diodes and Ni-Cr fuse links. Data can be electrically programmed by open-circuiting fuse in the field with simple programming equipment. These 1024-bit field programmable ROMs (PROMs) are composed of an address decoder, memory, output and chip enable TTL circuits.

FEATURES

- Field programmable ROM
- Low power dissipation: 0.40mW/bit
- Fast access time: 50ns (typ)
- 5V±5% single supply voltage
- Inputs and outputs TTL-compaticle
- Open collector outputs
- Two chip enable inputs ($\overline{E_1}$, $\overline{E_2}$) for easy memory expansion
- Organized as 256 words of 4 bits
- 16-pin ceramic or plastic package
- Interchangeable with MMI's 6300 in pin configuration and electrical characteristics

PIN CONFIGURATION (TOP VIEW)



Outline 16K1 (M54700K)
16P1 (M54700P)
16S1 (M54700S)

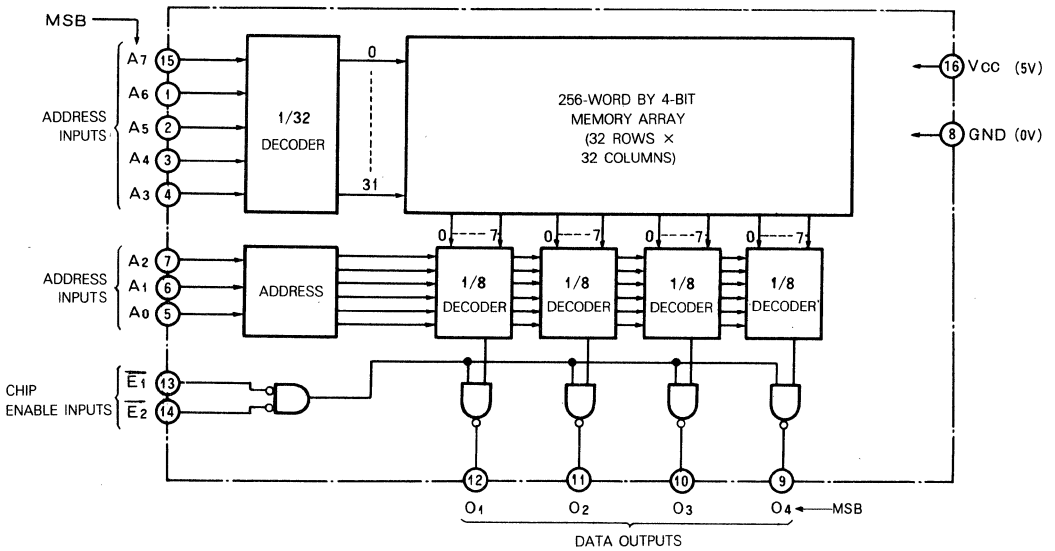
APPLICATION

- Programmable memory for the M58710S 8-bit parallel CPU. Used for prototype design, microprogramming and control storage.

FUNCTION

The diode matrices of these 1024-bit ROMs are organized as 256 words of 4 bits. Their memories are accessed by address inputs A_0~A_7, selecting one of 256 words. The 4 bits are read out in parallel on data outputs 0_1~0_4. All inputs are TTL-compatible. An external decoder is not necessary. All outputs are open-collector outputs, so it is possible to AND-tie them to other ROMs and TTL devices. The AND-tie fanout of each output can accommodate up to 10 standard TTL loads. The chip enables $\overline{E_1}$ and $\overline{E_2}$ are used to inhibit data outputs O_1~O_4.

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

1024-BIT (256-WORD BY 4-BIT) FIELD PROGRAMMABLE ROM

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		7	V
V_I	Input voltage		5.5	V
V_O	Output voltage		V_{CC}	V
Topr	Operating free-air temperature		0~75	°C
Tstg	Storage temperature		−55~125	°C
V_O	Output apply voltage	In case of programming	27	V
V_E	Chip enable apply voltage		35	V
$t_{w(P)}/t_{c(P)}$	Duty cycle		25	%

READ OPERATION

Recommended Operating Conditions (Ta = 0~75°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5	5.25	V

Electrical Characteristics (Ta = 0~75°C, unless otherwise noted)

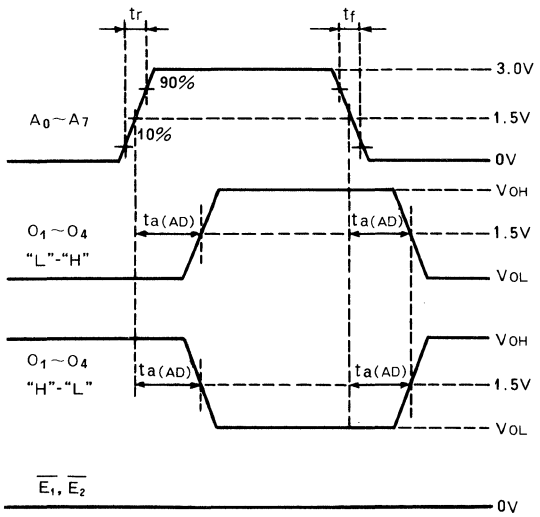
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ(Note1)	Max	
V_{OL}	Low-level output voltage	I_{OL} = 16mA		0.3	0.45	V
I_{OH}	High-level output voltage	V_{OH} = 5.25V			100	μA
I_{IL}	Low-level input current	V_I = 0.4V			−1.6	mA
I_{IH}	High-level input current	V_I = 2.4V			40	μA
		V_I = 4.5V			60	
I_{CC}	Supply current from V_{CC}			85	125	mA
V_{IC}	Input clamped voltage	I_I = −10mA			−1.5	V

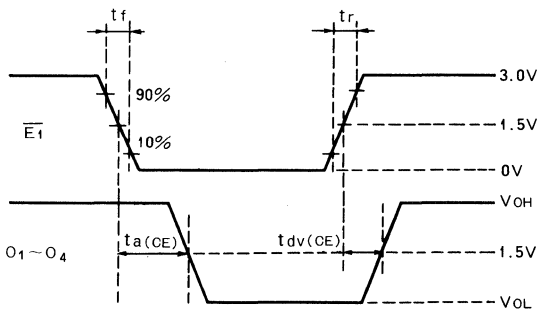
Note 1 : Typical values are at V_{CC} = 5V, Ta = 25°C

Switching Characteristics (V_{CC} = 5V, Ta = 25°C, unless otherwise noted)

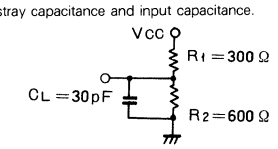
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{a(AD)}$	Address access time (Note 3)	See Timing Diagrams and Note 4			60	ns
$t_{a(CE)}$	Chip enable access time				35	ns
$t_{dv(CE)}$	Data valid time with respect to chip enable				35	ns

Timing Diagrams





Note 2 : Rise time $t_r \leqq 5ns$; fall time $t_f \leqq 5ns$
3 : The chip enable inputs $\overline{E_1}$ and $\overline{E_2}$ should be low-level at measurement time during address access time
4 : Load circuit: capacitance (C_L) includes stray capacitance and input capacitance.



6

1024-BIT (256-WORD BY 4-BIT) FIELD PROGRAMMABLE ROM

PROGRAMMING OPERATION

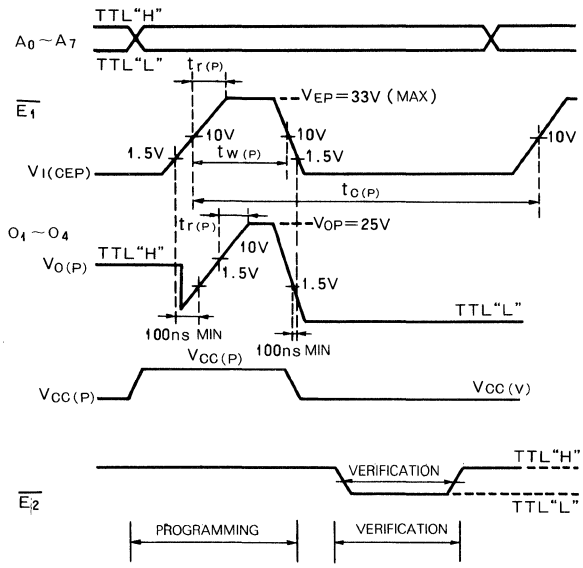
Recommended Operating Conditions

Symbol	Test conditions	Limits			Unit
		Min	Nom	Max	
$V_{I(CEP)}$	Chip enable program input voltage	29		33	V
$V_{O(P)}$	Output apply voltage			25	V
$V_{CC(P)}$	Program input voltage	5.40	5.50	5.60	V
$V_{CC(V)}$	Program verify input voltage	4.10	4.20	4.30	V

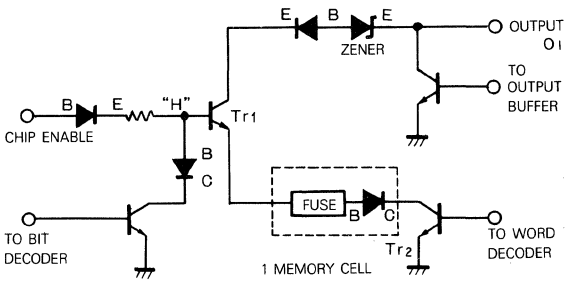
Timing Requirements

Symbol	Test conditions	Limits			Unit
		Min	Typ	Max	
$t_{r(P)}$	Pulse rise time	10	25	100	μs
$t_{w(P)}$	Pulse width	0.04		100	ms
$t_{w(P)}/t_{c(P)}$	Duty cycle			25	%

Timing Diagram



Programming Circuit



Programming (Writing) Procedure

All 1024 Ni-Cr fuse-link memory elements are manufactured in a high-logic-level (fuse closed) output conditon. To program:

1. Apply 5.5V to the supply voltage V_{CC} and select a fuse link to be programmed with address inputs A_0~A_7.
2. Apply a high-logic-level to the chip enable input $\overline{E_2}$.
3. After applying a program pulse $V_{I(CEP)}$ to the chip enable input $\overline{E_1}$ (see Timing Diagrams), apply an output pulse $V_{O(P)}$ to the fuse link of the output to be programmed. The output pulses should be separately applied to each output.
4. After programming, the fuse link is open and the output level is changed to a low-logic-level.
5. After programming is completed, apply an additional three programming pulses.
6. Test the programmed memory to verify that the outputs are low-level or high-level as desired. Both chip enable inputs $\overline{E_1}$ and $\overline{E_2}$ must be low-level for testing.

The word decoder circuit selects any one of 32 columns, and sets the transistor Tr_2 to the on state. The bit decoder circuit selects any four of 32 rows, and supplies the base current to transistor Tr_1 from chip enable input $\overline{E_1}$.

The fuse link is opened not by the base current, but by the collector current which is supplied to transistor Tr_1 from the selected output O_1~O_4, plus the base current. At this time, the other three fuse links of the selected word line are in a half-selected stage and the remaining 1020 fuse links are in a non-selected state.

Typical Programming Conditions

Condition sequence	Pulse sequence	Pulse width $t_{w(P)}$ (ms)	Chip enable program voltage $V_{I(CEP)}$ (V)	Output voltage (V)
1	1 ~ 4	0.5	29	25
2	5 ~ 8	1	29	25
3	9 ~ 12	5	30	25
4	13~19	20	33	25

1024-BIT (256-WORD BY 4-BIT) FIELD PROGRAMMABLE ROM

APPLICATIONS

Chip Enable Circuit

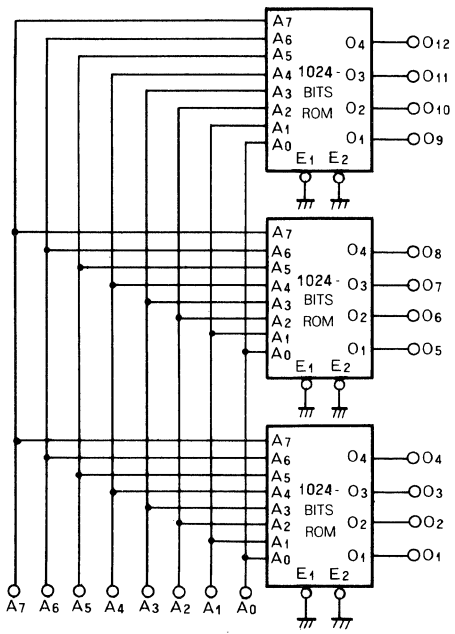
The chip enable inputs $\overline{E_1}$ and $\overline{E_2}$ are used for activating or inhibiting output O_1~O_4. $\overline{E_1}$ and $\overline{E_2}$ are NORed. Output is inhibited when any of the inputs are high-logic-level. Chip enable inputs $\overline{E_1}$ and $\overline{E_2}$ allow easy memory expansion by one of the following procedures:

1. Expanding the Number of Bits in a Word

For example, using three 1024-bit ROMs, each organized as 256 words of 4 bits, the number of bits in a word can be expanded as described below:

1. Apply a low-logic-level to both chip enable inputs $\overline{E_1}$ and $\overline{E_2}$ of each ROM.
2. Connect address inputs A_0~A_7 of each ROM in parallel. Memory is thus expanded and reorganized as 256 words of 12 bits.

Fig. 1 Expansion of number of bits

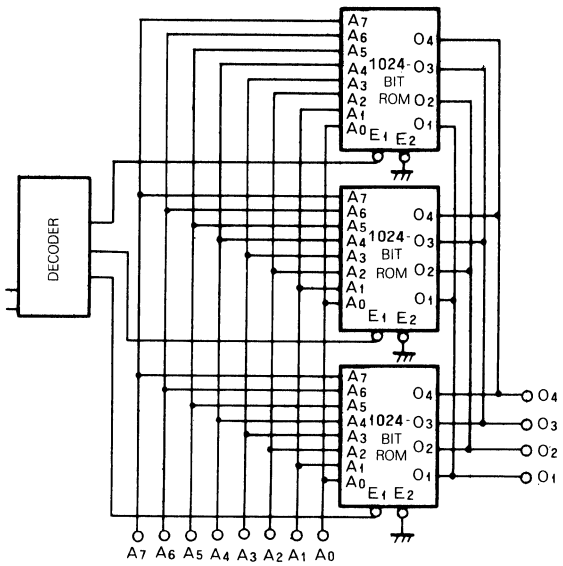


2. Expanding the Number of Words in Memory

For example, using three 1024-bit ROMs, each organized as 256 words of 4 bits, the number of words in memory can be expanded as described below:

1. Connect one of the chip enable inputs $\overline{E_1}$ or $\overline{E_2}$ of each ROM to the decoder while keeping the remaining input at low-logic-level.
2. Connect the outputs from each ROM with AND-tie connections so that each output is an open-collector output circuit or a three-state output. Memory is thus expanded and organized as 768 words of 4 bits.

Fig. 2 Expansion of number of words



3. Expanding the Number of Words in Memory and the Number of Bits in a Word

For example, using nine 1024-bit ROMs, each organized as 256 words of 4 bits, and by combining procedures 1 and 2 above, the number of words in memory along with the number of bits in a word, can be expanded as described below:

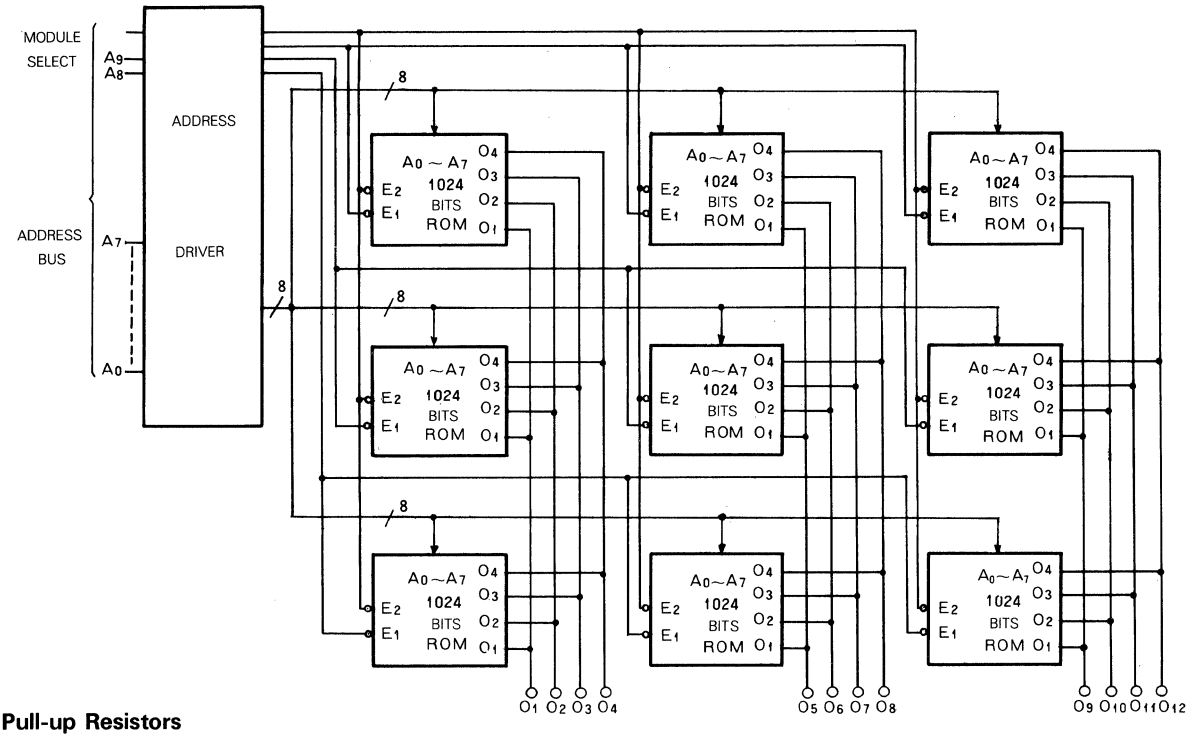
1. The chip enable input $\overline{E_2}$ of all ROMs is connected in parallel for module selection.
2. The chip enable input $\overline{E_1}$ activates selected ROMs the same as 2 above.

Memory is thus expanded and reorganized as 768 words of 12 bits.

6

1024-BIT (256-WORD BY 4-BIT) FIELD PROGRAMMABLE ROM

Fig. 3 ROM module



Pull-up Resistors

The outputs are open collectors; therefore, AND-tie connections are also possible, and normal loads can be connected. The resistance of a pull-up resistor R_L that may be connected between the voltage supply and the collectors of the output transistors should be determined by equations (1) and (2) as shown below:

$$R_L(max) = \frac{\overline{V_{CC}} - \underline{V_{OH}}}{M \cdot \overline{I_{OH}^*} + N \cdot \overline{I_{IH}}} \quad \text{----------(1)}$$

where, M : number of AND-ties
N : number of fanouts (number of loads)
$\overline{V_{CC}}$: maximum value of supply voltage
$\underline{V_{OH}}$: minimum value of high-level output voltage
$\overline{I_{OH}^*}$: maximum value of high-level output current at the open collector output
$\overline{I_{IH}}$: maximum value of high-level input current

$$R_L(min) = \frac{\underline{V_{CC}} - \overline{V_{OL}}}{\overline{I_{OL}} - N \cdot \overline{I_{IL}}} \quad \text{----------(2)}$$

where, $\underline{V_{CC}}$: minimum value of supply voltage
$\overline{V_{OL}}$: maximum value of low-level output voltage
$\overline{I_{OL}}$: maximum value of low-level output current
$\overline{I_{IL}}$: maximum value of low-level input current

then,

$$R_L(min) < R_L < R_L(max) \quad \text{----------(3)}$$

The resistance of a pull-up resistor R_L should be within the range as shown in equation (3). R_L (min) and R_L (max) should be calculated using the appropriate number of AND-ties and fanouts. Calculation examples of TTL load are shown below:

(1) When

$M = 4$, $N = 3$, $\overline{V_{CC}} = 5.25V$, $\underline{V_{OH}} = 2.4V$, $\overline{I_{OH}^*} = 100\mu A$, $\overline{I_{IH}} = 40\mu A$

$$R_L(max) = \frac{\overline{V_{CC}} - \underline{V_{OH}}}{M \cdot \overline{I_{OH}^*} + N \cdot \overline{I_{IH}}} = \frac{5.25V - 2.4V}{4 \times (100\mu A) + 3 \times (40\mu A)} = 5090\Omega$$

(2) When

$N = 3$, $\underline{V_{CC}} = 4.75V$, $\overline{V_{OL}} = 0.45V$, $\overline{I_{OL}} = 16mA$, $\overline{I_{IL}} = 1.6mA$

$$R_L(min) = \frac{\underline{V_{CC}} - \overline{V_{OL}}}{\overline{I_{OL}} - N \cdot \overline{I_{IL}}} = \frac{4.75V - 0.45V}{16mA - 3 \times (1.6mA)} = 384\Omega$$

M54730K, M54730P, M54730S

Alternative Designation 6330

256-BIT (32-WORD BY 8-BIT) FIELD PROGRAMMABLE ROM

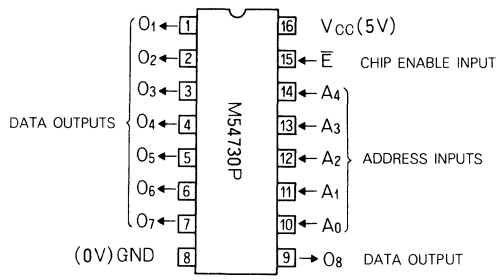
DESCRIPTION

The memory cells of the M54730K, P, S are a matrix of diodes and Ni-Cr fuse links. Data can be electrically programmed by open-circuiting fuse in the field with simple programming equipment. These 256-bit field programmable ROMs (PROMs) are composed of an address decoder, memory, output and chip enable TTL circuits.

FEATURES

- Field programmable ROM
- Low power dissipation: 1.5mW/bit
- Fast access time: 45ns (typ)
- 5V±5% single supply voltage
- Inputs and outputs TTL-compatible
- Open-collector outputs
- Chip enable inputs ($\overline{E}$) for easy memory expansion
- Organized as 32 words of 8 bits
- 16-pin ceramic or plastic package
- Interchangeable with MMI's 6300 in pin configuration and electrical characteristics

PIN CONFIGURATION (TOP VIEW)



Outline 16K1 (M54730K)
16P1 (M54730P)
16S1 (M54730S)

APPLICATION

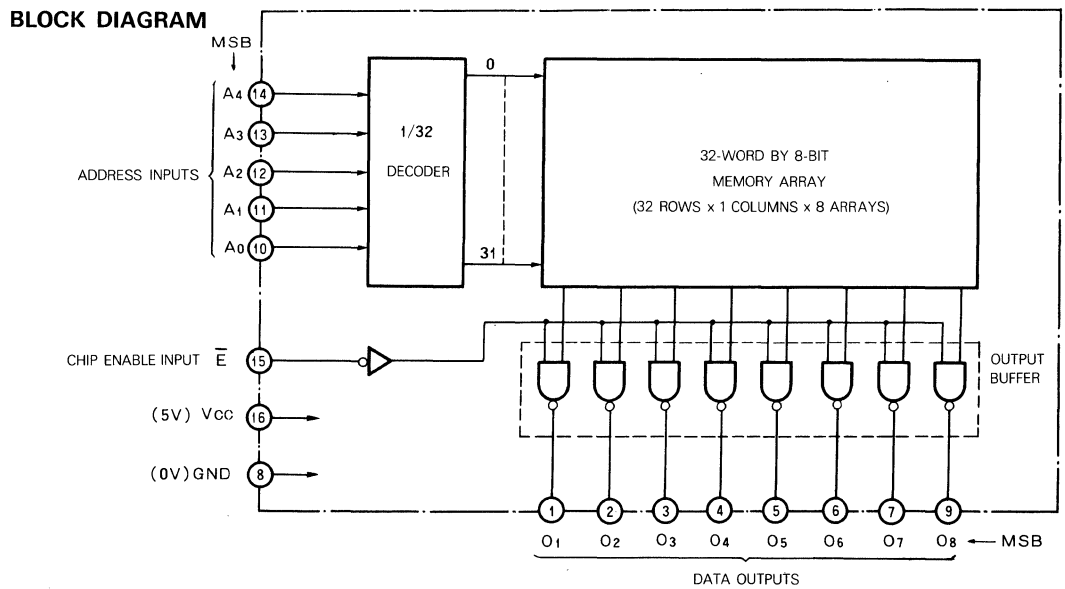
- Programmable memory for the M58710S 8-bit parallel CPU. Used for prototype design, microprogramming and control strage.

FUNCTION

The diode matrices of these 256-bit ROMs are organized as 32 words of 8 bits. Their memories are accessed by address inputs A_0~A_4, selecting one of 32 words.The 8 bits are read out in parallel on data outputs 0_1~0_8. All inputs are TTL-compatible. An external decoder is not necessary. All outputs are open-collector outputs, so it is possible to AND-tie them to other ROMs and TTL devices. The AND-tie fanout of each output can accommodate up to 10 standard TTL loads. The chip enable $\overline{E}$ is used to inhibit data ouputs O_1~O_8.

6

BLOCK DIAGRAM



M54730K, M54730P, M54730S

Alternative Designation 6330

256-BIT (32-WORD BY 8-BIT) FIELD PROGRAMMABLE ROM

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		7	V
V_I	Input voltage		5.5	V
V_O	Output voltage		V_{CC}	V
T_{opr}	Operating free-air temperature		0~75	°C
Tstg	Storage temperature		−55~125	°C
V_O	Output apply voltage	In case of programming	27	V
$t_{w(P)}/t_{c(P)}$	Duty cycle		25	%

READ OPERATION

Recommended Operating Conditions (Ta = 0~75°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5	5.25	V

Electrical Characteristics (Ta = 0~75°C unless otherwise noted)

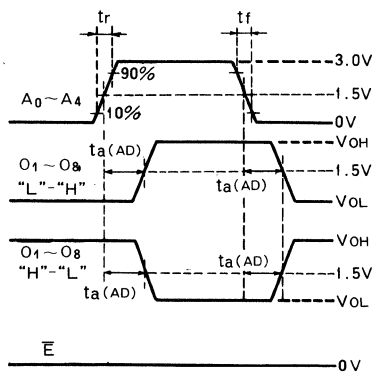
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ(Note1)	Max	
V_{OL}	Low-level output voltage	I_{OL} = 16mA		0.3	0.45	V
I_{OH}	High-level output voltage	V_{OH} = 5.25V			100	μA
I_{IL}	Low-level input current	V_I = 0.4V			−1.6	mA
I_{IH}	High-level input current	V_I = 2.4V			40	μA
		V_I = 4.5V			60	
I_{CC}	Supply current from V_{CC}			85	125	mA
V_{IC}	Input clamped voltage	I_I = −10mA			−1.5	V

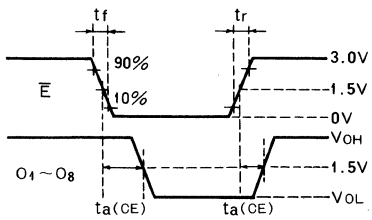
Note 1 : Typical values are at V_{CC} = 5V, Ta = 25°C

Switching Characteristics (V_{CC} = 5V, Ta = 25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{a(AD)}$	Address access time	See Timing Diagrams			50	ns
$t_{a(CE)}$	Chip enable access time				30	ns
$t_{dv(CE)}$	Data valid time with respect to chip enable				30	ns

Timing Diagrams

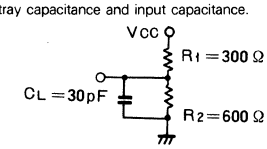




Note 2 : Rise time $t_r \leqq 5ns$; fall time $t_f \leqq 5ns$

3 : The chip enable input E should be low-level at measurement time during address access time

4 : Load circuit: capacitance (C_L) includes stray capacitance and input capacitance.



MITSUBISHI ELECTRIC

PROGRAMMING OPERATION

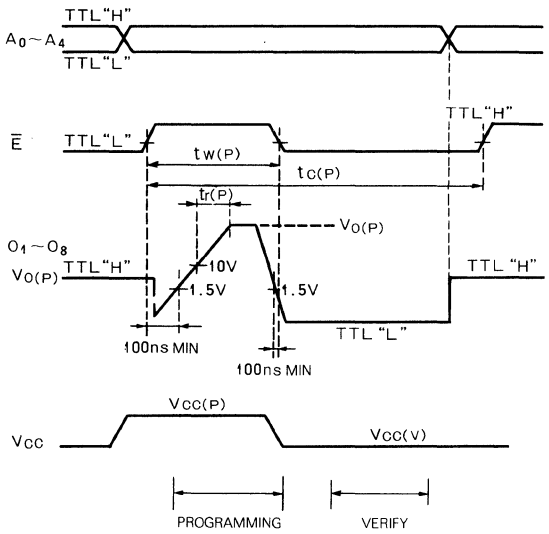
Recommended Operating Conditions

Symbol	Test conditions	Limits			Unit
		Min	Nom	Max	
$V_{I(CEP)}$	Chip enable program input voltage	29		33	V
$V_{O(P)}$	Output apply voltage	20		25	V
$V_{CC(P)}$	Program input voltage	5.40	5.50	5.60	V
$V_{CC(V)}$	Program verify input voltage	4.10	4.20	4.30	V

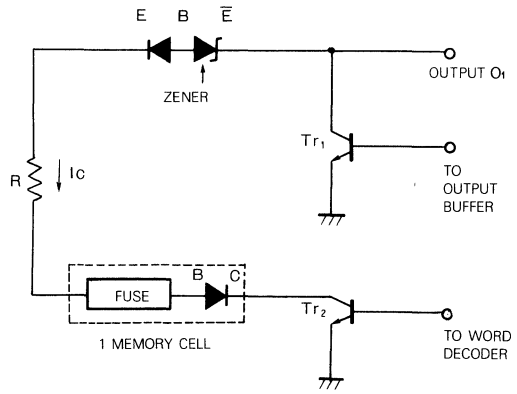
Timing Requirements

Symbol	Test conditions	Limits			Unit
		Min	Typ	Max	
$t_{r(P)}$	Pulse rise time	10	25	100	μs
$t_{w(P)}$	Pulse width	0.04		100	ms
$t_{w(P)}/t_{c(P)}$	Duty cycle			25	%

Timing Diagram



Programming Circuit



Programming (Writing) Procedure

All 256 Ni-Cr fuse-link memory elements are manufactured in a high-logic-level (fuse closed) output conditon. To program:

1. Apply 5.5V to the supply voltage V_{CC} and select a fuse link to be programmed with address inputs A_0~A_4.
2. Apply a high-logic-level to the chip enable input $\overline{E}$.
3. After applying a program pulse $V_{I(CEP)}$ to the chip enable input $\overline{E}$ (see Timing Diagram), apply an output pulse $V_{O(P)}$ to the fuse link of the output to be programmed. The output pulses should be separately applied to each output.
4. After programming, the fuse link is open and the output level is changed to a low-logic-level.
5. After programming is completed, apply an additional three programming pulses.
6. Test the programmed memory to verify that the outputs are low-level or high-level as desired. Chip enable input $\overline{E}$ must be low-level for testing.

As the chip enable input $\overline{E}$ is kept high-level during programming, transistor Tr_1 maintains the off state. The word decoder circuit selects any one of 32 words, and sets the transistor Tr_1 to the on state. The collector current of the transistor Tr_2, which is supplied from the selected output O_1, opens the fuse links. At this time, the other seven fuse links of the selected word line are in a half-selected state and the other 248 fuse links are in a nonselected state.

Typical Programming Conditions

Condition sequence.	Pulse sequence	Pulse width $t_{w(P)}$ (ms)	Chip enable program voltage $V_{I(CEP)}$ (V)	Output voltage (V)
1	1 ~ 4	0.5	29	25
2	5 ~ 8	1	29	25
3	9 ~ 12	5	30	25
4	13 ~ 19	20	33	25

M54730K, M54730P, M54730S

Alternative Designation 6330

256-BIT (32-WORD BY 8-BIT) FIELD PROGRAMMABLE ROM

APPLICATIONS

Chip Enable Circuit

The chip enable input $\overline{E}$ is used for activating or inhibiting output $O_1 \sim O_8$. Chip enable $\overline{E}$ allows easy memory expansion by one of the following procedures:

1. Expanding the Number of Bits in a Word.

For example, using three 256-bit ROMs, each organized as 32 words of 8 bits, the number of bits in a word can be expanded as described below:

1. Apply a low-logic-level to chip enable input $\overline{E}$ of each ROM.
2. Connect address inputs $A_0 \sim A_4$ of each ROM in parallel. Memory is thus expanded and reorganized as 32 words of 24 bits.

2. Expanding the Number of Words in Memory

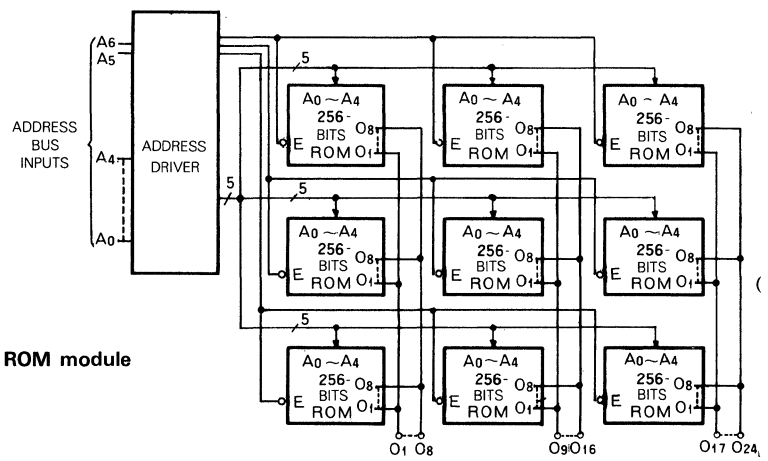
For example, using three 256-bit ROMs, each organized as 32 words of 8 bits, the number of words in memory can be expanded as described below:

1. Connect the chip enable input $\overline{E}$ of each ROM to the decoder.
2. Connect the outputs from each ROM with AND-tie connections.
3. Connect each address input $A_0 \sim A_4$ commonly. Memory is thus expanded and organized as 96 words of 4 bits.

3. Expanding the Number of Words in Memory and the Number of bits in a Word

For example, using nine 256-bit ROMs, each organized as 32 words of 8 bits, and by combining procedures 1 and 2 above, the number of words in memory along with the number of bits in a word, can be expanded as shown in the diagram below.

Memory is thus expanded and reorganized as 96 words of 24 bits.



ROM module

Pull-up Resistors

The outputs are open collectors; therefore, AND-tie connections are also possible, and normal loads can be connected. The resistance of a pull-up resistor R_L that may be connected between the voltage supply and the collectors of the output transistors should be determined by equations (1) and (2) as shown below:

$$R_{L(max)} = \frac{\overline{V_{CC}} - V_{OH}}{M \cdot \overline{I_{OH}^*} + N \cdot \overline{I_{IH}}} \quad \cdots\cdots (1)$$

where M : number of AND-ties
N : number of fanouts (number of loads)
$\overline{V_{CC}}$: maximum value of supply voltage
V_{OH} : minimum value of high-level output voltage
$\overline{I_{OH}^*}$: maximum value of high-level output current at the open collector output
$\overline{I_{IH}}$: maximum value of high-level input current

$$R_{L(min)} = \frac{V_{CC} - \overline{V_{OL}}}{\overline{I_{OL}} - N \cdot |\overline{I_{IL}}|} \quad \cdots\cdots (2)$$

where V_{CC} : minimum value of supply voltage
$\overline{V_{OL}}$: maximum value of low-level output voltage
$\overline{I_{OL}}$: maximum value of low-level output current
$\overline{I_{IL}}$: maximum value of low-level input current

then

$$R_{L(min)} < R_L < R_{L(max)} \quad \cdots\cdots (3)$$

The resistance of a pull-up resistor R_L should be within the range as shown in equation (3). R_L (min) and R_L (max) should be calculated using the appropriate number of AND-ties and fanouts. Calculation examples of TTL load are shown below:

(1) When

$M = 4$, $N = 3$, $\overline{V_{CC}} = 5.25V$,
$V_{OH} = 2.4V$, $\overline{I_{OH}^*} = 100\mu A$,
$\overline{I_{IH}} = 40\mu A$

$$R_{L(max)} = \frac{\overline{V_{CC}} - V_{OH}}{M \cdot \overline{I_{OH}^*} + N \cdot \overline{I_{IH}}} = \frac{5.25V - 2.4V}{4 \times (100\mu A) + 3 \times (40\mu A)} = 5090\Omega$$

(2) When

$N = 3$, $V_{CC} = 4.75V$,
$\overline{V_{OL}} = 0.45V$, $\overline{I_{OL}} = 16mA$,
$\overline{I_{IL}} = 1.6mA$

$$R_{L(min)} = \frac{V_{CC} - \overline{V_{OL}}}{\overline{I_{OL}} - N \cdot |\overline{I_{IL}}|} = \frac{4.75V - 0.45V}{16mA - 3 \times (1.6mA)} = 384\Omega$$

SHIFT REGISTERS

7

M58502P, M58503P, M58504P

1024-BIT DYNAMIC SHIFT REGISTER

DESCRIPTION

The M58502P, M58503P and M58504P are 1024-bit dynamic shift registers which are fabricated with the P-channel silicon-gate MOS process and adopt capacitance pull-up circuits. The M58502P is organized as 256 words of 4 bits, the M58503P as 512 words of 2 bits, and the M58504P as 1024 words of 1 bit.

FEATURES

- Fast data frequency: 3MHz (max)
- Fast clock frequency: 1.5MHz (max)
  Low power dissipation: 15μW/bit (typ)
- Small input capacitance: 140pF (typ)
- All inputs and outputs TTL-compatible
- M58502P interchangeable with Intel's 1402A in pin configuration and electrical characteristics

APPLICATION

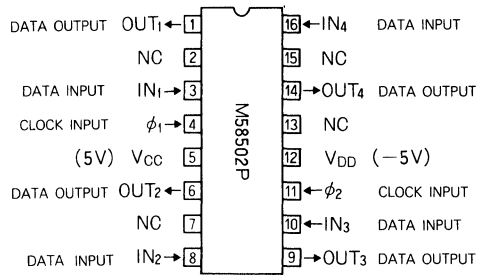
- Buffer memory for peripheral terminal equipment
- Small capacity memory system
- Analog delay line

FUNCTION

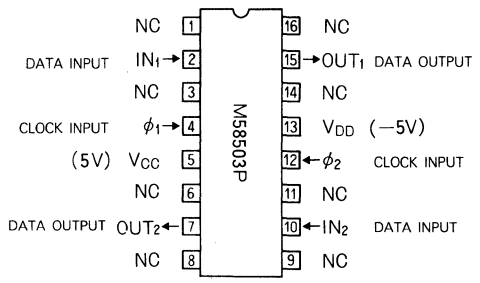
The adoption of capacitance pull-up circuits provides fast operation at low power dissipation. The M58502P is interchangeable with Intel's 1402A in pin configuration and electrical characteristics. The M58503P and the M58504P are functionally interchangeable with Intel's 1403A, 1404A (TO-5 package). Power dissipation is only 15μW/bit, about 1/20 or less the value for Intel's 1402A, 1403A and 1404A. The read/write data frequency is fast—up to 3MHz at a clock frequency of 1.5MHz. The minimum clock frequency is 500Hz, allowing use over a wide range of frequencies. All inputs and outputs are directly compatible with TTL, so that no special interface circuit is required. The V_{DD} supply voltage and the supply voltage for clock can be used in common.

PIN CONFIGURATION (TOP VIEW)

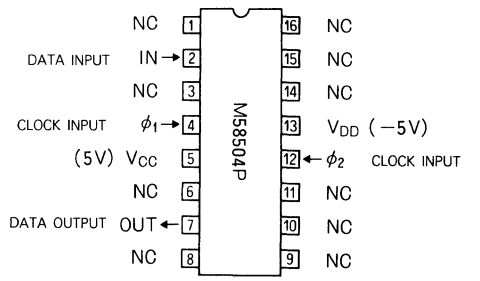
M58502P



M58503P



M58504P



Outline 16P1

7

M58502P, M58503P, M58504P

1024-BIT DYNAMIC SHIFT REGISTER

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{DD}	Supply voltage	With respect to V_{CC}	0.3～−20	V
V_I	Input voltage		0.3～−20	V
$V\phi$	Clock voltage		0.3～−20	V
V_O	Output voltage		0.3～−20	V
Pd	Power dissipation	Ta=25℃	600	mW
Topr	Operating free-air temperature range		−10～75	℃
Tstg	Storage temperature range		−40～125	℃

RECOMMENDED OPERATING CONDITIONS (Ta=−10～75℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{DD}	Supply voltage	−4.75	−5	−5.25	V
V_{IH}	High-level input voltage	V_{CC}−1.5		V_{CC}	V
V_{IL}	Low-level input voltage	V_{CC}−15		V_{CC}−4.2	V
$V_{IH(\phi)}$	High-level clock input voltage	V_{CC}−1		V_{CC}	V
$V_{IL(\phi)}$	Low-level clock input voltage	V_{CC}−17		V_{CC}−15	V

ELECTRICAL CHARACTERISTICS (Ta=−10～75℃, V_{CC}=5V±5%, V_{DD}=−5V±5%, $V_{IL(\phi)}-V_{CC}$=−15V～−17V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{OH}	High-level output voltage	V_{IH}=3.5V, R_L=3K, I_{OH}=100μA	2.4	3.5		V
V_{OL}	Low-level output voltage	V_{IL}=0.8V, R_L=3K, I_{OL}=1.6mA		−0.3	0.5	V
R_{ON}	ON output resistance	V_{IL}=3.5V, I_O=−1mA		0.5		kΩ
R_{OFF}	OFF output resistance	V_{IL}=0.8V, V_O=0V	1			MΩ
I_I	Input current	V_{IL}=V_{CC}−17V			1	μA
I_{DD}	Supply current from V_{DD}	f=1MHz, $V_{IL(\phi)}$=V_{CC}−17V		−1.5	−3	mA
C_i	Input capacitance	V_{IL}=0V, f=1MHz, 25mVrms			5	pF
C_o	Output capacitance	V_{OL}=0V, f=1MHz, 25mVrms			5	pF
$C_{i(\phi)}$	Clock input capacitance	$V_{IL(\phi)}$=0V, f=1MHz, 25mVrms		140	200	pF
$C_{i(\phi1-\phi2)}$	Capacitance between clock 1 and clock 2	$V_{IL(\phi)}$=0V, f=1MHz, 25mVrms		30	45	pF

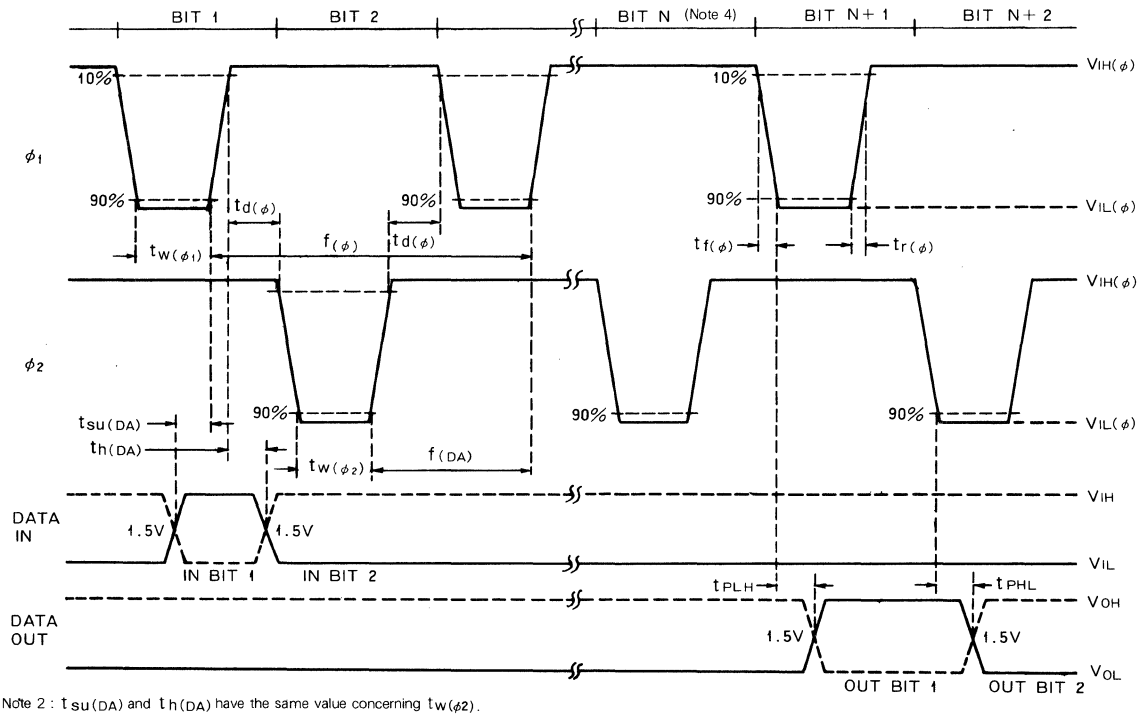
Note 1 : Current flowing into an IC is positive; out is negative.

SWITCHING CHARACTERISTICS

($T_a = -10 \sim 75°C$, $V_{CC} = 5V \pm 5\%$, $V_{DD} = -5V \pm 5\%$, $V_{IL(\phi)} - V_{CC} = -15V \sim -17V$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$f_{(DA)}$	Data frequency	$R_L = 3k\Omega$			3	MHz
$f_{(\phi)}$	Clock frequency		0.0005		1.5	MHz
$t_{w(\phi 1)}$	Clock 1 pulse width	See Timing Diagram	220		10000	ns
$t_{w(\phi 2)}$	Clock 2 pulse width		220		10000	ns
$t_{d(\phi)}$	Clock pulse delay time	$tw(\phi 1)$, $tw(\phi 2) = 220ns$	60			ns
$t_{r(\phi)}$	Clock pulse rise time	See Timing Diagram			1000	ns
$t_{f(\phi)}$	Clock pulse fall time				1000	ns
$t_{su(DA)}$	Data setup time		40			ns
$t_{h(DA)}$	Data hold time		40			ns
t_{PHL}	High-to-low-level output propagation time				90	ns
t_{PLH}	Low-to-high-level output propagation time				90	ns

TIMING DIAGRAM

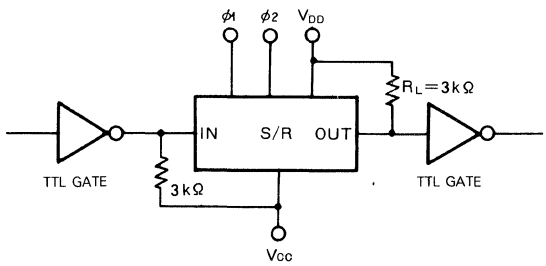


Note 2 : $t_{su(DA)}$ and $t_{h(DA)}$ have the same value concerning $t_{w(\phi 2)}$.

3 : The rise time and fall time of the input waveform are less than 10ns and the output load is one TTL gate.

4 : N equals 256 in the M58502P, 512 in the M58503P and 1024 in the M58504P.

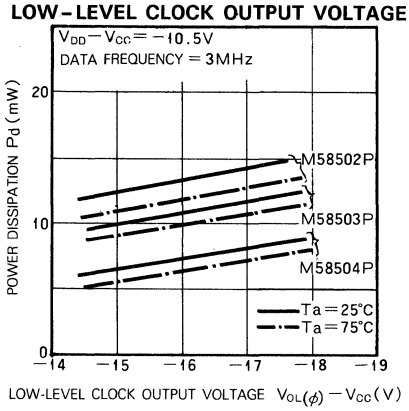
INTERFACE WITH TTL



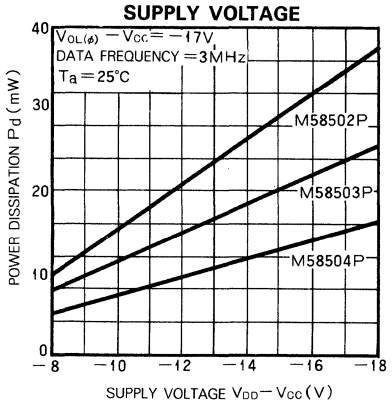
1024-BIT DYNAMIC SHIFT REGISTER

TYPICAL CHARACTERISTICS

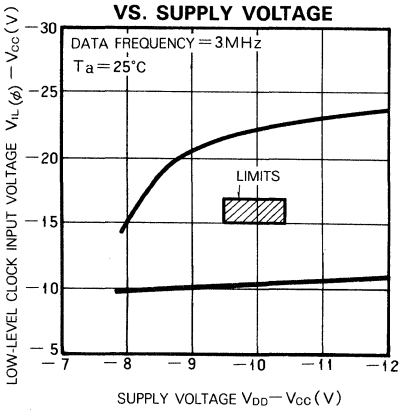
POWER DISSIPATION VS. LOW-LEVEL CLOCK OUTPUT VOLTAGE



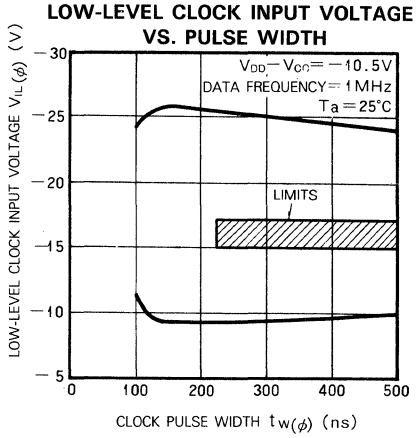
POWER DISSIPATION VS. SUPPLY VOLTAGE



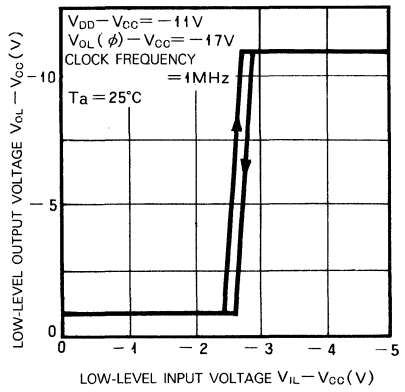
LOW-LEVEL CLOCK INPUT VOLTAGE VS. SUPPLY VOLTAGE



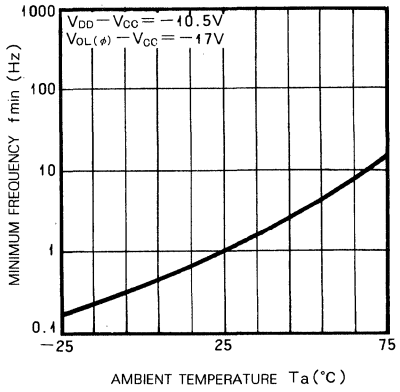
LOW-LEVEL CLOCK INPUT VOLTAGE VS. PULSE WIDTH



EFFECTIVE INPUT CHARACTERISTICS



MINIMUM FREQUENCY VS. AMBIENT TEMPERATURE



LSIs FOR PERIPHERAL CIRCUITS

8

M58609-XXS

KEYBOARD ENCODER

DESCRIPTION

The M58609-XXS is a keyboard encoder for reed switches of terminal equipment. It is fabricated using P-channel aluminum-gate MOS technology and is packaged in a 40-pin DIL package. It contains a 3168-bit mask-programmable read-only memory in which each key's code is stored. The 9-bit code corresponding to any one of 88 keys, each of which can be in any one of 4 mode shifts, can be read out. The outputs are TTL/DTL-compatible. The output consists of an 8-bit code and a parity bit. The address is selected by the 8-bit and 11-bit ring counters. Custom-programmed coding is available. The XX in the type code stands for a 2-digit decimal number that identifies the customer's specification to which the ROM has been programmed.

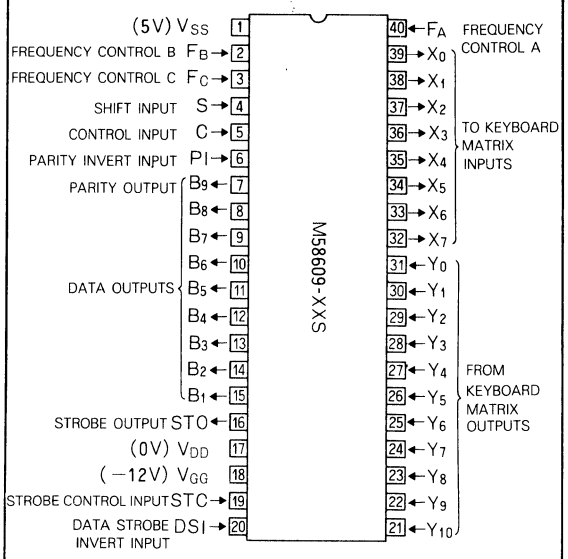
FEATURES

- TTL/DLT-compatible (except X, Y terminals)
- Two-key rollover operation
- N-key lockout operation
- Self-contained clock generator circuit
- Strobe delay circuit for eliminating key contact bounce
- External control for output polarity (positive or negative logic)
- External control for selecting odd or even parity

APPLICATION

- Encoder for full-keyboard terminal equipment

PIN CONFIGURATION (TOP VIEW)



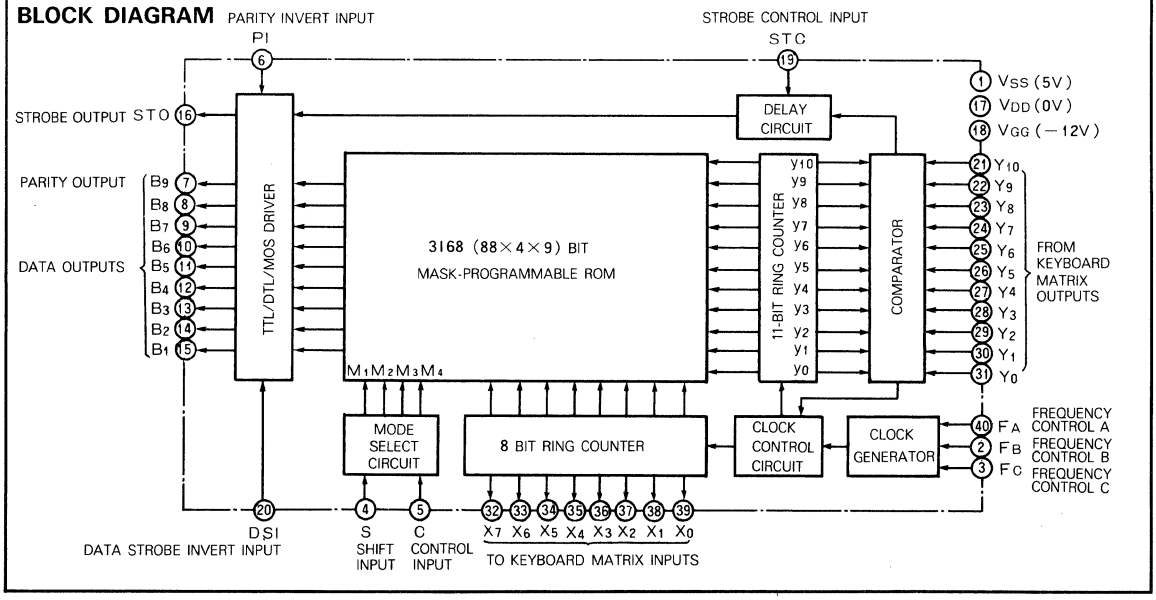
Outline 40S1

FUNCTION

Outputs (X_0~X_7) of the 8-bit ring counter and inputs (Y_0~Y_{10}) of the 11-bit comparator are wired to the keyboard to form an 8×11 (88-cross points) switch matrix.

When the key connected with X_i and Y_j is depressed, a path is formed between them. When the level of Y_j matches that of X_i, which comes from the 8-bit ring counter, the comparator generates a coincidence signal for clock control and delay circuit. This clock control stops the clock signals to the ring counter and data outputs (B_1~B_9) stabilizing the selected 9-bit code. The stabilization is indicated by a valid signal on the strobe output. A strobe output signal is generated at the time set by the externally controlled delay circuit which receives the coincidence signal. Data outputs and strobe output remain stable until the key is released.

BLOCK DIAGRAM



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KEYBOARD ENCODER

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{GG}	Supply voltage	With respect to V_{SS}	0.3～−20	V
V_{DD}	Supply voltage		0.3～−20	V
V_I	Input voltage		0.3～−20	V
Topr	Operating free-air temperature range		−20～75	°C
Tstg	Storage temperature range		−40～125	°C

RECOMMENDED OPERATING CONDITIONS (Ta = −20～75°C, unless otherwise noted)

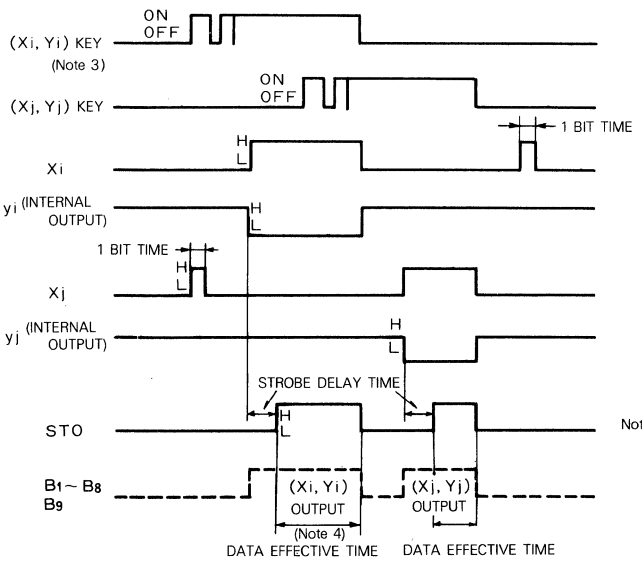
Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{GG}	Supply voltage	−11	−12	−13	V
V_{DD}	Supply voltage		0		V
V_{SS}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{SS}−1			V
V_{IL}	Low-level input voltage			0.8	V
$f_{(\phi)}$	Clock frequency	20	50	100	kHz
$t_{D(STO)}$	Strobe delay time		1.5		ms
R_{OFF}	Switch off resistance	10			MΩ
R_{ON}	Switch on resistance			300	Ω

ELECTRICAL CHARACTERISTICS (Ta = −20～75°C, V_{GG} = −12±1V, V_{SS} = 5±0.5V, V_{DD} = 0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$V_{OH(Bi,STO)}$	High-level output voltage, B_1～B_9 and STO	I_{OH} = −100μA	V_{SS}−1			V
$V_{OH(Xi)}$	High-level output voltage, X_0～X_7	I_{OH} = −100μA	V_{SS}−1.3			V
$V_{OL(Bi,STO)}$	Low level output voltage, B_1～B_9 and STO	I_{OL} = 1.6mA			0.4	V
$V_{OL(Xi)}$	Low-level output voltage, X_0～X_7	I_{OL} = 1μA			−3	V
R_I	Input resistance, S. C. DSI and PI	V_I = −12V	1			MΩ
Pd	Power dissipation	Ta = 25°C		70	200	mW
Ci	Input capacitance	V_I = 0V, f = 1MHz, Ta = 25°C			15	pF

Note 1 : Current flowing into an IC is positive; out is negative.

TIMING DIAGRAM



Note 2 : DSI = "L"

3 : (Xi, Yi) KEY indicates the key switch that is located at the cross point of Xi and Yi of the keyboard matrix.

4 : (Xi, Yi) OUTPUT indicates the code output of the key that is selected by the (Xi, Yi) KEY.

FUNCTION TABLES

Data ($B_1 \sim B_9$) Invert

DSI (Pin ⑳)	Code table ($B_1 \sim B_9$)	Data output ($B_1 \sim B_9$)
H	↑	L
L	↑	H
H	0	H
L	0	L

Strobe (STO) Invert

DSI (Pin ⑳)	Internal strobe (Note 3)	STO (Pin ⑯)
H	H	L
L	H	H
H	L	H
L	L	L

Parity (B_9) Invert

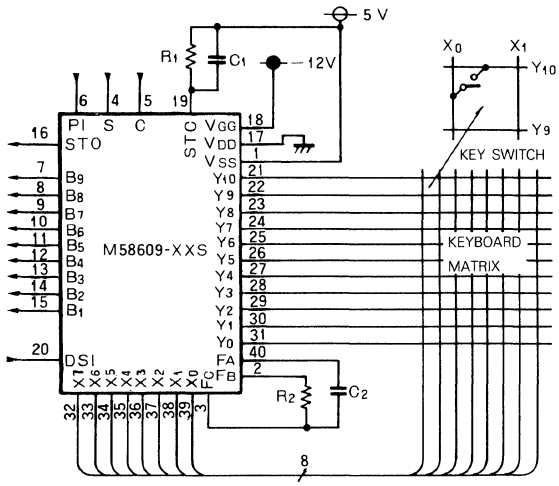
P_1 (Pin ⑥)	Code table (B_9)	B_9 (Pin ⑦)
H	↑	L
L	↑	H
H	0	H
L	0	L

Mode Select

S (Pin ④)	C (Pin ⑤)	Mode
L	L	M_1
H	L	M_2
L	H	M_3
H	H	M_4

Note 3 : The internal signal of the strobe output (STO) becomes high-level when the strobe signal is generated.

EXAMPLE OF APPLICATION CIRCUIT



Note 4 : $R_1 = 1.5M\Omega$, $C_1 = 0.001\mu F$ provides approximately 1.5ms delay time.
5 : $R_2 = 75k\Omega$, $C_2 = 50pF$ provides approximately 50kHz clock frequency.

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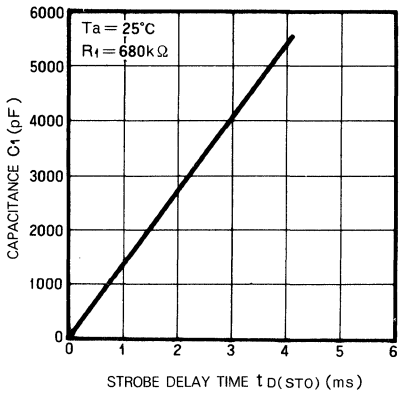
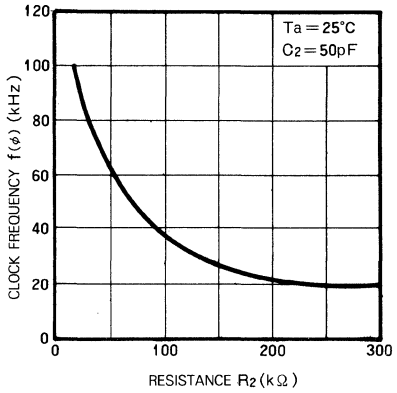
KEYBOARD ENCODER

TYPICAL CHARACTERISTICS (V_{GG} = −12V, V_{DD} = 0 V, V_{SS} = 5 V)

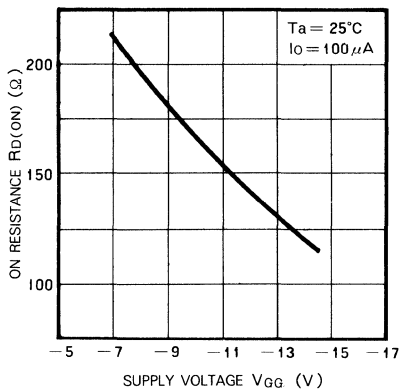
CAPACITANCE VS. STROBE DELAY TIME



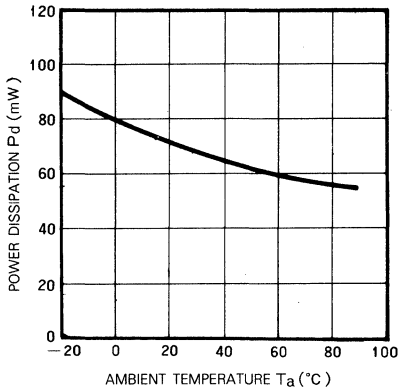
CLOCK FREQUENCY VS. RESISTANCE



ON RESISTANCE OF OUTPUT DRIVER VS. POWER SUPPLY VOLTAGE



POWER DISSIPATION VS. AMBIENT TEMPERATURE



KEYBOARD ENCODER (JIS CODE STANDARD PRODUCT)

DESCRIPTION

The M58609-04S is a standard product of the M58609-XXS. the 8-bit codes specified in JIS C6220-1969 "Codes for Information Interchange" are stored in this ROM. The codes can be odd or even parity. The function, pin configuration and electrical characteristics are the same as those of an M58609-XXS.

FUNCTION

Data output and parity output

The relationships between B_1~B_8 in the code table and B_1 ~B_8 in data outputs are shown in Table 1, and those between the parity output B_9 and the parity bit, in Table 2. The parity bit in the table is defined as a '0' when the number of '1's in the code B_1~B_8 is odd and a '1' when it is even.

Mode selection is shown in Table 3.

Table 1 Relationship between code table and data outputs

B_1 ~ B_8 Code table	Data strobe invert input DSI	Data output B_1 ~ B_8	Logic
1	L	H	Positive logic
1	H	L	Nogative logic
0	L	L	Positive logic
0	H	H	Negative logic

Table 2 Parity output

Parity bit	Parity invert input PI	Parity output B_9
1	L	H
1	H	L
0	L	L
0	H	H

Table 3 Mode selection

Shift input S	Control input C	Selected mode
L	L	1
H	L	2
L	H	3
H	H	4

CODE TABLE (JIS-C-6220-1969)

NUMBER OF BITS

* B_9	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1	ROW \ COL	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
PARITY BIT										0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
										0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
										0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
										0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
					0	0	0	0	0	NUL	DLE	SP	0	@	P	、					—	タ	ミ		
					0	0	0	1	1	SOH		!	1	A	Q					。	ア	チ	ム		
					0	0	1	0	2	STX		"	2	B	R					「	イ	ツ	メ		
					0	0	1	1	3	ETX		#	3	C	S					」	ウ	テ	モ		
					0	1	0	0	4	EOT		$	4	D	T					、	エ	ト	ヤ		
					0	1	0	1	5	ENQ	NAK	%	5	E	U					・	オ	ナ	ユ		
					0	1	1	0	6	ACK	SYN	&	6	F	V					ヲ	カ	ニ	ヨ		
					0	1	1	1	7	BEL	ETB	'	7	G	W					ァ	キ	ヌ	ラ		
					1	0	0	0	8	BS	CAN	(	8	H	X					ィ	ク	ネ	リ		
					1	0	0	1	9	HT	EM	)	9	I	Y					ゥ	ケ	ノ	ル		
					1	0	1	0	10	LF	SUB	*	:	J	Z					エ	コ	ハ	レ		
					1	0	1	1	11	VT	ESC	+	;	K	[		{			ォ	サ	ヒ	ロ		
					1	1	0	0	12	FF		,	<	L	¥		|			ャ	シ	フ	ワ		
					1	1	0	1	13	CR		−	=	M	]		}			ュ	ス	ヘ	ン		
					1	1	1	0	14	SO		.	>	N	^		~			ョ	セ	ホ	゛		
					1	1	1	1	15	SI		/	?	O	_		DEL			ッ	ソ	マ	゜		

* B_9 parity is odd for an 8-bit code system.

Note : A '1' or '0' in the code table indicates that the output level goes high for '1' and low for '0' when input DSI and PI are low-level.

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KEYBOARD ENCODER (JIS CODE STANDARD PRODUCT)

CODE ARRANGEMENT TABLE

Yi \ Xi	Mode	X0	X1	X2	X3	X4	X5	X6	X7
Y0	1	NUL	DLE	^	0	;	L	O	9
	2	NUL	DLE	−	NUL	+	NUL	NUL	)
	3	NUL	DLE	ヘ	ワ	レ	リ	ラ	ヨ
	4	NUL	DLE	NUL	ヲ	NUL	NUL	NUL	ョ
Y1	1	SOH	6	0	−	／	K	I	8
	2	SOH	6	0	=	?	NUL	NUL	(
	3	SOH	6	0	ホ	メ	ノ	ニ	ユ
	4	SOH	6	0	NUL	・	NUL	NUL	ュ
Y2	1	STX	7	1	P	．	J	U	7
	2	STX	7	1	NUL	>	NUL	NUL	'
	3	STX	7	1	セ	ル	マ	ナ	ヤ
	4	STX	7	1	NUL	。	NUL	NUL	ャ
Y3	1	ETX	8	2	(	,	H	Y	6
	2	ETX	8	2	¦	<	NUL	NUL	&
	3	ETX	8	2	°	ネ	ク	ン	オ
	4	ETX	8	2	「	、	NUL	NUL	ォ
Y4	1	EOT	9	3	¥	M	G	T	5
	2	EOT	9	3	|	NUL	NUL	NUL	%
	3	EOT	9	3	−	モ	キ	カ	エ
	4	EOT	9	3	NUL	NUL	NUL	NUL	ェ
Y5	1	ENQ	NAK	4	BS	N	F	R	4
	2	ENQ	NAK	4	BS	NUL	NUL	NUL	$
	3	ENQ	NAK	4	BS	ミ	ハ	ヌ	ウ
	4	ENQ	NAK	4	BS	NUL	NUL	NUL	ゥ
Y6	1	ACK	SYN	5	NUL	B	D	E	3
	2	ACK	SYN	5	_	NUL	NUL	NUL	#
	3	ACK	SYN	5	口	コ	シ	イ	ア
	4	ACK	SYN	5	NUL	NUL	NUL	イ	ァ
Y7	1	BEL	ETB	+	]	V	S	W	2
	2	BEL	ETB	+	｜	NUL	NUL	NUL	"
	3	BEL	ETB	+	ム	ヒ	ト	テ	フ
	4	BEL	ETB	+	」	NUL	NUL	NUL	NUL
Y8	1	=	CAN	SP	CR	C	A	Q	I
	2	=	CAN	SP	CR	NUL	NUL	NUL	!
	3	=	CAN	SP	CR	ソ	チ	タ	ヌ
	4	=	CAN	SP	CR	NUL	NUL	NUL	NUL
Y9	1	SO	EM	・	LF	X	FF	HT	@
	2	SO	EM	・	LF	NUL	FF	HT	`
	3	SO	EM	・	LF	サ	FF	HT	｀
	4	SO	EM	・	LF	NUL	FF	HT	NUL
Y10	1	SI	SUB	−	DEL	Z	ESC	VT	:
	2	SI	SUB	−	DEL	NUL	ESC	VT	*
	3	SI	SUB	−	DEL	ツ	ESC	VT	ケ
	4	SI	SUB	−	DEL	ッ	ESC	VT	NUL

SYMBOLS AND THEIR NAMES

Symbol	Code name	Col/Row in code table	X/Y/Mode in code arrangement table
SP	Space	2 / 0	2/8/1～4
!	Exclamation mark	2 / 1	7/8/2
"	Quotation mark, umlaut	2 / 2	7/7/2
#	Number sign	2 / 3	7/6/2
$	Dollar sign	2 / 4	7/5/2
%	Percentage	2 / 5	7/4/2
&	Ampersand	2 / 6	7/3/2
'	Apostrophe, acute accent	2 / 7	7/2/2
(	Left parenthesis	2 / 8	7/1/2
)	Right parenthesis	2 / 9	7/0/2
*	Asterisk, multiplication sign	2 / 10	7/10/2
+	Positive sign, plus sign	2 / 11	2/7/1～4,4/0/2
,	Comma	2 / 12	4/3/1
−	Negative sign, subtraction sign	2 / 13	2/10/1～4,3/1/1
.	Period	2 / 14	2/9/1～4,4/2/1
/	Slash, virgule, division sign, per	2 / 15	4/1/1
:	Colon	3 / 10	7/10/1
;	Semicolon	3 / 11	4/0/1
<	Less than sign	3 / 12	4/3/2
=	Equal sign	3 / 13	0/8/1～4,3/1/2
>	Greater than sign	3 / 14	4/2/2

Symbol	Code name	Col/Row in code table	X/Y/Mode in code arrangement table
?	Question mark	3 / 15	4/1/2
@	At mark	4 / 0	7/9/1
[	Left bracket	5 / 11	3/3/1
¥	Yen sign	5 / 12	3/4/1
]	Right bracket	5 / 13	3/7/1
^	Circumflex accent	5 / 14	2/0/1
_	Underline	5 / 15	3/6/2
`	Grave accent	6 / 0	7/9/2
{	Left brace	7 / 11	3/3/2
|	Separate sign, logical add sign	7 / 12	3/4/2
}	Right brace	7 / 13	3/7/2
¯	Overline, logical not sign	7 / 14	2/0/2
。	Japanese period	10 / 1	4/2/4
「	Japanese initial quotation mark	10 / 2	3/3/4
」	Japanese final quotation mark	10 / 3	3/7/4
、	Japanese comma	10 / 4	4/3/4
・	Middle dot	10 / 5	4/1/4
ー	Long vowel mark	11 / 0	3/4/3
゛	Voiced consonant mark	13 / 14	7/9/3
゜	Semi-voiced consonant mark	13 / 15	3/3/3

M58620-XXXS

KEYBOARD ENCODER

DESCRIPTION

The M58620-XXXS is a keyboard encoder for solid-state switches and is fabricated with P-channel aluminum-gate MOS technology.

All codes are stored in a 3640-bit ROM. It can store codes for up to 91 keys, and each key can have 4 mode shifts. The mode shift is selected by the combination of shift input, control input and shift control input. The output consists of a 9-bit plus parity bit code. All inputs and outputs are TTL-compatible.

Custom programming is available. The XXX in the type code stands for a 3-digit decimal number that identifies the customer's specification to which the ROM has been programmed.

FEATURES

- All inputs and outputs are TTL-compatible
- Output buffer register
- Strobe inhibit circuit for unused codes
- One shot output (the pulse width is variable) or static output for strobed output
- Chip enable terminal
- 2-key rollover capability (N-key rollover is also available, if the logic output of the switches is pulsive)

APPLICATION

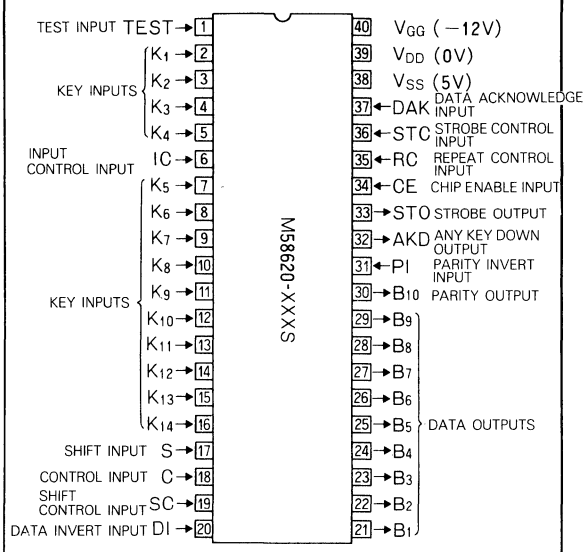
- Encoder for full-keyboard terminal equipment

FUNCTION

The output of each keyboard switch is connected to 2-key inputs selected from $K_1 \sim K_{14}$ (2 of 14) to form 91 addresses. Therefore, the character code for output is selected by 2 of 14 key inputs, shift input, control input and shift control input.

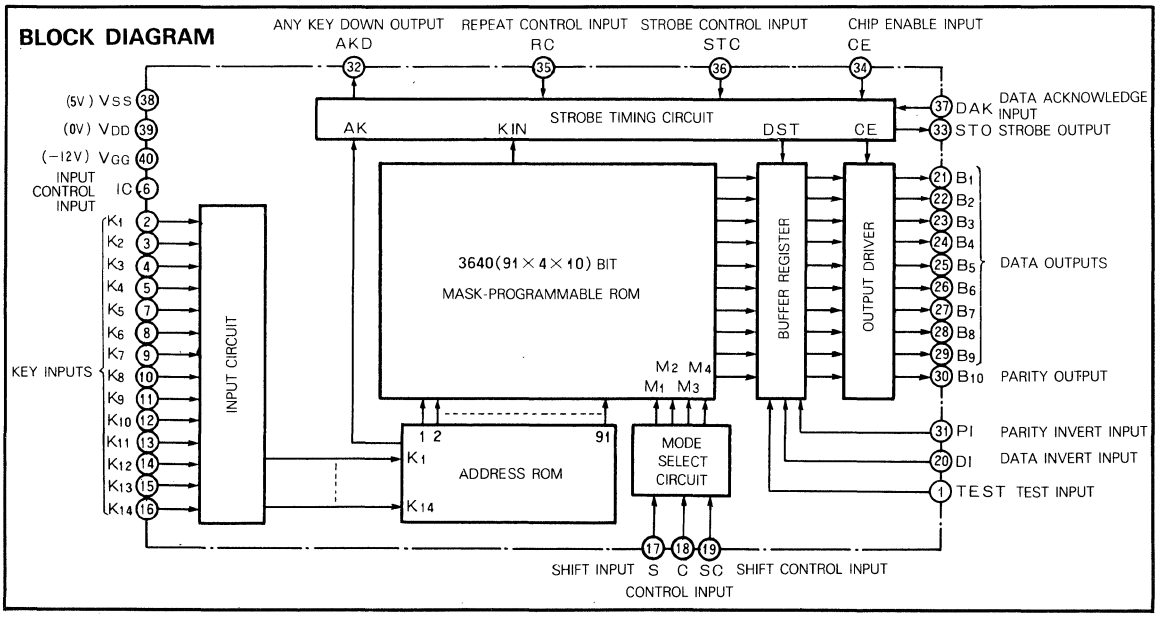
When a key is depressed, the output of that keyboard switch is applied to two key inputs selected from $K_1 \sim K_{14}$; the address ROM generates an address that is used for input to the 3640-bit ROM. After the encoded data from the ROM is transferred to the buffer register, a strobed output is generated, validating the encoded data.

PIN CONFIGURATION (TOP VIEW)



Outline 40S1

BLOCK DIAGRAM



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KEYBOARD ENCODER

OPERATION

1. 2-Key Rollover (N-Key Lockout)

When more than 2 keyboard switches are depressed at the same time, all outputs 1~91 of the address ROM go high-level, and the 3640-bit ROM is not addressed. The internal key input signal also is not applied to the timing circuit; as a result, a strobe signal is not generated. Also, the coded outputs hold the preceding state. Then, if any one key (key 1) is not released while the other keys are, key 1 becomes valid.

2. N-Key Rollover

If the key input signals are pulsive, the primary depressed key (key 1) is read; after the coded output of key 1 is transferred to the buffer register, a strobe signal is generated and the coded output becomes valid. Then, if a second key is depressed while key 1 is in the depressed state, the second key (key 2) is read; and the coded output of key 2 is transferred to the buffer register succeeding the coded output of key 1 described above. A strobe signal is generated, and the coded output becomes valid. Then if a third, fourth . . . Nth key is depressed while preceding keys are still in the depressed state, its code will become valid as described above.

3. Any-Key-Down Output

When any one or more of the 91 keys are depressed, an internal any-key signal is transferred from the address ROM to the timing circuit where an any-key-down signal (AKD) is generated.

4. Strobe Inhibit When an Unused Code Is Addressed

If either an unused mode of the 4 modes or an unused key is selected (its ROM code is 0000000000), the strobe output is inhibited and it makes the key invalid. The data output still holds the preceding state.

5. Repeat Function

When a repeat signal is applied to the repeat control input (RC), a strobe signal is repeatedly generated so that any character can be repeated. The strobe signal is inhibited when the RC terminal is high.

6. Data Acknowledge Input

The strobe output is reset by applying a data acknowledge input. The pulse width of the strobe signal output can be adjusted with a resistor and a capacitor connected between the strobe output terminal (STO) and the data acknowledge input terminal (DAK).

7. Data Invert and Parity Invert Inputs

The level of each output B_1~B_9 and B_{10} can be inverted when data invert input (DI) and parity invert input (PI) are high-level.

8. Chip Enable Input

Data outputs B_1~B_{10}, strobe output and any-key-down output are in the floating state when chip enable input (CE) is high.

This floating state means a high-impedance state and is equivalent to an open-circuit output.

9. Input Control Input

When input control input (IC) is high, key inputs (K_1~K_{14}) can be operated with high-level signals.

10. Strobe Control Input

The strobe delay time can be set by the strobe control input STC terminal. The delay time is set to $t_{d(ST-B)}$, which depends on the internal delay circuit when the strobe control input terminal is connected to V_{SS}.

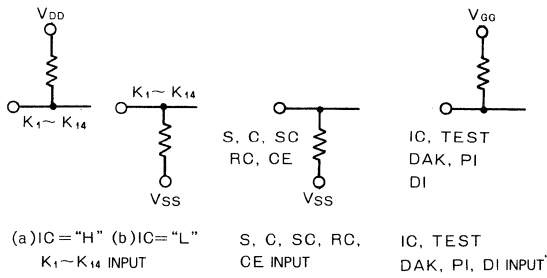
11. Test Input

Data outputs (B_1~B_{10}) can be independently set either high or low irrespective of the 3640-bit ROM outputs. When test input (TEST) is high, B_1~B_{10} goes high if both DI and PI are low, and B_1~B_{10} goes low is both DI and PI are high.

12. Pull-up Resistors

External resistors are not required because pull-up resistors are built-in at all input terminals. But if the strobe control input terminal is not used, it should be connected to V_{SS}. To determine the value of the resistor required, see Electrical Characteristics.

Pull-up resistors



(a) IC = "H" (b) IC = "L" K_1~K_{14} INPUT

S, C, SC, RC, CE INPUT

IC, TEST DAK, PI, DI INPUT

Table 1 Data-output level in relation to data invert (DI), parity invert (PI) and chip enable (CE)

ROM CODE	DI, PI	CE	B1~B10
1	H	L	L
	L	L	H
0	H	L	H
	L	L	L
1	H	H	Z
	L	H	Z
0	H	H	Z
	L	H	Z

Note 1 : Z indicates a floating state.
2 : The code table is described in positive logic, for outputs B_1 ~B_{10}, when DI and PI are low.

Table 2 Function table of the mode select circuit

S	C	SC	MODE
H	H	H	—
L	H	H	—
H	L	H	—
L	L	H	M4
H	H	L	M4
L	H	L	M3
H	L	L	M2
L	L	L	M1

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{GG}	Supply voltage	With respect to V_{SS}	0.3～−20	V
V_{DD}	Supply voltage		0.3～−20	V
V_I	Input voltage		0.3～−20	V
Pd	Power dissipation	Ta＝25°C	1.0	W
Topr	Operating free-air temperature range		−20～75	°C
Tstg	Storage temperature range		−40～125	°C

RECOMMENDED OPERATING CONDITIONS (Ta＝−20～75°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{GG}	Supply voltage	−10.8	−12	−13.2	V
V_{DD}	Supply voltage		0		V
V_{SS}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage, all inputs except STC	V_{SS}−1.5		V_{SS}	V
V_{IL}	Low-level input voltage	V_{DD}		V_{SS}−3.5	V
t_r	Rise time (10～90%), all inputs except DAK			1	μs
t_f	Fall time (10～90%)			1	μs
$t_{r(DAK)}$	Rise time (10～90%), DAK			100	μs
$t_{f(DAK)}$	Fall time (10～90%), DAK			100	μs

ELECTRICAL CHARACTERISTICS (Ta＝−20～75°C, V_{GG}＝−12V±10%, V_{DD}＝0V, V_{SS}＝5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{OH}	High-level output voltage	I_{OH}＝−100μA	V_{SS}−1			V
V_{OL}	Low-level input voltage	I_{OL}＝1.6mA, (Note 2)			0.4	V
$I_{I(1)}$	Input current, TEST, IC, DI, PI, and DAK	V_I＝V_{GG}		−0.01	−10	μA
$I_{I(2)}$	Input current, K_1～K_{14}	V_I＝V_{DD}, $V_{I(IC)}$＝V_{IH}		−0.02	−20	μA
$R_{I(1)}$	Input resistance, IC, PI, DI, DAK, and TEST	V_I＝V_{SS}, Ta＝25°C	100	180	300	kΩ
$R_{I(2)}$	Input resistance, S, C, SC, CE, and RC	V_I＝V_{DD}, Ta＝25°C	5		30	kΩ
$R_{I(3)}$	Input resistance, K_1～K_{14}	V_I＝V_{SS}, $V_{I(IC)}$＝V_{IH}, Ta＝25°C	10	20	40	kΩ
$R_{I(4)}$	Input resistance, K_1～K_{14}	V_I＝V_{DD}, $V_{I(IC)}$＝V_{IL}, Ta＝25°C	2	5	15	kΩ
Pd	Power dissipation	Ta＝25°C		350	500	mW
Ci	Input capacitance	All terminals except the tested terminal are 0V. V_I＝0V, Vrms＝25mV, f＝1MHz			15	pF

Note 1 : Current flowing into an IC is positive; out is negative.

2 : When all outputs are at I_{OL}＝1.6mA, V_{OL}max＝0.6V

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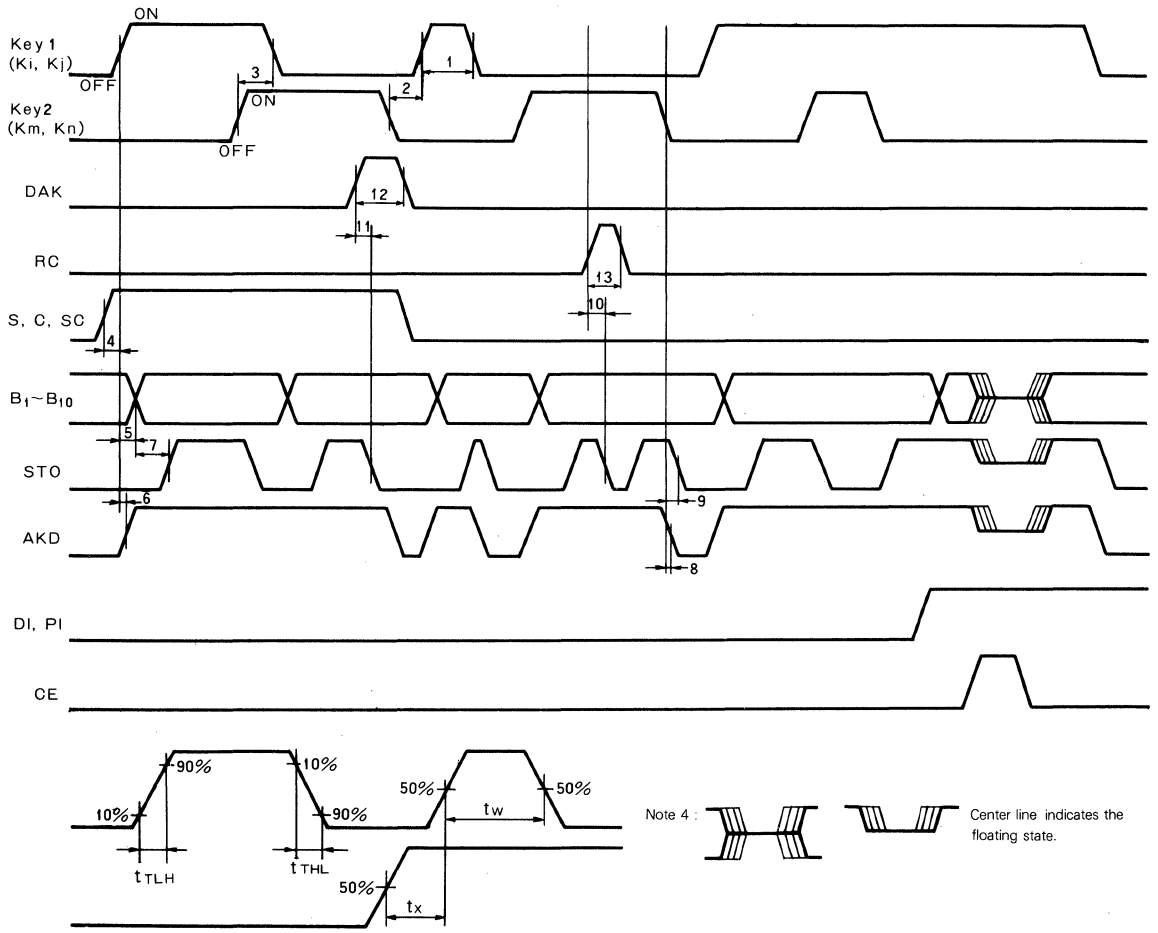
KEYBOARD ENCODER

SWITCHING CHARACTERISTICS (T_a=25°C, V_{GG}=−12V±10%, V_{DD}=0V, V_{SS}=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions (Note 3)	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-to-high-level output transition time	C_L=50pF, I_{OH}=−0.1mA		0.7	2	μs
t_{THL}	High-to-low-level output transition time	C_L=50pF, I_{OL}=1.6mA		0.5	1.5	μs
$t_{w(KI)}$	Key input pulse width	*1, tw	30			μs
$t_{d(KILH-K2HL)}$	Delay time from key 1 low-to-high-level	*2, tx	10			μs
$t_{h(K1-K2)}$	Key 1 hold time with respect to key 2	*3, tx	10			μs
$t_{su(M-KON)}$	S, C, SC setup time with respect to key input (ON)	*4, tx			1.5	μs
$t_{D(B-KON)}$	Delay time from key input (ON) to B_1~B_{10}	*5, tx	2	7	15	μs
$t_{D(AK-KON)}$	Delay time from key input (ON) to AKD	*6, tx		0.5	2	μs
$t_{d(ST-B)}$	Delay time from B_1~B_{10} to STO	*7, tx, C_L=50pF, STC-Vss shorted	1	5	12	μs
$t_{D(AK-KOF)}$	Delay time from key input (OFF) to AKD	*8, tx, C_L=50pF		0.5	2	μs
$t_{D(ST-KOF)}$	Delay time from key input (OFF) to STO	*9, tx, C_L=50pF		4	10	μs
$t_{(ST-RC)}$	Delay time from RC to STO	*10, tx, C_L=50pF		3.5	20	μs
$t_{D(ST-DAK)}$	Delay time from DAK to STO	*11, tx, C_L=50pF		4	10	μs
$t_{w(DAK)}$	DAK pulse width	*12, tw	10			μs
$t_{w(RC)}$	RC pulse width	*13, tw	15			μs
$t_{w(STO)}$	STO pulse width	tw, C_L=50pF, STO-DAK shorted	1	4	10	μs

Note 3 : See the Timing Diagram for 'tw' and 'tx'. Numbers 1 through 13 in the diagram correspond to *1 through *13 above.

TIMING DIAGRAM

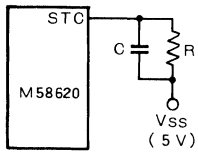


Note 4 : Center line indicates the floating state.

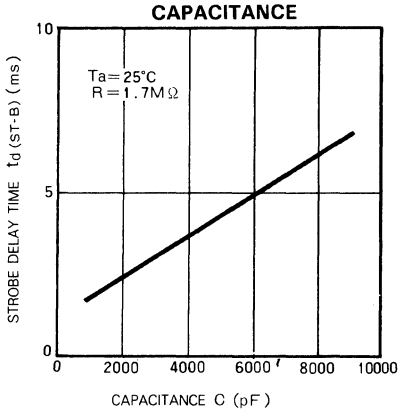
MITSUBISHI ELECTRIC

TYPICAL CHARACTERISTICS ($V_{GG}=-12V$, $V_{DD}=0V$, $V_{SS}=5V$)

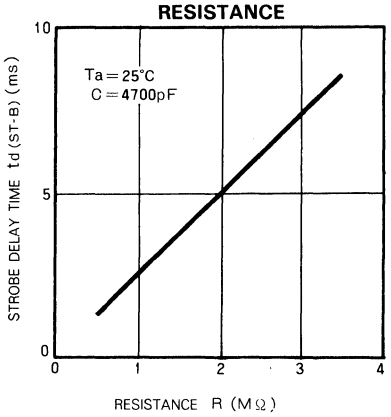
MEASUREMENT CIRCUIT



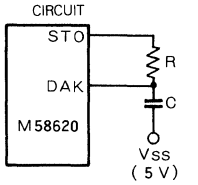
STROBE DELAY TIME VS. CAPACITANCE



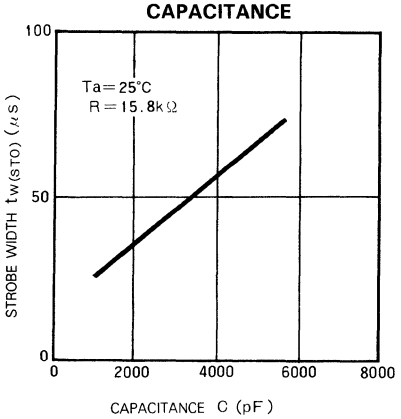
STROBE DELAY TIME VS. RESISTANCE



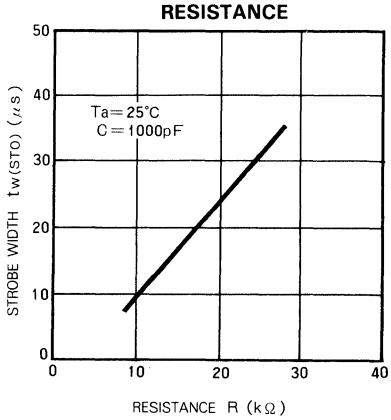
MEASUREMENT CIRCUIT



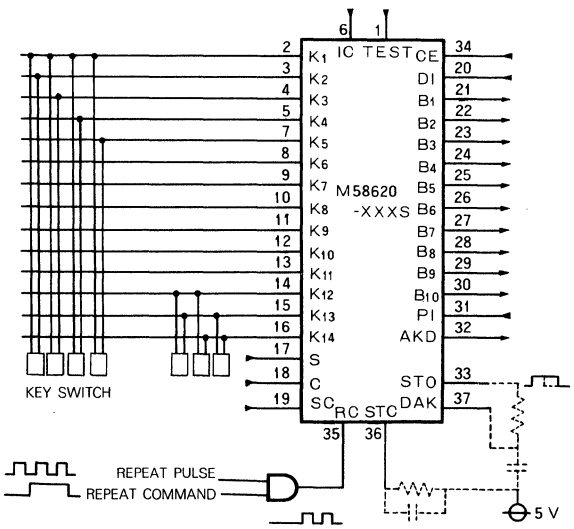
STROBE WIDTH VS. CAPACITANCE



STROBE WIDTH VS. RESISTANCE



TYPICAL APPLICATION CIRCUIT



Use a key switch having outputs that are open-collector, or mutually separated by diodes.

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M58620-001S

KEYBOARD ENCODER (JIS CODE STANDARD PRODUCT)

DESCRIPTION

The M58620-001S is a standard product of the M58620-XXXS. The 7-bit and 8-bit codes specified in JIS publication C6220-1969 "Codes for Information Interchange" are stored in this ROM. Odd parity is available for the 7-bit code, and either odd or even parity for the 8-bit code. The function, pin configuration and electrical characteristics are the same as a M58620-XXXS.

FUNCTION

The relationships between B_1~B_8 in the code table and B_1 ~B_8 in data outputs are shown in Table 1, and those between the parity output (B_{10} or B_9) and the parity bit, in Tables 2 and 3. The parity bit in the tables is defined as a '0' when the number of '1's in the code (B_1~B_8 or B_1~B_7) is odd and a '1' when it is even.

Mode selection is shown in Table 4.

Table 1 Relation between code table and outputs

B_1~B_8 in code table	Data invert input DI	Data output B_1~B_8	Logic
1	L	H	Positive logic
1	H	L	Negative logic
0	L	L	Positive logic
0	H	H	Negative logic

Table 2 Parity output of 8-bit code

Parity bit	Parity invert output PI	Parity output B_{10}
1	L	H
1	H	L
0	L	L
0	H	H

Table 3 Parity output of 7-bit code

Parity bit	Data invert input DI	Data output B_9
1	L	H
1	H	L
0	L	L
0	H	H

Table 4 Mode selection

Shift input S	Control input C	Shift control input SC	Selected mode
L	L	L	1
H	L	L	2
L	H	L	3
H	H	L	4
L	L	H	4
H	L	H	—
L	H	H	—
H	H	H	—

CODE TABLE (JIS-C-6220-1969)

NUMBER OF BIT																			
									0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
									0	0	0	0	1	1	1	1	0	0	0	1	1	1	1	1
									0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
									0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
B_{10}†	B_9*	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1	ROW \ COL	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
PARITY BIT						0	0	0	0	0	NUL	DLE	SP	0	@	P	、					—	タ	ミ		
						0	0	0	1	1	SOH	DC1	!	1	A	Q					。	ア	チ	ム		
						0	0	1	0	2	STX	DC2	"	2	B	R					「	イ	ツ	メ		
						0	0	1	1	3	ETX	DC3	#	3	C	S					」	ウ	テ	モ		
						0	1	0	0	4	EOT		$	4	D	T					、	エ	ト	ヤ		
						0	1	0	1	5	ENQ	NAK	%	5	E	U					・	オ	ナ	ユ		
						0	1	1	0	6	ACK	SYN	&	6	F	V					ヲ	カ	ニ	ヨ		
						0	1	1	1	7	BEL	ETB	'	7	G	W					ァ	キ	ヌ	ラ		
						1	0	0	0	8	BS	CAN	(	8	H	X					ィ	ク	ネ	リ		
						1	0	0	1	9	HT	EM	)	9	I	Y					ゥ	ケ	ノ	ル		
						1	0	1	0	10	LF	SUB	*	:	J	Z					ェ	コ	ハ	レ		
						1	0	1	1	11	VT	ESC	+	;	K	[		{			ォ	サ	ヒ	ロ		
						1	1	0	0	12	FF		,	<	L	¥		|			ャ	シ	フ	ワ		
						1	1	0	1	13	CR		−	=	M	]		}			ュ	ス	ヘ	ン		
						1	1	1	0	14	SO		.	>	N	^		~			ョ	セ	ホ	゛		
						1	1	1	1	15	SI		/	?	O	_		DEL			ッ	ソ	マ	゜		

* B_9 is an odd parity bit for the 7-bit code(B_1~B_7).

† B_{10} is an odd parity bit for the 8-bit code(B_1~B_8).

Note : When inputs DI and PI are low-level, a '1' in the code table indicates that the output level goes high, a '0' that it goes low.

KEYBOARD ENCODER (JIS CODE STANDARD PRODUCT)

CODE ARRANGEMENT TABLE

Kn \ Km	Mode	K2	K3	K4	K5	K6	K7	K8	K9	K10	K11	K12	K13	K14
K1	1	Z	X	C	V	B	N	M	,	.	／		A	S
	2								<	>	?	_		
	3	ツ	サ	ソ	ヒ	コ	ミ	モ	ネ	ル	メ	ロ	チ	ト
	4	ッ							，	。	・			
K2	1		D	F	G	H	J	K	L	;	:	)	Q	W
	2					•				+	*	¦		
	3		シ	ハ	キ	ク	マ	ノ	リ	レ	ケ	ム	タ	テ
	4											」		
K3	1			E	R	T	Y	U	I	O	P	@	「	1
	2										゛	、	」	!
	3			イ	ス	カ	ン	ナ	ニ	ラ	セ	゜	。	ヌ
	4			ィ									「	
K4	1				2	3	4	5	6	7	8	9	0	—
	2				"	#	$	%	&	'	(	)		=
	3				フ	ア	ウ	エ	オ	ヤ	ユ	ヨ	ワ	ホ
	4					ァ	ゥ	ェ	ォ	ャ	ュ	ョ	ヮ	
K5	1					^	¥	DEL	SP	SOH	STX	ETX	EOT	ENQ
	2					~	|	DEL	SP	SOH	STX	ETX	EOT	ENQ
	3					^	~	DEL	SP	SOH	STX	ETX	EOT	ENQ
	4							DEL	SP	SOH	STX	ETX	EOT	ENQ
K6	1						ACK	BEL	BS	HT	LF	VT	FF	CR
	2						ACK	BEL	BS	HT	LF	VT	FF	CR
	3						ACK	BEL	BS	HT	LF	VT	FF	CR
	4						ACK	BEL	BS	HT	LF	VT	FF	CR
K7	1							SO	SI	DLE	DC1	DC2	DC3	NAK
	2							SO	SI	DLE	DC1	DC2	DC3	NAK
	3							SO	SI	DLE	DC1	DC2	DC3	NAK
	4							SO	SI	DLE	DC1	DC2	DC3	NAK
K8	1								SYN	ETB	CAN	EM	SUB	ESC
	2								SYN	ETB	CAN	EM	SUB	ESC
	3								SYN	ETB	CAN	EM	SUB	ESC
	4								SYN	ETB	CAN	EM	SUB	ESC
K9	1									NUL	+	—	=	•
	2									NUL	+	—	=	•
	3									NUL	+	—	=	•
	4									NUL	+	—	=	•
K10	1										1	2	3	4
	2										1	2	3	4
	3										1	2	3	4
	4										1	2	3	4
K11	1											5	6	7
	2											5	6	7
	3											5	6	7
	4											5	6	7
K12	1												8	9
	2												8	9
	3												8	9
	4												8	9
K13	1													0
	2													0
	3													0
	4													0

SYMBOLS AND THEIR NAMES

Symbol	Code name	Col/Row in code table	km/kn/Mode in code arrangement table
SP	Space	2／0	K9 / K5 / 1～4
!	Exclamation mark	2／1	K14 / K3 / 2
"	Quotation mark, umlaut	2／2	K5 / K4 / 2
#	Number sign	2／3	K6 / K4 / 2
$	Dollar sign	2／4	K7 / K4 / 2
%	Percentage	2／5	K8 / K4 / 2
&	Ampersand	2／6	K9 / K4 / 2
'	Apostrophe, acute accent	2／7	K10 / K4 / 2
(	Left parenthesis	2／8	K11 / K4 / 2
)	Right parenthesis	2／9	K12 / K4 / 2
*	Asterisk, multiplication sign	2／10	K11 / K2 / 2
+	Positive sign, plus sign	2／11	K10 / K2 / 2 *
,	Comma	2／12	K9 / K1 / 1
—	Negative sign, subtraction sign	2／13	K14 / K4 / 1 *
.	Period	2／14	K10 / K1 / 1 *
／	Slash, virgule division sign, per	2／15	K11 / K1 / 1
:	Colon	3／10	K11 / K2 / 1
;	Semicolon	3／11	K10 / K2 / 1
<	Less than sign	3／12	K9 / K1 / 2
=	Equal sign	3／13	K14 / K4 / 2 *
>	Greater than sign	3／14	K10 / K4 / 2

* See K11～K14/K9/1～4

Symbol	Code name	Col/Row in code table	km/kn/Mode in code arrangement table
?	Question mark,	3／15	K11 / K1 / 2
@	At mark	4／0	K12 / K3 / 1
[	Left bracket	5／11	K13 / K3 / 1
¥	Yen sign	5／12	K7 / K5 / 1
]	Right bracket	5／13	K12 / K2 / 1
^	Circumflex accent	5／14	K6 / K5 / 1
_	Underline	5／15	K12 / K1 / 2
`	Grave accent	6／0	K12 / K3 / 2
{	Left brace	7／11	K13 / K3 / 2
|	Separate sign, logical add sign	7／12	K7 / K5 / 2
}	Right brace	7／13	K12 / K2 / 2
~	Overline, logical not sign	7／14	K6 / K5 / 2
。	Japanese period	10／1	K10 / K1 / 4
「	Japanese initial quotation mark	10／2	K13 / K3 / 4
」	Japanese final quotation mark	10／3	K12 / K2 / 4
，	Japanese comma	10／4	K9 / K1 / 4
・	Middle dot	10／5	K11 / K1 / 4
ー	Long vowel mark	11／0	K7 / K5 / 3
゛	Voiced consonant mark	13／14	K12 / K3 / 3
゜	Semi-voiced consonant mark	13／15	K13 / K3 / 3

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M58740P, M58740S

Alternative Designation 8255

PROGRAMMABLE PERIPHERAL INTERFACE

DESCRIPTION

The M58740P and M58740S are general-purpose programmable input/output devices designed for use with an 8-bit parallel M58710S CPU as input/output ports. This device are fabricated using N-channel silicon-gate ED-MOS technology for a single supply voltage. They are simple input and output interfaces for TTL circuits, having 24 input/output pins which correspond to three 8-bit input/output ports.

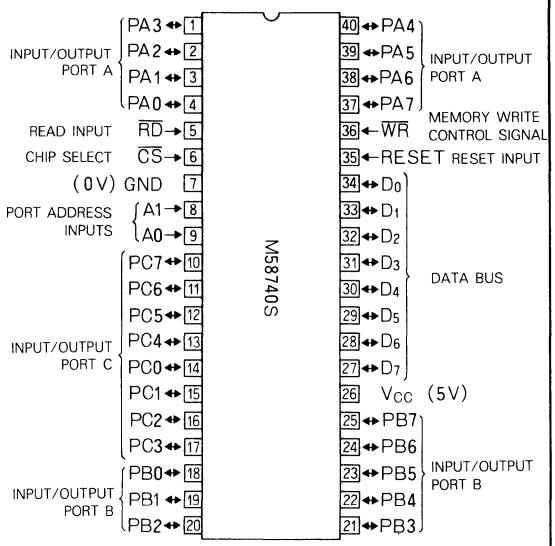
FEATURES

- 24 programmable I/O pins
- Single 5V supply voltage
- TTL-compatible I_{OL} = 1.9mA (max)
- Fully compatible with MELPS 8 microprocessor series
- Direct bit set/reset capability
- A source current of 1mA at 1.5V for Darlington transistor direct drive
- Interchangeable with Intel's 8255 in terms of function, electrical characteristics and pin configuration.

APPLICATION

- Input/output ports for MELPS 8 microprocessor

PIN CONFIGURATION (TOP VIEW)



Outline 40P1 (M58740P)
40S1 (M58740S)

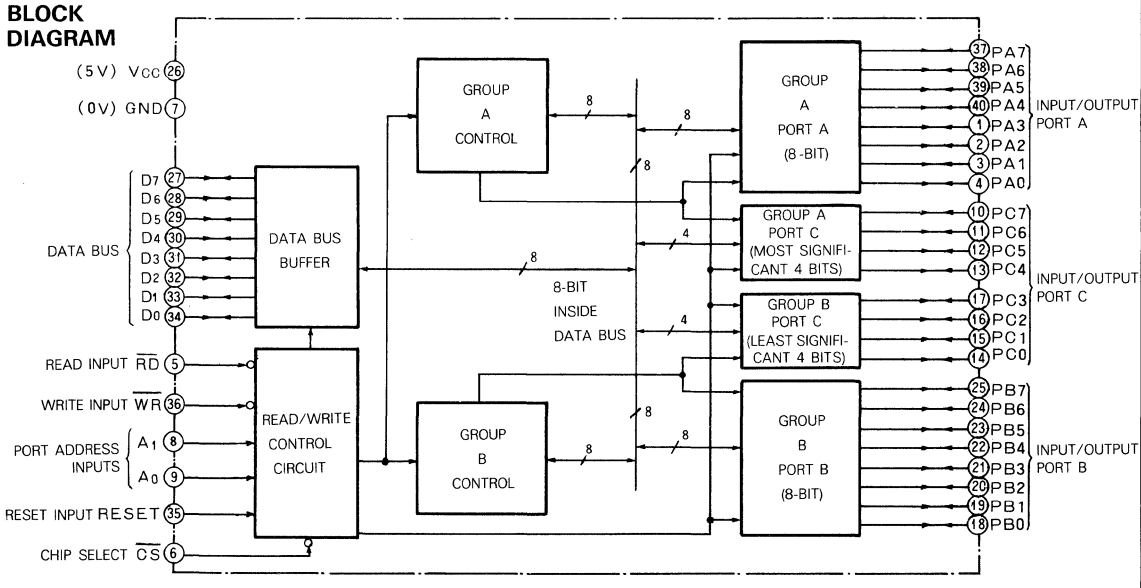
FUNCTION

The M58740P and M58740S have 24 input/output terminals which may be individually programmed in two 12-bit groups A and B with mode control commands from a CPU. It is used in three major modes of operation, mode 0, mode 1 and mode 2.

Operating in mode 0, each group of 12 pins may be programmed in sets of 4 to be inputs or outputs. In mode 1, the 24 I/O terminals may be programmed in two 12-bit groups, group A and group B. Each group contains one 8-bit data port, which may be programmed to be an input or an output, and one 4-bit control-data port used for handshaking and interrupt control signals. Mode 2 is used with group A only, as one 8-bit bidirectional bus port and one 5-bit control port.

Bit set and reset is controlled from a CPU. A high-level reset input (RESET) clears all internal registers, and they are set to the input mode (high-impedance state).

BLOCK DIAGRAM



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PROGRAMMABLE PERIPHERAL INTERFACE

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Conditions	Limits	Unit
V_{CC}	Supply voltage		With respect to V_{SS}	− 0.5～7.0	V
V_I	Input voltage			− 0.5～7.0	V
V_O	Output voltage			− 0.5～7.0	V
P_d	Power dissipation		T_a=25°C	1000	mW
T_{opr}	Operating free-air temperature range			0 ～70	°C
T_{stg}	Storage temperature range	M58740P		−40～125	°C
		M58740S		−65～150	°C

RECOMMENDED OPERATING CONDITIONS (T_a=0～70°C, unless otherwise noted)

Symbol	Parameter	Limit			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V

ELECTRICAL CHARACTERISTICS (T_a=0～70°C, V_{CC}=5V±5%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{OH}	High-level output voltage	V_{SS}=0V, I_{OH}=−50μA (Note 2)	2.4			V
V_{OL}	Low-level output voltage	V_{SS}=0V, I_{OL}=1.9mA			0.4	V
I_{OH}	High-level output voltage (Note 3)	V_{SS}=0V, V_{OH}=1.5V, R_{EXT}=390Ω		2.0		mA
I_{CC}	Supply current from V_{CC}	V_{SS}=0V			60	mA
I_{IH}	High-level input voltage	V_{SS}=0V, V_I=5.25V	−10		10	μA
I_{IL}	Low-level input voltage	V_{SS}=0V, V_I=0V	−10		10	μA
I_{OZ}	Off-state output current	V_{SS}=0V, V_I=0.4～5.25V	−10		10	μA
C_i	Input capacitance	V_{IL}=V_{SS}, f=1MHz, 25mVrms Ta=25°C			10	pF
$C_{i/O}$	Input/output terminal capacitance	$V_{I/OL}$=V_{SS}, f=1MHz, 25mVrms Ta=25°C			15	pF

Note 1 : Current flowing into an IC is positive; out is negative.

2 : I_{OH}=−100μA for D_7 through D_0

3 : It is valid only for any 8 input/output pins.

TIMING REQUIREMENTS (T_a=0～70°C, V_{CC}=5V±5%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
$t_{w(\overline{WR})}$	Write pulse width	450			ns
$t_{su(DA-\overline{WR})}$	Data setup time with respect to write	10			ns
$t_{h(DA-\overline{WR})}$	Data hold time with respect to write	20			ns
$t_{su(AD-\overline{WR})}$	Address setup time with respect to write	35			ns
$t_{h(AD-\overline{WR})}$	Address hold time with respect to write	20			ns
$t_{su(\overline{CS}-\overline{WR})}$	Chip select setup time with respect to write	20			ns
$t_{h(\overline{CS}-\overline{WR})}$	Chip select hold time with respect to write	35			ns
$t_{w(\overline{RD})}$	Read pulse width	430			ns
$t_{su(PE-\overline{RD})}$	Peripheral setup time with respect to read	50			ns
$t_{h(PE-\overline{RD})}$	Peripheral hold time with respect to read	50			ns
$t_{su(AD-\overline{RD})}$	Address setup time with respect to read	50			ns
$t_{h(AD-\overline{RD})}$	Address hold time with respect to read	380			ns
$t_{su(\overline{CS}-\overline{RD})}$	Chip select setup time with respect to read	50			ns
$t_{h(\overline{CS}-\overline{RD})}$	Chip select hold time with respect to read	5			ns
$t_{w(\overline{ACK})}$	Acknowledge pulse width	500			ns
$t_{w(\overline{STB})}$	Strobe pulse width	350			ns
$t_{su(PE-\overline{STB})}$	Peripheral setup time with respect to strobe	150			ns
$t_{h(PE-\overline{STB})}$	Peripheral hold time with respect to strobe	150			ns

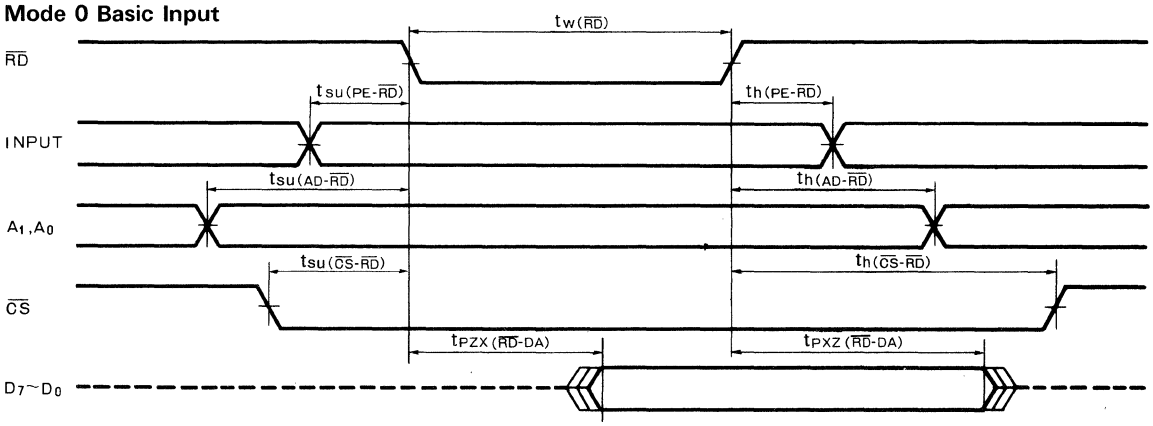
SWITCHING CHARACTERISTICS

(T_a=0~70°C, V_{CC}=5V±5%, oad =50pF 1TTL, unless otherwise noted)

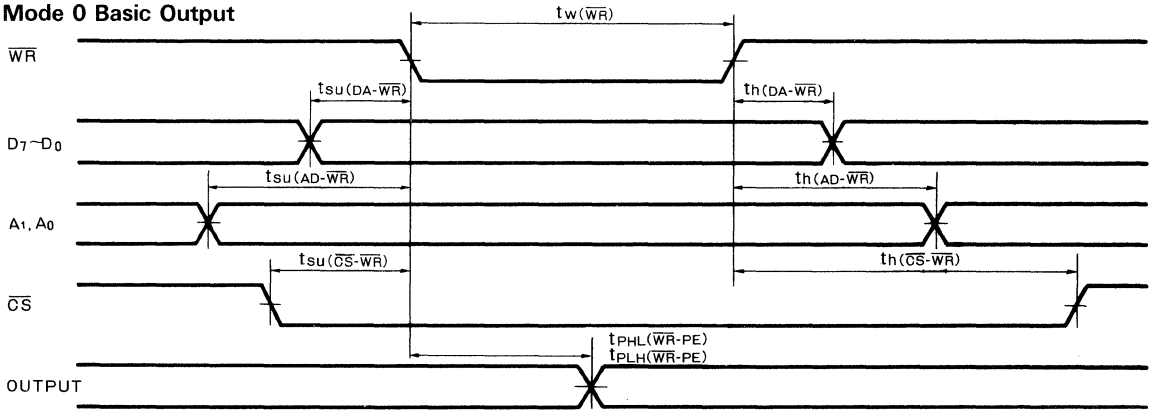
Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
$t_{PHL(\overline{WR}\text{-}PE)}$ $t_{PLH(\overline{WR}\text{-}PE)}$	Propagation time from write to output			500	ns
$t_{PZX(\overline{RD}\text{-}DA)}$	Propagation time from read to output			500	ns
$t_{PXZ(\overline{RD}\text{-}DA)}$	Propagation time from read to output floating			150	ns
$t_{PZX(\overline{ACK}\text{-}PE)}$	Propagation time from acknowledge to output			500	ns
$t_{PXZ(\overline{ACK}\text{-}PE)}$	Propagation time from acknowledge to output floating			350	ns
$t_{PHL(\overline{WR}\text{-}\overline{OBF})}$	Propagation time from write to $\overline{OBF}$ flag			350	ns
$t_{PLH(\overline{ACK}\text{-}\overline{OBF})}$	Propagation time from acknowledge to $\overline{OBF}$ flag			500	ns
$t_{PLH(\overline{STB}\text{-}IBF)}$	Propagation time from strobe to IBF flag			600	ns
$t_{PHL(\overline{RD}\text{-}IBF)}$	Propagation time from read to IBF flag			300	ns

TIMING DIAGRAMS REFERENCE LEVEL =1.5V

Mode 0 Basic Input



Mode 0 Basic Output



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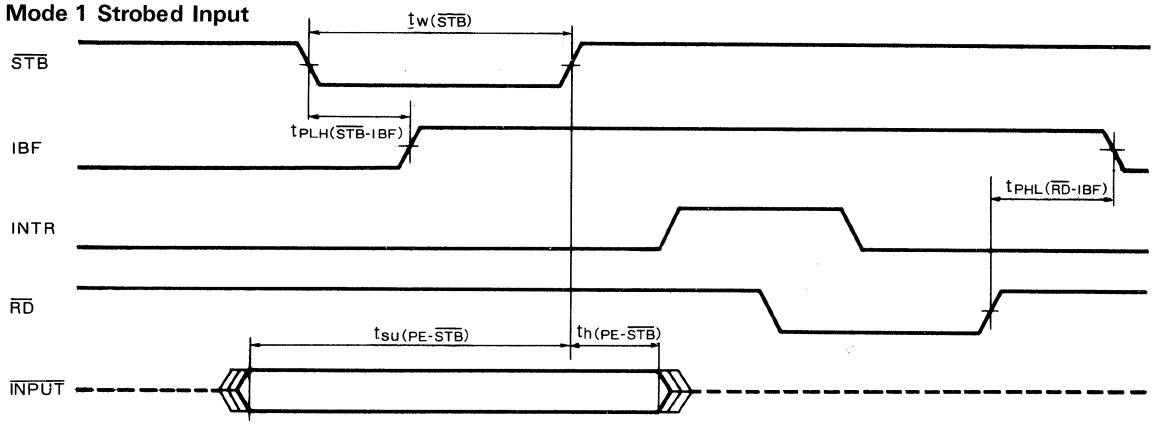
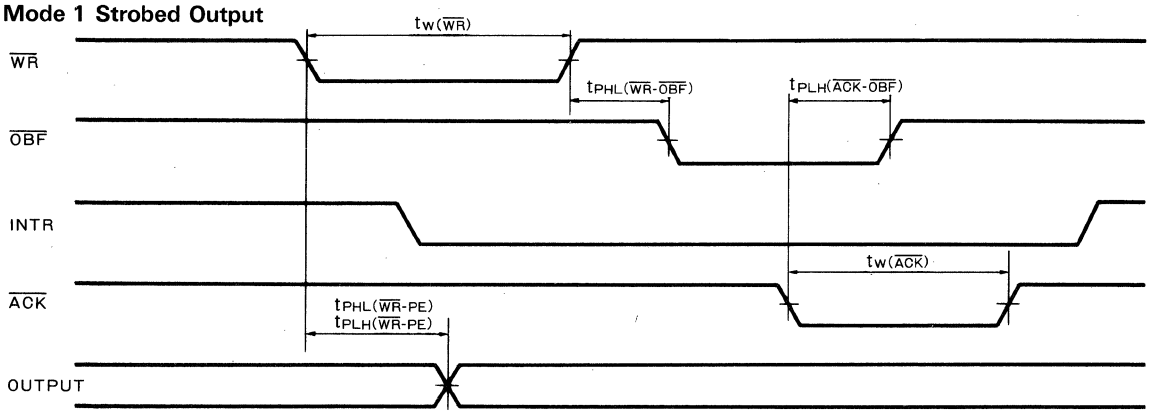
PROGRAMMABLE PERIPHERAL INTERFACE

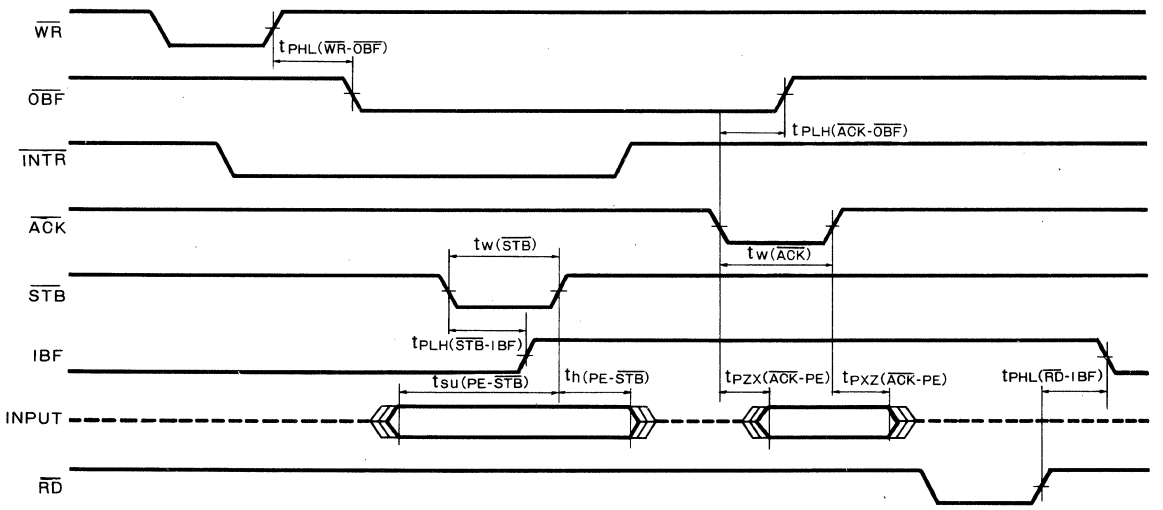
Mode 1 Strobed Input



Mode 1 Strobed Output



Mode 2 Bidirectional



M54550P

Alternative Designation 8224

CLOCK GENERATOR AND DRIVER FOR CPU M58710S

DESCRIPTION

The M54550P is a clock generator/driver for M58710S or 8080A CPUs. It is controlled by a crystal, selected by the user, to meet a variety of system speed requirements. It is fabricated by using Schottky TTL technology.

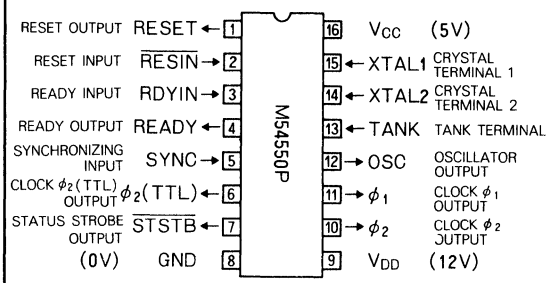
FEATURES

- Crystal controlled for stable clock frequency generation
- Clock outputs ϕ_1, ϕ_2, and ϕ_2(TTL level), and an oscillator output are brought out
- Power-up reset for CPU auto-reset
- Status latch signal
- Synchronizing ready signal output
- Interchangeable with Intel's 8224 in terms of pin configuration and electrical characteristics

APPLICATION

- Single chip clock generator/driver for M58710S and 8080A CPUs

PIN CONFIGURATION (TOP VIEW)



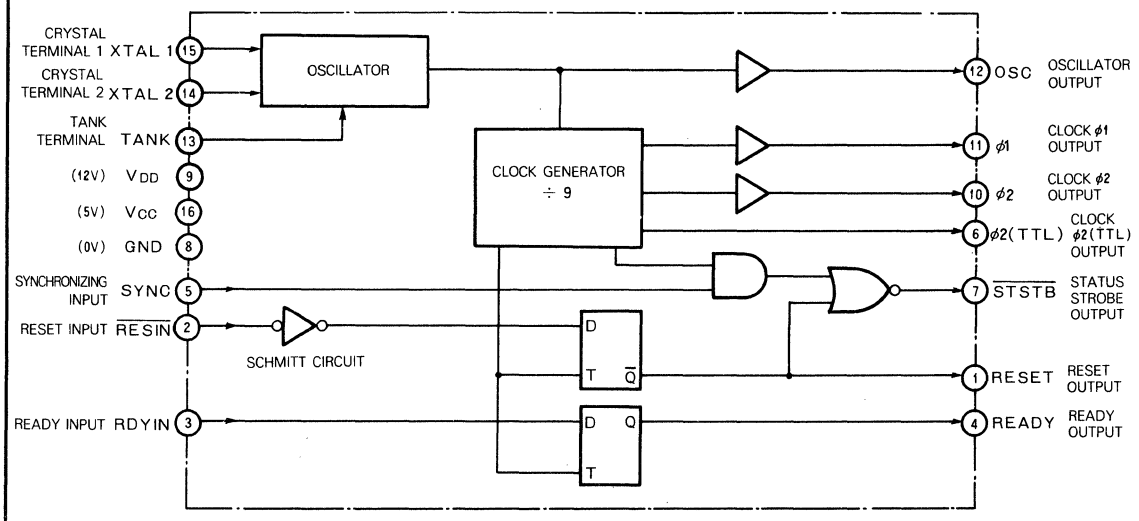
Outline 16P1

FUNCTION

When an 18MHz crystal is connected between XTAL1 and XTAL2, clock outputs ϕ_1, ϕ_2, and ϕ_2(TTL level), along with oscillator output, are brought out for a CPU with a basic cycle time of 500ns. At this time, ϕ_1 pulse width is 110ns (2X55ns), ϕ_2 pulse width is 275ns (5X55ns). When an overtone mode crystal is used, the external LC network is connected to the TANK input to provide additional gain.

If an external RC network is connected to $\overline{\text{RESIN}}$ at system power-up time, a reset signal is generated; and the system is reset automatically. When a signal from a CPU is applied to the SYNC, $\overline{\text{STSTB}}$ is generated. The RDYIN input sends a synchronous "wait request" signal to the internal D-type flip-flop, and a synchronized READY signal is generated.

BLOCK DIAGRAM



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M54550P

Alternative Designation 8224

CLOCK GENERATOR AND DRIVER FOR CPU M58710S

ABSOLUTE MAXIMUM RATINGS (Ta=0~75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		7.0	V
V_{DD}	Supply voltage		13.5	V
V_I	Input voltage		7.0	V
V_O	Output voltage, all outputs except ϕ_1 and ϕ_2		V_{CC}	V
P_d	Power dissipation		800	mW
Topr	Operating free-air temperature range		0~75	°C
Tstg	Storage temperature range		−55~125	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0~75°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	V
V_{DD}	Supply voltage	11.4	12	12.6	V
I_{OH}	High-level output current, $\phi1$, $\phi2$, READY, RESET			−100	μA
I_{OH}	High-level output current, all other outputs			−1	mA
I_{OL}	Low-level output current, $\phi1$, $\phi2$, READY, RESET, $\overline{STSTB}$			2.5	mA
I_{OL}	Low-level output current, all other outputs			16	mA
f_{rmax}	Maximum repetition frequency			27	MHz

ELECTRICAL CHARACTERISTICS (Ta=0~75°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage, $\overline{RESIN}$		2.6			V
V_{IH}	High-level input voltage, all other inputs		2.0			V
V_{IL}	Low-level input voltage				0.8	V
$V_{IH}-V_{IL}$	Input hysteresis voltage, $\overline{RESIN}$	V_{CC}=5.0V, V_{DD}=12.0V	0.25			V
V_{IC}	Input clamped voltage	V_{CC}=4.75V, I_{IC}=−5mA			−1.0	V
V_{OH}	High-level output voltage, $\phi1$, $\phi2$	V_{CC}=4.75V, V_{DD}=11.4V, I_{OH}=−100μA	9.4			V
V_{OH}	High-level output voltage, READY, RESET	V_{CC}=4.75V, V_{DD}=11.4V, I_{OH}=−100μA	3.6			V
V_{OH}	High-level output voltage, other outputs	V_{CC}=4.75V, V_{DD}=11.4V, I_{OH}=−1mA	2.4			V
V_{OL}	Low-level output voltage, $\phi1$, $\phi2$, READY, RESET, $\overline{STSTB}$	V_{CC}=4.75V, V_{DD}=11.4V, I_{OL}=2.5mA			0.5	V
V_{OL}	Low-level output voltage, all other outputs	V_{CC}=4.75V, V_{DD}=11.4V, I_{OL}=16mA			0.5	V
I_{IH}	High-level input current	V_{CC}=5.25V, V_{DD}=12.6V, V_I=5.25V			10	μA
I_{IL}	Low-level input current	V_{CC}=5.25V, V_{DD}=12.6V, V_I=0.5V			−0.25	mA
I_{OS}	Short-circuit output current (Note 3)	V_{CC}=5.0V, V_{DD}=12.0V V_O=0V, V_{IH}=4.5V, V_{IL}=0V	−10		−60	mA
I_{CC}	Supply current from V_{CC}	V_{CC}=5.25V, V_{DD}=12.6V, V_{IH}=4.5V V_{IL}=0V			115	mA
I_{DD}	Supply current from V_{DD}				12	mA

Note 1 : All voltages are with respect to GND terminal. Reference voltage (pin 8) is considered as 0V, and all maximum and minimum values are defined in absolute values.

2 : Current flowing into an IC is positive; out is negative. The maximum and minimum values are defined in absolute values.

3 : All measurements should be done quickly, and two outputs should not be measured at the same time. Outputs $\phi1$ and $\phi2$ should not be short-circuited to GND.

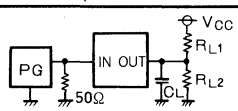
TIMING REQUIREMENTS (Ta=25°C, V_{CC}=5V, V_{DD}=12V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(RDYIN)}$	RDYIN setup time with respect to $\overline{STSTB}$	$\overline{STSTB}$ output terminal C_L=15pF R_{L1}=2kΩ R_{L2}=4kΩ	$50-\frac{4t_C}{9}$			ns
$t_{h(RDYIN)}$	RDYIN hold time with respect to $\overline{STSTB}$		$\frac{4t_C}{9}$			ns

SWITCHING CHARACTERISTICS (Ta=25°C, V_{CC}=5V, V_{DD}=12V, unless otherwise noted)

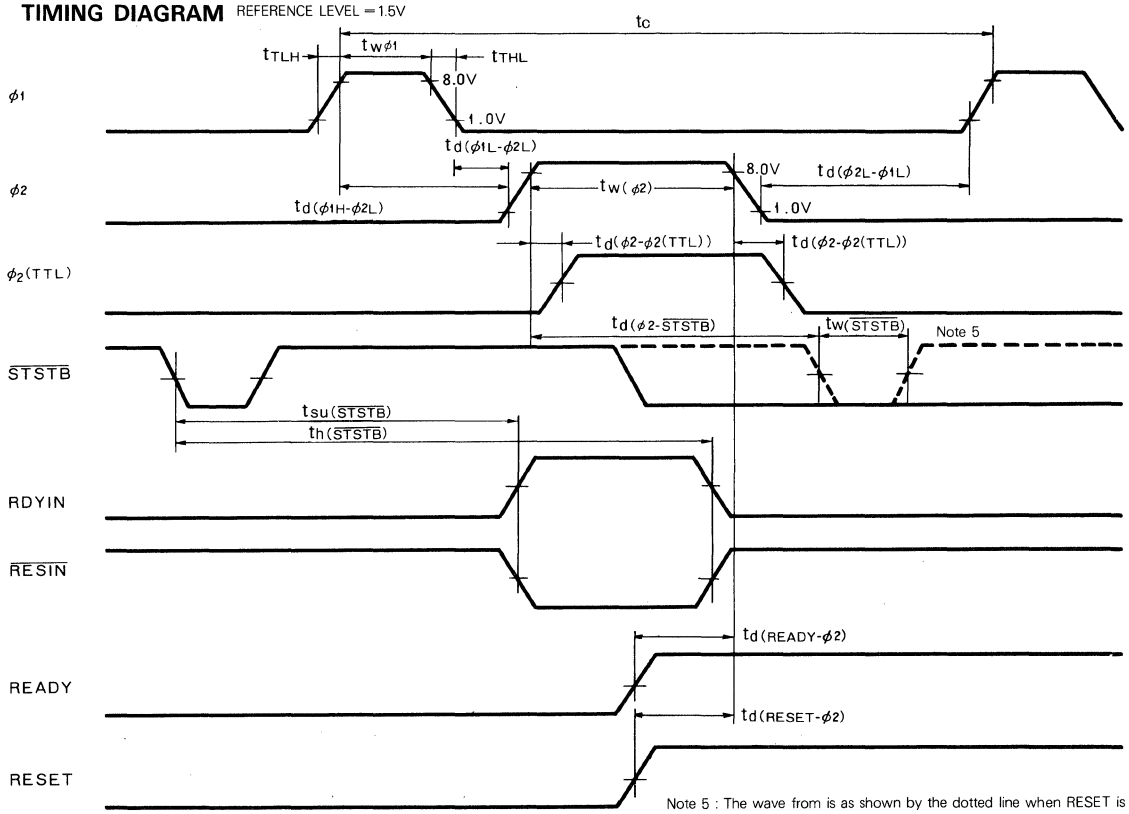
Symbol	Parameter	Test conditions (Note 4)	Limits			Unit
			Min	Typ	Max	
$t_{w(\phi 1)}$	Clock $\phi 1$ pulse width	C_L=20~50pF R_{L1}=∞Ω, R_{L2}=∞Ω	$\frac{2t_C}{9}-20$			ns
$t_{w(\phi 2)}$	Clock $\phi 2$ pulse width		$\frac{5t_C}{9}-35$			ns
$t_{d(\phi 1L-\phi 2L)}$	Delay time from $\phi 1$ low-level to $\phi 2$ low-level		0			ns
$t_{d(\phi 2L-\phi 1L)}$	Delay time from $\phi 2$ low-level to $\phi 1$ low-level		$\frac{2t_C}{9}-30$			ns
$t_{d(\phi 1H-\phi 2L)}$	Delay time from $\phi 1$ high-level to $\phi 2$ low-level		$\frac{2t_C}{9}-5$		$\frac{2t_C}{9}+25$	ns
t_{TLH}	Transition time, low-to-high-level $\phi 1$ and $\phi 2$	C_L=20~50pF			20	ns
t_{THL}	Transition time, high-to-low-level $\phi 1$ and $\phi 2$	R_{L1}=∞Ω, R_{L2}=∞Ω			20	ns
$t_{d(\phi 2-\phi 2(TTL))}$	Delay time from $\phi 2$ to $\phi 2$ (TTL)	$\phi 2$(TTL) output C_L=30pF, R_{L1}=300Ω, R_{L2}=600Ω	−10		20	ns
$t_{d(\phi 2-\overline{STSTB})}$	Delay time from $\phi 2$ to $\overline{STSTB}$	$\overline{STSTB}$ output	$\frac{6t_C}{9}-30$		$\frac{6t_C}{9}$	ns
$t_{w(\overline{STSTB})}$	$\overline{STSTB}$ pulse width	C_L=15pF, R_{L1}=2kΩ, R_{L2}=4kΩ	$\frac{t_C}{9}-15$			ns
$t_{d(READY-\phi 2)}$	Delay time from READY to $\phi 2$	READY, RESET output	$\frac{4t_C}{9}-25$			ns
$t_{d(RESET-\phi 2)}$	Delay time from RESET to $\phi 2$	C_L=10pF, R_{L1}=2kΩ, R_{L2}=4kΩ				

Note 4 : Measurement circuit:



Voltage measurement points:

TIMING DIAGRAM REFERENCE LEVEL = 1.5V



Note 5 : The wave from is as shown by the dotted line when RESET is low.

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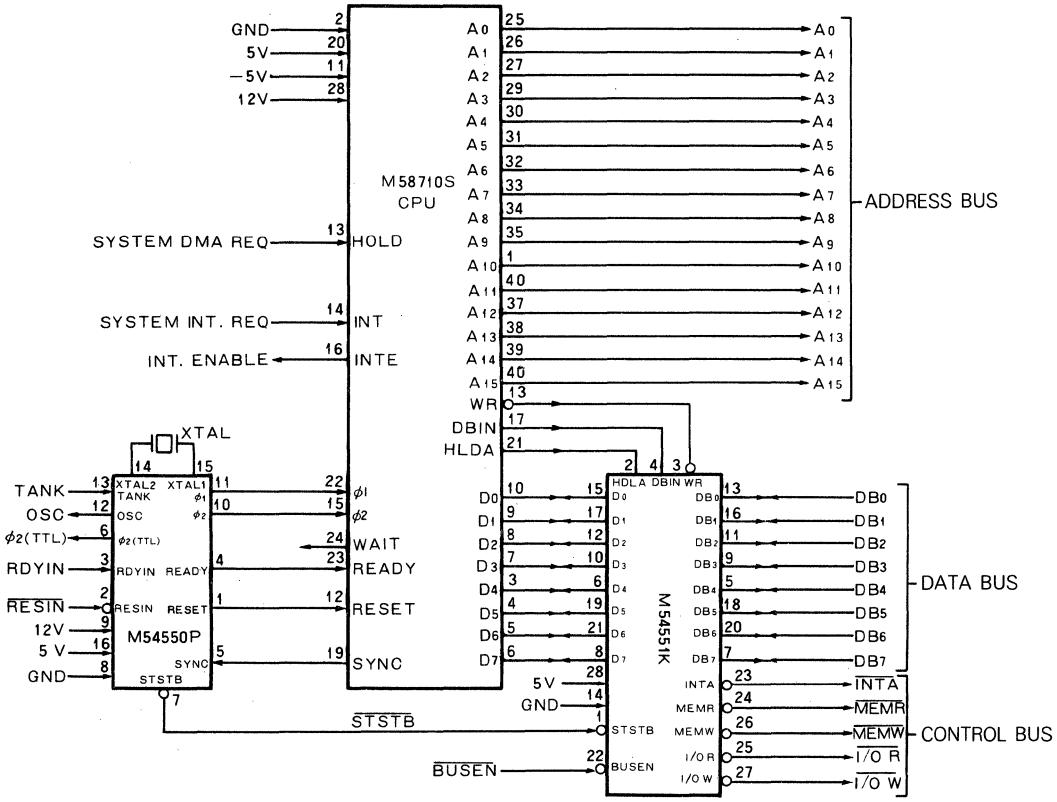
CLOCK GENERATOR AND DRIVER FOR CPU M58710S

TYPICAL APPLICATION CIRCUIT



MITSUBISHI ELECTRIC

SYSTEM CONTROLLER AND BUS DRIVER FOR CPU M58710S

DESCRIPTION

The M54551K is a system controller and bus driver for M58710S or 8080A CPUs. It generates all signals required to directly interface the MELPS 8 series RAMs, ROMs and input/output devices. A bidirectional bus driver, along with system control signals, provides for high system TTL fan-out. It is fabricated using Schottky TTL technology.

FEATURES

- Built-in bidirectional bus driver for data bus isolation
- Built-in status signal
- High system TTL fan-out
- User selected single level interrupt vector (RST 7)
- Interchangeable with Intel's 8228 in terms of pin configuration and electrical characteristics

APPLICATION

- Data bus driver and status signal generation for M58710S and 8080A CPUs

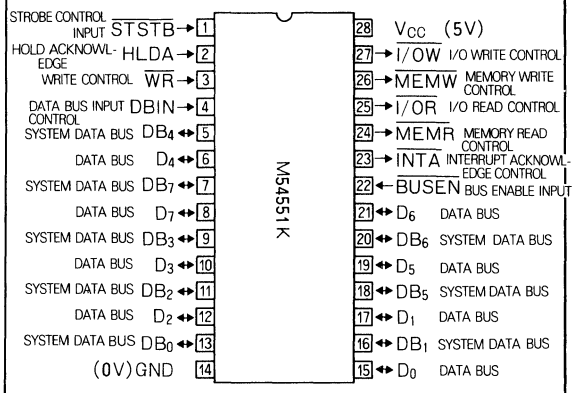
FUNCTION

The bidirectional bus driver provides high system TTL fanout, as well as isolation for an M58710S or 8080A CPU data bus from memory and I/O devices.

Status signals from a CPU are latched in the internal status latch when the status strobe signal $\overline{STSTB}$ goes low. The gating array generates control signals (memory read $\overline{MEMR}$, memory write $\overline{MEMW}$, input/output read $\overline{I/OR}$, input/output write $\overline{I/OW}$, and interrupt acknowledge $\overline{INTA}$) by gating the output of the status latch with the control signals DBIN, $\overline{WR}$ and HLDA from a CPU. The bus enable input $\overline{BUSEN}$ forces the data bus output buffers and control signal buffers to high-impedance state if they are in the high-state.

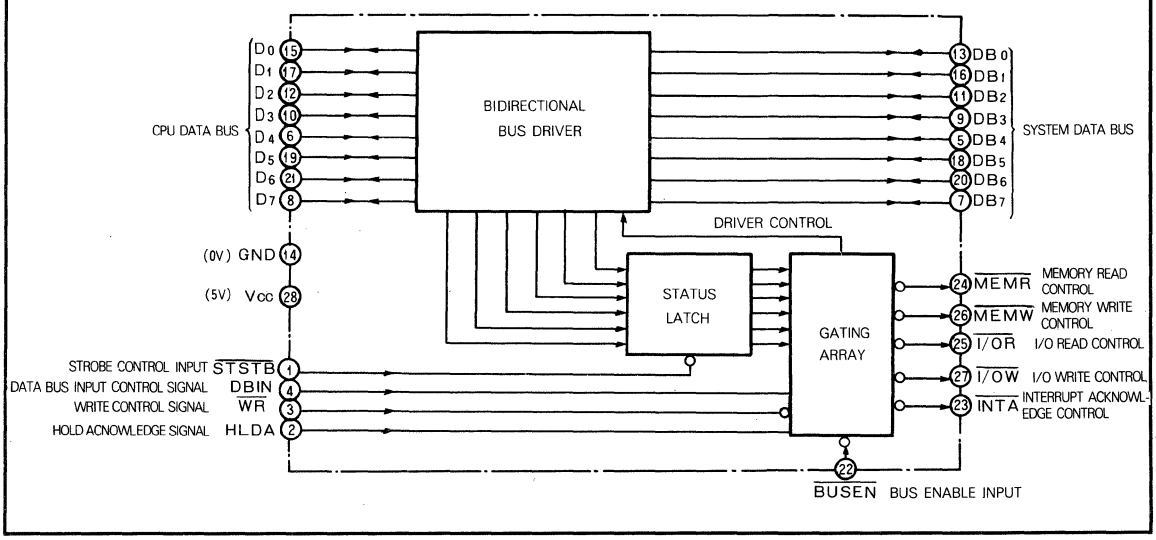
An RST 7 instruction gated to the bus as an interrupt is acknowledged when the DBIN input is active and a 12V supply in series with a 1kΩ resistor is connected to the acknowledge output $\overline{INTA}$.

PIN CONFIGURATION (TOP VIEW)



Outline 28K1

BLOCK DIAGRAM



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M54551K

Alternative Designation 8228

SYSTEM CONTROLLER AND BUS DRIVER FOR CPU M58710S

ABSOLUTE MAXIMUM RATINGS (Ta = 0 ~ 75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		7.0	V
V_I	Input voltage, $D_0 \sim D_7$ and $\overline{STSTB}$ input		V_{CC}	V
V_I	Input voltage, all other inputs		7.0	V
V_O	Output voltage		V_{CC}	V
P_d	Power dissipation		1.0	W
Topr	Operating free-air temperature		0 ~ 75	°C
Tstg	Storage temperature		−55 ~ 125	°C

RECOMMENDED OPERATING CONDITIONS (Ta = 0 ~ 75°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	V
I_{OH}	High-level output current, $D_0 \sim D_7$ outputs			−10	μA
I_{OH}	High-level output current, all other outputs			−1	mA
I_{OL}	Low-level output current, $D_0 \sim D_7$ outputs			2	mA
I_{OL}	Low-level output current, all other outputs			10	mA

ELECTRICAL CHARACTERISTICS (Ta = 0 ~ 75°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
V_{IC}	Input clamp voltage	V_{CC} = 4.75V, I_{IC} = −5mA			−1.0	V
V_{OH}	High-level output voltage, $D_0 \sim D_7$ outputs	V_{CC} = 4.75V, V_{IH} = 2.0V, V_{IL} = 0.8V, I_{OH} = −10μA	3.6			V
	High-level output voltage, all other outputs	V_{CC} = 4.75V, V_{IH} = 2.0V, V_{IL} = 0.8V, I_{OH} = −1mA	2.4			
V_{OL}	Low-level output voltage, $D_0 \sim D_7$ outputs	V_{CC} = 4.75V, V_{IH} = 2.0V, V_{IL} = 0.8V, I_{OL} = 2mA			0.5	V
	Low-level output voltage, all other outputs	V_{CC} = 4.75V, V_{IH} = 2.0V, V_{IL} = 0.8V, I_{OL} = 10mA			0.5	
I_{OZ}	Three-state output current	V_{CC} = 5.25V, V_{IH} = 2.0V, V_{IL} = 0.8V, V_O = 5.25V			20	μA
	Three-state output current	V_{CC} = 5.25V, V_{IH} = 2.0V, V_{IL} = 0.8V, V_O = 0.5V			−20	
I_{IH}	High-level input current, $\overline{STSTB}$ input	V_{CC} = 5.25V, V_{IH} = 4.5V, V_{IL} = 0V, V_I = 5.25V			100	μA
	High-level input current, $DB_0 \sim DB_7$ inputs				20	
	High-level input current, all other inputs				100	
I_{IL}	Low-level input current, $\overline{STSTB}$ input	V_{CC} = 5.25V, V_{IH} = 4.5V, V_{IL} = 0V, V_I = 0.5V			−0.5	mA
	Low-level input current, D_2, D_6 inputs				−0.75	
	Low-level input current, D_0, D_1, D_4, D_5, D_7 inputs				−0.25	
	Low-level input current, all other inputs				−0.25	
I_{OS}	Short-circuit output current (Note 3)	V_{CC} = 5.0V, V_{IH} = 4.5V, V_{IL} = 0V	−15		−90	mA
$I_{I(\overline{INTA})}$	$\overline{INTA}$ terminal current	V_{DD} = 12V, R_L = 1kΩ ±10%			5	mA
I_{CC}	Supply current from V_{CC}	V_{CC} = 5.25V, V_{IH} = 4.5V, V_{IL} = 0V			190	mA

Note 1 : All voltages are with respect to GND terminal. Reference voltage (pin 14) is considered as 0V, and all maximum and minimum values are defined in absolute values.

2 : Current flowing into an IC is positive; out is negative. The maximum and minimum values are defined in absolute values.

3 : All measurements should be done quickly, and two outputs should not be measured at the same time.

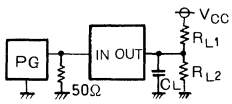
TIMING REQUIREMENTS (Ta = 0 ~ 75°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{w(\overline{STSTB})}$	$\overline{STSTB}$ pulse width		22			ns
$t_{su(DA)}$	$D_0 \sim D_7$ setup time with respect to $\overline{STSTB}$		8			ns
$t_{su(DB)}$	$DB_0 \sim DB_7$ setup time with respect to HLDA		10			ns
$t_{h(DA)}$	$D_0 \sim D_7$ hold time with respect to $\overline{STSTB}$		5			ns
$t_{h(DB)}$	$DB_0 \sim DB_7$ hold time with respect to HLDA		20			ns

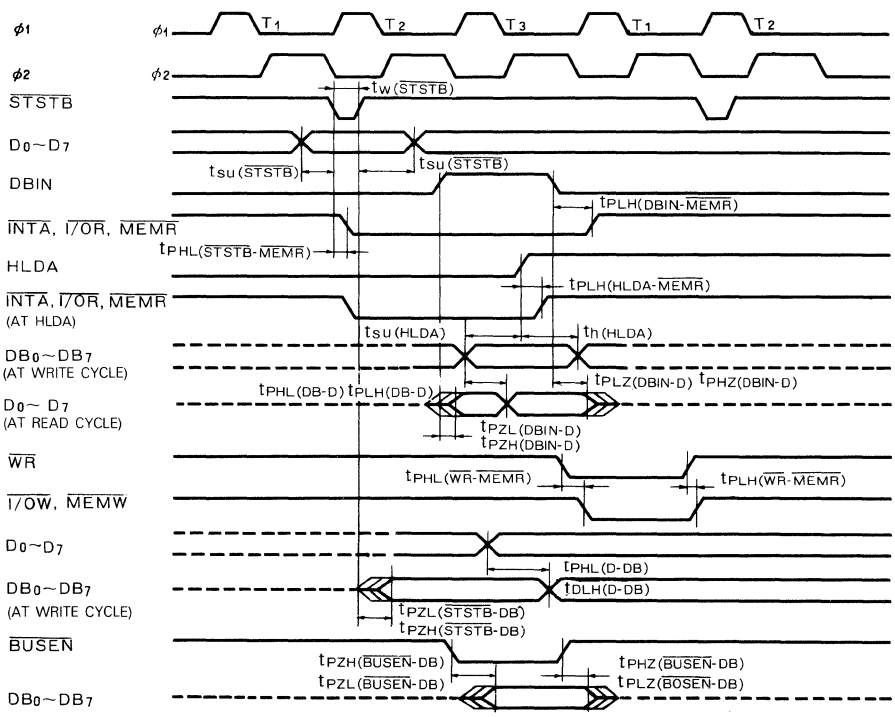
SWITCHING CHARACTERISTICS (Ta = 25°C, V_{CC} = 5V, unless otherwise noted)

Symbol	Parameter	Test conditions (Note 4)	Limits			Unit
			Min	Typ	Max	
$t_{PHL(\overline{STSTB}\text{-}\overline{MEMR})}$	High-to-low-level output propagation time, from input $\overline{STSTB}$ to output $\overline{MEMR}$, $\overline{I/OR}$ and $\overline{INTA}$	V_{IH} = 4.5V, V_{IL} = 0V, C_L = 100pF, R_{L1} = 500Ω, R_{L2} = 1kΩ	20		70	ns
$t_{PLH(DBIN\text{-}\overline{MEMR})}$	Low-to-high-level output propagation time, from input DBIN to output $\overline{MEMR}$, $\overline{I/OR}$ and $\overline{INTA}$				40	ns
$t_{PZL(DBIN\text{-}D)}$ $t_{PZH(DBIN\text{-}D)}$ $t_{PHZ(DBIN\text{-}D)}$ $t_{PLZ(DBIN\text{-}D)}$	Z-to-low-level, Z-to-high-level, high-to-Z-level and low-to-Z-level output propagation time, from input DBIN to outputs $D_0 \sim D_7$	C_L = 25pF, R_{L1} = 4kΩ, R_{L2} = ∞Ω			55	ns
$t_{PHL(DB\text{-}D)}$ $t_{PLH(DB\text{-}D)}$	High-to-low-level and low-to-high-level output propagation time, from inputs $DB_0 \sim DB_7$ to outputs $D_0 \sim D_7$				40	ns
$t_{PHL(\overline{WR}\text{-}\overline{MEMW})}$ $t_{PLH(\overline{WR}\text{-}\overline{MEMW})}$	High-to-low-level and low-to-high-level output propagation time, from input $\overline{WR}$ to outputs $\overline{MEMW}$ and $\overline{I/OW}$	C_L = 100pF, R_{L1} = 500Ω, R_{L2} = 1kΩ	5		55	ns
$t_{PZL(\overline{STSTB}\text{-}DB)}$ $t_{PZH(\overline{STSTB}\text{-}DB)}$	Z-to-low-level and Z-to-high-level output propagation time, from input $\overline{STSTB}$ to outputs $DB_0 \sim DB_7$				40	ns
$t_{PHL(D\text{-}DB)}$ $t_{PLH(D\text{-}DB)}$	High-to-low-level and low-to-high-level output propagation time, from inputs $D_0 \sim D_7$ to outputs $DB_0 \sim DB_7$		5		50	ns
$t_{PZL(\overline{BUSEN}\text{-}DB)}$ $t_{PZH(\overline{BUSEN}\text{-}DB)}$ $t_{PHZ(\overline{BUSEN}\text{-}DB)}$ $t_{PLZ(\overline{BUSEN}\text{-}DB)}$	Z-to-low-level, Z-to-high-level, high-to-Z-level and low-to-Z-level output propagation time, from input $\overline{BUSEN}$ to outputs $DB_0 \sim DB_7$				40	ns
$t_{PLH(HLDA\text{-}\overline{MEMR})}$	Low-to-high-level output propagation time, from input HLDA to outputs $\overline{MEMR}$, $\overline{I/OR}$ and $\overline{INTA}$				35	ns

Note 4 : Measurement circuit:



TIMING DIAGRAM REFERENCE LEVEL = 1.5V



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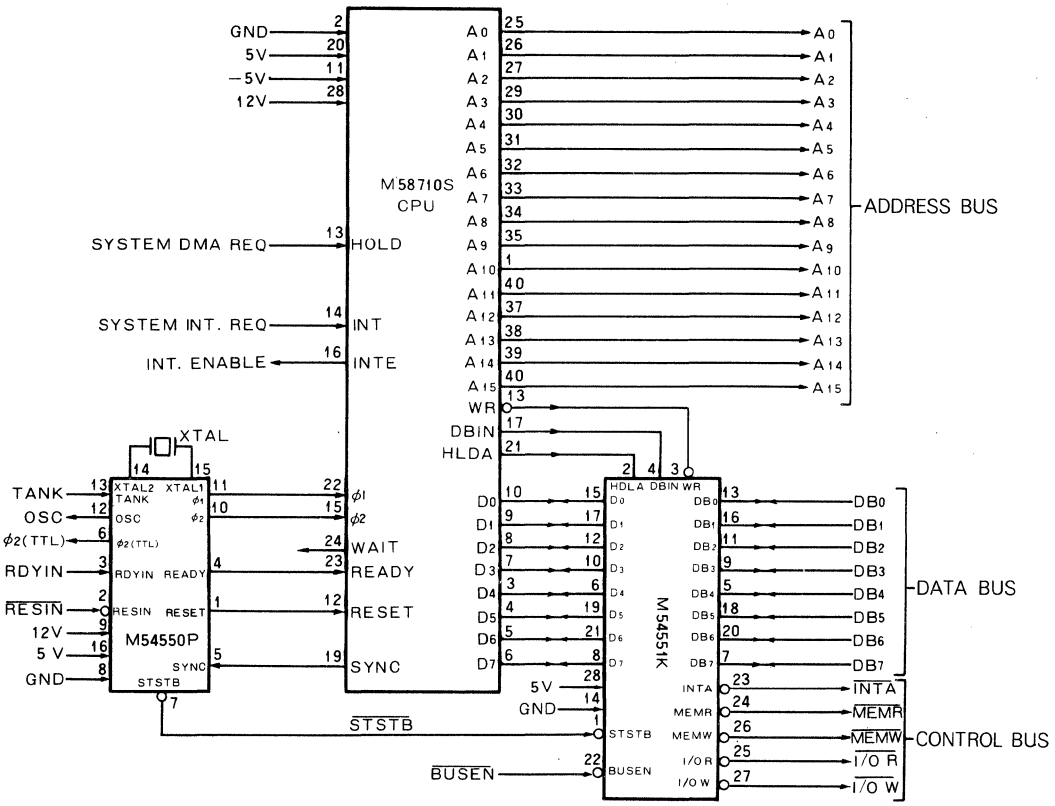
M54551K

Alternative Designation 8228

SYSTEM CONTROLLER AND BUS DRIVER FOR CPU M58710S

TYPICAL APPLICATION CIRCUIT



MITSUBISHI ELECTRIC

8-BIT INPUT/OUTPUT PORT

DESCRIPTION

The M54552P is an input/output port consisting of an 8-bit latch with 3-state output buffers along with control and device selection logic. Also included is a service request flip-flop for the generation and control of interrupts to a microprocessor. It is fabricated using bipolar Schottky TTL technology.

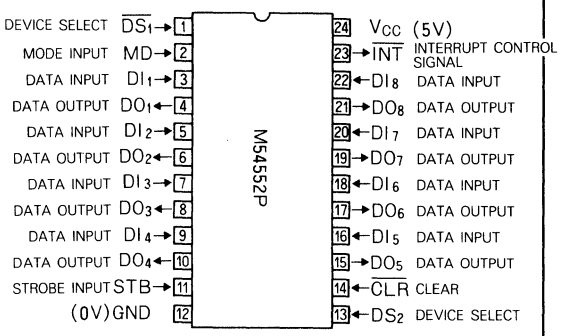
FEATURES

- Parallel 8-bit data register and buffer
- Service request flip-flop for interrupt generation
- Three-state outputs
- Low input load current: I_{IL} = absolute 250μA (max)
- High output sink current: I_{OL} = 16mA (max)
- High-level output voltage for direct interface to a M58710S CPU: V_{OH} = 3.65V (min)
- Interchangeable with Intel's 8212 in terms of electrical characteristics and pin configuration

APPLICATION

- Input/output port for a M58710S CPU
- Latches, gate buffers or multiplexers
- Peripheral and input/output functions for microcomputer systems

PIN CONFIGURATION (TOP VIEW)



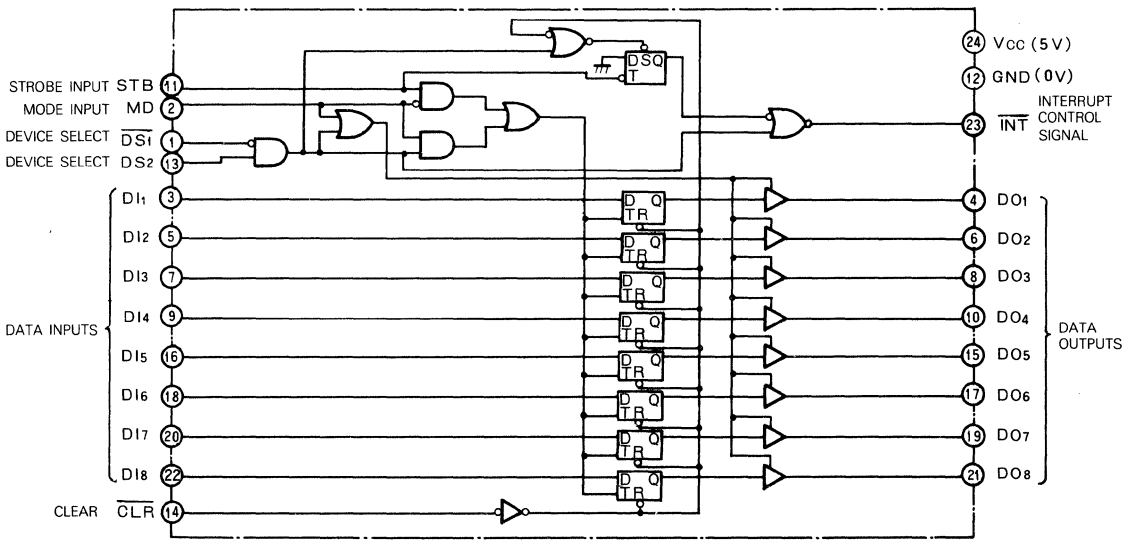
Outline 24P1

FUNCTION

Device select 1 ($\overline{DS_1}$) and device select 2 (DS_2) are used for chip selection when the mode input MD is low. When $\overline{DS_1}$ is low and DS_2 is high, the data in the latches is transferred to the data outputs DO_1~DO_8; and the service request flip-flop SR is set. Also, the strobed input STB is active, the data inputs DI_1~DI_8 are latched in the data latches, and the service request flip-flop SR is reset.

When MD is high, the data in the data latches is transferred to the data outputs. When $\overline{DS_1}$ is low and DS_2 is high, the data inputs are latched in the data latches. The low-level clear input $\overline{CLR}$ resets the data latches and sets the service request flip-flop SR, but the state of the output buffers is not changed.

BLOCK DIAGRAM



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M54552P

Alternative Designation 8212

8-BIT INPUT/OUTPUT PORT

ABSOLUTE MAXIMUM RATINGS (Ta = 0 ~ 75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		7.0	V
V_I	Input voltage, $\overline{DSI}$, MD inputs		V_{CC}	V
V_I	Input voltage, all other inputs except $\overline{DSI}$, MD		5.5	V
V_O	Output voltage		V_{CC}	V
P_d	Power dissipation		800	mW
T_{opr}	Operating free-air temperature range		0 ~ 75	°C
T_{stg}	Storage temperature range		−55 ~ 125	°C

RECOMMENDED OPERATING CONDITIONS (Ta = 0 ~ 75°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	V
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			16	mA

ELECTRICAL CHARACTERISTICS (Ta = 0 ~ 75°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.85	V
V_{IC}	Input clamp voltage	V_{CC} = 4.75V, I_{IC} = −5mA			−1	V
V_{OH}	High-level output voltage	V_{CC} = 4.75V, V_{IH} = 2V, V_{IL} = 0.85V, I_{OH} = −1mA	3.65			V
V_{OL}	Low-level output voltage	V_{CC} = 4.75V, V_{IH} = 2V, V_{IL} = 0.85V, I_{OL} = 16mA			0.5	V
I_{OZ}	Three-state output current	V_{CC} = 5.25V, V_{IH} = 2V, V_{IL} = 0.85V, V_C = 5.25V			20	μA
I_{OZ}	Three-state output current	V_{CC} = 5.25V, V_{IH} = 2V, V_{IL} = 0.85V, V_O = 0.5V			−20	μA
I_{IH}	High-level input current, STB, DS2, $\overline{CLR}$, DI_1 ~ DI_8 inputs	V_{CC} = 5.25V, V_I = 5.25V			10	μA
I_{IH}	High-level input current, MD input	V_{CC} = 5.25V, V_I = 5.25V			30	μA
I_{IH}	High-level input current, $\overline{DS1}$ input	V_{CC} = 5.25V, V_I = 5.25V			40	μA
I_{IL}	Low-level input current, STB, DS2, $\overline{CLR}$, DI_1 ~ DI_8 inputs	V_{CC} = 5.25V, V_I = 0.5V			−0.25	mA
I_{IL}	Low-level input current, MD input	V_{CC} = 5.25V, V_I = 0.5V			−0.75	mA
I_{IL}	Low-level input current, $\overline{DS1}$ input	V_{CC} = 5.25V, V_I = 0.5V			−1	mA
I_{OS}	Short-circuit output current (Note 3)	V_{CC} = 5.25V	−20		−65	mA
I_{CC}	Supply current from V_{CC}	V_{CC} = 5.25V			130	mA

Note 1 : All voltages are with respect to GND terminal. Reference voltage (pin 12) is considered as 0V, and all maximum and minimum values are defined in absolute values.

2 : Current flowing into an IC is positive; out is negative. The maximum and minimum values are defined in absolute values.

3 : All measurements should be done quickly, and two outputs should not be measured at the same time.

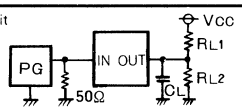
TIMING REQUIREMENTS (Ta = 25°C, V_{CC} = 5 V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{w(DS2)}$	Input pulse width, $\overline{DS1}$, DS2 and STB		30			ns
$t_{w(CLR)}$	Input pulse width $\overline{CLR}$		45			ns
$t_{su(DA)}$	Data setup time with respect to $\overline{DS1}$, DS2 and STB		15			ns
$t_{h(DA)}$	Data hold time with respect to $\overline{DS1}$, DS2 and STB		20			ns

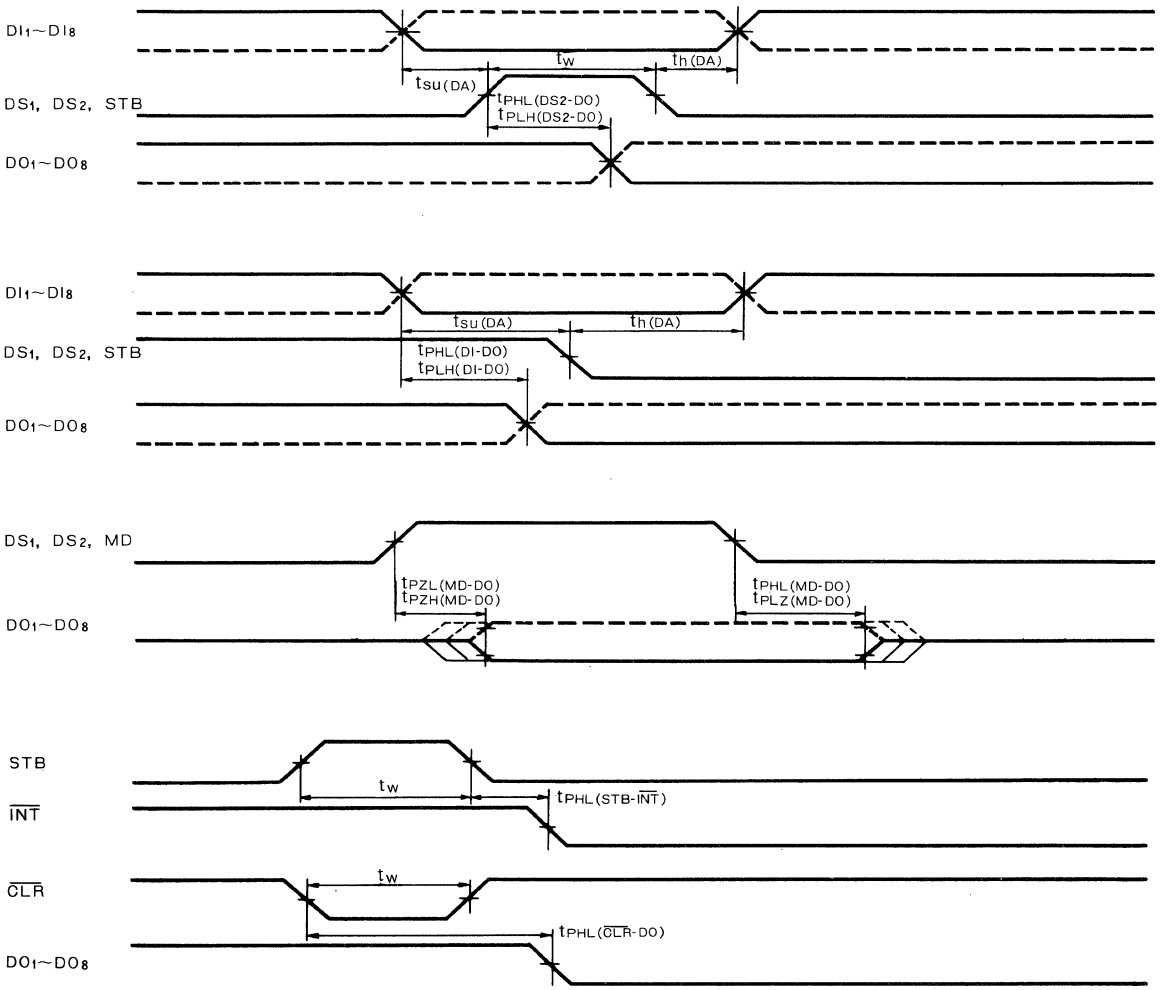
SWITCHING CHARACTERISTICS (Ta = 25°C, V_{CC} = 5V, unless otherwise noted)

Symbol	Parameter	Test conditions (Note 4)	Limits			Unit
			Min	Typ	Max	
$t_{PHL(DI-DO)}$ $t_{PLH(DI-DO)}$	High-to-low-level and low-to-high-level output propagation time, from input DI to output DO	C_L = 30pF, R_{L1} = 300Ω, R_{L2} = 600Ω			35	ns
$t_{PHL(DS2-DO)}$ $t_{PLH(DS2-DO)}$	High-to-low-level and low-to-high-level output propagation time, from inputs $\overline{DS1}$, DS2 and STB to output DO				50	ns
$t_{PHL(STB-\overline{INT})}$	High-to-low-level output propagation time, from input STB to output $\overline{INT}$				40	ns
$t_{PZL(MD-DO)}$ $t_{PZH(MD-DO)}$	Z-to-low-level and Z-to-high-level output propagation time, from inputs MD, $\overline{DS1}$ and DS2 to output DO	C_L = 30pF, R_{L1} = 1kΩ, R_{L2} = 1kΩ			70	ns
$t_{PHZ(MD-DO)}$ $t_{PLZ(MD-DO)}$	High-to-Z-level and low-to-Z-level output propagation time, from inputs MD, $\overline{DS1}$ and DS2 to output DO	C_L = 5pF, R_{L1} = 1kΩ, R_{L2} = 1kΩ			45	ns
$t_{PHL(\overline{CLR}-DO)}$	High-to-low-level output propagation time, from input $\overline{CLR}$ to output DO	C_L = 30pF, R_{L1} = 300Ω, R_{L2} = 600Ω			55	ns

Note 4 : Measurement circuit



TIMING DIAGRAMS REFERENCE LEVEL = 1.5V



8

MELPS SOFTWARE

9

SOFTWARE CODES

SOFTWARE CODES

Software products for Mitsubishi's MELPS microprocessors are designated by the following alphanumeric codes.

1. PROGRAMS

Example: G A 1 AS 0101

- G: Mitsubishi MELPS microprocessor software
- Kind of microprocessor
  - A: MELPS 8 8-bit parallel CPU
  - Z: General
- Operation system
  - 1: For host computer systems
  - 2: For target computer systems
- Kind of program
  - AP: Application program
  - AS: Assembler
  - TL: Compiler
  - SB: Subroutine
  - SM: Simulator
- Identifying serial number

2. MANUALS AND SUPPORT MATERIALS

Example: G A M – SR 00 – 01 A <5 2 B 0>

- G: Mitsubishi MELPS microprocessor software
- Kind of microprocessor
  - A: MELPS 8 8-bit parallel CPU
  - Z: General
- Language
  - E: English
  - M: Japanese
- Kind of Material
  - HR: Hardware manual
  - SR: Software manual or operating manual
  - PS: Program manual
  - SS: Software support materials
  - SH: Consumables
- Identifying serial number
- Availability
  - A: Unrestricted
- Year of issue—last digit, starting from 1976 = 6
- Month of issue
  - 1: January
  - ⋮
  - 9: September
  - X: October
  - Y: November
  - Z: December
- Fully revised edition
  - A: First
  - B: Second
  - etc.
- Partial revision (advance of full revision resets to 0)

AVAILABLE MATERIALS

AVAILABLE MATERIALS

Program	Program code number	Normal shipping media	Source language	Page

HOST COMPUTER PROGRAMS

MELPS 8 PL/Iμ cross compiler on MELCOM 7000 (B-version)	GA1TL 0400	Magnetic tape	FORTRAN Ⅳ	9—7
MELPS 8 cross assembler on MELCOM 70 (A-version)	GA1AS 0100	Magnetic tape	FORTRAN Ⅳ (parts in assembler)	9—11
MELPS 8 simulator on MELCOM 70 (B-version)	GA1SM 0100	Magnetic tape	FORTRAN Ⅳ (parts in assembler)	9—17

Manual	Manual number	Number of pages	Page

PL/Iμ CROSS COMPILER MANUALS

MELPS 8 PL/Iμ Compiler Summary (B-version)	GAM-SR00-07A	70	9-7
MELPS 8 PL/Iμ Compiler Language Manual (B-version)	GAM-SR00-08A	30	9-7
MELPS 8 PL/Iμ Cross Compiler Operating Manual (B-version)	GAM-SR00-09A	51	9-7

CROSS ASSEMBLER MANUALS

MELPS 8 Assembly Language Manual (A-version)	GAM-SR00-01A	83	9-11
MELPS 8 Cross Assembler Operating Manual (A-version)	GAM-SR00-02A	35	9-11

SIMULATOR MANUALS

MELPS 8 Simulator Operating Manual (B-version)	GAM-SR00-03A	35	9-17

HARDWARE MANUALS

MELPS 8 Hardware Manual	GAM-HR00-01A	36	—

GENERAL DESCRIPTION

MELPS 8 software is the name used to designate a software series provided by Mitsubishi for developing application programs or operating systems for equipment in which a MELPS 8 CPU is used.

MELPS 8 software is divided into two parts. The first is software used as a tool to develop application programs, and the second is software used as a part of application programs for MELPS 8 CPUs. MELPS 8 software can also be divided into two classifications: the first, 'host programs', which are developed to run on a host computer; and the second, 'target programs', which are developed to run on a MELPS 8 microcomputer.

SOFTWARE CONFIGURATION

	Language processor	Program debug	Mask ROM automatic generator	Execution computer
Host programs	PL/Iμ Cross compiler Compiles a source program written in PL/Iμ language and produces as output an object program in machine language. The complete Intel PL/M language is a subset of PL/Iμ, therefore, any program written in PL/M can be compiled using a PL/Iμ compiler. Additional functions have been included in PL/Iμ that make it easy to use. Cross assembler Translates a symbolic source program written in assembly language and produces as output an object program in machine language. Parts of a program can be translated and tested, after which they can be combined and linked because the individual outputs are relocatable. This makes it easy to develop modules and then combine them to form a complete program.	Simulator Executes and checks a user's program on the pseudo CPU in a host computer. This allows more efficient program debugging and provides more extensive checking than can be accomplished by hardware. FEATURES: • Provides traces and other debugging aids • Provides simulated I/O operations • Provides simulated interrupt operations • Simplifies program modifications • Provides flexibility for symbolic addresses • Provides data for evaluation of execution time • Batch or conversational processing can be used	Mask read-only memories can be automatically programmed to a customer's specifications. M58730-XXXS 1024-word by 8-bit mask ROM M58731-XXXS 2048-word by 8-bit mask ROM M58609-XXS keyboard encoder M58620-XXXS keyboard encoder The following are automatically generated by a host computer for customized ROMs from data prepared by the customer. 1. The plotter instructions for automatic mask production 2. A check list for verifying that the customer's specifications have been met 3. A test program to assure that the production ROMs meet specifications	• MELCOM 7000 large computer • MELCOM 70 minicomputer It is easy to convert these programs for use on other host computers because they are written in FORTRAN IV and can easily be made transportable.
Target programs	Assembler Translates a source program written in assembly language to an object program written in machine language for execution on the microcomputer. Paper tape is used as the source program input medium. The assembled object program is in MELPS 8 binary object format and is punched out on paper tape. Functions and language specifications of the assembler are included in the specifications of the cross assembler.	Basic operating monitor This is a basic operating monitor program to control execution of a program as well as to facilitate debugging a program. This program has a structure which makes it easy to expand or reduce the functions. The monitor can be used for a MELPS 8 CPU with any memory arrangement or organization. FUNCTIONS • Program execution control • Program debugging • Input/output control • Program loading • Memory readout	General subroutine integer arithmetic operation The M58730-00IS Mask ROM provides arithmetic operations for binary or decimal (16 bits or 32 bits) numbers as well as logical operations. Utility (loader, punch, print) Data can be represented in Three basic forms: 1. MELPS 8 binary 2. Hexadecimal 3. BNPF Input/output control Input/output macroinstructions are used to make it easy for users to develop I/O control sections of their application programs.	• MICROCOMPUTER Microcomputer: MELPS 8 CPUs or other CPUs encompassing the specifications of MELPS 8 CPUs. Memory allocation is free because the programs are relocatable.

DEVELOPMENT OF APPLICATION PROGRAMS

DEVELOPMENT OF APPLICATION PROGRAMS

The user can develop his application programs in any of three ways.

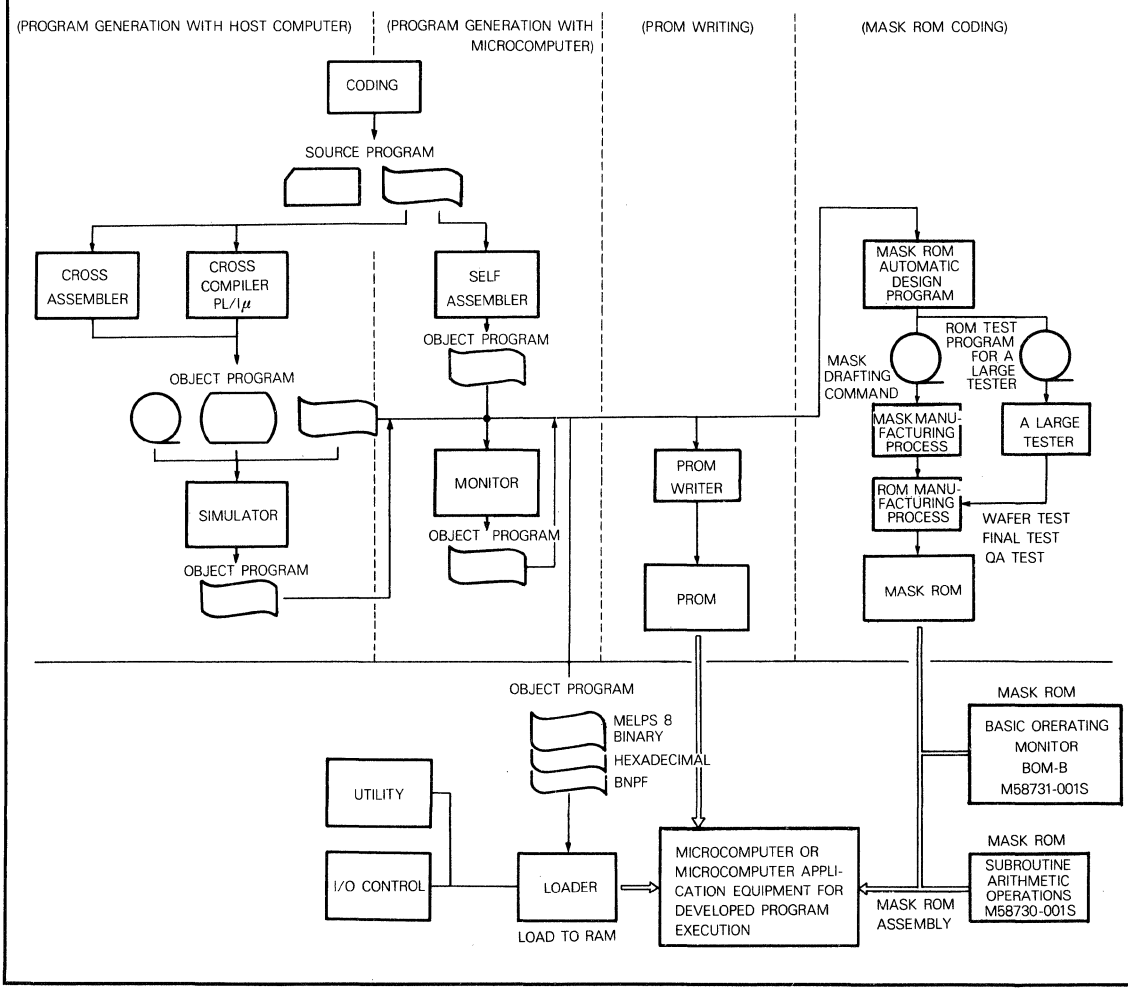
1. On a host computer: the MELPS 8 cross compiler or cross assembler is used for object program generation, and the simulator is used for program debugging.
2. On a microcomputer: the MELPS 8 assembler is used for object program generation, and the microcomputer is used for execution and implementation of programs.
3. On a combination of host computer and microcomputer: object programs are produced by the MELPS 8 cross compiler and/or the MELPS 8 cross assembler on a host computer. The object programs are debugged and implemented on a MELPS 8 microcomputer under control of the basic operating monitor.

The user can develop MELPS 8 programs using general-purpose subroutines for functions such as arithmetic operations, input/output control and logical operations.

Full utilization of these subroutines can facilitate program development, debugging and implementation. The final media of a developed program can be any of the following:

1. Paper tape: there are four basic forms of object programs on paper tape—MELPS 8 binary, simple (IPL) binary, hexadecimal and BNPF. Object programs on paper tape are stored in RAMs and are loaded by the appropriate loader.
2. PROM: the developed program is programmed in a PROM using the PROM writer; then this PROM is installed in the appropriate PROM socket of the microcomputer.
3. Mask ROM: Mitsubishi Electric is ready to produce a mask ROM to a user's specifications. The object program can be in MELPS 8 binary, hexadecimal or BNPF form.

PROGRAM DEVELOPMENT



MELPS 8 PL/Iμ CROSS COMPILER

DESCRIPTION

Mitsubishi supplies this cross compiler on magnetic tape to users of MELPS 8 CPUs. The cross compiler is written in FORTRAN IV for execution on the MELCOM 7000 and can be easily run on other host computers with a FORTRAN IV compiler.

The PL/Iμ language gives MELPS 8 microcomputer users the same advantages that users of mini and large computer systems have with the high level programming languages that are currently available. It has the same language structure as PL/I and has been designed to take advantage of the system architecture of the microprocessor. System designers can use PL/Iμ to quickly and easily implement new applications. In addition, programs written in PL/Iμ are self-documenting so they can be easily changed and maintained. PL/Iμ is recognized as one of the best suited languages for programming microcomputer applications because the user retains the control and efficiency of an assembly language.

FEATURES OF THE PL/Iμ CROSS COMPILER

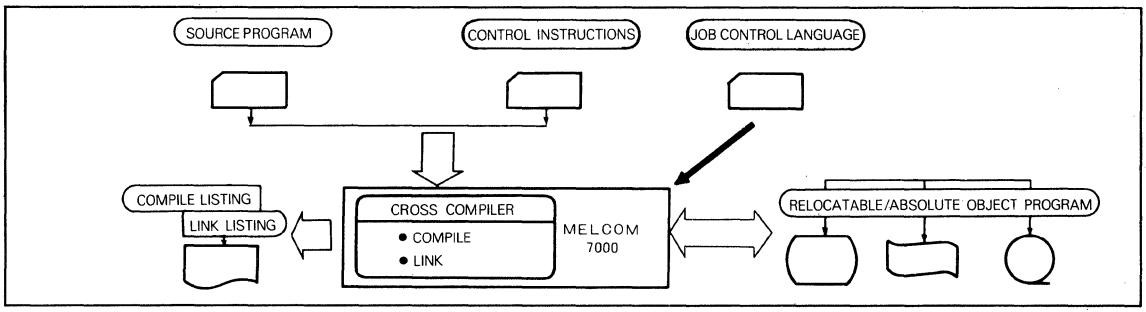
- Conditional compile with preprocessor
- Inline assembly
- Source program editing at compile-time
- Assignment of programs to ROM or RAM regions
- Generates a relocatable object program
- Linking function
- Easily understood error messages
- Flexibility in input/output media
- Execution computer: MELCOM 7000 (BPM/UTS monitor)
- Implementation computer: MELPS 8 microcomputer
- Implementation language: FORTRAN IV

PL/Iμ has a preprocessor that allows user to modify programs under development at compile-time through the use of conditional compile, exchange, exclude and include functions. A program is divided into fixed and variable segments, and these segments are automatically assigned to the appropriate memory (RAM or ROM) during compiling. The link editor can link up to 20 object programs (files).

FEATURES OF THE PL/Iμ LANGUAGE

- Bit operations
- Three-level structure
- One-dimensional arrays
- Allocation of variables to specified absolute addresses
- Multi-entry function
- Interrupt function

Fig. 1 PL/Iμ cross compiler processing system



ORDERING INFORMATION

Programs

Program name	Ordering number	Program and software manuals included	
MELPS 8 PL/Iμ cross compiler	GAITL0400	Source Program	
		MELPS 8 PL/Iμ Compiler Summary Manual (B-version)	GAM-SR00-07A
		MELPS 8 PL/Iμ Compiler Language Manual (B-version)	GAM-SR00-08A
		MELPS 8 PL/Iμ Cross Compiler Operating Manual (B-version)	GAM-SR00-09A
		MELPS 8 MELCOM 7000 PL/Iμ Cross Compiler Operating Manual	GAM-SR00-10A

Reference Manuals for Separate Ordering

Manual name	Manual number
MELPS 8 PL/Iμ Compiler Summary Manual (B-version)	GAM-SR00-07A
MELPS 8 PL/Iμ Compiler Language Manual (B-version)	GAM-SR00-08A
MELPS 8 PL/Iμ Cross Compiler Operating Manual (B-version)	GAM-SR00-09A
MELPS 8 Assembly Language Manual (A-version)	GAM-SR00-01A
MELPS 8 Cross Assembler Operating Manual (A-version)	GAM-SR00-02A
MELPS 8 Simulator Operating Manual (B-version)	GAM-SR00-03A
MELPS 8 Hardware Manual	GAM-HR00-01A

MELPS 8 PL/Iμ CROSS COMPILER

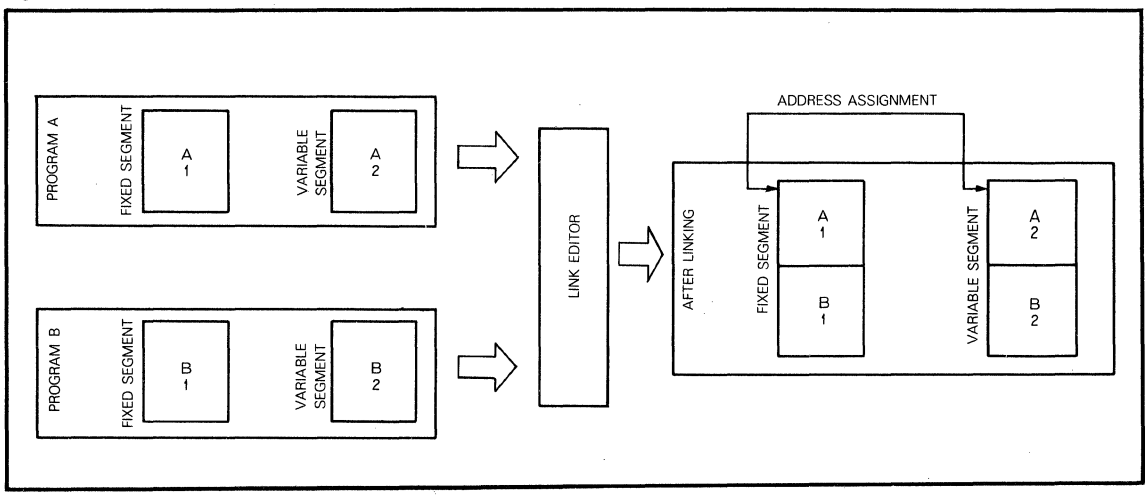
ASSOCIATED FUNCTION

Users of PL/Iμ will find it flexible and easy to use because of its many special features such as the preprocessor, the link editor and the memory manager.

The preprocessor has 10 statements that can be used at compile-time to edit a PL/Iμ source program. These can generate, exchange or delete program text, as well as modify definitions, references and macroinstructions.

The link editor is able to link up to 20 object programs that have been generated by MELPS 8 software. The memory manager divides PL/Iμ programs into fixed and variable segments and assigns the segments to the appropriate memory. A fixed segment is assigned to a non-write area (ROM) while a variable segment is assigned to a write area (RAM) during compiling; at the same time, the starting address of each segment is recorded for linking (see Fig. 2).

Fig. 2 Linking of two programs



PL/Iμ LANGUAGE

The PL/Iμ language is a subset of the popular PL/I language with the addition of special functions to take advantage of the microprocessor's architecture. The main features of the PL/Iμ language are as follows:

Easy to Read and Write

The statements are written in free-format and are independent of columns and lines. The statements are formatted in natural language. It is easy to express, read and understand the programs. Programs written in PL/Iμ are self-documenting.

Block-Structured Language

Programs written in PL/Iμ consist of one or more blocks which are called procedures. A procedure (block) can be thought of as a subroutine. The block structure of PL/Iμ simplifies modular programming. Each procedure can be conceptually simple and, therefore, easy to formulate and debug.

BASIC LANGUAGE SPECIFICATIONS

1. Statements

The basic unit of the PL/Iμ language is called a statement. A procedure (block) is composed of one or more statements, and a program is composed of one or more procedures. The statements are categorized as follows:

Statements	– Procedure definition	:	PROCEDURE statement
	– Declaration	:	DECLARATIVE statement
	– Condition	:	IF statement
	– Non-condition	:	Assignment statement, DO group, and others

The last character of a statement must be a semicolon ';'. A statement may have a label (identifier) which is the name of the statement.

Example **EXAMPLE** : **X**=**Y**+**Z**;

2. Identifiers

PL/Iμ identifiers are used to name variables, procedures, macroinstructions and statements. An identifier may be up to 31 characters in length, and the first character must be an @, ? or alphabetic (A~Z) character. The remaining 30 characters may be alphanumeric (A~Z, 0~9), @ or ?.

Reserved words may not be used as identifiers in the PL/Iμ language.

3. Data Elements

The PL/Iμ data elements represent constants or variables (1–16 bits in length), arrays (1 dimension) and 3-level structure. Constants can be expressed in several different ways in PL/Iμ. PL/Iμ accepts constants in binary, octal, decimal and hexadecimal bases and character strings (ASCII or ISO code).

Example of a PL/Iμ program

```
/* THIS IS A SAMPLE FOR A CATALOG */ ①
DECLARE I BINARY (7),
        FOREVER BINARY (7) INITIAL (1); ②

  /* IF VARIABLE FOREVER IS TRUE, THE STATEMENTS
     UP TO THE CORRESPONDING END ARE EXECUTED */
  DO WHILE FOREVER; ③
    /* READ INPUT PORT 10 AND SAVE IN VARIABLE I */
    I=INPUT (10); ④
    /* THIS VALUE I IS USED TO SELECT ONE OF
       THE STATEMENTS OF DO-CASE TO EXECUTE */
    DO CASE I; ⑤
      /* I=0 */
      DO;
        /* WRITE 8 AT OUTPUT PORT 5 AND HALT */
        OUTPUT (5)=08H; ⑥
        HALT;
        END;
      /* I=1 */
      OUTPUT (5)=80H;
      /* I=2 */
      OUTPUT (5)=40H;
    END;
END;
```

① . Comments are preceded by '/*' and followed by '*/'.

② . The initial value of a type declared variable 'FOREVER' is 1.

③ . DO-WHILE group.

④ . The device number of an input instruction is expressed using a number.

⑤ . DO-CASE group.

⑥ . 08H used in the output instruction indicates a hexadecimal number of value 08_{16}.

MELPS 8 PL/Iμ CROSS COMPILER

LANGUAGE SPECIFICATIONS

Item	Specification
Character set	55-character set Alphabetic: A~Z, Currency unit ($), Numeric: 0~9 Special: = + − * / , . : ; < > % ' ( ) @ ? (blank)
Comments	/* *//
Identifiers	31 or less alphanumeric characters
Reserved words	ADDRESS, ALIGNED, AND, BASED, BINARY, BY, BYTE, CALL, CASE, DATA, DECLARE, DISABLE, DO, ELSE, ENABLE, END, ENTRY, EOF, EXTERNAL, GENERATE, GO, GOTO, HALT, IF, INITIAL, INTERNAL, INTERRUPT, LABEL, LITERALLY, MAIN, MINUS, MOD, NOT, ON, OPTIONS, OR, PLUS, PROCEDURE, RELOCATE, RETURN, THEN, TO, UNALIGNED, WHILE, XOR
Constant types	Binary, octal, decimal, hexadecimal character string
Variable declaration option	BINARY(n) 1≦n≦15、BIT(m) 1≦m≦16 LABEL INITIAL BASED DATA BYTE ADDRESS EXTERNAL INTERNAL ALIGNED UNALIGNED
Operators	* / MOD + − PLUS MINUS < <= <> = >= > NOT AND OR XOR
Arrays	One-dimensional, 1~255 elements
Structures	Three-level, array structure
Expressions	Arithmetical expression, logical expression, structured expression
Statements	Insert statement, CALL statemant, DECLARE statemant, DISABLE statemant, DO group, ENABLE statemant, ENTRY statemant, GENERATE statement, GOTO statement, HALT statement, IF statement, NULL statement, ON statement, PROCEDURE statement, RELOCATE statement, RETURN statemant
DO group	DO WHILE, repeat DO, DO CASE
Library functions	CARRY, DEC, HIGH, INPUT, LAST, LENGTH, LOW, MEMORY, OUTPUT, PARITY, ROL, ROR, SHL, SHR, SIGN, TIME, ZERO
Preprocessor statements	% insert statement, %ACTIVATE statement, %DEACTIVATE statement, %END statement, %EXCLUDE statement, %GOTO statement, %IF statement, %INCLUDE statement, %MACRO statement, %NULL statement

MELPS 8 CROSS ASSEMBLER

DESCRIPTION

This cross assembler is used to convert source programs in assembly language to object programs in MELPS 8 format (8-bit binary format) on a host computer. The assembly language consists of mnemonic instructions (each mnemonic instruction corresponds to a machine language instruction), pseudo instructions and macroinstructions. It is obvious that the assembly language makes programming and modification of programs easy. The pseudo instructions and control commands in this cross assembler give the user flexibility and improve programming efficiency.

FEATURES OF THE CROSS ASSEMBLER

- Generates a relocatable object program
- Linking function
- Multi-assembly
- Conditional assembly
- Flexibility in input/output media
- Output of symbolic table of the object program
- Execution computer: MELCOM 70 (memory capacity more than 24K words, monitor BDOS)
- Implementation language: FORTRAN IV (parts are written in assembly language)

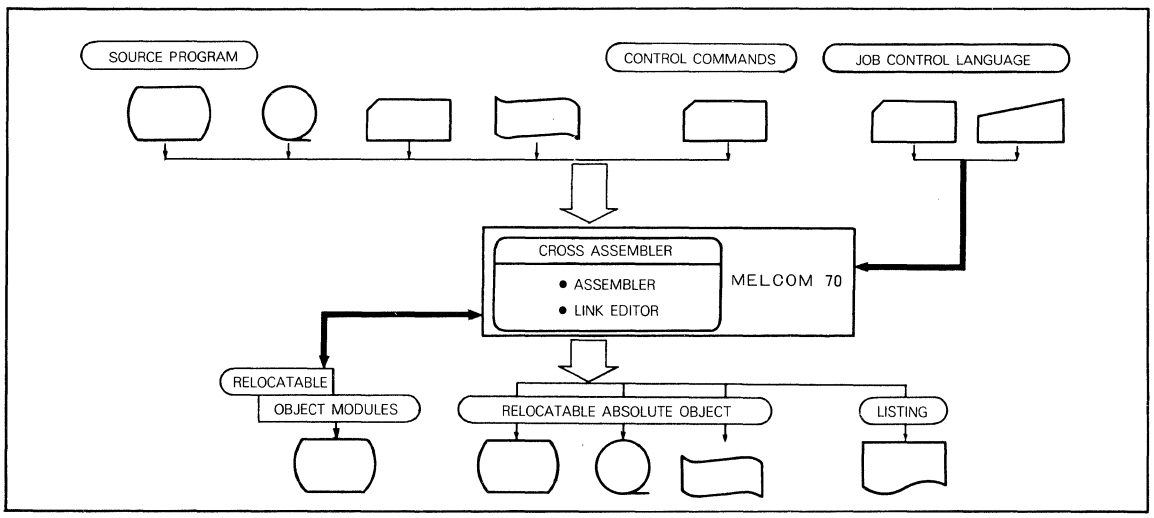
FEATURES OF THE ASSEMBLY LANGUAGE

- 13 pseudo instructions
- Algebraic expressions
- Character constants and strings
- Octal, decimal and hexadecimal numbers
- The mnemonic codes of the machine instructions are the same as Intel's.

INPUT/OUTPUT MEDIA

- Source input : Punched card, paper tape, magnetic tape and magnetic disk
- Object input : Magnetic disk
- Control command input : Punched card
- Object output : Paper tape, magnetic tape and magnetic disk

CROSS ASSEMBLER PROCESSING SYSTEM



ORDERING INFORMATION

Programs

Program name	Ordering number	Program and software manuals included	
MELPS 8 cross assembler	GA1AS0100	Source Program	
		MELPS 8 Assembly Language Manual (A-version)	GAM-SR00-01A
		MELPS 8 Cross Assembler Operating Manual (A-version)	GAM-SR00-02A
		MELPS 8 Cross Assembler & Simulator Operating Manual (on MELCOM 70)	GAM-SR00-04A

Reference Manuals for Separate Ordering

Manual name	Manual number
MELPS 8 Assembly Language Manual (A-version)	GAM-SR00-01A
MELPS 8 Cross Assembler Operating Manual (A-version)	GAM-SR00-02A
MELPS 8 Simulator Operating Manual (B-version)	GAM-SR00-03A
MELPS 8 Hardware Manual	GAM-HR00-01A

9

MELPS 8 CROSS ASSEMBLER

FUNCTION

The control commands and pseudo instructions in this cross assembler give the user flexibility and improve the efficiency of programming. The cross assembler allows linking, multi-assembly and conditional assembly.

The control commands are shown in Table 1, and the features and their limitations are shown in Table 2.

Table 1 List of control commands

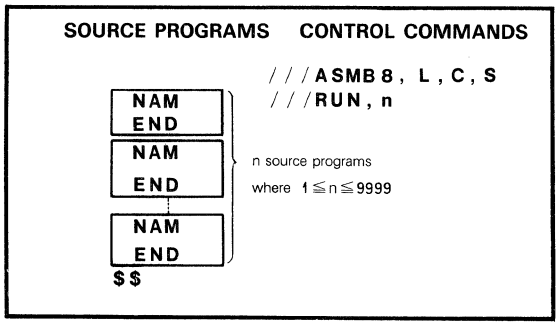
Classification		Control command name	Mnemonic
Assembler control		Execution start	RUN
		End	END
Execution control	Assembly control command	Input/output assignment	ASMB8
		Block assignment	BLOCK
		File assignment	SDISK
			ODISK
			BDISK
	Link control command	Link assignment	LINKG
		Link location assignment	LKLOC

Table 2 Cross assembler features and their limitations

Features	Limitations
Relocatable object programs	
Link editor	Maximum 20 programs on the disk
Program segmented to non-write area (ROM) and write area (RAM)	
Multi-assembly	Maximum 9999 programs
Conditional assembly	Maximum 20 blocks
Flexibility in I/O media selection	Card, disk, paper tape, magnetic tape

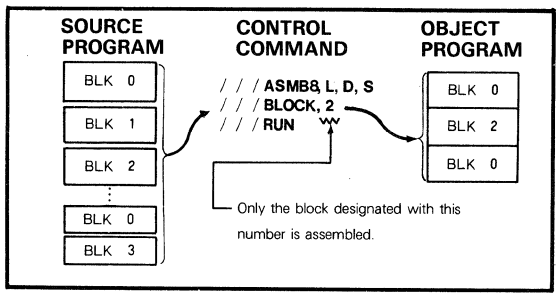
Multi-Assembly

Many programs can be batch-assembled in one run.



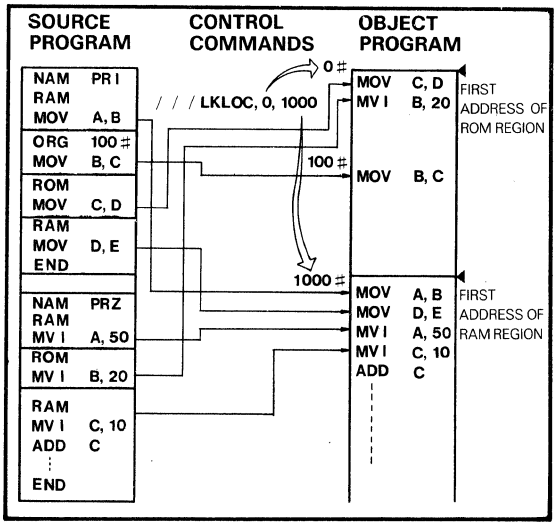
Conditional Assembly

Only the designated blocks of a source program are assembled.



Linking of ROM/RAM regions

ROM and RAM regions are linked separately.



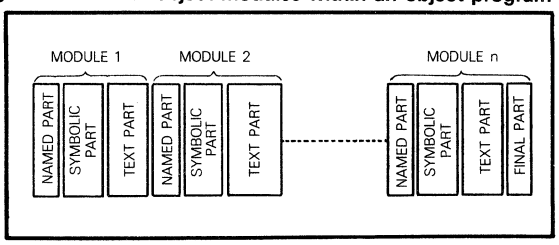
CROSS ASSEMBLER OBJECT PROGRAM

The cross assembler object program is composed of many object modules, and each module is composed of a name, a symbolic part and a text part. A final part ends each object program.

The symbolic part contains the symbolic name corresponding to symbols. It is possible to program using symbolic names because each module contains a symbolic part.

The object is composed of an 8-bit binary code, and one byte of the instruction code is expressed with one character (8 bits).

Fig.1 Structure of object modules within an object program



ASSEMBLY LANGUAGE FUNCTIONS

The assembly language consists of mnemonic instructions (each corresponding to a machine language instruction), pseudo instructions and macroinstructions.

Pseudo instructions are executed by the cross assembler when a source program is being assembled, and they modify the object program. Macroinstructions are converted to small segments of machine instructions that are then inserted in the object program. These inserted segments execute the functions of the macroinstruction.

Algebraic expressions, alphanumeric constants, character strings, octal numbers, decimal numbers, hexadecimal numbers and symbols may be used as an operand in instructions.

1. Machine Instructions:

There are 78 basic machine instructions. These are converted to their corresponding machine language instructions and then inserted in the object program.

A summary of the machine instructions is given in Table 3.

Table 3 Summary of machine instructions

Classification	Instruction functions
Data transfer instructions	Direct data set Between registers Between memory and registers
Addition, subtraction, logical operations and compare instructions	Addition, subtraction, comparing and logical operations using the accumulator together with registers, memory or carry flag
Increment and decrement instructions	Registers, register pairs and memory incremented or decremented
Circulate and shift instructions	Circulate or shift the accumulator's contents
Accumulator adjust instructions	Complement, decimal adjust
Carry instructions	Complement, set
Jump instructions	Unconditional jump Conditional jump
Subroutine call instructions	Unconditional subroutine call Conditional subroutine call
Return instructions	Unconditional return Conditional return
Input/output control instructions	Input and output control
Interrupt control instructions	Enable interrupts Disable interrupts
Stack operation instructions	Saves the contents of registers Restores the contents of registers
Others	CPU halt No operation

2. Pseudo Instructions

Pseudo instructions control the execution of the cross assembler while source programs are being assembled. They are not assembled as instructions in the object programs. As shown in Table 4, there are 13 pseudo instructions.

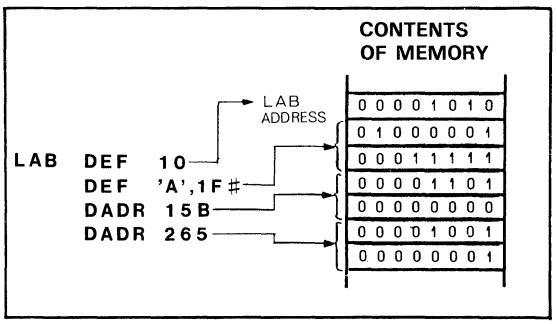
Table 4 List of pseudo instructions

Classification	Instruction mnemonic symbols	Names of instructions
Assembler control instructions	**NAM**	Program name declaration
	ORG	Program counter setting
	ROM	ROM region declaration
	RAM	RAM region declaration
	BLK	Block declaration
	END	End declaration
Link symbol assignment instructions	**ENT**	Entry name declaration
	EXT	External reference symbol declaration
Memory contents Definition instructions	**EQU**	Value symbol setting
	DEF*	Data setting
	DADR*	Address setting
Storage allocation instructions	**BSS****	Storage allocation
List control instructions	**EJE**	Page eject declaration

* DEF and DADR pseudo instructions set the data or the address in the memory location where the instruction is. See Fig. 2.

** BSS pseudo instruction sets the program counter to the value of the operand.

Fig. 2 Example of DEF and DADR pseudo instructions



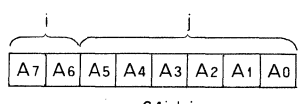
3. Macroinstructions

Macroinstructions are converted to object program segments in machine language that executes the macroinstruction functions. The following two macroinstructions are included in this cross assembler.

Table 5 Macroinstructions

Instructions	Name	Corresponding statement
GET i , j	Data input instruction	**IN n**
PUT i , j	Data output instruction	**OUT n**

where



n=64i+j

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MACHINE INSTRUCTIONS

Instr. classi.	Mnemonic	Instruction code D7 D6	D5 D4 D3	D2 D1 D0	16mal notan	No. of states	No. of bytes	No. of cycles	Functions	Flags S	Z	P	CY2	CY1	Address bus Contents	Mach. cycle *	Data bus Contents	I/O	Mach. cycle †
Data transfer	MOV r1, r2	0 1	D D D	S S S		5	1	1	(r1) ← (r2)	X	X	X	X	X					
	MOV M, r	0 1	1 1 0	S S S		7	1	2	(M) ← (r) Where, M = (H) (L)	X	X	X	X	X	M	M4	(r)	O	M4
	MOV r, M	0 1	D D D	1 1 0		7	1	2	(r) ← (M) Where, M = (H) (L)	X	X	X	X	X	M	M4	(M)	I	M4
	MVI r, n	0 0	D D D	1 1 0		7	2	2	(r) ← n	X	X	X	X	X			<B2>	I	M4
			<B2>																
	MVI M, n	0 0	1 1 0	1 1 0	3 6	10	2	3	(M) ← n Where, M = (H) (L)	X	X	X	X	X	M	M5	<B2>	I	M5
			<B2>																
	LXI B, m	0 0	0 0 0	0 0 1	0 1	10	3	3	(C) ← <B2>	X	X	X	X	X			<B2>	I	M2
			<B2>						(B) ← <B3> Where, m = <B3> <B2>								<B3>	I	M3
			<B3>																
	LXI D, m	0 0	0 1 0	0 0 1	1 1	10	3	3	(E) ← <B2>	X	X	X	X	X			<B2>	I	M2
			<B2>						(D) ← <B3> Where, m = <B3> <B2>								<B3>	I	M3
			<B3>																
	LXI H, m	0 0	1 0 0	0 0 1	2 1	10	3	3	(L) ← <B2>	X	X	X	X	X			<B2>	I	M2
			<B2>						(H) ← <B3> Where, m = <B3> <B2>								<B3>	I	M3
			<B3>																
	LXI SP, m	0 0	1 1 0	0 0 1	3 1	10	3	3	(SP) ← m	X	X	X	X	X			<B2>	I	M2
			<B2>														<B3>	I	M3
			<B3>																
	SPHL	1 1	1 1 1	0 0 1	F 9	5	1	1	(SP) ← (H) (L)	X	X	X	X	X					
	STAX B	0 0	0 0 0	0 1 0	0 2	7	1	2	((B) (C)) ← (A)	X	X	X	X	X	(B) (C)	M4	(A)	O	M4
	STAX D	0 0	0 1 0	0 1 0	1 2	7	1	2	((D) (E)) ← (A)	X	X	X	X	X	(D) (E)	M4	(A)	O	M4
	LDAX B	0 0	0 0 1	0 1 0	0 A	7	1	2	(A) ← ((B) (C))	X	X	X	X	X	(B) (C)	M4	((B) (C))	I	M4
	LDAX D	0 0	0 1 1	0 1 0	1 A	7	1	2	(A) ← ((D) (E))	X	X	X	X	X	(D) (E)	M4	((D) (E))	I	M4
	STA m	0 0	1 1 0	0 1 0	3 2	13	3	4	(m) ← (A)	X	X	X	X	X	m	M4	(A)	O	M4
			<B2>																
			<B3>																
	LDA m	0 0	1 1 1	0 1 0	3 A	13	3	4	(A) ← (m)	X	X	X	X	X	m	M4	(m)	I	M4
			<B2>																
			<B3>																
	SHLD m	0 0	1 0 0	0 1 0	2 2	16	3	5	(m) ← (L)	X	X	X	X	X	m	M4	(L)	O	M4
			<B2>						(m+1) ← (H)						m+1	M5	(H)	O	M5
			<B3>																
	LHLD m	0 0	1 0 1	0 1 0	2 A	16	3	5	(L) ← (m)	X	X	X	X	X	m	M4	(m)	I	M4
			<B2>						(H) ← (m+1)						m+1	M5	(m+1)	I	M5
			<B3>																
	XCHG	1 1	1 0 1	0 1 1	E B	4	1	1	(H) (L) ↔ (D) (E)	X	X	X	X	X					
	XTHL	1 1	1 0 0	0 1 1	E 3	18	1	5	(H) (L) ↔ ((SP)+1) ((SP))	X	X	X	X	X	(SP)	M2	((SP))	I	M2
															(SP)+1	M3	((SP)+1)	I	M3
Arithmetic, logical, compare	ADD r	1 0	0 0 0	S S S		4	1	1	(A) ← (A) + (r)	O	O	O	O	O					
	ADD M	1 0	0 0 0	1 1 0	8 6	7	1	2	(A) ← (A) + (M) Where, M = (H) (L)	O	O	O	O	O	M	M4	(M)	I	M4
	ADI n	1 1	0 0 0	1 1 0	C 6	7	2	2	(A) ← (A) + n	O	O	O	O	O			<B2>	I	M4
			<B2>																
	ADC r	1 0	0 0 1	S S S		4	1	1	(A) ← (A) + (r) + (CY2)	O	O	O	O	O					
	ADC M	1 0	0 0 1	1 1 0	8 E	7	1	2	(A) ← (A) + (M) + (CY2) Where, M = (H) (L)	O	O	O	O	O	M	M4	(M)	I	M4
	ACI n	1 1	0 0 1	1 1 0	C E	7	2	2	(A) ← (A) + n + (CY2)	O	O	O	O	O			<B2>	I	M4
			<B2>																
	DAD B	0 0	0 0 1	0 0 1	0 9	10	1	3	(H) (L) ← (H) (L) + (B) (C)		X			O	X				
	DAD D	0 0	0 1 1	0 0 1	1 9	10	1	3	(H) (L) ← (H) (L) + (D) (E)		X			O	X				
	DAD H	0 0	1 0 1	0 0 1	2 9	10	1	3	(H) (L) ← (H) (L) + (H) (L)		X			O	X				
	DAD SP	0 0	1 1 1	0 0 1	3 9	10	1	3	(H) (L) ← (H) (L) + (SP)		X			O	X				
	SUB r	1 0	0 1 0	S S S		4	1	1	(A) ← (A) − (r)	O	O	O	O	O					
	SUB M	1 0	0 1 0	1 1 0	9 6	7	1	2	(A) ← (A) − (M) Where, M = (H) (L)	O	O	O	O	O	M	M4	(M)	I	M4
	SUI n	1 1	0 1 0	1 1 0	D 6	7	2	2	(A) ← (A) − n	O	O	O	O	O			<B2>	I	M4
			<B2>																
	SBB r	1 0	0 1 1	S S S		4	1	1	(A) ← (A) − (r) − (CY2)	O	O	O	O	O					
	SBB M	1 0	0 1 1	1 1 0	9 E	7	1	2	(A) ← (A) − (M) − (CY2) Where, M = (H) (L)	O	O	O	O	O	M	M4	(M)	I	M4
	SBI n	1 1	0 1 1	1 1 0	D E	7	2	2	(A) ← (A) − n − (CY2)	O	O	O	O	O			<B2>	I	M4
			<B2>																
	ANA r	1 0	1 0 0	S S S		4	1	1	(A) ← (A) ∧ (r)	O	O	O	0	O					
	ANA M	1 0	1 0 0	1 1 0	A 6	7	1	2	(A) ← (A) ∧ (M) Where, M = (H) (L)	O	O	O	0	O	M	M4	(M)	I	M4
	ANI n	1 1	1 0 0	1 1 0	E 6	7	2	2	(A) ← (A) ∧ n	O	O	O	0	O			<B2>	I	M4
			<B2>																
	XRA r	1 0	1 0 1	S S S		4	1	1	(A) ← (A) ∀ (r)	O	O	O	0	0					
	XRA M	1 0	1 0 1	1 1 0	A E	7	1	2	(A) ← (A) ∀ (M) Where, M = (H) (L)	O	O	O	0	0	M	M4	(M)	I	M4
	XRI n	1 1	1 0 1	1 1 0	E E	7	2	2	(A) ← (A) ∀ n	O	O	O	0	0			<B2>	I	M4
			<B2>																
	ORA r	1 0	1 1 0	S S S		4	1	1	(A) ← (A) ∨ (r)	O	O	O	0	0					
	ORA M	1 0	1 1 0	1 1 0	B 6	7	1	2	(A) ← (A) ∨ (M) Where, M = (H) (L)	O	O	O	0	0	M	M4	(M)	I	M4
	ORI n	1 1	1 1 0	1 1 0	F 6	7	2	2	(A) ← (A) ∨ n	O	O	O	0	0			<B2>	I	M4
			<B2>																
	CMP r	1 0	1 1 1	S S S		4	1	1	(A) − (r)	O	O	O	O	O					
	CMP M	1 0	1 1 1	1 1 0	B E	7	1	2	(A) − (M) Compare; Where, M = (H) (L)	O	O	O	O	O	M	M4	(M)	I	M4
	CPI n	1 1	1 1 1	1 1 0	F E	7	2	2	(A) − n	O	O	O	O	O			<B2>	I	M4
			<B2>																
Register increment/Decrement	INR r	0 0	D D D	1 0 0		5	1	1	(r) ← (r) + 1	O	O	O	X	O					
	INR M	0 0	1 1 0	1 0 0	3 4	10	1	3	(M) ← (M) + 1 Where, M = (H) (L)	O	O	O	X	O	M	M4	(M)	I	M4
	DCR r	0 0	D D D	1 0 1		5	1	1	(r) ← (r) − 1	O	O	O	X	O					
	DCR M	0 0	1 1 0	1 0 1	3 5	10	1	3	(M) ← (M) − 1 Where, M = (H) (L)	O	O	O	X	O	M	M4	(M)	I	M4
	INX B	0 0	0 0 0	0 1 1	0 3	5	1	1	(B) (C) ← (B) (C) + 1	X	X	X	X	X					
	INX D	0 0	0 1 0	0 1 1	1 3	5	1	1	(D) (E) ← (D) (E) + 1	X	X	X	X	X					
	INX H	0 0	1 0 0	0 1 1	2 3	5	1	1	(H) (L) ← (H) (L) + 1	X	X	X	X	X					
	INX SP	0 0	1 1 0	0 1 1	3 3	5	1	1	(SP) ← (SP) + 1	X	X	X	X	X					
	DCX B	0 0	0 0 1	0 1 1	0 B	5	1	1	(B) (C) ← (B) (C) − 1	X	X	X	X	X					
	DCX D	0 0	0 1 1	0 1 1	1 B	5	1	1	(D) (E) ← (D) (E) − 1	X	X	X	X	X					
	DCX H	0 0	1 0 1	0 1 1	2 B	5	1	1	(H) (L) ← (H) (L) − 1	X	X	X	X	X					
	DCX SP	0 0	1 1 1	0 1 1	3 B	5	1	1	(SP) ← (SP) − 1	X	X	X	X	X					
Rotate & shift contents of accumulator	RLC	0 0	0 0 0	1 1 1	0 7	4	1	1	Left shift CY2 ← A7 A6 ····· A1 A0 ← A7	X	X	X	O	X					
	RRC	0 0	0 0 1	1 1 1	0 F	4	1	1	Right shift CY2 → A7 A6 ····· A1 A0 → CY2	X	X	X	O	X					
	RAL	0 0	0 1 0	1 1 1	1 7	4	1	1	Left shift CY2 ← A7 A6 ····· A1 A0 ← CY2	X	X	X	O	X					
	RAR	0 0	0 1 1	1 1 1	1 F	4	1	1	Right shift CY2 → A7 A6 ····· A1 A0 → A7	X	X	X	O	X					
Accumu. compen.	CMA	0 0	1 0 1	1 1 1	2 F	4	1	1	(A) ← $\overline{(A)}$	X	X	X	X	X					
	DAA	0 0	1 0 0	1 1 1	2 7	4	1	1	Results of binary addition are adjusted to BCD	O	O	O	O	O					
Carry set	STC	0 0	1 1 0	1 1 1	3 7	4	1	1	(CY2) ← 1	X	X	X	1	X					
	CMC	0 0	1 1 1	1 1 1	3 F	4	1	1	(CY2) ← $\overline{(CY2)}$	X	X	X	O	X					

*: State is T_1. †: State is T_2.

Item / Instr. class	Mnemonic	Instruction code D7 D6 D5 D4 D3 D2 D1 D0	16-mal notatn	No. of states	No. of bytes	No. of cycles	Functions	Flags S Z P CY2 CY1	Address bus Contents	Address bus Mach. cycle *	Data bus Contents	Data bus I/O	Data bus Mach. cycle**
Jump	**JMP m**	1 1 0 0 0 0 1 1 <B2> <B3>	C3	10	3	3	(PC)← m	X X X X X			<B2> <B3>	I I	M2 M3
	PCHL	1 1 1 0 1 0 0 1	E9	5	1	1	(PC)←(H)(L)	X X X X X					
	JC m	1 1 0 1 1 0 1 0 <B2> <B3>	DA	10	3	3	(CY2) = 1	X X X X X					
	JNC m	1 1 0 1 0 0 1 0 <B2> <B3>	D2	10	3	3	(CY2) = 0 If condition is true (PC)← m	X X X X X	If condition is true				
	JZ m	1 1 0 0 1 0 1 0 <B2> <B3>	CA	10	3	3	(Z) = 1	X X X X X			<B2> <B3>	I I	M2 M3
	JNZ m	1 1 0 0 0 0 1 0 <B2> <B3>	C2	10	3	3	(Z) = 0	X X X X X					
	JP m	1 1 1 1 0 0 1 0 <B2> <B3>	F2	10	3	3	(S) = 0 If condition is false (PC)← (PC) + 3	X X X X X					
	JM m	1 1 1 1 1 0 1 0 <B2> <B3>	FA	10	3	3	(S) = 1	X X X X X					
	JPE m	1 1 1 0 1 0 1 0 <B2> <B3>	EA	10	3	3	(P) = 1	X X X X X					
	JPO m	1 1 1 0 0 0 1 0 <B2> <B3>	E2	10	3	3	(P) = 0	X X X X X					
Subroutine call	**CALL m**	1 1 0 0 1 1 0 1 <B2> <B3>	CD	17	3	5	((SP) − 1)((SP) − 2)← (PC) + 3, (PC)← m (SP) ← (SP) − 2	X X X X X	(SP) 1 (SP) 2	M4 M5	<B2> <B3> ((PC)+3)7 4 ((PC)+3)3 0	I I O O	M2 M3 M4 M5
	RST n	1 1 A A A 1 1 1		11	1	3	((SP) − 1)((SP) − 2)←(PC) + 1, (PC)← n × 8, (SP) ← (SP) − 2 Where, 0 ≤ n ≤ 7	X X X X X	(SP) 1 (SP) 2	M4 M5	((PC)+1)7 4 ((PC)+1)3 0	O O	M4 M5
	CC m	1 1 0 1 1 1 0 0 <B2> <B3>	DC	17/11	3	5/3	(CY2) = 1	X X X X X					
	CNC m	1 1 0 1 0 1 0 0 <B2> <B3>	D4	17/11	3	5/3	(CY2) = 0 If condition is true	X X X X X	If condition is true				
	CZ m	1 1 0 0 1 1 0 0 <B2> <B3>	CC	17/11	3	5/3	(Z) = 1 ((SP) − 1)((SP) − 2)← (PC) + 3 (PC)← m	X X X X X	(SP) 1 (SP) 2	M4 M5	<B2> <B3> ((PC)+3)7 4	I I O	M2 M3 M4
	CNZ m	1 1 0 0 0 1 0 0 <B2> <B3>	C4	17/11	3	5/3	(Z) = 0 (SP)← (SP) − 2	X X X X X			((PC)+3)3 0	O	M5
	CP m	1 1 1 1 0 1 0 0 <B2> <B3>	F4	17/11	3	5/3	(S) = 0	X X X X X					
	CM m	1 1 1 1 1 1 0 0 <B2> <B3>	FC	17/11	3	5/3	(S) = 1 If condition is false (PC)←(PC) + 3	X X X X X					
	CPE m	1 1 1 0 1 1 0 0 <B2> <B3>	EC	17/11	3	5/3	(P) = 1	X X X X X					
	CPO m	1 1 1 0 0 1 0 0 <B2> <B3>	E4	17/11	3	5/3	(P) = 0	X X X X X					
Return	**RET**	1 1 0 0 1 0 0 1	C9	10	1	3	(PC) ← ((SP) + 1)((SP)), (SP)← (SP) + 2	X X X X X	(SP) (SP) + 1	M4 M5	((SP)) ((SP) + 1)	I I	M4 M5
	RC	1 1 0 1 1 0 0 0	D8	11/5	1	3/1	(CY2) = 1 If condition is true	X X X X X	If condition is true				
	RNC	1 1 0 1 0 0 0 0	D0	11/5	1	3/1	(CY2) = 0	X X X X X					
	RZ	1 1 0 0 1 0 0 0	C8	11/5	1	3/1	(Z) = 1 (PC)← ((SP) + 1)((SP))	X X X X X	(SP) (SP) + 1	M4 M5	((SP)) ((SP) + 1)	I I	M4 M5
	RNZ	1 1 0 0 0 0 0 0	C0	11/5	1	3/1	(Z) = 0 (SP)← (SP) + 2	X X X X X					
	RP	1 1 1 1 0 0 0 0	F0	11/5	1	3/1	(S) = 0	X X X X X	If condition is false				
	RM	1 1 1 1 1 0 0 0	F8	11/5	1	3/1	(S) = 1 If condition is false	X X X X X					
	RPE	1 1 1 0 1 0 0 0	E8	11/5	1	3/1	(P) = 1 (PC)← (PC) + 1	X X X X X					
	RPO	1 1 1 0 0 0 0 0	E0	11/5	1	3/1	(P) = 0	X X X X X					
Input/ output control	**IN n**	1 1 0 1 1 0 1 1 <B2>	DB	10	2	3	(A) ← (Input buffer) ← (Input device of number n)	X X X X X			<B2> (Input data)	O I	M4 M5
	OUT n	1 1 0 1 0 0 1 1 <B2>	D3	10	2	3	(Output device of number n) ← (A)	X X X X X	<B2> B2>	M5	<B2> <B2> <B2>	O O	M4 M5
Interrupt control	**EI**	1 1 1 1 1 0 1 1	FB	4	1	1	(INTE)← 1	X X X X X					
	DI	1 1 1 1 0 0 1 1	F3	4	1	1	(INTE)← 0	X X X X X					
Stack control	**PUSH PSW**	1 1 1 1 0 1 0 1	F5	11	1	3	((SP) − 1) ← (A), ((SP) − 2) ← (F) (SP) ← (SP) − 2	X X X X X	(SP) 1 (SP) − 2	M4 M5	(A) (F)	O O	M4 M5
	PUSH B	1 1 0 0 0 1 0 1	C5	11	1	3	((SP) − 1) ← (B), ((SP) − 2) ← (C) (SP) ← (SP) − 2	X X X X X	(SP) − 1 (SP) − 2	M4 M5	(B) (C)	O O	M4 M5
	PUSH D	1 1 0 1 0 1 0 1	D5	11	1	3	((SP) − 1) ← (D), ((SP) − 2) ← (E) (SP) ← (SP) − 2	X X X X X	(SP) 1 (SP) − 2	M4 M5	(D) (E)	O O	M4 M5
	PUSH H	1 1 1 0 0 1 0 1	E5	11	1	3	((SP) − 1) ← (H), ((SP) − 2) ← (L) (SP) ← (SP) − 2	X X X X X	(SP) − 1 (SP) − 2	M4 M5	(H) (L)	O O	M4 M5
	POP PSW	1 1 1 1 0 0 0 1	F1	10	1	3	(F) ← ((SP)), (A) ← ((SP) + 1) (SP) ← (SP) + 2	O O O O O	(SP) (SP) + 1	M4 M5	((SP)) ((SP) + 1)	I I	M4 M5
	POP B	1 1 0 0 0 0 0 1	C1	10	1	3	(C) ← ((SP)), (B) ← ((SP) + 1) (SP) ← (SP) + 2	X X X X X	(SP) (SP) + 1	M4 M5	((SP)) ((SP) + 1)	I I	M4 M5
	POP D	1 1 0 1 0 0 0 1	D1	10	1	3	(E) ← ((SP)), (D) ← ((SP) + 1) (SP) ← (SP) + 2	X X X X X	(SP) (SP) + 1	M4 M5	((SP)) ((SP) + 1)	I I	M4 M5
	POP H	1 1 1 0 0 0 0 1	E1	10	1	3	(L) ← ((SP)), (H) ← ((SP) + 1) (SP) ← (SP) + 2	X X X X X	(SP) (SP) + 1	M4 M5	((SP)) ((SP) + 1)	I I	M4 M5
Others	**HLT**	0 1 1 1 0 1 1 0	76	7	1	1	(PC) ← (PC) + 1	X X X X X					
	NOP	0 0 0 0 0 0 0 0	00	4	1	1	(PC) ← (PC) + 1	X X X X X					

*: State is T_1. **: State is T_2.

Symbol	Meaning
r	Register
m	Two-byte data
n	One-byte data
<B2>	Second byte of instruction
<B3>	Third byte of instruction
AAA	Binary representation for RST instruction n
F	8-bit data from the most to the least significant bit S, Z, 0, CY1, 0, P, 1, CY2
PC	Program counter
SP	Stack pointer

Symbol	Meaning
SSS or DDD	Bit pattern designating register or memory. Where, M = (H)(L)

Register or memory	SSS or DDD
B	0 0 0
C	0 0 1
D	0 1 0
E	0 1 1
H	1 0 0
L	1 0 1
M	1 1 0
A	1 1 1

Symbol	Meaning
←	Data is transferred in direction shown
( )	Contents of register or memory location
∨	Inclusive OR
∀	Exclusive OR
∧	Logical AND
¯	1s complement
X	Content of flag is not changed after execution
O	Content of flag is set or reset after execution
I	Input mode
O	Output mode

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CODING EXAMPLES

Examples of coding using control commands and the assembler language of the cross assembler follow.

1. Control Commands

1. Control commands are in the following general form:

```
///Symbol[,Parameter List]
```

2. Two source programs are read in from the card reader, and the assembly lists are printed.

```
///ASMB8,L,C,S
///RUN,2
```

3. Four object programs (files) F11, F12, F13 and F14 on the disk are linked together and a relocatable object program is generated and filed in RF11 on the disk.

```
///LINKG,R,N,D,F11,F12,F13,F14
///BDISK,RF11
///RUN
```

2. Assembly Language

1. A statement is of the following general form:

```
[Symbol]␣Mnemon␣[Operand]
```

Where, ␣ indicates a blank, and [ ] defines a field that is optional.

2. This example evaluates the data in address INDATA against the table at address TA01. It then jumps to the appropriate processing program according to the evaluation. The first address of the corresponding processing program is located at address SENS.

```
*
*  ***  EXAMPLE  OF  CODING  ***                    ①
*
        NAM     PROM                                ②
        EXT     TAB1,TAB2,TAB3                      ③
        EXT     TAB4,TAB5,TAB6
        ENT     MAIN                                ④
        ROM                                         ⑤
MAIN    EQU     *                                   ⑥
        LXI     H,TA01                              ⑦
        MVI     C,0
        MVI     B,6B                                ⑧
        LDA     INDATA
LOOP1   CMP     M
        JZ      LOOP2
        INX     H
        INR     C
        DCR     B
        JNZ     *-7                                 ⑨
        JMP     1000    ERR,SHORI                   ⑩
*
LOOP2   MVI     H,0
        MOV     L,C
        LXI     B,SENS
        DAD     H
        DAD     B
        PCHL
*
        RAM                                         ⑪
INDATA  DEF     45H                                 ⑫
*
        ROM
TA01    DEF     'MELPS8'                            ⑬
SENS    DADR    TAB1                                ⑭
        DADR    TAB2
        DADR    TAB3,TAB4
        DADR    TAB5,TAB6
*
        END
```

① An asterisk in the first column indicates that the entire statement is a comment.

② The program name is declared as 'PROM'.

③ The external programs referenced by this program are declared.

④ The external programs that reference this program are declared.

⑤ The program segment from here to the next RAM pseudo instruction is regarded as a ROM region.

⑥ The symbol MAIN refers to the value in the program location counter at this source program statement.

⑦ Locations can be referred to by symbols.

⑧ Octal numbers can be used.

⑨ Expressions can be used in the operand field.

⑩ The statement following a blank after an operand field is a comment.

⑪ Declares the start of a RAM region.

⑫ Hexadecimal numbers can be used.

⑬ Character constants in ASCII code can be used.

⑭ The address of symbol TAB 1 is set to the location of address SENS and SENS+1.

MELPS 8 SIMULATOR

DESCRIPTION

A pseudo CPU and a pseudo memory are modeled in the host computer by the simulator, and programs in the pseudo memory are executed by the pseudo CPU to debug and test programs.

The simulator contains a powerful set of 26 control commands for efficient program debugging.

FEATURES

- Set of 26 powerful control commands
- Batch and conversational processing
- Symbolic addressing
- Execution time calculations
- Intermediate results saved in specified format
- Look-back option when tracing
- Binary, octal, decimal and hexadecimal numbers are selectable
- Assignment of program segments to ROM or RAM region
- Memory protection
- Interrupt function
- Flexibility in input/output media
- Continuous processing of input/output data
- Execution minicomputer: MELCOM 70 (memory capacity more than 24K words, monitor BDOS)
- Programming language: FORTRAN IV (parts are written in assembly language)

FUNCTION

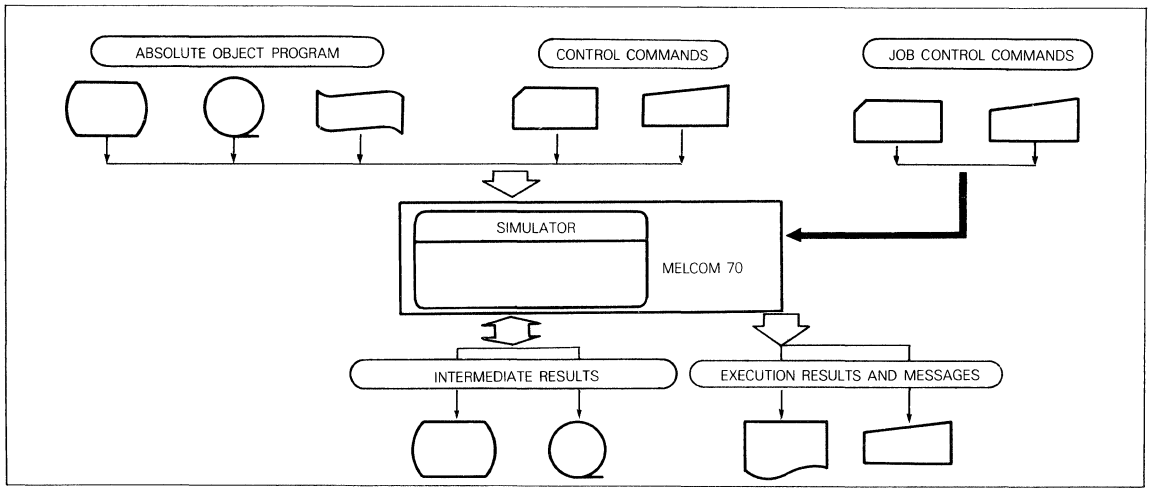
The trace command function assigns a specific trace region so that it traces only the specified program steps. Execution of the simulation can be halted by a breakpoint which can be assigned to any location. Program debugging efficiency can be expected to increase by the use of these functions.

Memory protect and ROM regions are simulated. This means the simulator will not allow writing in a ROM region and will not allow either reading or writing in a memory protect region. Therefore, the program under simulation is completely simulated, including the state of the memory in the object computer system.

Input/output media

- Object program input : Paper tape, magnetic tape and magnetic disk
- Control command input : Punched card and keyboard
- Simulation intermediate results output : Magnetic tape and magnetic disk
- Simulation result output : List
- Input/output data : Punched card, keyboard, paper tape and magnetic tape

SIMULATOR PROCESSING SYSTEM



ORDERING INFORMATION

Programs

Program name	Ordering number	Program and software manuals included
MELPS 8 simulator (B-version)	GA1SM0100	Source Program MELPS 8 Simulator Operating Manual (B-version) GAM-SR00-03A MELPS 8 Cross Assembler & Simulator Operating Manual (on MELCOM 70) GAM-SR00-04A

Reference Manuals for Separate Ordering

Manual name	Manual number
MELPS 8 Assembly Language Manual (A-version)	GAM-SR00-01A
MELPS 8 Cross Assembler Operating Manual (A-version)	GAM-SR00-02A
MELPS 8 Simulator Operating Manual (B-version)	GAM-SR00-03A
MELPS 8 Hardware Manual	GAM-HR00-01A

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CODING METHOD OF CONTROL COMMANDS

The input formats for control commands are shown in Fig. 1.

Fig. 1 Input formats for control commands

Column no.	1				72	73	80
Contents	Blank	Command	Blank	Parameter list	Blank	Comment	Sequence number
No. of columns	1 or more columns	The number of characters in the command	1 or more columns	The number of characters in the parameter list	1 or more columns	Free	8 columns
Remarks			The command, parameter list and comment must be less than 73 columns.				Not required if the command is typed in from the system typewriter

CONTROL COMMANDS

The simulator includes 26 control commands as shown in Table 1.

Table 1. List of control commands and their functions

	Functions \ Item	Control commands: Action	Control commands: Mnemonic command	Comments
Simulator control commands	Start	Start simulation	START	Starts simulation and designates the input unit for control commands.
		Reinitialize	REINIT	Sets the state to the same state it was after the START command execution was completed.
	End	End simulation	END	Returns to the monitor when executed during simulation.
	Program loading or saving intermediate results	Load object program	LOAD	The absolute object program or the saved intermediate partially executed program is loaded.
		Save intermediate results	SAVE	All information such as executed commands, contents of registers and flags, and so forth, are saved in external memory.
	Changing control command input unit	Changes to card reader	BATCH	The command input unit is changed to the card reader.
		Changes to system typewriter	TYPE	The command input unit is changed to the system typewriter.
Executive control commands	Start	Starts execution of the object program	GO	The stop point can be designated by either an address or the number of instructions to be executed.
		Starts execution of the object program	RUN	Continues execution until a HLT instruction is encountered.
	Stop	Assigns a breakpoint	BREAK	A breakpoint is assigned by an address or a range.
		Releases an assigned breakpoint	NOBREAK	A breakpoint assigned is released.
		Steps	STEP	Breakpoints are assigned after every specified number of machine instructions.
	Assigning memory regions	Assigns a ROM region	ROM	It is declared that region assigned with this command is the ROM region.
		Releases an assigned ROM region	NOROM	The assigned ROM region is released.
		Assigns a memory protection region	PROT	A memory protect (unaccessible) region is assigned.
		Releases an assigned memory protect region	NOPROT	An assigned memory protect region is released.
	Trace	Assigns a trace region	TRACE	Printing out the contents of registers, the program counter and flip-flops along with the executed instruction codes while executing the instructions in a trace region.
		Releases an assigned trace region	NOTRACE	The assigned trace region is released.
	Set data		SET	Registers, stack pointers, program counter, flag flip-flops, I/O ports and the contents of memory are set.
	Interrupt		INTER	If interrupt is enabled, the 1-byte instruction associated with this command is executed.
	Counts the number of cycles		TIME	Counts the total number of cycles of the machine instructions executed before this command is encountered.
	Printing out	Assigns a base	BASE	A base for printing is assigned.
		Prints out	DISPLAY	The contents of registers, stack pointers, program counter, flag flip-flops, I/O ports, and memory are printed according to the assigned base. Look-back is possible.
	Conversion of values		CONV	The current program counter or the assigned value is printed out in binary, octal, decimal or hexadecimal.
I/O commands	Input/output simulation	Input simulated	IP	Defines an input string for a machine instruction IN.
		Output simulated	OP	Defines an output string for a machine instruction OUT.

Note 1 : The underlined part of the mnemonic command can be used as a short mnemonic.
2 : The control command 'START' is the first command, and its input unit must be the card reader.

EXAMPLE OF SIMULATION

The program shown in Fig. 2 is simulated using the control command in the sequence shown in Table 4. The program in Fig. 2 is named 'CON102'. It converts a decimal integer (0~65,535) to a binary number.

The decimal number to be converted is stored in addresses DED1~DED5 in ASCII code, and the converted result is stored in addresses BID and BID+1 (see Table 2). Further, if characters other than 0~9 are found in addresses DED1~DED5, the A register is set to '1' as an error flag; and if the converted result is more than 65,535, the carry flip-flop is set to '1' as an error flag.

The simulation is executed in three segments as follows:

1. The test values are set in memory addresses DED1~DED5.
2. The program is executed.
3. The simulator confirms that the contents of addresses BID and BID+1 are the correct value for the conversion of data in addresses DED1 (address 9113)~DED5 (address 9117). At the same time, it confirms that the contents of the A register and the carry flip-flop are correct.

The objective program listing is shown in Fig. 2, and explanations of the simulation control commands using this example are shown in Table 4.

Table 2 Memory location and contents

Address	Contents	Explanation of contents
DED1	a	The 5-digit decimal integer is a $\times 10^4 + b \times 10^3 + c \times 10^2 + d \times 10 + e$, and a, b, c, d and e are set in ASCII code.
DED2	b	
DED3	c	
DED4	d	
DED5	e	
BID	Converted results	Low-order 8 bits are stored in BID and high-order 8 bits in BID+1.
BID+1		

Table 3 Error flags for conversion

Item / Number to be converted	Error and no error display		Converted result
	A register	Carry flip-flop	
Integer 0~65,535	0	0	Correct
More than 65,535	0	1	Not correct
Character other than decimal digits	1	0	Not converted

Fig. 2 Assembly listing of the objective program "CON102"

```
**CROSS ASSEMBLER OF 8-BIT MICROPROCESSOR
0001*                 *
0002*      CON102     *
0003*                 *
0004 2328                        ORG  9000
0005 2328 219923      CON102     LXI  H,DED1
0006 232B 0605                   MVI  B,5
0007 232D 7E          CO100      MOV  A,M
0008 232E FE3B                   CPI  48
0009 2330 DA9423                 JC   ER
0010 2333 FE3B                   CPI  59
0011 2335 D29423                 JNC  ER
0012 2338 23                     INX  H
0013 2339 05                     DCR  B
0014 233A C22C23      D23        JN2  CO100
0015 233D 3A9D23      CO000      LDA  DED5
0016 2340 D630                   SUI  48
0017 2342 2600                   MVI  H,0
0018 2344 6F                     MOV  L,A
0019 2345 3A9C23      CO001      LDA  DED4
0020 2348 D630                   SUI  48
0021 234A 110A00                 LXI  D,10
0022 234D CA5523      CO101      JZ   CO002
0023 2350 19                     DAD  D
0024 2351 3D                     DCR  A
0025 2352 C34D23                 JMP  CO101
0026 2355 3A9B23      CO002      LDA  DED3
0027 2358 D630                   SUI  48
0028 235A 116400                 LXI  D,100
0029 235D CA6523      CO102      JZ   CO003
0030 2360 19                     DAD  D
0031 2361 3D                     DCR  A
0032 2362 C35D23                 JMP  CO102
0033 2365 3A9A23      CO003      LDA  DED2
0034 2368 D630                   SUI  48
0035 236A 11E803                 LXI  D,1000
0036 236D CA7523      CO103      JZ   CO004
0037 2370 19                     DAD  D
0038 2371 3D                     DCR  A
0039 2372 C36D23                 JMP  CO103
0040 2375 3A9923      CO004      LDA  DED1
0041 2378 FE37                   CPI  37H
0042 237A D29023                 JNC  OV
0043 237D D630                   SUI  48
0044 237F 111027                 LXI  D,10000
0045 2382 CABA23      CO104      JZ   CO005
0046 2385 19                     DAD  D
0047 2386 3D                     DCR  A
0048 2387 C38223                 JMP  CO104
0049 238A 229E23      CO005      SHLD BID
0050 238D C39723                 JMP  CO006
0051 2390 37          OV         STC
0052 2391 C39723                 JMP  CO006
0053 2394 3E01        ER         MVI  A,11
0054 2396 A7                     ANA  A
0055 2397 00          CO006      NOP
0056 2398 76                     HLT
0057 2399 00          DED1       DEF  0
0058 239A 00          DED2       DEF  0
0059 239B 00          DED3       DEF  0
0060 239C 00          DED4       DEF  0
0061 239D 00          DED5       DEF  0
0062 239E 0000        BID        DADR
0063 2328                        END
```

Table 4 An example of the use of simulation control commands.

START M70,CARD	MELCOM 70 is used as the host computer, and the input unit for the control commands is selected to be the card reader.
LOAD START,5	The object program is input from the paper tape reader (device number 5).
SET CPU SP=10000 PC=9000	The stack pointer is set to the value 10,000, and the program counter is set to the value 9,000.
SET MEMORY,DED1=31# SE M,DED2:DED5=32#,33#,35#,37#	Data is set in memory. 31# is stored in location DED1, 32# in DED2, 33# in DED2+1, 35# in DED2+2, and 37# in DED5.
BREAK CO002,CO003,CO004,CO005	Breakpoints are assigned.
DISPLAY CPU,SP,PC	Displays the contents of the stack pointer (SP) and the program counter (PC) for confirmation.
D M,DED1:DED5	Confirms whether or not the correct value is set in memory. Here, D is the abbreviated command for DISPLAY and M for MEMORY.
GO *	The program is executed until the machine instruction HLT is encountered, printing out the contents of the PC and SP registers and flip-flops at each breakpoint that was assigned by BREAK above.
D M,9119:9120(@)	Confirms whether the conversion is correct or not, displaying the result of the conversion in binary form. It can also be confirmed by finding the change of the contents of registers H and L in the list that is printed out during execution.
TIME	The number of cycles executed is counted.
NOBR CO002,CO003,CO004,CO005	The breakpoints assigned with BREAK are released.
S M,DED1=36# S M,DED2:DED5=35# S M,DED4=43#	36# is set in address DED1, 35# in addresses DED2～DED5 and 43# in address DED4.
S CP,PC=9000	9,000 is set in the program counter.
GO	Executes until a HLT instruction is encountered.
D M,9113:9120	The data and the result are printed in the hexadecimal because the BASE command is not used. In this case, including a character other than 0～9 confirms whether or not a '1' is set in the A register after execution.
SAVE 2,SAV1	Intermediate results are saved in file SAV1 of the disk.

START M70,C	MELCOM 70 is used as the host computer, and the input unit for the control commands is selected to be the card reader.
LO CONT,2,SAV1	The intermediate results that were saved are loaded from the disk. The file name is 'SAV1'.
TYPE	The input unit for control commands is changed from the card reader to the keyboard.
S CUP,SP=10000,PC=9000	The program counter and the stack pointer are set.
S M,DED1:DED5=37#,35#	37# is set in address DED1, 35# in DED1+1, 37# in DED1+2, 35# in DED1+3 and 37# in DED5.
GO	Executes until a HLT instruction is encountered. Confirms whether or not a '1' is set in the carry flip-flop because the data exceeded 65,535.
S CPU,PC=9000	The start address is set.
S M,DED1:DED5=30#	30# is set in addresses DED1～DED5.
GO	Executes until an HLT instruction is encountered.
D M,9113:9120	Confirms the conversion result.
S CPU,PC=9000	The start address is set.
S M,9113=36# S M,9115=35#	36# is set in address 9113, 35# in address 9115.
GO	Execution starts. Executes until an HLT instruction is encountered.
D M,9113:9120	Confirms the conversion result.
END	Declares the end of simulation.

APPLICATIONS

10

1. CODE CONVERSION PROGRAMS

There are 4 code conversion programs for conversions between hexadecimal numbers and their corresponding ASCII code in binary notation. Details of these programs are given below.

Table 1 Correspondence of number formats

Hexadecimal symbols	Machine language binary number	ASCII code in binary notation for hexadecimal symbols
0	0000	00110000
1	0001	00110001
2	0010	00110010
3	0011	00110011
4	0100	00110100
5	0101	00110101
6	0110	00110110
7	0111	00110111
8	1000	00111000
9	1001	00111001
A	1010	01000001
B	1011	01000010
C	1100	01000011
D	1101	01000100
E	1110	01000101
F	1111	01000110

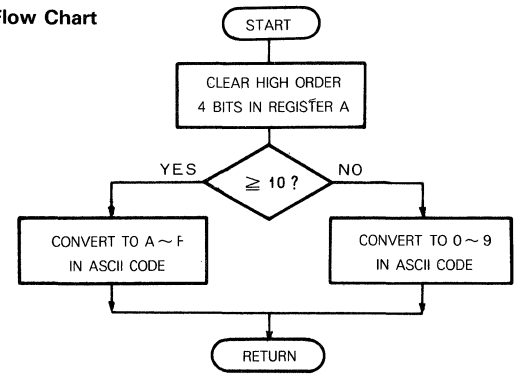
1.1 Binary (4 Bits) to ASCII (1 Character) Conversion (BTA)

This program converts the low order 4 bits in register A (a hexadecimal number 0~F) to the corresponding 8-bit ASCII-coded hexadecimal symbol '0'~'F'. The result is retained in register A. Registers B, C, D, E, H and L are not affected.

Register Status

Register	Contents at start	Contents at return
A	Binary number to be converted in the low order 4 bits	8-bit ASCII code for the high order hexadecimal symbol
B,C,D,E, H and L		Contents at start

Flow Chart



Program Listing

```
*
*  ***  SUB(BTA)  */BINARY TO ASCII
*
BTA     ANI     0FH
        CPI     10
        JNC     B1
        ADI     48
        RET
B1      ADI     55
        RET
```

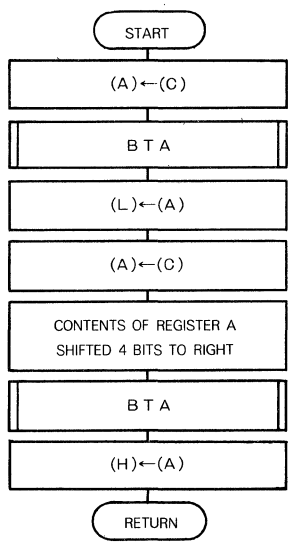
1.2 Binary (8 Bits) to ASCII (2 Characters) Conversion (BTA 2)

This program converts the 8 bits in register C (a 2-digit hexadecimal number 00~FF to the 2 corresponding 8-bit ASCII-coded hexadecimal symbols '0'~'F'. The results are retained in registers H (high order) and L (low order). Registers B, D and E are not affected.

Register Status

Register	Contents at start	Contents at return
A		8-bit ASCII code for the high order hexadecimal symbol
C	Binary number to be converted	Binary number to be converted
H		8-bit ASCII code for the high order hexadecimal symbol
L		8-bit ASCII code for the low order hexadecimal symbol
B, D and E		Contents at start

Flow Chart



Program Listing

```
*
*  ***  SUB(BTA2)  *
*  *BINARY TO TWO ASCII CHARACTERS
*
BTA2    MOV     A,C
        CALL    BTA
        MOV     L,A
        MOV     A,C
        RRC
        RRC
        RRC
        RRC
        CALL    BTA
        MOV     H,A
        RET
```


MITSUBISHI ELECTRIC

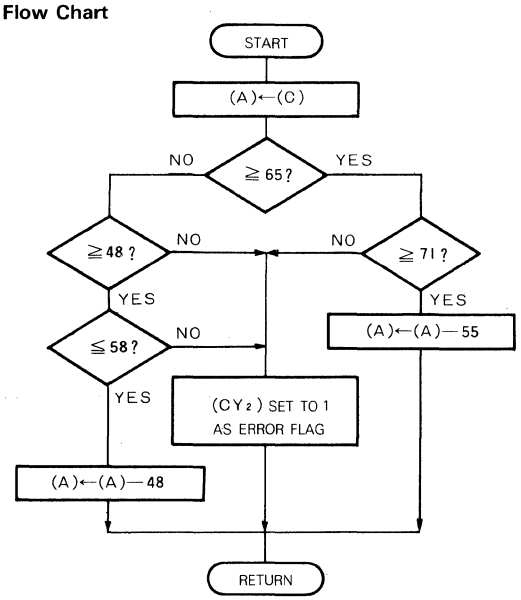
1.3 ASCII (1 Character) to Binary (4 Bits) Conversion (ATB)

This program converts the 8-bit ASCII code in register C (a hexadecimal symbol '0'~'F') to a 4-bit binary number 0000 ~1111. The result is retained in the low order 4 bits of register A. If register C contains a code for a character other than a hexadecimal symbol 0~F, it is recognized as an error; the carry flip-flop is set, and the program is exited. Registers B, D, E, H and L are not affected.

Register Status

Register	Contents at start	Contents at return
A		Hexadecimal number in binary form in the low order 4 bits
C	ASCII coded hexadecimal symbol to be converted	ASCII coded hexadecimal symbol to be converted
B, D, E, H and L		Contents at start

Flow Chart



Program Listing

```
1  2  3  4  5  6  7  8  9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33
*
*  ***  SUB(ATB)      */ASCII TO BINARY
*
ATB       MOV     A,C
          CPI     65
          JC      A1
          CPI     71
          JNC     A3
          SUI     55
          RET
A1        CPI     48
          JC      A3
          CPI     58
          JNC     A3
A2        SUI     48
          RET
A3        STC
          RET
```

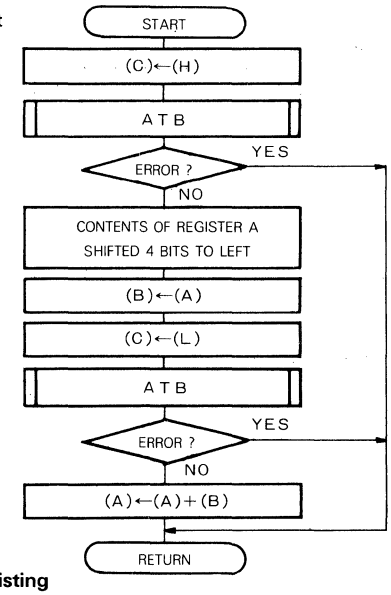
1.4 ASCII (2 Characters) to Binary (8 Bits) Conversion (ATB 2)

This program converts the two 8-bit ASCII codes in registers H and L (2 hexadecimal symbols '0'~'F', high order in register H and low order in register L) to an 8-bit binary number ($0 \sim 255_{10}$). The result is retained in register A. If register H or L contains a code for a character other than a hexadecimal symbol '0'~'F', it is recognized as an error; the carry flip-flop is set, and the program is exited. Registers D and E are not affected.

Register Status

Register	Contents at start	Contents at return
A		8-bit binary number (2 hexadecimal digits)
B		4-bit binary number in the high order 4-bits conversion of high order hexadecimal symbol
C		Low order ASCII coded hexadecimal symbol to be converted
H	High order ASCII coded hexadecimal symbol to be converted	High order ASCII coded hexadecimal symbol to be converted
L	Low order ASCII coded hexadecimal symbol to be converted	Low order ASCII coded hexadecimal symbol to be converted
D and E		Contents at start

Flow Chart



Program Listing

```
1  2  3  4  5  6  7  8  9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33
*
*  ***  SUB(ATB2)  *
*  /TWO ASCII CHARACTERS TO BINARY
*
ATB2      MOV     C,H
          CALL    ATB
          RC
          RLC
          RLC
          RLC
          RLC
          MOV     B,A
          MOV     C,L
          CALL    ATB
          RC
          ADD     B
          RET
```

2. SORTING PROGRAM (SORT)

This program sorts records (1 byte in length) in descending order. Up to 65 535 records can be sorted. The binary number 255_{10} cannot be used as data because it is reserved for the end-of-data mark. This data is stored in descending order according to the rank of its sort key.

The program sorts by comparing a data item with all other data items, thus determining its rank. The data associated with the sort key is then stored in descending order according to that rank.

This program can also recall the data associated with any record. If the rank k ($1 \leqq k \leqq 65\,535$) is stored in memory locations ORD and ORD+1, the 1-byte data associated with that rank is stored in register A; and then control is returned to the user's program. If k is specified as zero, register A is set to zero and control is returned to the user's program.

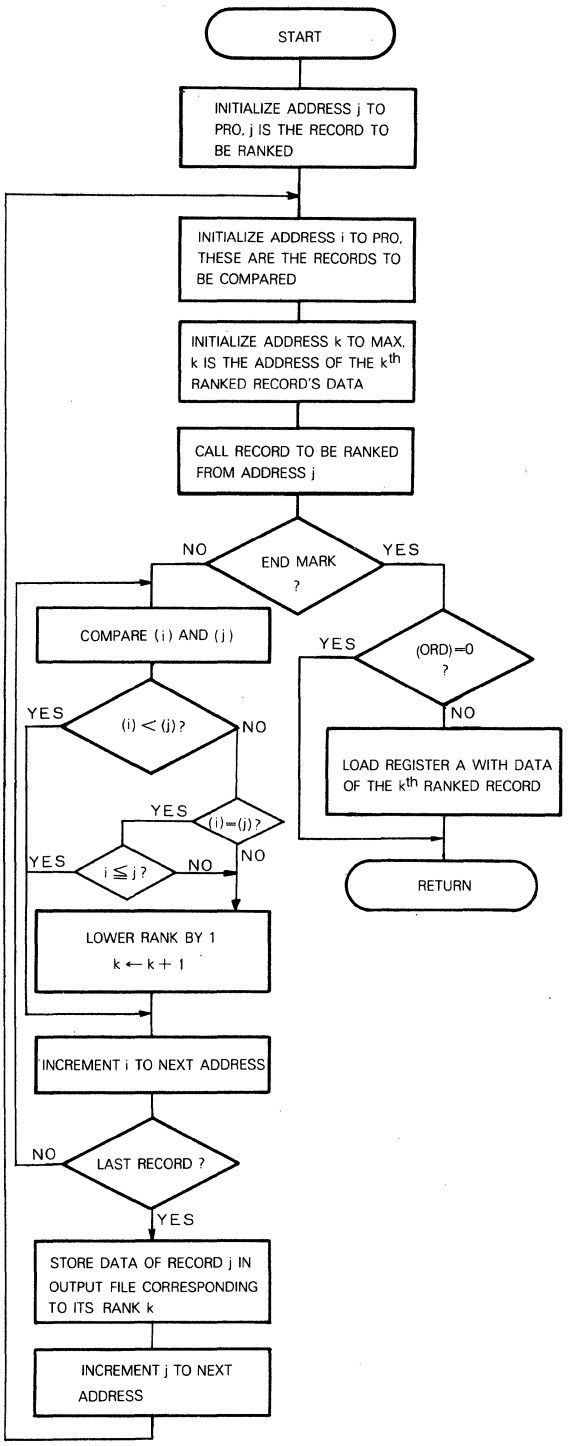
Register Status

Register	Use during execution	Contents changed at return
A	Calculates and recalls data of rank k	yes
B	Data being compared is stored	yes
C	Not used	no
D	Memory address for storing data after ranking	yes
E		yes
H	Memory address of data to be ranked	yes
L		yes

Symbolic Memory Address

Symbolic address		Use during execution	No. of bytes	Contents changed at return
User's area	ORD	k (the rank of data to be recalled)	2	no
	PRO	Storage area for records to be sorted (PRO is the first address)	n+1	no
	MAX	Storage area for sorted data (MAX is the first address)	n+1	yes
Control area	DADD	Address in PRO of record being sorted	2	no
	RADD	Address in MAX for storing result	2	no
	M1	Address of record to be ranked	2	yes
	M2	Address of record being compared	2	yes
	COUNT	Counter for number of records	2	yes

Flow Chart



Program Listing

```
*
*  ***  SUBROUTINE (SORT)  ***
*
*  /SORTING PROGRAM
*
        NAM     SORT                    ①
*  <USERS DATA AREA>  *                 ②
ORD     DADR    0
PRO     DEF     1
        DEF     55
        DEF     100                     ③
        DEF     15
        DEF     FF#                     ④
MAX     BSS     MAX-PRO                 ⑤
*
*  <CONTROL DATA AREA>
DADD    DADR    PRO
RADD    DADR    MAX
M1      DADR    0
M2      DADR    0
COUNT   DADR    0
*
*  ***  PROGRAM START  ***  *
*
        ROM                             ⑥
SORT    LHLD    DADD
        XCHG
        LXI     H,0
R1      SHLD    COUNT
        LHLD    RADD
        XCHG
*
R2      MOV     B,M
        CPI     FF#
        JZ      R8
        SHLD    M1
        LHLD    DADD
R3      MOV     A,M
        SHLD    M2
        CPI     FF#
        JZ      R7
        CMP     B
        JC      R6
        JNZ     R5
        PUSH    PSW
        LHLD    M1
        LDA     M2
        SUB     L
        LDA     M2+1
        JC      R4
        POP     PSW
        JMP     R6
R4      POP     PSW
R5      INX     D
R6      INX     H
        JMP     R3
*
R7      LHLD    M1
        INX     H
        MOV     A,B
        STAX    D
        XCHG
        LHLD    COUNT
        JNX     H
        JMP     R1
*
R8      LHLD    COUNT
        XCHG
        LHLD    RADD
        DAD     D
        MOV     M,A
*
        LHLD    ORD
        MOV     A,L
        ORA     H
        JZ      R9
        DCX     H
        XCHG
        LHLD    RADD
        DAD     D
        MOV     A,M
R9      RET
```

Explanation Keyed to Program Listing

① The program name is defined as 'SORT'.

② If column 1 of a statement is '*', it is considered a comment.

③ Defines the value of data.

④ The '#' in FF# indicates that FF is a hexadecimal number.

⑤ Reserves a region to store the results.

⑥ The above program is defined as a RAM region because its contents are variable at time of execution, and this is a ROM region because its contents are fixed.

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MELPS 8 SUBROUTINE 1

INTEGER ARITHMETIC OPERATIONS
MASK ROM M58730-001S

DESCRIPTION

The MELPS 8 Subroutine 1 'Integer Arithmetic Operation' is programmed on a standard M58730-001S mask ROM. It includes 18 subroutines for a MELPS 8 CPU. Although the basic unit of a MELPS CPU is 1 byte (8 bits), units of 2 bytes (16 bits) and 4 bytes (32 bits) can be easily processed using these subroutines.

These subroutines contain sections of common coding; therefore, when using the subroutines, the CPU must be running in interrupt disable mode.

These subroutines can be divided into the following general classifications:

- Addition routines
- Subtraction routines
- Multiplication routines
- Division routines
- Shift operation routines
- Logic operation routines

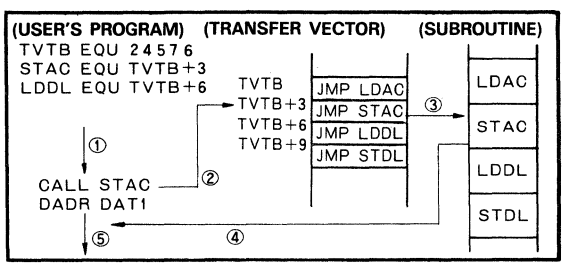
FEATURES

- All programs implemented using a pseudo accumulator in a RAM region.
- Easy processing of 2-byte or 4-byte data.
- Jump to subroutines via transfer vectors.

1. SUBROUTINE REFERENCE

In a user's program, the subroutine calling sequence is as follows:

Fig. 1.1 Subroutine reference



Note 1 : The processing order is ①, ②, ③, ④ and ⑤. A transfer vector is used to set the entry address of each subroutine.

2 : Transfer vectors are used for subroutine calls because they are not affected by changes in program size.

3 : The absolute address of a subroutine or its transfer vector must be defined before it is called.

4 : The absolute address of a subroutine or its transfer vector refers to the table of subroutine functions.

2. RESERVED MEMORY LOCATIONS

Memory locations 6000_{16}~$63FF_{16}$ of the ROM region are reserved. In addition, a 50-byte RAM region, locations $3FCE_{16}$~$3FFF_{16}$, is reserved for executing the ROM subroutines.

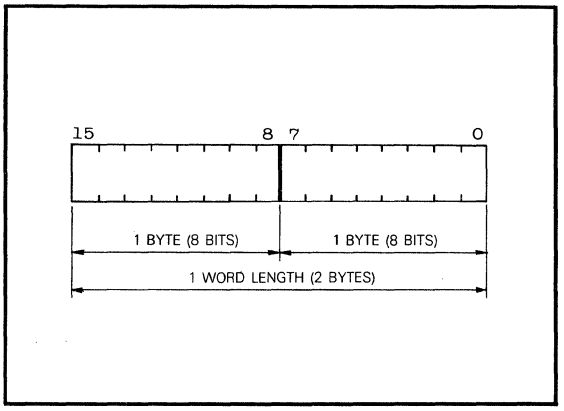
3. DATA PROCESSING UNITS OF SUBROUTINES

The MELPS 8 CPU processes data units of 8 bits (occasionally 16 bits) while these subroutines process data units of 2 bytes (16 bits) or 4 bytes (32 bits).

3.1 One Word Length (2 bytes)

A data unit of 2 bytes (16 bits) can be represent three binary coded decimal digits, 16 logical elements, a binary number with a range of -2^{15}~$2^{15}-1$, or two characters. This data structure is shown in Fig. 3.1.

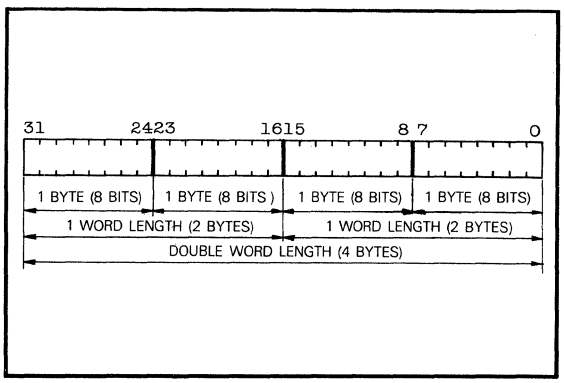
Fig. 3.1 Data structure of one word length (2 bytes)



3.2 Double Word Length (4 bytes)

A data unit of 4 bytes (32 bits) can represent seven binary coded decimal digits, a binary number with a range of -2^{31}~$2^{31}-1$, or four characters. The data structure is shown in Fig. 3.2.

Fig. 3.2 Data structure of double word length (4 bytes)



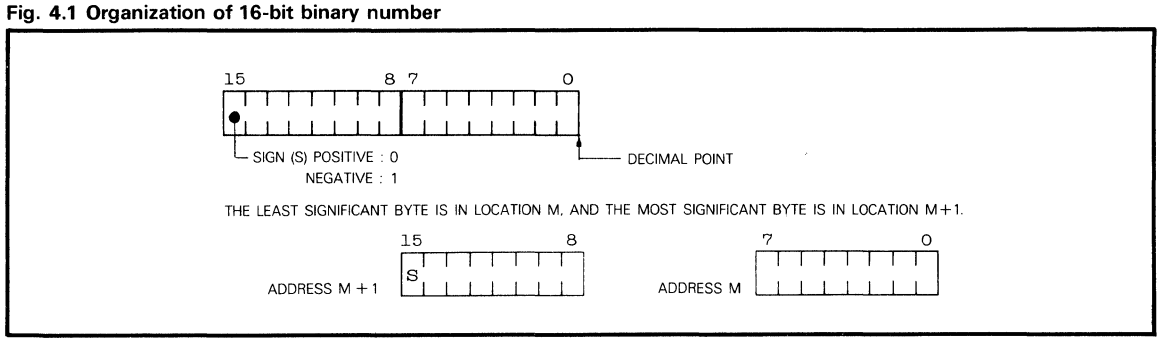
4. NUMERICAL EXPRESSIONS

Numbers can be organized in 16-bit or 32-bit units as shown below.

4.1 16-Bit Binary Number

This binary number of 16 bits is organized as one unit. Negative numbers are in 2's complement form. The number has a range of -2^{15}~$2^{15}-1$ (−32768~32767).

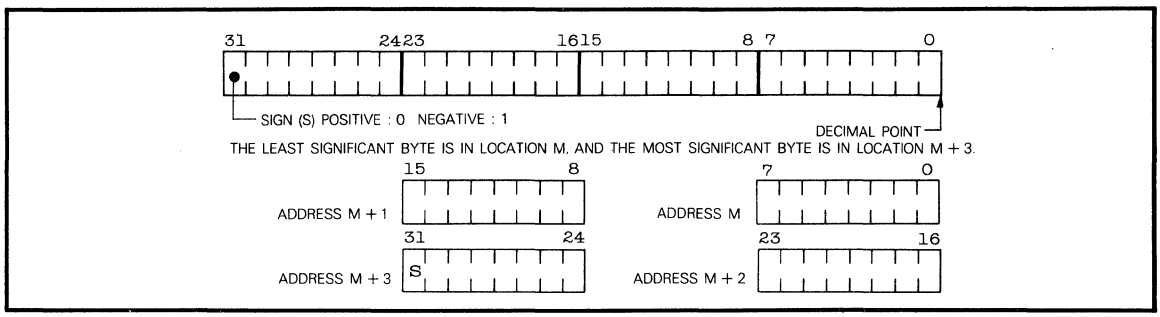
Fig. 4.1 Organization of 16-bit binary number



4.2 32-Bit Binary Number

This binary number of 32 bits is organized as one unit. Negative numbers are in 2's complement form. The number has a range of -2^{31}~$2^{31}-1$ (−2147483648~2147483647).

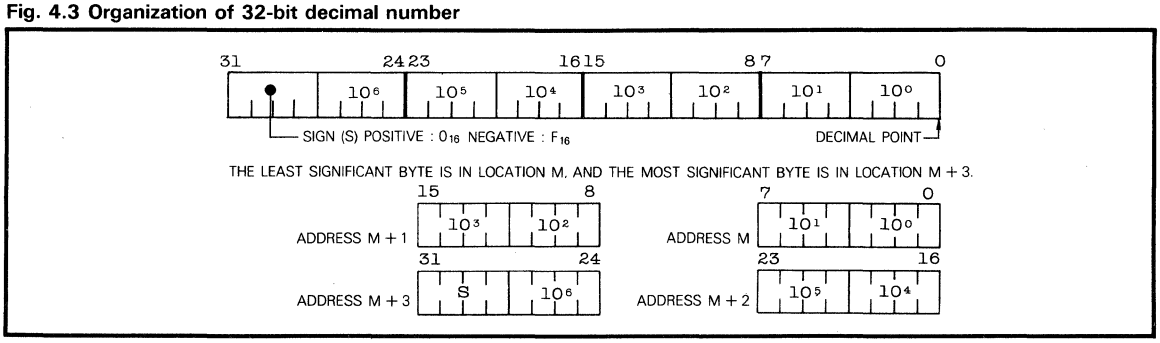
Fig. 4.2 Organization of 32-bit binary number



4.3 32-Bit Decimal Number

This decimal number of 32 bits consists of a 7 decimal digit numerical part and a 1 digit sign part. The number has a range of -10^7+1~10^7-1 (−9999999~9999999).

Fig. 4.3 Organization of 32-bit decimal number



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INTEGER ARITHMETIC OPERATIONS
MASK ROM M58730-001S

5. SUBROUTINE FUNCTIONS

Subroutine name	Function and error condition	Number of steps	Absolute address in hexadecimal (in decimal)	Transfer vector symbolic address	Processing time (max) in ms
LDAC	LOAD one word (2 bytes) data into the pseudo ACCUMULATOR. (Note 1)	19	60B7 (24576)	TVTB (Note 2)	0.2
STAC	STORE one word (2 bytes) data of the pseudo ACCUMULATOR in the location specified by the operand address.	14	60CA (24778)	TVTB+3	0.2
LDDL	LOAD DOUBLE LENGTH (4 bytes) data into the pseudo accumulator.	20	60D8 (24792)	TVTB+6	0.3
STDL	STORE DOUBLE LENGTH (4 bytes) data of the pseudo accumulator in the location specified by the operand address.	20	60EC (24812)	TVTB+9	0.3
SLDL	SHIFT LEFT DOUBLE LENGTH (4 bytes) data in the pseudo accumulator n bits. When n does not satisfy the inequality $1 \leqq n \leqq 32$, it is considered an error condition. Then register A is set to 1, and the pseudo accumulator is not shifted.	39	6100 (24832)	TVTB+21	0.3
SRDL	SHIFT RIGHT DOUBLE LENGTH (4 bytes) data in the pseudo accumulator n bits. When n does not satisfy the inequality $1 \leqq n \leqq 32$, it is considered an error condition. Then register A is set to 1, and the pseudo accumulator is not shifted.	39	6127 (24871)	TVTB+24	0.3
ARDL	ARITHMETIC shift RIGHT DOUBLE LENGTH (4 bytes) data in the pseudo accumulator n bits. When n does not satisfy the inequality $1 \leqq n \leqq 31$, it is considered an error condition. Then register A is set to 1, and the pseudo accumulator is not shifted.	64	614E (24910)	TVTB+27	0.3
XRAC	EXCLUSIVELY OR the pseudo ACCUMULATOR (2 bytes) data and the operand. The result is retained in the pseudo accumulator.	18	618E (24974)	TVTB+18	0.2
NDAC	AND the pseudo ACCUMULATOR (2 bytes) data and the operand. The result is retained in the pseudo accumulator.	18	61A0 (24992)	TVTB+12	0.2
ORAC	Inclusive OR the pseudo ACCUMULATOR (2 bytes) data and the operand. The result is retained in the pseudo accumulator.	18	61B2 (25010)	TVTB+15	0.2
ADAC	ADD the contents of the pseudo ACCUMULATOR (2 bytes) and the operand. The sum is retained in the pseudo accumulator. If a carry is generated by the addition, register A is set to 1 (overflow); otherwise, it is set to 0.	12+(20) (Note 3)	61C4 (25028)	TVTB+30	0.3
ADDL	ADD the contents of the DOUBLE LENGTH pseudo accumulator (4 bytes) and the operand. The sum is retained in the pseudo accumulator. If a carry is generated by the addition, register A is set to 1 (overflow); otherwise, it is set to 0.	12+(22) (Note 3)	61D0 (25040)	TVTB+36	0.3
SBAC	SUBTRACT the operand from the contents of the pseudo ACCUMULATOR (2 bytes). The difference is retained in the pseudo accumulator. If a borrow is generated by the subtraction, register A is set to 1 (overflow); otherwise, it is set to 0.	12+(20) (Note 3)	61F0 (25072)	TVTB+33	0.3
SBDL	SUBTRACT the operand from the DOUBLE LENGTH pseudo accumulator (4 bytes). The difference is retained in the pseudo accumulator. If a borrow is generated by the subtraction, register A is set to 1 (overflow); otherwise, it is set to 0.	12+(22) (Note 3)	61FC (25084)	TVTB+39	0.3
MLAC	MULTIPLY the contents of the pseudo ACCUMULATOR (2 bytes) by the operand. The product is retained in the pseudo accumulator.	67	621E (25118)	TVTB+42	12.0
DVAC	DIVIDE the contents of the pseudo ACCUMULATOR (4 bytes) by the 2-byte operand. The quotient is retained in the high order 2 bytes, and the remainder in the low order 2 bytes of the pseudo accumulator. If the 2-byte operand (divisor) is greater than or equal to the high order 2 bytes of the dividend or is 0, it is considered an error condition. Then register A is set to 1, and the contents of the pseudo accumulator are unaltered.	195	6261 (25185)	TVTB+45	15.0
DCAD	DECIMALLY ADD the contents of the pseudo accumulator (4 bytes) and the operand. The sum is retained in the pseudo accumulator. If a carry is generated by the addition (overflow), it is considered an error condition; and register A is set to 1.	12+(155) (Note 3)	6324 (25380)	TVTB+48	0.7
DCSB	DECIMALLY SUBTRACT the operand from the contents of the pseudo accumulator (4 bytes). The difference is retained in the pseudo accumulator. If a carry is generated by the subtraction (overflow), it is considered an error condition, and register A is set to 1.	12+(155) (Note 3)	6330 (25392)	TVTB+51	1.3

Note 1 : The pseudo accumulator is a double length (4 bytes) register reserved in the RAM.
2 : The starting address of the transfer vector table (TVTB) is 24576.
3 : The number in ( ) is the number of steps in common routines.
4 : The subroutines occupy 800 bytes of memory. The transfer vector table occupies 54 bytes of memory. The save registers B, C, D, E, H and L; and return routines occupy 129 bytes of memory. Total memory requirement is 983 bytes.

6. BASIC CALLING SEQUENCE

```
Label      Instruction  Operand
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
           CALL         SUB
           DADR         ABC
ABC        BSS          4
```

Describes the subroutine named 'SUB' being called.

Symbolic address of the operand (ABC) used by the called subroutine.

Defines the operand (ABC) and reserves memory for it.

In this example using this subroutine, the program adds two 4-byte binary numbers and stores the sum in locations WORK~WORK+3.

```
Label      Instruction  Operand
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
           ORG          3700H
TVTB       EQU          2456H7
LDDL       EQU          TVTB+6
STDL       EQU          TVTB+9
ADDL       EQU          TVTB+36
DATA1      DEF          9CH
           DEF          2AH
           DEF          45H
           DEF          03H
ABC        DEF          09H
           DEF          23H
           DEF          19H
           DEF          0AH
WORK       BSS          4
           CALL         LDDL
           DADR         DATA1
           CALL         ADDL
           DADR         ABC
           CALL         STDL
           DADR         WORK
           END
```

Absolute address of the program's start.

Absolute address of the transfer vector table's start.

Absolute address of subroutine LDDL's transfer vector.

Absolute address of subroutine STDL's transfer vector.

Absolute address of subroutine ADDL's transfer vector.

Operand

Operand

Reserves a 4-byte region to store the sum.

Loads operand (DATA 1) into the pseudo accumulator.

Adds operand (ABC) to the contents of the pseudo accumulator and retains the result in the pseudo accumulator.

Stores the sum in locations WORK ~ WORK + 3.

Note : '#' flags a hexadecimal number.

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