

In-System Programming on a PC

ISP Programming

This section discusses the many ways Lattice ISP™ devices can be programmed using an IBM®-compatible PC. This information provides a basic understanding of the programming tools Lattice offers to make using ISP devices easy.

Selecting a Lattice Programming Tool

Lattice provides a wide variety of programming tools to meet your ISP programming needs. To select the appropriate programming tool, use the guidelines listed in Table 1.

Table 1. Selecting the Appropriate Programming Tool

Development Environment	Appropriate Tool
IBM-PC/Windows	ISP Daisy Chain Download for Windows
IBM-PC/DOS	ISP Daisy Chain Download for DOS
Custom	ispCODE

Programming and Verifying

This section presents an example of ISP programming and verification using each of the Lattice ISP programming tools. It is not intended as a complete reference for using Lattice programming tools. Instead, it provides a basic overview of each of the Lattice ISP programming products.

Examples are provided for the Lattice products listed below. The complete reference manual for each of these products is listed in parentheses after the product name. Refer to these documents for detailed information about each product.

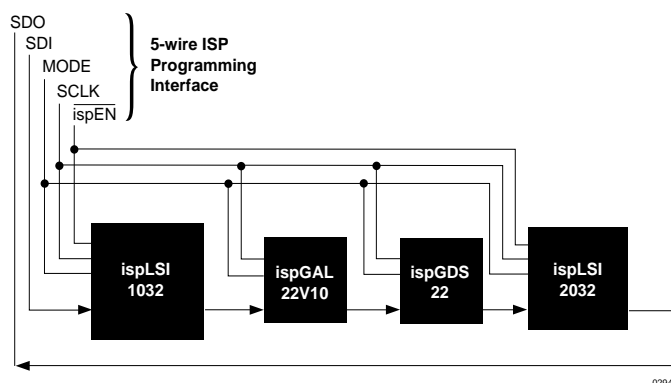
- ISP Daisy Chain Download for Windows—ISP Daisy Chain Download Reference Manual
- ISP Daisy Chain Download for DOS—ISP Daisy Chain Download Reference Manual
- ispCODE™—1996 Lattice Semiconductor Data Book, ispCODE Software Section

ISP Daisy Chain Download for Windows

ISP Daisy Chain Download for Windows allows you to program one or more ISP devices connected in a daisy chain using an IBM PC. ISP Daisy Chain Download for Windows requires the following:

- A JEDEC file for each device you want to program
- An ispDOWNLOAD™ Cable to attach to the parallel port of an IBM-compatible PC
- Microsoft Windows® 3.x
- Target hardware (circuit board) with ISP interface (see Figure 1) or the Lattice isp Engineering Kit Model 100

Figure 1. Five-Wire ISP Interface



Download Process

Follow the steps below to download to your ISP daisy chain:

1. Invoke ISP Daisy Chain Download for Windows.
2. Generate a new configuration file.
3. Verify the configuration file.
4. Program the chain.

These steps are explained in more detail in the following sections.

Note: The configuration file, *design.DLD*, can be used in the DOS or Windows environment.

In-System Programming on a PC

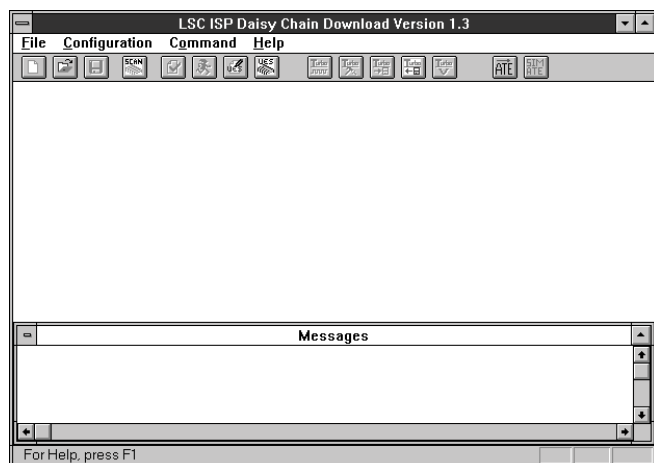
Invoking ISP Daisy Chain Download for Windows

To invoke ISP Daisy Chain Download for Windows, double click the ISP Daisy Chain Download for Windows icon as shown in Figure 2. The main window appears (Figure 3).

Figure 2. ISP Daisy Chain Download for Windows



Figure 3. The ISP Daisy Chain Download for Windows Main Window



Generating a Configuration File

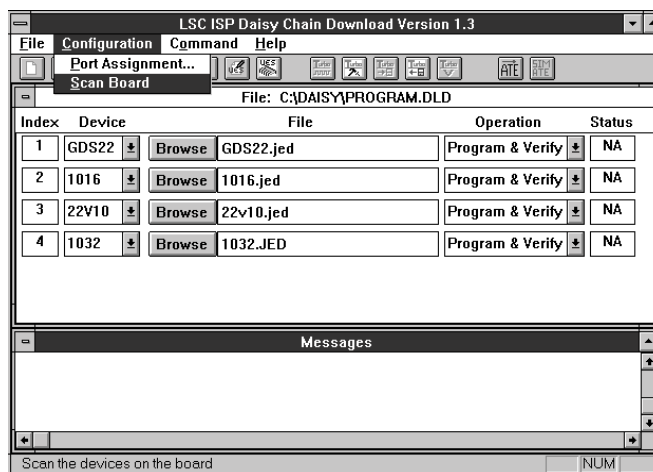
ISP Daisy Chain Download for Windows uses a configuration file to define the following information about your chain:

- The position and type of each device
- Which operation to perform (read, program, verify, etc.) on each device

If the PC is connected to the target hardware or ISP Engineering Kit Model 100, the easiest approach to creating a configuration file is to use the **Configuration** ➔ **Scan Board** command. This creates a basic configuration file which contains all the devices in the chain, but no information about which operation to perform or which JEDEC files to use.

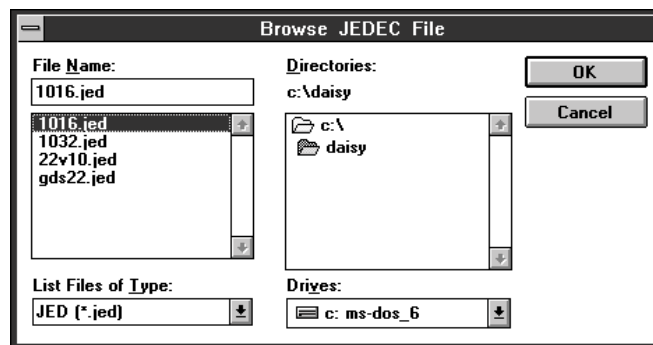
To create the configuration file, select the **Configuration** ➔ **Scan Board** Option (Figure 4).

Figure 4. Selecting Configuration ➔ Scan Board



The next step is to select a JEDEC file for each device in the chain that you want to program. You can do this by either entering the file name directly or using the browse button (Figure 5).

Figure 5. Selecting a JEDEC File from Browse Button

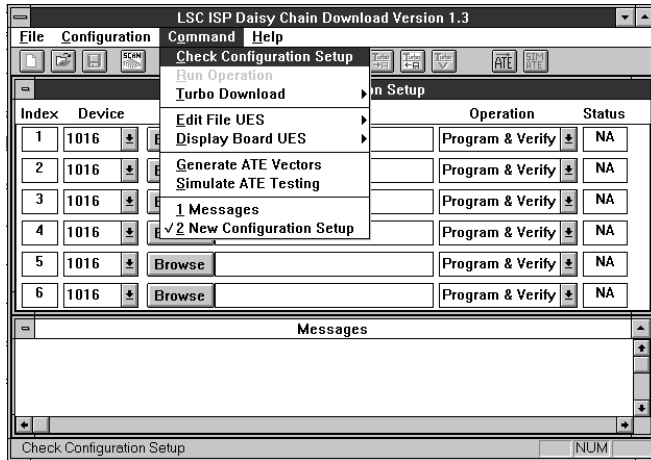


Verifying the Configuration File

Once you have created a configuration file, verify that the configuration file is valid by using the **Command** ➔ **Check Configuration Set** option (Figure 6).

In-System Programming on a PC

Figure 6. Verifying the Configuration File

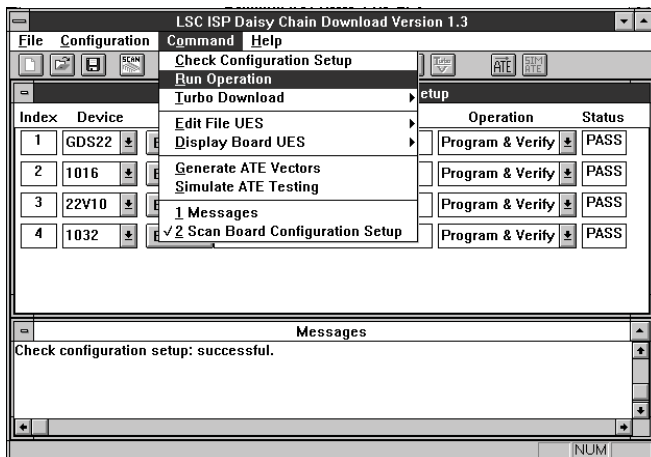


If your configuration file passes this test, then you can proceed to programming the chain.

Programming or Verifying the Chain

Once you have a valid configuration file, you can perform operations on the chain. To do this, select the **Command** → **Run Operation** from the main menu (Figure 7).

Figure 7. Performing Operations on the Chain

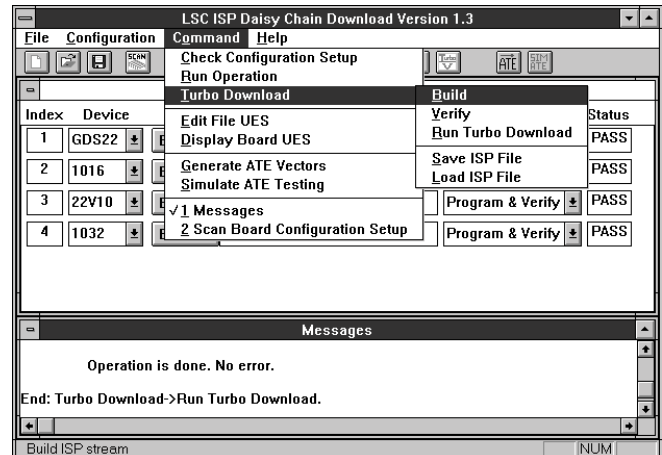


ispTURBO Programming with Windows Download

When programming time is critical, LSC provides ispTURBO Download within the Windows download environment. ispTURBO Download allows you to program multiple devices in parallel. Either by choosing the Turbo Download option of the command menu or by selecting the Windows button, an ispSTREAM file is generated. This file is used to program single or multiple ISP devices

in parallel. In the production environment, this time savings will result in a significant programming cost reduction.

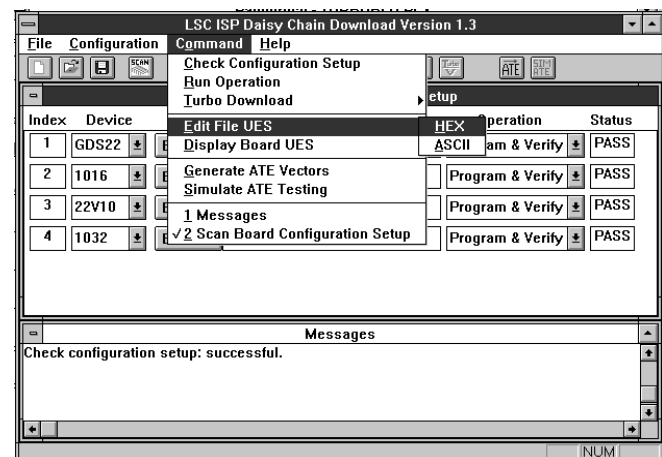
Figure 8. Configuration → Turbo Download → Build Menu Option



Updating UES with Windows Download

All ispLSI and pLSI devices comes with User Electronic Signature (UES) bits which can be used to identify the devices even when the devices are secured. As an option of the Windows Download software, the ISP device UES can be read or written from the programming environment. The format for UES option can be hexadecimal or ASCII.

Figure 9. Command → Edit File UES → Hex Menu Option

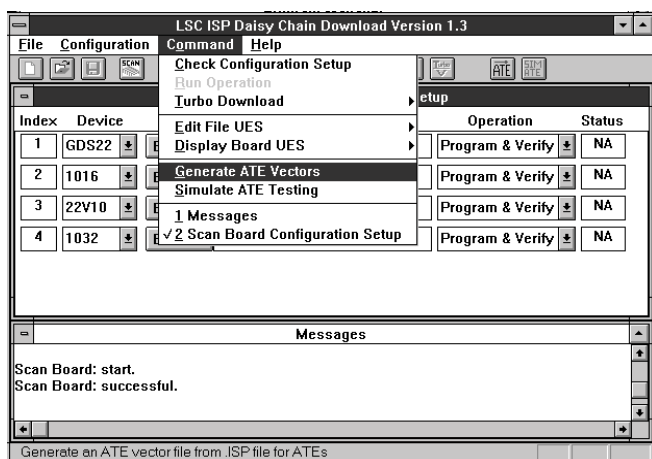


In-System Programming on a PC

ispATE

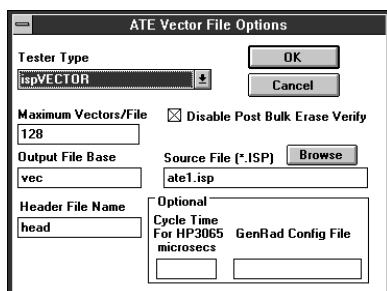
The option for generating ISP programming test vectors for widely popular Automatic Test Equipment is now integrated into the Windows Download software. There are four general vector formats: LSC generic ispVECTOR, HP, GenRAD and Teradyne. The software also allows the user to divide the vectors into multiple vectors to adjust to the capabilities of the individual tester. The easily understandable generic ispVECTOR format is used for future expandability where a test engineer with a tester that is not supported with the Windows Download can easily adapt the ispVECTOR format to the specific tester format.

Figure 10. Command → Generate ATE Vectors Menu Item



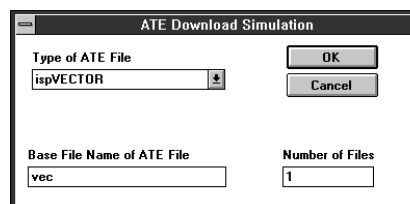
The associated ATE Vector File Options window allows you to select the tester type, number of vectors per file (determined by the maximum vector file size), input .ISP file, output file name, and an option to disable bulk erase device verification.

Figure 11. ATE Vector File Options Dialog Box



Once the vectors are generated, they are ready to be loaded into the tester environment. Before loading the vectors, they can be tested with the actual vector set through Lattice's ispDOWNLOAD cable via the PC parallel port. The Sim ATE option allows you to exercise the ispVECTOR format through the PC parallel port. In order to program the devices, the system board must have the option to connect the ispDOWNLOAD cable.

Figure 12. Command → Simulate ATE Testing Menu Item



For more information on ispATE, its vector format and hardware considerations, refer to the ispATE Software section of the 1996 Lattice Semiconductor Data Book.

ISP Daisy Chain Download for DOS

Lattice provides a DOS version of the download software for programming an ISP daisy chain. ISP Daisy Chain Download for DOS requires the following:

- A JEDEC file for each device you want to program
- An ispDOWNLOAD cable to attach to the parallel port of a PC
- Target hardware (circuit board) with an ISP interface (see Figure 1) or the Lattice isp Engineering Kit Model 100

Download Process

The following is a step by step guide for downloading to an ISP daisy chain using ISP Daisy Chain Download for DOS:

1. Invoke ISP Daisy Chain Download for DOS.
2. Create a download configuration file.
3. Verify the download.
4. Program or Verify the chain.

These steps are explained in more detail in the following sections.

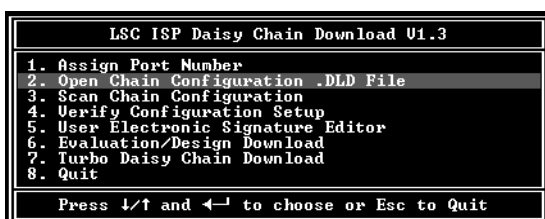
In-System Programming on a PC

Invoking ISP Daisy Chain Download for DOS

From the DOS command line, enter `ddownload`. The ISP Daisy Chain Download for DOS main window appears (Figure 13).

Note: It is preferable to invoke ISP Daisy Chain Download for DOS from the DOS prompt and not from Windows DOS. Invoking the program from Windows DOS can cause timing variations.

Figure 13. ISP Daisy Chain Download for DOS Main Menu



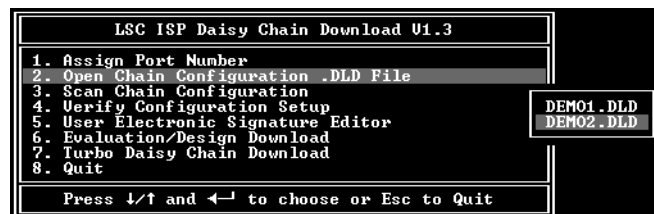
Creating a Configuration File

ISP Daisy Chain Download for DOS uses a configuration file to define the following information about your chain:

- The position and type of each device
- What operation to perform (read, program, verify, etc.) on each device.

To open an existing configuration file with the .DLD extension, simply select Open Chain Configuration and the files within the specified directory will be displayed as shown in figure 14.

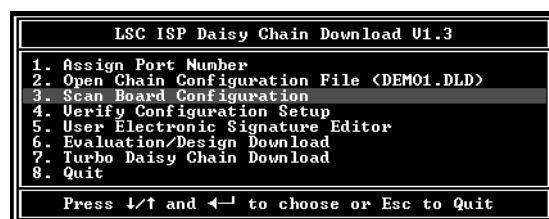
Figure 14. Open Configuration Screen



If the PC is connected to your target hardware, the easiest approach to creating a configuration file is to use the ISP Daisy Chain Download for DOS Scan Board Configuration command. This creates a basic configuration file which contains all the devices in the chain, but no information on which operation to perform or which JEDEC files to use.

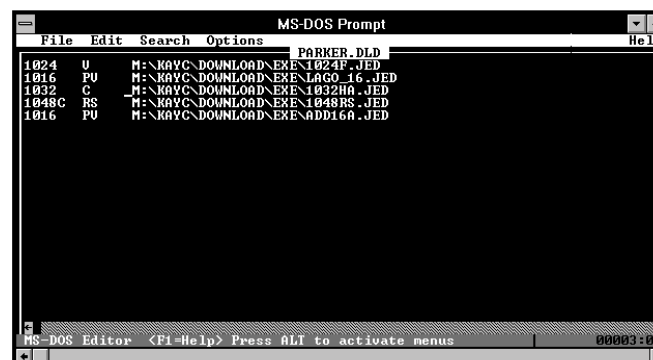
To create the configuration file, select the Scan Board Configuration command (Figure 15).

Figure 15. The Scan Board Configuration Command



This creates a basic configuration file with the name you specify. Now use a text editor to enter the operations and JEDEC files needed by each device (Figure 16). Table 2 lists the operation codes entered in the second column of the configuration file.

Figure 16. Sample .DLD File



In-System Programming on a PC

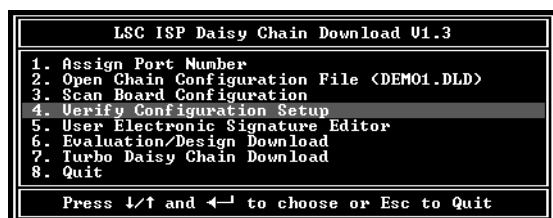
Table 2. Configuration File Operation Codes

Code	Operation
pv	program & verify
v	verify
c	checksum
rs	read & save
e	erase
nop	no operation

Verifying the Configuration File

Since creating the configuration file is a manual process, it is important that you verify the file before proceeding. To do this, select the **Check Configuration Setup** command from the ISP Daisy Chain Download for DOS menu (Figure 17). This ensures that your configuration file is valid.

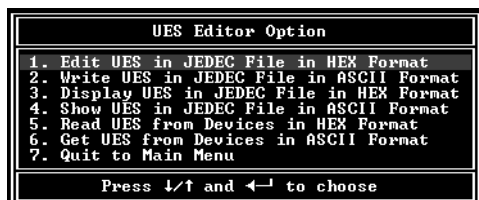
Figure 17. Verifying the Configuration File



Updating the User Electronic Signature (UES)

Similar to the Windows Download, the DOS Download also allows the user to update the UES in two formats — ASCII or hexadecimal. Selection 5, User Electronic Signature Editor, puts the user to the UES Editor Option screen. The editor allows the user either to read the UES from the device or write to the JEDEC fupmap in either of the two data formats.

Figure 18. UES Editor Screen



Programming Options with DOS Download

Selections 6 and 7 of the main programming menu allow you to select between the two programming options. The Evaluation/Design Download option programs the devices one at a time in either single device or multiple device daisy chain hardware configuration. The Turbo Daisy Chain Download option programs the selected devices in parallel.

Evaluation/Design Download

Since this option programs the devices one at a time, the software allows flexible programming options such as reading the checksum from an individual device in the programming chain. To further reduce programming time, the Turbo Download option takes full advantage of the advanced programming capability by programming the ISP devices in parallel.

Figure 19. Evaluation/Design Download Option

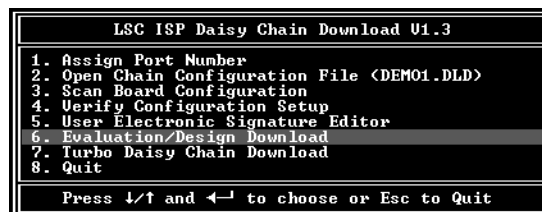
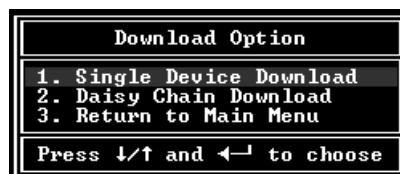


Figure 20. Download Option Menu



Turbo Daisy Chain Download

As mentioned before, this option programs the ISP devices in parallel to minimize programming time in the manufacturing environment. This option builds an ispSTREAM file which is then used to drive the parallel programming sequence through the same five-wire interface. The ispSTREAM file allows you to select program/verify, verify or NOP (No Operation) operations on the devices via the .DLD configuration file. The figure below shows the available options from the Turbo Daisy Chain Download Options menu.

Figure 21. Turbo Download Menu





Copyright © 1996 Lattice Semiconductor Corporation.

E²CMOS, GAL, ispGAL, ispLSI, pLSI, pDS, Silicon Forest, UltraMOS, Lattice Logo, L with Lattice Semiconductor Corp. and L (Stylized) are registered trademarks of Lattice Semiconductor Corporation (LSC). The LSC Logo, Generic Array Logic, In-System Programmability, In-System Programmable, ISP, ispATE, ispCODE, ispDOWNLOAD, ispGDS, ispStarter, ispSTREAM, ispTEST, ispTURBO, Latch-Lock, pDS+, RFT, Total ISP and Twin GLB are trademarks of Lattice Semiconductor Corporation. ISP is a service mark of Lattice Semiconductor Corporation. All brand names or product names mentioned are trademarks or registered trademarks of their respective holders.

Lattice Semiconductor Corporation (LSC) products are made under one or more of the following U.S. and international patents: 4,761,768 US, 4,766,569 US, 4,833,646 US, 4,852,044 US, 4,855,954 US, 4,879,688 US, 4,887,239 US, 4,896,296 US, 5,130,574 US, 5,138,198 US, 5,162,679 US, 5,191,243 US, 5,204,556 US, 5,231,315 US, 5,231,316 US, 5,237,218 US, 5,245,226 US, 5,251,169 US, 5,272,666 US, 5,281,906 US, 5,295,095 US, 5,329,179 US, 5,331,590 US, 5,336,951 US, 5,353,246 US, 5,357,156 US, 5,359,573 US, 5,394,033 US, 5,394,037 US, 5,404,055 US, 5,418,390 US, 5,493,205 US, 0194091 EP, 0196771B1 EP, 0267271 EP, 0196771 UK, 0194091 GB, 0196771 WG, P3686070.0-08 WG. LSC does not represent that products described herein are free from patent infringement or from any third-party right.

The specifications and information herein are subject to change without notice. Lattice Semiconductor Corporation (LSC) reserves the right to discontinue any product or service without notice and assumes no obligation to correct any errors contained herein or to advise any user of this document of any correction if such be made. LSC recommends its customers obtain the latest version of the relevant information to establish, before ordering, that the information being relied upon is current.

LSC warrants performance of its products to current and applicable specifications in accordance with LSC's standard warranty. Testing and other quality control procedures are performed to the extent LSC deems necessary. Specific testing of all parameters of each product is not necessarily performed, unless mandated by government requirements.

LSC assumes no liability for applications assistance, customer's product design, software performance, or infringements of patents or services arising from the use of the products and services described herein.

LSC products are not authorized for use in life-support applications, devices or systems. Inclusion of LSC products in such applications is prohibited.

LATTICE SEMICONDUCTOR CORPORATION

5555 Northeast Moore Court
Hillsboro, Oregon 97124 U.S.A.

Tel.: (503) 681-0118

FAX: (503) 681-3037

<http://www.latticesemi.com>

November 1996
