





PRODUCT GUIDE

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FOREWORD

This 1973 Analog Devices' PRODUCT GUIDE has been prepared for the designer of instrumentation and systems which accept, analyze, process, convert, transmit, display and react to analog signals. In addition to cataloging all current products available from us, it also classifies products, presents product orientation and explanatory data to make it as simple as possible for you to decide upon and specify our products for your application. We suggest that you spend a couple of moments now acquainting yourself with the format and how to use it to assure that you receive maximum service from it. Since the information contained in this GUIDE updates that in the 1972 edition, in many places considerably, we strongly urge you to use this 1973 edition as your primary information source.

GUIDE PROFILE

You will notice from the table of contents, five major product categories are presented: AMPLIFIERS; CONVERTERS; DIGITAL PANEL METERS; FUNCTION MODULES; LINEAR INTEGRATED CIRCUITS. Each has a "product guide" which is a straight-forward product presentation including narrative and specification tables. The AMPLIFIERS, CONVERTERS, DIGITAL PANEL METERS and MULTIPLIERS/DIVIDERS (under FUNCTION MODULES) also contain an "orientation" preceding the "product guide" which presents decision making criteria upon which to base product choice. Both discrete and integrated circuit products are discussed in these sections.

In addition to the product descriptions, diagramatic views of the style and dimensions of the packaging into which our products are designed are presented in one convenient location. The package designations are referenced in the respective sections for each product.

Two quick reference product/page indices, one organized by product category and class, the other by model number, are also included.

This GUIDE also contains a discussion of significant new products, a worldwide business guide, and an overview of Analog Devices, a worldwide service-oriented company. The company you do business with is as important a consideration in the product selection process, as the product itself. The summary of our company presented here should, we believe, be reviewed with the same interest as the product presentations.

HOW TO USE THIS GUIDE

There are a number of ways to use this publication depending upon your particular product needs, level of understanding of the technology, and knowledge of the Analog Devices product line. In general:

- IF you want to reference a product that you know by model number, THEN simply refer to the Model Number Page Index (page 208).
- IF you know what class of product (i.e., High Resolution A/D Converters), but need to decide on a specific model, THEN refer to that product class listing in the table of contents. On the page indicated you will find sufficient information to make a choice.
- All of the integrated circuits are presented both in the LINEAR INTEGRATED CIRCUITS section as well as the AMPLIFIER PRODUCTS section. Thus, if your requirement is definitely for an IC use the information in the IC section. If you are undecided, the data in the AMPLIFIER PRODUCTS section on both modules and IC's will help you choose.

• In addition to their presentation beginning on page 10, new products, improvements in performance and price reduction are called out in color in the margin of the page where that product is listed, and by a color block on the table of specifications for that product within a series.

In most cases, the information contained in this GUIDE should provide sufficient information to make a product choice. Of course, additional documentation and application information are available on all of these products from our representative in your area or directly from the factory. Information request cards are attached for your convenience.

Your comments regarding this GUIDE are always welcome, and we thank you for your continued interest in our company, its products and services.

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A WORLDWIDE SERVICE-ORIENTED COMPANY

This 1973 PRODUCT GUIDE reflects Analog Devices' ongoing commitment to provide the user community with the most meaningful product support program. It is this type of demonstrated commitment in all areas of our operation which is user-recognized and which is responsible for our maintaining the position of leadership in our field.

Programs of this nature underscore Analog Devices basic operating philosophy: to understand what the user – designer, researcher, buyer – really needs, and to respond beyond the expected. This objective transcends simply providing the best in products. The objective demands considerations of such factors as: product breadth; product reliability; product availability; product innovations; customer support; and vendor stability.

Unless these criteria are included in your decision making process, you are not exercising your full prerogatives in making the best overall choice.

ANALOG DEVICES, INC.: The company has grown in sales volume from a half-million dollars in 1965 to over \$15 million in 1972. The company employs more than 600 people worldwide. We recently announced and have already begun to implement a five year expansion plan with the objective to become the dominant supplier of devices, modular instruments and subsystems to the instrumentation and control markets. Expansion in sales and earnings is projected at 25 percent per year. The company will continue to offer the broad range of products presented in this PRODUCT GUIDE. We will also expand our technological base in the area of integrated circuits, modular instrumentation and analog input/output peripherals for minicomputers. In addition to continued investment in product development, we continue to seek selective external opportunities in support of our program.

As we entered 1973, we reorganized into a divisional structure comprised of the Modular Instrumentation Division which will concentrate on the development of modular instruments and analog I/O devices, and the Microcircuit Division, consisting of three operating groups which will provide us with the advanced IC technology to meet our internal requirements and those specialized requirements of the open marketplace. The three groups are: Nova Devices in Wilmington, Massachusetts specializing in bipolar thin film IC's; Resistor Products Division in Rochester, New York, specializing in the development of thin film resistor networks and substrates; and our Santa Clara, California operation which will concentrate on high performance monolithic transistors and analog CMOS devices.

Our confidence in the longer term future grows each year as the opportunities accessible to Analog Devices become more visible and our resources continue to develop and mature.

(Analog Devices is a publicly owned company and its stock is traded over-the-counter. NASDAQ symbol: ANLG)







Net Sales

PRODUCT BREADTH: Once dissatisfied users themselves, Analog Devices' founders launched their company in 1965 with a line of high performance operational amplifiers. Since then, the company has continually monitored the market requirements and now offers, at all price/performance levels, a broad range of amplifiers, converters, computation and function modules and accessories in both discrete and integrated circuit packaging. The Analog Devices product line is composed of some three dozen product classifications, and more than 200 models with over 350 standard variations. The continued expansion of our digital panel meter line, the recent introduction of our data control and communication modules, and our ongoing development of bipolar, FET and CMOS integrated circuits are further expressions of our committment to provide special, and often unique, solutions to your broadest range of design problems.

PRODUCT RELIABILITY: Product breadth is irrelevant if the products do not perform as expected. Our products are used in scientific and medical instrumentation, industrial control equipment, environmental systems, aerospace and military systems and other applications characterized by "hostile" conditions or critical operating requirements. Thus,

Active laser trimming used in our IC fabrication is a fast and accurate technique for producing custom trimmed devices on a mass production basis. Although previously used for amplifiers, a recent breakthrough was the application of laser trimming of the thin film resistors directly on the chip of a new internally trimmed monolithic multiplier, AD532. reliability is a paramount consideration. Our wide ranging quality assurance program begins even before a component reaches our receiving dock.

First, we engineer reliability into our products by selecting only the best components suited to the task, and the best production and test methods. Next, our strict vendor qualification and rating procedure assures us that the components we don't make ourselves, meet the quality and performance standards expected of the components we do make, and of the end product we build.







Automatic power supply tester can check a dozen power supplies in a matter of minutes to assure that the units will meet specifications for such parameters as output voltage and output tracking accuracy, line and load regulation, ripple and noise, and short circuit protection. All of our products are subjected to rigid quality assurance procedures.



Our product, performing reliably in your application, is the basis for our overall quality assurance program which also includes: extensive incoming component inspection; selection and grading in a controlled environment; visual and electrical checkouts during assembly; and environmental testing both before and after compensation (for our discrete products). We also have a regular program for burn-in of selected products (168 hours on each digital panel meter, for example), and for checkout and calibration of our testing equipment. Our integrated circuit devices are built to MIL-STD-883 performance specifications; a discussion on this technique can be found in the section on Linear Integrated Circuits.

Quality assurance doesn't end at the shipping dock. Occasionally units will not operate as expected. We have a department whose sole responsibility it is to investigate why products are returned (or rejected in manufacture), and to make recommendations for redesign, for new methods, or for whatever remedial action is necessary. Because of control procedures used during production, components used in our modular products can be traced to source lots, and the unit's production history can be referenced. This ability permits a more thorough analysis of why a unit failed.

In addition to repair work processed in our factories, we also maintain a repair depot in Karlsruhe, West Germany, to service the requirements of our European customers.

In short, our quality assurance program exceeds the boundaries of the usual or standard approaches. We'd rather have our products fail while they are being built, so they won't fail after you get them.

PRODUCT AVAILABILITY: Next to performance, delivery is a most critical product consideration. The more widely specified products in our line are usually shipped directly from inventory. Forecasting techniques for product demand and our computerized raw material availability system provide reasonable assurances that we can meet these general requirements. Our Modular Instrumentation Division in Norwood, Massachusetts, and our Microcircuit Division facilities in Wilmington, Massachusetts, Rochester, New York and Santa Clara, California feature the most up-to-date, advanced techniques to meet virtually any delivery requirement for standard or special units. Our field and factory service staff is continually informed about the scheduled availability of specific items, and can quote specific delivery dates.



A portion of our assembly area in our Modular Instrumentation Division facility is shown here.

CUSTOMER SUPPORT: We won't forget you. Analog Devices maintains several programs to keep users, and other interested parties, informed of new product developments, new techniques and new applications, and to keep us informed of user needs. These programs include: extensive product and application literature; handbooks; buyers' guides; technical seminars; a world wide advertising and technical communications program; and our international journal, ANALOG DIALOGUE. (If you would like to receive this publication, use the information request card in this publication.)

Our customer support program is personalized by more than 150 professional sales engineers in 74 worldwide locations. Our field sales force is comprised of both Analog Devices personnel and representatives, all chosen for their applications expertise. They not only assist the user in understanding our products and business policies, but will lend assistance with applications engineering.

This field force is factory-supported by a team of account service representatives. Each account is assigned to one of these representatives who is responsible to that account to assure all orders are processed efficiently, to answer any questions regarding price and delivery, to inform you of the status of returns, repairs and warranties, and, in general, to assist with all facets of ordering procedures.

Each account is also assigned a factory-based applications service representative to provide technical information and application assistance when this is not readily available from the local representative.

The depth of our total service establishment has been carefully planned to assure that it is as easy as possible to conduct business with Analog Devices.

The wafer diffusion area at our Microcircuits Division facility in Wilmington, Massachusetts is shown here. We recently doubled our facilities at the Nova Devices subsidiary to 25,000 square feet.

50,000 technical people worldwide.

Meaningful technical communications has become synonomous with Analog Devices. Our international technical journal, ANALOG DIALOGUE, for example, is read regularly by some



An AD2010 digital panel meter is shown here undergoing final test and calibration prior to packaging and burn-in.





PRODUCT INNOVATIONS: The same engineering and design expertise which has propelled Analog Devices into the forefront of its industry continues to explore and affect new techniques in product design. Among the many milestones credited to Analog Devices are:

- popularizing encapsulated chopper stabilized op amps and power supplies (most recently, 234)
- the first modular isolation amplifier for critical applications (272)
- the first to develop and manufacture encapsulated D/A converters (MINIDACS)
- first to build a true 16-bit binary D/A converter (DAC-16)
- first to develop and market monolithic current and voltage switches with 12-bit D/A capability and also provide the resistor network (AD550, AD555, AD850 series)
- first high performance, wideband pulse-modulation multiplier (424)
- first noninverting chopper op amp (260)
- first truly self-contained monolithic analog multiplier (AD530)
- first low cost, small, modular 1 microsecond A/D converter (ADC-F)
- first low drift, sub-picoamp, parametric op amp (310/311)
- first laser-trimmed IC FET op amp (AD506)
- first easy-to-apply ultra stable IC op amp (AD504)
- first complete monolithic instrumentation amplifier (AD520)
- first true 16-bit binary A/D converter (ADC-16Q)
- price and size breakthroughs in digital panel meter technology (AD2000 family)
- nonlinear multifunction module (433)

This automatic wave soldering machine complements other facets of our manufacturing facilities geared for volume with quality.

Volume production of our IC products includes automatic wafer scribing. The unit's diamond-tip stylus moves along scribe lines oriented to the crystal lattice structure of the silicon wafer to produce perfectly scribed dice.



Most of these units, or new generation improvements of them, are currently in our product line. And, as we move into 1973 we continue to offer innovative, state-of-the-art advances including:

- revolutionary technique for data control and communications in factory and laboratory applications (SERDEXTM Modules)
- monolithic multiplier whose thin film resistors are deposited directly on the multiplier circuit and then laser-trimmed (AD532)
- super beta transistors that are practical at high voltages (AD815)

These and future design innovations are not the result of engineering for engineering sake but reflect our design response to customers' practical needs, at a favorable pricing structure, and with no compromise in performance.

In addition to product innovations, Analog Devices has constantly demonstrated its leadership position in interpreting product specifications and applications information, for establishing meaningful cataloging standards, and for simplifying the designers' selection and procurement processes. More than 5,000 organizations around the world currently comprise the Analog Devices user community. If yours is one, you have learned to expect these wide-ranging capabilities of Analog Devices described here. Independent surveys compiled from the opinions of professionals like you, consistently reflect enthusiastic preference for Analog Devices' products and services. In fact, a recent study of a leading electronics industry publication ranked Analog Devices in the top 15 companies most preferred of all suppliers in the industry. The reason: confidence in doing business with a leader.

We are certain that this GUIDE, and subsequent updates and new editions, will make it even more convenient to do business with us. To those designers, researchers, and buyers not fully acquainted with Analog Devices, we welcome the opportunity to develop a strong working relationship with you.

March, 1973



The electrical characteristics of the active elements of IC wafers are continually tested in process on a sample basis to insure that the processing is in conformance with the circuit design standards.

NEW PRODUCTS

The following are capsule descriptions of the products introduced by Analog Devices during the past year and scheduled for formal introduction during the next couple of months. In addition to new products, this selection includes brief descriptions of product improvements and product price changes. Additional information on these products can be found on the pages noted, except those entries indicated as "advance information." Unless otherwise stated, these products are currently available.

DATA CONTROL/COMMUNICATION



SERial Data EXchange Modules

A revolutionary data exchange system which permits the interrogation and control of factory, process and laboratory control devices using only a standard teletypewriter was introduced by the Modular Instrumentation Division in March.

Called SERDEXTM Modules, the new system is comprised of five modules which convert parallel output data from devices such as analog-to-digital converters into ASCII serial data that can be handled by a teletypewriter or other similar input/output device. Conversely, the modules translate ASCII serial output data into parallel data required by digital input devices such as D/A converters. Nine standard printing ASCII characters are used to control the operation of the modules, and to control system components such as valves, sensors, motors, pumps, and switches.

Although a SERDEX Module System can be manually controlled from a standard teletypewriter, it can also be readily controlled by any computer with a teletypewriter port. The use of standard ASCII characters permits all computer programming to be done in a high level language such as BASIC or FOCAL. Furthermore, since the only connection to the computer is through the teletypewriter port, no computer hardware interface is required.

SERDEX Module Systems offer substantial cost savings over techniques currently used to handle data control in industrial automation and control systems. The greatly simplified software and the elimination of complex computer hardware interfacing offer not only direct cost savings, but indirect savings since computer professionals are not needed to design and implement the system.

All of the modules within the system can be interconnected with inexpensive, easy-to-use twisted pair wires instead of the generally required shielded cabling whose cost can exceed that of the hardware with which it is used.

The data is transmitted over the twisted pair wire via standard 20mA optically isolated current loops. This results in highly reliable data transfer even in the presence of very high common mode noise likely to be found in industrial environments.

SERDEX Modules In Detail

The five units which comprise the SERDEX Module family are: a serial data transmitter, STX1003; a serial data receiver, SRX1005; two modules which make up a multiplexer, SMC1007/SMX1004; and a clock, SCL1006.

When commanded, the serial transmitter will initiate a conversion in an A/D converter, and, after the conversion, send back the output data to the terminal or computer that requested it.

The serial receiver receives up to 8 data characters (or more if expanded with external circuitry) which can be used to supply input data to a D/A converter or other digital input devices.

The multiplexer, which consists of two module types, allows a single teletypewriter or computer to control a total of 8 or 16 transmitters and receivers. It is addressed from the controlling terminal or computer, and more than one rank of multiplexing may be used, resulting in unlimited system expansion capability.

The clock module is an accessory module that supplies clock pulses and -15V power to the other modules in the system. One is required at each module location.

All SERDEX Modules feature 0.025'' square wire wrapping pins, and require only +5 volts power. The STX1003 transmitter, SRX1005 receiver, and SMC1007 multiplexer are each housed in a $4.25'' \times 3.3'' \times 0.625''$ case. The SMX1004 multiplexer and SCL1006 clock are each in cases measuring 2.1''-x $2.1'' \times 0.6''$.

SERDEX Modules are controlled by nine standard ASCII characters: ? / = * ! % ' and #

Depending upon the mode of operation, interrogation or control, these characters represent different commands. In operation, SERDEX Modules will ignore all extraneous, user generated inputs into the system. For instance, in the statement: WHAT IS THE LEVEL IN THE TANK? the SERDEX Modules will act only upon the control character that was transmitted, namely the question mark.

This feature allows the user either during manual operation with a teletypewriter, or when programming for computer control, to use logical English statements in conjunction with the minimal instruction set.

Complete information on SERDEX Modules is available from the factory or your local Analog Devices' representative.

NEW DEVELOPMENTS IN TECHNOLOGY: CMOS

A new technology - - Complementary Metal Oxide Semiconductor (CMOS) - - is used for a new generation of analog and digital/analog interface products which will soon be available from Analog Devices, Inc. This technology allows for simpler designs and great reduction in power dissipation for a particular function.

CMOS QUAD SWITCH - AD7510, AD7510A

The AD7510 and AD7510A consist of four independent switches controlled by TTL, DTL or CMOS compatible logic. The switches have an "ON" resistance of about 70Ω with extremely low "standby" power - dissipation (below 5μ W). (Availability: May 1973.)

CMOS 8 CHANNEL MULTIPLEXER - AD7501, AD7502

The AD7501 is a single 8 channel multiplexer controlled by TTL, DTL or CMOS compatible logic, while the AD7502 is a differential 4 channel multiplexer. Both units have an "ON" resistance of about 200Ω with a "standby" power dissipation below 5μ W. (Availability: May 1973.)

DIGITAL PANEL METERS



Analog Devices pioneered the design of +5VDC logic-powered DPM's, introducing the first model, the AD2001, in 1971. By powering the DPM from +5VDC, the size and cost of the DPM was markedly reduced, AC power line noise pickup was reduced and increased reliability was achieved. In the last year, Analog Devices introduced four more +5VDC powered DPM's, offering a model for nearly every application. The DPM line offered by Analog Devices will be augmented in 1973 with additional designs including AC line-powered units. (Page 116)

AD2010, 3½ DIGITS, LOW COST, SMALL SIZE, LED DISPLAY, RATIOMETRIC OPTION. The AD2010 is a general purpose DPM, utilizing LED display packaged with MSI counters and latches to greatly reduce the overall design complexity, size, and cost. A ratiometric option allows measuring voltages compared to an externally supplied reference voltage. Leading zero suppression can be initiated externally.

AD2004, 4½ DIGITS, HIGH PERFORMANCE, ISOLATED IN-PUT, LED DISPLAY. The AD2004 has a floating optically isolated analog section to provide excellent common mode rejection (120dB) at high common mode voltages (±300V). The LED display section contains MSI counters and latched data outputs.

AD2003, $3\frac{1}{2}$ DIGITS, HIGH PERFORMANCE, NUMITRON DISPLAY. The differential input of the AD2003 provides 80dB of common mode rejection at common mode voltages of ± 2.5 V. The display uses large RCA Numitron tubes with a green filter matched to the response of the human eye.

AD2002, 2½ DIGITS, LOW COST, ANALOG METER RE-PLACEMENT, NUMITRON DISPLAY. The AD2002 is a unipolar, single-ended DPM designed to be competitive in cost with high accuracy analog meters. BCD data outputs are optional.

AD2006, AC LINE-POWERED DPM (ADVANCE INFORMA-TION). For those applications requiring a DPM powered by AC line power, Analog Devices has designed the AD2006, a $3\frac{1}{2}$ digit panel meter using Sperry gas discharge displays. The AD2006 has a bipolar, differential input with a full scale range of 0 to ± 1.999 V. Maximum error is 0.05% of reading ± 1 digit. The ratiometric option allows measurement of voltages compared to an externally supplied voltage. Common mode rejection is 70dB at common mode voltages of ± 300 V (± 5 V with digital interface connections). The AD2006 is internally set for 5 conversions per second; external triggering can provide up to 90 conversions per second without display. AC power is connected on a separate rear panel terminal strip for lower noise pickup and greater safety. Pricing and availability: summer 1973.

AMPLIFIERS (MODULAR)



WIDE BANDWIDTH FAST SETTLING (Page 44)

MODEL 50 SETTLING TO 0.1% IN 90ns: Model 50 features an 100MHz gain bandwidth product, settling time of 90ns to 0.1%, and an output capability of 100mA. Slew rate sensitivity and settling time for an LSB step are far better than anything previously available.

Drift is only $15\mu V/^{\circ}C$ (Model 50K), and when operated in a bandwidth of 5Hz to 2MHz, noise is only $8\mu V$ rms.

LOW NOISE, LOW DRIFT FET AMPLIFIER (Page 40)

MODEL 43K, $5\mu V/^{\circ}C$ DRIFT: Designed for low level signal processing, the Model 43K is an update on the 43J design which combines low drift of $5\mu V/^{\circ}C$ with low noise of $2\mu V$ rms in a 10kHz bandwidth. The differential FET inputs, with bias currents of only 10pA, may be operated in both inverting and non-inverting applications. The full power bandwidth and slew rate have guaranteed specifications of 200kHz and 12V/ μ sec, respectively.

HIGH VOLTAGE AMPLIFIER (Page 54)

ANALOG

ANALOG

MODEL 171, $\pm 150V$ FET AMPLIFIER: Designed for applications such as high voltage buffers, followers with gain, and high voltage integrators, Model 171 can be operated from a wide range of inexpensive power supplies. Power Supply Rejection is 7μ V/V and CMR is greater than 100dB.

ISOLATION AMPLIFIER (Page 58)

MODEL 274J, GAIN 1-100 WITH A SINGLE RESISTOR: A new amplifier with additional isolation features and externally adjustable gains, allows low-level signals to be amplified using either its ECG or EEG input terminals. It also has $\pm 10V$ output swing, transformer isolation of the power source from the output as well as the input, and a choice of input terminals for applications, such as EEG's, and low noise industrial applications, in which lower noise may be traded for protection (e.g., from direct application of defibrillators).

INSTRUMENTATION AMPLIFIER – IMPROVED PER-FORMANCE (Page 56)

MODEL 605, EXCELLENT LINEARITY AND LOW DRIFT: Model 605, offering CMR of 70dB with a 1k Ω source unbalance, nonlinearity of 0.005% and RTI drift to 0.5μ V/°C now has improved RTO drift. Drift of 150μ V/°C has now been reduced to 100μ V/°C for the J version, 75μ V/°C for 605K and 50μ V/°C for the 605L. These improved specifications are being offered at no additional cost.

ELECTROMETER AMPLIFIERS – IMPROVED SPECIFICA-TIONS (Page 52)

MODEL 42, BIAS CURRENT TO 75fA DRIFT TO $25\mu V/^{\circ}C$: The popular Model 42, long recognized as an excellent electrometer amplifier, now has dramatically improved specifications. The key parameters for electrometer applications, offset voltage drift and bias current, can now be selected to $25\mu V/^{\circ}C$ and 75fA, respectively, on Model 42L. Model 42J and Model 42K offer similar improvements. And all are offered in a small 1 1/8" package at very low cost.

LOW NOISE CHOPPER AMPLIFIER (ADVANCE INFORMATION)

MODEL 261, GUARANTEED NOISE OF LESS THAN $1\mu V$: The Model 261 is a second generation design which typically provides a significant improvement in the noise and bandwidth characteristics of Model 260 and other competitive models. Operating at a higher carrier frequency, this non-inverting design features extremely low noise, $0.4\mu V$ p-p in a 1Hz bandwidth; low drift, $0.1\mu V/^{\circ}$ C; and an output that is virtually free of chopper spikes.

Model 261 also offers a solution to beat frequency problems caused by a low frequency carrier mixing with harmonics of the AC line. The carrier frequency on this design is nearly a decade higher than that of models previously available, thereby eliminating the possibility of any interaction with the line frequency or its harmonics.

The new model should be considered for all new instruments and circuit applications, or wherever improved performance,

at no increase in cost, is desirable for existing sockets. Models 260 and 261 are mechanically and electrically interchangeable for these applications.

Model 261 will be available in production quantities by June of 1973. Evaluation units are currently available.

FAST SETTLING – PRICE REDUCTION (Page 44)

MODEL 48, SETTLING TO 0.01% IN 500ns MAX: Model 48, an ultra fast differential amplifier, has a 15MHz bandwidth, settles to 0.01% in 300ns typical (500ns max), has a CMR of 80dB, and slews at $125V/\mu s$. The new price reduction now makes this amplifier the best choice for high speed applications requiring 20mA or less of output current.

CONVERTERS





LOW COST DUAL SLOPE A/D (Page 94)

ADC1100, 3½ BCD DIGITS PLUS SIGN: A compact module ideally suited for use in data acquisition systems, or for driving a display, or for doing both jobs at the same time. It has an input range of ± 199.9 mV, but the input can withstand up to ± 20 V indefinitely without damage.

The unit features automatic zero correction before each conversion, and a gain temperature coefficient of less than 50ppm/°C over its full operating temperature range of 0 to +70°C. The only power required is +5.00VDC. The ADC1100 can be set for a normal mode noise rejection ratio of at least 40dB for either 50Hz or 60Hz power line noise. All logic inputs and outputs are TTL compatible.

HIGH SPEED A/D (Page 96)

ADC1103, 12 BITS IN 3.5 μ s: A very high speed A/D converter in a compact 2" x 4" module. Designed for high speed data acquisition systems and other applications requiring high throughput rates. It employs the successive approximation technique to perform an 8 bit conversion in 1.0 μ s, a 10 bit conversion in 1.2 μ s, or a 12 bit conversion in 3.5 μ s.

Three user-selected input ranges are available: 0 to +10V, \pm 5V, \pm 10V. Output coding can be natural binary, offset binary, or two's complement. There are no missing codes from 0 to +50°C. Differential nonlinearity error is \pm ½LSB maximum. All logic inputs and outputs are TTL compatible.

LOW COST SUCCESSIVE APPROXIMATION A/D (Page 90) ADC-12QZ, 12 BITS IN 40 μ s FOR ONLY \$129: A low cost general purpose 12 bit successive approximation A/D converter offering 40 μ s conversion time, ±½LSB maximum differential nonlinearity error, and a gain TC of ±30ppm/°C maximum. It has no missing codes from 0 to +50°C.

The ADC-12QZ is packaged in a $2'' \times 4'' \times 0.4''$ module, and offers four user selected input ranges: 0 to +10V, 0 to +5V, $\pm 10V$, $\pm 5V$. Output coding can be natural binary, offset binary, or two's complement. An easy-to-use serial data output is provided, and all logic inputs and outputs are fully TTL compatible.

HIGH RESOLUTION SAMPLE-AND-HOLD (Page 100) SHA-6, SETTLES TO 0.00075% IN 5ms: A 2" x 4" x 0.4" sample-and-hold amplifier designed as a companion to Analog Devices' ADC-16Q 16 bit A/D converter. It will acquire and hold an input signal to 16 bit accuracy long enough for the ADC-16Q to convert it.

Careful design and layout, an instrumentation amplifier-type input buffer, and high-stability resistor networks with excel-

lent tracking TCR's are used. This results in the SHA-6 being stable over temperature within 2ppm/°C, and over time within 2ppm/month.

SYNCHRO/DIGITAL CONVERSION PRODUCTS (Page 102)

A new line of synchro/digital conversion products was added early in 1973. The line initially is comprised of a 14-bit S/D converter series (SDC1602), a 10-bit S/D converter series (SDC1604), and a 5-digit synchro angle display meter (API1617). The SDC1602 features 14-bit resolution ± 1 arc-minute error, 1440°/second tracking rate and is less than 7 cubic inches in size. The SDC1604 with 10-bit resolution (1024:1) and 30' accuracy provides excellent performance in applications that do not require the exacting 14-bit resolution of the SDC1602.

The API1617 angular position indicator provides LED readout and a BCD or binary output of angles from 0° to 359.98° (continuous rotation), with 0.02° resolution $< 0.05^{\circ}$ error, at tracking speeds up to 1440°/second.

FUNCTION MODULES





DIVIDER WITH VARIABLE GAIN (Page 137)

MODEL 434, $e_0 = Y \frac{Z}{X}$, ACCURACY TO ¼%: Similar to Model 433 in design, Model 434 has been optimized for divider

applications. Accuracy can be held to within ¼% over a signal range of 100mV to 10V without the use of any external trims. External trimming may be performed, if desired, to eliminate offsets at the temperature of concern.

MULTIFUNCTION MODULE (Page 137) MODEL 433B, 4% ACCURACY, $e_0 = Y \left(\frac{Z}{X}\right)^m$: During

1972, an extremely versatile function module, Model 433J, was introduced to implement a wide range of computational circuits. Capable of raising ratios to a power and multiplying by a third variable, the 433J provides ½% accuracy over a signal range of 100:1.

Model 433B has all the capabilities of Model 433J, but has twice the accuracy, $\frac{1}{4}$ % vs. $\frac{1}{2}$ %, and guaranteed temperature performance over the range of -25° C to $+85^{\circ}$ C. The 433B also has a lower intial offset and offset vs. temperature.

VOLTAGE/CURRENT LOG RATIO (Page 143)

MODEL 756, ½% ACCURACY, LOW COST, SMALL PACKAGE: Designed primarily for photometer applications, Model 756 is a general purpose log ratio module capable of processing input signals spanning four decades.

This design improves on log modules previously available in that it may be used to process either voltages or currents, and both inputs are continuously variable signal inputs.

HIGH OUTPUT POWER REGULATED SUPPLY (Page 144)

MODEL 920, ± 15 Volts at $\pm 200mA$: Model 920, the latest addition to the modular power supply line, features a clean regulated output of up to 200mA at ± 15 volts. Operating from 115VAC input, this design provides a higher output current than the popular Model 902 (+15VDC at 100mA), and sacrifices nothing in reliability. It is packaged in a black anodized aluminum case, which guarantees a low thermal resistance path for internally generated heat.

POWER SUPPLY

INTEGRATED CIRCUITS



DUAL SUPER BETA NPN TRANSISTORS AT HIGH BREAK-DOWN VOLTAGES (Page 187)

AD814 SERIES: Betas of 1000 and 2000 min are achieved with respective breakdown voltages of 35V and 20V. The AD814, AD815 and AD816 are manufactured using a proprietary NPN transistor process and advanced silicon nitride passivation techniques. Offsets of less than 1mV and drifts of less than $5\mu V/^{\circ}C$ make these devices ideal for extremely high gain differential input stages.

LOG CONFORMANCE DUAL NPN TRANSISTORS (Page 188)

AD818: The AD818 dual NPN transistor is specifically designed for excellent conformance to the ideal logarithmic relationship between V_{BE} and I_E over a wide collector current range, up to 1mA. The AD818 also exhibits very low voltage noise (2nV/ $\sqrt{\text{Hz}}$ @ 10Hz) and low collector saturation levels.

DUAL MONOLITHIC PNP TRANSISTORS (Page 189)

AD820 SERIES: The AD820, AD821 and AD822 are small signal, dual monolithic PNP transistors providing high gain over wide collector current ranges and voltage breakdowns in excess of 60V. The excellent matching characteristics guarantee offsets of less than 0.5mV and drifts better than 2.5μ V/°C.

EXTREMELY LOW NOISE DUAL MONOLITHIC FETS (Page 184) AD840 SERIES: TRAK-FETSTM AD840, AD841 and AD842 are large geometry, dual monolithic silicon N-channel J-FETS designed for super low voltage noise, less than $15nV/\sqrt{\text{Hz}}$ @ 10Hz, and outstanding matching characteristics: 5mV and $5\mu V/^{\circ}C$ (AD840).

These units are ideal for sensing very small signals from high impedance transducers commonly found in biomedical, optoelectronic and nuclear applications.

HIGH TRANSCONDUCTANCE, WIDEBAND DUAL FETS (ADVANCE INFORMATION)

2N5911/AD845 SERIES: The 2N5911/5912 are dual hybrid FETS with very high transconductance and low input capacitance. The AD845 and AD846 are monolithic versions of the 2N5911 and 2N5912 respectively. These dual FET's are excellent performers for frequencies up to 100MHz. (Availability: June 1973.)

HIGH ACCURACY FET-INPUT OP AMP (Page 151)

AD506L: The AD506L is a low drift, high accuracy FET-input operational amplifier which combines the low current characteristics typical of FET amplifiers with the offset voltage stability commonly found only in bipolar devices. The AD506L features bias currents below 5pA max and maximum offset voltage drifts of $10\mu V/^{\circ}C$.

LOW COST FET-INPUT OP AMP (Page 153)

AD540J: The AD540J is the lowest priced, high performance IC FET-input operational amplifier available which provides the user with low bias currents, high overall performance and accurately specified operation. The device achieves a maximum bias current of 50pA, minimum gain of 20,000, CMRR of 70dB and a slew rate of $6V/\mu$ sec.

LOW DRIFT, LOW NOISE OP AMP (Page 157)

AD504M: The AD504M is the lowest drift, lowest noise, high accuracy IC operational amplifier available. The device achieves a maximum nulled offset drift of 0.5μ V/°C, minimum gain of







 10^6 , and $0.6\mu V$ (p-p) maximum input noise voltage (0.1Hz to 10Hz bandwidth).

LOWEST COST, HIGH ACCURACY OP AMPS (Page 158) *AD741J/S:* The AD741J and AD741S are high accuracy versions of the industry standard AD741C and AD741. In addition, both devices offer the user the further advantages of high guaranteed output current and gain at low values of load impedance. The AD741J and AD741S guarantee a minimum gain of 25,000 swinging $\pm 10V$ into a $10k\Omega$ load.

AD301AL: The AD301AL is the highest accuracy version of the popular AD101A, AD201A, AD301A series of operational amplifiers. The AD301AL provides substantially increased accuracy by reducing the errors due to offset voltage (0.5mV max), offset voltage drift $(5\mu V/^{\circ}C max)$, bias current (30nA max), offset current (5nA max) and CMRR (90dB min).

WIDEBAND FAST SLEWING OP AMP (Page 163)

AD507S: The AD507S is a low cost, monolithic operational amplifier that is designed for general purpose applications where high gain bandwidth and speed are significant requirements and operation over the extended temperature range is essential. The device also provides excellent dc performance with maximum bias and offset currents (15nA), maximum offset voltage of 4mV, and a guaranteed maximum offset voltage drift of $20\mu V/^{\circ}C$ from -55°C to +125°C.

HIGH SPEED, FAST SETTLING OP AMP (Page 164)

AD509: The AD509J, AD509K and AD509S are monolithic operational amplifiers specifically designed for applications requiring fast settling times to high accuracy. The AD509K and AD509S are 100% tested and guaranteed to settle to 0.1% in 500nsec maximum and 0.01% in 2μ sec maximum, while typically the settling times are faster.

HIGH SPEED, LOW COST OP AMP (Page 165)

AD518: The AD518J, AD518K and AD518S are precision high speed monolithic operational amplifiers designed for applications where high slew rate and high bandwidth are required, but low cost and ease of use are essential. The devices are internally compensated for unity gain applications with a 60° phase margin to insure stability, a minimum slew rate of $50V/\mu$ sec and a bandwidth of 12MHz.

INTERNALLY TRIMMED, MONOLITHIC MULTIPLIER (Page 170)

AD532: The AD532 is the first fully trimmed monolithic multiplier/divider. It requires no external networks or op amps to achieve 1% accuracy (AD532K) at full scale, ± 10 volts. It is pin compatible with the popular AD530, but features differential inputs for even greater flexibility and ease of use.

QUINT SWITCH FOR D/A AND A/D CONVERTERS (Page 174)

AD552, 120nsec SETTLING, FULL TTL COMPATIBILITY: The AD552 expands the popular AD551 quad current switch to five bits for 5 and 10 bit converter applications. It features fast settling time and is supplied in the 16-pin ceramic dualin-line package.



AMPLIFIER PRODUCTS

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AMPLIFIER PRODUCTS

WHICH AMPLIFIER FOR THE JOB

Selecting the best amplifier for a particular application has become almost an art when you consider the overwhelming proliferation of both operational amplifiers and committed gain amplifiers in recent years. During 1971, Analog Devices made several significant advances in operational amplifier design. Proprietary monolithic designs (IC's) moved ahead strongly with improved bias current, drift and speed characteristics challenging the high performance of today's better discrete component devices. These include both FET and bipolar input circuits.

By the same token, discrete designs also moved ahead especially in the area of fast settling and low drift amplifiers. No longer can it be said that designers should consider discretes for higher performance and monolithics for moderate performance, small size or economy. Economy and performance are now available in either form factor, making the selection process more complex than a year ago.

In the area of committed gain amplifiers, Analog Devices has added new designs which represent major improvements over models previously available. For data acquisition requirements, high speed and low drift have been achieved in its new instrumentation amplifiers. For medical and industrial applications, isolation amplifiers appear for the first time to satisfy patient safety and equipment isolation requirements.

The following sections are intended to guide the user to the best amplifier for his application whether he be expert or new-comer to the art of selecting amplifiers. The extent of his familiarity with amplifier types and their specifications will determine how rapidly he moves to his final decision.

HOW AMPLIFIERS ARE CLASSIFIED

To assist the designer in distinguishing among the multitude of models, many with comparable specifications, Analog Devices has listed all amplifiers in this catalog by application class. Identifying a key parameter will usually lead the designer to the best amplifier for his job. To assist in the selection process, the chart below ties the key application parameters to the relevant amplifier class which can then be located on the designated page.

Classification of Amplifiers

To assist you in selecting the best amplifier for the application, we have classified products into eleven cate-

Key Feature	Application	Amplifier Classification	Page
Low drift and noise, long term stability	Medical and industrial, transducers, amplifiers, preamps	Low drift chopper Low drift differential	48 50
Low bias current	High source impedance, integrators, charge amplifiers	General purpose FET electrometer	52
Wideband and fast settling	D/A, A/D converters, sample and holds, comparators	Wide bandwidth fast settling	44
Economy, moderate performance	Function generators, general designs, active filters	General purpose bipolar General purpose FET	38 40
High CMRR, CMV	Long cable transmissions, noisy signal environments, instrument preamps	Isolation Instrument	58 56
Input-output isolation	Medical patient safety currents, isolation, programmable equipment	Isolation	58
Battery operation	Portable equipment, low noise, preamps	Low drift differential	50
Log or antilog	Signal compression, linearization, photometric ratios	Logarithmic	139
Voltage and/or current booster	Audio and servos, power regulators, galvanometers, current source	High output capability	54

gories. In doing this we have established what we believe to be the optimum point of departure for proper amplifier selection. In some exceptional cases, an amplifier has been included in more than one category because of its outstanding versatility. But in most instances we have focused on one single attribute or key parameter for amplifier classification. For example, the chopper stabilized group focuses on low drift, but includes several models which could qualify for high output capability or wide bandwidth. We believe that low drift is the key feature.

Many designers are faced with the problem of selecting the best amplifier whether it be a microcircuit or discrete component module. To ease their task, Analog Devices has listed these devices together in this amplifier section making direct comparisons more convenient. The monolithics are also listed separately in their own section and should be referred to there when the choice must clearly be a microcircuit device.

1. General purpose - moderate performance

Amplifiers in this group include Analog's lowest cost devices. They are best suited for general purpose designs with moderate drift requirements in the range from 5 to $75\mu V/^{\circ}C$, unity gain bandwidths to 1MHz, and full power response to 100kHz. Typical applications include summing, inverting, impedance buffering (followers) and active filtering. They are also useful for developing nonlinear transfer functions.

2. General purpose FET - low bias current, high $Z_{\rm IN}$

These models should meet most design requirements, especially those which cannot be satisfied by bipolar input designs because of excessive bias currents or too low input impedance. The lower bias currents (1 to 100pA) and higher input impedances (10¹¹ ohms) of FET's make them a natural choice when amplifier gain networks exceed 100k ohms and it is necessary to minimize input loading and current offset errors for improved accuracy. Significant applications include integrators, sample and hold amplifiers, current to voltage converters and low bias current log circuits.

3. Wide bandwidth - fast settling

Amplifiers in this group feature both differential FET and bipolar input stages which afford a wide choice of drift and bias current specifications. They emphasize exceptionally fast response and wide bandwidths (to 40MHz, 100ns settling) for applications in data acquisition and pulse data transmission systems. Critical specifications are step response settling time, full power response and current output. These amplifiers are useful for sample and hold circuits, A/D converters or as high speed buffers and integrators. Offering high output current capability, they should be considered for video or line driver circuits, D/A output amplifiers or as deflection coil amplifiers.

4. Low voltage drift - chopper stabilized

These amplifiers are widely accepted as the best choice when it is essential to maintain low voltage offsets and bias currents with time and temperature or whenever external offset adjustments are not practical in the application. Using carrier modulation techniques, these designs achieve bandwidths to 20MHz, drifts to $0.1\mu V/^{\circ}C$ and long term stability of $2\mu V$ /month. Typical applications include error summing amplifiers for servo loops, precision regulators, or as input amplifiers for laboratory grade metering instruments and test equipment.

5. Low voltage drift - differential input, high CMRR

"Chopperless" low drift designs with differential inputs should be considered for high accuracy instrumentation, low level transducer bridge circuits, precision voltage comparators and for impedance buffer designs. In general, they should be selected over single ended choppers where a differential input is required or whenever possible chopper modulation spikes are objectionable in the circuit design.

Amplifiers in this group feature differential bipolar transistor input stages achieving input drifts as low as $1/4 \ \mu V/^{\circ}C$, offset voltages to $100 \mu V$ and exceptionally stable long term drifts of $3 \mu V$ /month. These devices offer differential performance with input noise of $1 \mu V$ p-p, a CMV of 10V and 100d3 of CMR. For comparison, chopper stability approaches $1 \mu V/$ month but they are useful as single ended amplifiers only.

6. Electrometer - ultra low bias current

Amplifiers with bias currents less than 1pA are classified as suitable for electrometer use where frequency response and voltage drift are usually secondary requirements. Both varactor bridge and FET input designs are employed to achieve these bias currents ranging from one picoamp (10^{-12} A) to ten femptoamps (10^{-14} A) . These amplifiers are used as current-to-voltage converters with high impedance transducers such as photomultiplier tubes, flame detectors, pH cells and radiation detectors.

7. High output - voltage/current

Amplifiers offered here have bipolar or FET inputs with output voltage swings of ± 20 volts or output current to ± 100 mA. Also included is model B100, a 100mA wideband booster for op amps. Typical applications include audio amplifiers, voltage or current regulators and driver stages for sonar transducers, galvanometers and deflection coils.

8. Instrumentation

The instrumentation amplifier is a committed gain amplifier with internal precision feedback networks. Its excellent drift, linearity and noise rejection capability make it a natural choice for extracting and amplifying low level signals in the presence of high common mode noise voltages. These devices are commonly used as transducer amplifiers for thermocouples, strain gage bridges, current shunts and biological probes. As preamplifiers they are capable of extracting small differential signals superimposed on large common mode voltages. Wideband designs are also available for data acquisition systems.

9. Isolation - medical, industrial

Isolation amplifiers are committed gain designs with FET inputs and total ground isolation between input and output signals. With 120dB of CMR, they are useful for processing millivolt signals in noisy environments (up to 1000 volts CMV) or for interrupting ground loops in medical or industrial applications. Using carrier modulation techniques and fail safe designs, the isolation amplifier is an excellent choice for ECG patient amplifier designs, offering complete patient protection, and for off-ground measurement systems.

10. Logarithmic Amplifier and Elements

Log modules from Analog Devices develop the instantaneous value of the log or antilog of an input signal. Contrary to communications type log amplifiers, which basically compress AC signals, the 700 series log modules operate on single polarity inputs from DC to an upper cutoff frequency. These temperature-compensated designs will work over 6 decades of input current (1nA to 1mA) and 4 decades of voltage (1mV to 10V). Typical applications include transducer linearization, data compression and basic computational circuits for acoustical and optical instruments in chemical, medical and industrial design.

11. Comparators

Comparators in this group are specialized operational amplifiers with differential inputs and two bi-stable output states. They are available with either FET or bipolar input stages and have been optimized for stable switching and threshold characteristics. These devices are useful as threshold level detectors for A/D converters, voltage to frequency converters, pulsewidth modulators and a wide variety of square wave and pulse generators.

HOW TO SELECT OPERATIONAL AMPLIFIERS

INTRODUCTION

In selecting the right device for a specific application, you should have clearly in mind your design objectives and a firm understanding of what published specifications mean. Beyond this, you should detail the significant variables that are pertinent to your application. The purpose of this section is to put these many decision factors into perspective to help you make the most meaningful buying decisions.

To properly choose an operational amplifier for any given set of requirements, the designer must have:

> 1. A complete definition of the design objectives. Signal levels, accuracy desired, bandwidth requirements, circuit impedance, environmental conditions and several other factors must be well defined before selection can be effectively undertaken.

2. Firm understanding of what the manufacturer means by the numbers published for the parameters. Frequently, any two manufacturers may have comparable published specifications, which may have been arrived at using differing measurement techniques. This creates a pitfall in op amp selection. To avoid these difficulties, the designer must know what the published specifications mean and how these parameters are measured. He then must be able to translate these published specifications in terms meaningful to his design requirements. In the following discussion, Analog Devices provides the designer: 1) a checklist which he can apply to his application to assure that all significant factors are taken into account; 2) meaningful definitions for each of our published specifications; and 3) illustrations of how the requirements of his design are translated in terms of these specifications to help make an effective and economical choice.

APPLICATION CHECKLIST

By way of an application checklist, the designer will need to account for the following:

Character of the application: The character of the application (inverter, follower, differential amplifier, etc.) will often influence the choice of amplifier. Chopper stabilized amplifiers, for example, are not generally applicable where differential inputs are required.

Accurate description of the input signal: It is extremely important that the input signal be thoroughly characterized. Is the input a voltage source or current source? Range of amplitude? Source impedance? Time/frequency characteristics? *Environmental conditions:* What is the maximum range of temperature, time, and supply voltage over which the circuits must operate (to the required accuracy) without readjustment?

Accuracy desired: The accuracy requirement determines the extent to which the foregoing considerations are critical, and ultimately points the way to a device (or series of devices) which are acceptable. Accuracy must, of course, be defined in terms meaningful to the application with regard to bandwidth, DC offset, and other parameters.

SELECTION PROCESS

In general, the objective of amplifier selection should be to choose the least expensive device which will meet the physical, electrical, and environmental requirements imposed by the application. This suggests that a "General Purpose" amplifier will be the best choice in all applications where the desired performance requirements can be met. Where this is not possible, it is generally because of limitations encountered in two areas — bandwidth requirements, and/or offset and drift parameters.

To make it easier to relate bandwidth requirements with the drift and offset characteristics, a capsule view of bandwidth considerations precedes the DC discussions below. The reader is then returned to an expanded discussion of gainbandwidth considerations.

Gain Bandwidth Considerations, A Capsule View

Although all selection criteria must be met simultaneously, determination of the bandwidth requirements is a logical starting point because:

A) If DC information is not of interest, a suitable blocking capacitor can usually be connected at the amplifier input and all of the "drift" specifications may be ignored, and

B) Where high frequency (>10MHz) characteristics are of primary importance, the choice will be limited to those amplifiers designated "Wide Bandwidth/Fast Settling."

Where DC information is required and where frequency requirements are relatively modest (full power response below 100kHz, unity gain of less than 1.5MHz) other criteria will probably influence the final choice. It is important, however, to choose an amplifier with which an adequate value of loop gain is assured (at the maximum frequency of interest) to obtain the desired accuracy. Loop gain is the excess of open loop gain over closed loop gain, and is responsible for the diminishing error due to fluctuations in the open loop gain due to time, temperature, etc. Typically, a loop gain of 100 will yield an error of no more than 1%, 0.1% from loop gain of 1000, etc. Where undistorted response is required, the specifications for full linear response and slewing rate should be chosen such that they are not exceeded at the highest frequency of operation.

Offset and Drift Considerations

In the majority of op-amp applications, final selection is determined by the DC offset and drift characteristics. To undertake amplifier selection in these cases, it is necessary to translate the requirements listed above as follows. (It is assumed that bandwidth requirements have been established at this point.)

1. What input impedance must the circuit present to the signal source? This depends primarily on the source impedance, R_s , and the amount of loading error which is acceptable. Most amplifier circuits are designed around either the inverting or noninverting circuit of Figure 1. The choice is often made between the two to accommodate the impedance requirement. Input impedance for the inverting circuit is approximately equal to the summing impedance, R_i and the upper limit on the magnitude of R_i is determined by the allowable drift error because of input bias current as discussed below. The noninverting circuit offers inherently higher input impedance than the inverting circuit (due to "bootstrapping" feedback) and in this case input impedance of the amplifier R_{cm} .

2. How much drift error can be tolerated? The question is related to the input signal level, e_s , and the required accuracy. For example, to amplify or otherwise manipulate a DC input signal of one volt with an accuracy of 0.1%, the offset drift error, V_d , must be one millivolt or less. (This assumes that other sources of error such as input loading, noise and gain error have already been allowed for.) By the same reasoning, the allowable drift error for a 1 volt signal and 0.01% accuracy would be $100\mu V$.

When this has been defined, the allowable limits of offset voltage (e_{os}) , bias current (i_b) , and difference current can be calculated by the equations of Figure 1.

Figure 1 gives the equations which relate offset voltage (e_{OS}) , bias current (i_b) , difference current (i_d) and the external circuit impedances to the drift error, V_d , for both the inverting and the noninverting circuits. From these equations it can be seen how the input impedance requirements of the foregoing paragraphs are related to the drift error.

For example, in the case of the inverting circuit, an offset error voltage, $i_b R_i$, is generated by the bias current flowing through the summing impedance. This error increases for increasing R_i . Since R_i also sets the input impedance, there is a conflict between high input impedance and low offset errors. Likewise, for a given offset error, higher values for R_i can be used with an amplifier which has lower bias current.

Where it will otherwise function properly, the noninverting circuit generally makes a better choice for high input impedance circuits. Also, for the same source and input impedance requirement, a given amplifier will generate lower offset errors for the noninverting circuit than for the inverting circuit. This is so because the bias current flows only through R_s for the noninverter and this will always be less than the input impedance, R_i , of the inverter. Input impedance of the noninverter (approximately R_{CM}) is typically 10^7 ohms even for the least expensive bipolar amplifiers and up to 10^{11} ohms for FET types.

Unfortunately, however, the noninverting configuration can not always be used since it will not perform many circuit functions such as integration or summation. A further limitation occurs in high accuracy applications, where common mode errors may rule out this circuit configuration.

Initial offsets can usually be zeroed at room temperature so that only the maximum temperature excursion (Δ T) from +25°C need be considered. For example, over the range of -25 to +85°C, the maximum temperature excursion (Δ T) from +25°C would be 60°C. As a practical matter, offset errors due to supply voltage and time drift can generally be neglected since errors due to temperature drift are usually much greater.



Current Amplifier Considerations

Before leaving the subject of offset errors, we shall discuss briefly the current amplifier configuration which is shown in Figure 2A. The obvious approach to measuring current is to develop a voltage drop across a load resistor, R_f , and to measure this potential with a high impedance amplifier as shown in Figure 2B.

This approach has several disadvantages as compared to the circuit of Figure 2A. First the noninverting amplifier introduces common mode errors which do not occur for Figure 2A. Second, an ideal current meter would have zero impedance whereas, R_f in Figure 2B may become very large since this resistor determines the sensitivity of the measurement. Third, the changes of input impedance, R_{cm} , for the noninverting amplifier with temperature will cause variable loading on R_f and hence a change in sensitivity.

The current amplifier of Figure 2A circumvents all of these difficulties and approaches an ideal current meter; that is, there is essentially no voltage drop across the measuring circuit, since with enough open loop gain, A, the input impedance R_{IN} becomes very small.

In selecting a current amplifier, the most important consideration is current noise, and bias current drift. Measuring accuracy is largely the ratio of current noise and drift to signal current, i_s. To obtain the drift of error current I_{ϵ} referred to the input, use the following expression.

$$\Delta \mathbf{I}_{\boldsymbol{\epsilon}} = \left[\frac{\Delta \mathbf{e}_{\mathrm{os}}}{\Delta \mathrm{T}} \left(\frac{\mathrm{R}_{\mathrm{f}} + \mathrm{R}_{\mathrm{s}}}{\mathrm{R}_{\mathrm{f}} \mathrm{R}_{\mathrm{s}}}\right) + \frac{\Delta \mathrm{i}_{\mathrm{B}}}{\Delta \mathrm{T}}\right] \Delta \mathrm{T}$$

Now, to make a proper selection you must pick an amplifier with an error current, I_{ϵ} , over the operating temperature which is small compared to the signal current, i_s . Do not overlook current noise which may be more important than current drift in many applications.

Gain Bandwidth Considerations, Expanded Discussion

From the previous discussion, it is apparent that most general purpose operational amplifiers will usually give adequate performance for the DC and audio frequency range applications. However, to obtain unity gain bandwidth above 2MHz, full power response above 20kHz and slewing rate above $6V/\mu$ sec, in general, requires special design techniques. All amplifiers with wideband, fast response characteristics have been listed in the wide bandwidth group to simplify the selection for higher frequency applications.

One factor often overlooked is that stray capacitance and impedance levels of the external feedback circuit can be the major limitation in high frequency applications. For example, in Figure 1A, if R_f were one megohm and stray capacitance, C_s , were one picofarad then the closed loop bandwidth would be limited to 160kHz ($1/(2\pi R_F C_S)$) regardless of how fast the amplifier is. Moreover, output slewing rate will be limited by how fast C_S can be charged which in turn is related to signal level, e_s , and input impedance, R_i , by $de_o/dt = -e_s/R_iC_s$. For these reasons it is usually not possible to obtain both fast response and high input impedance for an inverting circuit since both R_i and R_f must be large to obtain high input impedance.

Another advantage of the noninverting circuit (Figure 1B) is that input impedance, being determined by potentiometric feedback, does not depend on the impedance levels for R_1 and R_2 . Therefore, a low impedance can be used for R_2 so that stray capacitance of C_s will not limit the circuit's bandwidth. In this case the minimum value for R_2 is constrained only by the output current rating of the amplifier. Again the trade-off between the frequency response and input impedance of the inverting and noninverting circuits must be evaluated in light of the common mode rejection error introduced by the noninverter.





Figure 2B. Voltage Amplifier With Sampling Resistor

In the past, many wideband amplifiers, especially chopper stabilized units, did not offer fast response on the positive input and therefore were restricted to use in inverting circuits. However, new FET amplifiers from Analog Devices are available to meet the needs for high speed performance for either configuration.

For greater emphasis wideband applications can be separated into two categories – steady state and transient. Since the amplifier requirements for the two are somewhat different, these categories will be discussed separately.

A. Steady State Applications

Steady state applications involve amplifying or otherwise manipulating *continuous* sinusoidal, complex or random waveforms. In these applications the significant issues in choosing an amplifier are as follows:

1. Is DC coupling required? If DC information is of no consequence, then the offset drift errors are not usually important and a capacitor can be used if necessary to block the output DC offset. Your only concern here is that DC offset at the output does not become so large, as might be the case with a high gain stage, that the output is saturated or the dynamic swing for AC signals is limited. One way to circumvent the latter problem is to use feedback to limit the gain at DC as shown in Figure 3. The gain of these circuits can be small at DC but large at high frequencies.

2. What closed loop gain and bandwidth are required? Closed loop gain, G, is dictated by the application. To a first approximation the intersection of the open and closed loop gain curves in Figure 4 gives the closed loop bandwidth, $f_{c1}(-3dB)$. For high gain, wideband requirements, it may be necessary, or more economical, to use two amplifiers in cascade each at lower gain.

3. What loop gain is required or alternatively what gain stability, output impedance and/or linearity are necessary? The available loop gain at a particular frequency or over a



Figure 3. DC Feedback Minimizes Output Offset for AC Applications

range of frequencies is very often more important than closed loop bandwidth in selecting an amplifier. Loop gain as illustrated in Figure 4, is defined as the difference, in dB, or as the ratio, arithmetically, of the open to closed loop gain ($A\beta = A/G$). You will find in most of the equations defining the closed loop characteristic of a feedback amplifier that the loop gain ($A\beta$) is the determining factor in performance. Some of the more notable examples of this point are as follows:

- a. Closed loop gain stability = $\triangle G/G$ $\triangle G/G = (\triangle A/A) [1/(1 + A\beta)]$ where $\triangle A/A$ is the open loop gain stability, usually about $1\%/^{\circ}C$.
- b. Closed loop output impedance = $Z_{ocl} = Z_o/(1 + A\beta)$, where Z_o is the open loop output impedance, usually 200 to 5000 ohms.
- c. Closed loop nonlinearity = $L_{cl} = L_{ol}/(1 + A\beta)$, where L_{ol} is the open loop linearity, usually less than 5%.

Loop gain of 100, or 40dB, is adequate for most applications and this is readily achievable at DC and low frequencies. But note that loop gain decreases with increasing frequency which makes it difficult to obtain large loop gains at high frequencies. For this reason it may be necessary to use a 10MHz unity gain amplifier in order to obtain adequate feedback over a 10kHz bandwidth.

4. What full power response and/or slew rate are required? You should examine your expected output waveform and select an amplifier whose slewing rate exceeds the maximum rate of change of output signal. For a sinusoidal waveform with a peak voltage output equal to the rated amplifier output the frequency should not exceed f_p, the full power response of the amplifier. As the output signal voltage is reduced below the rated output voltage, the usable maximum



frequency can be extended proportionately. If you do not observe these restrictions you will get distortion and unexpected DC offsets at the output of the amplifier.

There are many monolithic amplifier designs available today whose frequency response is not a simple 6dB roll-off and which may be shaped with external RC components for improved performance. Using feed-forward or phase lag compensation networks, gain-bandwidth product and/or full power response may be shaped to meet varying design requirements. Most discrete op amps offer the stable 6dB roll-off with specified unity gain-bandwidth and slew rate thereby limiting maximum speed and response to those published specifications.

B. Transient Applications

In applications such as A/D and D/A converters and pulse amplifiers, the *transient response* of the wideband amplifier is generally more important than the *gain bandwidtb* characteristic described above. Slewing rate, overload recovery and settling time are the specifications which determine the transient response.

When applying the high frequency amplifier, it is important to understand how amplifier performance is affected by component selection as well as impedance levels used around the amplifier.

Settling Time

The time and frequency response of a linear, bilateral network or amplifier are related by well known mathematics. For example, the step response for a well behaved, linear, 6dB/octave amplifier with a closed loop bandwidth of ω_{cl} is shown in Figure 5.



Figure 5. Step Response for Linear 6dB/Octave Amplifier

To a first approximation, the curve in Figure 5 can be used to relate settling time to closed loop bandwidth of Figure 4. *Settling time* is defined as the time elapsed from the application of a perfect step input to the time when the amplifier output has entered and remained within a specified error band symmetrical about the final value (Figure 6). Settling time therefore includes the time required for the amplifier to slew from the initial value, recover from slew rate limited overload, and settle to a given error in the linear range.

However, the approximation soon breaks down since settling time is determined by a combination of amplifier characteristics (both linear and non-linear) and because it is a closed loop parameter. Therefore, it cannot be readily predicted from the open loop specifications such as slew rate, small signal bandwidth, etc.

Analog Devices specifies settling time for the condition of unity gain, relatively low impedance levels, and no capacitive loading. A full-scale step input is used to determine settling time and the step is generally unipolar - i.e.: from zero to plus or minus full scale. The settling time indicated is generally the longest time resulting from a step of either polarity and is given as a percentage of the full scale step transition.

Settling time is a non-linear function. It varies with the input signal level and it is greatly affected by impedances external to the amplifier. The non-linear dependence of settling time on these two parameters can be demonstrated by an examination of experimental data from Analog Devices' wide bandwidth model 46 amplifier.



Figure 6. Typical Settling Time Characteristics

Settling Time vs. Signal Swing

The curves in Figure 7 illustrate model 46 settling time error versus input signal level. These "V" curves are useful as a design aid for bracketing settling time versus step input level. Percentage settling time error is calculated by forming the ratio of output error to input voltage step. Shown in Figure 7 are 1%, 0.1% and 0.01% error points for a $\pm 10V$ input step. The settling times for these errors are read off the vertical axis.

Because of nonlinear factors, extrapolation of settling times from one set of conditions to another becomes very difficult, if not impossible. This point becomes very apparent, in Figure 7, when reviewing settling time as a function of input signal swing. Using this measurement technique, the settling time error voltage, measured at point V, is equal to one-half of the null voltage between the input signal and the output signal.

Settling Time vs. R_f, R_i and C_L

Experience indicates that for wide bandwidths and ultra fast settling times, 500Ω to $2.5k\Omega$, gain resistors should be used to keep stray capacitance to a minimum. The effects of various resistance values on settling time are given in the following table. In developing the data, the test circuit of Figure 7 was used, but with an output load capacitor (C_L) added to the circuit.

TABLE	: 0.1% Settling	Time vs Rf, Ri, CL
$R_f = R_i$	t _s (0.1%)	Cap Load (CL)
2.5kΩ	115nsec	<10pF
$1.0 \mathrm{k}\Omega$	80nsec	< 10 pF
500Ω	64nsec	< 10 pF
$10.0 \mathrm{k}\Omega$	150nsec	270pF
$5.0 \mathrm{k}\Omega$	150nsec	190pF
$2.5 \mathrm{k}\Omega$	150nsec	100pF
$1.0 \mathrm{k}\Omega$	150nsec	65pF
500Ω	150nsec	55pF



With load capacitance set to zero, the settling time to 0.1% error improved two-fold as R_f and R_i were reduced from 2.5k Ω to 500 Ω . To show the interaction of R_f , R_i and C_L , settling time to 0.1% error was then held constant at 150ns while varying R_f , R_i and C_L . C_L was increased until settling time reached the 150ns level. This value of C_L did not create an oscillatory condition at the output, but was that value of capacitance which increased settling time to 150ns for a specified R_f and R_i . Heavier capacitive loads would have degraded settling time further because of rate limiting effects.

From these data, the effect of R_f and R_i on performance is significant enough to recommend selecting the proper range of R_f and R_i with the amplifier operating in its final configuration. The small feedback capacitor placed in parallel with R_f (Figure 7) partially cancels the pole formed in the loop gain response by the input resistor, R_i , and the amplifier input capacitance. It is selected to minimize settling time.



APPLYING THE INSTRUMENTATION AMPLIFIER

The preceding discussion has focused on developing selection criteria for op amps which require external feedback networks. In transducer and certain other instrumentation applications it is important that an amplifier be able to extract signals in the presence of common mode noise while retaining its gain adjustment ability. In the conventional operational amplifier, a mismatch between the input gain setting resistors can cause substantial errors in CMRR. An instrumentation amplifier, by virtue of its committed gain configuration, employing internal feedback networks, suffers minimal degradation in CMRR as the gain is varied.

From Figure 8, the instrumentation amplifier appears to be little more than an operational amplifier operated in a differential mode. In fact, the modern instrumentation amplifier is an appreciably more sophisticated device, which usually requires three basic differential amplifiers in order to provide for the *solution of "Common Mode" noise problems* as found in many industrial and laboratory environments.

The appearance of this noise in the simplest possible system is shown in Figure 9. It is clear that the single ended amplifier has no ability to differentiate between the signal voltage and the "Common Mode" voltage.

A first attempt to solve the problem might involve the use of an operational amplifier in the differential mode. In principle it works. In practice, its use is restricted to fixed, low gain situations for the following reasons. To avoid source loading errors, it is necessary to use high value resistor networks which can result in troublesome bias current noise and drift. Therefore, low gains are used to keep the gain ratio R_f/R_{in} as low as possible.

Another problem arises in maintaining high CMR with gain changes. Since CMR is directly related to gain resistor

balance, any resistor changes, as encountered when varying gain, will require a retuning. This procedure is both time consuming and impractical for most applications. These difficulties are highlighted in the example of Figure 10.

In this example a gain of 1000V/V is desired to amplify a 10mV signal. To avoid loading down the 1k Ω source impedance, a 1M Ω resistor is used for a 0.1% loading error. The desired gain is set using a 5M Ω feedback resistor and output attenuator. To preserve a CMR of 80dB for noise rejection, the gain resistor network must be balanced to an accuracy of 1 part in 10,000 which is difficult. If the gain must now be adjusted to another value, the delicate tweaking procedure must be repeated which is one of the difficulties in using this circuit. The second obstacle obviously arises from using high gains and resistor values which lead to excessive input noise and drift.

The instrumentation amplifier, with differential inputs, overcomes these two difficulties. High input impedance is achieved without an external summing resistor and high CMRR is maintained as gain adjustments from 1 to 1000V/V are made by varying only one resistor. The circuit of Figure 8 demonstrates that gain adjustment using one resistor does not require changing several sets of resistors as is required to alter the gain with differential amplifiers. Close matching of internal gain resistors and other components during manufacture assures extremely high CMRR. An output sense terminal is usually available to either convert the output for current feedback operation or to allow the use of a booster amplifier inside the feedback loop.

The equivalent model of Figure 8 reveals the main circuit elements to consider when applying this device. Z_{CM} and Z_d will yield gain errors due to loading of the source resistance and are frequency dependent. Z_d will vary with gain and is specified at its minimum value. Z_o will also yield small gain error under heavy loading.







Specifying the Instrumentation Amplifier

When applying the instrumentation amplifier, several new parameters appear which are not common to the operational amplifier. For example, using a committed gain configuration eliminates open loop gain as a parameter which leads to new gain non-linearity and stability terms. Drift terms also appear differently and are gain dependent since input and output amplifiers make up the total design. Drift is specified as "referred to input (RTI) or output (RTO)" at minimum and maximum gains. Total drift, referred to input, is then calculated as: Total RTI drift = [RTI drift + RTO drift/gain] μ V/°C.

Probably the quickest way to understand and specify the instrumentation amplifier is to apply this device in a straightforward application. This is done in Figure 8. An error budget for the design is developed below to illustrate a possible selection technique. For the example shown, a 5.9% error results using the amplifier parameters as specified in the chart. If this error is excessive, then key areas to consider for improvement are drift and CMRR. Using a $1\mu V/^{\circ}C$ (RTI) amplifier would significantly reduce drift error by 180mV (3.6%) to 40mV (0.8%). If CMV is relatively constant (and for a bridge circuit this is the case), then a simple offset adjustment can reduce the CMRR gain error to virtually zero (1% improvement). The total error will then be approximately $\pm 55mV$ (1.1%) which demonstrates the importance of selecting the proper drift and CMRR for the application, keeping in mind that CMRR errors can be compensated by using gain trim if CMV is constant. A high CMRR rating will be required for widely varying CMV.

ERROR BUDGET ANALYSIS (For Circuit of Figures)

Amplifier Specifications
e_{os} Drift = ± 1 mV/°C (RTO), $\pm 10\mu$ V/°C (RTI)
Gain Drift = $\pm 0.01\%$ (G = 1000 V/V)
$I_{B} = 20nA$ $Z_{d} = 300M\Omega$ $Z_{CM} = 1000M\Omega$
$Gain = 1000B$ $Gain = 1000V/V$ Non-Linearity = ±0.01% $R_0 = 10\Omega$

COMPUTATION							
Error Source	Value	% Full Scale 5V	Calculation				
Gain Drift	±10mV	0.2%	= $\pm 0.01\%$ C x \triangle T x E _{OUT}				
Offset Drift	±220mV	4.4%	= (RTI drift x Gain + RTO drift) x \triangle T				
Total Drift Error	+230mV	4.6%	$(+5^{\circ}C \text{ to } +45^{\circ}C) = \Delta T$				
Linearity Error	±10mV	0.2%	0.01% @ 10V (independent of output level)				
CMRR Error	±50mV	1%	$A_{CM} = (Ad/_{CMRR}) \times E_{CM}$				
Offset Error	$\approx 0 \mathrm{V}$		e _{os} (RTI) x Gain = 1mV x 1000				
			(adjust to 0V)				
Input Loading Error	$\approx 0 V$		$\approx R_s/R_d = 0.0002\%$ (negligible)				
Output Loading Error	5mV	0.1%	$R_o/R_{LOAD} \ge e_{out}$				
Total Error (200) +25°C	±65mV	1.3%	(a) constant temperature				
Total Error $(+5^{\circ}C \text{ to } +45^{\circ}C)$	±295mV	5.9%	$(\pm 230 mV + 65 mV)$				

APPLYING THE ISOLATION AMPLIFIER

Analog Devices has recently developed and introduced a series of unique DC coupled isolation amplifiers. Offering total ground isolation and low stray coupling capacitance (< 10 pF) between input and output grounds, these compact modules develop extremely high CMR (115dB @ 60Hz) and CMV ratings (to 5kV) using modulation techniques with transformer isolation. Capable of transmitting millivolt signals in the presence of up to 1000 volts common mode, with unity gain or with adjustable gain, these amplifiers are ideal for medical (ECG) applications where it is important to isolate hospital patients from potentially lethal ground fault currents, and for industrial applications, to interrupt ground loops between transducers and output conditioning circuits.

All models are designed to improve on the existing patient safety specifications of Underwriter's Laboratories and other regulatory agencies. When used for ECG and EEG patient-monitoring equipment, these amplifiers will do their job without exposing the hospital patient to the hazards of microshock and possible electrocution.

ISOLATION VS INSTRUMENTATION AMPLIFIERS

There are several aspects of the isolation amplifier design which make it a useful alternative to the instrumentation amplifier for a specific set of operating conditions. In general, isolation amplifiers should be considered for applications requiring: 1) moderate gain (1 to 10V/V); 2) high CMR and CMV under heavy source imbalance $(5k\Omega)$; 3) moderate RTO drifts (to $300\mu V/^{\circ}$ C); and 4) wherever it is necessary to eliminate bias currents for two wire systems or the more carefree three lead transducer hook-ups. Total signal ground isolation is an added feature which may be found useful for improving overall performance.

Circuit Description

These designs have committed gain circuits with internal feedback networks as do instrumentation amplifiers. Each model in this series operates from DC to 2kHz and is designed in two parts — an isolated front end amplifier section, followed by a grounded output section. The front end circuitry includes: 1) an input op amp with fixed gain (see Figure 11 for models 272, 273) or adjustable gain (see 274 block diagram in product specification section); 2) a modulator; and 3) a DC regulator circuit, all enclosed in a floating guard-shield. The output section contains a demodulator circuit with low pass filter and power oscillator circuit operating from a single +15VDC supply. Operating power is transformer-coupled into the shielded input circuits and capacitively or magnetically coupled (model 274) to the output demodulator circuit.

CMR Holds Up at Low Gain

Common mode performance of isolation amplifiers is independent of amplifier gain, and is determined primarily by the amount of stray capacitance from input circuit to guard-shield (CMR 1) and from guard-shield to output common (CMR 2) (see Figure 12). Shielding and transformer design are essential to high common-mode rejection. Conversely, CMR performance of instrumentation amplifiers is gain dependent, although significantly improved over conventional differential amplifier designs.

At gains below 10, CMR is reduced to typical values of 60dB with $1k\Omega$ source imbalance. For isolation amplifiers, typical ratings of 150dB with a $5k\Omega$ source imbalance are not uncommon – 90dB (3000:1) improvement. High CMV ratings up to 1000 volts are also readily achieved with isolation designs which do not require the well balanced and complex circuits used in instrumentation amplifiers.

Zero Bias Current, Low RTO Drift, Linearity

Isolation amplifiers operating with single ended input stages result in only differential current flow between input high and signal ground with zero net bias current flow. Instrument amplifiers, with differential inputs and signal ground returns, have bias current and differential current flow which require the use of a third wire return or external circuitry to accommodate these "housekeeping" bias currents.

Regarding amplifier drift and linearity: at low gains (below 10V/V), drift of instrument amplifiers (typically 100 to $500\mu V/^{\circ}C$ RTO) usually becomes a significant part of the overall drift specification and approaches the performance of isolation amplifiers (typically $100\mu V/^{\circ}C$ x Gain). Gain nonlinearity in certain models (272/273) is amplitude dependent, improving from 0.2% at 4V p-p inputs to 0.02% at 40mV p-p inputs. For model 274J, nonlinearity is approximately $\pm 0.5\%$ at ± 10 volts full scale output.

GUIDELINES FOR MEDICAL APPLICATIONS

Several unique problems arise when designing front-end amplifiers for biological applications. These relate to: 1) electrode voltage offsets setting a limit on amplifier gain; 2) trading off amplifier input noise to achieve defibrillator protection; and 3) dealing with multiple CMV noise sources arising along the surface of a patient's body and between patient/amplifier ground points. The following discussion describes isolation amplifier features which afford some design relief when applying these devices in medical applications.

Two CMR Ratings Available

The guard shield, enclosing the input circuitry, is brought out to an external pin for connection to a common mode source voltage. In fact, the transformer isolation technique develops two common mode barriers, one on either side of the guard shield. This makes it possible to reject two sources of common mode error voltage. These conditions appear as CMV voltages, CMV1 and CMV2 in Figure 12, with typical values of CMR also shown.

These features are useful when CMV sources and their internal impedances are obscured or buried as might occur in fetal heart monitoring and ECG monitoring applications, whenever signal and transducer sources are not discretely defined, or when the amplifier is not in close proximity to the signal source.

Effects of Electrode Offset Voltage (ECG, EEG, etc.) Biological signals are frequently superimposed on normal mode (as opposed to common mode) offset voltages which arise from galvanic bias potentials at the patient/electrode interface. These signals, which may be as high as 500mV (ECG) limit the amount of amplifier gain one may use before AC coupling the signal to the following high gain circuits. The unity gain buffers (272, 273) with $\pm 3V$ signal range are useful for processing the larger ECG signals. If amplification is desired, a gain of 20V/V may be taken with the 274J to process ECG signals before saturation occurs at offsets beyond 500mV. With lower offsets, as encountered with EEG electrodes and direct blood pressure transducer circuits, higher gains of up to 100V/V may be taken in the model 274 amplifier.

Amplifier Noise Performance vs Defibrillator Protection Relatively large noise voltage is developed in the large input resistor used to support repeated blasts of up to 5kV of defibrillator voltage. This resistor is required to limit the maximum input current to the FETS, but unfortunately introduces noise according to the expression:

$\epsilon_{\rm n} = 0.825 \sqrt{R(M\Omega) \times BW(Hz)} \mu V p - p$

The Johnson noise for a 1 megohm resistor is 8.25μ V p-p in a 100Hz bandwidth, based on the above equation. Combined with $3-5\mu$ V p-p FET input noise, the 273J with 1 megohm input resistor has approximately 10μ V p-p of input noise in a 100Hz bandwidth. Model 272J has approximately 35μ V p-p of noise.

For ECG and direct blood pressure transducer amplifiers, it would be desirable to combine in one module, 273J noise performance with 272J defibrillator protection. For even lower noise applications, such as EMG and EEG where defibrillator protection usually is not required, an even lower noise level (3 to 5μ V p-p) would be advantageous. Analog Devices has developed models 273K and 274J to accommodate both of these requirements.





Figure 12. Patient-Amplifier Interconnection Diagram

DEFINITION OF SPECIFICATIONS

Absolute Maximum Differential

Under most operating conditions, feedback maintains the error voltage between inputs to near zero volts. However, in some applications, such as voltage comparators, the voltage between inputs can become large. E_d defines the maximum voltage which can be applied between inputs without causing permanent damage to the amplifier.

Common Mode Rejection

An ideal operational amplifier responds only to the difference voltage between inputs (e+ minus e-) and produces no output for a common mode voltage, that is, when both inputs are at the same potential. However, due to slightly different gains between the plus and minus inputs, common mode input voltages are not entirely subtracted at the output. If the output error voltage is referred to the input (dividing by closed loop gain) it reflects the common mode error voltage between the inputs. Common mode rejection ratio (CMRR) is defined as the ratio of common mode voltage to common mode error voltage. CMRR is sometimes expressed in dB.

Precisely specifying CMRR is complicated by the fact that common mode voltage error, e_{CCM} , can be a highly nonlinear function of common mode voltage and it also varies with temperature. This is particularly true for FET input amplifiers. As a consequence, CMRR data published by Analog Devices are average figures assuming an end point measurement at the common mode voltage specified. The incremental CMRR about some large common mode voltage may be less than the average CMRR which is specified. Published CMRR specifications apply only to DC input signals. CMRR becomes lower with increasing frequency.

Drift vs. Supply

Offset voltage, bias current and difference current vary as supply voltage is varied. Usually errors due to this effect are negligible compared to temperature drift.

Drift vs. Time

Offset voltage, bias current and difference current change with time as components age. It is important to realize that the published time drift for amplifiers does not accumulate linearly. For example, voltage drift for a chopper stabilized amplifier (which is by far the best amplifier type for long term stability) might be quoted as 1μ V/day whereas cummulative drift over 30 days would not exceed 5μ V nor 15μ V in a year. In general the drift accumulation may be extrapolated by multiplying the specified drift/day by the square root of the number of days. Since our catalog specifies drift/month, divide by $\sqrt{30}$ or 5.5 to obtain drift/ day.

Full Power Response

The large signal and small signal response characteristics of operational amplifiers differ substantially. An amplifier will not respond to large signal changes as fast as the small signal bandwidth characteristics would predict, primarily because of slew rate limiting in the output stages. We specify full power response in two ways: Full linear response and full peak response.

Full linear response, f_p, is the maximum frequency at unity closed loop gain, for which a sinusoidal input signal will produce full output at rated load without exceeding pre-determined distortion level. Note that this specification does not relate to "response" in the sense of gain reduction with frequency but refers only to distortion in the output signal. There is no industry wide accepted value for the distortion level which determines the full linear response limitation but we use 3% as a maximum acceptable limit. One subtle point here is that in many applications the distortion which is caused by exceeding the full linear response can be comfortably ignored. But a far more serious effect, often overlooked, is that a DC offset voltage can be generated when the full linear response is exceeded. This is due to rectification of the asymmetrical feedback waveform or overloading the input stage with large distortion signals at the summing junction.

Certain amplifiers designed to optimize high frequency performance will provide full output swing substantially beyond the full linear response (3% distortion) limit described above. Since linear waveshape is not generally a consideration in the use of these devices, they are specified to the maximum frequency at which they will produce full output swing. This is termed "full peak response" and is indicated as such on the specification charts by the word "peak" in the row marked "Full Power Response."

Initial Bias Current

Bias current, ib, is defined as the current required at either input from an infinite source impedance to drive the output to zero (assuming zero common mode voltage). For differential amplifiers, bias current is present at both the negative and positive inputs. All Analog Devices specifications pertain to the worst of the two (not average or mean). For single ended amplifiers, bias current refers to the current at the negative input only.

Initial bias current, I_b, is the bias current at either input measured at +25°C, rated supply voltages and zero common mode voltage. The designation (0.+) or (0.-) indicates that no internal compensation has been used to reduce initial bias current and hence the polarity is always known. The sign indicates to which power supply voltage an external

compensating resistor should be connected to zero the initial bias current. The designation (\pm) indicates that internal compensation has been used to reduce initial bias current and that the residual bias current may be of either polarity. In general, compensating initial bias current has little effect on the bias current temperature coefficient. One should note that the bias current of FET amplifiers increases by a factor of 2 for each 10° C rise in temperature.

Initial Difference Current

Difference current, id, is defined as the difference between the bias currents at each input. The input circuitry of differential amplifiers is generally symmetrical so that bias currents at both inputs tend to be equal and tend to track with changes in temperature and supply voltage. Therefore, difference current is about .1 times the bias current at either input, assuming that initial bias current has not been compensated.

Input Impedance

Differential input impedance, R_d, is defined as the impedance between the two input terminals, measured at +25°C, assuming that the error voltage e_{ϵ} is nulled or very near zero volts. To a first approximation, dynamic impedance can be represented by a capacitor, C_d, in parallel with R_d.

Common mode impedance, R_{cm} , is defined as the impedance between each input and ground (or power supply common) and is specified at +25 °C. For most circuits common mode impedance on the negative input R_{cm} -, has little significance except for the capacitance which it adds to the summing junctions. However, common mode impedance on the plus input, R_{cm} +, sets the upper limit on closed loop input impedance for the non-inverting configuration. Dynamic impedance can be represented by a capacitor, C_{cm} , in parallel with R_{cm} which usually runs from 5 to 25pF on the plus input.

Common mode impedance is a non-linear function of both temperature and common mode voltage. For FET amplifiers, common mode impedance is reduced by a factor of two for each 10°C temperature rise.

As a function of a common mode voltage, R_{cm} is defined as average impedance for a common mode voltage change from zero to $\pm E_{cm}$, that is, maximum common mode voltage. Incremental R_{cm} about some large common mode voltage may be considerably less than the specified average R_{cm} , especially for FET input amplifiers.

Initial Offset Voltage

Offset voltage, eos, is defined as the voltage required at the input from a zero source impedance to drive the output to

zero. Initial offset voltage, E_{OS} , defines the offset voltage at +25°C and rated supply voltages. In most amplifiers, provisions are made to adjust initial offset to zero with an external trim potentiometer.

Input Noise

Input voltage and current noise characteristics can be specified and analyzed very much like offset voltage and bias current characteristics. In fact, drift can be considered noise which occurs at very low frequencies. The primary difference in measuring and specifying noise as opposed to DC drift is that bandwidth must be considered. At low frequencies, 100Hz or less, 1/f noise prevails which means that the noise per root cycle increases inversely with the square root of frequency. At the mid-band frequencies noise per root cycle is constant or "white."

For this reason two noise specifications are given. Low frequency noise in a bandpass of 0.01 to 1Hz is specified as peak-to-peak with a 3.3σ uncertainty, signifying that 99.9% of the observed peak-to-peak excursions will fall within the specified limits. Wideband noise in a bandpass of 5Hz to 50kHz is specified as rms.

Maximum Common Mode Voltage

For differential input amplifiers, the voltage at both inputs can be raised above ground potential. Common mode voltage, $E_{\rm cm}$, is defined as the voltage (above ground) when both inputs are at the same voltage. $E_{\rm cm}$ is defined as the maximum peak common mode voltage which will produce less than a 1% error at the output. $E_{\rm cm}$ establishes the maximum input voltage for the voltage follower connection.

Open Loop Gain

Open loop gain, A, is defined as the ratio of a change of output voltage to the error voltage applied between the amplifier inputs to produce the change. Gain is usually specified only at $DC(A_0)$, but in many applications the frequency dependence of gain is also important. For this reason the typical open loop gain response is published for each amplifier.

Overload Recovery

Overload recovery, τ , defines the time required for the output voltage to recover to the rated output voltage E₀ from a saturated condition. In some amplifiers the overload recovery will increase for large impedances (greater than 50k Ω) in the input circuit. Published specifications apply for low impedances and assume that overload recovery is not degraded by stray capacitance in the feedback network. Overload recovery is defined for 50% overdrive.

Rated Output

Rated output voltage is the minimum peak output voltage which can be obtained at rated output current before
clipping or excessive non-linearity occurs. Rated output current is the minimum guaranteed value of current supplied at the rated output voltage. Load impedance less than E_O/I_O can be used but E_O will decrease, distortion may increase and open loop gain will be reduced. (All models are short circuit protected.)

Settling Time

(See discussion on previous section on Selecting an Amplifier.)

Slewing Rate

Slewing rate, S, usually in volts/ μ sec, defines the maximum rate of change of output voltage for a large input step change. S = $2\pi f_p E_0$

Temperature Drift

Offset voltage, bias current and difference current all change or "drift" from their initial values with temperature. This is by far the most important source of error in most applications. The temperature coefficients of these parameters, $\Delta e_{OS}/\Delta T$, $\Delta i_{D}/\Delta T$, and $\Delta i_{d}/\Delta T$ are all defined as the average slope over a specified temperature range. In general, however, drift is a non-linear function of temperature and the slopes are greater at the extremes of temperature than around normal (+25°C) ambient which generally means that for small temperature excursions, the specification is conservative.

For example, a rather popular method of specifying this extremely important parameter consists of: a) arithmetically subtracting the measured offset values at the upper and lower temperature extremes and b) dividing this difference by the temperature excursion. This can yield an extremely misleading result, particularly where offset drifts in the same direction at the two extremes. It is obviously possible to have no difference in the two end-point measurements, yet severe slopes may exist between the two as illustrated in Figure 13. In this case the apparent (specified) drift would be zero $\mu V/^{\circ}C$.

Analog Devices employs two methods of drift specification – a "true butterfly" curve characteristic for the high performance/low drift models, and a "modified butterfly" for the lower cost amplifiers. Both overcome the deficiencies described above. A comparison of these methods is shown with definitive equations in Figure 14. Essentially, the butterfly characteristic insures that if the amplifier is adjusted to zero at room temperature (T_r), the offset at any temperature would, in no case, exceed the value predicted by multiplying the specified drift rate (in $\mu V/^{\circ}C$) by the temperature excursion.

Unity Gain Small Signal Response

Unity gain small signal response, f_t , is the frequency at which the open loop gain becomes unity or zero dB. "Small signal" indicates that in general it is not possible to obtain large output voltage swing at high frequencies because of distortion due to slew rate limiting or signal rectification. For amplifiers with symmetrical response on each input, f_t may be obtained by either the inverting or non-inverting configurations. Some wideband amplifiers with feed forward design have fast response only on the negative input which restricts high speed use to the inverting circuit.



CAPSULE SELECTION TABLE AMPLIFIER PRODUCTS

		Open Loop Gain	Rated Output		Frequency Response		
Description	Model	V/V	v	mA	Unity Gain MHz	Full Power kHz	Slew Rat
General Purpose – Bipolar Moderate Performance On Ampr							
Good Performance Economy	118 A/K	250k	+10	+5	1.5	100	6.0
Low Cost, 20mA Output	119 A/K	500k	±10	±20	1.5	100	6.0
Economy, Speed, IC	AD201A	50k	±10	±5	1.0	10	0.5
Lowest Cost, General Purpose, IC	AD741 J/K/L*	50k	±10	±10/5/5	1.0	10	0.5
Super Beta-Low 2nA Ibias IC	AD208/A	50k/80k	±13	±1.3	1.0	10	0.3
High Accuracy IC	AD301 AL	80k	±10	±5	1-10	0-150	0.25-9
General Purpose FET -							
Low Bias Current, High Zin Op Amps							
Lowest Cost Discrete	40 J/K	50k	±10	±5	4.0	100	6.0
Guaranteed CMR – Low Bias	43 J/K	50k	±10	±5	4.0	100/200	6.0/12.0
Lowest Bias – High CMR	41 J/K/L	100k	±10	15	1.0	50	3.0
Rest Chaine Freeman IC	140 J/K	100k	±10 ±10	±20	5.0	150	10
Hybrid - Lowest Offcet & Bigs 1C	AD505 J/K	208/308	±10 ±10	+5	1.0	70	5.0
High GBW Slew Rate IC	AD513 I/K*	20k/50k	+10	+5	1.0	to 800	to 50
Low Voc Economy IC	AD506 I/K/L*	20k/50k/75k	+10	+5	1.0	100	6.0
Low Vos Externally Compensated IC	AD516 I/K	20k/50k	±10	±5	1.0	100	6.0
Economy IC	AD540J	20k	±10	±5	1.0	100	6.0
Wide Bandwidth -							
Fast Settling Op Amps							
1000V/µs Slew, 100ns Settling, 100mA	46 J/K	25k	±10	±100	40	10MHz	1000
125V/µs, 250ns Settling to 0.1%	48 J/K	100k	±10	±20	15	1.5MHz(inv.)	125 (inv.
100mA Output - 80MHz fp - Diff Input	50 J/K	25k	±10	±100	40	80MHz	500
Lowest Cost - 1µs Settling to 0.01%	45 J/K	50k	±10	±20	10	1MHz	75
0.01% Buffer, 1µs to 0.01%	44 J/K	100k	±10	±20	10	1MHz	75
100MHz GBW, Lowest Drift	120 A/B	500k	±10	±25	10-100	4MHz	250
Wideband, 130V/µs, IC	AD505 J/K*	100k/250k	±10	±5	10	2MHz	120
Slew Rate, High Gain, IC	AD507 J/K*	80k	±10	±10	35	320	20
High Speed, Diff Input IC	AD509 J/K*	15k	±12	±10	1.6/2.0	1600/2000	120
High Speed, Low Cost IC	AD518 J/K*	200k	±13	±10	±12	10,000	70
Low Voltage Drift –							
Chopper Stablized Op Amps	224 1/12/1	1014	110	1.5		500	
$0.1\mu V/CDHIT = Lowest Noise$	234 J/K/L	10M	±10	15	2.5	500	30
Low Cost Non-Inverting High 7:	255 J/K/L 260 1/K	5.0	±10	±5 +5	0.5	4.0	0.25
General Purpose $= 25 \text{ mA} \text{ Output}$	200 J/K 231 I/K	10M	+10	+25	0.5	2-30112	0.2
High Bandwidth -20 mA Output	210/211	100M	+10	+20	20	500	100
Low Voltage Drift -	210/211	100111	-10	-20	20	500	100
Differential Input, High CMR Op Amps							
Lowest Cost $-0.25\mu V/^{\circ}C$	184 J/K/L	300k	±10	±5	1.0	5.0	0.3
Battery Powered - General Purpose	153 J/K	50k	±1.0	±1.0	0.15	5.0	0.02
Lowest Bias, $4nA$, $0.5\mu V/^{\circ}C$	180 J/K	300k	±10	±2.5	1.0	10	0.6
Super Beta, $1\mu V/^{\circ}C$, 20nA, IC	AD508 J/K/L*	250k/1M/1M	±10	±5	0.3	1.5	0.12
Highest CMR, Low Offset and Drift, IC	AD504 J/K/L*3	250k/500k/1M	±10	±5	0.3	1.5	0.12
Electrometers -							
Ultra Low Bias Current							
Varactor, Inverting	310 J/K	100k	±10	±5	2kHz	7Hz	0.4V/ms
Varactor, Non-Inverting	311 J/K	100k	±10	±5	2kHz	7Hz	0.4V/ms
Lowest Cost – High Gain FET	42 J/K/L	300k	±10	±5	1.0	4.0	0.25
High CMR, Wideband	41 J/K/L	100k	±10	±5	1.0	50	3.0
	AD523 J/K/L*	75k	±10	±5	0.5	70	5.0
High Output Voltage or Current Op Amps	Diag		110	1.000			
200 A Douter - Lowest Cost	B100	0.85	±10	±100	-	1MHz	-
200, 2000 A Output – High CMR	103 A/K	500k	±20	±20	1.5	50	6.0
140V Output	105 A/K	250k	±20	15	1.5	50	6.0
100mA Output = 80MHz fn = Diff Input	50 L/K	254	±140	+100	2.0	15	10
Guaranteed 10mA vs. Temp. IC	AD512 K/S	50k	±12/±10	±12/±10	1.0	10	0.5
Instrumentation Amplifiers					1.0	10	0.5
Low Drift - High CMR	605 I/K/I	1-1000	+10	+5	0.3	1.5	0.1
Low Cost, General Purpose	603 J/K/L	1-2000	±10	±5	1.0	10	2.0
Low Drift - Fixed Gains	602 110/		-10		1.0	10	2.0
	J100/K100	10/100/100	±10	±4	75kHz	-1%@1kHz	-
Low Cost, General Purpose, IC	AD520 J/K/S	1-1000	±10	±5	0.2	75	4.0
Isolation Amplifiers,							1.0
Medical, Industrial							
EEG/ECG Inputs, Adjust Gain	2741	1-100	±10	1.0	3.0kHz	200Hz	-
ECG Input, 5kV Safety	273K	1.0	±3	0.5	4kHz	200Hz	-
	2721	1.0	+2	0.5	4kHz	200Hz	-
Low Noise Buffer	2755	1.0	- 5	0.5			

¹Rated specifications for J, K, and L versions apply over the 0° C to +70°C temperature range; for A and B versions over

-25°C to +85°C; for S and T versions over -55°C to +125°C. ²IC devices priced at 1-24 units, others at 1-9.

Offset Voltage vs. Temperature	Input Bia @25°C	s Current vs. Temperature	Inpu Impeda	it	Inp V	ut Noise oltage	Prices/Small Quantity ²	
$\mu V/^{\circ} C max$	рА	pA/°C	Differential Ω	Common Mode Ω	0.01-1Hz μV,p-p	5-50kHz μV,rms	Dollars \$	
$\pm 20/\pm 5$	0,+35nA	$\pm 0.6/\pm 0.5 \text{ nA/°C}$	10°	109	1.0	3.0	11/21	
120/15	0,+35nA +75nA	±0.6/±0.5nA/ C	10°	10	1.0	5.0 5.0 (10Hz to 10kHz)	24/34	
+15/±5	±75nA		4×10^{6}	_	2.0	4.0 (10Hz to 10kHz)	1 85/3 40/9	
$\pm 15/\pm 5$	±2.0nA	_	10×10^{6}	-	-	-	10.50/21	
±5	30nA	0.1nA/°C	4 x 10 ⁶	-	2.0	4.0 (10Hz to 10kHz)	6	
$\pm 50/\pm 20$	0,-50/-20	2x/10°C	1011	1011	6.0	3.0	12/19	
±30/±5 +25/+10/+25	0,-10/0,-20	2x/10 C	1013	1013	6.0/2.0 max	3.0/2.0	20/26	
+7/+2	0,-0.3/-0.13	$2x/10^{\circ}C$	10	1011	6.0	16	55/68	
±75/±25	0,-30/-20	$2x/10^{\circ}C$	10 ¹¹	1012	15	5	14 80/21	
±75/±25	025/-10	$2x/10^{\circ}C$	1011	1012	30	15	20/24	
±75/±25	0,-30/-20	$2x/10^{\circ}C$	1011	1012	30	15	11/13.50	
$\pm 75/\pm 25/\pm 10$	15/10/5	$2x/10^{\circ}C$	10^{11}	1012	30	15	13/15.50/24	
±75/±25	30/20	$2x/10^{\circ}C$	10 ¹¹	10 ¹²	30	15	13/15.50	
±75	50	2x/10°C	10 ¹¹	10 ¹²	15	5	6.45	
175/125	0.100	2 (10°C	toll	Toll	10	5.0	75/02	
±75/±25	0,-100	$2x/10^{\circ}C$	1011	10	2.0	3.0	13/92	
+50/+15	0,-30/-23 0-2nA	$2x/10^{\circ}C$	1011	1011	5	3.0 (10Hz to 10kHz)	75/92	
+50/+15	0.50/-25	$2x/10^{\circ}C$	1011	1011	5.0	3.0	37/47	
+50/+15	0,-50/-25	$2x/10^{\circ}C$	1011	1011	2.0	3.0	42/52	
$\pm 15/\pm 8$	0, 507 25 0, +55nA	$0.9/0.7 \text{ nA/}^{\circ}\text{C}$	2×10^5	-	0.5	3.0	65/75	
$\pm 15/\pm 8$ typ	±75/±25nA	-	2×10^{6}		8(0.01 to 10Hz)	20	15/18	
±15/±15 max	±25nA	-	$40 \ge 10^{6}$		-	7.0 (1 to 100kHz)	9/15	
20	125/100nA		300×10^{6}	-		-	11.50/18.75	
4.0/2.0mV	120nA		3×10^{6}				3/7.20/12.00	
	101010-01						51// 5/00	
$\pm 1.0/\pm 0.3/\pm 0.1$	±100	±4/±2/±2	3×10^{5}	NA	1.0	2.0	54/65/89	
$\pm 1.0/\pm 0.3/\pm 0.1$	±50 +300	±2/±1/±0.5	6 X 10 8 x 10 ⁴ //0.01//E	10 ⁹ //0.020E	1.0	5.0	49/64	
$\pm 0.37\pm 0.1$ $\pm 0.25/\pm 0.1$	+100/+50	$\pm 1/\pm 0.5$	$3 \times 10^{-70.01 \mu r}$	NA	1.5	5.0	80/115	
±0.5/±1.0	±100/±150	±1/±3	5 x 10 ⁵	NA	5/10	10	157/113	
			4	0				
$\pm 1.5/\pm 0.5/\pm 0.25$	0,+25nA	±0.25nA/°C	4×10^{6}	2×10^9	1.0	4.0	39/55/65	
$\pm 5.0/\pm 2.0$	±3nA	$\pm 0.1 \text{ nA/°C}$	100	$2 \times 10^{\circ}$	1.0	4.0	40/50	
$\pm 1.5/\pm 0.5$	±4nA	±0.1/±0.05nA/ C	$2 \times 10^{\circ}$	100 - 106	1.0	4.0	21 20/29 80/38	
±5.0/±3.0/±1.0	±200/±100/±80	200	4×10 10^{6}	100 x 10	1.0	2.0	11.20/19.80/28	
±30/±10	±10fA	±1fA/°C	3 x 10 ¹¹	-	10	10 (1 to 100Hz)	59/95	
$\pm 30/\pm 10$	±10fA	±1fA/°C	3×10^{11}	- 12	10	10 (1 to 100Hz)	59/95	
±50/±15/±25	350/100/75fA	$4(0 \text{ to } +70^{\circ}\text{C})$	1013	1013	6.0	8.0	25/32/36	
$\pm 25/\pm 10/\pm 25$ $\pm 90/\pm 30/\pm 60$	0,-0.5/-0.25/-0.15 -1.0/-0.5/-0.25	4(0 to +70 C) $2x/10^{\circ}\text{C}$	10 ¹³ 10 ¹²	10 ¹³ 10 ¹³	8.0	10	45/55/64 21/25/28	
±1.0mV/°C	+50004		9 × 10 ³	NIA		_	30	
+20/+5	$\pm 300 \mu A$ 0 $\pm 35 \mu A$	$+0.6/+0.5 \text{ pA/}^{\circ}C$	106	10 ⁹	1.0	4.0	36/46	
+20/+5	0,+35nA	$\pm 0.6/\pm 0.5 \text{ nA/}^{\circ}\text{C}$	106	109	1.0	4.0	24/34	
±50/±15	-50/-20	2x/10°C	1011	1011	4.0	2.5 (10Hz to 10kHz)	69/79	
±50/±15	0,-2nA	$2x/10^{\circ}C$	1011	1011	5	3.0 (10Hz to 10kHz)	75/92	
±20/±25	±200nA	-	2 x 10 ⁶	-	4.0	5.0 (10Hz to 10kHz)	6/9	
3/±1/±0.5(G=1000)	0,+100nA	-1.0nA/°C	109	109	1.5(G=1000)	5 (G=1)	59/65/80	
50/±15/±5(G=1000)	0,-50/-20/-20	2x/10°C	1012	1012	2(G=1000)	80 (G=1)	39/45/50	
±10/±1000/±200 ±10/±5/±5(G=1000)	±50nA ±40/±20/±20nA	±1.0nA/°C 0.5/0.2/0.5nA/°C	10^9 2 x 10 ⁹	_		_	59/55/75 18/24/33	
100 RTI, G=100 tvp	0,-50	$2x/10^{\circ}C$	1012	1011	3	5	115	
100 typ	0,-50	2x/10°C	1012	1011	3	5	109	
±100 typ	0,-50	2x/10°C	10 ¹²	1011	3	5	109	
±125 typ	0,-50	2x/10°C	1012	1011	6	15	109	

(Specifications typical $(= +25^{\circ}C \text{ and } \pm 15 \text{ VDC} \text{ power supply unless otherwise noted.})$

³ Also available in "M" version - 0.5mV/°C max Offset Voltage Drift; 0.6mV p-p max Input Voltage Noise (0.1 to 10Hz); \$30.00 (1-24) *Also available in "S" version.

GENERAL PURPOSE-MODERATE PERFORMANCE MODELS II8, II9, 20IA, 74I, 208, 30IAL

GENERAL DESCRIPTION

Amplifiers in this group include Analog's lowest cost devices. They are best suited for general purpose designs with moderate drift requirements in the range from 5 to $40\mu V/^{\circ}C$, unity gain bandwidths to 1MHz, and full power response to 100k Hz. Using silicon bipolar transistors as the differential input stage, bias currents range from 2 to 75 nA placing upper limits of 10k to 100k ohms on circuit impedances for best performance. Typical applications include linear designs for summing, inverting, impedance buffering (followers) and active filtering. They are also useful for developing non-linear transfer functions.

MODEL 118 A/K: LOWEST COST

The first op amp to consider for general purpose applications is model 118, a discrete component amplifier which surpasses the performance of lower cost IC's. It has high open loop gain and good slew rate with drifts of $20\mu V/^{\circ}C$ (118A) and $5\mu V/^{\circ}C$ (118K). Careful component selection and advanced design techniques yield low bias current and low thermal overshoots for improved performance over earlier discrete op amp designs.

MODEL 119 A/K: 20mA OUTPUT

Model 119 A(K) is identical to 118 A(K) except for its higher 20mA output current at $\pm 10V$. For ± 20 volt output voltage requirements, select model 163 to replace model 118, and model 165 for model 119 replacement. (See page 54, "High Output-Voltage, Current.")

AD201/AD201A: ADJUSTABLE BANDWIDTH

The low cost AD201 series combines the dynamic response flexibility, afforded by external frequency compensation, with good DC performance. Because frequency compensation is performed externally, the AD201 provides a greater degree of design control, and permits the dynamic operating characteristics to be fitted to the specific system application. Other models to consider in this series are AD101A (military grade) and AD301A (industrial grade). The device offers full short circuit protection, external offset voltage nulling, and the absence of latch-up. (See also Linear IC Section.)

AD301AL: LOW COST, HIGH ACCURACY, SPEED

The low cost AD301AL combines the dynamic response flexibility afforded by external frequency compensation with excellent DC performance. The amplifier increases overall accu-



	Discrete
	Good Performance, Economy 118
Model	A K
Open Loop Gain	
DC Rated Load, V/V min	250,000
Rated Output, min	±10V@5mA
Frequency Response Unity Gain, Small Signal Full Power Response, min Slewing Rate, min Overload Recovery	1.5MHz 100kHz $6V/\mu s^1$ 0.5ms
Input Offset Voltage Initial, 25° C, (adj. to zero) max Avg. vs. Temp, max vs. Supply Voltage vs. Time	$ \begin{array}{c} \pm 5 \text{mV} \\ \pm 20 \qquad \pm 5 \mu \text{V}/^{\circ}\text{C} \\ \pm 10 \mu \text{V}/\% \\ \pm 200 \mu \text{V/mo.} \end{array} $
Input Bias Current Initial, 25°C, max Avg. vs. Temp, max	±35nA ±0.6
Input Difference Current Initial, 25°C, max Avg. vs. Temp, max	±3 nA ±0.1 ⊯0.05 nA/°C
Input Impedance Differential Common Mode	$10^6 \Omega$ $10^9 \Omega$
Input Noise Voltage, 0.01 to 1Hz, p-p 10Hz to 10kHz, rms Current, 0.01 to 1Hz, p-p	1μV 2μV 20pA
Input Voltage Range Common Mode Voltage, min Common Mode Rejection Max Safe Differential Voltage	±10V 86dB ±15V
Power Supply Range (VDC) Rated Specification (VDC)	±(12 to 18)V ±15V@4mA
Temperature Range Operating, Rated Specification	$-25 \text{ to } +85^{\circ}\text{C} \text{ 0 to } +70^{\circ}\text{C}$
Package Outline Case Dimensions	M-1 1" x 1" x 0.5"
Price 1-9 10-24	\$11.00 \$21.00 \$10.50 \$19.00

(1)20kHz and $1.2V/\mu s$ for non-inverting operation. (2)Compensated gain of 20dB. racy over the standard AD201A by 30%, and by a factor of 4 over the AD301A by reducing errors due to V_{OS} , $\triangle V_{OS}$ / $\triangle T$, I_b , CMRR, etc. (See also Linear IC Section.)

AD741 J/K/L/S: LOWEST COST, HIGH ACCURACY

These low cost devices are general purpose op amps with internal frequency compensation and significantly tighter specifications which allow substantial upgrading in performance of designs desiring 741 simplicity and operating familiarity. Results of error budget analyses of typical applications show factors of improvement in accuracy ranging from 2.5 to 8 over the industry-standard AD741 and AD741C. (See also Linear IC Section.)

AD208/208A: LOW BIAS CURRENT

Using a superbeta input device, AD208A offers low bias current, to 2nA, for use with higher circuit impedances or for lower current drift. The "A" selection has lower offset voltage and drift with specified minimum gain and CMRR ratings. Included in this series are models AD108/AD108A (military grade) and AD301/AD301A (industrial grade) with varying specifications for temperature operating range and input characteristics. (See also Linear IC Section.)

	Microcircuit										
Low Cost, 20mA Output 119	Economy, Speed AD201A	Economy, Speed Low Cost High Accuracy AD201A AD741				Super Low 2n AD2	Beta A Bias 208	High Accuracy, Economy, Speed AD301AL			
A K		J	К	L	S	AD208	AD208A				
500,000	50,000		50.0	000		50,000	80,000	80,000			
±10V@5mA	±10V@5mA	±10V@10mA	±10V@5mA	±10V@5mA	±10V@10mA	±13V@	1.3mA	±10V@5mA			
1.5MHz 100kHz 6V/µs ¹ 0.5ms	1MHz 10k Hz typ 0.5V/µs typ 		1MH 10kH 0.5V/µ –	łz z typ s typ		1M 10kH 0.3V/	1-10MHz 6-150kHz 0.25-9V/µsec —				
$ \begin{array}{c} \pm 5 \text{mV} \\ \pm 20 & \pm 5 \mu \text{V}/^{\circ}\text{C} \\ \pm 10 \mu \text{V}/\% \\ \pm 200 \mu \text{V}/\text{mo}. \end{array} $	±2mV ±15μV/°C 15μV/% max	±3mV ±20μV/°C 100μV/V max	±2mV ±15μV/°C	±0.5mV ±5μV/°C 15μV/V max	±2mV ³ ±15 15μV/	$ \begin{array}{c} \pm 0.5 \text{mV} \\ \pm 5 \mu \text{V}/^{\circ}\text{C} \\ \% \text{ max} \end{array} $	±0.5mV ±5μV/°C 90dB min -				
$\begin{array}{c} \pm 35 \text{ nA} \\ \pm 0.6 & \pm 0.5 \text{ nA}/^{\circ} \text{C} \end{array}$	±75nA	±200nA	±75nA	±50nA	±75nA	±2	nA	±30nA			
±3nA ±0.1	±10nA ±0.2nA/°C	±50nA ±0.1nA/°C ±	±10nA 0.2nA/°C max	± 5nA ±0.1nA/°C max	±10nA ±0.25nA/°C max	±0.2 ±2.5p	2nA A/°C	±5nA ±0.1nA/°C			
$10^6 \Omega$ $10^9 \Omega$	4 x 10 ⁶ Ω		2 x 1	0 ⁶ Ω		70 x	$10^6 \Omega$	4 x 10 ⁶ Ω			
1μV 2μV 20pA	2μV 4μV		2µ 3µ	V V				2μV 4μV –			
±10V 86dB ±15V	±12V 96dB ±30V		±12 100 ±30	V dB V		±1 100 No	4V 0dB te ⁴	±12V 100dB ±30V			
±(12 to 18)V ±15V@2mA	±(3 to 22)V ±15V@3mA	±(5 to 18)V	±15V@	±(5 to 22)V 2.8mA		±(2 to ±15V@	20)V 0.6mA	±(3 to 18)V ±15V@3mA			
$-25 \text{ to } +85^{\circ}\text{C} \text{ 0 to } +70^{\circ}\text{C}$	-25 to +85°C		0 to +	70°C		-25 to	+85°C	0 to +70°C			
F-1 1.5" x 1.5" x 0.4"	TO-99	TO-	99, Mini-DIP —		TO-99	TO-	-99	TO-99, Mini-DIP –			
\$24.00 \$20.00 \$34.00 \$29.00	\$4.10 \$4.10	\$1.85 \$1.85	\$3.40 \$3.40	\$5.00 \$9.00	\$4.95 \$4.95	\$10.50 \$10.50	\$21.00 \$21.00	\$6.00 \$6.00			

(3)No provision for external V_{os} null.

(4)Shunt-diode input protection. Current must be limited to ±10mA.

GENERAL PURPOSE FET-LOW BIAS, HIGH Z_{IN} MODELS 40, 43, 41, 146, AD503, AD506, AD540, AD511, AD513

GENERAL DESCRIPTION

General purpose FET amplifiers should be considered for moderate performance designs requiring high input impedance, low bias currents and bandwidths to 1MHz. These models should meet most design requirements, especially those which cannot be satisfied by bipolar input designs because of excessive bias currents or too low input impedance. The lower bias currents (1 to 100pA) and higher input impedances (10¹¹ ohms) of FETS make them a natural choice when amplifier gain networks exceed 100k ohms and it is necessary to minimize input loading and current offset errors for improved accuracy. Significant applications include integrators, sample and hold amplifiers, current to voltage converters and low bias current log circuits.

MODEL 40 J/K: ECONOMY, LOW BIAS

The popular model 40J is a best choice for OEM designs and for the general class of applications requiring low bias current (50pA), moderate offset drift ($50\mu V/^{\circ}C$), and high input impedance ($10^{11}\Omega$). Designed with minimum performance tradeoffs, it has high gain, for improved closed loop accuracy, and 4MHz bandwidth with stable 6dB roll-off. Select model 40K for a lower $20\mu V/^{\circ}C$ offset drift and a bias current of 20pA.

MODEL 43J: GUARANTEED 80dB CMR

Closely resembling model 40J in performance, model 43J has improved bias currents of 10pA and offset drift of $30\mu V/^{\circ}C$. It is especially noted for its guaranteed CMR of 80dB at ±11 volts for accurate noninverting buffer or differential applications. Its 10pA bias and high input impedance are desirable for accurately amplifying small current or voltage signals approaching those levels requiring electrometer designs.

MODEL 43K: $5\mu V/^{\circ}C$, LOWEST NOISE

The best FET's available have been designed into model 43K to produce the lowest noise FET amplifier in the line. This new, low noise, low drift design features a guaranteed noise specification of 2μ V rms (max) in a 10kHz bandwidth, and only 5μ V/°C (max) of voltage drift from 0 to +70°C. Bias current of 10pA and input impedance of $10^{11}\Omega$ are also compatible with the excellent drift and noise performance of this amplifier.

MODEL 41 J/K/L: HIGH CMR, 0.5pA DIFFERENTIAL FET

Model 41 has guaranteed bias currents from 0.5 pA to 0.15 pA max, typical CMR of 94dB, and a 1MHz bandwidth. It was specifically designed for low level current measurements demanding minimal errors when used with high impedance sources such as pH transducers, photomultipliers and long term integrators. Its speed, high CMR and low input capacitance also make it useful for medium speed automated test systems.



MODEL 42 J/K/L: LOWEST BIAS CURRENT, 110dB GAIN

Undoubtedly one of the best values for OEM designs, the model 42 is an ultra low bias current FET useful for measuring low level currents or voltages from high source impedance such as photo/ion detectors and pH transducers. Typical specifications include 110dB open loop gain, 1 MHz bandwidth and CMR of 66dB at ±1V for differential designs. Models are available with bias current as low as 75fA and drift to $15\mu V/^{\circ}$ C. Refer to Electrometer Amplifier product group for further information.

MODEL 146 J/K: LOWEST VOLTAGE DRIFT

Model 146 features low voltage and current drift for use with high impedance sources. High CMR performance make this differential FET amplifier especially useful for bridge circuits and buffer designs where good CMR performance is required for accuracy. For source impedances below 100k Ω , the 184 series low drift amplifiers are a good alternative to model 146. The models 146J and 146K have $7\mu V/^{\circ}C$ and $2\mu V/^{\circ}C$ voltage drift respectively, with 80dB CMR and 20mA output. Other specifications include $10^{11}\Omega$ input impedance, 5MHz bandwidth, $10V/\mu$ sec slew rates, bias currents to 20pA and 100dB gain for use with high speed integrators, current to voltage converters, accurate buffer designs and, in general, where speed and FET characteristics must be combined with good drift performance.

AD503 J/K/S GENERAL PURPOSE, LOW PRICED IC

These internally compensated FET op amps, with stable 6dB roll-off provide a good combination of economy and performance for most FET applications. In addition to their high CMRR, slew rate and low bias current, the nulling technique for trimming offset voltage results in only minor changes in drift performance – unlike other comparable IC FET designs.

AD506 J/K/L/S HIGH ACCURACY IC

These devices are high accuracy FET-input op amps which combine the low current characteristics typical of FET amplifiers with the low initial offset voltage and offset voltage stability of bipolar amplifiers. Active laser trimming and close matching of circuit elements provide maximum warmed-up offset voltage below 1.0mV, maximum offset voltage drift of $10\mu V/^{\circ}C$, and warmed-up bias current below 5pA max. Other excellent characteristics include open loop gain above 75,000 and minimum CMRR of 80dB.

AD540J LOWEST COST IC

The AD540J is the lowest priced IC FET-input op amp which provides the user with low bias currents, high overall performance, and accurately specified, predictable operation. Despite its low cost, the AD540J provides such benefits as bias current and offset voltage specified under fully warmed-up conditions, gain guaranteed with the offset voltage both nulled and unnulled, and minimal variation in offset voltage drift with nulling.

AD511 A/B: HYBRID, LOWEST BIAS AND OFFSET

These devices are low cost replacements for AD501 and ADP501 type hybrid amplifiers and are manufactured by combining FET input chips with a monolithic bipolar op amp on a laser trimmed substrate. Offsets are held below 1mV while drift and bias currents are less than $25\mu\text{V}/^{2}\text{C}$ and 5pA respectively. See linear IC section for more information.

AD513 J/K, AD516 J/K HIGH SPEED

Useful for high speed comparators, integrators, sample/hold or peak detectors, the AD513 offers external frequency compensation for adjusting gain bandwidth and slew rate performance. Using either simple lag or feedforward compensation, GBW products and slew rates of 30MHz and 50V/ μ sec may be achieved with ease. AD513J has offsets of 20mV, bias currents of 20pA and drifts to 25μ V/°C. For comparable performance with lower offsets to 3mV, select the AD516 series with laser trimmed offsets. See Linear IC section also.

		Disc	rete				
	Lowest Cost Discrete-\$12 40	Econo Guarantee Low B 43	my d CMR ias	High Perfor Lowest B High CM 41	mance lias IR	Lowes 20mA 1	t Drift Output 46
Model	ј к	L	К	ј <mark>к</mark>	L	J	к
Open Loop Gain DC Rated Load, V/V min	50,000	50,0	00	100,0	DO	100	000
Rated Output, min	±10V@5mA	±10V@	5mA	±10V(@5	5mA	±10V@	20mA
Frequency Response Unity Gain, Small Signal Full Power Response, min Slewing Rate, min Overload Recovery	4MHz 100kHz 6V/μs 4μs	$ \begin{array}{c c} 4M1 \\ 100 \text{kHz} \\ 6 \text{V}/\mu \text{s} \\ 4 \mu \text{s} \end{array} $	4MHz 100kHz 200kHz 6V/μs 12V/μs 4μs 0.5μs		1MHz 50kHz 3V/µs 2µs		1Hz kHz //µs fms
Input Offset Voltage Initial, 25°C, (adj. to zero) max Avg. vs. Temp, max vs. Supply Voltage vs. Time	$\begin{array}{c} \pm 2mV^{1} \\ \pm 50 & \parallel \pm 20 \mu V / \\ \pm 50 \mu V / \\ \pm 250 \mu V / \\ \end{array} \\ \end{array}$	⁶ C ^{±2m} ^{±50} ^{±250}	V^{1} $ \pm 5\mu V/^{\circ}C$ $ \pm 10\mu V/\%$ $ \pm 50\mu V/mo.$	$\begin{array}{c c} \pm 2mV \\ \pm 25 & & \pm 10 \\ \pm 10 \mu V \\ \pm 250 \mu V \end{array}$	7^{2} $7/9_{0}$ $1 \pm 25 \mu V /^{\circ} C$ /mo.	±0.7 ±7 ±15µ ±100µ	$ mV^{3} $
Input Bias Current Initial, 25°C, max (Doubles every +10°C)	0, -50pA 0, -20	оА 0, -10рА 	0, -20pA	0, -0.5pA -0.25pA -0.15pA		0, -30pA -20pA	
Input Difference Current Initial, 25°C (Doubles every +10°C)	±25pA ±10	οΛ ±3ϝ	A	±0.2pA ±0.1pA ±0.1pA		±10	ррА
Input Impedance Differential Common Mode	$10^{11} \Omega//3.5 pF$ $10^{11} \Omega//3.5 pF$	$\frac{10^{11}\Omega}{10^{11}\Omega}$	/3.5pF /3.5pF	$10^{1.3} \Omega //3.5 \text{pF}$ $10^{1.3} \Omega //3.5 \text{pF}$		$10^{11} \Omega$ $10^{11} \Omega$	//3.5pF //3.5pF
Input Noise Voltage, 0.01 to 111z, p-p 511z to 50kHz, rms Current, 0.01 to 111z, p-p	6μV 3μV 0.1pA	6μV 3μV 0.1	2μV max 3μV max pA	8μV 10μV	/	6µ 16µ 0.1	V 4V pA
Input Voltage Range Common Mode Voltage, min Common Mode Rejection Max Safe Differential Voltage	+8, -10V 80dB(+8, -10V) ±15V	±10 80dB min @±10V ±15	9V 80dB@(+8V, -10V) 9V	±10V 94dB ±15V	/ 4 /	±1 80dB(+5 ±1	0V , -10V) 5V
Power Supply Range, ±V _S (VDC) Rated Specification (VDC)	±(12 to 18)V ±15V@5.5mA	±12 to ±15V@5.5mA	±15V@8mA	±(12 to ±15V@	18)V 8mA	±(12 to ±15V0	0 18)V 95mA
Temperature Range Operating, Rated Specifications	0 to $+70^{\circ}$ C	0 to +	70°C	0 to +7	°0°C	0 to -	+70°C
Package Outline Case Dimensions	M-2 1" x 1" x 0.5"	M- 1″ x 1″	-2 ' x 0.5"	F-2 1.5" x 1.5"	x 0.4"	F- 1.5" x 1.	-1 5″ x 0.4″
Price 1-9 10-24	\$12 \$11.80 \$17	19 \$20 10 \$19	\$29 \$28	\$45 \$55 \$42 \$51	\$64 \$60	\$55 \$53	\$68 \$63

With external 499 Ω trim
 With trim terminals open
 With external trim resistor supplied
 CMR @ ±5V. Option 'V' provides 80dB CMR @ ±10V

							Microcircuit					
	General Purpose Low Cost AD503			High Accuracy AD506				Lowest Cost AD540J	Low Cost Minipackage Replacement AD511		High Slew (Low AD513	GBW, Rate Offset) (AD516)
J	к	S	J	К		L	S		A	В	J	к
20,000	50,000 ±10V@5mA	50,000	20,000	50,000 ±10)V@5m/	75,000 A	50,000	20,000 ±10V@5mA	25,00 ±10V@5	0 mA	20,000 ±10V	50,000 @5mA
	1MHz 100kHz typ 6V/µs typ			1 100 6V.	lMHz kHz typ /µsec ty	p	6.3.1	1MHz 100kHz typ 6V/µsec typ	1МН 70kH 5V/µ 6µs	z z s	1M Up to 800kHz Up to 50V/µs	IIIz typ (Feedforward typ (Feedforward)
±50mV ±75 ±12	±20mV ±25 ±6	±20mV ±50μV/°C ±6μV/%	±3.5mV ±75 ±12	±1.5mV ±25 ±6		±1.0mV ±10 ±6	±1.5mV ±50μV/°C ±6μV/%	±50mV ±75μV/°C ±12μV/% -	±2mV ±75 ±15μV	±1mV 25µV/°C /%	±50mV ±75 ±50	±2ὑmV ±25μV/°C ±15μV/%
-15pA	-10pA	-10pA	-15pA	-10pA	I	-5pA	-10pA	-50pA	-25pA	-10pA	-30pA	-20pA
±10pA	±5pA	±5pA	±10pA	±5pA	1	±2.5pA	±5pA	±25pA			±20pA	±10pA
	$10^{11}\Omega$ $10^{12}\Omega$			1	$10^{11}\Omega$ $10^{12}\Omega$			$10^{10}\Omega$ $10^{10}\Omega$	10 ¹¹ 10 ¹²	2	10 ¹ 10 ¹	$^{1}\Omega$ $^{2}\Omega$
	15μV 5μV —			15µ 70nV/√H 25nV/√H	$\frac{dV}{dz} (p-p)$ $\frac{dV}{dz} (f = 1)$ $\frac{dV}{dz} (f = 1)$) DOHz) kHz)		15μV 5μV –	30µV 15µV		30µ 15µ	1V 1V
90dB	±10V 90dB ±4V(for I _b level)	90dB		± 9 ±4V (f	10V 90dB or I _b lev	vel)		±10V 80dB ±20V	±10V 86dB		±1 70dB ±V	0V 80dB /S
±(5 to 18)V	±(5 to 18)V ±15V@3mA	±(5 to 22)V	±(5 to 18)V	±(5 to 18) ±15	V@5mA	±(5 to 18)V	±(5 to 22)V	±(5 to 18)V ±15V@3mA	±(5 to 1 ±15V@4	8)V mA	±(5 to ±15V0	18)V 94mA
0 to +70°C	0 to +70°C	55°C to +125°C	0 to +70°C	0 to $+70^{\circ}$ C	1	0 to +70°C	-55°C to +125°C	0 to +70°C	-25 to +	85°C	0 to	+70°C
	TO-99 -				TO-99 -			TO-99 -	P-1 0.6" x 0.6"	x 0.25"	TO	-99
\$14.80 \$14.80	\$21.00 \$21.00	\$27.00 \$27.00	\$13.00 \$13.00	\$15.50 \$15.50		\$24.00 \$24.00	\$26.50 \$26.50	\$6.45 \$6.45	\$20 \$18	\$24 \$21	\$11.00(\$13.00) \$11.00(\$13.00)	\$13.50(\$15.50) \$13.50(\$15.50)

WIDE BANDWIDTH-FAST SETTLING MODELS 45, 46, 47, 48, 50, 44, 120, AD505, AD507, AD509, AD518

GENERAL DESCRIPTION

Amplifiers in this group feature both FET and bipolar designs with differential and single ended input stages to provide a wide choice of drift and bias current specifications. They emphasize exceptionally fast response and wide bandwidths for applications in data acquisition and pulse data transmission systems. Critical specifications are step response settling time, full power response and stable 6dB roll-off. Low output impedance and output current capability also become important for line driving applications and immunity from capacitive loads or oscillations. Typical performance numbers are unity-gain bandwidths to 40MHz, 0.1% settling times to 100ns, 1000V/ μ s slew rates, and 10MHz full power response.

These amplifiers are useful for sample and hold circuits, A/D converters, or as high speed buffers and integrators. Offering high output current capability, they should be considered for video or line driver circuits, D to A output amplifiers or as deflection control amplifiers.

MODEL 46 J/K: 1000V/µs DIFFERENTIAL, 100ns SETTLING FET

The model 46, an extremely fast amplifier, should be considered if settling time, slew rate or bandwidth are critical requirements for digital and linear signals in the 100ns and 10MHz region. It is an exceptionally stable FET amplifier offering guaranteed $1000V/\mu s$ slew rate, 100ns settling time to 0.1% and 40MHz bandwidth with -6dB per octave roll off.

MODEL 45 J/K: ECONOMY, 1µsec SETTLING FET

Designed for use with A to D, D to A and multiplexer circuits, the model 45 FET amplifier is the best choice for most inverting and noninverting applications. It offers a good balance between cost and performance with 75 V/µsec slew rate, 10MHz unity gain bandwidth and 20mA output for driving up to 700pF of capacitance. Models 45J ($50\mu V/^{\circ}C$, 25pA bias) and 45K ($15\mu V/^{\circ}C$, 10pA bias) settle to 0.01% in 1 µsec (max) inverting; CMR capability is 74dB at +5V, -10V CMV making it useful as a follower at minimum gains of 2V/V, noninverting.

MODEL 50: FASTEST SETTLING, 100mA OUTPUT, 100MHz GAIN BANDWIDTH PRODUCT

The new model 50 combines a high gain bandwidth product of 100MHz with an output current of 100mA, and settles to 0.1% in less than 100ns. Unlike most high speed amplifiers, the model 50 does not require high input drive voltage in order to achieve fast settling. See Figures 1 and 2 that compare model 50 to model 46 which has been accepted as being an industry standard for fast amplifiers.

A typical application of model 50 is that of current to voltage conversion, where the output of a D/A converter is applied directly to the amplifier's summing junction. In this configura-



tion, the high speed amplifier is usually operated in a noise gain of about 5 (Noise Gain = $1 + R_f/R_{out of D/A}$). This condition represents a significant variance from the point of unity gain where all high speed amplifiers are specified. Most high speed amplifiers will suffer severe degradation in settling

	Lowes 1 µs to	t Cost 0.01%	1000V/µs, Differential 46		
Model	J	К	J	К	
Open Loop Gain DC Rated Load, V/V min Rated Output, min	50,1 ±10V(a	000 20mA	25 ±10V(a	009)100mA	
Frequency Response Unity Gain, Small Signal Full Power Response, min Slewing Rate, min Overload Recovery Settling Time to 0.01% Settling Time to 0.1%	10N 1M 75V 0.5 1.0μs, 50	1Hz Hz /μs max Ons	40 10 1000 0. 250ns, 100ns	MHz MHz 2μs max, 0.05% max	
Input Offset Voltage Initial, 25°C, (Adj. to zero) Avg. vs. Temp, max vs. Supply Voltage vs. Time	±2n ±50 ±50µ ±250µ	V^4 $\pm 15\mu V/^{\circ}C$ V/% V/mo.	±3 ±75 ±30) ±5004	mV ±25µV/ °C ₽V/% €V/mo.	
Input Bias Current Initial, 25°C, max Avg. vs. Temp, max	050pA 2x/1	0, -25рА 0 °С	0, -1 2x/	00pA 10°C	
Input Impedance Differential Common Mode	$10^{11} \Omega$ $10^{11} \Omega$	7/3.5pF //3.5pF	10 ¹¹ Ω 10 ¹¹ Ω	2/3.5pF 2/3.5pF	
Input Noise Voltage, 0.01 to 1Hz, p-p 50Hz to 50kHz, rms Current, 0.01 to 1Hz, p-p	5 μV 3 μV 0.1 pA		10 No 0.1	μV te ⁶ pA	
Input Voltage Range Common Mode Voltage, min Common Mode Rejection @ ±10V Max. Safe Differential Voltage	74dB(±1	- +5, -10V) ⁷ 5V	±1 72dF ±1	0V min 5V	
Power Supply Range (VDC) Rated Specification (VDC)	±(12 t ±15V	υ 18)V @7mA	±(12 t ±15V@	ο 18)V 955mΛ	
Temperature Range Operating, Rated Specifications	0 to	+70 °C	0 to	+70°C	
Package Outline Case Dimensions	QC 1.125''x1.	C-1 125'' x 0.4''	N- 1.22'' x 1.	-1 88'' x 0.6''	
Price 1-9 10-24	\$37 \$36	\$48 \$46	\$75 \$62	\$92 \$75	

(1)External trim adjustment

(2)Model 48 non-inverting slew rate-90V/µs (3)Model 44 non-inverting slew rate-50V/µs (4)With fixed 499 Ω external trim (5)200k Ω at DC; 10k//3pF above 10Hz

44 AMPLIFIERS

time and slew rate when operated in gains other than unity. Model 50 with its 100MHz gain bandwidth easily achieves fast settling, since it is still far from the point of being bandwidth limited.

(i.e.) At a gain of 4, model 50 has a bandwidth of 20MHz which represents a time constant of 8ns. (T = $1/2\pi F = 0.16/20 \times 10^{+6}$). For 0.1% settling the bandwidth limitation is 6.9 time constants or only 55.2ns.

In addition to the 100MHz gain bandwidth product, the high transconductance of the input stage also provides the ability to achieve fast slew rates for small signals. See Figure 2.



Figure 1. Settling Time vs. Gain (V/V)



Figure 2. Slew Rate vs. Error Signal

MODEL 48 J/K: 300ns SETTLING, 80dB CMR Model 48 is an ultra fast differential amplifier, optimized for D/A and A/D converter applications demanding excellent slew rate, settling time and DC characteristics. When used with these high speed circuits, its smooth settling response and wideband CMR capability are particularly useful for resolving small bit increments and for rejecting logic ground noise.

Typical specifications for this FET design include 300ns settling to 0.01% (inverting or noninverting), CMR of 80dB at \pm 10V, open loop gain of 100dB and 125V/µsec slew rate

Dis	screte								
300ns Smooth 4	300ns to 0.01% Accurate Buffe Smooth Settling 1µs to 0.01% 48 44		te Buffer 0.01% 4	Wideband 250V 12	100MHz 7/μs 20	Fastest 100ns at Ga	Settling to 0.05% ain of 5 50	Fast Se Hermetical 47	ttling ly Sealed
J	К	J	К	A	В	J	К	A	В
100	0,000	100	,000	500,	000	25	,000	100,0	000
±10V@	@20mA	±10V@	920inA	±10V@	25mA	±10V @	9 100mA	±10V @	20mA
15M 1.5 MHz inv 125 V 0.5 30 25	MHz 1MHz noninv V/μs ² 5 μs 90ns 90ns	10/ 1N 75V 0.5 1.0µs 50	4Hz HHz /μs ³ 5μs , max Ons	10 to 1 4M 250V 10 1.0	00MHz ¹ Hz 7/μs μs μs	80 81 500 200ns ma 100ns	MHz MHz DV/μs 2μs x, 0.05% 5 max	10M 800 50V 0.5 1.0µs 14	HHz kHz ζ/μs ζ, max ts
±2n ±50 ±250µ	nV^4 $\pm 15 \mu V/ °C$ $\mu V/mo.$	±2n ±50 ±250j	$\int_{uV/mo.}^{uV^{4}} \frac{15 \mu V}{c}$	Adjust ±15 20μV 50μV	to 0 ±8µV/°C V/% /mo	±3n ±50 15µ' ±500µ	nV │ ±15µV/°C V/% V/mo.	±2n ±50 - ±250µ	V^4 $\pm 15 \mu V/^{\circ} C$ V/mo.
0, -50pA	0, -25pA_	0, -50pA	0, -25pA	0, +5	5nA	0, -:	2nA	0,-50pA	0, -25pA
2x/1	10 °C	2x/1		0.9 0	.7nA/°C max	2x/1	10°C	2x/	10°C
$10^{11} \Omega$ $10^{11} \Omega$	2//3.5pF 2//3.5pF	$10^{11} \Omega$ $10^{11} \Omega$	//3.5pF //3.5pF	Not	c ⁵	$10^{11}\Omega$ $10^{11}\Omega$	//3.5pF //3.5pF	$10^{11}\Omega$ $10^{11}\Omega$	//3.5pF //3.5pF
24	uV	2 µ	V	0.5µ	IV	5μV		2μV	
34	uV	3 µ	V	3µ	V	Note ⁶		3μV	
0.1	IpA	0. 1	pA	100	pA	1.0pA		0.1pA	
±1	1V	±1	1V	N/	A	±1	0V	±1	11V
80dB	3 min	80dB	min	N/	A	60dI	3 min	66dI	3, min
±1	5V	±1	5V	±15	V	±1	5V	±1	5V
±(12 t	o 18)V	±(12 to) 18)V	±(13 t	o 18)V	±(12 t	o 18)V	±(12	to 18)V
±15V	@9mA	±15V@	99mA	±15V@	20mA	±15V (9 40mA	±15V	@ 9mA
0 to	+70 °C	0 to +	-70 °C	-25 to	+85 °C	0 to	+70°C	-25°C	to +85°C
QC	2-1	QC	-1	F-	3	N	-1	1.125" x 1	C-1
1.125" x 1.	125" x 0.4"	1.125" x 1.1	25'' x 0.4''	1.5" x 1.5	'' x 0.4''	1.22" x 1	88'' x 0.6''		.125'' x 0.4''
\$41	\$52	\$42	\$52	\$65	\$75	\$75	\$92	\$69	\$79
\$39	\$48	\$39	\$48	\$62	\$71	\$62	\$75	\$62	\$72

(6)Model 46 $- 25\mu$ V rms, 5Hz to 2MHz; Model 50 $- 6\mu$ V rms, 5Hz to 2MHz. (7)CMR specified at +5V, -10V. Option "V" provides CMR of 74dB min at ±10V. (inverting). Extremely stable at 15MHz bandwidths, model 48 has good immunity to oscillations under heavy load capacitance, to 750pF. This device is available in two drift selections, $50\mu V/^{\circ}C$ (48 J) and $15\mu V/^{\circ}C$ (48K), and uses monolithic input stages to minimize thermal feedback affects for improved small signal resolution.

MODEL 44 J/K: 0.01% BUFFER, 1 µsec SETTLING FET

Model 44 is a fast differential amplifier with guaranteed CMR of 80dB at $\pm 10V$ for high speed non-inverting buffer applications requiring high open loop gain and 0.01% full scale accuracy with 1 μ sec settling times. Capable of driving 1000pF capacitive load, its smooth settling characteristics make it a good choice for 12-bit D/A, A/D circuits, multiplexers, peak detectors, and sample/hold circuits where overall speed is affected by this cascaded circuit element. Other specifications include 100dB open loop gain, 10MHz bandwidth, $50V/\mu$ sec slew rate, 20mA output. Model 44J is available with $50\mu V/^{\circ}$ C drift and model 44K with $15\mu V/^{\circ}$ C drift.

MODEL 47 A/B: FAST SETTLING, HERMETICALLY SEALED

Model 47 with all hermetically sealed devices is recommended to upgrade models 44 and 45 for wider temperature range applications as required in military grade circuits. Settling time is 1μ s to 0.01% (inverting and noninverting) and CMR is 86dB at \pm 10V. Other specifications parallel those of model 44 J/K.

MODEL 120 A/B: 100MHz BANDWIDTH, 1 µsec SETTLING

The model 120 offers design flexibility in an inverting amplifier with bipolar input stage and externally adjustable gainbandwidth product from 10MHz to 100MHz. Requiring only a single resistor for frequency response shaping, it is very useful for providing large gains at wide bandwidth, as used in video circuits, radar signal processing, fast Fourier Transformer or, in general, whenever fast low level signals must be amplified accurately. At lower gains, it achieves $25 \text{ OV}/\mu\text{sec}$ slew rates and $1\mu\text{sec}$ settling with 0.01% error for use in comparators, D/A converters or in other high speed circuits.

Optimized for use with circuit impedances below $10k\Omega$, the model 120 will deliver 25mA and is available in two versions: 120A $(15\mu V/^{\circ}C)$ and 120B $(8\mu V/^{\circ}C)$.

AD505 J/K/S: 150V/µsec, HIGH DC ACCURACY, MONOLITHIC

Model 505, with bipolar input, features high gain, low voltage drift and wide bandwidth when operated in the inverting mode. Using external frequency compensation, these devices should be considered for high speed applications requiring fast slew rates and settling times or whenever high loop gain is required at wideband frequencies. Typical applications include active filters, sample/hold circuits, D/A and A/D converters.

Specifications include high open loop gain, typical slew rate of $150V/\mu$ sec and bias current below 40nA. (The AD505 is availa-

					Microcircuit	
	1	Wideband 150V/µs Inverte AD505	er		Low Cost Wideband AD507	
Model	J	к	S	J	К	S
Open Loop Gain DC Rated Load, V/V min Pated Output, min	100,000	250,000	250,000	80,000	100,000	100,000
Frequency Response Unity Gain, Small Signal Full Power Response, min Slewing Rate, min Overload Recovery Settling Time to 0.01% Settling Time to 0.1%		10MHz 2MHz typ 120V/µs typ 2µs 800ns			35MHz 320kHz 20V/µsec	
Input Offset Voltage Initial, 25°C, (Adj. to zero) Avg. vs. Temp, max vs. Supply Voltage vs. Time	±5.0mV ±15	$\begin{vmatrix} \pm 2.5 \text{mV} \\ \pm 8 \\ \pm 45 \mu\text{V}/\% \\ - \end{vmatrix}$	$ \begin{vmatrix} \pm 2.5 \text{mV} & \text{max} \\ \pm 10 \mu \text{V}/^{\circ} \text{C typ} \end{vmatrix} $	±5mV ±15 typ ±30µV/%	±3mV ±15 max ±15µV/% max	±4mV max ±20μV/°C max ±15μV/% max
Input Bias Current Initial, 25°C, max Avg. vs. Temp, max	75nA	25nA	25nA	25nA	15nA	15nA
Input Impedance Differential Common Mode		Note ¹			300x10 ⁶	
Input Noise Voltage, 0.01 to 1Hz, p-p 50Hz to 50kHz, rms Current, 0.01 to 1Hz, p-p	8µV 20) 2001	7(0.01Hz to 10 2V(10Hz to 1M 5A(0.01Hz to 1	Hz) IHz) 0Hz)		-	
Input Voltage Range Common Mode Voltage, min Common Mode Rejection @ ±10V Max. Safe Differential Voltage		NA NA ±10V			±11V 100dB ±12V	
Power Supply Range (VDC) Rated Specification (VDC)		±(5 to 18)V ±15V@6mΛ			±(5 to 20)V ±15V@4mA	
Temperature Range Operating, Rated Specifications	$0 \text{ to } + 70^{\circ} \text{C}$	0 to $+70^{\circ}$ C	-55 to +125°C	0 to +70°C	0 to +70°C	-55°C to +125°C
Package Outline Case Dimensions		TO-100			TO-99 _	
Price -9 10-24	\$15 \$15	\$18 \$18	\$21 \$21	\$9.50 \$9.50	\$15.00 \$15.00	\$22.50 \$22.50

ble in two accuracy selections: J, K for 0 to $+70^{\circ}$ C operation; and, S for -55° C to $+125^{\circ}$ C operation.)

AD507 J/K/S: LOW COST, 35V/µsec, HIGH ACCURACY

Model AD507 is recommended for use where low cost and allaround excellent performance, especially at high frequencies, are needed. It is particularly well suited as a fast high impedance comparator, integrator, or wideband amplifier, and in sample-and-hold circuits. It is unconditionally stable for all closed loop gains above 10 without external compensation. The frequency compensation terminal is used for stability at lower closed loop gains.

The AD507 provides a gain bandwidth of 100MHz, minimum slew rate of $25V/\mu$ sec (K), maximum I_b and I_{OS} of 15nA (K) and, for wide-temperature range applications, drift below $20\mu V/^{\circ}C$ (S).

AD509 J/K/S: 2µsec MAX TO 0.01%, 20MHz BANDWIDTH

Model AD509 is a fast differential input amplifier whose combination of low cost and excellent dynamic performance makes it a preferred choice for 12 bit D/A and A/D circuits, sample/ hold circuits, multiplexers, and other applications requiring fast settling time to low error levels. The AD509 is stable for all values of closed-loop gain >3, and can be stabilized for any value of closed-loop gain with a single external capacitor.

Specifications include maximum settling time to 0.01% of

2.0 μ sec (K), typical slew rate of 120V/ μ sec, 20MHz typical bandwidth, and ±10mA minimum output current at ±10V.

AD518 J/K/S: HIGH SPEED, LOW COST

The AD518 is a precision monolithic operational amplifier designed for applications where high slew rate and wide bandwidth are required but low cost and ease of use are essential. The devices are internally compensated for unity gain applications with a 60° phase margin to insure stability, a minimum slew rate of 50V/ μ sec, and a bandwidth of 12MHz. The AD518's DC performance is consistent with its precision dynamic characteristics. The devices feature offset voltages below 2mV, maximum offset voltage drifts of 10 μ V/°C, and offset currents below 50nA max.

The high slew rate, fast settling time, ease of use and low cost make the AD518 ideal for use with D/A and A/D converters. as well as active filters, sample and hold circuits, and as a general purpose amplifier.

	Fast Settling to High Accuracy AD509		H	ligh Speed, Low Cos AD518	t
J	К	s	J	К	S
7,500	10,000	10,000	25,000	50,000	50,000
	±10V@10mA			±12V@10mA	
120kHz 80V/µs	20MHz 150kHz 100V/µs	150kHz 100V/μs		12MHz 	
200ns typ 1.0μs typ	500ns max 2.0µs max	500ns max 2.0µs max		2µs 800ns	
10mV max 20 typ 200	8mV max 30 max 100	8mV max 30 max µV/°C 100µV/V max	10mV	$ \begin{array}{r} 4mV \\ 10\mu V/^{\circ}C \\ 80dB \\ - \end{array} $	4mV
250nA	200nA _	200nA	500nA	200nA _	200nA
$40M\Omega$ min	50MΩ min _	50M Ω min		3MΩ 	
	-			-	
74dB min ²	±10V 80dB min ² ±15V	80dB min ²	70dB	±10V 80dB	80dB
	±(5 to 20)V ±15V@4mA			±(5 to 20V) ±15V	
$0 \text{ to } +70^{\circ}\text{C}$	0 to +70°C	-55°C to +125°C	0 to +70°C	0 to $+70^{\circ}$ C	-55°C to +125°C
	TO-99 _			TO-99 —	
\$11.50 \$11.50	\$18.75 \$18.75	\$26.00 \$26.00	\$3.00 \$3.00	\$7.20 \$7.20	\$12.00 \$12.00

LOW VOLTAGE DRIFT-CHOPPER STABILIZED MODELS 234, 233, 260, 261, 231, 210

GENERAL DESCRIPTION

Chopper stabilized amplifiers employ modulation techniques for processing the "low frequency" components of a signal and an AC coupled amplifier for the higher frequencies. This chopping technique makes it possible to process wideband signals and yet achieve superior low drift and long term stability. Analog Devices, a pioneer in the development of encapsulated chopper stabilized amplifiers, offers designs with drifts between 0.1 to $1\mu V/^{\circ}$ C, low frequency voltage noise to $1\frac{1}{2}\mu V$ p-p and bias currents from 50 to 300pA. Long term stability averages $1\mu V/month$. These amplifiers are widely accepted as the best choice when it is essential to maintain either low voltage offsets and bias currents versus time or against severe environmental changes, or whenever external offset adjustments are not possible or desirable.

MODEL 234 J/K/L: LOWEST NOISE, WIDEBAND

This latest inverting amplifier design from Analog Devices is virtually free of chopper spikes and is singled out as the industry's quietest, wide band chopper stabilized amplifier in a low cost module. To illustrate the significant improvement in performance, comparative noise signals are presented in the figure for model 234 and its predecessor model 232.

Available in three drift selections (1, 0.3 and $0.1\mu V/^{\circ}C$), model 234 specifications include voltage noise of $1\frac{1}{2}\mu V$ p-p, current noise of 2pA p-p, and 2.5MHz bandwidth. Slew rate is $30V/\mu$ sec. The wide bandwidth of 234 makes it especially useful for 16-bit D/A converters, high speed integrators as well as for low frequency applications including control systems, DVM input amplifier designs and other precision instrumentation. Attractively priced, its consistent unit-to-unit performance makes it an ideal choice for new OEM designs.

MODEL 233 J/K/L: LOWEST COST, $0.1\mu V/^{\circ}C$ The popular model 233 is a good choice for many low drift, high gain applications including precision integrators, instrument preamplifiers and null detectors as used to resolve microvolt error signals.

The combination of IC's and improved design techniques in this 0.4" high module results in good performance at low cost for OEM designs.

Typical specifications for this inverting amplifier include 500kHz bandwidth, $0.25V/\mu$ sec slew rate, 50pA bias current and $3\mu V$ p-p noise in a 10Hz bandwidth. It is available with three drift selections: 1; 0.3; and $0.1\mu V/°C$.

MODEL 260 J/K: $10^9 \Omega$ NONINVERTING, $0.1\mu V/^{\circ}C$ Analog Devices pioneered in the development of new "chopper" amplifier designs to provide high input impedance without compromising the excellent low frequency characteristics of chopper type amplifiers. As embodied in the model 260, this design is useful as a noninverting buffer amplifier for processing microvolt signals with minimal source loading errors. Typical specifications for the model 260 are $10^9 \Omega$ input impedance, drift to $0.1\mu V/^{\circ}C$ and CMR of 110dB at ±1V.

MODEL 261: GUARANTEED NOISE OF LESS THAN $1\mu V$ The model 261 is a second generation design which typically provides a significant improvement in the noise and bandwidth characteristics of model 260 and other competitive models.



	Lowest Cost General Purpose 233						
Model	J	К	L				
Open Loop Gain DC Rated Load, V/V min		10 ⁷					
Rated Output, min		±10V@5mA	A				
Frequency Response Unity Gain, Small Signal Full Power Response, min Slewing Rate, min Overload Recovery		500kHz 4kHz 0.25V/µs					
Input Offset Voltage Initial, 25°C (Adj. to zero) max Avg. vs. Temp (0°C to 70°C) max vs. Supply Voltage vs. Time	±50μV ±1.0	$\begin{vmatrix} \pm 20\mu V \\ \pm 0.3 \\ \pm 0.2\mu V/\% \\ \pm 2\mu V/mo. \end{vmatrix}$	$\begin{vmatrix} \pm 20 \mu V \\ \pm 0.1 \mu V /^{\circ} C \end{vmatrix}$				
Input Bias Current Initial, 25°C, max Avg. vs. Temp (0°C to 70°C) max	±2	±50pA ±1	±0.5pA/°C				
Input Impedance Differential Common Mode		600kΩ NA					
Input Noise Voltage, 0.01 to 1Hz, p-p 0.1 to 10Hz, p-p 10Hz to 10kHz, rms Current, 0.01 to 1Hz, p-p 0.1 to 10Hz, p-p		$ \begin{array}{c} 1 \mu V \\ 3 \mu V \\ 3 \mu V \\ 3 pA \\ 6 pA \end{array} $					
Input Voltage Range Common Mode Voltage, min Common Mode Rejection Max Safe Differential Voltage		NA NA ±15V					
Power Supply Range (VDC) Rated Specification (VDC)		±(12 to 18) ±15V@5mA)V A				
Temperature Range Operating, Rated Specifications		0 to $+70^{\circ}$	C				
Package Outline Case Dimensions	1.5	F-3 " x 1.5" x	0.4"				
Price 1-9 10-24	\$45 \$40	\$54 \$49	\$75 \$68				

Operating at a higher carrier frequency, this noninverting design features extremely low noise, 0.4μ Vp-p in a 1Hz bandwidth; low drift, 0.1μ V/°C; and an output that is virtually free of chopper spikes.

Model 261 also offers a solution to beat frequency problems caused by a low frequency carrier mixing with harmonics of the AC line. The carrier frequency on this design is nearly a decade higher than that of models previously available, thereby eliminating the possibility of any interaction with the line frequency or its harmonics.

The new model should be considered for all new instruments and circuit applications, or wherever improved performance, at no increase in cost, is desirable for existing sockets. Models 260 and 261 are mechanically and electrically interchangeable for these applications.

Model 261 will be available in production quantities by June of 1973. Evaluation units are available from stock.

MODEL 231 J/K: 25mA OUTPUT, 0.1µV/°C

Model 231, available in two drift selections $(231J, 0.25\mu V)^{\circ}C$ and 231K, 0.1 $\mu V/^{\circ}C$) is an inverting chopper stabilized amplifier with increased output current capability (25mA). With stable 3kHz full power response and low drift, it offers higher output without use of an additional booster stage for heavier load requirements.

MODELS 210/211: 100V μ sec WIDEBAND, $1\mu V/^{\circ}C$

Models 210/211 with 20mA output, are inverting chopper stabilized amplifiers for that class of application requiring low drift performance with good high frequency performance. This design will provide slew rates of 100V/ μ sec and 90dB of loop gain at 10kHz for improved wideband accuracy. Incorporating internal limiting circuitry, these amplifiers have exceptionally fast overload recovery, (0.2 μ sec) and stable input characteristics for high speed integrator and comparator designs. They are available in two drift selections (model 210, 1μ V/°C, model 211, 2μ V/°C).



DC to 1kHz Noise, Referred to the Input; 234 vs 232.

Η 1μV	High Performance Wideband μV p-p Lowest Noise 234		Low Cost Non-Inverting High Z _{IN} 260		General Purpose 25mA Output 231		High Banc 20mA Or 210/2	lwidth utput I 1
J	K	L	J	к	J	K	210	211
	10 ⁷		5 x 10 ⁶			10 ⁷	108	3
	±10V@5mA		±10V@5m.	A	±10	V@25mA	±10V@2	20mA
	2.5MHz 500kHz 30V/µs		100Hz 2 to 50H 100V/s 30ms	Z	50 0. 3	00kHz 3kHz 2V/µs 3.0sec	20M 500k 100V 0.2µ	Hz Hz /μs Ls
±50μV ±1.0	$\begin{vmatrix} \pm 25\mu V \\ \pm 0.3 \\ \pm 0.2\mu V/\% \\ \pm 2\mu V/mo. \end{vmatrix}$	$\begin{array}{c} \pm 25 \mu V\\ \pm 0.1 \mu V/^{\circ} C\end{array}$	$\begin{array}{c} \pm 25\mu\text{V}\\ \pm 0.3 & \ \pm 0\\ \pm 0.1\mu\text{V}/\%\\ \pm 1.0\mu\text{V}/\text{mod}\end{array}$	0.1μV/°C , o.	$\pm 15 \mu V$ ± 0.25 $\pm 0.$ ± 1.0	$\begin{vmatrix} \pm 10 \mu V \\ \pm 0.1 \mu V /^{\circ} C \\ 1 \mu V / \% \\ \rho \mu V / mo. \end{vmatrix}$	±100/ ±0.5 ±10µV ±1.0µV	μV ±1μV/°C 7/% /day
±4	±100pA ±2	±2pA/°C	±300pA ¹ ±10pA/°C	3	±100pA ±1.0	±50pA ±0.5pA/°C	±100pA	±150pA ±3pA/°C
	300kΩ NA		${80 k \Omega / /0.01 \over 10^9 \Omega / /0.02}$	μF μF	30	00kΩ NA	500k NA	Ω
	0.7μV 1.5μV 2μV 2pA 4pA		0.4μV 1.0μV 4pA 10pA		1. 1 5 1 3	5 μV 0 μV 5 μV 0pA 5 pA	5μV 10μV 10μV 10pA	
	NA NA ±15V		±1.0V 110dB ±20V		±	NA NA 15V	NA NA ±15	J
	±(12 to 18)V ±15V@5mA	/	±(10 to 18) ±15V@6mA)V A	±(12 ±15V@+	to 18)V -8, -10mA	±(12 to ±15V@+30	18)V , -4mA
	0 to $+70^{\circ}$ C		0 to $+70^{\circ}$	С	0 to	+70°C	0 to +7	0°C
1.5	F-3 5" x 1.5" x (0.4''	FA-6 1.5" x 1.5" x	0.62''	W. 3.6" x 1	A-1 .6" x 0.4"	R-7 2.87" x 1.37	и х 0.99″
\$54 \$49	\$65 \$59	\$89 \$82	\$49 \$45	\$64 \$58	\$80 \$74	\$115 \$105	\$157 \$148	\$113 \$107

LOW VOLTAGE DRIFT-DIFFERENTIAL INPUT, HIGH CMR MODELS 184, 153, 180, AD508, AD504

GENERAL DESCRIPTION

These "chopperless" amplifiers with differential input feature high open loop gain, low drift and good CMR for improved linearity and gain accuracy as required for many low level signal applications. As single ended or differential amplifiers they may be used for precision comparators, transducer and bridge circuits, or in general, to precisely amplify and process low level signals of moderate bandwidths. They should be selected over single-ended choppers whenever chopper noise and spikes are objectionable in the circuit design.

Advanced circuit techniques, coupled with careful component selection and processing, have made possible economical amplifier designs which challenge the low voltage drift of the chopper amplifier. Amplifiers in this group use differential bipolar input stages to achieve offset voltages and drifts up to 100μ V and 4μ V/°C respectively with good offset stability of 3μ V/month. These devices offer differential performance with input noise of 1μ V p-p and 100dB of CMR at ±10V. For comparison, chopper stability approaches 1μ V/month and are useful as single ended amplifiers only.

MODEL 184 J/K/L: 0.25µV/°C, 100dB CMR

These low drift "chopperless" amplifiers challenge the low drift and long term stability of choppers while avoiding "chopper noise and spikes." Their low noise $(1\mu V p-p)$ and low drift (to $0.25\mu V/^{\circ}C$, 184L) also make them the best choice among other amplifier types for processing low level transducer and bridge signals with source impedances up to $100k\Omega$. With internally trimmed offsets to $100\mu V$ (184 K, L), open loop gains of 110dB and a CMR of 100dB, the model 184 will provide good linearity and gain stability for singleended or differential amplifier configurations.

MODEL 153 J/K: BATTERY POWERED, 70 μ A CURRENT DRAIN

Incorporating the best features of the "chopperless" class of differential amplifiers, the model 153 has a bipolar input stage and is designed to operate from ± 2.7 VDC to ± 15 VDC power supply voltages. Using two 2.7VDC batteries, power consumption is held to 190 μ W at 70 μ A current drain while providing 2μ V/°C drift, 94dB of CMR and 2μ V rms of wideband noise. The model 153 is a best choice for amplifying low level signals from source impedances to 100k Ω where excellent power supply rejection is demanded such as in battery operated equipment.

MODEL 180 J/K: LOW BIAS CURRENT

These devices, with drifts of $1.5\mu V/^{\circ}C$ (180 J) and $0.5\mu V/^{\circ}C$ (180 K), are companion designs to model 184 but with reduced bias currents (4nA versus 25nA for 184). This sixfold improvement in bias current is achieved using current compensation techniques thereby permitting better current drift performance with higher source impedances (to 500k Ω). Package size is reduced below that of model 184 for critical space requirements.



	Lowest Cost Low Drift 184				
Model	J	К	L		
Open Loop Gain DC Rated Load, V/V min		300,000			
Rated Output, min Frequency Response Unity Gain, Small Signal Full Power Response, min Slewing Rate, min Overload Recovery		±10V@5mA 1MHz 5kHz 0.3V/µs			
Input Offset Voltage Initial, 25°C, max Avg. vs. Temp (0 to 70°C) max vs. Supply Voltage vs. Time	±25 0μV ±1.5	$\begin{vmatrix} \pm 100\mu V \\ \pm 0.5 \\ \pm 5\mu V/\% \\ \pm 3\mu V/mo.^3 \end{vmatrix}$	$\begin{vmatrix} \pm 100 \mu V \\ 0.25 \mu V / °C \end{vmatrix}$		
Input Bias Current Initial, 25°C, max Avg. vs. Temp (0 to 70°C) max		0, +25nA ±0.25nA/°C			
Input Difference Current Initial, 25°C, max Avg. vs. Temp (0 to 70°C) max		±2nA ±0.02nA/°C			
Input Impedance Differential Common Mode		$4 \times 10^{6} \Omega$ 2 x 10 ⁹ Ω			
Input Noise Voltage, 0.01 to 1Hz, p-p 5Hz to 50kHz, rms Current, 0.01 to 1Hz, p-p		1μV 4μV 10pA			
Input Voltage Range Common Mode Voltage, min Common Mode Rejection @ ±10V Max Safe Differential Voltage		±10V 100dB ±15V			
Power Supply Range (VDC) Rated Specification (VDC)		±(10 to 18) ±15V@9mA	V		
Temperature Range Operating, Rated Specifications		0 to $+70^{\circ}$:		
Package Outline Case Dimensions	1.5	F-1 " x 1.5" x	0.4"		
Price 1-9 10-24	\$39 \$37	\$55 \$52	\$65 \$62		
(1)±2.7 VDC supply voltage. (2)V _{OS} nulled.	(3)Wa	rm-up drift ±1	0 µ V, 20 mir		

AD504 J/K/L/M: LOW COST, $0.5\mu V/^{\circ}C$, $0.6\mu V$ (p-p) MAX NOISE

The monolithic AD504 is an extremely low drift, low noise operational amplifier that is designed for high precision applications where moderate source impedances are used. A double integrator circuit concept combined with a precise thermally balanced layout achieves gain greater than 10^6 , offset voltage drift below $0.5\mu V/^{\circ}C$, maximum noise (0.1Hz to 10Hz) of $0.6\mu V$ (p-p), bandwidth of 300kHz, and slew rate of $0.12V/\mu$ sec. The inputs and output are fully protected, and the amplifier will drive 1000pF of load capacitance. This combination of performance characteristics makes the AD504 ideally suited for numerous low level applications in precision measurement, telemetry, and data acquisition.

AD508 J/K/L: HIGHEST ACCURACY, LOW I_b , LOW DRIFT

Its combination of low drift $(0.5\mu V/^{\circ} C max)$, low input currents (1.0nA max I_{OS} , 10nA max I_b), and long term stability (10 μ V/month max) make the AD508 operational amplifier an excellent choice for all applications requiring the utmost in precise, highest accuracy performance. Guaranteed parameters also include gain greather than 10⁶, PSRR less than 10 μ V/V, CMRR above 110dB, and V_{OS} below 0.5mV. Dynamic performance is more than adequate with a unity gain slew rate of 0.12V/ μ sec and bandwidth of 300kHz. The outstanding long term stability of the AD508 is attained by subjecting 100% of the devices to special stabilization burn-in processing, with the AD508L achieving its maximum drift specification of 10 μ V/month following 600 hours of monitored operation.

Discrete						Micro	circuit					
Low Off Low Bias	fset Drift s Current 80	Battery General	Powered Purpose		Low Noise Low Offset, Drift, Cost AD504			Hi Lo	uracy Drift			
J	К	J	К	J	К	L	м	J	к	L		
300	.000	50	.000	250.000	500.000	1.000.000	1.000.000	250.000	500,000	1,000,000		
±10V@	02.5mA	±1V ¹	@1mA		±	10V@5mΛ			±10V@5m	Λ		
1MHz 10kHz 0.6V/μs 2.0ms		150 5kHz 0.02 2.	300kHz 1.5kHz typ 0.12V/µs typ			(300kHz 1.5kHz ty 0.12V/µs t	p yp				
$\begin{array}{c c} 25 \ 0\mu V & \pm 100\mu V \\ \pm 1.5 & \pm 0.5 \mu V/^{\circ}C \\ \pm 2 \mu V/\% \\ \pm 5 \mu V/m_{O} \end{array}$		±1.0mV ±5.0 ±1.0 ±5µ	$\begin{vmatrix} \pm 0.25 \text{mV} \\ \pm 2.0 \mu \text{V}/^{\circ}\text{C} \\ 0 \mu \text{V}/\% \\ \text{V/mo.} \end{vmatrix}$	$\begin{array}{c c c c c c c c c c c c c c c c c c c $			±2.5mV ±3.0 ±15	$\pm 0.5 \text{ mV}$ ± 0.5 $\pm 1.0 \mu \text{V/s}$ ± 10	$\begin{vmatrix} \pm 0.5 \text{mV} \\ \pm 1.0 \mu \text{V}/^{\circ} \text{C}^{2} \\ \end{vmatrix}$			
±4nA 0.1 ±0.05nA/°C		±3nA ±0.1nA/°C		$\begin{array}{ c c c c c c c c c c c c c c c c c c c$			±25nA ±100	±10nA ±40	±10nA ±40pA/°C typ			
±1 ±0.02	InA 2nA/°C	± ±0.0	3nA 5nA/°C	$\pm 40 nA$ $\pm 15 nA$ $\pm 10 nA$ $\pm 10 nA$ $\pm 10 nA$ $\pm 50 pA/^{\circ}C typ$		±40nA = ±15nA		$\pm 40nA \mid \pm 15nA \mid \pm 10nA \mid \pm 10nA \\ \pm 50pA/^{\circ}C typ$		±5.0nA ±14	±1.0nA ±4	$\frac{\pm 1.0 \text{ nA}}{\pm 4 \text{ pA}/^{\circ} \text{C typ}}$
2 x 10	$10^6 \Omega$	10 2 x	$ \begin{array}{c c} 10^6 \Omega & & & \\ x \ 10^8 \Omega & & & \\ 10^5 \Omega 4 pF \end{array} $			$4 \ge 10^6 \Omega$ $10^8 \Omega 4 pF$		2 F				
1μV 4μV 50pA		$\frac{1\mu V^1}{4\mu V}$ $\frac{10 pA}{2}$		(0.1 to 10Hz) 1.0µVp-p (100Hz) 10nV/√Hz rms (1kHz) 8nV/√Hz rms 9nV/√Hz rms max			(0.1 to (1001 (1kH	o 10Hz) 1. lz) 12nV/v z) 10nV/v	$0\mu V p-p$ $\sqrt{Hz} rms$ $\sqrt{Hz} rms$			
±1 100 ±1	10V 0dB 15V	$\pm 1V^1$ 94dB $\pm 10V$		±10V ±10V ±10V ±10V 120dB ±15V			±10V	±10V 120dB ±15V	±10V			
±(10 t ±15V@	to 18)V @5.5mA	±(2.5 ±2.7\	to 18)V /@70μA	±(5 to 18)V ±(5 to 15)V ±15V@1.5mA ±15'		t(5 to 18 15V@1.5r)V nA					
0 to	+70°C	0 to	+70°C		0	to $+70^{\circ}$ C			0 to $+70^{\circ}$	°C		
Q 1.125'' × 1.	2–1 125'' x 0.62''	1.5" x 1	F-1 1.5" x 0.4"			TO-99			TO-99			
\$72	\$90 \$84	\$40 \$38	\$50	\$11.20 \$11.20	\$19.80	\$28.00	\$30.00	\$21.20 \$21.20	\$29.80	\$38.00		

ELECTROMETER-ULTRA LOW BIAS CURRENT MODELS 310, 311, 41, 42, AD523

GENERAL DESCRIPTION

Amplifiers with bias currents less than 1pA are classified as suitable for electrometer use where frequency response and voltage drift are usually secondary requirements. Both varactor bridge and FET input designs are employed to achieve these bias currents ranging from one pico amp (10^{-12} A) to ten femptoamps (10^{-14} A) .

Available with either inverting, noninverting or differential inputs, these amplifiers are used as current to voltage converters with high impedance transducers such as photomultiplier tubes, flame detectors, pH cells and radiation detectors. To minimize RFI and other noise pickup problems, the varactor modulated amplifiers, operating at 10fA, are available with shielded cases.

VARACTOR BRIDGE ELECTROMETERS

MODEL 310 (INVERTING), MODEL 311 (NON INVERTING) These operational amplifiers feature extremely low input bias currents and high input impedances. They are applicable to a wide range of electrometer applications which have been traditionally fulfilled using vacuum tube types. Because of varactor bridge inputs, the solid state models 310 and 311 are best suited for applications characterized by extremely high source impedance or where infinitesimal currents must be measured or amplified accurately. In principle, the varactor bridge amplifier design is similar to that of the vibrating reed electrometers (parametric), but with the inherent advantages of solid state circuitry.

Typical specifications for models 310 and 311 include open loop gain of 100dB, 2kHz unity gain response, 0.4V/msec slew rate, initial bias current of 10^{-14} A, with 10^{-15} A/°C current stability, and low current and voltage noise of 10^{-15} A and 10μ V p-p (1Hz bandwidth) respectively. Two voltage drift selections are available: 310J, 311J with 30μ V/°C, and 310K, 311K with 10μ V/°C. Each is housed in an aluminum enclosure for improved shielding.

Model 310, with inverting input only, is most appropriate for use with current source signals such as gas chromatographs flame detectors and photomultiplier tubes. It is also useful for precision long term integrators or where extremely wide dynamic current range is needed as in log compression amplifiers. Current to voltage converters may also be developed using a feedback resistor for setting the conversion scale factor.

Model 311 has a single noninverting input for measuring voltage from very high source impedances where bias currents would create substantial offset errors. Such sources include pH cells or stored capacitor charge as found in long term track and hold applications. Common mode rejection is 100dB at ± 25 V with $10^{14}\Omega$ impedance to ground for reduced source loading errors.

FET INPUT ELECTROMETERS

MODELS 41, 42, AD523 (MONOLITHIC): This family of FET input amplifiers fully complements the varactor bridge



	Lowest Cost High Gain FET 42
Model	J K L
Open Loop Gain	
DC Rated Load, min	300,000
Rated Output, min	±10V@5mA
Frequency Response Unity Gain, Small Signal Full Power Response, min Slewing Rate, min Overload Recovery	1MHz 4kHz 0.25V/µs 10ms
Input Offset Voltage Initial, 25°C, (adj. to zero) Avg. vs. Temp (0 to 70°C) max vs. Supply Voltage vs. Time	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$
Input Bias Current Initial, 25°C, max Inverting Input (Varactor) Non-Inverting Input (Varactor) Avg. vs. Temp (0 to 70°C)	350fA 100fA 75fA
Input Impedance Differential Inverting Input (to common) Non-Inverting Input (to common) Common Mode (FET)	$10^{13} \Omega //3 pF$
Input Noise Voltage, 0.01 to 1Hz, p-p 5Hz to 50kHz, rms Current, 0.1 to 10Hz, p-p 1 to 100Hz, rms (Varactor)	6μV 8μV 5fA
Input Voltage Range Common Mode Voltage, min Common Mode Rejection Max Safe Differential Voltage	±10V 66dB@±1V ±15V
Rated Specification (VDC)	$\pm (12 \text{ to } 18)V$ $\pm 15V@2mA$
Temperature Range Operating, Rated Specifications	0 to $+70^{\circ}$ C
Package Outline Case Dimensions	QB-1 1.1" x 1.1 " x 0.57"
Price	
1-9 10-24	\$25 \$23 \$29 \$37 \$37
(1)With external 4.99k trim.(2)With trim terminal open.	(3)Max bias at 70°C (4)Signal input only

designs for electrometer applications. Available in three package sizes, these designs provide high input impedance, sub-picoamp bias currents and improved bandwidth characteristics. They may be used single-ended or differentially for making low level current or voltage measurements from photo/ion current transducers, pH cells, photometers or, in general, where speed and low input capacitance are essential for accurate measurements at high impedance levels as found in automated test systems. Other applications include fast integrators, charge amplifiers, differentiators and long term integrators. In addition, these carrier-less units overcome certain RFI problems which may arise in extremely noisy environments using the varactor bridge modulator types.

Model 42 J/K/L Improved Performance: Undoubtedly one of the best values for OEM designs, this differential FET amplifier has 110dB open loop gain, for improved closed loop accuracy, 1MHz unity gain response and CMR of 66dB at \pm 1V CMV. It is available in three current selections ranging from 0.35pA to 75fA. Each device features all hermetically sealed semiconductors, with monolithic front end, in a compact module for improved reliability and good thermal transient response. Model 41 J/K/L: This device combines outstanding bias current and drift specifications with speed and full differential input capability for use in a broad range of electrometer and integrator applications as well as for wideband differential and buffer circuitry. Typical specifications include 50kHz full power response, 94dB CMR at \pm 5V (80dB at \pm 10V), 100dB gain for improved closed loop performance, and three bias current and drift selections: 41J, 0.5pA and 25 μ V/°C; 41K, 0.25pA and 10 μ V/°C; and 41L, 0.15pA and 25 μ V/°C. Special packaging techniques assure 10¹³ input impedance, free from internal current leakage paths, and a maximum 4pA bias current rating at +70°C.

Model AD5 23: This unit is a very low bias current IC op amp. It features maximum steady-state bias currents (either input) as low as 0.25pA, in a special low-leakage TO-99 metal can package that minimizes case leakage by utilizing a special guard pin and high resistivity glass insulation. The AD523 is short circuit protected and offset voltage nullable, and features drift of $15\mu V/^{\circ}$ C, slew rate of $4V/\mu$ sec, and large signal voltage gain of 25,000 V/V. It is available in J, K, L (0 to +70°C) and S (-55°C to +125°C) specification versions. (See also LInear IC Section).

Discrete			Microcircuit			
Wideband High CMR 41	Varactor Inverting 310	Varactor Non-Inverting 311	Differential 0.25pA Guarded Input AD523			
J K L	ј к	Ј К	J K L			
100,000	100,000	100,000	25,000 40,000 40,000			
±10V@5mA	±10V@5mA	±10V@5mA	±10V@5mA			
1MHz 50kHz 3V/μs 2μs	2kHz 7Hz 0.4V/ms 10ms	2kHz 7Hz 0.4V/ms 10ms	500kHz 50kHz typ 3.0V/μs 6μs			
$\begin{array}{ccc} \pm 2mV^2 \\ \pm 25 & \begin{array}{c} \pm 2mV^2 \\ \pm 10 \\ \pm 10 \mu V/\% \\ \pm 250 \mu V/mo. \end{array}$	Adjust to zero ±30 ±10µV/°C ±100µV/% ±100µV/mo.	Adjust to zero ±30 ±10µV/°C ±100µV/% ±100µV/mo.	$\begin{array}{c ccccc} \pm 50 mV & \pm 20 mV & \pm 20 mV \\ \pm 90 & \pm 30 & \pm 60 \mu V/^{\circ} C \\ \pm 30 & \pm 15 & \pm 15 \mu V/\% \end{array}$			
0, -0.5pA -0.25pA -0.15pA 	±10fA ±1nA ±1fA/°C ⁴	±1nA ±10fA ±1fA/°C ⁴	0, -1.0pA -0.5 -0.25pA 			
$10^{13} \Omega //3 \mathrm{pF}$	3 x 10 ¹¹ Ω	$\begin{array}{c} 3 \times 10^{11} \Omega \\ 10^9 \Omega \\ 10^{14} \Omega \end{array}$	$10^{12} \Omega$ 			
8μV 10μV 5fA	10μV 10μV(1 to 100Hz) 1fA (0.01 to 1Hz) 2fA	10μV 10μV(1 to 100Hz) 1fA (0.01 to 1Hz) 2fA	20µV 			
±10V 94dB@±5V ±15V	NA NA ±300V	±25V 100dB@±25V ±300V	±8V 70dB min 80dB min ±10V			
±(12 to 18)V ±15V@8mA	±(12 to 18)V ±15V@+15, -6mA	±(12 to 18)V ±15V@+15, -6mA	±(5 to 18)V ±15V@7mA			
0 to +70°C F-2	0 to +70°C W-1	0 to +70°C W-1	0 to +70°C			
1.5" x 1.5" x 0.4"	3" x 1.65" x 0.67"	3" x 1.65" x 0.67"	(guard pin 8 conn. to case)			
\$45 \$55 \$64 \$42 \$51 \$60	\$59 \$95 \$55 \$90	\$59 \$95 \$55 \$90	\$22 \$30 \$22 \$30 \$34 \$34			

HIGH OUTPUT VOLTAGE, CURRENT MODELS BIOO, 50, 163, 165, 171, AD512



GENERAL DESCRIPTION

Amplifiers in this category are unique with respect to their output voltage and/or current capability. In general, amplifiers offered here have bipolar or FET inputs with output voltage swings of ± 20 volts or output currents to ± 100 mA. These amplifiers may be used to achieve higher output voltage or current swings, or as boosters for op amps. Typical applications include galvanometer amplifiers, audio amplifiers, deflection amplifier drives, voltage or current regulators and sonar transducer drives.

MODEL B100: 100mA OP AMP BOOSTER

As a unity gain current booster, the B100 will deliver up to 100mA at \pm 10 volts output and operate in a closed loop configuration with an op amp. Its 1MHz full power response rolls off at a stable 6dB per octave making it suitable for use with op amps designed to have crossover frequencies up to 1MHz. B100, with short circuit protected output, is useful as a power booster for instrument servo loops, audio systems, galvanometer drivers, and wherever clean power must be delivered to loads at moderate bandwidths, to 1MHz.

MODEL 50 J/K: WIDEBAND 100mA DRIVER AMPLIFIER

The model 50, an extremely fast amplifier, should be considered for higher current outputs if settling time, slew rate or bandwidth are critical. This differential FET op amp will deliver 100mA at ±10 volts, up to 10MHz, for a wide range of high frequency designs, including boosters and driver stages as used in CRT deflection amplifiers. Typical specifications include 86dB open loop gain, 1nA bias, 80ns settling to 0.1%, CMR of 72dB at ±10V and two drift selections: $50\mu V/^{\circ}C$ (J) and $15\mu V/^{\circ}C$ (K).

MODEL 163 A/K: 20 VOLT/20mA ECONOMY

The model 163 offers good performance at a low cost for designs requiring higher output capability of ± 20 volts at 20mA. This differential amplifier with bipolar input stage may be used in most general purpose designs with source impedances up to $10k\Omega$ for best performance.

MODEL 165 A/K: 20V/5mA ECONOMY

Model 165, a companion design to model 163, has reduced 5mA output at ± 20 volts with equivalent performance at even lower costs. Two offset drift selections are available: $5\mu V/^{\circ}C$ (K) and $20\mu V/^{\circ}C$ (A).

herwise noted.)	100mA Booster Lowest Cost B100		
Model			
Open Loop Gain			
DC Rated Load, V/V, min	0.85		
Rated Output, min	±10V@100mA		
Frequency Response			
Unity Gain, Small Signal			
Full Power Response, min	1MHz		
Slewing Rate, min	65V/µs		
Overload Recovery			
Input Offset Voltage			
Initial, 25°C, (Adj. to zero)	±200mV (no adj.)		
Avg. vs. Temp, max	±1mV/°C		
vs. Supply Voltage			
vs. Time	***		
Input Bias Current	12 (200 Mar 1/2)		
Initial, 25 C, max	±500nA		
Avg. vs. Temp, max	***		
Input Difference Current			
Initial, 25 C	NA		
Avg. vs. Temp			
Difference	0 1030		
Common Mode	9 x 10- 52		
Input Naisa	NA		
Voltage 0.01 to 1Hz p-p			
10Hz to 10kHz rms	NA		
Current, 0.01 to 1Hz, p-p	1973		
Input Voltage Range			
Common Mode Voltage, min	NA		
Common Mode Rejection	NA		
Max Safe Differential Voltage	±15V		
Power Supply Range (VDC)	±(14 to 16)V		
Rated Specification (VDC)	±15V@8mA		
Temperature Range			
Operating, Rated Specifications	-25 to +85°C		
Package Outline	0-1		
Case Dimensions	1.1" x 1.1" x 0.4'		
Price			
1-9	\$30		
10-24	\$29		

MODEL 171: ±20V TO ±150V FET AMPLIFIER

Model 171 is an extremely versatile differential FET amplifier featuring output voltages to within 10V of the supplies, for supplies ranging from $\pm 20V$ to $\pm 150V$. Asymmetrical supplies may also be used with combinations of -0V, +300V, or -300V, +0V, or any combination of + and - supplies where the difference between supplies is held to less than 300V.

This design also features low drift of $15\mu V/^{\circ}C$ for 171K, $7\mu V/V$ of power supply rejection and common mode rejection of greater than 100dB for common mode voltages to within 10V of either supply.

AD512 K/S: HIGH CURRENT

Models AD512K and AD512S are monolithic operational amplifiers specifically designed for high output current capability. High efficiency output transistors, thermally balanced chip design and precise short circuit current control insure against gain degradation at high current levels and temperature extremes. Typical specifications include 12mA at $\pm 10V$ output from 0 to $+70^{\circ}$ C, $20\mu V/^{\circ}$ C drift, 5nA bias current, 90dB CMR and $0.5V/\mu$ sec slew rate at full load. The AD512S is designed to operate from -55° C to $+125^{\circ}$ C. (Also see Linear IC Section).

		Discrete							Micr	ocircuit			
20V Output 20V Output 20mA, High Gain Economy High Gain 163 165		140V Output 171			100mA Dr Wideband 10M 50	100mA Driver Wideband 10MHz f _p 50		ed 12/10mA c. Temp. D512					
А	к	Α	к	J		к	J	к	К	S			
±20	500,000 0V@20mA	250,000 ±20V@5r	D nA		10 ⁶ ±115V@10mA		25,000 ±10V@100)mA	5) ±10V@12mA	0,000 ±10V@10mA			
	1.5MHz 50kHz 6V/µs 0.5µs	1.5MHz 50kHz ¹ 6V/μs 0.5 μs		2MHz 15kHz 10V/μs 5μs		2MHz 15kHz 10V/µs 5µs		2МНz 15kHz 10V/µs 5µs		80MHz 8MHz 500V/µ 0.2µs	5	1. 1 0.5	OMHz OkHz V/μs typ
±20 ±2	±5mV ±5μV/°C ±10μV/% 200μV/mo.	$\begin{array}{c} \pm 5 \text{mV} \\ \pm 20 \\ \pm 10 \mu \text{V} \\ \pm 200 \mu \text{V} \end{array}$	±5μV/°C % πο.	±50	±1mV μ ±1μV/% ±250μV/mo.	±15µV/°C	±3mV ±50 ±30μV/ ⁴ ±500μV/r	±15µV/°C % no.	±3r ±20 ±1:	$\frac{1}{5 \mu V/\%} \pm 25 \mu V/^{\circ} C$			
±0.6	+35nA ±0.5nA/°C	+ 35 nA ±0.6	±0.05nA/°C	-50	2x/10°C	-20pA	0, -2n/ 2x/10°	C	±2	200nA —			
±0.1	±3nA ±0.05nA/°C	±0.1 1	±0.05nA/°C	±25	2x/10°C	±10pA	±50pA 2x/10°C	:	±0.1	50nA ±0.1nA/°C			
	10 ⁶ Ω 10 ⁹ Ω	10 ⁶ Ω 10 ⁹ Ω			$10^{11}\Omega$ $10^{11}\Omega$		$10^{11}\Omega$ $10^{11}\Omega$		2 x	10 ⁶ Ω			
	1μV 2μV 20pA	1μV 2μV 20pA			4μV 2.5μV 0.1pA		5μV 3μV 0.1pA			2μV 4μV			
	±20V 86dB ±40V	±20V 86dB ±40V			±115V 100dB ±125V		±10V 86dB ±15V		3 5 3	12V 90dB 30V			
±(2 ±2	2 to 26)V 24V@2mA	±(22 to 2 ±24V@4	26)V nA		±(25 to 150)V ±125@6mA		±(12 to 18 ±15V@40	n)V mA	to ±18V ±15	to ±22V max V@2mA			
25 to +85°C	$ \begin{vmatrix} 0 & to + 70^{\circ}C \\ F-1 \\ t & 1.5'' & x & 0.4'' \end{vmatrix} $	-25 to +85°C M-1 1″ x 1″ x	0 to +70°C		0 to +70°C B-1 1.8″ x 2.4″ x 0.6	,"	0 to +70° N-1 1.2″ x 1.8″ x	C 0.6″	0 to +70°C To	-55 to +125°C D-99			
\$36 \$34	\$46 \$43	\$24 \$20	\$34 \$29	\$69 \$66		\$79 \$75	\$75 \$62	\$92 \$75	\$6 \$6	\$9 \$9			

INSTRUMENTATION AMPLIFIERS MODELS 603, 605, 602, AD520

GENERAL DESCRIPTION

The instrumentation amplifier is a commited gain amplifier containing precision feedback networks. Its excellent linearity and noise rejection capability make it a natural choice for extracting and amplifying low level signals in the presence of high common mode noise voltages. These devices are commonly used as transducer amplifiers for thermocouples, strain gauge bridges, current shunts, biological amplifiers, or simply as preamplifiers for processing small differential signals superimposed on common mode voltages.

Differing from operational amplifiers with uncommitted gain, the instrumentation amplifier has a differential input stage usually requiring only one resistor adjustment to vary the gain over a wide range (typically 1 to 1000V/V). These compact devices may be placed in close proximity to the signal source for further noise reduction. Products from this group are available with low drift (under $1\mu V/^{\circ}C$), fast settling time (25μ sec to 0.01%) and economy. Models are also available with high CMRR, excellent linearity, and moderate drift for general purpose use.

MODEL 605 J/K/L: LOW DRIFT, IMPROVED PERFORMANCE

For moderate bandwidth applications requiring excellent drift, gain linearity and stability, the model 605 is a top performer when used with source impedances up to $10k\Omega$. This design requires one gain setting resistor for operation and includes output remote sense terminal, and output reference adjust terminal. Typical specifications are: 0.01% gain nonlinearity; 1 to 1000V/V gain range; 94dB CMR at G = 100V/V; 100nA bias and three RTI drift selections: $\frac{1}{2}\mu V/^{\circ}C$ (L); $\frac{1}{\mu}V/^{\circ}C$ (K) and $\frac{3}{\mu}V/^{\circ}C$ (J) at 1000V/V gain. Its low RTO drift now guaranteed at $50\mu V/^{\circ}C$ (L) makes it especially attractive for low gain applications.

MODEL 603 J/K/L: GENERAL PURPOSE, PRICE REDUCTION

This FET input design features high input impedance and low bias current to meet most general purpose applications operating with both high and low impedance signal sources at moderate bandwidths. Model 603 is available in three RTI drift selections $-50\mu V/^{\circ}C$ (J); $15\mu V/^{\circ}C$ (K); and $5\mu V/^{\circ}C$ (L) for 1000V/V gain. This model incorporates other desirable features, including: remote output sense terminal, permitting its use as a current feedback amplifier or use with a booster; output reference adjust terminal, allowing ±10 volts output swing adjustment independent of gain; and gain adjustment from 1 to 2000V/V, using a single resistor. Key specifications include: 0.2% gain nonlinearity; 1MHz bandwidth and 40μ sec settling time to 0.1%, all at 1V/V gain; RTO drift of $500\mu V/^{\circ}C$, and operation from 12 to 20VDC dual power supplies.

Simplification of this design has been made possible by the advent of improved semiconductors. This savings is being passed on resulting in a new low 1-9 price of \$50 for model 603L.



(Specifications typical @ +25°C and ±15VDC power supply unless otherwise noted.) Economy eral Purpose FET 603 L Model K Gain 1 to 2000 Range $G = 10^5 / Rg$ Formula ±3.0% Deviation From Formula, max ±50ppm/°C vs. Temp, max ±0.2%/mo. vs. Time ±0.2% Nonlinearity, max ±10V@5mA Rated Output, min Frequency Response Unity Gain, Small Signal, (-3dB) 1.0MHz G = 1 1.0kHz G = 100010kHz Full Power Response, min $\frac{2V/\mu s}{40\mu s(G = 1)}$ Slew Rate Unity Gain Settling Time to 0.1% Offsets Referred to Input Adjust to 0 Initial Offset Voltage ±0.5mV/°C vs. Temp, max G = 1 ±50 ±15 1 ±5 µV/°C G = 1000±1.0mV/% G = 1vs. Supply ±3.5 µV/% G = 1000Input Bias Current 0, -50pA 0, -20pA 0, -20pA Initial, 25°C $2x/10^{\circ}C$ vs. Temp Input Difference Current Initial, 25°C ±10pA $2x/10^{\circ}C$ vs. Temp. Input Impedance $10^{12} \Omega //5 pF$ Differential $10^{12} \Omega //5 pF$ Common Mode Noise Referred to Input Voltage Noise, 0.01 to 1Hz, p-p 100µ V G = 2.0 µV G = 1000Voltage Noise, 10Hz to 10kHz, rms 80µV G = 1Input Voltage Range Linear Differential Input ±10V Max Differential Input $\pm V_{S}$ ±V. Max Common Mode CMR @ ±10V. DC to 60Hz 70dB@ ±8V $(1k\Omega Imbalance G = 1)$ 80dB G = 1000Reference Terminal $10^7 \Omega$ R_{in} ±10V Output Offset Range Gain Offset Range 1±0.03 +0. -2µA **Bias** Current Power Supply Range, ±V_s(VDC) ±(12 to 20)V Operating, Rated Specifications (VDC) ±15V@7mA Temperature Range 0 to $+70^{\circ}C$ Operating, Rated Specifications Package Outline FA-5 1.5" x 1.5" x 0.62" **Case** Dimensions Price 1-9 \$39 \$45 \$50 10-24 \$37 \$43 \$45

MODEL 602 J/K: FIXED GAIN, LOW DRIFT

Unlike most instrumentation amplifiers, with externally adjustable gain, model 602 gain is internally trimmed to 0.05% accuracy, for gains of 10V/V (602J-10) and 100V/V(602J-100). For added versatility, an external resistor may then be used to increase gain ten fold to 100V/V and 1000V/V respectively. These design, with bipolar input, feature low RTI drift of $10\mu V/^{\circ}C$ (602J) and $2\mu V/^{\circ}C$ (602K) with low initial voltage offset making the 602 "ready to use" for a wide range of applications with source impedances up to $10k\Omega$. An active shield drive terminal is also provided to bootstrap the input cable capacitance for improved high frequency performance when using long cable runs.

AD520 J/K/S: LOW DRIFT, MONOLITHIC

The model AD520 is a monolithic instrumentation amplifier which incorporates many features found in more expensive modular type designs. These include: two external resistors for setting gain from 1 to 1000V/V; remote output sense terminal for current amplifier applications; and reference adjustment terminal for setting output level up to $\pm 10V$ independent of gain. Other characteristics include $5\mu V/^{\circ}C$ RTI drift (AD520 K/S); 106dB CMR (1k Ω imbalance), all at Gain = 1000V/V; 40nA bias; and 0.02% gain nonlinearity.

Discrete	Microcircuits			
High CMR, Low Drift 0.005% Linearity 605	Low Offset Fixed Gain 602	Economy Monolithic AD520		
J K L	J-10 J-100 K-100	J K S		
1 to 1000 G = 1 + (200k/Rg) ±0.1% ±15ppm/°C ±0.0003%/mo. ±0.005% ±10V@5mA	$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	$ \begin{array}{c} 1 \text{ to } 1000 \\ G = 10^5 / Rg \\ \pm 0.05\% \\ - \\ - \\ \pm 0.02\% \text{ typ} \\ \pm 10V@5mA \end{array} $		
300kHz 300Hz 1.5kHz typ 0.1V/μs 130μs(0.01%, G = 1)	75kHz -1%@1kHz 200µs 50µs 50µs	200kHz 25kHz 50kHz typ 2.5V/µs typ		
$\begin{array}{c c} Adjust to & 0 \\ \pm 100 & & \pm 75 \\ \pm 3 & & \pm 1.0 \\ \pm 0.2 m V/{}^{\circ}_{0} \\ \pm 4 \mu V/{}^{\circ}_{0} \end{array}$	$\begin{array}{c c c c c c c c c c c c c c c c c c c $	$\begin{array}{c c c c c c c c c c c c c c c c c c c $		
0. +100nA -1nA/°C max	±50nA ±1nA/°C	±40nA ±20nA ±20nA ±0.5 ±0.2 ±0.5nA/°C		
±100nA max ±1nA/°C max	±5nA ±1nA/°C	±10nA ±0.1nA/°C		
10 ⁹ Ω 10 ⁹ Ω	10 ⁹ Ω//50pF 10 ⁹ Ω//50pF	2 x 10 ⁹ Ω 2 x 10 ⁹ Ω		
15μV(0.1 to 10Hz) 1.5μV(0.1 to 10Hz) 5.0μV	2.5μV RTI 2.5μV RTI at specified gain	5μV (dc to 10Hz, G = 1000) 1mV (10Hz to 200kHz, G = 1) 2μV (1Hz to 5kHz, G = 1000)		
±10V	±1.0V = ±0.1V = ±0.1V	±10V		
$\pm 20V$ $\pm V_s$	±10V ±10V ±10V	±Vs ±Vs		
70dB ³ 94dB(120dB typ)DC to 5Hz ³	80dB 100dB 100dB	80dB 95dB 106dB 106dB		
10 ⁴ Ω ±10V +1.00 200nA	NA 	5 x 10 ⁷ Ω ±10V +1.000 500nA		
±(12 to 18)V ±15V@7mA	±(15 to 16)V ±15V@14mA	±(5 to 18)V ±15V@4mA		
0 to +70°C F-5	0 to +70°C FA-2	-55°C to 0 to +70°C 0 to +70°C +125°C TO-116		
1.5" x 1.5" x 0.4"	1.5" x 1.5" x 0.62"	-		
\$59 \$65 \$80 \$56 \$62 \$75	\$59 \$55 \$75 \$55 \$52 \$72	\$18.00 \$24.00 \$33.00 \$18.00 \$24.00 \$33.00		

ernally	adju	stable	to	100.	Speci-	

- Externally adjustable to 100. Specifications shown for G = 10.
- Externally adjustable to 1000. Specifications shown for G = 100.
- ±0.1% amplitude accuracy to 1kHz min.
- Constant with gains from 3V/V to 1000V/V.
- (5) Minimum CMR with $1k\Omega$ imbalance.

ISOLATION AMPLIFIERS MODELS 272, 273, 274

INTRODUCTION

During 1971 Analog Devices developed and introduced a series of DC coupled isolation amplifiers which are unique to the industry. Offering total ground isolation and low stray coupling capacitance (< 10pF) between input and output grounds, these compact modules develop extremely high CMR (115dB @ 60Hz) and CMV ratings (to 5kV) using modulation techniques with transformer isolation. Capable of transmitting millivolt signals in the presence of up to 1000 volts common mode, with unity gain or with adjustable gain, these amplifiers are ideal for medical (ECG) and industrial applications where it is important to isolate hospital patients from potentially lethal ground fault currents or, in industrial applications, to interrupt ground loops between transducers and output conditioning circuits.

All models are designed to improve on the existing patient safety specifications of Underwriter's Laboratories and other regulator agencies. When used for ECG and EEG patient-monitoring equipment, these amplifiers will do their job without exposing the hospital patient to the hazards of microshock and possible electrocution.

GENERAL DESCRIPTION

(The block diagram for the 272 and 273 can be found in the section "Applying the Isolation Amplifier," page 29). Isolation amplifiers are available as unity gain buffer amplifiers (models 272J, 273J, 273K) or with externally adjustable gain (model 274J). All devices are package and pin compatible except for model 274 which has two additional pins; an additional input pin for low noise applica-



tions and a gain trim pin. Electrically they feature FET input op amps for use with high source impedance circuits as well as "fail safe" front end circuitry and 10μ A fault current limit for improved patient safety in medical applications.

Typical specifications include 115dB CMR ($5k\Omega$ source imbalance), 5kV CMV, patient safety leakage current of $1\mu A @ 117VAC$ ($2\mu A @ 220VAC$) and 2-wire +15VDC power input. Isolation is achieved using carrier modulation techniques (150kHz) with transformer coupling for superior reliability and low cost. Small signal frequency response is from DC to 2kHz with full power response to 200Hz.

Defibrillator and "fail safe" protection is achieved using passive elements for ultimate reliability. Each model will repeatedly support a 5kV defibrillator pulse from input to output or directly across the ECG input leads, except for model 273J. Eliminated is the need for any additional patient circuit current limiters or other special external devices (spark gaps, neon bulbs, zener diodes, FETS), which tend to degrade CMR, decrease reliability and increase cost. Patient safety test circuits (272, 273, 274) for these designs are shown in Figures 2 and 3.



Figure 1. Block Diagram – MODEL 274J



LOW NOISE, ADJUSTABLE GAIN: MODEL 274J

Offered as the most versatile isolation amplifier in the series, this design has a full ± 10 volt output swing, adjustable gain (1 to 100V/V) and two "high" input terminals for optional degrees of input protection and noise performance. Referring to Figure 12, Page 30, the two input terminals tie into the same amplifier point with terminal #1 (ECG) connected through a $2M\Omega$ series input resistor and terminal #2 (EEG) connected directly with no input amplifier-protection resistor.

Gain is set by varying the gain ratio network formed by the internal $2M\Omega$ feedback resistor and external resistor, R_x . The $2M\Omega$ feedback resistor appears as a noise source, whose noise level referred to the amplifier input, decreases as gain level increases and R_x decreases. Increasing amplifier gain, therefore, reduces input noise. The external resistor, R_x , can range from infinity to $20k\Omega$ as gain varies from 1V/V to 100V/V. Larger gains are possible at a sacrifice in reduced loop gain and overall amplifier accuracy, which nevertheless may be adequate for the application. It should be noted that the output circuit and power supply circuit are transformer isolated from each other as well as from the input circuit. The 5kV isolation rating applies input to either power or signal grounds with a reduced rating applying between power ground and output low.

Applications

For industrial or medical applications, gain should be taken in the amplifier consistent with normal mode offset voltages to reduce noise and drift referred to the input. The proper choice of input high terminal (#1 or #2) depends on the degree of input amplifier protection required for the application. Input #1 (2M Ω input) should be selected for defibrillator protection (5kV) with gains set from 1 to 20V/V (assuming a worst case 500mV galvanic offset potential). Over this gain range, noise will vary from approximately 16µV p-p (G = 1V/V) to $12\mu V p - p(G = 20V/V)$ in a 100Hz bandwidth. EEG, EMG or direct blood pressure monitoring circuits may use input #2 terminal with maximum allowable gain for lowest noise performance. Noise will vary from 12µV p-p (G = 1V/V) to 5µV p-p (G = 100V/V) in a 100Hz bandwidth. Input protection is dependent on the value and wattage ratio of R_x. When using a one watt resistor, differential input protection is 1000V to 200V as gain varies from 1 to 100V/V. $R_x = 20k\Omega$, 1W at 100V/V gain. Input/ output isolation of 5kV is independent of gain connection or amplifier-input protection resistor. It is interesting to note that 274J may be used as an ECG and EEG amplifier in one design through appropriate lead and gain selection using a two pole-two position function switch.

LOW NOISE, DEFIBRILLATOR PROTECTED INPUT: MODEL 273K

This unity gain device is electrically and mechanically interchangeable with models 272J and 273J except for a different value of input safety resistor. Referring to the 272/273 block diagram, the 273K uses a $2M\Omega$ input resistor versus $20M\Omega$ for 272J and $1M\Omega$ for 273J. This change has the net effect of combining, in one module, the desired 5kV input protection of the 272J at a slight increase in noise above that of 273J.

The 273K should be considered for all new and original equipment designs requiring 272J defibrillator input protection and 273J input noise performance. Noise levels are typically 12μ V p-p in a 100Hz bandwidth. All other isolation amplifier characteristics not involving this input resistor change remain essentially the same.

LOW NOISE, LOW DRIFT: MODEL 273J

Very similar to models 272J and 273K, except for its $1M\Omega$ input resistor, model 273J provides an isolation amplifier with the lowest voltage drift and noise level available. Noise at 8μ V p-p is a factor of 3 below that of 272J.

Model 273J with \pm 3V dynamic range and 75 μ V/°C drift will support 400VAC differentially for defibrillator free input signals while retaining a 5kV rating from input terminals to output common. It is useful as a unity gain buffer for medical applications not requiring input defibrillator protection or where other external protection devices may be used successfully to protect the amplifier against 5kV. It is mechanically interchangeable with 272J and 273K.

UNITY GAIN, DEFIBRILLATOR PROTECTED INPUT: MODEL 272J

This design is available to meet the most demanding requirements for amplifier and patient protection simultaneously. Referring to model 272 block diagram and the safety circuits (Figures 2 and 3) the input stage employs a $20M\Omega$ guarded resistor (R) to limit differential fault currents to 10μ A in the event a catheterized patient develops 220VAC between patient-connected high and low electrode. This can occur through an inadvertent connection to power ground through misapplication or via other equipment grounds. Of course, a full 5kV defibrillator voltage is easily supported across the inputs and from all input leads to output common. The price of this protection is a relatively high amplifier noise level (typically $35\mu V/p-p$) arising from the 20M Ω Johnson noise. Model 272J, with ± 3 volt dynamic signal swing and unity gain, is most useful for those designs requiring ultimate safety to both amplifier and patient (or transducer) circuit. It is extremely useful in high radiation environments where strong emission may destroy input circuitry.

		1µA Safety Current, 5	kV Isolation
	Buffer Ultimate Safety	Low Noise Buffer 273	Adjustable Gain ECG/EEG Inputs Lowest Noise
Model	272J	J K	274J
Gain (Non-Inverting)			
Gain (50k Load)	1V/V	1V/V	1 to 100V/V
Gain Temp Coefficient	0.015%/°C	0.015%/°C	0.015%/°C
Gain Accuracy	±3%	±3%	+0, -2%
Safety Current Limits	Fig. 2 & 3	Fig. 2 & 3	Fig. 2 & 3
Input	0	0	
Input Impedance: Differential	$10^{12} \Omega / / 3 pF$	$10^{12} \Omega //3 pF$	$10^{12} \Omega //3 pF$
Overload Conditions	$20M\Omega$ min	$1M\Omega \min \left[2M\Omega \min \right]$	$2M\Omega$ min
Common Mode	$10^{11} \Omega / (1 \text{ pF})$	$10^{11} \Omega //20 nF$	$10^{11} \Omega / 20 pF$
Input Offset Voltage	10	10 //2000	
Initial, 25°C	±50mV	+50mV	±2mV
Refer to Output (RTO)	125 UV/°C	$100 \mu V/^{\circ}C$	$(100G + 200)\mu V/^{\circ}C$
vs. Supply Voltage	20µV/%	20/1V/%	2011V/%
Input Bias Current	204 11/0	20 μ V / /0	204 17.0
Initial 25°C	-5004	-5004	-50pA
vs. Temp $(0 \text{ to } 70^{\circ}\text{C})$	2×/10°C	2:/10°C	$2x/10^{\circ}C$
vs. Supply Voltage	2x/10 C	2X/10 C	0.1pA/%
Input Noise	0.1pA/ %	0.1pA/%	
Voltage $(0.05 \text{ to } 100\text{Hz})$ C = 1			
Voltage (0.05 to 100H2), G = 1	25 1111	0.011	164V p-p 124V p-p(G=100
Input #1	35µv p-p	8μv p-p 12μv p-p	$12\mu V$ p-p $5\mu V$ p-p(G=100
(5Up to 1b(lp))	INA 15 UN	NA	Sulv rms
(5HZ (0 KHZ))	$15\mu v \text{ rms}$	$5\mu v rms$	0 InA rms
Current (0.05 to 100Hz)	0.1pA mis	0.1pA mis	o. ipit inis
Abashuta Man Differential of CMV			5000V (Input #1)
(10 see of 60Hz pulse train)	5000V peak	400V 5000V	Depends on Gain (Input #2
(10 sec of oonz pulse train)	5000v peak	4001 00001	Depends on Gam (mput #2
(input to output signal)	1000V neak	1000V peak	1000V peak
(input to output signal) $CMD \otimes COULT = SLO Courses Imbolances C = 1 V/V$	1000v peak	1000 v peak	1000v peak
CMR (\bigcirc 00Hz, 5K52 Source Imbalance, G = 1 V/V	115 dP	115dB	115dP(C=1 to 100)
Between Input and Output, min	f DdB	60dB	60dP(C=1 to 100)
Between inputs & Shield	OUUD	ooub	000B(G=1 10 100)
Output (50k32 Load)	+21/	+21/	1101
Rated Output, min	0.2%@4V p-p	0.2%@4V p-p	±10V
Linearity	0.2% w + v p p	0.2% etv p-p	±0.5%@20V p-p
Output Impedance	1.5K56	1.5836	1.5K32
Frequency Response	21.11-	41-11-	21.11
Small Signal (-3dB)	2612	4882	ZKHZ
Full Power, 3% THD	200Hz	200Hz	200Hz
Settling Time to $100\mu V$ after Applying			
Max Diff. Input Voltage	200ms	200ms	200ms
Power Supply' Range			
Rated Specification	(+12 to +28)VDC	(+12 to +28)VDC	+15VDC
Operating	(+9 to +28)VDC	(+9 to +28)VDC	(+12 to +18)VDC
Current, Quiescent @ +15 VDC	15mA	15mA	55mA
Temperature Range	0 to $+70^{\circ}$ C	0 to $+70^{\circ}$ C	0 to +70°C
Package Outline	H-1	H-1	H-3
Case Dimensions	3.5" x 2.5" x 1.25"	3.5" x 2.5" x 1.25"	3.5" x 2.5" x 1.25"
Price			
1-9	\$109	\$109	\$125
10-24	\$92	\$92	\$99

(1)5k Ω in any lead or combination of input leads and shield. (2)Protected for Power Supply Reversal





GENERAL DESCRIPTION

Comparators in this group are specialized operational amplifiers with differential inputs and two bi-stable states. Used to digitize relative amplitude information, these comparators become the key element in the analog-to-digital conversion process. They are useful as threshold level detectors for A/D converters, voltage to frequency converters, pulse-width modulators and a wide variety of square wave and pulse generators. Available with either FET or bipolar input stage, they have been optimized for fast switching and stable threshold characteristics.

MODEL 350 A/B/C: FET COMPARATOR

Model 350 is a comparator module with high impedance with FET inputs, excellent "trip point" stability, fast response and logic compatible output. Operating as an open loop amplifier with bi-stable output stages, model 350 switching and offset parameters have been optimized for use in DC to 100kHz comparator circuits including level detectors, pulse-width modulators and fast reset pulse circuits. Typical specifications include 20V/400 μ V sensitivity at 1.5k Ω load, CMR of 60dB at 10V and two output ratings; ±10V at ±7mA (500ns switch time) or 0 to 5 volt swing at 15mA (100ns switch time) when its output limit pin is connected for digital logic compatibility. There are three drift options available: 75 μ V/°C (A), 40 μ V/°C (B), and 25 μ V/°C (C).

MODEL AD351 J/K/S

Model AD351 is a high performance monolithic comparator which includes additional front end circuitry, usually added externally with other IC designs, to achieve low bias and offset currents with high input impedance. Although its speed is modestly reduced by incorporating these user conveniences, AD351 fulfills the need for a high speed comparator for a wide range of applications including zero-crossing detectors, threshold detectors and window comparators. Typical specifications include 84dB gain, 250nA bias, CMR of 70dB at $\pm 10V$ and 1 to 7 volt output swing (400ns switch time) with $10k\Omega$ output impedance.

	F	ET Compa 350	rator	Monolithic Comparator 351			
Model	A	В	С	J	к	S	
Gain, V/V, min	50,0)00@1.5kS	2 load	15,000			
Rated Output Voltage Levels, min	$\pm 10V@7mA$ or $\pm 5V@15mA$, $0V@20mA^1$			+71	/ @ no loa +1V@2mA	d to	
Input Bias Current, max Avg. vs. Temp Input Offset Voltage Initial, 25°C, (adj. to zero), max vs. Temp, max	50pA 5nA 75	30pA 3nA ±2mV 40	$\frac{30 \text{pA}}{3 \text{nA}^2}$	20	250nA ~4nA/°C ±6mV 5	10µV/°C	
Input Impedance Differential Common Mode Input Voltage Range Safe Differential Voltage Common Mode Rejection @ ±10V Common Mode Voltage, min	1	$ \frac{1}{10^{11} \Omega / 3.5} \\ \frac{1}{10^{11} \Omega / 3.5} \\ \frac{1}{30V} \\ \frac{1}{60dB} \\ \pm 10V $	pF pF	70dB	$\frac{10M \Omega//4pl}{10M \Omega//4pl}$ $\frac{\pm 30V}{\min (5V c}$ $\frac{\pm 10V}{2}$	F F Putput)	
Response Time Switching (0 to 5V) Output Delay		100ns 5μs ³		2501	400ns ns (2.5V ou	itput)	
Power Supply Positive Voltage (VDC) Negative Voltage (VDC) Temperature Range	+(15 -(15	to 16)V@ to 16)V@ 25 to +85	93.5mA 3.5mA °C	+(7 -1 0 to +70°C	to 18)V@2 8V max@0.5 0 to +70°C	.5mA mA 55 to +125°C	
Package Outline Case Dimensions	1.5'	F-1 ' x 1.5" >	0.4"	TO-100 -			
Price 1-9 10-24	\$40 \$38	\$50 \$48	\$70 \$67	\$11.70 \$11.70	\$18 \$18	\$24 \$24	

(1)+5V, 0V reduced swing using limit connection of 350.
(2)Total drift -25 to +85°C.

(3)Input overdrive of 10mV.

OPEN LOOP PERFORMANCE CHARACTERISTICS GENERAL PURPOSE-MODERATE PERFORMANCE

MODELS 118, 119-----







GENERAL PURPOSE FET LOW BIAS, HIGH Z in



MODEL 146 AD503, AD511, AD540J-----



WIDE BANDWIDTH-FAST SETTLING MODELS 44, 45

MODEL 48 _____ MODEL 46 _____ MODEL 50







LOW VOLTAGE DRIFT-CHOPPER STABILIZED









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LOW VOLTAGE DRIFT-DIFFERENTIAL INPUT, HIGH CMRR







ELECTROMETER- ULTRA LOW BIAS CURRENT







HIGH OUTPUT VOLTAGE, CURRENT

MODEL 171







INSTRUMENTATION







ISOLATION



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CONVERTER PRODUCTS

HOW CONVERTER PRODUCTS ARE CLASSIFIED

The converter products in this catalog are divided into four major classes:

1. *Digital-to-Analog Converters* in which the analog output voltage or current is generated in accordance with a digital input data word. For convenience in selection, d/a converters are subdivided into the following categories:

- Low Cost, General Purpose
- High Performance, General Purpose
- Fast, Display, very high speed fixed reference
- converters, of the types most frequently used for spot position control in CRT displays, and for construction of very fast A/D converters.
- High Resolution, converters with 16 bit resolution, having linearity and stability appropriate for true 16 bit performance.
- Multiplying, D/A converters designed for AC or varying DC reference, rather than for fixed internal or external reference.
- Military Grade, converters specifically designed for operation in the military environment.

In addition, most DAC's are available with either current output – at very high speed – or voltage output, with the added delay of an internal operational amplifier. Voltageoutput DAC's are the most convenient to use and, with the exception of those designed specifically for high speed, will serve in all but those applications calling for μ s and sub- μ s settling times. Current-output DAC's are used in applications where high speed is more essential than stiff voltage output, such as in circuits with comparators (e.g., A/D converters), or where fast amplification is to be provided externally (e.g., CRT deflection amplifiers).

2. Analog-to-Digital Converters in which a digital output is generated that is proportional to the value of the analog input signal. A/D converters are subdivided into the following categories:

- Low Cost, General Purpose
- High Performance, General Purpose
- Dual Slope Converters, particularly well suited for applications where the input signal contains significant power line noise
 - Fast Converters, with a total conversion time of 3.5μ s or less
- High Resolution Converters, offering true state-of-the-art
- performance in an A/D converter with 16 bit resolution and accuracy
- Low Power Converters, intended specifically for remote or
- portable operation from batteries

Three analog-to-digital conversion techniques are represented in Analog Devices' A/D converters. In general, the countercomparator or staircase technique permits the building of a very inexpensive converter; the dual slope integrating approach offers excellent rejection of power line noise; and the successive approximation technique is the best choice where moderate to high speed is required.

3. *Multiplexers*, which are high speed analog switches that provide the capability of sharing a single D/A or A/D converter among a number of analog input or output channels.

4. Sample and Hold Amplifiers which acquire and track a signal that may be varying with time and, upon command, hold the value as of a given time constant so that it can be processed accurately by following circuits (usually A/D converters). Several types are available, which have primary features ranging from low cost to high speed, to very high accuracy.

Other devices frequently used as accessories in conversion subsystems may be found in other sections of this product guide. These include power supplies, isolation amplifiers, instrumentation amplifiers, analog multipliers, and operational amplifiers for buffer or signal conditioning service. μ DAC IC quad and quint switches and thin film resistor networks may be used for construction of precision D/A and A/D converters.

HOW TO SELECT CONVERTERS

The very large number of converter products available in the marketplace can overwhelm even an experienced engineer faced with the problem of selecting a device for a . given application. Interpretation of the specifications adds another dimension to the task, which is further complicated by the virtual absence of standardized specification definitions among the manufacturers.

Only two basic factors hold the key to selecting the right device:

A. A complete definition of the design objectives. Factors such as signal levels, accuracy required, throughput rate, a detailed knowledge of the signal and control interface, environmental conditions and several others must be well defined before selection can be effectively undertaken.

B. A firm understanding of what the manufacturer means by his set of specifications. It should not be assumed that any two manufacturers mean the same thing when they publish identical numbers defining a given parameter. In most cases, the manufacturer has honestly attempted to provide accurate information about his product. That information must be interpreted, however, in terms meaningful to the user's requirements, and this requires a knowledge of how the terms are defined.

Application Checklist

The designer will generally require specific information in the following categories, before proceeding to the selection process:

A. Accurate description of input and output

1. analog signal range and source or load impedance

2. digital code needed – binary, offset binary, 2's complement, BCD, etc.

3. logic level system, i.e., TTL/DTL compatible

B. What is the needed data throughput rate?

C. What are the control interface details?

D. What does the system error budget allow for the converter?

E. What are environmental conditions – temperature range, time, supply voltage – over which the converter should operate to the desired accuracy?

Considerations For D/A Converters

A designer faced with the need to select a d/a converter for a specific application should usually give consideration to each of the following application details.

- A. What resolution is needed? How many bits (8, 10, 12 or other) make up the data word that will be controlling the DAC? Must the DAC be monotonic?
- B. What logic levels and logic codes can be provided by the equipment that will operate the DAC? The most popular logic system is TTL, and the most frequently used codes are binary, offset binary, two's complement, binary-coded decimal, and their complements.
- C. What kind of output signal from the DAC is needed for the system, a current or a voltage? What is the desired full scale range?
- D. What are the speed requirements? What is likely to be the shortest time between data changes going into the DAC? After a change in the digital input data, how long can the system wait for the output signal of the DAC to settle to the desired accuracy?
- E. Over how wide a temperature range (at the module) must the converter operate? Over how much of this range must the converter perform essentially within its specifications without readjustment?

F. How stable are the terminal voltages of the power supplies that will be used for powering the DAC? Is the power supply sensitivity specification adequate to hold errors from this source to reasonable limits?

These considerations are typical of those involved in the application of most converters.

Considerations For A/D Converters

The process of selecting an A/D converter is very similar to that involved in the selection of D/A converters. The following considerations are typical.

- A. What is the analog input voltage range, and to what resolution must the signal be measured?
- B. What is the requirement for linearity error (or relative accuracy error)?
- C. To what extent must the various sources of error be minimized as environmental temperature changes?
- D. How much time can be allowed in the system for each complete conversion?
- E. How stable is the system power supply? What errors will result from power supply terminal voltage variations of this order?
- F. Is monotonicity important to this application, or can the system tolerate a few missed codes (out of 4096 total true codes in a 12 bit ADC, for instance). Please note the discussion of monotonicity in the section on Definitions of Specifications.
- G. What is the character of the input signal? Is it noisy, sampled, filtered, rapidly-varying, slowly-varying? What kind of pre-processing is to be (or can be) done that will affect the choice (and cost) of the converter?

Considerations For Multiplexers And Sample-And-Holds When a sampled data system is to be assembled, in which we will time-share one A/D converter among many input channels by using a multiplexer and a sample and hold, it is important to consider the impact of these accessory devices on the system performance.

Multiplexers

- A. How many input channels are needed?
- B. Is each channel single-ended or differential?
- C. What kind of channel address selection code is used?
- D. When switching from one channel to another, how much time is needed for settling to the desired accuracy?
- E. What error is produced by the leakage current passing through the source resistance?

- F. If the signals are AC, how much error is produced by crosstalk between channels?
- G. Is there any danger of damage to active signal sources when power is turned off? MOSFET multiplexers are inherently "safe," since the switches open when power is removed. J-FET multiplexers usually close when power is removed, making it possible to interconnect, and therefore damage, active signal sources. (The MPX-8A uses MOSFETS as switches.)
- H. What will be the dynamic range of signals feeding into the multiplexer?
- I. Is it desirable to be completely flexible regarding channel switching rate – even to the point of allowing the system to be stopped on one channel, for test and calibration purposes?
- J. What will be the multiplexer transfer error (error produced by voltage division of the "On" resistance of a channel feeding into the input resistance of the following sample and hold)?

Sample-and-Hold Amplifiers

- A. What is the nonlinearity?
- B. Considering the slewing rate of the signal, or the desired channel switching rate of the preceding multiplexer, how much time is available for acquiring the signal in the sample and hold?
- C. What is the error component produced by input bias current passing through the source resistance (source resistance includes signal source resistance and the maximum "On" resistance of the multiplexer switch)?
- D. What is the offset drift error (the offset temperature coefficient multiplied by the anticipated deviation of temperature)?
- E. What is the offset error due to variation in the terminal voltage of the power supply we expect to provide?

In addition to the above error sources, there exists an uncertainty due to the aperture delay jitter. That is, in a sample and hold with a given aperture time (e.g. 40ns) there usually exists an aperture time uncertainty (or jitter) of perhaps 5ns peak. The effect of aperture time is considered to be a correctable factor, since it is comparable to a delay in the sample-to-hold switching operation. The jitter cannot be compensated, however, and a 5ns jitter applied to a signal slewing at, say, $1V/\mu$ s produces an uncertainty of 5mV. Since this uncertainty is directly proportional to signal slewing rate, it can be anticipated by thorough knowledge of the nature of the input signals.

INITIAL SELECTION CRITERIA FOR SYSTEM COMPONENTS

It seems that the most economical process for selection of appropriate components to meet a system requirement will probably be a method of successive approximations: make an arbitrary choice, and run through a complete error analysis to check the adequacy. Where the error analysis demonstrates either performance far in excess of need (therefore possibly unnecessarily costly) or inadequate accuracy or stability, make a new choice and run through the error analysis once again.

In practice, the usual engineering criterion appears to work: for a multi-component system, choose each component to be roughly ten times better than desired in the final system. Thus, for a system of the 0.1% desired maximum error class, use a 0.01% converter (12 bits) with compatible multiplexer and sample and hold. As you will see in the typical system error analysis that follows, this approach leads to quite acceptable system errors.

THE SELECTION PROCESS

To best illustrate the complete selection process for a converter product, we have created a hypothetical situation. With this approach, one can more easily understand specification usage and applicability to a given problem.

The Problem

A computer data acquisition system is to be built to process data from a number of strain gages. Signal conditioning hardware, to be purchased with the gages, delivers $\pm 10VFS$ signals from 10 ohm sources. Signal channels must be sequentially scanned in no more than 50μ s per channel. Maximum allowable error of the system is approximately 0.1% of FS. System logic is to be TTL, and hardware may work in either binary or two's complement code. Parallel data readout will be used.

Probable temperature range in the equipment cabinets (including equipment temperature rise) is $+25^{\circ}$ C to $+55^{\circ}$ C. Sufficient ± 15 V and +5V power is available, but the ± 15 V has regulation of only 150mV. What converter products should be chosen?

First Approximation

Since desired accuracy is about 0.1% for the system, we first choose an A/D converter with 12-bit resolution (0.01% = ½LSB). Reviewing the available ADC's, we find the ADC-12QM to be a possible choice. Since it is packaged in a small 2" x 4" x 0.4" module, it can be conveniently incorporated in a compact subsystem.

The ADC-12QM completes a conversion in $25\mu s$ and, since it is felt that a sample and hold is necessary, the

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SHA-1A module is chosen because it is compatible and it has settling time of 5μ s. Thus, the combination of ADC-12QM and SHA-1A will operate in 30μ s safely within our limit of 50μ s per channel for the system.

Since multiplexer scanning will be sequential, we won't be concerned about settling time when channels are switched. The multiplexer can be switched to the next address as soon as the SHA goes into "hold" on data from the current address. Thus it has a quite adequate 30μ s to settle before a measurement is called for. For convenience, we'll use the MPX-8A as the multiplexer; the small module package fits into the packaging concept, and the built-in complete binary address decoding makes it very easy to work with.

Error Analysis

It's clear that the MPX-8A, the SHA-1A and the ADC-12QM generally meet the problem's requirements for speed and resolution. Now we must look further into the details of errors, to determine if the worst case situation is within the allowable 0.1% system error.

Error Analysis of MPX-8A Multiplexer

MPX-8A multiplexer, being a MOSFET circuit, is not subject to voltage offset errors. Errors here will be due to two factors:

1. Leakage current into the "ON" channel across the source impedance.

Leakage current @ 25° C = 10nA Source impedance = 10 ohms Error voltage = 10 x $10^{-8} = 10^{-7}$ V or 0.01ppm for a 10VFS signal (certainly can be neglected)

2. Transfer error due to voltage division across MOSFET "ON" resistance and input impedance of SHA-1A.

```
ON resistance = 1000 ohms max
SHA-1A R<sub>IN</sub> = 10<sup>12</sup> ohms
\frac{\text{E}\text{OUT}}{\text{E}\text{IN}} = \frac{10^{12}}{10^{12} + 10^3} = \frac{10^{12}}{10^3(10^9 + 1)} = \frac{10^9}{10^9 + 1}
```

Transfer error ≪1ppm

Error Analysis of SHA-1A Sample and Hold 1. Total throughput nonlinearity is 2mV over 20V range, or 0.01%.

2. Gain error of -0.05% max and other gain errors in the system (if small) may be compensated for overall when calibrating the system by setting of the Gain of ADC; not considered in this system's error budget.

3. Input bias current of 1nA (typical) causes an offset error

voltage in the source resistance.

Source resistance equals sum of "ON" resistance of MPX-8A and signal source resistance: 1010 ohms total Offset error = $1.01 \times 10^3 \times 10^{-9} = 1.01 \times 10^{-6} \text{V}$ out of 10VFS, or 0.1ppm.

- 4. Offset vs temp = $25\mu V/^{\circ}C$. Our housing temperature may change by $30^{\circ}C$. Offset error = $25\mu V \ge 30 = 750\mu V$ out of 10V, or 0.0075%.
- 5. Offset vs Supply = $100\mu V/\%$.

Supply may move 150mV out of 15V, or 1%. Offset error is therefore 100µV out of 10V, 0.001%.

By an analysis similar to the above, we would normally also prepare a system timing diagram, and assign operating time and settling time allowances. However, the components selected for this example allow several times more settling time than needed for 0.01% operation, consequently we can overlook the need for a formal timing analysis to determine whether settling times are adequate.

Error Analysis of ADC-12QM A/D Converter

1. Linearity error (relative accuracy) ½ LSB or 0.01%

2. Quantizing uncertainty; ½LSB or 0.01%. This is a resolution limitation, not considered in the error budget.

3. Temperature errors:

a) Gain Tempco 5ppm/°C for our 30°C possible shift;
150ppm total
Gain error: 150ppm or 0.015%
b) Zero Tempco 5ppm/°C
Zero error: 0.015%

 Power supply sensitivity error Sens = 0.002%/%. Power supply may move 1%, therefore PS error = 0.002%

In conclusion, the following is a summary of the significant sources of error in the system:

SHA linearity error	0.01%
SHA offset vs temp error	0.0075%
SHA supply offset error	0.001%
ADC linearity error	0.01%
ADC gain tempco error	0.015%
ADC zero tempco error	0.015%
ADC supply offset error	0.002%
Worst case sum of all errors:	$\approx 0.06\%$
a a a	

Square root of sum of squares: $\approx 0.03\%$ Since these values are certainly reasonable for a system with specification error of 0.1%, we should be satisfied that we have made reasonable choices in components.

DEFINITION OF SPECIFICATIONS

Absolute Accuracy

When the full scale point is adjusted on a converter, it will be set with respect to a reference voltage which, in turn, is referenced to the NBS voltage standard. The absolute accuracy of the converter is then the tolerance of the full scale set point referenced to the NBS standard.

Acquisition Time

The acquisition time of a sample and hold circuit is the time it takes to acquire the input signal to the given accuracy. Specifications on acquisition time given in Analog Devices' data sheets include the settling time of the output amplifier. Some manufacturers do not include settling time of the output amplifier when specifying acquisition time.

Aperture Time

This is the time it takes in a sample and hold circuit, for the switch to open after the control command has been given. In a good SHA, this should not exceed 50ns delay, including 10ns uncertainty.

Common-Mode Range

Common-mode rejection usually varies with the magnitude of the common-mode plus the differential (or "normal" mode) voltage applied to an amplifier. Common-mode range is that range of total input voltage over which optimum common-mode rejection is maintained. In good operational amplifiers, the common mode range is usually of the order of $\pm 10V$.

Common Mode Rejection (CMR)

The ability of an amplifier to reject the effect of voltage applied to both input terminals simultaneously. Usually expressed as the log of a "common-mode rejection ratio," i.e. 1,000,000:1 (CMRR) or 120dB (CMR). A CMRR of 1,000,000 to 1 means that a 1V common-mode voltage passes through the amplifier as though it were a differential signal of one microvolt at the input.

Common-Mode Voltage

An undesirable signal picked up in a transmission line by both wires making up the circuit, with reference to an arbitrary "ground." Amplifiers differ in their ability to amplify a desired signal accurately in the presence of a common-mode voltage.

Conversion Time

The time required for a complete measurement by an analog-to-digital converter is called conversion time. In successive approximations converters, conversion times are available between 1.0μ s for the 8 bit version of the ADC1103 and 400μ sec (for the ADC-16Q). The most popular general

purpose A/D converters, like the ADC-12QM, have conversion time of about $25 \,\mu$ s.

Crosstalk

Leakage of signals between circuits or channels of a multichannel system or device, such as a multiplexer. Crosstalk is usually determined by the impedance parameters of the physical circuit, and actual values are frequency-dependent.

Deglitcher

When a D/A increases or decreases the input code by small changes, it passes through what is known as major and minor transitions. The major transition is at half-scale, when the D/A switches around the MSB, and all switches change state, i.e., 01111111 to 10000000. If the switches are faster to switch off than on, this means that, for a short time, the D/A will give a zero output and then return to the required 1 LSB above the previous reading. This large transient spike is commonly known as a "glitch," and hence, a "deglitcher" is a device which removes these glitches. It normally consists of a hold-sample circuit which holds the output constant until the switches reach equilibrium.



Differential Linearity

In a digital converter, differential linearity describes the variation in size of adjacent steps over the full range of the circuit, or the closeness of each individual step to the ideal 1LSB. A differential nonlinearity of more than 1LSB may result in a non-monotonic D/A converter or missed codes in an A/D converter.

Droop Rate

When a sample-and-hold circuit using a capacitor for storage is in hold, it will not hold the information forever; droop rate is the rate at which the output voltage changes and, hence, loses the information. In practice, when using a SHA ahead of an ADC, the SHA should not droop more than 0.1 LSB during the conversion time of the ADC.

Dual-Slope Converter

An integrating analog-to-digital converter in which the unknown signal is converted to a proportional time interval, which is then measured digitally. This is done by integrating the unknown for a predetermined time. Then a reference input is switched to the integrator, and integrates "down"
from the level determined by the unknown until a "zero" level is reached. The time for the second integration process is proportional to the average of the unknown signal level over the predetermined integrating period. A digital time interval meter (i.e., counter) is generally used as the output indicator.



Four-Quadrant

In a multiplying DAC, "four-quadrant" refers to the fact that both the reference signal and the number represented by the input may be bipolar. A four-quadrant multiplier is expected to obey multiplication rules for algebraic sign.

Feedthrough

A term referring to that characteristic of a circuit or device manifested by undesirable signal leakage around switches or other devices that are supposed to be turned off or provide isolation.

Gain Adjustment

The "gain" of a converter is that analog scale factor setting that provides the nominal conversion relationship, e.g. 10V full scale.

Hold-to-Sample Transient

In a sample-and-hold amplifier, a switching transient usually occurs when switching from "HOLD" to "SAMPLE" modes. Such transients effectively slow the process of settling-in on the desired signal.

Least Significant Bit (LSB)

In a system in which a numerical magnitude is represented by a series of binary (i.e., two-valued) digits, the "least significant bit" is that digit (or "bit") that carries the smallest value or weight. For example, in the natural binary number 1101 (decimal 13, or $2^3 + 2^2 + 0 + 1$), the rightmost "1" is the LSB.

Linearity

The conventional definition for nonlinearity of a device is the deviation from a "best straight line." This means that to determine whether a device meets the stated linearity specification, the 'shape' of the nonlinearity and the magnitude have to be known so that the end points (e.g., the zero and full scale points for a unipolar converter) can be offset by a "best" amount to minimize linearity error.



As this definition is totally impractical for *users* of converters, we define nonlinearity as follows: the nonlinearity is the deviation from a straight line drawn between the end points as calibrated by a normal adjustment procedure. As shown in the figure, it is more conservative than the "best straight line" definition, since if all errors are of the same polarity, they may only be half as great.



The user of the converter now needs only to set the two end points to measure the linearity. The normal limit that is used for a good converter is $\pm \frac{1}{2}$ LSB (least significant bit). This then means that the sum of positive errors or the sum of the negative errors of the individual bits must not exceed $\frac{1}{2}$ LSB, which means further that, the errors of the bits themselves, must be considerably less than $\frac{1}{2}$ LSB.

For the higher resolution converters (14 and 16 bits), Analog computes and plots the nonlinearity for every code, to ensure that the converter meets our specification before shipment.

Line Regulation

Load Regulation

Stability parameters of a power supply: the variation of output voltage as a fraction of changes in input line voltage

or load current. These are among the most important specifications of a regulated supply. Regulation is often specified in terms of change in output (in either % or volts) per incremental change in line voltage or load current (in either % or actual change).

Monotonic

A monotonic D/A or A/D converter never has its output decrease in response to an increasing input stimulus (or vice versa). In high-speed converters, it is not especially hard to produce a monotonic design over limited temperature ranges. In order to be monotonic over very wide temperature ranges, error components of DAC switches and resistor networks must track each other very closely with temperature change. In ADC's, the counterpart of non-monotonic behavior is the "missed code," which is produced when a transition from one quantum of the analog range to the adjacent one does not result in the adjacent digital code, but in one removed by one or more counts. Monotonic behavior in high-resolution conversion over wide temperature ranges is not easy to accomplish at the present state of the art; consequently, converters like the ADC-QM, which are monotonic from 0° C to $+70^{\circ}$ C, at reasonable cost, are not commonly seen in the industry. Integrating converters, such as the ADC-I, are inherently monotonic; A/D converters of this class are also inherently slow (usually more than 35ms for a full conversion).

Most Significant Bit (MSB)

In a system in which a numerical magnitude is represented by a series of binary (i.e., two-valued) digits, the "most significant bit" is that digit (or "bit") that carries the largest value or weight. For example, in the natural binary number 1101 (decimal 13, or $2^3 + 2^2 + 0 + 1$), the leftmost "1" is the MSB, with a weight of 2^{n-1} , or 8.

Multiplying DAC

A multiplying DAC differs from the conventional fixedreference DAC in being designed to operate with varying (or AC) reference signals. The output signal of such a DAC is proportional to the product of the reference voltage and the fractional equivalent of the digital input number.

Noise, Peak

Peak: The peak noise output of a DAC being an analog signal, can be an important consideration, especially in high resolution DACs, such as the DAC-14QM and DAC-16QM. The resolution is not confidently assignable when the peak noise exceeds the LSB value for a reasonable bandwidth. For an ADC, input circuit noise may impart statistical properties to the input numbers and require additional processing for successful interpretation.

Noise, RMS

RMS: For Gaussian noise, the RMS noise should be oneseventh of the specified peak-to-peak noise, for less than 0.1% probability of encountering greater noise peaks. Both specs should be looked at very carefully, as large spikes could be present on the output from a chopper-stabilized amplifier (or coupled into the system). These spikes will contribute very little to driving the RMS noise out of spec, but could nevertheless be of considerable amplitude. If such a DAC is used in a display system, the noise will cause distortion of the pattern and hence, loss of useful resolution.

Offset

For almost all bipolar converters (e.g., ± 10 volts output) instead of actually generating negative currents to correspond to negative numbers, a unipolar DAC is used, and the output is offset by half full scale (1MSB). For best results, this offset voltage or current is derived from the same reference supply that determines the gain of the converter.

This makes the zero point of the converter independent of thermal drift of the reference. This is because the ½ scale offset completely cancels the weight of the MSB at zero, independently of the amplitude of both.

TRANSFER CHARACTERISTICS



"ON" Resistance

"ON" resistance of a device such as a FET, when used as a switch performing a function (such as multiplexing), refers to the ohmic resistance while turned on. For multiplexer service, a few hundred ohms or less will usually provide adequate accuracy. For other switching service, such as in a DAC, values of 10 ohms or less are desirable.

Power Supply Sensitivity

The sensitivity of a converter to changes in the power supplies is normally expressed in terms of percentage change in analog value (D/A output, A/D input) for a one percent change in power supply; e.g. 0.05%/% change in reading per volt change in power supply. For all good converters, the fractional change in reading should not be more than the % equivalent of ±½ LSB at full scale for a 3% change in power supply.

When power supply voltage changes affect conversion accuracy excessively, the trouble can usually be traced to a marginal "constant-current" circuit design for the reference zener diode.

Quantizing Uncertainty (or "Error")

The analog continuum is partitioned into 2^n discrete ranges for n-bit conversion. All analog values within a given range are represented by the same digital code, usually assigned to the nominal midrange value. There is, therefore, an inherent quantization uncertainty of $\pm \frac{1}{2}$ LSB, in addition to the actual conversion errors.

Relative Accuracy

Relative accuracy (error) is the difference between a voltage other than full scale, and its nominal value as a fraction of actual full scale (rather than an arbitrary standard). This error will be dependent on the linearity of the converter.

Settling Time

This is the time it takes for a DAC to settle for a full scale change, usually to within $\pm \frac{1}{2}$ LSB. For example, for the DAC-12QS, the settling time is specified as 5 μ s max, which is the time for a 0 to +10 volt change and settling to $\leq \pm 0.012\%$ ($\frac{1}{2}$ LSB of 12 bits). Another very important settling time characteristic is the settling time of a single LSB change, for example, in digital sweep generation.

Slew Rate (or Slewing Rate)

Slew rate in an operational amplifier is a limitation in the rate of change of output voltage, usually imposed by some basic circuit consideration, such as limited current to charge a capacitor. Amplifiers with slew rate of a few volts/ μ s are common, and moderate in cost. Slew rates greater than about 75 volts/ μ s are usually seen only in more sophisticated (and expensive) devices. The output slewing speed of a modern D/A converter is usually limited by the slew rate of the amplifier used at its output.

Stability

Stability of a converter usually applies to the insensitivity of its characteristics with time, temperature, etc. All measurements of stability are difficult and time consuming, but stability vs. temperature is sufficiently critical in most applications to warrant universal inclusion in tables of specifications. (See "Temperature Coefficient.")

Staircase

A waveform having the appearance of a staircase.



A very simple A/D converter, of low cost, can be built utilizing a staircase from a DAC, (generated by a digital count at its input) for comparison with the unknown input. The ADC-8S is a converter of this type.

Successive Approximations

Successive approximations is a high speed method of comparing an unknown against a group of weighted references. The operation of a successive approximations A/D converter is generally similar to the orderly weighing of an unknown quantity on a precision chemical balance, using a set of weights such as: 1 gram, 1/2 gram, 1/4 gram, 1/8 gram, 1/16 gram, etc.

Switching Time

In a DAC, the switching time is the time it takes for the switch to change from one state to the other ("delay time" plus "rise time" from 10%-90%), but does not include settling time, e.g. to $< \pm \frac{1}{2}$ LSB.

Temperature Coefficient

Gain: The gain of all converters will change with temperature due to two main causes.

a) The reference zener itself will have a temperature coefficient. A good zener will have a TC of $< 5 \text{ppm/}^{\circ}\text{C}$. b) The reference circuitry and switches will add about another $3 \text{ppm/}^{\circ}\text{C}$ max in very good converters. The total gain change with temperature will then be specified as x parts per million change per $^{\circ}\text{C}$.

Unipolar Zero: The temperature stability of a unipolar DAC is almost entirely due to the voltage zero stability of the output amplifier. As the output amplifiers are normally current-to-voltage converters, they are always running at a voltage gain not too different from unity, hence, the unipolar DAC zero T.C. can be expressed in $\mu V/^{\circ}C$ and will be independent of gain setting, i.e., 0-5V or 0-10V.

For an ADC, similar arguments apply, and its T.C. is dependent only on the voltage zero stability of the input buffer and comparator and, again, is usually expressed in $\mu V/^{\circ}C$ (of input).

Bipolar Offset: The temperature coefficient of the minus full scale point or offset of a bipolar converter is dependent on three variables:

1) The T.C. of the zener reference diode

2) The voltage zero stability of the output amplifier or input buffer and comparator

3) The tracking capability of the bipolar-offset resistors and the gain resistors.

The temperature coefficient of the minus full scale point will be specified in ppm/°C on the above specifications, since that is the normal "all-DAC-switches-*off*" point.

Transfer Accuracy

Refers to the loss of accuracy that results from the insertion of a less-than-perfect signal handling circuit into a measurement circuit.

Zero

The zero of a 0-10V DAC is set to zero volts for an all-0's input code. For an ADC, the first transition is offset by one-half LSB so that all subsequent transitions occur midway between the nominal code values. That is, only ½LSB of analog input is required before the LSB switches on.



HOW TO ADJUST ZERO AND GAIN OF CONVERTERS

Proper adjustment of zero and gain in DAC's and ADC's is a procedure that requires great care, and the use of extremely sensitive reference instruments. The voltmeter used to read the output of a DAC, or the voltage source used as a driving signal for the ADC, must be capable of stable and clear resolution of 1/10 LSB at both ends of the range of the converter; e.g., at zero and full scale.

Converter	Converter Range				
Resolution	20V	10V	5V		
8 bits	39.06mV	19.53mV	9.77mV		
10 bits	9.77mV	4.88mV	2.44mV		
12 bits	2.44mV	1.22mV	610µV		
14 bits	610µV	305µV	$153\mu V$		
16 bits	153µV	76µV	38µV		

Table 1. Voltage Equivalent of 1/2LSB for

Various Resolutions and Voltage Ranges

All DAC's and successive approximation ADC's manufactured by Analog Devices are provided with Zero and Gain adjustments which are completely independent of each other, as long as the adjustment of Zero is attempted only when the actual conversion circuit is producing Zero, and as long as the Zero (or Offset) adjustment is accurately completed before proceeding to adjustment of Gain (at full scale -1LSB). Of course, it is possible to make Zero and Gain adjustments in reverse order and at other points on the transfer function — but it must be expected that the adjustments will no longer be independent, and the procedure will require a series of successive approximations.

Adjustment Process

Particularly for bipolar converters, fast and successful adjustment requires knowledge of the technique used in the circuit to convert the inherently unipolar DAC or ADC for bipolar operation.

1. Sign & Magnitude Codes are generally obtained by use of a unipolar converter with separate means of reversing polarity. The Zero adjustment is always made by calling for a zero from the converter. (Logic zero into a DAC produces zero volts output, or zero volts into an ADC produces data zero output.) 2. Bipolar binary converters utilizing offset binary or two's complement coding usually employ analog offsetting to convert a unipolar design into bipolar. For instance, a 0 to +10V DAC may have its output amplifier offset by -5V, resulting in an output of -5 volts corresponding to 000000 input and +5 volts (minus 1 LSB) corresponding to a 111111 input. Such a converter should have its "Zero" adjusted at -5V.

An alternate explanation is as follows: converter Zero controls should always be set at the "All Bits Off" condition, and then Gain should be set at the "All Bits On" condition.

Adjustment For DAC's

ZERO: set input code so that all bits are "off", then adjust pot until output signal is within 1/10LSB of proper reading, or zero.

GAIN: set input code so that all bits are "on", then adjust pot until output signal reads within 1/10LSB of *Full Scale less 1LSB*.

Adjustment For ADC's

ZERO: set input voltage precisely at ½LSB above the "all bits off" specified input. Zero control should be adjusted so that the converter just switches in its LSB.

GAIN: set input voltage precisely at ½LSB less than "all bits on" input. Note that this is 1½LSB's less than the nominal full scale value: i.e., all 1's value of a zero to +10V 12-bit ADC is actually +9.9976. Gain adjustment should be made with an input ½LSB less, or +9.9962 volts. With input voltage set as described, GAIN control is rotated to the point where the last bit just comes on. For instance, in a 12 bit binary converter, reading of 11111111110 would change to 11111111111.

GENERAL SPECIFICATIONS COMMON TO MOST ANALOG DEVICES CONVERTER PRODUCTS

In order to simplify the presentation of specification information in the converter section of this catalog, a number of specification parameters common to most of the product line were omitted from the details in each table. They are:

1. All logic interfaces are compatible with TTL and DTL except for the model ADC-12QL, which is compatible with CMOS.

2. Positive true is our convention in defining all codes.

3. All products are designed to operate over an ambient temperature range of 0° C to $+70^{\circ}$ C. Certain products are also available in extended temperature versions.

4. All products are designed for storage in temperatures from -55° C to $+125^{\circ}$ C.

5. All converters are designed to have maximum linearity error of $\leq \pm \frac{1}{2}$ LSB @ $+25^{\circ}$ C.

6. All Analog to Digital converters have internal clocks.

7. All Analog to Digital converters provide a status signal and its complement for interface to system controls.

8. All products are designed with very high rejection of variations in the power supply, and errors due to variations of several millivolts in the ± 15 V supplies can almost always be neglected.

Complete details of the performance specifications of Analog Devices products are listed on individual data sheets on each product, available upon request.

CONVERTER PRODUCTS FOR EXTENDED TEMPERATURE SERVICE

Most converter products described in this catalog are intended for operation over the temperature range of 0 to $+70^{\circ}$ C. Performance of these converters does not usually deteriorate abruptly beyond these temperature limits, but rather degrades gradually, and finally may become unpredictable.

Several converters can be supplied in versions capable of stable operation over an extended temperature range. These ET versions are available only in the binary codes (i.e., ET versions of BCD coded units are not available).

The 8 and 10-bit converters are specified over the range of -55° C to $+85^{\circ}$ C. All ET converters are individually tested at high, low, and room temperatures prior to shipment.

The table below shows the maximum TC's to be expected over the full ET operating temperature range. For example, a 12-bit DAC-12QS/ET would have a maximum gain TC of \pm 11ppm/°C from -25°C to 0, \pm 7ppm/°C from 0 to +70°C, and \pm 12ppm/°C from +70°C to +85°C. The most commonly requested and readily available ET converters are shown below. The extended temperature version is ordered by adding /ET to the standard model number.

Model	Price (1-9)	Details on Page
DAC-12QM/ET	\$345	80
DAC-12QS/ET	\$285	80
DAC-10QS/ET	\$255	80
DAC-8QS/ET	\$210	80
ADC-12QM/ET	\$460	92
ADC-10QM/ET	\$420	92
ADC-8QM/ET	\$375	92
ADC-12QU/ET	\$470	92

TEMPERATURE COEFFICIENTS						
	-55° C to 0	-25°C to 0	0 to $+70^{\circ}$ C	$+70^{\circ}$ C to $+85^{\circ}$ C	$+70^{\circ}$ C to $+125^{\circ}$ C	
12 bit Models						
Diff. Linearity		±5ppm/°C	±3ppm/°C	±4.5ppm/°C		
Gain		±11ppm/°C	±7ppm/°C	±12ppm/°C		
Zero (Unipolar)		$\pm 45 \mu V/^{\circ} C$	$\pm 50 \mu V/^{\circ} C$	$\pm 50 \mu V/^{\circ} C$		
Offset (Bipolar)		±6ppm/°C	±5ppm/°C	±6ppm/°C		
10 bit Models						
Diff. Linearity	±15ppm/°C		±3ppm/°C		±12ppm/°C	
Gain	±15ppm/°C		±7ppm/°C		±18ppm/°C	
Zero (Unipolar)	$\pm 45 \mu V/^{\circ} C$		$\pm 50 \mu V/^{\circ} C$		$\pm 50 \mu V/^{\circ} C$	
Offset (Bipolar)	±12ppm/°C		±5ppm/°C		±12ppm/°C	
8 bit Models						
Diff. Linearity	±30ppm/°C		±3ppm/°C		±25ppm/°C	
Gain	±60ppm/°C		±7ppm/°C		±50ppm/°C	
Zero (Unipolar)	$\pm 45 \mu V/^{\circ} C$		$\pm 50 \mu V/^{\circ} C$		$\pm 50 \mu V/^{\circ} C$	
Offset (Bipolar)	±50ppm/°C		±5ppm/°C		±50ppm/°C	

These figures include 20% guard band over engineering test specs.

CAPSULE SELECTION TABLE

DIGITAL-TO-ANALOG CONVERTERS

SPECIFICATIONS (Typical @ +25°C unless otherwise noted)

		_											
Product Classification	Model ¹	Resolution	Linearity Error	Input Code Options ² (TTL/DTL Compatible)	Input Register		Output Options	Settling Time to % of Full Scale	Gain TC ⁴	Power Requirements	Package Size & Style	Price (1-9)	Price (100+)
Low Cost General Purpose	DAC-12QZ DAC-10Z MDA-10Z	12 bits 10 bits 10 bits	±0.0125% ±0.05% ±0.05%	C-B, COB, CBD BIN, OBN	NO	±5\	V,±10V,±2.5V,+5V,+10V -10V,±10V +2mA,±1mA	5μs to 0.01% 5μs to 0.05% 300ns to 0.05%	±30ppm/°C	±15V, +5V ±15V ±15V	2" x 2" x 0.4", C-1	\$ 79 \$ 49 \$ 49	\$47 \$27 \$27
High Performance	DAC-8QS DAC-10QS DAC-12QS	8 bits 10 bits 12 bits	±0.2% ±0.05% ±0.0125%	C-B, COB, CBD	NO	1	±2.5V,±5V,±10V, +5V,+10V	5µs to 0.01%	±7ppm/°C	±15V, +5V	2" x 2" x 0.4", C-1	\$ 140 \$ 170 \$ 190	
General Purpose	DAC-8QM DAC-10QM DAC-12QM	8 bits 10 bits 12 bits	±0.2% ±0.05% ±0.0125%	BIN, OBN, 2SC, BCD	YES	1	±2.5V,±5V,±10V, +5V,+10V	5µs to 0.01%	±7ppm/°C	±15V, +5V	2" x 4" x 0.4", C-3	\$ 170 \$ 210 \$ 230	
Fast, Display	DAC-10DF MDA-8F MDA-10F	10 bits 8 bits 10 bits	±0.05% ±0.2% ±0.05%	OBN, 2SC BIN, OBN	YES NO NO	}	±2.5V,±5V,±10V ±2.3mA,+4.7mA	500ns to 0.05% 40ns to 0.05% 40ns to 0.05%	±50ppm/°C ±25ppm/°C ±25ppm/°C	±15V, +5V ±15V ±15V	4 ¹ / ₂ " x 6", C-8	\$ 495 \$ 220 \$ 240	
High Resolution	DAC-14QG DAC-16QG DAC-14QM DAC-16QM	14 bits 16 bits 14 bits 16 bits	±0.003% ±0.0015% ±0.003% ±0.0015%	BIN, OBN, 2SC BCD, SMB, SMD C-B, COB, CBD	OPTIONAL OPTIONAL NO NO	}	±5V,±10V,+10V ±5V,±10V,+10V, ±1mA,-2mA	250μs to 0.0015%	±7ppm/°C	±15V, +5V	41/2" x 41/4", C-8 2" x 4" x 0.4", C-3	\$ 820 ⁵ \$1170 ⁵ \$ 395 \$ 745	
Multiplying ³	DAC-8M DAC-12M MDA-11MF	8 bits 12 bits 11 bits	±0.2% ±0.02% ±0.03%	BIN, OBN	NO	}	±10V ±2mA,+4mA	10μs to 0.2% 15μs to 0.01% 1.0μs to 0.01%	±25ppm/°C	±15V	2" x 2" x 0.4", C-1 2" x 4" x 0.4", C-3	\$ 195 \$ 295 \$ 150	
Military Grade	MDA-12QD	12 bits	±0.0125%	C-B, COB	NO		-2mA,±1mA	3µs to 0.01%	±15ppm/°C	±15V, +5V	1" x 1½" x 0.4", C-7	\$ 295	

NOTES

1. DAC's whose model numbers begin with MDA have current outputs, allowing the user to select the op amp of his choice. Those beginning with DAC include an internal op amp.

2. Logic Codes: BIN, Binary; C-B, Comp. Binary; OBN, Offset Binary; COB, Comp. Offset Binary; BCD, Binary Coded Decimal; CBD, Comp. BCD; 2SC, Two's Comp.; C2C, Comp. Two's Comp.; SMB, Sign-magnitude Binary; SMD, Sign-magnitude BCD.

3. Reference range of DAC-8M and DAC-12M is $\pm 10V$. Reference range of MDA-11MF is 0 to -10V.

4. Standard temperature range on all converters is 0 to $+70^{\circ}$ C, with storage temperature from -55° C to $+125^{\circ}$ C. Many models are available in an extended operating temperature version at extra cost. The extended operating temperature range is normally -25° C to $+85^{\circ}$ C.

5. Price is for stocked unit, which includes binary coding, input register, 0 to +10V range, 184L output amp, and deglitcher.

LOW COST GENERAL PURPOSE D/A CONVERTERS MDA-10Z, DAC-10Z, DAC-12QZ



GENERAL DESCRIPTION

These D/A converters are characterized primarily by low cost, but this economy has been attained by judicious use of materials, careful engineering, and by high volume manufacturing techniques. Consequently, there is no compromise with quality and reliability, and as a result, these products are excellent values.

MDA-10Z

The MDA-10Z is a fast 10-bit digital-to-current converter intended for use with external amplifiers. It is available with unipolar output or bipolar output, to suit the needs of a broad variety of applications. Fixed output range is provided.

DAC-10Z

The DAC-10Z is a fast 10-bit D/A converter with a built-in I.C. output amplifier. Available in unipolar or bipolar form, the DAC-10Z is an optimum value for applications requiring above average performance at an economy price.

DAC-12QZ

The DAC-12QZ is a general purpose 12-bit D/A converter in which an outstanding value is achieved. The Analog Devices' AD550 μ DAC current switches are used in conjunction with a matched close-tracking resistor network to provide fast 12-bit performance at an economy price. The user chooses one of five available output ranges by jumpering at the module terminals.



BLOCK DIAGRAM

ORDERING GUIDES

MODEL DAC-1	2QZ/ <u>XXX</u>
	BIN
	BCD
DAC-10Z-1	10-bit binary with amplifier, 0V to -10V output voltage.
DAC-10Z-3	10-bit binary with amplifier, 10V to -10V output voltage.
MDA-10Z-25	10-bit binary without amplifier, with 0mA to +2mA output current and $5k\Omega$ nominal (4.85k $\Omega \pm 1\%$) gain resistor.
MDA-10Z-110	10-bit binary without amplifier, -1mA to $+1mA$ output current and $10k\Omega$ nominal (9.70k Ω $\pm 1\%$) gain resistor.

reduced
prices:
MDA-10Z
, DAC-10Z
DAC-12QZ

Model	MDA-10Z	DAC-10Z	DAC-12QZ
Resolution (bits)	10	*	12
Digital Inputs			
Levels (Positive True)	TTL	*	*
Codes			
Unipolar	Binary	*	Complementar
			Binary & BCD
Bipolar	Offset Binary	*	Complementar
			Offset Binary
Output Ranges			
Unipolar	0 to 2mA	0 to -10V	+5V, +10V)
			$\pm 2.5 \mathrm{V}, \pm 5 \mathrm{V}, \rangle$
Bipolar	±1mA	$\pm 10V$	±10V
Settling Time			
(F.S. Step to ½LSB)	300ns	5µs	5µs
Linearity Error @ +25°C	±½LSB	*	*
Stability vs Temperature			
Unipolar			
Gain	30ppm/°C	*	*
Zero	$10 n A/^{\circ} C$	$100\mu V/^{\circ}C$	50μV/°C
Bipolar			
Gain	40ppm/°C	30ppm/°C	25ppm/°C
Offset	$30 n A/^{\circ} C$	$100\mu V/^{\circ}C$	$100\mu V/^{\circ}C$
Power Required	±15V @ 15mA	*	+15 @ 25mA
			-15 @ 30mA
			+5 @ 35mA
Package Style	C-1	*	*
Package Dimensions	2" x 2" x 0.4"	*	*
Price (100+)	\$27.	*	\$47.
(1-9)	\$49.	*	\$79.

*Specifications same as for Model MDA-10Z.

BLOCK DIAGRAM DAC-10Z & MDA-10Z



NOTE: NOT ALL OF THE PINS SHOWN WITH CONNECTIONS TO THEM APPEAR ON EACH MODEL. THE PINS DELETED ON EACH MODEL ARE SHOWN BELOW:

MODEL	DELETED PINS
DAC-10Z-1	PINS 25, 28
DAC-10Z-3	PIN 28
MDA-10Z-25	PIN 25
MDA-10Z-110	NONE

PINS SHOWN AS HAVING NO CONNECTIONS (N.C.) ARE ALSO DELETED. THE OUTPUT OP AMP ONLY APPEARS IN THE DAC-10Z's.

HIGH PERFORMANCE GENERAL PURPOSE D/A CONVERTERS DAC-QM, DAC-QS

GENERAL DESCRIPTION

The DAC-QM and DAC-QS digital-to-analog converters are characterized by high stability and high performance. They use Analog Devices μ DAC[®] monolithic quad current switches and μ DAC[®] monolithic thin-film resistor networks to provide high performance at moderate cost. Each type is available in 8, 10, and 12 bit versions.

DAC-QM

The DAC-QM contains within its 2" x 4" x 0.4" module a complete DAC, including $\mu DAC^{\mathbb{R}}$ quad switches and thinfilm resistor network, precision internal reference, a versatile output amplifier, and an input register. The user can select any of five voltage output ranges with jumpers at the module terminals.

DAC-QS

The DAC-QS is electrically identical to the DAC-QM, except that it does not contain an input register. As a result, the DAC-QS is packaged in the smaller $2'' \times 2'' \times 0.4''$ module, and its lower price reflects the change. As with the DAC-QM, its performance and stability are above average.



BLOCK DIAGRAM DAC-QS

ORDERING GUIDE: DAC-QM

MODEL DAC	XX	XX	XXX
	No. of Bits	Series	Input Code
Converter Type	8 10	QM	BIN (binary) 2SC (2's comp.)
	12		BCD

NOTE: BIN version is stocked. BCD and 2SC versions are built to order.

ORDERING GUIDE: DAC-QS

MODEL	DAC	XX	XX	XXX
		No. of Bits	Series	Input Code
Сол Тур	nverter pe	8 10 12	QS	C-B (comp. binary) CBD (comp. BCD)

NOTE: C-B version is stocked. CBD version is built to order.

Model	DAC-QM	DAC-QS
Resolution, Bits	8, 10, 12	*
Input Logic	TTL Positive True	*
Input Codes		
Unipolar	BIN ¹ BCD	$C-B^2$ CBD
Bipolar	2SC OBN	COB
Strobe Input Pulse Width	50ns min ³	N/A ⁴
Output Ranges	0 to +5V, 0 to +10V	*
1 0	$\pm 2.5 V, \pm 5 V, \pm 10 V$	*
F.S. Settling Time		
(to ½LSB)	5µs	*
Temperature Coefficients		
Gain (of reading)	7ppm/°C max	*
Offset		
Unipolar	$15\mu V/^{\circ}C$ max	*
Bipolar	$30\mu V/^{\circ}C max$	*
Power Requirement	+15V @ 25mA	*
	-15V @ 30mA	*
	+5V @ 150mA	+5V @ 35mA
Package Style	C-3	C-1
Package Dimensions	2" x 4" x 0.4"	2" x 2" x 0.4"
Prices (1-9)	DAC-8QM \$170.	DAC-8QS \$140.
	DAC-10QM \$210.	DAC-10QS \$170.
	DAC-12QM \$230.	DAC-12QS \$190.

SPECIFICATION SUMMARY (Typical @ +25°C unless otherwise noted)

 1 DAC-QM is stocked in the BIN version (which also gives OBN code in bipolar operation). The BCD and 2SC versions are built to order.

² DAC-QS is stocked in C-B version (which also gives COB code in bipolar operation). The CBD version is built to order.

³ The Strobe Input must be driven from a source capable of supplying 24 standard TTL unit loads.

⁴ The DAC-QS does not have a strobe input because it has no input register.

*Specifications same as those for the DAC-QM.

BLOCK DIAGRAM DAC-QM



DAC-12QS



2.10 124.1



TOP VIEW

FAST, DISPLAY D/A CONVERTERS DAC-IODF, MDA-IOF

GENERAL DESCRIPTION

These D/A converters are characterized primarily by very fast settling speeds. They are ideally suited for spot position control in CRT display systems, and for use in character generators, high speed test equipment, and very high speed A/D converters.

DAC-10DF

The DAC-10DF is a very fast voltage output D/A converter subsystem, featuring practically glitchless operation and 50ns settling to 0.05% of F.S. for 1LSB changes. Schottky TTL is used for the input register. The unit can be ordered with one of three output amplifiers, including the new model 50, which provides improved performance at no increase in price. With a model 46 or model 50 amplifier, the DAC-10DF can drive a terminated 100 ohm coaxial cable. Output connection is made through a μ DOT RF connector mounted on the DAC-10DF's P.C. board.

MDA-F

The MDA-10F is an ultra high speed digital-to-current converter offering 40ns full-scale settling time for 10-bit binary resolution. This exceptional speed is offered without compromise of the fine linearity and stability that is found in all Analog Devices products. The converter is packaged in a low-profile 2" x 4" module.

PIN DESIGNATIONS: DAC-10DF

PIN	FUNCTION	PIN	FUNCTION
Δ	BIT 1 (MSB)	N)	
B	BIT 2	P }	INTERLOCK
С	BIT 3	R	+5VDC
D	BIT 4	S)	
E	BIT 5	T	DIGITAL GRD
F	BIT 6	U)	
Н	BIT 7	V l	ANALOC CRD
J	BIT 8	ws	ANALOG GRD
K	BIT 9	X	+15VDC
L	BIT 10 (LSB)	Y	-15VDC
M	STROBE	Z	ANALOG GRD

ORDERING GUIDE: DAC-10DF

MODEL DAC-10DF	XXX Output Range	XX Output Amp
Converter Type	±2.5V	46
	$\pm 10V$	50

SPECIFICATION SUMMARY (Typical @ +25°C unless otherwise noted)

Model		MDA-10F		
Resolution, Bits	10	*	*	10^{2}
Logic Inputs	Schottky TTL, Positive True	*	*	TTL Positive True
Input Codes	Offset Binary	*	*	Comp. Binary
	2's Complement	*	*	or Comp. Offset Binary
Input Register	Yes	*	*	No
Output Amplifier	Model 46 ³	Model 48	Model 50 ³	None
Output Signal	$\pm 2.5V, \pm 5V, \pm 10V$	$\pm 2.5V, \pm 5V, \pm 10V$	$\pm 2.5 V, \pm 5 V, \pm 10 V$	0 to -4.7mA
	@ 100mA	@ 15mA	@ 100mA	or ±2.3mA
Settling Time (to ½LSB) ⁴				
For F.S. step	300ns max	500ns max	200ns max	40ns
For 1LSB step	50ns max	100ns max	40ns max	30ns
Glitch Amplitude	20mV max	5mV max	20mV max	Not Controlled
Temperature Coefficients				
Gain (of Reading)	±50ppm/°C max	*	*	±25ppm/°C
Zero (Unipolar)	N/A	*	*	$\pm 5 \text{ nA/}^{\circ}\text{C}$
(Bipolar)	±30ppm/°C max	±20ppm/°C max	±30ppm/°C max	±15ppm/°C
Power Required				
+15V	200mA max	80mA max	200mA max	60mA
-15V	200mA max	80mA max	200mA max	60mA
+5V	400mA max	*	*	N/A
Package Style	C-8	*	*	C-3
Package Size	4½" x 6" x 0.87"	4½" x 6" x 0.63"	4½" x 6" x 0.87"	2" x 4" x 0.4"
Price (1-9)	\$495.	*	*	\$240.

¹ The DAC-10DF can be ordered with any of three output amplifiers. The model 48 would generally be chosen where power consumption is of concern and a high output current is not required. When used with a model 46 or model 50, the DAC-10DF is intended to drive a terminated coaxial cable. The model 50 is a new amplifier, and offers improved performance as compared to the model 46.

² An 8-bit version of the MDA-10F, called the MDA-8F, is available for \$220 (1-9).

³ When used with a model 46 or model 50, the DAC-10DF is intended to drive a coaxial cable that is terminated in a resistance equal to the characteristic impedance of the cable.

 4 The settling times shown for the DAC-10DF are valid for the $\pm 2.5V$ output range. Settling times for the $\pm 5V$ and $\pm 10V$ ranges are somewhat greater.

*Specifications same as those for the DAC-10DF with a model 46 output amplifier.



HIGH RESOLUTION D/A CONVERTERS DAC-QM, DAC-QG

GENERAL DESCRIPTION

These D/A converters offer the limit of today's state-of-theart in resolution, linearity, and stability. Analog Devices' μ DAC monolithic quad switches and super precision thin film resistor networks provide the stability needed for 16-bit performance. These products are supplied with an error plot made during final testing, and with certification of the performance of the reference zener.

DAC-16QM

The DAC-16QM is a complete self-contained 16-bit D/A converter with both current and voltage outputs, offered in 16 or 14-bit linearity versions. This converter has an aged compensated reference that provides stability appropriate for high resolution converters. Settling time of the current output is about 1 μ s to 0.1% for full scale changes. As can be expected, however, settling time to full accuracy (0.0015%) for voltage output with the built-in IC output amplifier, is much greater. When faster settling is required, a fast external amplifier should be used. (See DAC-QM settling chart on next page.)



DAC-QG

The DAC-QG is a manifold board for the DAC-16QM, making provisions for the most-frequently required accessories. The standard (stocked) version of the DAC-16QG has an input register wired for binary code, and has a deglitcher mounted. It is wired for +10V output range, using the model 184L output amplifier (the optimum amplifier choice for both stability and speed, in this application).

PIN I	DESIGNATIONS: DAC-QG					
PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	
1-17	N.C.	E	BIT 5	S	BIT 15	
18	ANALOG SENSE LOW	F	BIT 6	Т	BIT 16 (LSB)	
19	ANALOG SOURCE LOW	Н	BIT 7	U	STROBE	
20	ANALOG SOURCE HIGH	J	BIT 8	V	N.C.	
21	ANALOG SENSE HIGH	K	BIT 9	W	+5V	
22	ANALOG REF. IN/OUT	L	BIT 10	X	+15V	
Α	BIT 1 (MSB)	M	BIT 11	Y	-15V	
В	BIT 2	N	BIT 12	Z	GRD	
С	BIT 3	Р	BIT 13			
D	BIT 4	R	BIT 14			

ORDERING GUIDE: DAC-QM

MODEL	DAC	XX	XX	XXX
		Linearity	Series	Input Code
Converter	Туре	14 Bits 16 Bits	QM	C-B (comp. binary) CBD (comp. BCD)

NOTE: Stock version is complementary binary.



NOTES:

¹ADI Convention: Positive true is normal. ²When no register is ordered, the DAC-QM that is mounted determines the coding.

SPECIFICATION SUMMARY	(Typical @ +25 C unless otherwise noted)	DAC-OC
Model	DAC-QM	DAC-QG
Resolution, Bits	lution, Bits 14, 16	
Input Logic	TTL Positive True	*
Input Codes	Complementary Binary	BIN^2 , BCD, 2SC
	Complementary BCD ³	Sign & Mag BIN & BCD
Linearity Error		
(straight line through		
zero and full scale)		
DAC-14XX	±<0.003%	*
DAC-16XX	±<0.0015%	*
Reference, Internal	+6.00V ±0.01% ±6ppm/°C ±8ppm/mo.	*
Temperature Coefficient-		
Voltage Mode		
(in ppm of FS/°C)	with int. amp.	with 184L amp.
Gain	±15ppm	±7ppm
Unipolar Offset	±9ppm	±0.5ppm
Bipolar Offset	±15ppm	±7ppm
Settling Speed	See figures	See figures
Power Requirement	+15V @ 20mA	+15V @ 35mA
	-15V @ 30mA	-15V @ 50mA
	+5V @ 40mA	+5V @ 220mA
Package Style	C-3	C-8
Package Dimensions	2" x 4" x 0.4"	4 ¹ / ₂ " x 4 ³ / ₄ " x 0.4"
Price $(1-9)$	DAC-14QM \$395.	DAC-16QG
	DAC-16QM \$745.	(complete) ² \$1170.
		DAC-14QG
		$(complete)^2$ \$820.

¹DAC-QG can be built to order with any DAC-QM from 8 to 16 bits. ²DAC-QG is stocked in a version containing the most popular options. All other versions are built to order. The stock version, available either with 14 or 16-bit resolution, contains: Binary input code with register, 0 to +10V range, 184L output amplifier, deglitcher to limit output switching transients to 5mV max.

³DAC-14/16QM is stocked in Complementary Binary code. Complementary BCD is built to order. *Specifications same as for Model DAC-16QM.



MULTIPLYING D/A CONVERTERS DAC-M, MDA-IIMF



GENERAL DESCRIPTION

Multiplying D/A converters are specifically designed for use with external reference signals, which may be of varying amplitude DC or AC. They act essentially as accurate digitally-controlled attenuators, and find broad application in synchro conversion, character generation for CRT displays, and hybrid computation.

DAC-M

The DAC-M is a complete self-contained four-quadrant multiplying D/A converter optimized for applications at the lower frequency end of the spectrum. It has both an input buffer and inverter, providing for four-quadrant operation from a single polarity (or phase) of reference input, if desired. With binary logic input code, it can be operated in bipolar fashion by use of the offset coding.



The MDA-11MF is a very high speed one or two quadrant multiplying digital-to-current converter designed particularly for the needs of the graphic display field. Operating as a single quadrant device, it can control a $10V/\mu s$ reference ramp with 11-bit resolution and feedthrough. An internal network provides for two quadrant operation.

LOW FEEDTHROUGH

The very low feedthrough of the MDA-11MF when operated in the single-quadrant mode is shown below. In both photographs the lower trace is a 500kHz, $10V/\mu$ s triangle wave driving the analog input (shown with a vertical scale of 5V/div.). The upper trace in both pictures is the amplified output of the DAC connected to an op amp such as an ADI model 48. The vertical scale is 5mV/div., which is approximately equal to 1LSB/div. The trace on the left shows the output with the LSB input on and all other inputs off. The right-hand trace shows the output with all digital inputs off, and clearly demonstrates that the feedthrough under these conditions is less than 1/2LSB.



Feedthrough with a 500kHz Triangle Wave



40

38

+15

33

35

BIT 11 O

SPECIFICATION SUMMA	RY (Typical @ +25 C u	nless otherwise no	ted)
Model	DAC-8M	DAC-12M	MDA-11MF
Resolution, Bits	8	12	11
Relative Accuracy			
(Error in % of FS)	0.2%	0.02%	0.03%
Slewing Rate	10V/µs	*	N/A ¹
Settling Time	10µs to 0.2%	15µs to 0.01%	$<1\mu$ s to 0.01%
Full Output			
Freq. (±10V)	200kHz	*	N/A
Reference Input			
Voltage	±10V p-p	*	0 to -10V
Impedance	$10 \mathrm{k}\Omega$	*	$4k\Omega$
Logic Input	TTL Positive True	*	*
Logic Code	Binary	*	Binary or Offset Binary
Output			onisee binary
Voltage	±10V	*	$\pm 1 \mathrm{V} \mathrm{max}^{1}$
Current	5mA	*	+4mA or ±2mA
Impedance	< 1 ohm	*	600 ohms
Temperature Coefficient			-
Gain	< 25ppm/°C	< 5ppm/°C	±30ppm/°C
Zero	$< 50 \mu V/^{\circ} C$	*	$\pm 75 \mu V/^{\circ} C^{2}$
Feedthrough	2.5mV @ 400Hz FS	*	Unipolar Mode < ½LSB
			with $10V/\mu s$ triangle wave
Power Required	+15V @ 17mA	*	+15V @ 30mA
	-15V @ 20mA	*	-15V @ 10mA
Package Style	C-1	*	C-3
Package Dimensions	2" x 2" x 0.4"	*	2" x 4" x 0.4"
Price (1-9)	\$195.	\$295.	\$150.

¹ Since there is no output amplifier, the MDA-11MF is not slewing rate limited in the usual sense. BW and slewing rate are more than adequate for accurate transconduction of a 10V/ μ s reference ramp. ² Measured using an ADI Model 48 as an output amplifier.

*Specifications same as for Model DAC-8M.



BLOCK DIAGRAM



DAC-12M



TOP VIEW

MILITARY GRADE D/A CONVERTER MDA-12QD



GENERAL DESCRIPTION

Products in this category have been designed and manufactured to meet the unique requirements of many military applications. They are designed with the ability to utilize MIL/QPL components. IC's used can be qualified to MIL-STD-883. Assembly and package are designed for qualification according to appropriate paragraphs of MIL-STD-202 and MIL-E-5272.



Pin 1 is indicated by blue glass sealant at base, and by black dot on top surface.

PIN DESIGNATIONS

PIN	FUNCTION
1	BIT 1 (MSB)
2	BIT 2
3	BIT 3
4	BIT 4
5	BIT 5
6	BIT 6
7	BIT 7
8	BIT 8
9	BIT 9
10	BIT 10
11	BIT 11
12	BIT 12 (LSB)
13	REFERENCE INPUT
14	BIPOLAR OUTPUT OFFSET
15	POWER AND SIGNAL GROUND
161	5V)
17	GAIN FEEDBACK
10}	5K RESISTORS
18)	,
19	INTERNAL REFERENCE OUTPUT
20	+15VDC SUPPLY INPUT
21	ANALOG OUTPUT
22	μ DAC's BASE LINE REFERENCE
23	-15VDC SUPPLY INPUT
24	+5VDC SUPPLY INPUT

MDA-QD

The MDA-12QD is a medium speed 12-bit current output D/A converter in a hermetically sealed metal enclosure, with 24-lead DIL pinning. Flatpack versions of the μ DAC quad converter switches and thin-film resistor networks are used along with flatpack reference amplifier, to provide outstanding linearity and stability in a package occupying only $1\frac{1}{2}$ " x 1" x 0.4".

Model	MDA-QD
Resolution, Bits	12
Linearity Error	±½LSB
Data Inputs	TTL Compatible
Input Codes	Complementary Binary
	Complementary Offset Binary
Output Range	0 to $-2mA$, $\pm 1 mA^{1}$
FS Settling Time (to ½LSB)	$3\mu s^2$
Output Impedance ³	
(Current Mode)	Less than 15k, 15pF
Temperature Coefficients	
Linearity	±3ppm/°C
Gain (with internal reference)	±15ppm/°C max
Gain (with external reference)) ± 10 ppm/°C max
Zero (unipolar)	$\pm 2nA/^{\circ}C$ max (up to $\pm 70^{\circ}C$)
Offset (bipolar)	± 10 nA/°C max (up to $\pm 70^{\circ}$ C)
Power Required	±15V @ +15mA, -20mA
	+5V @ 25mA
Operating Temperature Range	
Standard	0° C to $+70^{\circ}$ C
Extended ⁴	-55° C to $+125^{\circ}$ C
Package Style	- C-7
Package Dimensions	1 ¹ / ₂ " x 1" x 0.4"
Price (1-9)	MDA-12QD \$245.
	MDA-12QD/ET \$395.

¹ For use with external op amp, precision tracking feedback resistors are provided. Voltage output ranges with these feedback resistors are: $\pm 2.5V$, $\pm 5V$, $\pm 10V$, 0 to +5V, and 0 to +10V.

² When used with an AD507 output op amp or equivalent.

 3 For optimum linearity, current output should drive an essentially zero impedance point, such as an op amp summing junction. If resistance load must be used, $\rm R_L$ should be no greater than 1k ohms.

⁴ For extended temperature version, specify "MDA-12QD/ET."

CAPSULE SELECTION TABLE

ANALOG-TO-DIGITAL CONVERTERS

SPECIFICATIONS (Typical @ +25°C unless otherwise noted)												
Product Classification	Model	Resolution	Error (Relative to F.S.)	Conversion Time	Output Code Options ¹ (TTL/DTL Compatible)	Analog Input Options	Input Buffer	Gain TC ²	Power Requirements	Package Size & Style	Price (1-9)	Price (100+)
Low Cost General Purpose	ADC-8S ADC-10Z ADC-12QZ	8 bits 10 bits 12 bits	±0.2% ±0.05% ±0.0125%	1ms 20μs 40μs	BIN, OBN, 2SC, BCD BIN, OBN, 2SC BIN, OBN, 2SC	±5V,±10V,+5V,+10V	YES OPTIONAL ³ OPTIONAL ³	±60ppm/°C ±40ppm/°C ±30ppm/°C	±15V, +5V	2" x 3" x 0.4", C-2 2" x 4" x 0.4", C-3 2" x 4" x 0.4", C-3	\$ 79 \$ 99 \$ 129	\$47 \$67 \$92
High Performance	ADC-8QM ADC-10QM ADC-12QM	8 bits 10 bits 12 bits	±0.2% ±0.05% ±0.0125%	18μs 22μs 25μs	BIN, OBN, 2SC, BCD	±5V,±10V,+10V	YES	±5ppm/°C	±15V, +5V	2" x 4" x 0.4", C-3	\$ 250 \$ 280 \$ 305	
General Purpose ADC-8QU ADC-10QU ADC-12QU	ADC-8QU ADC-10QU ADC-12QU	8 bits 10 bits 12 bits	±0.2% ±0.05% ±0.0125%	6.4μs 8μs 15μs	BIN, OBN, 2SC, BCD	±5V,±10V,+5V,+10V	YES	±5ppm/°C	±15V, +5V	2" x 4" x 0.4", C-3	\$ 260 \$ 290 \$ 315	
Dual Slope	ADC1100 ADC-141 ADC-171	3½ digits 14 bits 17 bits	±0.05% ±1 bit ±0.01% ±1 bit ±0.01% ±1 bit	42ms 40ms 40ms	SMD SMB SMD	±199.9mV ±10V ±12V	YES NO NO	±50ppm/°C ±5ppm/°C ±5ppm/°C	+5V ±15V, +5V ±15V, +5V	2" x 4" x 0.4", C-3 3" x 4" x 0.4", C-5 3" x 4" x 0.4", C-5	\$ 99 \$ 259 \$ 259	\$67
Fast	ADC1103-001 ADC1103-002 ADC1103-003	8 bits 10 bits 12 bits	±0.2% ±0.05% ±0.0125%	1.0μs 1.2μs 3.5μs	BIN, OBN, 2SC	±5V, ±10V, +10V	NO	±10ppm/°C	±15V, +5V	2" x 4" x 0.75", CA-3	\$ 430 \$ 440 \$ 450	
High Resolution	ADC-16Q	16 bits	±0.0015%	400µs	BIN, OBN, 2SC	±5V, ±10V, +10V	YES	±8ppm/°C	±15V, +5V	4.5" x 6.0", C-8	\$1350	
Low Power CMOS	ADC-12QL/J ADC-12QL/K	12 bits	±0.01%	85 to 130µs	BIN, OBN	±5V,±10V,+5V,+10V	NO	±50ppm/°C ±20ppm/°C	±15V, +5V	3.6" x 4.1", C-8	\$ 675 \$ 950	

NOTES

- Logic Codes: BIN, Binary; C-B, Comp. Binary; OBN, Offset Binary: COB, Comp. Offset Binary; BCD, Binary Coded Decimal; CBD, Comp. BCD; 2SC, Two's Complement; C2C, Comp. Two's Comp.; SMB, Sign-Magnitude Binary; SMD, Sign-Magnitude BCD.
- Standard temperature range on all converters is 0 to +70°C, with storage temperature from -55°C to +125°C. Many models are available in an extended operating temperature version at extra cost. The extended operating temperature range is normally -25°C to +85°C.
- 3. Prices are for units without input buffer. In small quantities, add \$20 to unit price for buffer.

LOW COST GENERAL PURPOSE A/D CONVERTERS ADC-85, ADC-10Z, ADC-12QZ

GENERAL DESCRIPTION

These analog-to-digital converters are characterized by low cost, achieved through skilled engineering and high volume, efficient manufacturing. They offer an extremely high performance/cost ratio.

ADC-8S

The ADC-8S is an 8-bit A/D converter of moderate speed that even includes an input buffer. A counter generates a staircase at the output of an internal DAC, the output of which is compared against the signal input. This design requires only simple logic circuitry, helping to hold down cost. Conversion time is proportional to the magnitude of the input signal.

ADC-10Z

The ADC-10Z is a small modular A/D converter that performs a 10-bit conversion in 20μ s or less. It offers performance and features previously found only in much more expensive converters. It uses the successive approximations conversion technique, and contains an easy-to-use serial output.



ADC-12QZ

The ADC-12QZ is a 12-bit successive approximation type converter that offers reasonable speed and good performance at very low cost. Analog Devices' μ DAC[®] quad current switches and a unique combination of thick-film and hybrid technology has given the ADC-12QZ the basic performance of a much higher priced unit. Like the ADC-10Z, it features an easy-to-use serial output.

BLOCK DIAGRAM ADC-12QZ





BLOCK DIAGRAM



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SPECIFICATION SUMMARY (Typical @ +25°C unless otherwise noted)						
Model	ADC-8S	ADC-10Z	ADC-12QZ			
Resolution, Bits	8	10	12			
Linearity Error	±½LSB	*	*			

Analog Input			
Ranges [*] (Volts)	$\pm 5, \pm 10, \pm 5, \pm 10$	*	*
Impedance			
Without Buffer ²	$2.5k - 10k\Omega$	$6k - 12k\Omega$	$2.5k - 10k\Omega$
With Buffer ³	10° ohms	10° ohms	10° ohms
Conversion Time	1ms^4	20µs	40µs
Digital Control			
Inputs & Outputs	TTL/DTL Compatible	*	*
Data Outputs Output Codes	TTL Positive True	*	*
Standard ⁵	BIN, OBN, 2SC	BIN, OBN, 2SC	BIN, OBN, 2SC
Optional	BCD	-	
Status or Busy	"1" during	*	
Output	Conversion		
Serial Data Output	No	Yes	Yes
Temperature Coefficient			
Gain (of Reading)	±60ppm/°C	±40ppm/°C	±30ppm/°C
Zero (Unipolar)	±20ppm/°C	±25ppm/°C	±5ppm/°C
Offset (Bipolar)	±60ppm/°C	±30ppm/°C	±10ppm/°C
Power Required	+15V @ 28mA	+15V @ 18mA	+15V @ 20mA
	-15V @ 28mA	-15V @ 25mA	-15V @ 30mA
	+5V @ 120mA	+5V @ 170mA	+5V @ 210mA
Package Style	C-2	C-3	C-3
Package Dimensions	2" x 3" x 0.4"	2" x 4" x 0.4"	2" x 4" x 0.4"
Price (100+)	\$47.	\$67.	\$92.
(1-9)	\$79.	\$99. ³	\$129. ³

¹Desired input range is selected with jumpers and connections at the module's terminals.

² Input impedance without buffer depends on input range selected, but will be within the indicated limits.

³ Input buffer is standard on ADC-8S, but the unit may be wired for a direct input, if desired. On ADC-10Z and ADC-12QZ, input buffer is optional. In small quantities, add \$20 to price for input buffer. Units with a buffer may be wired for direct input, if desired.

⁴ Conversion time for a full-scale input signal is approximately 1ms. For input signals with a magnitude of less than full-scale, the conversion time is proportionately less.

⁵ Output code is natural binary for unipolar input, but it can be either offset binary or two's complement at the user's option with a bipolar input.

*Specifications same as for ADC-8S.







ORDERING GUIDE

ADC-	8S	
ADC-8S/BIN	BIN	_
ADC-8S/BCD	BCD	

ADC-10Z		
ADC-10Z-002	NO BUFFER	
ADC-10Z-022	BUFFER	

ADC-1	12QZ
ADC-12QZ-003	NO BUFFER
ADC-12QZ-023	BUFFER

HIGH PERFORMANCE GENERAL PURPOSE A/D CONVERTERS ADC-QM, ADC-QU

GENERAL DESCRIPTION

These converters are characterized primarily by high performance and general utility. The use of $\mu DAC^{\textcircled{B}}$ monolithic quad switches with μDAC monolithic thin film resistance networks provide these converters with the best stability and linearity generally available. Prices are kept at moderate levels by large volume manufacturing.

ADC-QM

The ADC-QM is a high performance, general purpose A/D converter packaged in a low profile 2" x 4" module. It offers excellent stability over both time and temperature at moderate cost. It is complete with an input buffer, and the desired input range is selected by the user with jumpers and connections at the module terminals. The digital output code of the binary version is natural binary for a unipolar input, but is selected by the user to be either offset binary or two's complement with a bipolar input. The ADC-QM is available in 8, 10, and 12 bit versions.

BLOCK DIAGRAM



ADC-QU

The ADC-QU is a modular analog-to-digital converter that is very similar to the ADC-QM, except that it offers an appreciably shorter conversion time. The 12 bit version performs a conversion in 15μ s maximum. The ADC-QU's speed is the result of the use of Analog Devices' AD551 μ DAC[®] high speed quad current switches in its internal DAC. The ADC-QU is pin-compatible with the ADC-QM, and in most applications can serve as a direct plug-in replacement for it. When mounted on an AC4451 mounting card, the ADC-QU becomes a pincompatible substitute for the older model ADC-U.



Note: In the ADC-8QM and ADC-8QU, bit 8 is the LSB, and pins 48, 50, 52 and 54 are deleted. In the ADC-10QM and ADC-10QU, bit 10 is the LSB, and pins 48 and 50 are deleted.

DATA ACQUISITION APPLICATIONS

An ADC-QM or an ADC-QU can be combined with a SHA-1A or SHA-2A sample-and-hold amplifier, and one or more MPX-8A multiplexers to form a data acquisition subsystem. The table below shows the maximum throughput rates (conversions/ sec) that can be achieved using various combinations of these products. The settling time of the MPX-8A does not affect the throughput rate because it can be settling on a new input signal at the same time the A/D converter is converting the signal being held constant by the sample-and-hold amplifier.

ADC	SHA	MAX. THROUGHPUT RATE
ADC-12QM	SHA-1A	34kHz
ADC-12QM	SHA-2A	39kHz
ADC-12QU	SHA-1A	50kHz
ADC-12QU	SHA-2A	67kHz

ORDERING GUIDE: ADC-QM and ADC-QU

ADC-XX	XX	/XXX
No. of Bits	Series	Output Code
8	QM	BIN (binary)
10	QU	BCD (binary)
12		coded decimal)

92 CONVERTERS

SPECIFICATION SUMMA	RY (Typical @ +25°C unless or	therwise noted)
Model	ADC-QM	ADC-QU
Resolution, Bits	8, 10, 12	*
Linearity Error	±½LSB	*
Analog Input		
Ranges ¹ (Volts)	$\pm 2.5, \pm 5, \pm 10,$	*
6	+10, +5	
Input Impedance		
Without Buffer ²	2.5k - 10k ohms	*
With Buffer	10 ⁸ ohms	*
Conversion Time	18µs 22µs 25µs	6.4µs 8µs 15µs
Digital Control		
Inputs & Outputs	TTL/DTL Compatible	*
Data Outputs	TTL Positive True	*
Output Codes		
Standard	BIN, OBN, 2SC	*
Optional	BCD	
Status or Busy		
Output	"1" During Conversion	*
Serial Data Output	No	Yes
Temperature Coefficient		
Gain (of Reading)	5ppm/°C	*
Offset (Unipolar)	50μV/°C	*
(Bipolar)	75μV/°C	*
Power Required	+15V @ 25mA	+15V @ 25mA
	-15V @ 35mA	-15V @ 50mA
	+5V @ 200mA	+5V @ 300mA
Package Style	C- 3	*
Package Size	2" x 4" x 0.4"	*
Price (1-9)	ADC-8QM \$250.	ADC-8QU \$260.
	ADC-10QM \$280.	ADC-10QU \$290.
	ADC-12QM \$305.	ADC-12QU \$315.

¹The desired input range is selected by the user with connections and jumpers at the module terminals.

² Input impedance without buffer is proportional to input voltage range.

*Specifications same as for ADC-QM.

TIMING DIAGRAM ADC-QM

M

'1' '0' '0' '1

- 100nsec MIN

'0' '1' '0' '1'

'0' '0' '1' '0'

1 2 3 4 5 6 7 8 9 10 11 12

'1'

'O'

'1'

11

·0'





CONVERT COMMAND

STATUS

CLOCK

MSB

2SB

3SB

4SB

5SB

LSB

COMPARATOR OUTPUT

CONVERTERS 93

DUAL SLOPE A/D CONVERTERS ADC-I4 I, ADC-I7 I, ADCII00

Annalog Devices Annalog Devices Annalog Devices Annalog Devices Annalog Devices Annalog Devices

GENERAL DESCRIPTION

Dual slope integrating A/D converters perform a conversion by first integrating the input signal for a fixed period of time, and then measuring the time required to return the integrator to zero when it is integrated in the opposite direction with a fixed reference signal. A major benefit of this technique is that it results in very high rejection of normal mode noise when the signal integration time period is set equal to one cycle of the power line.

ADC-14I and ADC-17I

These two high resolution converters are identical except for output coding. The ADC-14I has 14-bit binary plus sign coding, while the ADC-17I has 4½ digits plus sign output coding. Both feature a normal mode rejection ratio of 70dB, an automatic zero correction cycle, and a gain TC of only ±10ppm/°C.

ADC1100

The ADC1100 is a new dual slope A/D converter in a compact $2'' \times 4'' \times 0.4''$ module. It can be triggered externally, or internally at a rate of about 4 conversions/sec, or it can be wired to start a new conversion when the conversion in progress is completed. It is ideal for driving a display, or feeding data to a computer, or for doing both jobs simultaneously. Since it requires only +5V power, and has a normal mode noise rejection ratio of 40dB minimum, it is a natural choice for installation at transducer locations.



new product: ADC 1100

SPECIFICATION SUMMARY (Typical @ +25°C unless otherwise noted)

Model	ADC-14I	ADC-17I	ADC1100
Resolution	14 binary bits	4 ¹ / ₂ BCD digits ¹	3½ BCD digits
	plus sign	plus sign	plus sign
Linearity Error	±0.01%	*	±0.05%
Analog Input			
Range	±10V	$\pm 12V$	±199.9mV
Impedance	180kΩ	*	$10^8 \Omega$
Bias Current	N/A	*	1.5nA
Resolution	0.61mV/bit	1.0mV/bit	0.1mV/bit
Continuous Overload ²	±100V max	*	±20V max
Normal Mode Rejection			
@ 60Hz ³	70dB	*	40dB min ⁴
Conversion Time	40ms max	*	42ms max ⁵
Digital Control			
Inputs and Outputs	TTL/DTL Compatible	*	*
Data Outputs	TTL Positive True	*	*
Output Code	Sign plus	Sign plus	Sign plus
	magnitude binary	magnitude BCD	magnitude BCD
Temperature Coefficients			
Gain	±10ppm/°C	*	±50ppm/°C max
Offset	$\pm 10 \mu V/^{\circ} C$	*	±2ppm/°C max
Power Required	+15V @ 30mA	*	+5V @ 200mA
	-15V @ 30mA	*	_
	+5V @ 200mA	*	-
Package Style	C-5	*	C-3
Package Dimensions	3" x 4" x 0.4"	*	2" x 4" x 0.4"
Price (1-9)	\$259.	*	\$99.
(100+)			\$67.

¹ Maximum digital output code is 11999, which corresponds to an input of 11.999V.

² Maximum overload that can be sustained indefinitely, with power on or off, without endangering the unit.

³ Both the ADC-I and ADC1100 can be adjusted by the user to optimize the normal mode rejection of 50Hz noise, rather than 60Hz noise, if desired.

⁴ The ADC1100 has provisions for connecting an external phase locked loop that can increase the normal mode noise rejection ratio to over 100dB.

⁵ In the event of an overload, it can take as long as 70ms to complete a conversion.

*Specifications same as for model ADC-14I.



Delay of $\sim 1\%$ clock periods to reset counter and strobe comparator for polarity data.

7ms min delay for drift correction phase.

TIMING DIAGRAM ADC1100



¹ Reference integration time t = $\frac{E_{IN}}{200mV}$ x 16.67ms. In the event of an overloaded input, t_{max} = 50ms.

 $^{\rm 2}$ Polarity data is valid anytime after the completion of the signal integration time period.

time period. ³ In the event of an overloaded input, the overload output will go to a logic "1" approx. 42ms after the conversion commences. However, the status output will not return to zero until the integrator has been integrated back to zero, which can be as long as 70ms after the conversion began.

FAST A/D CONVERTER ADCII03



GENERAL DESCRIPTION

These analog-to-digital converters are characterized primarily by very high speed. They are especially well suited for applications requiring high throughput rates with no compromise in accuracy. They can be considered general purpose devices as well, however, and are a natural choice for large data acquisition systems. Among other typical applications are geophysical data acquisition, simultaneous sample-and-hold systems, and conversion for data entry into digital filters and correlators.

BLOCK DIAGRAM

ADC1103

The ADC1103 is a very fast successive approximation converter packaged in a small 2" x 4" module. The 12 bit versi performs a full conversion in less than $3.5\mu s$. The ADC1102 a complete self-contained converter, requiring only standare $\pm 15V$ and $\pm 5V$ power, and the usual control signals. The inj range and output coding are user selected.

AND PIN DESIGNATIONS ADC1103 72 BIPOLAR OFFSET REF ZENER +5V m DIGITAL GRD 2 0 1 COMPARATOR 70 GAIN ADJ -0 +15V 4 0 ~~~ -15V 6 0-\$ MSB 8 0 t REF AMP BIT 1 (MSB) 10 BIT 2 12 0 61 DATA STROBE PRECISION HIGH SPEED 58 SERIAL DATA BIT 3 15 0 BIT 4 17 55 ANALOG GRD BIT 5 19 0 54 ANALOG GRD BIT 6 21 0 BIT 7 23 50 SIG GRD SENSE 0 -0 49 COMP IN BIT 8 25 0--0 48 INPUT 2 47 INPUT BIT 9 27 46 OFFSET ADJ 0 BIT 10 30 TTL LOGIC AND 42 CONVERT CMD BIT 11 32 BIT 12 34 39 STATUS 38 STATUS 38 CLOCK 37 CLK INHIBIT

Note: The standard model does not have a serial output, and therefore pins 58 and 61 are deleted from it. In addition, the ADC1103-002 does not contain pins 32 and 34, and the ADC1103-001 does not contain pins 27, 30, 32, and 34.

SPECIFICATION SUMMARY (Typical @ +25°C unless otherwise not

Model	ADC1103		
Resolution			
ADC1103-001	8 Bits		
ADC1103-002	10 Bits		
ADC1103-003	12 Bits		
Conversion Time			
ADC1103-001	$1.0\mu s max$		
ADC1103-002	$1.2\mu s max$		
ADC1103-003	$3.5\mu s max$		
Accuracy			
Error Relative to Full Scale	±½LSB max		
Diff. Nonlinearity Error	±½LSB max		
Gain TC	±10ppm/°C max		
Analog Input Ranges	0 to $\pm 10V, \pm 10V, \pm 5V$		
Input Impedance	5.00k Ω on ±10V Range		
	2.50k Ω on other Ranges		
Digital Inputs & Outputs	TTL Compatible		
Output Codes			
With Unipolar Input Range	Positive True Binary		
With Bipolar Input Range	Positive True Offset Binary		
	or Two's Complement		
Power Required	+15V @ 85mA max		
•	-15V @ 80mA max		
	+5V @ 525mA max		
Package Style	C-3		
Package Dimensions	2" x 4" x 0.75"		
Prices (1-9)			
ADC1103-001	\$430		
ADC1103-002	\$440		
ADC1103-003	\$450		

HIGH RESOLUTION A/D CONVERTER ADC-16Q

GENERAL DESCRIPTION

When maximum resolution and accuracy are required, a 16 bit state-of-the-art A/D converter is called for. An analog-to-digital converter with 65,536 distinct output codes, where an LSB is only 152μ V, demands advanced engineering, skilled manufacturing, and the use of the highest quality available components, without compromise.

ADC-16Q

The 16 bit ADC-16Q offers unprecedented linearity, accuracy, and stability in a very compact package. The 4½" x 6" P.C. board holds two modules: a standard DAC-16QM, and the I/O (input/output) module which contains successive approximations logic, a precision comparator, and a differential input buffer that features high common mode rejection. The noeffort-spared engineering that went into the design of the ADC-16Q took into account not only the internal design

PIN DESIGNATIONS: ADC-16Q

PIN	FUNCTION	PIN	FUNCTION
1	$\overline{\text{BIT}}$ 1 ($\overline{\text{MSB}}$)	А	BIT 1 (MSB)
2	N.C.	В	BIT 2
3	N.C.	С	BIT 3
4	N.C.	D	BIT 4
5	INTERLOCK	E	BIT 5
6	f interested	F	BIT 6
7	N.C.	Н	BIT 7
8	EXTERNAL CAPACITOR	J	BIT 8
9	FOR CLOCK RATE	K	BIT 9
10	N.C.	L	BIT 10
11	BIT 14	M	BIT 11
12	BIT 15	N	BIT 12
13	BIT 16 (LSB)	Р	BIT 13
14	SERIAL OUTPUT	R	CLOCK OUTPUT
15	CONVERT INPUT	st	SHORT CYCLE RETURN
16	STATUS OUTPUT	Т	STATUS OUTPUT
17	DIGITAL 5V COMMON	U	+5VDC INPUT (V_L)
18	+15VDC INPUT (+VS)	V	-15VDC INPUT (-VS)
19‡	±15V COMMON	Wİ	±15V COMMON
20*	SIGNAL (-) INPUT	X*	SIGNAL (-) INPUT
21	SIGNAL (+) INPUT	Y*	SIGNAL (-) INPUT
22*	SIGNAL (-) INPUT	Z*	SIGNAL (-) INPUT

*Pins 20, 22, X, Y, Z all connected internally to signal (¬) input. Do not use as tie points for any function other than signal input. ‡Pins 19 and W are connected together internally. Use one for power ground and the other for signal source ground return. †Must be tied to Pin #17 for 16-bit operation.

NOTES:

- 1. In buffered modes, input is true differential. Thus reversal of input connections would yield ranges of 0 to -10V, $\pm 10V$, and $\pm 5V$.
- 2. When shipped, units will be jumpered for ±10V operation with buffer. User can change jumpers to select a different input voltage range, and/or omit input buffer.



problems, but also the system problems faced by a user who needs to make sure that the converter will perform in his system to the accuracy of which it is capable. Each ADC-16Q is supplied with a reference certificate and an error plot of its DAC made during final production test.

SPECIFICATION SUMMARY (Typical @ +25°C unless otherwise noted)

Model	ADC-16Q
Resolution, Bits	16 Binary
Linearity Error	±0.0015%
Analog Input	
Ranges (Volts)	$\pm 5, \pm 10, +10$
Impedance	
Direct	5k or 10k ohms ¹
with Buffer	10 ⁹ ohms
Conversion Time to	
Full Accuracy	$400\mu s^2$
Settling Time of	
Input Buffer to	
Full Accuracy	3.6ms ²
Digital Control	
Inputs and Outputs	TTL/DTL Compatible
Data Outputs	TTL Positive True
Output Codes	BIN, OBN, 2SC
Output Formats	Parallel & Serial
Reference	Internal precision
	reference
Temperature Coefficient	
Gain	$0.0008 \%/^{\circ} C max$
Offset	$0.0002\%/^{\circ}C \pm 25\mu V/^{\circ}C max$
Power Required	+15V @ 18mA
	-15V @ 41mA
	+5V @ 350mA
Package Style	C-8
Package Dimensions	4½" x 6.0" x 0.44"
Price (1–9)	\$1350.

¹ Direct input impedance is 10k ohms for ±10V input range, and 5k ohms for other input ranges.

² ADC-16Q can be operated at higher speeds with reduction in accuracy, or short-cycled.

LOW POWER A/D CONVERTER ADC-12QL

GENERAL DESCRIPTION

Low power converters have been developed to solve the problems of operation in remote areas with limited power. Ideally suited for operation from battery power, these products are particularly useful for ocean buoy installation, as well as for remote meteorlogical data acquisition. The small size and light weight also make them useful in portable medical and scientific instruments.

CURRENT DRAIN VS CONVERSION RATE



ADC-12OL

The ADC-12QL is an A/D converter having total power consumption of about 1/2000 of that of a conventional design. Requiring only a single battery to supply all its power



Model	ADC-12QL			
Resolution, Bits	12			
Linearity Error	±1/2	LSB		
Analog Input Ranges	$+5V \pm 5V$	$+10V$ $\pm 10V$ ¹		
Input Impedance	4.1k 8.2k	8.2k 16.4k		
Conversion Time ²	85µs with logic	supply at +15V		
	130 μ s with logic supply at +6			
Digital Inputs and Outputs ²	TTL compatible with +6V logic supp			
	C/MOS compatible with +15V logic supply			
Parallel Data Output	12-bit binary	12-bit binary, positive true		
Serial Data Output	Negative true, MSB first			
Convert Command	1.0µs pulse min, 70% of logic power level			
Status or Busy Signal	"1" during conversion			
Temperature Coefficient	J	K		
Gain (of Range)	50ppm/°C max	20ppm/°C max		
Zero (Unipolar)	$50\mu V/^{\circ} C max$	*		
Offset (Bipolar, -FS)	20ppm/°C max	*		
Power Required ²	Logic: +6V to +15V	Analog: $+12V$ to $+15V$		
a anna anna anna anna anna anna anna a	(can be operated fro	m single 15V battery)		
Package Style	C-	-8		
Package Dimensions	4.1" x 4.02	5'' x 0.35''		
Price: (1-4)	J	K		
	\$675.	\$950.		

² Logic supply utilizes separate connection, to allow the user the convenience

of either C/MOS or TTL compatibility. *Specifications same as for Model ADC-12QL/J.



needs, it allows the systems engineer to make important savings in power source weight and volume. The ADC-12QL normally rests in a standby state. The converter is turned on by the convert command, fully stabilizes in a few microseconds; at the end of the conversion, it returns automatically to the standby state.

PIN DESIGNATIONS: ADC-12QL

		-		
PIN	FUNCTION	PIN	FUNCTION	
1	N.C.	A	BIT 1 (MSB)	
2	CLOCK	В	BIT 2	
3	EXTERNAL CLOCK CAP.	С	BIT 3	
4	STATUS	D	BIT 4	
5)		E	BIT 5	
65	N.C.	F	BIT 6	
7)		Н	BIT 7	
8	SERIAL OUT	J	BIT 8	
9)		K	BIT 9	
10		L	BIT 10	
11		м	BIT 11	
12	N.C.	N	BIT 12 (LSB)	
13		P 、	New Proventies	
14)		R		
15	SUPPLY GROUND	s>	N.C.	
16	N.C.	Т		
17	LOGIC SUPPLY	U /		
18	ANALOG INPUT	V	CONVERT COMMAND	
19	SIGNAL GROUND	W	N.C.	
20)		X	N.C.	
21	N.C.	Y	ANALOG SUPPLY	
22)		Z	N.C.	

ORDERING GUIDE: ADC-QL

MODEL ADC	12QL	X	XX
	Series	Gain Stability	Input Range
Converter Type	QL	J – 50ppm/°C K –20ppm/°C	+ 5 (V) $\pm 5 (V)$ +10 (V) $\pm 10 (V)$

MULTIPLEXER MPX-8A

	· C LSB 290
0 1 -15 ANA	LOG B 28 0
0 2 +15 DEVI	CESZA MSB 27 0
0 3 + 5 PASTORIZA D	IVISION MODE 26 0
O 4 GRD MADE IN L	ISA A OUT 250
0 5 CH 7 IN	ENBL 4 24 0
O & CH & IN	INV 3 IN 230
07 CH 5 IN	INV 3 OUT 220
0 8 CH 4 IN	ENBL 3 21 0
0 9 CH 4-7 OUT	INV 2 IN 20 C
0 10 CH 0-3 OUT	INV 2 OUT 190
O11 CH 3 IN	ENBL 2 18 0
012 CH 2 IN	INV 1 IN 17 C
013 CH 1 IN	INV 1 OUT 16 C
014 CH 0 IN	ENBL 1150
MULTIP	LEXER

GENERAL DESCRIPTION

The MPX-8A is an accurate high-speed 8-channel MOSFET multiplexer complete with versatile binary address control logic. It can be used either with A/D converters to acquire data from a number of sources, or with D/A converters to distribute data to a number of loads.

The control logic contained within the MPX-8A allows the user to connect the unit as either an 8-channel single-ended multiplexer, or as a 4-channel differential mode multiplexer. All of the logic needed to expand to up to 64 channels is also included.

SPECIFICATION SUMMARY (Typical $@+25^{\circ}$ C unless otherwise noted)

Model	MPX-8A	
Channels		
Single-Ended	8 ¹ , ²	
Differential	4	
Voltage Range		
Rated Operation	$\pm 10 V$	
Overload Protection	$\pm 15 V$	
Transfer Error	0.01%	
Settling to 0.01%	$<2\mu s$	
Cross Channel Coupling	<-80dB	
Common Mode Rejection		
DC	120dB	
60Hz	106dB	
Channel Addressing	Binary Code	
Address Logic	TTL Compatible/Positive True	
Power Requirement	+15V, ±1V @ 6.2mA	
	-15V, -1V, +0V @ 4mA	
	+5V, ±10% @ 102mA	
Package Style	C-1	
Package Dimensions	2" x 2" x 0.4"	
Price (1-9)	\$175.	

¹ Single-ended or differential operation is determined by jumper at module pins.

² MPX-8A includes logic for expansion to 64 channels.

MPX-8A B 280-00 9 CH 4 C 290-(LSB) 0 CH 7

LOGIC FLOW DIAGRAM

DR1 55	X +		Do		5 IN 6 CH 6
(IV T IN	L¥.		•D•		7 GH 5
CHAN	(MSR)		-Do		8 CH 4 O IN 10 CH 0- 3
A	270-00-00-00-00-00-00-00-00-00-00-00-00-0)	1P		-0 OUT -0 CH 3 11 IN
DER 01	21 18 20		P		O CH 2 12 IN
E XPAN	24 0				-0 ^{CH 1} 13 ^{IN}
MODE			-		14 IN
	20 0 INV IN 20 0 INV OUT			\sim	

SAMPLE-AND-HOLD AMPLIFIERS SHA-IA, 2A, 3, 4, 5, 6



SHA-5

The SHA-5 is a low cost general purpose sample-and-hold that offers good performance at a very low price. It settles to 0.01% in 15 μ s, and has a droop rate of only 5 μ V/ms.

SHA-6

The SHA-6 was designed as a companion to the high resolution ADC-16Q A/D converter. It will acquire a signal to 16 bit accuracy (0.00075%) in 5ms, and then hold it long enough for the ADC-16Q to convert it to a 16 bit digital word. It features excellent gain stability over both time and temperature.

GENERAL DESCRIPTION

Analog Devices' wide selection of Sample-and-Hold Amplifiers (SHA's) permits the selection of a SHA that is well suited for virtually any application. Each type offers a unique combination of speed, accuracy, and cost.

SHA-1A

The SHA-1A is a general purpose SHA offering moderately high speed and accuracy at a reasonable price. It settles to 0.01% in under 5 μ s, and its droop rate (decay when in HOLD) is no greater than 50 μ V/ μ s.

SHA-2A

The SHA-2A is a very fast Sample-and-Hold module with accuracy and dynamic performance that make it appropriate for use with very fast 12 bit A/D converters. It settles to 0.1% in less than 300ns, and to 0.01% in less than 500ns.

SHA-3 and SHA-4

These two SHA's were designed for high accuracy at longer hold times. They settle to 0.01% in 75μ s or less. The two differ in that when switched from HOLD to SAMPLE, the SHA-4 settles more rapidly than does the SHA-3.



ILLUSTRATION OF SPECIFICATIONS



PIN DESIGNATIONS: SHA-5

1. ANALOG GROUND	8. LOGIC GROUND
215V	9. N.C.
3. +15V	10. N.C.
4. N.C.	11. N.C.
5. N.C.	12. ANALOG OUTPUT
6. SIGNAL IN	13. NO PIN
7. CONTROL IN	14. N.C.

APPLICATIONS	General Purpose	Fast	Low Droop Slow Settle	Low Droop Fast Settle	Low Cost	High Resolution
Model ¹	SHA-1A	SHA-2A ²	SHA-3 ³	SHA-4 ³	SHA-5	SHA-6
Acquisition	5µs to	500ns to	75µs to	75µs to	15µs to	5ms to
Time	0.01%	0.01%	0.01%	0.01%	0.01%	0.00075%
Droop Rate	$50\mu V/ms max$	$10\mu V/\mu s$	$10\mu V/ms$	$10\mu V/ms$	$5\mu V/ms$	10mV/sec max
Input Range	±10V	±10V	±10V	±10V	±10V	±11V
Gain	1	1	1	1	1	1 to 1000
Gain Error	+0, -0.05%	+0, -0.01%	±0.01%	±0.01%	±0.01%	±0.2% ⁴
Input						
Impedance	$10^{12}\Omega$	$10^{11}\Omega$	10 ⁸ Ω	10 ⁸ Ω	$4 \times 10^9 \Omega$	10 ⁹ Ω
Aperture Delay	40ns	10ns	50ns	50ns	40ns	-1.7µs
Aperture						
Jitter	5ns	0.25ns	5ns	5ns	4ns	10ns
Power Require-						
ments ±15V @	15mA	100mA	15mA	18mA	25mA	17mA
Package Size	2" x 2" x 0.4"	2" x 3" x 0.4"	1 1/8" x 2" x 0.4"	1 1/8" x 2" x 0.4"	1 1/8" x 2" x 0.4"	2" x 4" x 0.4"
Package Style	C-1	C-2	C-4	C-4	C-4	C-3
Price (1-9)	\$150.	\$225.	\$95.	\$120.	\$47. (100+) \$32.	\$375.

SPECIFICATION SUMMARY (Typical @ +25°C unless otherwise noted)

¹Mode control input on all SHA's is TTL/DTL compatible. On all models except SHA-6, Logic "1" is sample and Logic "0" is hold. On SHA-6, Logic "0" is sample and Logic "1" is hold.

 2 SHA-2A may be used as a follower or inverter. It can also be used at gains higher than unity with appropriate degradation in bandwidth. 3 SHA-3 and SHA-4 differ only in that SHA-4 settles much faster when switched from HOLD to SAMPLE. Settling Time to ± 1 mV is 100 μ s for SHA-3 and 20 μ s for SHA-4.

⁴ Gain error from formula used to calculate value of gain resistor. Gain stability is ±0.0002%/month and ±0.0002%/°C.



SHA-1A

CONVERTERS 101

TRACKING SYNCHRO TO DIGITAL CONVERTERS SINGLE AND TWO SPEED

GENERAL DESCRIPTION

The "SDC" series converters are continuous tracking synchro or resolver to digital converters intended for military and industrial control applications.

Key to the small size and high reliability of the units is extensive use of monolithic analog switches, linear integrated circuits, MSI logic functions and thin film resistor networks.

The SDC series converters are highly accurate devices which are relatively insensitive to input amplitude variations, AC source excitation frequency variations, harmonic distortions and power supply variations. Accuracies, including all error sources, of ± 4 arc-minutes are achieved in the 14 bit version, and ± 30 arc-minutes in the 10 bit version, resulting from the basic ratiometric conversion technique and careful selection of IC components.

SINGLE SPEED 10 AND 14 BIT

Eight basic models are offered which cover the three primary variations which have a cost impact. These are 1) 14 bit or 10 bit resolution, 2) standard (SN) or extended (ET) operating temperature range, and 3) 400Hz or 60Hz.

The 400Hz units include the input isolating and scaling transformers within the module. Since 60Hz transformers are larger, they are packaged in a separate module, the associated converter module being less transformers.

# of Bits	Temp. range	Freq.	Converter	Transformers
14	SN	400Hz	SDC 1602	integral to conv.
14	ET	400Hz	SDC 1603	ı ıı
10	SN	400Hz	SDC 1604	" "
10	ET	400Hz	SDC 1605	" "
14	SN	60Hz	SDC 1606	plus SDC 1610
14	ET	60Hz	SDC 1607	- " "
10	SN	60Hz	SDC 1608	" "
10	ET	60Hz	SDC 1609	" "

TWO SPEED 10 BIT

These units are intended for use with electrically or mechanically coupled two speed systems for which they provide the coarse channel converter. For binary weighted systems, one module contains both a 10 bit S to D converter, plus a two speed processor and synchronizing logic. The number of bits used will be equal to the gear box ratio. Specifications of the 10 bit S to D portion are the same as the SDC 1604, 1605, 1608 or 1609. Gear Ratios available are 8:1, 16:1, and 32:1. Models are:

#	of Bits	Temp. range	Freq.	Converter	Transformers
	10	SN	400Hz	TSC 1611	integral to conv
	10	ET	400Hz	TSC 1612	<i>"" "</i>
	10	SN	60Hz	TSC 1613	plus SDC 1610
	10	ET	60Hz	TSC 1614	" "

TWO SPEED LOGIC

For non-binary gear ratios (9:1 and 36:1) a separate module is required in addition to two single speed S to D converters. This module includes only the two speed processor and synchronizing logic. There is a rounding down error to the closest binary ratio. The coarse converter provides either 5 bits (36:1) or 3 bits (9:1). A 19 bit two speed (36:1) system requires only three modules, a TSC, a 14 bit S/D and a 10 bit S/D. Models are:

TSL 1615	Std. temp.	non-binary	two speed logic	
TSL 1616	Ext. temp.	non-binary	two speed logic	



MODELS ¹	14 BIT UNITS	10 BIT UNITS
400Hz	SDC1602	SDC 1604 or TSC 1611
400Hz	SDC1603	SDC 1605 or TSC 1612
60Hz	SDC1606 plus SDC1610	TSC 1613 or SDC 1608 plus SDC 1610
60Hz	SDC1607 plus SDC1610	TSC 1614 or SDC 1609 plus SDC 1610
ACCURACY ² (max):	±4 arc minutes	±30 arc-minutes
RESOLUTION:	14 bits (1 LSB = 1.3 arc-minutes)	10 bits (1 LSB = 21 arc-minutes)
OUTPUT (in parallel):	14 bits natural binary angle	10 bits natural binary angle
IGNAL VOLTAGES: (Line-to-Line)		
Low Level	Synchro 11.8V rms L-L	•
	Resolver 11.8V rms L-L	•
High Land	Resolver 26.0V rms L-L	•
High Level	Synchro 90.0V rms L-L	
	Resolver 115 OV rms L-L	
IGNAL IMPEDANCE:	Resolver 119.0 v mis E E	
Low Level	20k ohms L-L Balanced	•
High Level	200k ohms L-L Balanced	•
EFERENCE VOLTAGE:	4 19 10	
Low Level	26V rms 400Hz or 60Hz as appropriate	*
High Level	115V rms 400Hz or 60Hz as appropriate	*
REFERENCE IMPEDANCE:		
Low Level	20k ohms	*
High Level	200k ohms	*
RANSFORMER ISOLATION:	500VDC	•
RACKING RATE:	1440°/second	•
CCELERATION:	180°/sec ² for 1 LSB Error	•
TEP RESPONSE (179°/step):	300 milliseconds for 1 LSB Error	*
OWER SUPPLIES ³ :	+15V at 40 milliamps -15V at 40 milliamps + 5V at 200 milliamps	+15V at 30 milliamps -15V at 30 milliamps + 5V at 150 milliamps
OWER DISSIPATION (max)	2.5 Watts	2 0 Watts
OGIC OUTPUTS	DTI /TTI Compatible	*
Solie Corrers	Fan out: four TTL Input Loads	
CONVERTER BUSY	Positive Pulse 2 Microseconds	
	Duration During Output Update	*
NHIBIT	DTL/TTL Compatible	*
	Fan in one TTL Input Load	•
EMP. RANGE OPERATING: SDC1602, SDC1604, SDC1606	0 to +70°C (standard)	· · · · ·
SDC 1608, TSC 1611 and TSC 1613 SDC1603, SDC1605, SDC1607, SDC 1609, SDC 1610, TSC 1612	-55°C to +105°C (extended)	
and TSC 1614	55° C	
EMP. KANGE STORAGE (all)	-55 C to +125 C	•
VARM UP:	5 minutes to rated accuracy	*
All (average SDC1 (10)	2 1 2 5" * 2 6 2 5" * 0 9"	
SDC1610	3.125 x 2.625 x 0.8 1.5" x 3.125" x 0.9"	•
/EIGHT:	7 oz. (200gm)	*
RICE (1-9)	SDC1602 - \$680	SDC1604 - \$480
	SDC1603 - \$775	SDC1605 - \$540
	SDC1606/SDC1610 - \$730	SDC1608/SDC1610 - \$530
	SDC1607/SDC1610 - \$825	SDC1609/SDC1610 - \$585
		TSC 1611 - \$635
		TSC 1612 - \$735
		TSC 1613/SDC 1610 - \$685

NOTES: 1.

2.

Nominal 60Hz units operate over range of 50 to 400Hz. Accuracy applies over the operating temperature range and for 3.

14 bit units will operate down to ±12VDC 10 bit units will operate down to ±10VDC

±10% signal & reference amplitude variation (a) (b)

 \pm 10% reference frequency variation 10% signal and reference harmonic distortion (c)

(d) ± 5% power supply variation

ANGLE POSITION INDICATOR API 1617

GENERAL DESCRIPTION

The API 1617 is an angular position indicator that provides a LED readout (and a BCD or binary output) of angles from 0° to 359.98° with 0.02° resolution and 0.05° error, at tracking speeds up to 1440°/second.

The API 1617 utilizes a modular approach in its design which includes separate plug-in modules for the 14 bit binary tracking synchro-to-digital converter and the binary to BCD converter.

The synchro (or resolver) input is dedicated to a particular signal/reference voltage range and frequency, by selection of an appropriate SDC 1602 or SDC 1606/SDC 1610. Versatility may be gained by purchasing additional SDC modules to match other expected input types and ranges.

The 5 digit BCD display may be specified in either degrees and decimal fractions of degrees or degrees and minutes. The BCD digital output matches the selected display coding, or may optionally be the original 14 bit binary data.

Accuracy of the unit is maintained over 10% variations of signal/reference amplitude and frequency variations and 10% signal/reference harmonic distortions. The unit's accuracy is also maintained over its operating temperature range. There is no warm-up drift. The basic S to D converter needs no adjust-

ORDERING GUIDE

API 1617

The user must specify three items when ordering: I) specific SDC to be used; II) type of display and III) type of digital output.

- I) A. Select either an SDC 1602 (400Hz) or SDC 1606/ SDC 1610 combination (60Hz).
- I) B. Specify SYNCHRO or RESOLVER input.
- I) C. Specify signal voltage level from the API 1617 SPECIFICATION table.
- II) Specify display in degrees and decimal fractions of degrees or display in degrees and minutes.
- III) Specify digital outputs as BCD or binary. (The BCD outputs will match the selection in II above.)



ment, consequently no potentiometers are included in the unit.

Since the API 1617 uses a continuous tracking technique it does not require an external convert command pulse to make it operate. However, it may be externally controlled and the logic necessary to this is built in. A "converter busy" pulse is made available to allow external gating. An externally applied "converter inhibit" command will free the data, while a "display enable" command will output the data.

BDM 1618

Included within the API 1617 is a 14 bit binary to five decimal digit converter, the BDM 1618. This module is available as a separate item for those applications where the user may wish to package his own display of synchro data. It is also used in those applications where synchro or resolver data must be converted and presented in BCD form.

Two options are available on the BCD output data; either degrees and decimal fractions of degrees (359.98°) or degrees and minutes $(359^{\circ} 59')$. In the fractional degree version, there is a slight rounding off error since 14 bits binary is equivalent to 0.02° and a 15 bit binary S to D converter would be required for 0.01°

SPECIFICATION SUMMARY (Typical @ +25°C and nominal line voltage.)

	0	
Accuracy	±0.05°	
Resolution	±0.02	
Display	5 digit 5x7 dot matrix LED	
Angle Range	000.00° to 359.98° continuous rotation	
	or	
	000°00' to 359°59' continuous rotation	
Tracking rate	1440°/sec	
Synchronizing time	300 milliseconds	
Signal Voltages: (line-to-line)		
Low Level	Synchro 11.8V rms L-L	
	Resolver 11.8V rms L-L	
	Resolver 26.0V rms L-L	
High Level	Synchro 90.0V rms L-L	
	Resolver 90.0V rms L-L	
	Resolver 115.0V rms L-L	
Signal Impedance:	N TO THE REPORT	
Low Level	$20k\Omega$ L-L balanced	
High Level	200 k Ω L-L balanced	
Reference Voltage:		
Low Level	26V rms 400Hz or 60Hz as appropriate	
High Level	115V rms 400Hz or 60Hz as appropriate	
Reference Impedance:		
Low Level	20kΩ	
High Level	200kΩ	
Transformer Isolation:	500VDC	
AC Line Input:		
Voltage & Power	115V rms ±10% @ 30VA	
Frequency	45 to 450Hz	
Control	Front Panel on/off	
Digital Signals	DTL/TTL compatible	
Converter Inhibit	"0" = track "1" = hold	
Converter Busy	"0" = data stable "1" = busy	
Display Enable	"0" = up-date (follow) "1" = hold	
Outputs	5 BCD decades or 14 bits binary	
Temperature Range	$0 \text{ to } +50^{\circ}\text{C}$	
Size	10.50" deep x 9.49" front panel width x	
	1.74" front panel height	
Price	(1-9) (10-24)	
API 1617	\$1645 \$1563	
BDM 1618 only	\$ 355 \$ 340	

DIGITAL TO SYNCHRO CONVERTERS

GENERAL DESCRIPTION

These units are continuously updating digital to synchro (or resolver) converters intended for military or industrial control applications. The converter accepts a 14 bit natural binary angle and converts this into sine/cosine format for resolvers or 3 wire synchro format.

For 400Hz operation the output isolation or Scott-T transformers are included within the module. For 60Hz the transformers are supplied in a separate module. Sufficient power (approximately 2W) is available to directly drive most control transformers, a high power Scott-T is available for heavier loads. Two speed processors are also available for two speed D to S systems. Accuracy of ± 5 minutes is maintained over the operating temperature range, $\pm 10\%$ reference amplitude and frequency variation, 10% reference harmonic distortion and $\pm 5\%$ power supply variation; in any combination. ET versions are available for operating.

ORDERING GUIDE

- 1. Specify basic model number.
- 2. Specify SYNCHRO or RESOLVER output.
- 3. Specify output voltage level per SPEC SUMMARY.

SPECIFICATION SUMMARY (Typical @ +25°C and nominal power supplies, unless otherwise noted.)

±5 arc-minutes
includes variations as noted
above in general description
14 bits $(1LSB = 1.3 \text{ arc-minutes})$
11.8V rms L-L Synchro or
Resolver
90.0V rms L-L Synchro
100Ω L-L balanced @ 11.8V rms
5500Ω L-L balanced @ 90V rms
26V rms for 11.8V outputs into
20kΩ
115V rms for 90V outputs into
200kΩ
±15V at 160mA ave, 700mA peak
+5V at 200mA
DTL/TTL compatible @ 2 TTL loads
0 to $+70^{\circ}$ C (standard)
-55° C to $+105^{\circ}$ C (extended)
3.125" x 2.625" x 0.8"
4.4" x 1.5" x 1.9"
\$535
\$635
\$585
\$685

MULTIPLEXED SYNCHRO TO DIGITAL CONVERTERS

GENERAL DESCRIPTION

The SSD series of modular converters are intended for use with multi-channel time shared synchro and/or resolver inputs in avionic and marine applications. The SSD series is designed for easy expansion to a 48 channel system by adding functional input modules which feed a single converter. The functional blocks are:

- 1. a signal isolation transformer, dual sample and hold with multiplexer.
- 2. reference isolation transformer, peak detector.
- 3. 14 bit binary resolver to digital converter.

Inputs to the system may be either high or low level synchros, or low level resolvers, 400Hz or 60Hz. Different references may be handled by adding a reference transformer/peak detector for each reference powering a set of synchros or resolvers. 400Hz and 60Hz modules may be intermixed in a given system.

THEORY OF OPERATION

All channels are simultaneously sampled on the peak of the reference waveform. The signal transformer isolates the inputs (synchro or resolver) and provides two outputs in V_P sin wt sin θ and V_P sin wt cos θ form. These outputs feed two high speed sample and hold amplifiers (one each for sin θ and cos θ) per signal input. When in hold, the S/H outputs are then multiplexed (either sequentially or random access) into a common converter. The resolver to digital converter is a high speed successive approximation type.

SPECIFICATION SUMMARY (Typical @ +25°C, unless

otherwise noted.)	
Accuracy (min)	±4 minutes of arc ±0.9 LSB
Resolution	14 Bits
Output	14 Bits of natural parallel binary angle
Input	3 wire synchro 11.8V L-L rms
	3 wire synchro 90V
	2 wire resolver 26V rms
Reference	26V rms
	115V rms
Convert Command	Positive pulse, 100ns wide, min
	Leading edge ("0" to "1") resets
	previous data
	Trailing edge ("1" to "0")
	initiates conversion
Conversion Time (max)	50µs
Conversion Time (min)	Up to 48 conversions per cycle or
	19200 conversions per second
Channel Access	Random or Sequential
Acquisition Time (max)	50µs
Sampling	At reference peaks
Logic Levels	TTL/DTL Levels
Temperature Range	$0 \text{ to } +70^{\circ} \text{C or } -55^{\circ} \text{C to } +125^{\circ} \text{C}$
Power Supplies	±15VDC and +5VDC
Power	4 Watts

ORDERING GUIDE:

SSD 1627 Isolation, dual S/H, std temp 400Hz, \$200
SSD 1628 Isolation, dual S/H, ext temp 400Hz, \$275
SSD 1629/SDC 1610 Isolation, dual S/H, std temp 60Hz, \$250
SSD 1630/SDC 1610 Isolation, dual S/H, ext temp 60Hz, \$325
SSD 1631 Ref. trans., peak detector, std temp 400Hz, \$200
SSD 1636 Ref. trans., peak detector, ext temp 400Hz, \$275
SSD 1632/SDC 1610 Ref. trans., peak detector, std temp 400Hz, \$275
SSD 1632/SDC 1610 Ref. trans., peak detector, std temp 60Hz, \$250

SSD 1637/SDC 1610 Ref. trans., peak detector, ext temp 60Hz, \$325

SSD 1633 14 bit resolver to dig. conv., std temp, \$625 SSD 1634 14 bit resolver to dig. conv., ext temp, \$875


DIGITAL PANEL METERS

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DIGITAL PANEL METERS

INTRODUCTION

Today's digital panel meters (DPM's) are extremely useful and valuable components for making precise electrical measurements. They are capable of providing accurate, unambiguous readouts which satisfy a wide range of application requirements for test and laboratory instrumentation. The availability of digital output signals in some DPM designs extend their usefulness in data acquisition systems where it is desirable to interface with data logging or digital control instrumentation.

GENERAL CONFIGURATION OF DPM's

A basic understanding of how a DPM works can give the user a firmer basis for the selection and application of DPM's. A DPM is basically an analog-to-digital converter with a visual readout. The DPM samples the input voltage, converts the voltage to a digital signal, and presents the data as a visual display and data interface outputs.

There are four functional sections in a digital panel meter: the input section, including the input signal conditioning and conversion circuitry, the display, the data outputs, and the power supply inputs.

Processing the Input Signal

The primary function of the input section is converting an input voltage to a digital signal for display. In many applications, the DPM must also reject noise picked up on input lines, measure the ratio of two voltages, or compensate for large variations in operating temperature. These requirements must be satisfied by design of the input section.

In its simplest form, the input section is only an analog-todigital converter with a single-ended input. The dual slope converter used in most high accuracy DPM's provides normal mode rejection of high frequency noise by averaging the input signal over a fixed sampling period. By adjusting the averaging period to line frequency, very high rejection of power line noise can be achieved. The staircase converter sometimes used in lowresolution, low-accuracy, low-cost DPM's requires RC filtering of the input signal to provide normal mode noise rejection.



DPM Simplified Block Diagram

To further reduce the noise picked up on signal lines, one can isolate the input of the DPM with a differential input amplifier. Signals appearing on both input leads simultaneously will be attenuated by the common mode rejection ratio. Besides reducing noise, a differential input allows measurement of differences between two voltages as required in bridge or balanced circuits.

Reduction in the effects of ground loops can be made by isolating the analog and digital sections of the DPM. Optical or transformer isolation of the digital control logic and transformer coupling the DC to DC converter power supply section results in a fully floating analog section. The use of such techniques provides high quality isolation between the analog input section and the display and BCD output registers, and very large (>300V) common mode voltages can be accommodated.

Dual slope converters compare the input voltage to a stable reference voltage generated in the input section. By providing an external input for the reference voltage, the input can be compared to any user supplied reference, and the meter reading will be a function of the ratio of the two voltages.

To preserve the accuracy of the DPM over changes of time and temperature, one must correct for zero offset and gain drifts. Automatic zero correction circuitry can be designed into the DPM to reestablish the correct zero level between each measurement. Careful component specification and selection can greatly reduce aging and temperature effects.

Displaying the Data – Which Display for the Job?

Once the input signal has been processed into digital data bits, it is decoded and displayed for visual readout. Numerous types of displays are available today, including liquid crystal, gas discharge (e.g. Sperry), light-emitting diode (LED), or incandescent (e.g. RCA Numitron). Although liquid crystals have very low power requirements, they do not have good readability in all conditions and Analog Devices feels that their reliability has not yet been proven sufficient for DPM applications. LED's are extremely rugged and reliable. The availability of LED displays integrated with MSI counters and latches simplifies DPM design, enhances reliability and allows extremely small DPM packages. The 0.27" character size of these LED displays makes them easily readable for bench-top or other close-in operating conditions (less than 8'), under normal ambient lighting.

The large Sperry and Numitron displays are the most visible, being easily readable at distances of 10 feet or more even in high ambient light conditions. Sperry displays require high voltage and are, therefore, generally used in AC line-powered DPM's. The Numitron display works well with logic-powered DPM's, and their "white" light output allows filtering for color coded displays.

Producing Digital Outputs

Since the data display is decimal, DPM's use binary-coded decimal (8421 BCD) counters in the conversion circuitry. For display simplicity, the data outputs are usually available parallel, that is all BCD data bits are available simultaneously on separate lines. Although serial data makes wiring simpler (you need 13+ lines for 3½ digits BCD parallel, versus 2 lines for BCD serial), decoding of the data must be done at the receiving end of the serial line, increasing circuit complexity. If serial data is desired, Analog Devices' new serial control modules (see New Products Section) can provide for conversion to serial data as well as providing interfaces to teletypes and other data terminals.

Data outputs can be unlatched, latched, or buffered. Unlatched outputs are taken directly from the counter in the converter circuit, and erroneous data will be present on the data lines during conversion. Unlatched outputs simplify circuitry and are perfectly adequate if proper care is taken in interfacing these outputs.

Latched outputs accept the data from the converter section and hold the data for display and processing during the next conversion. At the end of each conversion, the data being held in the latches are updated. Latched outputs simplify processing since the data are available during relatively long time periods and no noise is present on the data lines during conversion.

Buffered outputs are similar to latched outputs except the output data is gated onto the data lines by an external "STROBE" signal. Buffered outputs make multiplexing of digital data easier, since many devices can share common data lines and each can be gated onto the lines sequentially. However, buffered outputs require gates for each data output line to allow strobing data, requiring, for example 17+ AND gates for a 4½ digit DPM. The added circuit complexity and cost can rarely be justified for a DPM, and is not often used.

Output data and control inputs are commonly DTL/TTL compatible since DTL/TTL is the most widely used digital logic. Future DPM's will require COS/MOS compatibility.

Powering the DPM

Line Power or Logic Power? Analog Devices pioneered the design of +5VDC logic-powered digital panel meters. By operating the DPM from the +5V power supply commonly available in today's instrumentation, the size, weight, and cost of the meter can be greatly reduced, and the DPM can operate in a cooler environment. In addition, DPM's using line power often require shielding of the low level inputs from AC power lines, especially in designs using a common terminal connector for inputs, logic signals, and AC power. Even operational testing is safer, since no AC line voltage is present on the panel.

However, 5VDC powered DPM's may draw 0.5 to 1.5A current from the instrument power supply. In addition, the current required by the display can vary by a factor of 3 in extreme cases (all 1's to all 8's) requiring a power supply with good transient regulation. If sufficient +5VDC power is not available or power supply regulation cannot prevent interactions with other system logic, an AC line powered DPM may provide easier integration into the measurement system.

A Word About Reliability and Quality

A highly competitive market has brought about greatly reduced DPM prices leading to their widespread usage in scientific and medical instrumentation, industrial control equipment, environmental systems, and aerospace and military systems which require extremely high reliability. A DPM must, therefore, be designed for low cost but not at the expense of reliability.

Designing a unit for high reliability and competitive cost requires devising simple circuits with a low parts count and making extensive use of high-reliability integrated circuits. The use of aluminum cases rather than plastic provide better heat transfer and lower operating temperature. Analog Devices uses high-volume buying and manufacturing techniques as well as utilizing in-house components to further lower cost without sacrificing quality and reliability.

Good quality assurance includes incoming inspection of components and selection and grading of components in a controlled environment. Continuous visual and electrical inspections and tests are conducted during production. Final testing and calibration are followed by a long burn-in period to insure that all DPM's meet our exacting requirements for performance and reliability.

WHICH METER FOR THE APPLICATION – DIGITAL OR ANALOG?

With the new low costs for DPM's, it is reasonable to consider DPM's for new instrument designs which previously used analog displays. Described below are several benefits to be gained by selecting a DPM for the design.

First the digital display is completely free of ambiguity or interpolation errors. Even the most unskilled personnel can accurately read the large digital display. Secondly, it is not necessary for the operator to be close to or directly in front of the meter, thereby avoiding parallax errors. DPM's can be easily read at distances of 10-30 feet or more as well as over wide viewing angles. The high resolution and large dynamic signal range of a DPM is also important. An analog meter will require considerable range switching to equal the performance of a 3½ or 4½ digit DPM. The resolution of a DPM can conveniently extend the useable range of measurements and accuracy of instruments formerly limited by the resolution of analog meters.

The all solid state input circuitry of a DPM also provides several other distinct advantages. Because the DPM uses solid state input circuitry and feedback techniques, high input impedances (above 100 Megohms) are easily achieved and source loading errors are thereby avoided. Input bias currents are typically below 100 nanoamps. However, it is not uncommon for a high accuracy analog meter to draw 0.1-1mA of source current at full scale. At this level, unless a low impedance signal source is available, source loading errors can become significant and a high input impedance op amp may be required to reduce loading errors. The complexity of the meter installation increases significantly, thereby defeating the analog meter's asset of application simplicity.

The DPM's fast conversion rate and its ability to be externally triggered makes multiplexing of several inputs to one meter an easy task. Interfacing the BCD data outputs to a line printer can eliminate the need for any manual data logging. These outputs may also be used as parts of a digital loop for sensing signal levels and controlling instrumentation digitally.

The physical size of the DPM is now an advantage. A 0.5% (2½ digit) DPM requires only a 3" x 2" panel space; a d'Arsonval meter of equivalent resolution requires a scale length of about 7" and about 7" x 6" of front panel space. The all solid state DPM circuitry makes for a very rugged component, thus modern-day requirements for small size, light weight, ruggedness and portability often dictate the use of a DPM.

Are Digital Meters Always the Best Choice? – Other Considerations

One cannot draw the conclusion that DPM's are always a better choice than analog meters. The lowest cost DPM's are still in the \$50 price range and many applications require low cost, low resolution meters out of the DPM range. And in many applications, an experienced operator can derive much useful information from the "acceleration" and fluctuations of the pointer of an analog meter. Anticipatory adjustment and control often hinges on estimating rate and acceleration, making an analog display mandatory in such circumstances.

The electronic nature of the DPM can also negate its usefulness in some applications. The IC circuits require a separate power supply (+5VDC or 115VAC) which may not be easily available in the instrument design. Installing an analog meter in a circuit is quite easy, whereas the possible circuit interactions of a DPM (such as ground loops and digital noise) require more careful circuit design.

SELECTION OF A DPM

To select the proper DPM, one must review the design requirements of the application. This review should include a characterization of the input signal: its range, polarity, resolution, and accuracy required, whether any common mode voltage is present, and if noise pickup may be a problem. Maximum viewing distance and viewing angle may dictate the type of visual display required. Is +5 VDC logic power available or is a linepowered unit necessary? Are data outputs required for data logging or feedback control?

Once the required specifications of the application have been identified, they must be compared to the specifications provided by the DPM manufacturers. Since no industry standards for DPM specifications exist, it is very important to understand how a manufacturer defines his particular specifications. The checklist below can be used as a guide to the proper selection of a DPM.

Selection Checklist

WHAT PERFORMANCE IS DESIRED? What resolution and accuracy are required? These specifications will determine the number of display digits and the level of accuracy need. A 2¹/₂ digit meter can be used to replace most analog meters, a 3¹/₂ digit DPM is usually adequate for general purpose applications, and a 4¹/₂ digit DPM provides high resolution capability.

WHAT INPUTS ARE TO BE MEASURED? The designer must know the range of voltages to be measured, bipolar or unipolar, the source impedance, what common mode voltage must be accommodated (if any), and if ratiometric measurements must be made with respect to external reference voltages.

ARE ENVIRONMENTAL CONDITIONS HARSH? If the DPM is to be used in a noisy electrical environment, good CMR and NMR are necessary. A large range of operating temperatures requires a good temperature coefficient.

WHAT INPUT POWER IS AVAILABLE? Will the DPM share the +5VDC power supply used for other logic circuitry or will a separate +5VDC power supply be needed? Are there limitations on power drain? Is only AC line power available? Is signal and power line ground isolation necessary?

WHAT DISPLAY TYPE IS DESIRED? Must the display be large enough to be read from a long distance? Is color coding necessary? Is ruggedness a factor? Is ambient light level high?

IS PACKAGE SIZE CRITICAL? Is there any restriction on the size of the DPM, either in panel space or depth? Is internal heat rise critical, as in small portable instrument designs? ARE DATA OUTPUTS NECESSARY? If automatic data logging is desired or if external feedback control, via a data link, is part of the design, then BCD digital data outputs from the DPM must be available for interfacing to other system circuitry. Are latched outputs needed? Are the proper logic levels available? Is conversion speed adequate for the system? Is logic ground isolation required?

Understanding Performance Specifications

Currently, there are no industry standards on DPM specifications, and comparing specifications of DPM's from different manufacturers may require some analysis. A section of DPM specification definitions has been included, but an elaboration on several of these is included below to help in understanding fully how specifications relate to performance requirements.

Resolution, Accuracy, and Stability - - these three specs are very important in the selection of a DPM. Although more digits may mean more resolution, the digits themselves are useless unless the accuracy is sufficient for the digits to have real meaning. Therefore, accuracy and resolution should be comparable.

Independent of temperature, there are three components which lead to DPM inaccuracies. They are zero offset error, gain error, and digital indecision. In any device using a counter and clock to determine a digital output, there is always a potential ± 1 count error in the output. This is caused by the timing of the input gate of the counter; when the gate closes asynchronously with the clock, a clock pulse that occurs just as the gate closes may or may not be counted, hence the fixed ± 1 digit inaccuracy.

Zero level offsets in the analog circuitry cause errors specified as a percentage of full scale reading. These errors can be corrected by a zero calibration potentiometer requiring periodic resetting, or by internal calibration circuits that sense and set the zero level automatically between each reading, assuring no zero level contribution to the error.

Gain variations occur as a function of signal level in the analog circuitry and produce errors which are specified as a percentage of the reading. These are the hardest errors to design out of a DPM circuit, but they can be minimized by component specification and selection. A range adjustment potentiometer is used for periodic adjustment of the gain.

Since all the electronic components used in the design of a DPM have some temperature dependence, one can expect the accuracy of the DPM to be affected by changes in operating temperature. If automatic zero correction circuitry is not used, the zero level may drift with temperature. Variations in the reference voltage circuitry and its associated switches will cause changes in the gain of the DPM, but careful selection and matching of components can minimize this error.

Operational amplifiers used on DPM inputs typically use FET inputs which double their bias current for every +10°C rise in temperature. Analog Devices uses their own linear IC op amps with superbeta transistor inputs to reduce the bias currents and provide greater bias current stability. By providing a more stable input bias current, one can reduce loading errors.

To illustrate these specifications, consider a $3\frac{1}{2}$ digit DPM (1999 counts full scale). The resolution of the unit is the value of one digit, 1 part in 2000 or 0.05% of full scale. If the accuracy is comparable to the resolution (exclusive of digital indecision), the DPM should have a maximum error of $\pm 0.05\%$ ± 1 digit.

Temperature coefficient specifications for a DPM should be very good to maintain the accuracy. A tempco of only $50\text{ppm/}^{\circ}\text{C} (0.005\%)^{\circ}\text{C}$) will produce an additional error of $\pm 0.05\%$ over a range of only $\pm 10^{\circ}\text{C}$.

Since each manufacturer tends to use a different method of specifying accuracy and temperature coefficients, specifications must be expressed in common terms to be comparable. For example, one may find specifications for 3½ digit DPM's in the formats shown below.

- Unit 1: max error: ±0.05% R ±1 digit, tempco: ±50ppm(R)/°C
- Unit 2: max error: ±0.02% R ±0.03% F.S. ±1 digit, tempco: ±0.004%R ±0.001% F.S./°C
- Unit 3: max error: ±0.05% R ±0.05% F.S. ±1 digit, for temperature +15°C to +35°C

To compare the three units, one must establish a common ground: full scale reading, temp range $+15^{\circ}$ C to $+35^{\circ}$ C ($\pm 10^{\circ}$ C). The specification then becomes:

Unit 1:	$\pm 0.05\%$ F.S. ± 1 digit $\pm (50$ ppm(F.S.)/ C x ± 10 C)
	$= \pm 0.05\%$ F.S. ± 1 digit $\pm 0.05\%$ F.S.
	= 0.1% F.S. ±1 digit
Unit 2	±(0.02% F.S. ±0.03% F.S.) ±1 digit (0.004% F.S.
	$\pm 0.001\%$ F.S.)/°C x $\pm 10^{\circ}$ C
	= 0.05% F.S. ±1 digit ±0.05% F.S.
	= 0.1% F.S. ±1 digit
Unit 3:	±0.05% F.S. ±0.05% F.S. ±1 digit
	= 0.1% F.S. ±1 digit

Even though all units are specified differently, they have equivalent performance.

APPLICATIONS OF DPM'S

The ability of the DPM to provide accurate measurements over a wide range of voltage inputs has led to its widespread

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useage in instrumentation for medical, scientific, and industrial applications, as well as test instrumentation. When digital data outputs are provided, the DPM becomes a useful data acquisition element, providing data logging and feedback control as well as a visual output. Since the DPM input is easily scaled using attenuation or amplification, the DPM can be scaled to read directly in any engineering or physical units.

Typical Applications for DPM's Include:

• Medical, Analytical, and Scientific Instrumentation

Measuring:	Temperature	Reflectance & Transmittance
	Pressure	рН
	Power	Size
	Color Difference	Cardiac & Pulmonary Functions

- Systems Applications providing digital readout, automatic data logging, and digital feedback control
- Precision Differential Measurement

Described below are several applications illustrating the versatility and simplicity of DPM's for a wide variety of applications.

DIGITAL INDICATING MICROMETER: Linear variable differential transformers (LVDT) produce a DC output voltage proportional to the magnitude of a linear displacement. A typical LVDT may have a range of $\pm 1''$ and a maximum linearity error of $\pm 0.001''$. The typical output voltage varies 2mV/0.001''(2V/inch). By using a 3½ digit (199.9mV range) DPM such as the AD2003 or AD2010, and attenuating the LVDT output with a 20:1 voltage divider, the DPM will read directly in 0.001'' increments over the full range of the LVDT. The proper decimal point can be activated to provide direct readings in inches.



Digital Micrometer

DIGITAL WEIGHING PLATFORM SCALE: Platform transducers can be used to measure loads up to 1000 pounds. These transducers are stain gauge bridge units, typically producing 15mV at full scale loads with 10V excitation. By using an operational amplifier providing a gain of 6.67, 1000 pound load will produce a voltage of 100mV, measurable by a 3½ digit DPM (AD2003, AD2010). The readout will be directly in pounds.



Digital Scale

RATIOMETRIC MEASUREMENTS: Ratiometric operation allows readings to be normalized to an external reference. This is useful where the analog voltage to be measured is accurate relative to an external reference which in itself is not accurate. A ratiometric application is illustrated below using the AD2010/R. In this example, a position readout potentiometer operates with an external excitation supply which itself may not be very accurate. However, the potentiometer output relative to the reference supply will be accurate due to the potentiometer configuration.



Ratiometric Measurement

Circuit Application Guidelines for +5VDC Logic-Powered DPM's

The successful application of DPM's in an instrument design hinges on understanding the specifications and the interactions of the DPM with the rest of the instrument circuit. When developing circuit designs using DPM's operating from +5VDC, one should note the following:

Ground Loops: Correct grounding of a single-ended input DPM within the instrumentation system is essential for accurate readings. Since heavy supply currents (\sim 1A) flow through the power ground, under no circumstance should the input voltage be applied between the analog input and power ground. The voltage drop across even the few milliohms of contact resistance can produce erratic and variable offsets in the readings. Connections to power supplies should also be checked to insure that multiple ground connections are not causing ground loops. If shorting the inputs does not produce a zero reading, ground loops are most certainly present.

Power Supplies: Besides ground loops, power supplies can also affect DPM readings if there is noise present on the power

lines. If large noise spikes or large voltage variations are present, better filtering or regulation of the power supply may be necessary.

Digital Noise: Insure that all digital control lines (e.g. hold and trigger) connected to the DPM have a minimum of noise pickup. Noise on these lines can cause false triggering, prevent proper triggering, or affect the analog circuitry. If necessary, use coaxial cable for data lines to prevent noise pickup.

Attenuators: If an attenuator is used to scale the input signal to the DPM or to calibrate the readout in engineering or physical units, the attenuator network should be located as close as possible to the input terminals of the DPM. This avoids processing the attenuated signal over long lines, thereby reducing potential noise susceptibility.

Temperature Operating Range and Thermal Effects: DPM's can measure voltages with resolution as fine as 100μ V,

requiring consideration to be given to operating temperature. Input bias currents may change by several nA over the operating temperature range, but the effect on measurement can be minimized by keeping source impedance low (1nA through 10k Ω produces only a 10 μ V drop, <0.1 digit). Dissimilar metallic junctions in the wiring can produce thermocoupletype effects of up to 50 μ V/°C; especially be wary of electromechanical relays.

Common-Mode Interference: Stray pickup, input circuit impedance, line resistance, and shunt capacitance, if sufficiently unbalanced, can introduce common-mode errors even if the DPM has infinite CMR. Capacitance unbalance should be kept to a minimum; if needed, it can be further reduced by placing a shunt capacitor between the input at the meter.

More information on application of digital measuring devices to instrumentation systems can be found in Analog Devices' *Analog-Digital Conversion Handbook.*

DEFINITIONS-DPM TERMS AND SPECIFICATIONS

Accuracy (absolute): DPM's are calibrated with respect to a reference voltage which is in turn calibrated to a recognized voltage standard. The absolute accuracy error of the DPM is the tolerance of the full-scale set point referred to the absolute voltage standard.

Accuracy (relative): Relative accuracy error is the difference between the nominal and actual ratios to full scale of the digital output corresponding to a given analog input. See also: linearity.

Bias Current: The current required from the source at zero signal input by the input circuit of the DPM. Bias current is normally specified at typical and maximum values. Analog Devices' DPM's using transistor input circuitry are bias current sinks.

Binary Coded Decimal (BCD): Data coding where each decimal digit is represented by a group of 4 binary coded digits (called "quads"). Each quad has bits corresponding to 8, 4, 2, 1 and 10 permissible levels with weights 0-9. BCD is normally used where a decimal display is needed.

Common-Mode Rejection: A differential-input DPM will reject any input signals present at both input terminals simultaneously if they are within the common mode voltage range. Common mode rejection is expressed as a ratio and usually given in dB. (CMR = 20 log CMRR). 120dB of common-mode rejection (CMRR = 10^6) means that a 10V common-mode voltage is processed as though it were an additive-differential input signal of 10µV magnitude.

Common Mode Voltage: A voltage that appears in common at both input terminals of a device, with respect to its ground.

Conversion Rate: The frequency at which readings may be processed by the DPM. Specifications are typically given for internally clocked rates and maximum permissible externallytriggered rates.

Conversion Time: The maximum time required for a DPM to complete a reading cycle, specified for the full scale reading.

Dual-Slope Conversion: An integrating A/D conversion technique in which the unknown signal is converted to a proportional time interval, which is then measured digitally. This is done by integrating the unknown for a predetermined time. Then a reference input is switched to the integrator, and integrates "down" from the level determined by the unknown, until a "zero" level is reached. The time for the second integration process is proportional to the average of the unknown signal level over the predetermined integrating period.



Dual Slope Conversion

Input Impedance: The complex ratio of signal voltage to signal current at the input terminals. For DPM's, the input impedance is measured at DC.

Linearity: The conventional definition for nonlinearity of a DPM is the deviation from a "best" straight line which has been fitted to a calibration curve. Analog Devices, defines nonlinearity as the deviation from a straight line drawn between the zero and full scale end points. Not only is this an easier method for customer calibration, it is also a more conservative method of specifying nonlinearity.





Normal Mode Rejection: Filtering or integrating the input signal improves noise rejection of undesired signals present at the input. Normal mode rejection is expressed as the ratio of the actual value of the undesired signal to its measured value over a specified frequency range. (NMR (dB) = 20 log NMRR, e.g. NMR = 40 dB means an attenuation of 100:1).

Overload: An input voltage exceeding the full scale range of the DPM produces an overload condition. An overload condition is usually indicated by conspicuous manipulation of the display such as all dashes, flashing zeros, etc. On a 3½ digit DPM with a range of 199.9mV, a \geq 200mV signal will produce an overload condition.

Overrange: An input signal that exceeds full scale on a DPM, but is less than an overload. On a 3¹/₂ digit DPM with a full scale range of 199.9mV, full scale is 0-99.9mV, and signals from 100-199.9mV are said to fall in the 100% overrange region. Some DPM's have higher overrange capability. A 3¹/₄ digit DPM has a full scale range of 3.999 or 300% overrange.

Overvoltage Protection: The input section of the DPM must provide protection from large overloads. Specifications are given for sustained DC voltages that can be tolerated.

Range (Temperature Operating): The range of temperatures over which the DPM will meet or exceed its performance specifications, usually 0 to $+60^{\circ}$ C.

Range (Full Scale): The range of input signals that can be measured by a DPM before reaching an overload condition. A 3¹/₂ digit DPM provides three digits full scale and 100 percent overrange capability.

Ratiometric: DPM's compare voltage inputs to a stable internal reference voltage. In some systems, the voltage being measured is a function of another voltage, and accurate measurements should be made as the ratio of the two voltages. Some DPM's provide inputs for external reference voltages for ratiometric measurements.

Resolution: The smallest voltage increment that can be measured by a DPM. It is a function of the full scale range and number of digits of a DPM. For example, if a 3½ digit DPM has a resolution of 1 part in 2000 (0.05%) over a full scale range of 199.9mV, the DPM can resolve 0.1mV.

Digits	Counts (F.S.)	Resolution (% F.S.)		
21/2	199	0.5%		
31/2	1999	0.05%		
3¾	3999	0.025%		
41/2	19999	0.005%		
43/4	39999	0.0025%		

Staircase Conversion: A simple analog-to-digital conversion technique in which a clock and counter drives a digital-toanalog converter which produces an output voltage waveform resembling a staircase. A comparator stops the counter when the voltage exceeds the input voltage and the content of the counter is the digitized output.



Temperature Coefficient: The additive error term (ppm/°C or % Reading/°C) caused by effects of variations in operating temperature on the electronic characteristics of the DPM.

Unipolar Input DPM: A DPM designed to measure input voltages of only one polarity.

DIGITAL PANEL METERS AD2001, AD2002, AD2003, AD2004, AD2010

INTRODUCTION

In 1972, Analog Devices entered the digital panel meter market with a totally new concept: a DPM that operates off +5VDC power supplies commonly used for logic circuits. The user and application benefits of +5VDC powered DPM's have been well proven. In addition, input circuits were developed that sense and correct zero offset drift between each reading, providing more accurate DPM performance.

A GROWING PRODUCT LINE

But Analog Devices hasn't stopped yet. During 1972, five DPM models were introduced, covering most application requirements, and a continuing development program is underway to develop new products which combine those product features which satisfy the widest application needs of the industry.

WHY USE 5VDC POWER?

REDUCED NOISE PICKUP AND SUSCEPTIBILITY: Since line voltages are not required for operation, signal leads and internal circuitry need not be exposed to this source of noise, thereby, reducing power-frequency interference. A separate 5VDC power supply also provides additional isolation from line transients. Shielding and decoupling of the DPM circuits can also be eliminated. The DPM may be used as a component without danger of shock hazards to operational personnel or nearby circuitry.

IMPROVED RELIABILITY: Meters without power supplies generally require less space and generate less heat. The result is improved reliability while achieving lower cost. The smaller package size provides greater packaging flexibility and requires less ventilation behind the panel.

AN AWARD WINNING CASE DESIGN

All Analog Devices' DPM's except the AD2001 are packaged in similar cases, varying only in depth. The case is an aluminum extrusion with ABS plastic front and rear plates. The front plate has two panel retaining fingers on either side; the case snaps into the front panel and can be removed in seconds. A plastic lens assembly containing a colored filter snaps onto the case providing a very attractive front panel appearance. The filter can be screened with company logo or calibration units. *Industrial Design* magazine awarded the Analog Devices' DPM case an "Excellence of Design" Award in their 1972 Design Review Competition. The design was selected for its functional simplicity, flexibility, and overall aesthetic appeal.





AD2001, 3½ DIGIT, OEM APPLICATIONS, NUMITRON DISPLAY

The AD2001 is a 3½ digit panel meter designed for application in original equipment designs. The AD2001 was Analog Devices' initial entry into the DPM market, and it introduced the concept of logic-powered (+5VDC) DPM's.

The AD2001 has a bipolar, single-ended input with a range of 199.9mV and an accuracy of $0.05\% \pm 1$ digit. The AD2001 has a temperature coefficient of 50ppm/°C and automatic zero correction circuitry that never requires zero offset drift adjustment.

The digital readout is displayed on large, easily readable RCA Numitron seven-segment display tubes. Decimal points are externally programmable. The internal conversion rate is set at 5 conversions per second; rates from 20 conversions per second to an indefinite "hold" can be externally triggered.



AD2001 Simplified Block Diagram

AD2002, 2½ DIGIT, LOW COST ANALOG METER REPLACEMENT, NUMITRON DISPLAY

The AD2002 is a 2½ digit panel meter designed as a minimum cost replacement for updating new equipment designs formerly using analog meters. The staircase signal conversion technique used in the AD2001 requires fewer components and results in a low overall cost.

The AD2002 has a unipolar, single-ended input with a full scale range of 0 to 1.99V. The accuracy is $\pm 0.5\% \pm 1$ digit, and the temperature coefficient is 1/20 digit/°C.

The AD2002 display consists of green-filtered RCA Numitron seven-segment display tubes. Standard display features include filament test, programmable decimal points, automatic overload indication and a display rate of 4 readings per second. Up to 200 conversions per second are possible with an optional trigger and hold feature. The AD2002/DP option also provides parallel BCD data outputs on a multipin connector.



AD2002 Simplified Block Diagram

AD2003, 3½ DIGIT, HIGH PERFORMANCE, NUMITRON DISPLAY

The AD2003 is a high performance $3\frac{1}{2}$ digit panel meter with differential inputs. The differential instrumentation amplifier input provides 60dB common mode rejection, a common mode voltage of $\pm 2.5V$ and a normal mode rejection of 40dB.

The AD2003 accepts bipolar inputs in the range of 0 to ± 199.9 mV and has an accuracy of 0.05% ± 1 digit. Automatic zero correction circuitry corrects for zero offset drift, and the temperature coefficient is 50 ppm/°C.

The AD2003 displays the readings on green-filtered RCA Numitron seven-segment display tubes. The display also features polarity and overload indication, programmable decimal points, filament test, and a display rate of 5 readings per second. External triggering can adjust the rate from 16 readings per second maximum to an indefinite hold. Data outputs are latched, parallel BCD, DTL/TTL compatible.



AD2003 Simplified Block Diagram



AD2004, 4½ DIGIT, HIGH PERFORMANCE, ISOLATED INPUT, LED DISPLAY

The AD2004 is a high performance $4\frac{1}{2}$ digit panel meter designed for use in precision instrumentation and for processing critical signals in noisy electrical environments. Optical coupling is used to provide isolation for the signal channel, providing 120dB of common mode rejection at common mode voltages of up to ± 300 V.

The isolated input section can measure voltages in the range of 0 to $\pm 1.9999V$ with an accuracy of $\pm 0.01\% \pm 1$ digit. Automatic zero correction circuitry corrects for zero offset drift errors and the temperature coefficient is $15 \text{ ppm/}^{\circ}C$. Readings are displayed on a red LED display with automatic polarity and overload indication. Normal conversion rate is 4 readings per second; external triggering can vary sampling

rates from a maximum of 8 per second to an indefinite hold. Decimal points are externally programmable. Latched, parallel BCD data outputs are DTL/TTL compatible.



Simplified Block Diagram

AD2010, 3½ DIGIT, GENERAL PURPOSE, LED DISPLAY, RATIOMETRIC OPTION

The AD2010 is a general purpose $3\frac{1}{2}$ digit panel meter that sets new standards for size, price, and performance. The LED display, +5VDC power requirement, and innovative packaging permit a package size requiring only $3'' \ge 1.8''$ panel space and only $\frac{34''}{4}$ depth.

The AD2010 has a bipolar, single-ended input with a range of 199.9mV and an accuracy of $\pm 0.05\% \pm 1$ digit. The design offers 60dB of common mode rejection at common mode voltages up to ± 200 mV.

The AD2010 has a red LED display with leading zero suppression and programmable decimal points. Normal display rate is 4 readings per second or external triggering can vary rates from a maximum of 24 per second to an indefinite hold. The AD2010 can also be connected for automatic operation at its maximum conversion rate. Latched BCD data outputs are available for data logging or digital feedback control.

The AD2010/R option includes ratiometric input to allow inputs to be referenced to an external voltage source. The ratiometric option also includes a normal mode rejection optomization adjustment that increases NMR to 60dB.



Model		AD2001	AD2002	AD2003	AD2004	AD2010
Resolution (digits) and Range	2½ (1.99V) 3½ (199.9mV) 4½ (1.9999V)	•	•	•	•	•
Input Type	Single-Ended Differential Ground Isolated Unipolar Bipolar	•	•	•	•	• • ¹
Display	Numitron LED	•	•	•	•	•
Data Outputs	Parallel BCD Parallel BCD, Latched	•	• ²	•	•	•
Connector	PC Card Multipin	•	•	•	•	•
	Low Cost Analog Replacement General Purpose Instrumentation Amp Input	•	•	:	•	:
Applications	High Noise Immunity Ground Isolation Off Ground Measurements Ratiometric Measurements High Visibility Display (>8-10' & high ambient light) Extremely Rugged Display	•	•	•	•	•

CAPSULE SELECTION GUIDE DIGITAL PANEL METERS

 1 Limited Differential Input – CMR 60dB, CMV ±200mV 2 With DP Option

SPECIFICATION SUMMARY (Typical @ +25°C unless otherwise noted)						
Model	AD2001	AD2002	AD2003			
Display						
Number of Digits	31/2	21/2	31/2			
Type	Numitron	Numitron	Numitron			
Overload Indication	Zero's + "1" Flashes	Dashes	Dashes			
Decimal Points	Selectable at Input	Selectable at Input	Selectable at Input			
Filament Test	selectable at input	Ves	Ves			
Inament rest		105	105			
Turc	Single and ad	C 1 1 1	D'00			
Type Zaro	Single-ended	Single-ended	Differential			
Zero	Automatic	Automatic	Automatic			
Polarity	Bipolar	Unipolar	Bipolar			
Full Scale Range	$0 \text{ to } \pm 199.9 \text{mV}$	0 to +1.99V	$0 \text{ to } \pm 199.9 \text{mV}$			
Bias Current	<1nA	70nA typ/250nA max	3nA typ/7nA max			
Impedance	1000MΩ	>100MΩ	>100MΩ			
Overvoltage Protection w/o						
damage (sustained)	±20V	±50V	±50V			
Accuracy						
Maximum Error of Reading	0.05% ±1 Digit	0.5% ±1 Digit	0.05% ±1 Digit			
Resolution	0.1mV	10mV	0 1mV			
Temperature Range Operating	0 to $+60^{\circ}$ C	0 to $\pm 60^{\circ}$ C	$0 \text{ to } \pm 60^{\circ} \text{C}$			
Temperature Coefficient	± 50 ppm/°C	$1/20 \text{ Digit/}^{\circ}C$	<+50mm/°C			
Sneed		1720 Digiti C	C-Joppini C			
Internal Conversions/see	5					
External Conversions/sec	20	4 200 ((DB O)	3			
Hold & Bood on Command	20	200 (W/DP Option)	16			
Hold & Read on Command	Std	w/DP Option	Std			
Interface Signals						
(DTL/TTL Compatible)						
Inputs						
Externally Triggerable	Std	DP Option	Std			
External Hold	Std	DP Option	Std			
Outputs						
BCD Digits	Std	DP Option	Std, Latched			
Overrange Signal	Std	DP Option	Std. Latched			
Overload Signal	Std	DP Option	Std Latched			
Status Signal	Std	DP Option	Std Latched			
Polarity Signal	Std	User Programmable	Std.			
Connector	DCP	Maltinin (DD Ontine)	Multini			
Connector	PCB	Multiple (DP Option)	Multipin			
Normal Mode Rejection						
(@50-60Hz)	40dB	Requires Filter	>40dB			
Common Mode Rejection						
(DC-1kHz w/1k Ω unbalance)	N/A	N/A	>80dB			
Common Mode Voltage	N/A	N/A	±2.5V			
Power (+5VDC)						
Regulated ±5% (converter)	200m A	250-	250-4			
Uppergulated ±10% (display)	2001114	230mA	250mA			
Onregulated ±10% (display)	800mA	SOOMA	750mA			
Warm Up To Rated Accuracy	Essentially none	Essentially none	Essentially none			
Adjustments	Range Potentiometer	Range Potentiometer	Range Potentiometer			
Size	3"W x 1.75"H x 1.5"D	3"W x 1.8"H x 1.5"D	3"W x 1.8"H x 2"D			
Case Mounting	Bezel	Snap-In	Snap-In			
Price						
(1-9)	\$135	\$75	\$140			
(100's)	89	50	93			
Ontions						
Options		AD2002/DP, Data	AD2003/E, SOHZ NMR			
Options		AD2002/DP, Data Outputs	Optimization (NC)			
Options		AD2002/DP, Data Outputs (\$83, 1-9 each)	Optimization (NC)			

AD2004	AD2010
41/	
472 LED	3½ LED
Flashing Zeros	Flashing Zeros
Selectable at Input	Selectable at Input
No	No
True Floating	Limited Differential
Automatic	Automatic
Bipolar	Bipolar
0 to ±1.9999V	0 to ±199.9mV
$>100M\Omega$	100MQ
	100/1122
±100V	±20V
0.01% ±1 Digit	0.05% ±1 Digit
0.1mV	0.1mV
0 to +60°C	$0 \text{ to } +60^{\circ}\text{C}$
<±15ppm/°C	<±50ppm/°C
4	4 (auto. 24-40/sec)
8	24
Std	Std
Std	Std
Std	Std
Std, Latched	Std, Latched
Sta	Std, Latched
Multipin	РСВ
Sode	ADdB (to 60dB on
>00dB	AD2010/R)
	MD2010/R)
>120dB	60dB
±300V (fully isolated)	±200mV
1.4A	600mA
N/A	N/A
5 min	Essentially none
Range Potentiometer	Range Potentiometer
	Normal Mode Rejection
Ро	tentiometer (AD2010/R Only)
3"W x 1.8"H x 2.5"D	3"W x 1.8"H x 0.75"D
Snap-In	Snap-In
\$269	\$120
189	79
AD2004/E, 50Hz NMR	AD2010/R, Ratiometric
Optimization (NC)	(\$135, 1-9 each)
	AD2010/E 50Hz NMR
	Untimization (NC)



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FUNCTION MODULES MULTIPLIERS/DIVIDERS

PRODUCT PROFILE

Multipliers from Analog Devices use solid state techniques to develop the transfer function +XY/10. Most models are capable of performing division according to the function +10(Z/X), hence the term multiplier/divider. Except for models 424, 530 and 531, all units are factory trimmed to guaranteed accuracies and require no further adjustments unless higher accuracies are required for the job. External trimming of offsets, feedthrough and scale factor terms may yield up to a two-fold improvement in accuracy.

Multiplier/Divider circuits are a fundamental system component. Despite their fundamental nature, the historical high cost and application complexity of multiplier/divider modules limited their use by OEM's. Recent developments have yielded multiplier modules which are internally trimmed for ease of application and greatly reduced price. These new multiplier designs have not only gained wide acceptance as fundamental system building blocks, but they also are making feasible for the first time more complex circuit functions.

During 1971, Analog Devices accelerated efforts toward the development of a full line of multiplier/divider modules for a wide range of applications. No fewer than seven basic models were introduced with performance characteristics ranging from complete 1% monolithic multiplier/dividers (model 530) to models with accuracies from 0.1% to 2%, wide bandwidths to 10MHz and low error drifts to 0.02%/°C.

With these seven models, Analog Devices offers the broadest multiplier/divider product line available. Our continuing development program will further expand the range of price and performance alternatives for your applications.

APPLICATIONS FOR MULTIPLIERS/DIVIDERS

Multiplier/divider modules are highly versatile in their application. They can be utilized to develop the following circuit functions:

- Squarer
- RMS Circuit
- Phase Sensitive Demodulator
- Modulator
- Phase Locked Loops
- Square Root
- AGC Circuit
- Vector Transformation
- Correlator
- Voltage Controlled Filter

In each particular application, there is usually a dominant and a secondary parameter which influence multiplier choice. For low frequency applications (DC to audio), which is by far the most common application class, overall accuracy and drift are key parameters. At frequencies beyond 100kHz, feedthrough and nonlinearity terms are key.

Since all multipliers from Analog Devices operate over four quadrants, signal polarity restrictions may be ignored. For divider and square root circuits, signal polarity and magnitude restrictions are placed on the inputs with operation restricted to two quadrants. Dividers also are subject to reduced accuracy and bandwidth because of the basic feedback circuit configuration: If the best performance is required for the divider, high accuracy multipliers are usually specified.

In general, each multiplier/divider requirement should be carefully studied to ascertain which features are critical and where tradeoffs may be made to assure best price/ performance. The following discussion is intended to assist the user in choosing the best multiplier/divider for his application, whether he be expert or newcomer in the use and selection of these devices.

For customer convenience, a selection guide for multipliers by key parameter, is listed below. The relevant model descriptions and specifications follow this section.

Key Feature	Multiplier Application	Multiplier Model
Highest precision, lowest noise & drift	Analog computation, dividers, servo multipliers, correlators	424, 427
Low drift, good accuracy, lower cost	Wide temperature range, general purpose multiply/divide	428
Bandwidth, accuracy	Graphic displays, dividers	429, 422
Wide dynamic divide range, accuracy	Root and power generation	427, 433
External trim for accuracy	R & D, medical, laboratory, analog computation	424, 425
Economy, size	OEM designs, general purpose multiply/divide	530, 426, 432, 53
MIL spec. available	Military grade design	530, 531, 432, 43

IRCUIT TECHNIQUES FOR DEVELOPING MULTIPLIERS

n discussing multiplier selection, it is appropriate to review everal of the more popular circuit techniques used with oday's solid state multipliers. A comparison table of these lternate techniques is presented below highlighting their espective capabilities in five key performance areas – nultiplier accuracy, stability, offset drift, bandwidth and lew rate.

As with most designs, the choice of circuit technique essentially determines the performance range of the nultiplier in each of the five specification areas. The user should carefully review these criteria to assure the best device for the job.

TRANSCONDUCTANCE MULTIPLIERS exploit a useful property of the bipolar transistor: namely, that the forward collector current and the transconductance are linearly related. In most designs, the X signal is internally attenuated to a low level, and applied to the base of a transistor, and the Y signal linearly modulates the value of a current source producing I_c , and thereby modulates the transconductance of the transistor. The result is a signal proportional to the product X • Y.

These multipliers can be made to exhibit good accuracy and bandwidth, are low in cost, and well suited to most applications. Only wide temperature range and extreme stability requirements can displace this technique in favor of some alternate.

PULSE-WIDTH/AMPLITUDE MODULATION MULTIPLIERS are often called "averaging" multipliers, because the output is the average value of a pulse whose amplitude is modulated by X, and whose "ON" time (width, or duty-cycle) is modulated by Y. The average of such a pulse is proportional to the X ° Y product. By making the pulse-repetition (carrier) frequency high, the averaging time may be shortened to permit remarkably fast response.

These multipliers are exceptionally accurate and stable, and reasonably fast. While not as low in cost as the transconductance type, they are significantly superior for applications demanding the best accuracy attainable, over a wide temperature variation.

PIECEWISE-LINEAR APPROXIMATION (QUARTER-SQUARE) MULTIPLIERS: This class of multipliers uses biased-diode and resistor networks to generate approximate square-law responses to the sum and difference of the X and Y inputs, and then a fairly complex (and expensive) operational amplifier circuit to calculate the X-Y product as follows:

Б	1	[1]	(+ `	$Y \gamma^2$	12	K -	$Y \gamma^2$
Eo	= _K	[[-	2	-)-	(2	-)]

Unfortunately, the approximations involved in the squaring operations cause a "lumpy" error characteristic, and (even more unfortunately) cause "glitches" at the diode breakpoints, which severely limit the usefulness of these multipliers in many applications. Frequency response and accuracy can be good, but only at fairly high intrinsic cost . . . and this circuit must be classified as approaching obsolescence.

TRIANGLE-AVERAGING MULTIPLIERS: These circuits are very similar to pulse-width/height-modulated multipliers, but do not quite attain the accuracy or stability of the pulse averaging technique. Usually, they provide somewhat inferior performance to the pulse-averaging multipliers, at the same cost. (Some advanced transconductance multipliers will actually perform as well, at lower cost.) A recommended lower cost equivalent is the model 428 multiplier. This transconductance design combines good drift and linearity characteristics over wide signal ranges.

	COMPARATIVE CHARACTERISTICS OF MULTIPLIER TYPES & CLASSES							
Туре	Performance Class (See Note)	Maximum Error, % of F.S.	Accuracy Stability	Offset Stability	Bandwidth (–3dB, Small Signal)	Slewing Rate	Recommended ADI Models	Additional Notes
	Moderate Accuracy & Bandwidth	1%, 2%	0.04%/°C	2mV/°C	400kHz	5V/µsec	426, 432 530, 531	General purpose. Lowest cost.
Transcon- ductance	High Accuracy, Moderate Bandwidth	0.5%	0.02%/°C	200µV/°C	300kHz	5V/μsec	428	Maintains 1% max. error over ±25°C temperature range.
	High Accuracy Wideband	0.5%	0.04%/°C	1mV/°C	10MHz	120V/µsec	429	Fastest of any type
Pulse-Width/	High Accuracy Very Slow Response	0.1%	0.02%/ [°] C	100µV/°C	100Hz 1kHz	0.6V/msec to 6V/msec	Substitute ADI 427	Low bandwidth restricts use to "DC." Lowest T.C. of all.
Averaging	High Accuracy, Moderate Bandwidth	0.1%	0.02%/°C	150µV/°C	100kHz	3V/μsec	424, 425 427	Best for high-accuracy dynamic computing
Piecewise- Linear Approx.	High Accuracy Wide Bandwidth	0.25%	0.05%/°C,	500µV/°C	1MHz	2V/µsec	Substitute ADI 427	Pulse-width type offers better accuracy and T.C. for bandwidths to 100kHz.
Triangle Averaging	High Accuracy Slow Response	0.5%	0.03%/°C	200μV/°C	1kHz	5V/msec	Substitute ADI 428	Replaced by high-accuracy transconductance

NOTE: Slow Response = 100Hz to 10kHz; Moderate Bandwidth = 10kHz to 1MHz; Wide Bandwidth = 1MHz to 10MHz. All at -3dB Frequency Response.

MULTIPLIER CIRCUIT

In theory, a multiplier has an output which is ideally the product of two input variables, X and Y. However, the practical multiplier is subject to various offset errors and nonlinearities which must be accounted for in its application. The discussion below is intended to assist the designer in understanding and interpreting multiplier specifications and to offer him insight into its operation.

In practice, the multiplier is designed in two parts, one of which contains a multiplying cell, M, whose output feeds into a gain conditioning op amp, A. Also summed at the op amp input is the variable, Z, which is used as an input in the divide mode. Z is normally connected to the output during multiplication. To divide, Z and X become inputs and Y is tied to the output. Shown below is a practical multiplier illustrating both offset and nonlinear components, (Figure 1). Although the circuit details are quite sophisticated, the concept and block diagram are reasonably straightforward. The basic equation for the multiplier, including offsets (X_0, Y_0, Z_0) and nonlinearity (F [X, Y]) is given here. Multiplier specifications may be readily interpreted from this expression and are described below.

Eo	$= \frac{XY}{10B} \pm$	$= \frac{X_{o} Y}{10B}$	$\pm \frac{X Y_0}{10B}$	$ \stackrel{\pm}{\longrightarrow} Z_{0} + f(X, Y) $
	Product (B = scale factor error)	(X offset) Feed	(Y offset)	Output Offset Nonlinearity

ESTIMATING SMALL-SIGNAL MULTIPLIER ERRORS After all the adjustments have been made, multipliers have an irreducible error called "nonlinearity," a function of both x and y, [f(x, y)]. In general, it is small near zero and increases rapidly near full scale. By taking advantage of nonlinearity specifications on the data sheet, you can often

use a less-costly multiplier to obtain adequate small-signal

accuracy, and you can determine which input to use for best accuracy, if one of the input signals has a small range of variation.

This is done by using the approximation:

f (x, y) \cong |x | ϵ_x + |y | ϵ_y , where ϵ_x and ϵ_y are the fractional nonlinearities specified for the x and y inputs *EXAMPLE*: For Model 426, $\epsilon_x = 0.6\%$, $\epsilon_y = 0.3\%$. What maximum error can one expect for x = 5V, y = 1V? Can one get less by interchanging inputs?

- 1. Nominal output is xy/10 = (5)(1)/10 = 500 mV
- 2. Expected error is (5) (0.006) + (1) (0.003) = 33mV, 6.6% of output (0.33% F.S.)
- 3. Interchanging inputs, (1) (0.006) + (5) (0.003) = 21mV, 4.2% of output (0.21% F.S.)

Compare this with the overly-conservative error predicted by the overall 1% of full scale specification: 100mV, or 20% of output.

DIVIDER CIRCUIT

High accuracy multipliers are recommended for divider operation because of their high linearity and low drift, which become critical in the divide mode since these errors are inversely dependent on denominator, X, as expressed in the equation here. The multiplier of Figure 1 is shown connected as a divider, in Figure 2.

 E_{NL} and ϵ_d , described previously as F (X, Y) and offset error drift, appear at the output of the multiplier cell, M. With X at full scale, the output divider error is the same as that of the multiplier for full scale outputs. However, as X decreases, divider errors (and noise to a lesser extent) increase inversely with amplitude which severely limits its useful dynamic range. Bandwidths vary directly with divisor, X, since the multiplier appears as a variable resistor in parallel with roll-off capacitor, C.



126 MULTIPLIERS/DIVIDERS

EFINITION OF SPECIFICATIONS

FFSET AND OFFSET DRIFT: Output offset is the output oftage observed when X = Y = 0:



VOISE is specified and measured with both inputs at zero ignal and zero impedance (i.e., shorted). For low frequency pplications, filtering the output of the multiplier may mprove small signal resolution significantly.

EEDTHROUGH: Assume now that both inputs are at zero, nd the output offset is trimmed to zero. Ideally, the output hould remain at zero even if only one of either input is at ero. In fact, it should not matter what the value of the ion-zero input signal is, within ratings; the product of that ignal and zero should yield zero output (Figure A). n practical multipliers, however, there is always a small but inite output error under these conditions, and this output s called the *feedthrough*. If we set X = 0, and measure the ℓ -channel feedthrough at, say, Y = 20V p-p, we define Y eedthrough offset as:

$$E_{FY} = E_{o}$$

X = 0
Y = 20V p-p, 50Hz (1)

Now, for Y = 0, there is an analogous X-channel feedthrough.

$$E_{FX} = E_{o}$$

 $Y = 0$
 $X = 20V \text{ p-p, 50Hz}$ (2)



NONLINEARITY: While errors due to output offset, feedthrough and scale factor can be substantially reduced by internal (and external) adjustments, nonlinearity remains as a basic, irreducible limitation to achievable accuracy. Nonlinearity is measured by applying a full scale DC signal to one input and a low frequency sine wave with full scale peak-topeak amplitude to the other. The AC output is then nulled against the AC input and the Scale Factor is adjusted for minimum error voltage. The residual peak-to-peak error voltage is then a measure of nonlinearity referred to a best straight line. This method of measuring and defining nonlinearity includes the nonlinear terms of the transfer function as well as the feedthrough functions.

GAIN ERRORS: The overall gain of the multiplier is not constant for any combination of inputs, therefore, we must expect a scale-factor error, $B \approx 1$, which can be trimmed to unity. Gain, in general, also varies with time, temperature, power supply voltage, signal level (nonlinearity) and, most significant, with frequency. Except in the most critical applications, the only gain error of any consequence is usually that caused by bandwidth. Also associated with gain error is a phase lag at the output. Note also that slewing rate errors (inability to "track" large, rapid output changes) limit the response time on full scale changes in output.



SLEW RATE BEHAVIOR

MULTIPLIER ACCURACY: As one measure of product performance, Analog Devices has chosen to combine all error contributions in one multiplier specification, multiplier output error. This error is the deviation of actual value from predicted value of the multiplier output voltage. It is given as a percentage of full scale output, ±10V, at a specified ambient temperature, +25°C, and it includes scale-factor error offset, nonlinearity and feedthrough terms combined. Therefore, because these factors have been accounted for in the overall error specifications, it is important not to duplicate these terms in your calculations when developing an error budget. Note that overall accuracy is specified, which due to error cancellation is usually less than the rms sum of its constituents. To account for temperature variations in overall error, add to the basic error term above the specified accuracy drift.

MULTIPLIERS/DIVIDERS 427, 424, 425, 426, 432, 428, 429, 422, AD530, AD531



MULTIPLIER CLASSIFICATION AND PRODUCT DESCRIPTION

To assist in selecting the best multiplier for the application, we have classified products according to the technique used to develop the multiply function which essentially determines the capabilities of the device. Analog Devices has focused on the pulse-width/height technique and the variable transconductance technique to develop the multiply/divide function. These two approaches are considered complementary and were selected because of their inherent ability to provide a good balance between performance and cost.

PULSE-WIDTH-HEIGHT MODULATION PRECISION MULTIPLIERS (PWH)

The pulse-width-height modulation technique is capable of producing multipliers of the highest precision. Typical specifications include accuracies from 0.1% to 0.25%, offset drifts to $100\mu V/^{\circ}$ C, output noise of $50\mu V$ rms and bandwidths to 100 kHz. Multipliers in this group should be used for wide temperature range applications, for analog computing elements, for dividers because of their inherently good drift, noise and low non-linearities, and, in general, for exacting multiplier/divider applications where wide dynamic signal swings are anticipated. Products in this group include models 427. 424, and 425.

MODEL 427 (HIGH ACCURACY): Based on the highly successful Model 424, the 427K is internally trimmed to specified accuracy and requires no external adjustments for multiplication. It uses pulse-width modulation to obtain accuracies to 0.2% (FS), offset drifts as low as $200\mu V/^{\circ}C$, and nonlinearity of 0.04% maximum, for both inputs. All semiconductors used in this design are hermetically sealed.

Unlike most high accuracy multipliers embodying the modulation principle, 427's high carrier frequency allows a bandwidth rating of 100kHz for -3dB response with no carrier ripple on output. Depending on how it is connected, the 427 can be used for multiplying, dividing, squaring, or square rooting.

The true capability of a multiplier can be best demonstrated when the unit is used in the divide mode, particularly with small denominators. Because the 427 features excellent small signal linearity, the errors are very much smaller than one would predict using 10/x for divider error.

MODEL 424 (HIGH ACCURACY): The model 424 J/K is an untrimmed multiply-only module with performance comparable to that of model 427. In every respect, except for the divide and external trim features, the 424 will perform the 427 task at lower component cost and should be considered for laboratory and industrial applications where external trimming may be conveniently performed to achieve the highest possible accuracies. When externally trimmed, model 424 will perform with 0.2% (424J) and ` 0.1% (424K) accuracies with bandwidths to 100kHz (- 3dB). It may be used to perform division when operated with an external op amp.

MODEL 425: Customers may purchase the model 424 mounted on a PC card which contains all necessary adjustment potentiometers to trim the multiplier to its rated accuracies. Designated model 425J (with 424J) and 425K (with 424K), these models are factory trimmed and offered at a nominal cost above that of 424 alone.

VARIABLE TRANSCONDUCTANCE TYPES

The popular variable transconductance technique complements the PWH approach and should be considered whenever wider bandwidths, to 10MHz, are required along with lower costs and good overall performance. Both discrete and monolithic devices are available using this design approach. Multiplier specifications include accuracies from 0.5% to 2%, bandwidths from 300kHz to 10MHz and drifts from $200\mu V/^{\circ}C$ to $2mV/^{\circ}C$. Each model is capable of 4-quadrant multiplication, or 2-quadrant division. Because the transconductance technique can be optimized in different ways to yield highly specialized performance, models may be classified as: general purpose (models 426, 432, 530 and 531; high performance (model 428); and wide bandwidth (models 429 and 422).

General Purpose

MODEL 426 (GENERAL PURPOSE 1%, 0.5%): Available as an internally trimmed 1% (J, K) or 0.5% (L) accurate multiplier/divider, Model 426 should be considered as a first choice for most general purpose designs and OEM applications. External trimming further improves performance to 0.6% (J, K) and 0.35% (L). Nonlinearities are held to a low 0.6% (X) and 0.3% (Y) for models 426 (J & K), allowing the user to assign that input signal with the widest dynamic range to the 0.3% (Y) input terminal for better accuracy. For even better performance, model 426 L should be selected for lowest drift and good linearity and feedthrough characteristics.

MODEL 432 (ECONOMY): Using hermetically sealed components, the models 432 J(K), 2%(1%) multiplier/ dividers, are internally trimmed and are available in a compact package for low cost OEM applications requiring field interchangeable modules with no additional trimming. External trimming will improve accuracy from 2%(1%) to 1%(0.6%). Performance, reliability and bandwidth are comparable to model 530. OEM discounts are available.

MODEL AD530 (MONOLITHIC): With the transfer function XY/10, the AD530 is the first IC multiplier/divider to include

the transconductance multiplying element, the built-in reference and the output op amp all on the same chip. Available in both industrial (AD530 J, K or L) and military grades (AD530S), its compact package and good performance make it an ideal choice for high reliability assignments. The AD530 needs only four trim pots to achieve accuracies to $\pm 0.5\%$ of full scale. Bandwidth is 1MHz and slew rate $45V/\mu$ sec. The AD530 is available in both the TO-100 metal can and TO-116 ceramic dual-in-line packages.

MODEL AD531 (MONOLITHIC): TRANSFER FUNCTION $(X_1 - X_2)Y/Z$. Not just a multiplier, the AD531 is truly a computation circuit that is ideally suited to such applications as AGC, True rms-to-DC conversion, ratio determination, absolute value and vector computation. Like the AD530, the AD531 combines the transconductance element, a precision stable reference and the output op amp on a single monolithic structure. Flexibility of operation is achieved by virtue of the programmable scale factor capability and the differential input feature. In addition to verification of accuracy at +25°C, the AD531L and AD531S are further tested for maximum error limits of ±1.5% and ±3.0%, respectively, at their extreme operating temperature limits. The AD531 is available in the TO-116 ceramic dual-in-line package.

MODEL AD532 (MONOLITHIC-INTERNALLY TRIMMED): TRANSFER FUNCTION $(X_1 - X_2)(Y_1 - Y_2)/10$. The AD532J, AD532K and AD532S are the industry's first internally-trimmed monolithic multiplier/dividers. They guarantee maximum multiplying errors of ±2.0%, ±1.0% and $\pm 1.0\%$ of full scale (10V) at $\pm 25^{\circ}$ C, respectively, without the need for any external trim networks or output op amp. In addition, the differential X and Y inputs provide significant operating flexibility for both algebraic computation and transducer instrumentation applications. Further, the AD532 can be used as a direct replacement for some popular IC multipliers that require external trimming, such as the AD530. The AD532J and AD532K are rated for operation from 0 to +70°C. The AD532S will operate from -55°C to +125°C with a maximum multiplying error of ±4.0% of full scale. All designs are available in both the TO-100 metal can and the TO-116 ceramic dual-in-line packages.

High Performance

MODEL 428: (LOW DRIFT): This device meets high performance requirements for many applications where component price and accuracy are key factors. As a transconductance multiplier, it approaches the performance of more expensive multipliers, using modulation techniques, but at lower costs. Factory trimmed to 0.5% with offset drift of $200\mu V/^{\circ}C$, enables model 428K to operate over a $50^{\circ}C$ temperature range with less than 1% error increase.

Both 428J and 428K may be externally trimmed for an improved accuracy of 0.25% and operated as dividers and square root circuits. The nonlinearity component of error is particularly low in this unit, resulting in excellent performance as a divider. For example: 50mV maximum error for a 10:1 dynamic range of denominator.

In addition to its excellent DC performance, it has 300kHz small signal bandwidth (-3dB) and full power output to beyond 70kHz, considerably exceeding the audio range.

Wideband

MODEL 429 (HIGH ACCURACY): This unit should be considered for all new multiplier/divider designs requiring the best possible speed, drift and accuracy performance. The model 429 factory trimmed, is available as a 429A (1%, $2mV/^{\circ}C$) and 429B (0.5%, $1 mV/^{\circ}C$) both with 10MHz response. Capable of multiplying or dividing, models 429 A/B may be easily converted to the divide mode with external pin interconnections. Accuracies may be improved upon for models 429A (from 1% to 0.7%) and 429B (from 0.5% to 0.3%) with external trimming. Note, that although model 429 is an improvement over model 422, these devices are not pin compatible.

MODEL 422 (HIGH FREQUENCY): This unit is available as a 1% multiplier with a 5MHz bandwidth, and may be operated as a divider when connected with an external op amp. Model 422A and 422K, with $2mV/^{\circ}C$ and $1mV/^{\circ}C$ offset drifts respectively, may be externally trimmed for 0.7% accuracy to improve on the 1% factory trimmed specification.

MULTIPLIERS/DIVIDERS (Discrete)

SPECIFICATION SUMMARY (Typical @ 25°C and ±15VDC unless otherwise specified)

	VARIABLE TRANSCONDUCTANCE TY				
Models ¹	Economy 432J (432K)	General Purpose 426A (426K) (426L)	Wideband 422A (422K)		
Full Scale Accuracy ²	2% (1%)	1% (1%) (0.5%)	1%		
Divides and Square Roots	YES	YES	Division requires external amp		
Multiplication Characteristics Output Function Error, Internal Trim (±) Error, External Trim (±) Accuracy vs. Temperature (±) Accuracy vs. Supply (±) Warm up Time to Specifications	XY/10 2% (1%) max 1.0% (0.6%) 0.06%/°C (0.04%/°C) 0.1%/% 1 min	XY/10 1% (1%) (0.5%) max 0.6% (0.6%) (0.35%) 0.05%/°C (0.04%/°Cmax) (0.04%/°Cmax) 0.03%/% 1 sec	XY/10 1% (1%) max 0.7% (0.7%) 0.05%/°C (0.04%/°C max) 0.05%/% 1 sec		
Output Offset (±) Initial Average vs. Temperature 0°C to +70°C Average vs. Supply	20mV (25mV max) 2mV/°C (1mV/°C) 10mV/%	20mV 2mV/°C (1mV/°C max) (1mV/°C max) 2mV/%	25mV 2mV/°C (1mV/°C max) 1mV/%		
Scale Factor (±) Initial Error	1% (0.5%)	0.5% (0.5%) (0.25%)	0.5%		
Non Linearity (±) X Input (X = 20V p-p, Y = ±10VDC) Y Input (Y = 20V p-p, X = ±10VDC)	0.8% (0.6% max) 0.4% (0.3% max)	0.6% (0.6%) (0.25%) max 0.3% (0.3%) (0.25%) max	0.6% max 0.3% max		
Feedthrough X = 0, Y = 20V p-p 50Hz with external trim Y = 0, X = 20V p-p 50Hz with external trim Feedthrough vs. Temperature, each input	80mV (50mV) p-p max 30mV p-p 120mV (100mV) p-p max N/A 1mV p-p/°C	60mV (60mV) (40mV) p-p max 20mV p-p 100mV (100mV) (40mV) p-p max 60mV (60mV) (20mV) p-p 2mV p-p/°C	50mV p-p max 8mV p-p 100mV p-p max 35 mV p-p 2mV p-p/°C		
Bandwidth - 3dB Small Signal Full Power Response Slew Rate Small Signal Amplitude Error (±) Small Signal Vector Error (±) Settling Time for ±10V Step Overload Recovery	1 MHz 700kHz 45 V/μsec 1% @ 40kHz 1% @ 10kHz 1μsec to 2% 3μsec	400kHz 80kHz 5V/μsec 1% at 40kHz 1% at 10kHz 3μsec to 1% 3μsec	5MHz min 2MHz min 120V/µsec min 1% at 300kHz min 1% at 50kHz min 0.4µsec to 1% 0.15µsec		
Output Noise 5Hz to 10kHz 5Hz to 5MHz	600µV rms 3mV rms	500µV rms 2.5mV rms	500µV rms 2.5mV rms		
Output Characteristics ⁴ Voltage at Rated Load (min) Current (min) Load Capacitance Limit	±10V ±5mA 0.001µF	±11V ±11mA 1µF	±11V ±11mA 0.01µF		
Input Resistance X/Y/Z Input	10M Ω /10k Ω /36k Ω	25k Ω /25k Ω /200k Ω	10k Ω /11k Ω /N/A		
Input Bias Current X/Y/Z Input	2µA each	+100nA/+100nA/-50µA	+100nA each		
Maximum Input Voltage For Rated Accuracy Safe Level	±10.1V ±Vs	±10.5V ±18V	±10.5V ±16V		
Power Supply (V _S) Rated Performance Operating Quiescent Current	±15V ±12 to ±18V ±4.5mA	$\pm 14.7 \text{ to } \pm 15.3 \text{V}$ $\pm 11.5 \text{ to } \pm 18 \text{V}$ $\pm 5 \text{ mA}$	±14.7 to ±15.3V ±14 to ±16V ±12mA		
Temperature Range ⁵ Rated Performance Operating Storage	0°C to +70°C -25°C to +85°C -55°C to +125°C	-25 to +85°C (0 to +70°C)(0 to +70°C) -25°C to +85°C -55°C to +125°C	-25°C to +85°C (0°C to +70°C) -25°C to +85°C -55°C to +125°C		
Package Outline Case Dimensions	QC-2 1.1" x 1.1" x 0.4"	FA-4 1.5" x 1.5" x 0.6"	FA-3 1.5" x 1.5" x 0.6"		
	\$29 (\$45) \$27 (\$43)	\$45 (\$59) (\$69) \$43 (\$57) (\$67)	\$109 (\$139) \$104 (\$129)		

NOTES:

¹ Parentheses indicate specification for the high performance (K or L version) model of each multiplier when it differs from the J or A version. For example, order Model 427J for 0.25% accuracy, Model 427K for 0.2% accuracy.

 2 All accuracy and error specifications, when expressed as percentages, refer to % of full scale (10V).

³Model 424 available for \$20 additional on printed circuit board with preadjusted trim pots. Card socket supplied. Order Model 425J or 425K.

second and the second		PRECISION (PWH) TYPES	
Accurate Wideband	Accurate Low Drift	High Accuracy	High Accuracy
429A (429B)	428J (428K)	424J (424K) 425 ³	427J (427K)
1% (0.5%)	0.5%	0.2% (0.1%)	0.25% (0.2%)
YES	YES	Division requires external amp	YES
XY/10	XY/10	XY/10	XY/10
1% (0.5%) max	0.5% (0.5%) max	Untrimmed	0.25% (0.2%) max
0.7% (0.3%)	0.25% (0.25%)	0.2% (0.1%) max	0.15% (0.1% max)
0.05%/°C (0.04%/°C max)	0.02%/°C (max)	0.02%/°C (max)	0.02%/°C max
0.05%/%	0.02%/%	0.02%/%	0.02%/%
20mV (10mV) max	10mV	Adj. to zero	5mV
2mV/°C (1mV/°C max)	0.5mV/°C (0.2mV/°C max)	0.2mV/°C (0.2mV/°C max)	0.2mV/°C (0.2mV/°C max
1mV/%	2mV/%	2mV/%	1mV/%
0.5% (0.25%)	0.25%	Adj. to 0.1% (0.05%)	0.1% (0.05%)
0.5% (0.2%) max	0.25% max	0.08% (0.04%) max	0.08% (0.04%) max
0.3% (0.2%) max	0.25% max	0.08% (0.04%) max	0.08% (0.04%) max
50mV (20mV) p-p max	40mV p-p max	N/A	20mV p-p max
16mV (10mV) p-p	10mV p-p	2mV (1mV) p-p	4mV p-p
100mV (30mV) p-p max	40mV p-p max	N/A	20mV p-p max
50mV (20mV) p-p	10mV p-p	4mV (2mV) p-p	5mV p-p
2mV p-p/°C	1mV p-p/°C	0.2mV p-p/°C	0.2mV p-p/°C
10MHz	300k Hz	100kHz	100k Hz
2MHz min	70k Hz	40kHz	30k Hz
120V/µsec min	4 V/µsec	3V/µsec	2V/μsec
1% at 300kHz min	1% at 40k Hz	0.1% at 4kHz	0.1% at 4k Hz
1% at 50kHz min	1% at 2k Hz	1% at 700Hz	1% at 700 Hz
0.5µsec to 1%	5µsec to 0.5%	15µsec to 0.1%	20μsec to 0.1%
0.15µsec	3µsec	10µsec	10μsec
200μV rms	500 μ V rms	50μV rms	50µV rms
1.5mV rms	2.5mV rms	1mV rms	1mV rms
±11V	±11V	±10V	±10.2V
±11mA	±11mA	±7mA	±7mA
0.01μF	0.001µF	0.01µF	0.01µF
$10k\Omega/11k\Omega/13k\Omega$	25k Ω /25k Ω /200k Ω	$10k\Omega/11k\Omega/N/A$	10k Ω /10k Ω /33k Ω
+100nA/+100nA/±40nA	+100nA/+100nA/-50µA	±3µA each	±3µA/±3µA/±10µA
±10.5V	±10.5V	±10.5V	±10.5V
±16V	±18V	±16V	±16V
^{±14.7} to ^{±15.3V}	±14.7 to ±15.3V	±14.8 to ±16V	±14.8 to ±15.3V
^{±14} to ^{±16V}	±11.5 to ±18V	±14.8 to ±16V	±14.8 to ±16V
^{±12mA}	±5mA	±16mA	±16mA
−25°C to +85°C	0°C to +70°C	0°C to +70°C	0°C to +70°C
−25°C to +85°C	-25°C to +85°C	-25°C to +85°C	-25°C to +85°C
−55°C to +125°C	-55°C to +125°C	-55°C to +125°C	-55°C to +125°C
FA-4	FA-4	D-1	D-2
1.5" x 1.5" x 0.6"	1.5" x 1.5" x 0.6"	1.6" x 3.0" x 0.6"	1.6" x 3.0" x 0.6"
\$109 (\$139)	\$89 (\$109)	\$139 (\$174)	\$159 (\$210)
	\$70 (\$98)	\$126 (\$157)	\$143 (\$189)

 4 All models are short-circuit-proof, from output to ground. Multipliers are not guaranteed short-circuit-proof from output to +VS or -VS.

⁵Most models designated 'J' or 'K' are available with extended temperature range operation to stated accuracy. Consult factory or your nearest Analog sales office.

MULTIPLIERS/DIVIDERS (Monolithic) SPECIFICATION SUMMARY (Typical @ +25°C and ±15VDC, unless otherwise specified.)

Models	VARIABLE TRANSCONDUCTANCE TYPES			
	530J (530K) (530L) (530S)	531J (531K) (531L) (531S)	532J (532K) (532S)	
Price 1-24 Price 25-99	\$22.50(\$33.50)(\$45.00)(\$51.00) \$18.00(\$27.00)(\$36.00)(\$41.00)	\$30.00(\$45.00)(\$54.00)(\$54.00) \$24.00(\$36.00)(\$44.00)(\$44.00)	\$26.00(\$36.00)(\$49.00) \$21.00(\$30.00)(\$40.00)	
Full Scale Accuracy	2% (1%) (0.5%) (1%)	2% (1%) (0.5%) (1%)	2% (1%) (1%)	
Divides and Square Roots	YES	YES	YES	
Multiplication Characteristics Output Function Error, Internal Trim (±) Error, External Trim (±) max Accuracy vs. Temperature (±) Accuracy vs. Supply (±) Warm up Time to Specifications	XY/10 N/A 2% (1%) (0.5%) (1%) 0.06(0.03)(0.01)(0.02 max)%/ ⁵ C 0.2%/% 1 sec	XY/I _{REF} N/A 2% (1%) (0.5%) (1%) 0.06(0.03)(0.01)(0.02 max)%/°C 0.2%/% 1 sec	$(X_1 - X_2)(Y_1 - Y_2)/10$ 2% (1%) (1%) N/A 0.06(0.03)(0.02)%/°C 0.2%/% 1 sec	
Output Offset (±) Initial Average vs. Temperature 0 to +70°C Average vs. Supply	Adj. to zero 0.2mV/°C 70mV/V	Adj. to zero 0.2mV/°C 70mV/V	±50mV max(±20mV max)(±20mV max) 0.7(0.7)(2.0 max)mV/°C 60mV/V	
Scale Factor (±) Initial Error	Fixed Adj. to 1%(0.5%)(0.2%)(0.5%)	Dynamically Variable Adj. to 1%(0.5%)(0.2%)(0.5%)	Fixed Adj. to 1%(0.5%)(0.5%)	
Non Linearity (±) X Input (X = 20V p-p, Y = ±10VDC) Y Input (Y = 20V p-p, X = ±10VDC)	0.8%(0.5%)(0.3%)(0.5%) 0.3%(0.2%)(0.2%)(0.2%)	0.8%(0.5%)(0.3%)(0.5%) ⁽¹⁾ 0.3%(0.2%)(0.2%)(0.2%) ⁽¹⁾	0.8%(0.5%)(0.5%) 0.3%(0.2%)(0.2%)	
Feedthrough X = 0, Y = 20V p-p 50Hz with external trim Y = 0, X = 20V p-p 50Hz with external trim Feedthrough vs. Temperature, each input	150mV(80mV)(+0mV)(80mV)p-p max 100mV(60mV)(30mV)(60mV)p-p max 2mV p-p/°C	150mV(80mV)(40mV)(80mV)p-p max ⁽¹⁾ 100mV(60mV)(30mV)(60mV)p-p max ⁽¹⁾ 2mV p-p/ [°] C	200mV(100mV)(100mV)p-p max 200mV(100mV)(100mV)p-p max 2mV p-p/°C	
Bandwidth -3dB Small Signal Full Power Response Slew Rate Small Signal Amplitude Error (±) Small Signal Vector Error (±) Settling Time for ±10V Step Overload Recovery	1MHz 750kHz 45V/µsec 1% @ 100kHz 1% @ 10kHz 1µsec to 2% 1µsec	1MHz 750kHz 45V/µsec 1% @ 100kHz 1% @ 10kHz 1µsec to 2% 1µsec	1MHz 750kHz 45V/µsec 1%@100kHz 1%@100kHz 1µsec to 2% 1µsec	
Output Noise 5Hz to 10kHz 5Hz to 5MHz	600μV rms 3mV rms	600μV rms 3mV rms	600μV rms 3mV rms	
Output Characteristics Voltage at Rated Load (min) Current (min) Load Capacitance Limit	±10V ±5mA 0.001µF	±10V ±5mA 0.001µF	±10V ±5mA 0.001µF	
Input Resistance X/Y/Z Input ²	$10M\Omega/6M\Omega/36k\Omega$	10ΜΩ/6ΜΩ/36kΩ	10ΜΩ/10ΜΩ/36kΩ	
Input Bias Current X/Y/Z Input	2μΑ/2μΑ/5μΑ	2μΑ/2μΑ/5μΑ	2µA/3µA/5µA	
Maximum Input Voltage For Rated Accuracy Safe Level	±10.1V ±Vs	±10.1V ±V _S	±10.1V ±V _S	
Power Supply (V _s) Rated Performance Operating Quiescent Current	±15V ±12 to ±18V ±4mA	±15V ±12 to ±18V ±4.5mA	$ \begin{array}{c} \pm 15V \\ \pm 10 \text{ to } \pm 18V \\ \pm 4\text{mA} \end{array} $	
Temperature Range Rated Performance Operating Storage	$ \begin{array}{c} J - 0 \ to \ +70^{\circ}C \ \ K - 0 \ to \ +70^{\circ}C \\ L - 0 \ to \ +70^{\circ}C \ \ S - 55^{\circ}C \ to \ +125^{\circ}C \\ -55^{\circ}C \ to \ +125^{\circ}C \\ -65^{\circ}C \ to \ +125^{\circ}C \end{array} $	$ \begin{array}{c} J - 0 \ to \ +70^{\circ}C \ \ K - 0 \ to \ +70^{\circ}C \\ L - 0 \ to \ +70^{\circ}C \ \ S \ - \ -55^{\circ}C \ to \ +125^{\circ}C \\ \ -55^{\circ}C \ to \ +125^{\circ}C \\ \ -65^{\circ}C \ to \ +125^{\circ}C \end{array} $	0 to +70°C(0 to +70°C)(-55°C to +125°C) -55°C to +125°C -65°C to +125°C	
Package Outline	TO-100 + TO-116	TO-116	TO-100 + TO-116	

(1) I_{REF} = full scale.

(2)Z input current is proportional to Z input voltage.

FUNCTION MODULES MULTI-FUNCTION 433 Y (Z/X)^m OPERATOR LOG, ANTILOG, MULTIPLIER, DIVIDER, EXPONENTIATOR

PRODUCT PROFILE

The model 433 is a multifunction module, consisting of all hermetically sealed semiconductors, which may be used to implement a wide range of computational circuits. Requiring only two external resistors for programming the exponent, m, the model 433 will perform multiplication, division or exponentiation up to the 5th power or root according to the expression, Y (Z/X)^m. It may also be used to develop more complex functions such as RMS or vector sums using inexpensive external operational amplifiers. Examples of these transfer functions are listed below along with a model 433 block diagram design.





The model 433 has proven to be extremely useful for generating both linear and nonlinear functions for on-thespot computations and for linearizing a wide range of transducer characteristics in medical, industrial and process control equipment design. Its excellent accuracy performance and programmability make it ideal for analog computation or simulation, test equipment designs or, in general, where one function module may be used to fulfill several design objectives. Model 433 is attractively priced for new OEM equipment designs.

EXAMPLES OF MODEL 433 TRANSFER FUNCTIONS

General Expression: $V_0 = \frac{10}{9} V_y (V_z/V_x)^m$

Limits:

 $1/5 \le m \le 5, 0 \le V_x, V_y, V_z \le 10V$

Using two programming resistors only:

Multiply:	$V_o = K V_y V_z$	Divide:	$V_0 = K (V_Z/V_X)$
Square:	$V_{o} = K(V_{z})^{2} = K V_{z}V_{y}$	Square Root:	$V_0 = K (V_Z)^{\frac{1}{2}}$
Powers:	$V_{o} = K V_{y}(V_{z}/V_{x})^{-1} \le 5$	Roots:	$V_o = K V_y (V_z/V_x)^{1/5} \le m < 1$
P/V/T:	$V_o = K V_y V_z / V_x$	Reciprocal:	$V_0 = K/V_X$

Using External Amplifiers:

True RMS to DC: $V_0 = \sqrt{\frac{V_1^2}{V_1^2}}$

Vector: $V_0 = \sqrt{V_1^2 + V_2^2}$

CIRCUIT TECHNIQUES

The model 433, using log circuit techniques, is designed in two parts and consists of log circuits followed by an antilog section. The log ratio section operates on inputs X and Z to develop the function, log Z/X. This ratio is then either amplified or attenuated, using external programming resistors, R1 and R2, to establish the exponent, m, where m > 1 for powers, m < 1 for roots. The signal, m log Z/X, is then summed with the log Y; and the antilog is developed to realize the final transfer function, $(10/9)(Y)(Z/M)^m$. The exponent, m, may have any value from 1/5 to 5. As with all log designs, operation is limited to one quadrant.

An internal reference voltage, V_{ref} , is also made available for the convenience of the user. When setting up the desired transfer function, all unused input terminals should be connected to V_{ref} . This reference voltage is temperature compensated, as is the entire 433 design, for good performance from 0 to +70°C.

OTHER DESIGN FEATURES

The designer, considering model 433 for one quadrant applications, can expect additional performance characteristics, better than those found in most transconductance multipliers.

Multiplier performance for outputs from 10mV to 10V (60dB), typically has less than 0.5% of full scale overall error, with a total error drift coefficient of $0.01\%/^{\circ}C$.

Square and square root circuits (m = 2, 1/2) also have typical errors of 50mV at 10 volts out, reducing to 20mV errors for 100mV outputs. For other roots (m \leq 1/2) and powers (m \geq 2), errors are typically less than 1% of full scale for 10mV to 10V outputs. Output noise, worst case, is 100 μ V

rms at X = +10V, increasing to about $300\mu V$ rms for X = 0.1V, in a 10Hz to 1kHz bandwidth. This is a threefold improvement over most transconductance type multipliers or dividers.

Small signal frequency response (-3dB) is signal-amplitude dependent, as is the case with all log circuits, and decreases from approximately 100kHz at 10 volt input levels to 400Hz at 10mV input levels for any multiplier or divider input. This is measured using a 10% small signal amplitude superimposed on the larger dc level. Full output responses for a ± 5 volt signal, superimposed on a 5VDC level is 50kHz for the multiplier and (V_x) X (5kHz) for the divider.

MODEL 433: 0.5% DIVIDER, WIDE DYNAMIC RANGE

Probably the most impressive performance improvement owing to model 433's log/antilog circuit approach, is its ability to hold high divider accuracies over wide, 100:1, input signal ranges. For example, when compared to a precision 0.1% multiplier/divider of conventional design, the model 433 offers greater than a tenfold improvement. As shown in Figure 1, the model 433 has only 30mV of error for a denominator of 100mV, as opposed to 300 to 500mV of error for the conventional multiplier/divider.

When using a conventional multiplier/divider as a divider, accuracy, offset drift, and noise performance are all degraded as the denominator is decreased. But, for model 433, accuracy, offset drift, and noise performance are all virtually independent of denominator level as illustrated in Figure 1, and this performance is obtained with no external trims.

It is apparent that as a one-quadrant divider, model 433's performance exceeds by wide margins those of higher accuracy dividers costing two to three times more.



Figure 1. Comparison of Divider Error vs. Denominator Level for Model 433 and a Conventional Multiplier/Divider

FEEDBACK TECHNIQUE VS DIRECT IMPLEMENTATION

The reason for the significant improvement of model 433 over other divider designs is apparent if one considers the basic sources of error arising from each design approach. Conventional divider circuits are implemented by using a multiplier cell in a feedback loop. As with all feedback designs, overall accuracy is directly tied to the accuracy and gain setting of the feedback element, a multiplier in this case. In this configuration, as X decreases, loop gain decreases, and divider accuracy therefore varies inversely with the denominator signal, X. The governing equation for this design is derived and presented in Figure 2 to illustrate its basic limitations.

Good performance for these designs requires using a fast, highaccuracy multiplier and a low-drift amplifier in the divider loop.

In contrast, the model 433 log circuit directly implements the divide function. Its accuracy, as shown in Figure 3, is virtually independent of denominator amplitude for constant signal ratios, thereby improving on the conventional divider approach. Drift nonlinearity and noise are also independent of denominator amplitude in contrast to feedback designs. Its only drawback is that operation is restricted to one quadrant (which is not usually a handicap for many applications).

MODEL 433B: HIGHER ACCURACY

Model 433B, an improved version of model 433J, offers ¼% accuracy for denominator levels of 100mV to 10V, has a lower initial offset voltage than the 433J, and offers guaranteed drift performance over a wider temperature range. Like the 433J, this new design contains all hermetically sealed semiconductors. The 433B will be available in production quantities by May of 1973.

MODEL 434:
$$e_0 = V_Y \frac{I_Z}{I_X}$$
 or $V_Y \frac{V_Z}{V_X}$

Model 434, a new member of the 433 family, contains all hermetically sealed semiconductors, is optimized for one quadrant divider applications, and may be trimmed externally to eliminate all DC offset errors. With no external trimming, quadrant divider applications, and may be trimmed externally to eliminate all DC offset errors. With no external trimming, accuracy is guaranteed to within ½% for model 434A, and to ¼% for model 434B. In order to facilitate the implementation of complex circuits, such as vector computations, the model 434 has input pins brought directly to the internal summing junctions. Current summing can then be done directly at the input pin without the use of an external amplifier. A separate set of input pins is brought out for voltage operation thereby offering complete flexibility on combinations of input signals.

Model 434 will be available in production quantities by May of 1973.



Figure 2. Divider Model

Figure 3. Simplified Logarithmic Divider. Error is a Constant Plus a Constant Fraction of Output.

SPECIFICATION SUMMARY (Typical @ +25°C unless otherwise noted)

GENERAL CHARACTERISTIC	Model 433J	
General Expression	$E_o = + \frac{10}{9} V_y \left(\frac{V_z}{V_x}\right)^m$	
Rated Output ¹	+10.5V @ 5m A	
Input	+10.5V @ 5MA	
Signal Range	$0 \le V$ V V $\le \pm 10V$	
Max. Safe Input	$V = V_X, V_Y, V_Z \leq \pm 10V,$	
Resistance	$\mathbf{v}_{\mathbf{X}}, \mathbf{v}_{\mathbf{Y}}, \mathbf{v}_{\mathbf{Z}} \approx \pm 18 \mathbf{V}$	
X terminal	$100k\Omega + 1\%$	
Y terminal	$90k\Omega \pm 10\%$	
Z terminal	$100k\Omega \pm 1\%$	
External Adjustment of the	100000 - 170	
Exponent m		
Range for $m \le 1$ (Root)	$1/5 \le m \le 1$ m = $\frac{R_2}{m}$	
	$R_1 + R_2$	
	$R_1 + R_2$	
Range for $m \ge 1$ (Power)	$1 \leq m \leq 5, m = \frac{1}{R}$	
	$(\mathbf{D}_{1}, \mathbf{D}_{2}) \leq 2 \cos \Omega$	
Poference Terrinel Valeral	$(R_1 + R_2) \leq 200\Omega$	
V (Internal Course)		
v _{ref} (Internal Source)	$+9.0V \pm 5\%$ (a) 1 mA	
	±0.005%/ C	
Power Supply Range		
Specified	\pm (14.7 to 15.3) VDC (a) 10mA	
Operating	$\pm(12 \text{ to } 18) \text{ VDC}$	
Caracifical	0° 0	
Specified	0 C to + /0 C	
Storage	-25 C to +85 C	
Case Dimensione	FA-7	
Drice (1 0)	$1\frac{1}{2} \times 1\frac{1}{2} \times 0.62$	
(10, 24)	\$75.	
$(10-24)^{\circ}$	\$69.	

MULTIPLIER/DIVIDER PERFORMANCE	CHARACTERISTICS:
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Model 433J Specifications	Divide	Multiply
Transfer Function	$E_{o} = +10(V_{z}/V_{x})$	$E_0 = \frac{+V_y V_z}{10}$
Accuracy ^{2, 3}		10
Total Output Error @ +25°C		
(for specified input range)		
Typical (RTO)	±5mV ±0.3% of output	*
Max. Error (RTO)	±50mV	*
Input Range ($V_z \leq V_x$)	0.01V to 10V, V ₂	0.01V to 10V, V
	0.1V to 10V, V _x	0.01V to 10V, V
vs Temp.	$\pm 1 \text{ mV/}^{\circ}\text{C}$	*
Output Offset Voltage (Not Adjusta	ble)	
Initial @ +25°C max	±10mV	*
Offset vs Temp.	$\pm 1 \text{mV}/^{\circ} \text{C}$	*
Noise, 10Hz to 1kHz		
$V_x = +10V$	$100\mu V rms$	*
$V_{x} = +0.1 V$	300µV rms	*
Bandwidth,		
Small Signal (-3dB) ⁴ ,		
$V_{v} = V_{z} = V_{x} = 10V$	100kHz	*
$V_V = V_z = V_x = 1V$	50kHz	*
$V_{V} = V_{z} = V_{x} = 0.1 V$	5kHz	*
$V_y = V_z = V_x = 0.01V$	40011z	*
Full Output (V_y or V_z = 5VDC ±5VAC)	$(V_x) \ge (5 \text{kHz})$	*

* Same as for divide mode. ¹ Terminals short circuit protected to ground only.

¹ Terminals short circuit protected to ground only.
² Multiplier scale factor must be trimmed at Y terminal using a 25kΩ trim pot.
³ Total errors defined as the difference between the measured output and the theoretical output voltage for any given pair of specified input voltages.
⁴ Small-signal measurements are conducted with V_x = V_y = V_z = V at a fixed DC level, and V_y or V_z a superimposed sine wave of amplitude 10%V. All active components hermetically sealed.

FUNCTION MODULES LOGARITHMIC AMPLIFIERS AND ELEMENTS

A Note On Nomenclature

Log modules from Analog Devices develop the instantaneous value of the log or antilog of an input signal. Contrary to communications type log amplifiers, which basically compress AC signals, the 700 series log modules operate on single polarity inputs from DC to an upper cutoff frequency. These temperature compensated designs will work over 6 decades of input current (1nA to 1mA) and 4 decades of voltage (1mV to 10V).

GENERAL DESCRIPTION

Analog Devices offers four types of circuit modules which may be used to develop the log or antilog of an input signal. Depending upon the user's expertise in log amplifier design, or the need for specialized performance, the designer may select: 1) the model 755, a versatile yet complete log/antilog amplifier; 2) the model 756 a versatile and complete log ratio module; 3) the model 752 log module requiring one external op amp to complete the design at lower cost; or 4) the model 751 log element requiring two external op amps and several other components for log operation. The external op amps are usually selected to reduce voltage drift or bias currents for improved performance over extended input signal ranges.

Typical applications for these circuits include data compression, transducer linearization, exponentiation, root extraction, and other computational functions for use in gas chromatography, acoustical and light measurements as well as medical and seismic instrumentation.

Circuit Techniques: In contrast to earlier techniques using diode-resistor breakpoint networks, all Analog Devices' log circuits use a combination of selected dual transistor networks that make use of the relationship between base emitter voltage and collector current. When properly temperature compensated, as supplied by Analog Devices, these improved circuits operate over wider dynamic ranges with better log conformity than most other techniques available. Reduced cost and compact circuitry are other user benefits of this design approach.

Logarithmic Circuits and Sources of Error: Voltage and current log amplifiers are identical in design, except for an input voltage summing resistor, and operate on the input current supplied directly to terminal I_{IN} . The obvious sources of error for log amplifiers arise from three areas: 1) amplifier offset and drift errors, 2) log conformity errors and 3) frequency limitations. These errors restrict both the static and dynamic range of performance.

Voltage and current offsets of the input amplifier, with their attendant drift and noise, limit the smallest value of input signal to be detected. Base spreading resistance of antilog transistor elements, on the other hand, set the maximum signal level for a given accuracy.

For completeness, offset error and drift terms are expressed by the transfer function in the specification table. From the table, it becomes apparent that voltage offset (E_{os}) should be trimmed to a small value compared to the lowest level of input voltage to be processed. For example, if E_{IN} is 1mV and E_{os} is 1/20 (50 μ V or 5%) of E_{IN} , the output error is compressed to 2% of a decade (log 1.05 = 2).

Assuming that offset and base resistance errors did not exist, there would still remain the question of how well the logging element conforms to the ideal log transfer characteristic. This is defined as log conformity and is expressed as a percent of the input signal. Typical nonlinearity (i.e. departure from a straight line on a semilog plot) ranges from 0.5% to 1% over several decades of signal change. This adds to those errors arising from the voltage offset and drift terms described above.

Since the gain-bandwidth product of the logging element is relatively constant, a change in gain will vary the bandwidth. This gain change occurs as the input current to the logging element varies with signal level. Consequently, frequency response and slew rate are specified as a function of signal level and will vary accordingly. At higher currents, amplifier frequency response is usually the limiting factor and not log elements.

Circuit Configurations: Shown below, with their appropriate transfer functions, are log and antilog amplifier configurations for models 755 and 752. Note that model 755 has an adjustable scale factor (2V, 1V, or 2/3V/decade) which is selected with external pin connections. The corresponding transfer curves for these circuit configurations are presented on the following page.

Each model, available from Analog Devices (models 755, 752, 751), is specified with an N or P suffix for operation with positive or negative input signals, respectively. It should be recalled that the log of zero is asymtotic; the appropriate polarity module is required depending upon whether the input signal is positive or negative.

LOG OF VOLTAGE/CURRENT: MODEL 755N

755(N) "K" SCALE FACTOR SELECT R ANTILOG +EIN O 1 ELEMENT $10k\Omega$ IIN O EOUT 0 **O** TRIM

LOG OF VOLTAGE/CURRENT: MODEL 752N



ANTILOG OF VOLTAGE: MODEL 755 OR 752



IDEALIZED TRANSFER FUNCTIONS

$$e_{out} = -K \log_{10} \frac{e_{in}}{E_{REF}} ; \text{log of voltage}$$
$$e_{out} = -K \log_{10} \frac{i_{in}}{I_{REF}} ; \text{log of current}$$

; log of current

 $e_{out} = E_{REF} \ 10^{-ein/K}$; antilog of voltage

LOGARITHMIC AMPLIFIERS AND ELEMENTS MODELS 755, 752, 751, 756

MODEL 755, COMPLETE LOG/ANTILOG AMPLIFIER

The model 755, a complete logarithmic amplifier with FET input, provides a choice of six decades of current logging (1nA to 1mA), or four decades of voltage logging (1mV to 10V). For increased flexibility, three scale factors (2V, 1V, 2/3 V/decade) and log or antilog operation may be selected through appropriate terminal pin connections. When two such amplifiers are connected in tandem, as a log and antilog amplifier, a wide range of fractional powers and roots may be developed for computational purposes. The model 755 offers the greatest value in a complete log/antilog amplifier and is the first choice for the application. Specify 755N for positive, and 755P for negative input signals, respectively.

MODEL 752, VERSATILE LOG/ANTILOG AMPLIFIER ELEMENT

The model 752, when operated with an external FET amplifier (e.g., model 40J), will perform over the same input dynamic range as the 755; six decades of current (1 nA to 1 mA) and four decades of voltage (1 mV to 10V). The module contains a temperature compensated log element and scaling resistors for good performance and 1V/decade sensitivity. Using an external input resistor and two adjustment pots, the scale factor, reference current and input dynamic range may be varied to suit a specific log or antilog application.

Another key feature of model 752 is the design freedom available to the user. He may select the best amplifier to optimize his design. For example, when used with a chopper stabilized amplifier (e.g., 233J), offset voltage errors are minimized for the most demanding applications. For economy, combining 752 with a general purpose FET amplifier (model 40J) will provide good current or voltage performance at prices below that of model 755. Specify 752N or 752P for use with positive or negative input signals, respectively.

MODEL 751, TEMPERATURE COMPENSATED LOG ELEMENT

Model 751, a log element building block, is considered the best choice for performance and economy when developing log ratio circuits as well as any other general purpose logcircuit. The 751 contains temperature compensated logging transistors with precision scaling networks which together yield a 1 volt per decade log ratio amplifier when combined with three op amps and several other components. Detailed application notes are available from Analog Devices to aid in applying 751 to a wide variety of circuit designs. Specify 751N for positive input signals or 751P for negative signals.

MODEL 756: NEW LOG RATIO MODULE

Capable of either current log ratio or voltage log ratio, the model 756 is the first module of its kind to be offered to the industry. This design consists of a complete log ratio module with two continuously variable signal inputs. Channel 1 features a high quality, 10pA bias current FET amplifier that is capable of processing up to four decades of input current. The second channel, intended to be used as a reference,



is also capable of signal processing, but the range is limited to 3 decades.

Designed primarily for photometer applications, model 756 replaces two log modules, a subtractor, and associated circuitry. The signal sources for these applications are usually photo diodes which should be operated in the zero-volt mode (short circuit current). When connected as shown in Figure 2, the summing junctions provide virtual grounds, thereby forcing the input currents to be the short circuit current of the photo diodes.

Principles of Operation

CURRENT LOG RATIO

Current log ratio is accomplished by model 756 when two currents, I_{sig} and I_{ref} , are applied directly to the input terminals. The two log amps process these signals providing voltages which are proportional to the log of their respective inputs. These voltages are then subtracted and applied to an output amplifier. The scale factor, when connected as shown, is 1V/dec. However, other scale factors may be achieved by using an external/feedback resistor for A_3 instead of the internal $15k\Omega$. The governing equation for this optional adjustment is:

$$R \approx \left(\frac{15k\Omega}{V}\right) K_{\text{DES}}$$

where R represents the total feedback resistance of A_3 , and K_{DES} is the desired scale factor.

As a specific example of gain setting assume it is desired to set the scale factor to 2V. For this application the feedback resistor must be approximately $\frac{15k\Omega}{V} \times 2V$ or $30k\Omega$. To accomplish this, the designer could either insert a $15k\Omega$ resistor from the output Pin to Pin 1, or he could leave Pin 1 open and connect a $30k\Omega$ resistor from Pin 2 to the output. In either case, the total feedback resistance is $30k\Omega$, and the desired scale factor will be achieved.

VOLTAGE LOG RATIO

The principle of operation for voltage log ratio is identical to that of current log ratio after the voltage signal has been converted to a current. To accomplish this conversion, an external resistor is attached from the voltage signal to the appropriate input current terminal of the 756. Input currents are then determined by:

$$I_{sig} = \frac{e_1}{R_1}$$
, $I_{ref} = \frac{e_2}{R_2}$



Log of Current



Plot of Output Voltage vs Input Voltage When Connected in Log Mode

Log of Voltage



SPECIFICATIONS (Typical @ 25°C and ±15VDC)

TRANSFER FUNCTIONS	DYNAMIC RANGE
Log of Voltage	80dB
$e_{out} = -K \log_{10} \frac{e_{in} - E_{OS}}{E_{REF}}$	10^{-3} V $\leq e_{in} \leq 10$ V
Log of Current	120dB

 $e_{out} = -K \log_{10} \frac{i_{in} - I_{OS}}{I_{REF}}$

Antilog of Voltage

 $e_{out} = E_{REF} 10^{-ein/K} \pm e_{os}$

$$10^{-3}$$
 V $\leq |e_{out}| \leq 10$ V

 $10^{-9} A \le |i_{in}| \le 10^{-3} A$

TRANSFER FUNCTION COEFFICIENTS (ALL MODELS)

Symbol	Value	Tolerance	Drift	See Notes
K =	2, 1, 2/3 V	±1%	±0.04%/°C	1, 2, 5
$E_{REF} =$	$10^{-1} V$	±2%	±0.05%/°C	1, 3, 5
$I_{REF} =$	10^{-5} A	±2%	±0.05%/°C	1, 3, 5
$E_{OS} =$	$0 V \pm tol.$	±400µV	$\pm 10 \mu V/^{\circ} C$	4
$I_{OS} =$	O A ±tol.	0, -10pA	$2 \text{ X}/10^{\circ} \text{C}$	4

ACCURACY OF LOG CONFORMITY (REFERRED TO INPUT) ALL MODELS

Input Current Range	Accuracy	Input Voltage Range	Accuracy	
1 nA to 10nA	±1%	1 mV to $1 V$	+0.5%	
100μ A to 1 mA	±1%	1 V to 10V	±1%	

NOTES:

- 1. Positive for positive input (N types), negative for negative inputs (P types).
- For model 755, select by external pin connections. For model 752, adjust externally from .5V.
- 3. Model 752; IREF, EREF are externally adjustable.
- 4. For 752 and 751, offset is a function of external op amp selection.
- 5. Parameter is a function of 751 log circuit design.

MODELS (N & P TYPES)	755	752/751
Small Signal Frequency Response of <i>i</i> _{in} (- 3dB down)		
10 ⁻⁹ A	80Hz	80Hz
10^{-7} A	1 kHz	1 kHz
10^{-4} A	40kHz	Depends on op amp
10^{-3} A	200kHz	Depends on op amp
Rated Output	±10V @ 5mA	Depends on op amp
Power Supply	±15VDC ±1% @ 10mA	Depends on op amp
Temperature, Rated		
Performance	$0 - 70^{\circ}C$	$0 - 70^{\circ}C$
Package Style	F-4	QB-2/M-3
Price (1–9)	\$55.	\$32.
(10-24)	\$49.	\$28.

Specify P Type for Negative Inputs; N Types for Positive Inputs.
SPECIFICATIONS FOR MODEL 756 N/P

Current Log Ratio Transfer Equation

$$e_0 = -K \log \frac{i_1}{i_2}$$
, $i_1 = sig$
 $i_2 = ref$

 $e_0 = -K \log \left| \frac{e_1}{e_2} X \frac{R_2}{R_1} \right|$

Transfer Equation including Error Terms

Transfer Equation including

$$e_0 = -K \left[log \left(\frac{i_1 - I_{b1}}{i_2 - I_{b2}} \right) + E_{os3} \right]$$

Voltage Log Ratio Transfer Equation

$$e_{0} = -K \left[log \left(\frac{\frac{e_{1} - E_{os1}}{R_{1}} - I_{b1}}{\frac{e_{2} - E_{os2}}{R_{2}} - I_{b2}} \right) + E_{os3} \right]$$

Parameter

Error Terms

Signal Current, i₁¹ Reference Current, i₂¹ Log Conformity²

Scale Factor, K^{1,3} Bias Current, I_{b1} Bias Current, I_{b2} Offset Voltage, E_{0s1} ³ Offset Voltage, E_{0s2} Output Offset, E_{0s3} ³ Package Style Price (1-9) Value

10nA to 100 μ A (4 decades) 100nA to 100 μ A (3 decades) ±0.5% (2 decades, i₂ constant) ±1.0% (4 decades, i₂ constant) 1V ±1% ±0.04%/°C 10pA, doubles/10°C 10nA, max, ±1%/°C ±1mV, max, 25 μ V/°C 0.5mV, max, 30 μ V/°C max ±10mV, max, 85 μ V/°C F-6 \$75.

¹ Positive for positive inputs (N type), negative for negative inputs (P type).
² The log conformity specification is referred to input (R.T.I.). Note: 1% error R.T.I. is equivalent to 4.3mV of error at output for K = 1V.
³ Externally trimmable.





Figure 2. Photometry Application of Model 756

ACCESSORIES MODULAR POWER SUPPLIES



900 SERIES: GENERAL PURPOSE POWER SUPPLIES The 900 series power supplies from Analog Devices have been widely accepted by designers as industry standards for reliability and performance. Useful in industrial and laboratory applications, these companion products to op amps are capable of delivering clean, well regulated power to IC and discrete op amps, digital converter products, and to transducer elements.

All designs are line operated with domestic and international voltage ratings offered. Available models feature short circuit protection with either +5VDC single output (with over-voltage protection) or ± 15 VDC dual output. Current output is ± 25 mA to ± 200 mA for dual outputs and 500mA and 1 amp for single outputs. To service its customers, Analog Devices maintains an off-the-shelf stock for immediate delivery. Substantial OEM discounts are available.

MPD SERIES: PRECISION POWER SUPPLIES

Analog Devices "MPD" series of power supplies are intended for applications where the extraordinary performance is required. These feature excellent regulation and low temperature coefficients. These devices may be used as stable references for the most demanding requirements in laboratory grade designs.

All MPD supplies are sealed in anodized aluminum enclosures for maximum ruggedness and minimum RFI. Employing switching techniques for high efficiency, these units feature low "see through" capacitance (typically 20pF) and are desirable for delivering isolated power to "floated circuits" and for use in systems having considerable ground noise.

900 SERIES, GENERAL PURPOSE							
Model	±15VDC Dual Op Amp Supplies 915 904 902		920	+5VDC Logic Supplies 903 905			
Rated Output Voltage	±15VDC (a) ±25mA	±15VDC (a) ±50mA	±15VDC (a) ±100mA	±15VDC @ ±200mA	+5VDC (a) +500mA	+5VDC (a) +1 amp	
Rated Input Voltage		105VAC to 125VAC ¹ 50Hz to 400Hz			105VAC t 50Hz t	o 125VAC ¹ to 400Hz	
Output Error (max) Regulation 105 to 125VAC Load, 0 to 100%	±1% 0.2% 0.2%	+200mV, =0mV 0.1% 0.1%	+300mV, -0mV 0.05% 0.1%	+300mV, -0mV 0.05% 0.1%	±1% 0.15% 0.3%	±1% 0.05% 0.1%	
Temperature Coefficient (/°C) Operating Temperature (°C) Warm Up Drift	0.02% -25 to +71 30mV	0.015% 0 to +71 ² 37mV (max)	0.015% 0 to +71 ² 45mV (max)	0.015% 0 to +71 ³ 45mV	0.02% 0 to +71 ³ 15mV	0.02% -25 to +71 ³ 40mV	
Ripple & Noise rms (max)	1 mV	0.5mV	0.5mV	0.5mV	1 mV	1 mV	
Short Circuit Protected Overvoltage Protected	-	all outputs		_	all o +6.5VDC	utputs +6.5VDC	
Package Price (1-9) (10-24)	11A-1 \$23. \$22.	11A-1 \$39. \$38.	H-2 \$49. \$47.	H-2 \$69. \$62.	H-2 \$49. \$47.	H- 2 \$69. \$66.	

SPECIFICATION SUMMARY (Typical @ 25°C and 115VAC unless otherwise noted)

MANIFOLDS



MODEL 194



MODEL 950: POWER SUPPLY MANIFOLD

This manifold permits use of the 900 series "H" cased modules on the design bench. In combination with these supplies the 950 provides a safe, convenient, and inexpensive bench supply for breadboarding, testing, or general laboratory use. Price is \$16 each (1-9).

MODEL 194 OPERATIONAL AMPLIFIER MANIFOLD The Model 194 manifold is ideal for experimenting, breadboarding, and/or teaching with op amps. Completely selfcontained, it includes a ±15VDC 100mA power supply, and accepts up to 5 amplifiers in the popular 7-pin "Q" case configuration, in sizes up to 1.5 inch square. Adapters are available for integrated circuits such as the Analog Devices AD741K or AD502 IC op amps. Provisions are made for a balance potentiometer for each amplifier. The unit is designed for maximum flexibility, with all connection points ¾ inch apart. Price is \$250 each (1–9), substantially less in higher quantity.

MPD SERIES, PRECISION REGULATED

±15VDC Dual Supply		+5VDC Logic Supply			
MPD 15/100A MPD 15/300A		MPD 15/300A MPD 5/150A			
±15VDC ⁴ @ ±100mA	±15VDC ⁴ @ ±300mA	+5VDC ⁵ , +150VDC 600mA, 5mA	+5VDC ⁵ @ 750mA		
105VAC 50Hz t	to 125VAC o 450Hz	105VAC to 125VAC 50Hz to 450Hz			
adju	stable	adjust	able		
0.005% 0.02%	0.005% 0.02%	0.005% 12.5mV	0.005% 12.5mV		
0.015% max -55 to +71 -	0.015% max -55 to +71 ⁶ -	0.015% max -55 to +71 -	0.015% max -55 to +71		
1mV	1mV	2mV	2mV		
to gr	round	+5VDC to ground	to ground		
-	-	-	_		
\$149.	\$275.	\$149.	\$149.		
\$141.	\$260.	\$141.	\$141.		

NOTES:

- 1. Specify: E option 220VAC ±10% (Europe) H option 240VAC ±10% (U.K.) F option 100VAC ±10% (Japan)
- 2. Derate $5 \text{mA/}^{\circ}\text{C}$ above $+55^{\circ}\text{C}$, $1 \text{ mA/}^{\circ}\text{C}$ below $+10^{\circ}\text{C}$.
- 3. Derate $12\text{mA/}^{\circ}\text{C}$ above $+50^{\circ}\text{C}$, $10\text{mA/}^{\circ}\text{C}$ below $+15^{\circ}\text{C}$.
- 4. Individually adjustable, ± 14 VDC to ± 16 VDC.
- 5. Adjustable, +4.7V to 5.3V.
- 6. Derate $7 \text{mA/}^{\circ} \text{C}$ above $+55^{\circ} \text{C}$.



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LINEAR INTEGRATED CIRCUITS

INTRODUCTION

The integrated circuits specified on these pages are indicative of a commitment to product expertise in I.C. technology coincident with Analog Devices' position of leadership in analog and converter modules. Achieving the optimum price/performance product is our goal; combining more than seven years of analog product design is our vehicle. In addition to that expressed by our products, our IC commitment is manifested in two other important ways . . . communication and cooperation.

Because we manufacture devices that are a cut above the usual IC in performance and applicability, and because we realize that your interest in these products is indicative of your need for excellent system performance, our service goes beyond product, price and delivery.

To get the most out of our circuits, you must clearly know how best to use them. This dictates the need for a high level of communication . . . provided by the completeness of our product data sheets and application notes, and by a team of circuit design-oriented engineers who are well versed in solving product and applications problems. And if our products are not specified exactly as required by your system application, if a max drift must be lower or a minimum gain higher, or if you need special device processing, we are ready to cooperate to meet your requirement.

Our broad line of I.C. products is presented in this section for the designer who specifically requires microcircuit products. For applications in which the choice of microcircuits is not dictated, these products are also presented on a functionally comparative basis with Analog Devices' modular amplifiers and multipliers in these product sections.

Introductory to the product descriptions, we have provided below: a brief overview of our current state-of-the-art production capability; a product line profile; and an abbreviated reference to the MIL 883 reliability standard to which our I.C.'s adhere.

I.C. TECHNOLOGY AT ANALOG DEVICES

Our broad line of linear I.C.'s is produced with a combination of design, processing, test capabilities, and innovations, with stringent process control.

Active-operation laser trimming of thin-film resistors deposited on the monolithic chip is an IC technology breakthrough unique with Analog Devices. It is used to manufacture the AD532 internally trimmed monolithic multiplier and is a technique that will find wide applications in future IC designs. Conventional, laser trimming is also performed on thinfilm resistors deposited on ceramic substrates to permit FET op amp offset voltages to be specified below 1.0 millivolt.

Thin film deposition on monolithic chips results in resistors that match within 50ppm and track within 5ppm to

produce voltage drifts below $0.5\mu V/^{\circ}C$ and multiplication error below 2% over the military temperature range.

Dual FET fabrication on a single chip employs uniformed epitaxy, low dislocation diffusion techniques, and silicon nitride passivation. This produces devices with ultra low gate leakage currents below 0.1pA, extremely low noise, tight matching characteristics, with linear tracking over temperature guaranteeing a temperature drift nonlinearity (TDN) of $\pm 1\mu V/^{\circ}C$.

Super beta transistors produce gains of 2500 to 3000 with breakdown voltages of 20 to 35 volts.

Hybrid assembly techniques provide circuits that combine the best individual characteristics of FET and bipolar chips into operational amplifiers that offer 250 femtoamp input currents and 6 volt/µsec slew rates.

Thermal balancing of the chip layout is a primary design criteria for all circuits to minimize the effects of power dissipation which causes thermal feedback that mismatches the critical input stage.

Stringent in-process control and 100% stress conditioning include pre-cap visual chip and bonding inspection, high temperature storage, high impact acceleration, and temperature cycling to eliminate defective units before they reach the customer.

Computerized and fully automatic equipment tests the circuits for all guaranteed DC parameters, and combines with a user-oriented philosophy to produce such nononsense criteria as measuring FET op amp gain with the offset voltage automatically nulled, and measuring multiplier accuracy in all four quadrants at three temperatures.

Thus, Analog Devices has uniquely combined the numerous design, processing, and manufacturing capabilities necessary to produce its broad line of high performance integrated circuits.

PRODUCT PROFILES

The I.C. product line is divided into eight main groups: FET input op amps; high accuracy op amps; instrumentation amplifiers; fast, wideband op amps; general purpose DC op amps; conversion components; multiplier/dividers; and dual transistors. These groups are subdivided into more than three dozen product series with more than 250 standard variations.

FET Input Operational Amplifiers

The AD503, AD506, AD513, AD516, AD523, and AD540 series all share the common functional characteristic of being able to accurately measure low level currents or small voltages from high impedance sources where bias current can be a primary source of error. Their FET inputs provide fully warmed up maximum bias currents as low as 0.25pA (AD523K), with offset voltages below 1.0mV (obtained with internal laser trimming) (AD506L), gains of 20k to 50k and CMRR's of 70 to 80dB. Offset voltage drifts with temperature are guaranteed as low as $10\mu V/^{\circ}$ C (AD506L), and vary very little with V_{OS} trimming. These amplifiers have a typical small signal bandwidth of 1.0MHz and a settling time to 0.1% of 10 μ sec. Higher first stage current levels permit minimum slew rates of 3.0V/ μ sec (AD513) where external compensation is possible.

High Accuracy Operational Amplifiers

The AD504 and AD508 series, and the AD301AL and AD741 J/K/L/S are specially designed, processed, and tested to achieve the highest possible accuracy and stability with both temperature and time, and permit error budgets as low as a few parts per million at surprisingly low cost. They provide gains ranging from 50k to more than 1 million (AD504, AD508), offset voltages as low as 0.5mV, offset voltage drifts from $20\mu V/^{\circ}C$ to below $0.5\mu V/^{\circ}C$, bias currents from 200nA to less than 10nA (AD508), offset currents as low as 1.0nA, and minimum CMRR's from 80 to 110dB. Typical noise is 1.0 to $3.0\mu V$ (p-p) in the 0.01Hz to 10Hz bandwidth, and the AD504M guarantees maximum 0.6µV (p-p) noise from 0.1 to 10Hz. An added benefit of the thermally balanced design of these amplifiers is their excellent output performance of up to $\pm 10V$ minimum into a $1k\Omega$ load at $+70^{\circ}$ C. Although these amplifiers are basically 300kHz to 1.0MHz small signal bandwidth devices, several are externally compensated, permitting considerable variation in bandwidth and slew rate.

Instrumentation Amplifiers

The AD520 is the first IC instrumentation amplifier. It is closed loop gain block with differential inputs and an accurately predictable input-to-output gain relationship. The AD520's performance is unlike that of conventional IC op amps because of an internal feedback design which permits gain adjustment from 1 to 1000 by varying the value of a single resistor. High Z_{in} is achieved at both inputs and both Z_{in} and CMRR remain high at all gain settings.

Fast, Wideband Operational Amplifiers

The AD505, AD507, AD509 and AD518 operational amplifiers are specifically designed for applications requiring wide bandwidth, high slew rate, fast settling time to high accuracy, predictable operation and low cost. Their excellent ac performance is characterized by small signal bandwidths up to 35MHz (AD507), slew rates above $120V/\mu$ sec (AD505), and settling times guaranteed below 2μ sec to 0.01% (AD509K). A high level of dc accuracy is maintained with gains above 80k, offset voltages below 5.0mV, and input bias currents below 75nA. Because these amplifiers are optimized for wideband, fast settling operation, certain practical stabilization and interconnection techniques are described in their specification sheets to insure proper operation and to minimize user experimentation.

General Purpose DC Operational Amplifiers

The AD101A, AD108, AD108A, AD502, and AD741 operational amplifiers are characterized by good to excellent dc performance provided by medium gain of 20k to 50k, offset voltages below 7.5mV, bias and offset currents as low as 0.2nA (AD108/108A), and common mode rejection ratios above 80dB. They typically have a small signal bandwidth of 1.0MHz, slew rates of 0.3 to $1.0V/\mu$ sec, and settling times to 0.1% of 10 μ sec. Several of them are externally compensated, and their ac performance can be significantly improved by applying various compensation schemes. In keeping with their general purpose applicability, these amplifiers are supplied in a number of packages, including the TO-99 metal can, TO-116 ceramic DIL, plastic mini-DIP, and TO-91 flat package.

Multipliers/Dividers

The AD530, AD531, and AD532 provide Analog with several IC multiplier firsts. The AD530 is the industry's first IC multiplier to include the transconductance multiplying element, stable reference, and output amplifier on a single monolithic chip. The AD531 is the first to provide a variable scale factor, and the AD532 is the first internally trimmed monolithic multiplier. The devices multiply and square in 4 quadrants; divide in 2 quadrants, and square root in one quadrant; the AD530 and AD532 with a fixed scale factor of 10, and the AD532 with a variable scale factor of kIz in volts. When multiplying, the AD530 provides the transfer function $V_{OUT} = V_X \cdot V_Y / 10$, the AD532, because of its differential inputs, $V_{OUT} = (V_{X_1} - V_{X_2}) (V_{Y_1} - V_{Y_2})/10$, and the AD531 $V_{OUT} = V_X \cdot V_Y / V_Z$ with V_Z set by an external resistor, or varied dynamically by an externally derived reference current. Both the AD530 and AD531 series are specified for max multiplying errors (with external trimming) as low as 0.5% at +25°C, 1.5% from 0 to +70°C, and 3.0% from -55°C to +125°C. The AD532 (requiring no external trimming) is specified for errors below 1% at +25°C, and 4% from -55°C to +125°C.

Conversion Components

Analog's IC conversion components, which are used in our own modular D/A and A/D converters, provide the user with a doit-yourself kit for the construction of very small and reliable D/A and A/D converters, which provide extremely high accuracy and resolution over the military temperature range. The components include integrated circuit switches and associated thin-film resistor networks which form the heart of D/A and A/D converters having 8-to-12-bit accuracy.

Four basic series are available: the AD550 and AD551 quad switches and the AD552 quint switch use current switching techniques, and are recommended where speed and accuracy requirements are paramount; the AD555 quad voltage switch is optimized for applications where both digital and analog signals vary, such as digital-to-synchro conversion or multiplying DAC applications.

Compatible thin-film resistor networks for binary current summing are also available: the AD850 (12-bit resolution), and the AD852/853 (8 bits/4 bits) set for use with the AD550, AD551 and AD552; the AD855 is a 12-bit R/2R network for voltage switching, and is used with the AD555.

Monolithic Dual Transistors

A complete line of low cost dual monolithic NPN and PNP transistors is available with excellent matching characteristics (0.5mV max) and exceptional high current gain (500).

Also available is an exclusive line of super beta transistors (beta's of 1000 to 3000) with outstanding breakdown voltages of 20 to 35 volts. These combined specs are nowhere else available!

To aid the circuit designer, Analog Devices developed a dual monolithic NPN transistor especially suited for logarithmic converters and computational circuits. This transistor, the AD818, is also unique with its extremely low voltage noise specification and low collector saturation voltage.

Dual Monolithic TRAK-FET's

The AD820, AD840, AD5906 and AD3954 Series are the result of recent breakthroughs in monolithic junction FET processes. The use of proprietary deposited diffusion techniques provide gate diffusion uniformities unattainable from standard gas diffusion sources. The inherent advantages of the TRAK-FET's are exhibited in low gate leakage, excellent drift linearity with temperature and tight G_{fs} and Y_{os} matching.

Unique characteristics are displayed by the AD830 Series where the gate leakage current is extremely low, 0.1pA max, while the AD840 Series show outstanding low noise specifications, $15nV/\sqrt{Hz}$ max at 10Hz.

MIL STANDARD 883

Analog Devices manufactures its modular, converter, and integrated circuit products to standards of quality that meet and consistently exceed our customers' requirements for high reliability applications in military, aerospace, instrumentation, and industrial systems. Because of their hermetically sealed packages, low component count, and minimum number of interconnections, integrated circuits offer the highest inherent reliability to the user. We optimize this reliability by adherence to exact manufacturing control, and to the processing and inspection requirements of MIL-STD-883, a government processing, testing, and inspection standard that defines the following levels of screening for integrated circuits.

- 1. Class A "Devices intended for use where maintenance and replacement are extremely difficult or impossible and reliability is imperative."
- 2. Class B "Devices intended for use where maintenance and replacement can be performed, but are difficult and expensive, and where reliability is vital."
- Class C "Devices intended for use where maintenance and replacement can be readily accomplished and downtime is not a critical factor."

Further guidance is provided:

"Since it is not possible to prescribe an absolute level of quality or reliability which would result from a particular screening level or to make a precise value judgment on the cost of a failure in an anticipated application, three levels have been arbitrarily chosen. The method provides flexibility on the choice of conditions and stress levels to allow the screens to be further tailored to a particular source, product or application based on user experience. The user is cautioned to collect experience data so that a legitimate value judgment can be made with regard to specification of screening levels. Selection of a level better than that required for the specific product and application will, of course, result in unnecessary expense and a level less than that required will result in an unwarranted risk that reliability and other requirements will not be met. In the absence of specific experience data, the Class B screening level is recommended for military applications."

Where particularly specified by the user, Analog Devices will supply its integrated circuits screened to Class A, B or C of MIL-STD-883 Method 5004. Standard highreliability products, denoted by a /883 suffix on the part number (e.g., AD530S/883), are screened to Level B.

new product: AD506L

HIGH ACCURACY FET-INPUT OP AMP AD506



GENERAL DESCRIPTION

The AD506J, AD506K, AD506L and AD506S are high accuracy FET-input op amps which combine the low current characteristics typical of FET amplifiers with the low initial offset voltage and offset voltage stability of bipolar amplifiers. Active laser trimming and close matching of circuit elements provide maximum warmed-up offset voltage below 1.0mV, maximum offset voltage drift of $10\mu V/^{\circ}C$, and warmed-up bias current

below 5pA max. Other excellent characteristics include open loop gain above 75,000 and minimum CMRR of 80dB. User-oriented circuit design and testing philosophy insure that full advantage can be taken of the high performance specifications of the AD506. Offset voltage nulling is accomplished without affecting the operating current of the FET's and results in small changes in temperature drift characteristics. For example, the drift induced by nulling the AD506 is only $\pm 0.8 \mu V/^{\circ}$ C per millivolt of nulled offset voltage. Further, the AD506 is guaranteed to meet its maximum Ib and VOS specs after full device warm-up caused by self-heating of the chip due to internal power dissipation. The bias current is specified as a maximum at each input, not as the average of the two inputs. Finally, gain is measured with the offset voltage nulled. Nulling a FET-input op amp can cause the gain to decrease below its specified limit. The minimum gain of the AD506 is guaranteed with VOS both nulled and unnulled. All models are supplied in the TO-99 metal can package. The AD506J, K and L are specified for operation from 0 to +70°C; the AD506S from -55°C to +125°C.

ELECTRICAL SPECIFIC	ATIONS (Typica	l at $+25^{\circ}$ C and	±15VDC, unless	otherwise noted)
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Parameter	AD506J	AD506K	AD506L	AD506S
Open Loop Gain (Note 1)				
$V_{OUT} = \pm 10V, R_I \ge 2k\Omega$	20,000 min	50,000 min	75,000 min	50,000 min
$T_A = \min to \max$	15,000 min	40,000 min	50,000 min	25,000 min
Output Characteristics				
Voltage @ $R_1 = 2k\Omega$, $T_A = \min to \max$	±10V min	•		
(a) $R_{L} = 10k\Omega$. $T_{A} = \min to \max$	±12V min	•	•	•
Load Capacitance (Note 2)	1000pF			
Short Circuit Current	25mA			
Frequency Response				
Unity Gain Small Signal	1.0MHz			
Full Power Response	100kHz			
Slew Pate Unity Cain	3 OV/usec min			
Settling Time Unity Gain	10usec			
Secting Thic, Only Gan	Topsee	1.5.11	10.11	
input Offset Voltage (Note 3)	3.5mV max	1.5mV max	1.0mV max	1.5mV max
vs. remperature, $!_A = \min to \max$	$75\mu V/C max$	$25\mu V/C max$	10µV/ C max	50µV/ C max
vs. Supply, $T_A = \min to \max$	$200\mu V/V max$	$100\mu V/V max$	$100\mu V/V max$	$100\mu V/V max$
Input Bias Current				
Either Input (Note 4)	15pA max	10pA max	5pA max	10pA max
Input Impedance				
Differential	$10^{11} \Omega 2 pF$	•		•
Common Mode	$10^{12} \Omega 2 pF$	•		•
Input Noise				
Voltage 0 1Hz to 10Hz	$15\mu V(p-p)$	•		•
f = 10Hz	280nV/1/Hz			•
f = 100 Hz	70nV/2/Hz			
f = 1kHz	25nV/2/Hz			•
I - INIL	251117 VII2			
Input Voltage Range	+417			
Differential	±4V ±10V ==:=			
Common Mode, $I_A = \min to \max$			00 ID'-	eo ID
Common Mode Rejection, $v_{in} = \pm 10v$	70dB min	SOUD IIIII	80dB min	and min
Power Supply	41.537			
Rated Performance	±15V			+/5 - 22)11
Operating	±(5 to 18)V			±(5 to 22)V
Quiescent Current	7mA max	•		
Temperature	0			
Operating, Rated Performance	0 to +70°C	•		-55°C to +125°C
Storage	-65°C to +150°C	•		•
Price (1-24)	\$13.00	\$15.50	\$24.00	\$26.50
(25-99)	\$11.00	\$12.80	\$19.20	\$21.80
(23-77)	\$11.00	411.00	417.20	417 (0

1.0pen Loop Gain is specified with V_{OS} both nulled and unnulled. 2.A conservative design would not exceed 750pF of load capacitance. 3.Input offset voltage specifications are guaranteed after 5 minutes of operation at $T_A = +25^{\circ}$ C. 4.Bias current specifications are guaranteed after 5 minutes of operation at $T_A = +25^{\circ}$ C. For higher temperatures, the current doubles every $+10^{\circ}$ C. *Specifications same as for AD506J.

HIGH SPEED FET-INPUT OP AMPS AD513, AD516

GENERAL DESCRIPTION

The AD513 and AD516 high speed FET op amps combine high DC accuracy with excellent dynamic response by utilizing the flexibility of external compensation. With simple lag compensation, the AD513 and AD516 achieve slew rate of 20V/µsec, and gain bandwidth of 1MHz at unity gain and 10MHz for gains greater than 100. With feedforward compensation a slew rate of 50V/µsec and gain bandwidth of 30MHz can be achieved. High accuracy DC specifications include max bias current as low as 20pA, a minimum gain of 50,000, and CMRR of 80dB.

The AD513 is suggested for all general purpose FET input amplifier requirements where low cost and frequency response flexibility are of prime importance. The AD516, with specifications otherwise similar to the AD513, offers significant improvement in offset voltage by supplementing the AD513 configuration with internal laser trimming of thin film resistors to provide typical offset voltages below 1mV.

The devices are also fully short circuit protected and can be externally offset voltage nulled. All the circuits are supplied in the TO-99 package in the same pin configuration as the AD101A and AD108/108A. The AD513J/AD516J and AD513K/AD516K are specified for 0 to +70°C temperature range operation; the AD513S/AD516S for operation from -55°C to +125°C.



OFFSET NULL **Offset Nulling** Scheme

PIN CONFIGURATION

Top View

Gain (Inv)	1.	1	10	10	10	100	100
$R_1(\Omega)$	10k	10k	10k	1k	1k	1k	100
$R_2(\Omega)$	10k	10k	100k	10k	10k	100k	10k
C_1 (pF)	30	1	8	1	0	1	0
C_2 (pF)	0	12	0	12	8	0	39
C_3 (pF)	0	150	0	0	150	0	0
BW (kHz)	1000	1000	500	1000	1000	100	300
Slew Rate (V/µs)	5	50	20	30	50	6	15

ELECTRICAL SPECIFICATIONS (Typical @ +25°C and ±15VDC unless otherwise specified.)

raianietei	AD313J/AD310J	AD313K/AD310K	AD3133/AD3103	
Open Loop Cain (Note 1)				
$V_{\text{res}} = \pm 10 V_{\text{res}} \ge 2 k \Omega$	20.000 min	50.000 min	50.000 min	
$V_{OUT} = 10V, K_{L} > 2K_{H}$	15 000 min	40,000 min	40,000 min	
$\Gamma_{\rm A}$ = min to max	15,000 mm	40,000 mm	40,000 mm	
Output Characteristics				
Voltage at $R_L = 2k\Omega_L$, $I_A = min$ to max	±10V min	1		
at $R_L = 10k\Omega 2$, $I_A = min$ to max	±12V min		1	
Load Capacitance, Unity Gain (Note 2)	1000pF	•	•	
 Short Circuit Current	25mA	•	*	
Frequency Response				
Unity Gain, Small Signal (Feedforward)	1MHz			
Slew Rate, Unity Gain (Feedforward)	50V/µsec	*	•	
Input Offset Voltage (Note 3)	50mV max/3.5mV max	20mV max/1.5mV max	20mV max/1.5mV max	
vs Temperature, $T_A = \min to \max$	$75\mu V/^{\circ}C max$	$25\mu V/^{\circ}C$ max	$50\mu V/^{\circ}C$ max	
vs Supply, $T_A = \min to \max$	300µV/V max	$200\mu V/V max$	$200\mu V/V max$	
Input Bias Current				
Either Input (Note 4)	30pA max	20pA max	20nA max	
Input Impedance	rop	Tohrtman	a o pri man	
Differential	1011011201			
Common Mode	10 ¹¹ Oll2pF			
Input Noise	10 32/12/1			
Voltage 0 1Hz to 10Hz	154V (p-p)			
SHz to S0kHz	SUV (rms)			
f = 1 kHz (spot poise)	25nV/2/Hz			
I = TKHZ (spot hoise)	251117 9 112			
Differencial	1.211			
Common Made To anti-	±2VS			
Common Mode, $I_A = \min to \max$	±10V min			
 Common Mode Rejection, $V_{in} = \pm 10V$	70dB min			
Power Supply				
Rated Performance	±15V	•		
Operating	\pm (5 to 18)V			
Quiescent Current	7mA max	*		
Temperature			10	
Operating, Rated Performance	0 to +70°C		-55"C to +125°C	
Storage	-65°C to +150°C	•		
Price				
(1-24)	\$11.00/\$13.00	\$13.50/\$15.50	\$21.00/\$26.50	
(25-99)	\$9.00/\$11.00	\$10.80/\$12.80	\$16.80/\$21.80	
	CONTRACTOR AND	CONTRACTOR CONTRACTOR CONTRACTOR		

NOTES:

1. Open Loop Gain is specified with V_{OS} both nulled and unnulled.

*Specifications same as for AD5131

2. A conservative design would not exceed 500pF of load capacitance.

3. Input Offset Voltage specifications are guaranteed after 5 minutes of operation at $T_A = +25^{\circ}C$.

4. Bias Current specifications are guaranteed after 5 minutes of operation at TA = +25°C. For

higher temperatures, the current doubles every +10°C

GENERAL DESCRIPTION

The AD503 and AD540 IC FET-input op amps provide medium to high performance at low cost for all general purpose applications where the measurement of low-level currents, or small voltages from high impedance sources is a primary requirement. Despite their low cost, both models offer such benefits as bias current (maximum for either input) and offset voltage specified under fully warmed-up conditions, minimum gain guaranteed with the offset voltage both nulled and unnulled, and minimal variation in offset voltage drift with nulling. The AD503 series provides higher accuracy with maximum bias currents below 10pA, maximum offset voltage of less than 20mV, maximum offset voltage drift below $25\mu V/^{\circ}C$ and minimum CMRR above 80dB. At a lower price, the AD540 has only slightly reduced accuracy, and provides the additional



benefit of a differential input voltage range of ±20V. Both circuits have excellent dynamic performance, with typical slew rates of $6V/\mu$ sec, and are supplied in the TO-99 package for operation from 0 to +70°C and -55°C to +125°C.

ELECTRICAL SPECIFICATIONS (Typical at $+25^{\circ}$ C and ± 15 VDC, unless otherwise noted)

PARAMETER	AD503J	AD503K	AD503S	AD540J
Open Loop Gain (Note 1)				
Volum = ± 10 V. R ₁ ≥ 2 k Ω	20.000 min	50.000 min	50.000 min	20.000 min
$T_A = min \text{ to max}$	15.000 min	40,000 min	25,000 min	15,000 min
Output Characteristics				
Voltage @ $R_I = 2k\Omega$, $T_A = min$ to max	±10V min	*	*	*
(a) $R_I = 10k\Omega$, $T_A = min to max$	±12V min	*	*	*
Load Capacitance	750pF	*	*	*
Short Circuit Current	25mA	*	*	• 7.8
Frequency Response				
Unity Gain, Small Signal	1.0MHz	*	*	*
Full Power Response	100kHz	*	*	*
Slew Rate, Unity Gain	3.0V/µsec min	*	*	6.0V/µsec
Settling Time, Unity Gain (to 0.1%)	10µsec	*	*	
Input Offset Voltage (Note 2)	50mV max	20mV max	20mV max	50mV max
vs Temperature, $T_A = \min to \max$	$75\mu V/^{\circ}C max$	$25\mu V/^{\circ}C max$	$50\mu V/^{\circ}C max$	$75\mu V/^{\circ}C max$
vs Supply, $T_A = \min to \max$	$400\mu V/V max$	$200\mu V/V max$	$200\mu V/V max$	400µV/V max
Input Bias Current				The Providence of the Providen
Either Input (Note 3)	15pA max	10pA max	10pA max	50pA max
Input Impedance				
Differential	$10^{11} \Omega 2 pF$	*	*	*
Common Mode	$10^{12} \Omega 2 pF$	*	*	
Input Noise				
Voltage, 0.1Hz to 10Hz	15μV (p-p)	*	*	•
5Hz to 50kHz	5.0µV (rms)	*	*	*
f = 1 kHz (spot noise)	30.0 nV/ \sqrt{Hz}	*	*	
Input Voltage Range				
Differential	±3.0V	*	*	±20V
Common Mode, $T_A = \min to \max$	±10V min	*	*	
Common Mode Rejection, $V_{in} = \pm 10V$	70dB min	80dB min	80dB min	70dB min
Power Supply				
Rated Performance	±15V	*	*	
Operating	±(5 to 18)V	*	±(5 to 22)V	±(5 to 18)V
Quiescent Current	7mA max	*	*	
Temperature				
Operating, Rated Performance	0 to $+70^{\circ}$ C	*	-55° C to $+125^{\circ}$ C	$0 \text{ to } +70^{\circ}\text{C}$
Storage	$-65^{\circ}C$ to $+150^{\circ}C$	*	*	
Price				
- (1-24)	\$14.80	\$21.00	\$27.00	\$6.45
(25-99)	\$12.00	\$16.80	\$21.50	\$5.70
(100-999)	\$9.90	\$14.00	\$18.00	\$4.90

NOTES:

1. Open Loop Gain is specified with VOS both nulled and unnulled.

2. Input offset specs are guaranteed after 5 minutes of operation at $T_A = +25^{\circ}C$.

3. Bias current specs are guaranteed after 5 minutes of operation at $T_A = +25^{\circ}$ C. For higher temperatures, the current doubles every $+10^{\circ}$ C. *Specifications same as for AD503J.

ELECTROMETER FET-INPUT OP AMPS AD523

GENERAL DESCRIPTION

The AD523J, AD523K, and 523L are internally compensated FET input IC operational amplifiers that feature sub-picoamp bias current performance, low drift, high common mode rejection, and high gain. Maximum bias currents as low as 0.25pA under warmed-up operating conditions are achieved by combining matched small geometry FET chips with a specially designed monolithic chip within a low leakage TO-99 package. The package is manufactured with high resistivity glass insulation and a guard pin connected to the can to minimize surface leakage currents, power supply induced input noise, and capacitive pickup. The AD523 is fully short circuit protected and offset voltage nullable, and offers maximum voltage drift of $30\mu V/^{\circ}C$, minimum CMRR of 80dB, and minimum gain of 40,000 V/V. The AD523J, K, and L are specified for operation over the 0° C to $+70^{\circ}$ C temperature range.



ELECTRICAL CHARACTERISTICS (Typical @ +25°C and ±15VDC, unless otherwise noted) AD523J Parameter AD523K AD523L Open Loop Gain $V_{OS} \ge 0, R_L = 2k\Omega$ 20,000 min (50,000 typ) 40,000 min (75,000 typ) 40,000 min (75,000 typ) (a) $T_A = 0$ to $+70^{\circ}C$ 15,000 min 25,000 min 25,000 min **Output** Characteristics Voltage @ $R_L = 2k\Omega$, $T_A = 0$ to $+70^{\circ}C$ ±10V min (±12V typ) Current, $T_A = 0$ to $+70^{\circ}C$ ±5mA min Load Capacitance 1000pF Short Circuit Current 25mA Frequency Response Unity Gain, Small Signal 500kHz Full Power Response 50kHz Slew Rate, Unity Gain 3V/µsec min (5V/µsec typ) Input Offset Voltage 20mV max (10mV typ) Initial 50mV max (25mV typ) 20mV max (10mV typ) $90\mu V/^{\circ}C \max (25\mu V/^{\circ}C tvp)$ vs. Temp $T_A = 0$ to $+70^{\circ}C$ $30\mu V/^{\circ}C \max (15\mu V/^{\circ}C typ)$ $60\mu V/^{\circ}C \max (25\mu V/^{\circ}C typ)$ $200\mu V/V max$ $100\mu V/V max$ $100\mu V/V$ max vs. Supply Input Bias Current Initial, each input, Vdiff ≤4V (Note 1) -1.0pA max (-0.4pA typ) -0.5pA max (-0.2pA typ) -0.25pA max (-0.1pA typ) Input Impedance 10¹²||3pF Differential 10¹³||3pF Common Mode Input Noise Voltage, 0.01 to 1Hz 20µV p-p 5Hz to 50kHz 15µV rms Input Voltage Range Differential, max safe ±10V Common Mode Rejection @ ±8V $T_A = 0$ to $+70^\circ C$ 70dB min (80dB typ) 80dB min (90dB typ) 80dB min (90dB typ) Power Supply **Rated** Performance ±15V ±(5 to 18)V Operating ±7.0mA max (±5.0mA typ) Current, quiescent

Rated Performance	0 to +70 C	•	
Operating	-55°C to +125°C	*	· •
Storage	-65° C to $+150^{\circ}$ C	•	*
Prices (1-24)	\$21.00	\$25.00	\$28.00
(25-99)	16.50	20.00	22.50
(100-999)	14.00	16.75	18.75
NOTE 1: Bias Current specification doubles every +10°C.)	on guaranteed after 5 minutes of operation at T	$A = +25^{\circ}$ C. (For higher ambient	temperatures, the current

*Specifications same as AD523].

Temperature Range

FET-INPUT GENERAL PURPOSE OP AMPS AD501, ADM501, ADP501



ADM501



GENERAL DESCRIPTION

The Analog Devices Model AD501 is a microcircuit FET input operational amplifier that is supplied in the industrystandard axial-lead and plug-in molded packages, and in the hermetically sealed TO-8 type of package. The AD501 features offset voltages of less than 1mV, offset voltage drifts below $25\mu V/^{\circ}C$ and bias currents of less than 5pA. The circuits are manufactured with strictly controlled hybrid assembly techniques, which have proven their high reliability and fault-free performance through three years of system usage. The AD501 is supplied in the end-lead mini-package; the ADP501 in the bottom-lead mini-package; and the ADM501 in the TO-8-type package.

ELECTRICAL CHARACTERISTICS (V_S = $\pm 15V$, T_A = $\pm 25^{\circ}$ C,* unless otherwise noted)

M5	01A M501B	M501C		
00kΩ 2	2.0 1.0	1.0	mV	
25°C to 7 5°C	75 25	25	μV/°C	
(10pA	25 10 (M501)	5.0	pA	
5°C 2 (1pA/°	2.5 1.0 C M501)	0.5	pA/°C	
,	(10pA °C (1pA/°	25 10 (10pA M501) °C 2.5 1.0 (1pA/°C M501)	$\begin{array}{cccc} 25 & 10 & 5.0 \\ (10pA M501) \\ ^{\circ}C & 2.5 & 1.0 & 0.5 \\ (1pA/^{\circ}C M501) \\ \hline $	$\begin{array}{ccccccc} & 25 & 10 & 5.0 & pA \\ & (10pA M501) & & & \\ & & \\ & & \\ & & \\ & C & 2.5 & 1.0 & 0.5 & pA/^{\circ}C \\ & & \\ & & (1pA/^{\circ}C M501) & & \\ \end{array}$

	ALL DEV	ICES				
Parameter	Conditions	MIN	TYP	MAX	Units	
Large Signal Voltage Gain	$R_{L} \ge 2k\Omega$ $V_{\Omega} = \pm 10V$	25,000	100,000		V/V	
Input Resistance	Differential		10^{11}		Ω	
	Common Mode		10^{11}		Ω	
Input Capacitance			4		pF	
Input Noise Voltage (rms)	5Hz to 50kHz		6		μV	
Input Voltage Range		±10	±12		V	
Common Mode Rejection	$V_{IN} = \pm 5 V$		80		dB	
Supply Voltage Rejection			50		$\mu V / \%$	
Output Voltage Swing	$R_L \ge 10 k\Omega$	±12	±14		V	
	$R_{L} \ge 2k\Omega$	±10	±13		V	
Output Short Circuit Current	2		25		mA	
Supply Current				9	mA	
Slew Rate		3	5		V/μs	
Unity Gain Bandwidth			4		MHz	
Full Power Response	$\begin{array}{l} R_L \ge 2k\Omega, \\ V_O \ge 10V \end{array}$	70			kHz	
Price (1–9)	501	30.00	35.00	40.00	\$	
	P501	30.00	35.00	40.00	\$	
	M501	35.00	40.00	45.00	\$	

*Typical Junction Temperature (T_j) is 10°C above Ambient Temperature (T_A) after 15 minutes warm-up at V_S = ±15V. *Doubles every 10°C.

FET-INPUT GENERAL PURPOSE OP AMPS AD5II, ADP5II

GENERAL DESCRIPTION

The Analog Devices AD511 and ADP511 series of FETinput operational amplifiers are low cost pin-for-pin replacements for the 501 and P501, 20–008 and 20–108, C-118 and 140801 FET op amps. They feature offset voltages of less than 1mV, offset voltage drifts below $25\mu V/^{\circ}$ C, and bias currents of less than 5pA. The AD511 and ADP511 series are manufactured by combining separate specially designed monolithic bipolar amplifier and FET chips on a laser-trimmed thick-film substrate. This technique provides extremely high performance and reliability at a significant reduction in assembly cost – making possible a low selling price. The circuits are available in A, B and C specification variations for



operation over the -25° C to $+85^{\circ}$ C temperature range The AD511 is supplied in the end-lead mini-package; the ADP511 in the bottom-lead mini-package.

	C !!!!						
Parameter	Conditions	511A P511A	511B P511B	511C P511C	Units		
Initial Input Offset Voltage	$R_{S} \leq 100 k\Omega$	3.5	1.5	1.0	mV		
Average Temp Coef of Input Offset Voltage (max)	$T_A = -25^{\circ}C$ to +85°C	75	25	25	μV/°C		
Initial Input Bias Current		25	10	5.0	pА		
Average Temp Coef of Input Bias Current (typ)**	$T_A = 25^{\circ}C$	2.5	1.0	0.5	pA/°C		
	ALL DEV	ICES					
Parameter	Conditions	MIN	ТҮР	MAX	Units		
Large Signal Voltage Gain	$R_{\rm L} \ge 2k\Omega$ $V_{\rm O} = \pm 10V$	25,000	100,000		V/V		
Input Resistance	Differential		10 ¹¹		Ω		
	Common Mode		10 ¹²		Ω		
Input Capacitance			2		pF		
Input Noise Voltage (rms)	4Hz to 10kHz		7		μV		
Input Voltage Range		±10	±12		V		
Common Mode Rejection Ratio		70	86		dB		
Supply Voltage Rejection Ratio			100		$\mu V/V$		
Output Voltage Swing	$R_I \ge 10 k \Omega$	±12	±14		V		
	$R_{L} \ge 2k\Omega$	±10	±13		V		
Output Resistance	2		75		Ω		
Output Short Circuit Current			25		mA		
Supply Current				7	mA		
Slew Rate		3	5		V/µs		
Unity Gain Bandwidth			1		MHz		
Full Power Response	$\begin{array}{l} R_{L} \geq 2 k \Omega, \\ V_{O} \geq 10 V \end{array}$		70		k Hz		
Transient Response	$R_L \ge 2k\Omega$,						
Rise Time	$C_L^- \leq 100 pF$		300		ns		
Overshoot			5		%		
Overload Recovery			6		μs		
Price $(1-9)$		20.00	24.00	29.00	\$		
(10-24)		18.00	21.00	26.00	\$		

** Doubles every 10° C

LOW DRIFT, LOW NOISE OP AMP

GENERAL DESCRIPTION

The AD504J, AD504K, AD504L, and AD504M are moderately priced operational amplifiers which combine ultra-low drift and noise and extremely high gain with the frequency response and slew rate of general purpose I.C. op amps. A new double integrator circuit concept combined with a precise thermallybalanced layout achieves maximum nulled offset drift below $0.5\mu V/^{\circ}$ C, max input noise voltage of $0.6\mu V$ (p-p), and minimum gain of 10^6 . Unity gain small signal bandwidth is 300kHz and the slew rate is $1.2V/\mu$ sec at a gain of 10. The amplifier is externally compensated for unity gain with a single 390pF capacitor; no compensation is required for gains above 500. The AD504 has fully protected inputs, which permit differential input voltages of up to $\pm V_S$ without voltage gain or bias current degradation due to reverse breakdown. The output is also pro-



lew

roduct: AD504M

tected from short circuits to ground and/or either supply voltage, and is capable of driving 1000pF of load capacitance. All models are specified for operation over the 0 to +70°C temperature range, and are supplied in the TO-99 can package.

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MODEL	AD504J	AD504K	AD504L	AD504M
OPEN LOOP GAIN				
$V_{os} = \pm 10V, R_L \ge 2k\Omega$	250,000 min	500,000 min	10° min	10° min
(a) $T_A = 0^{\circ}C$ to $+70^{\circ}C$	125,000 min	250,000 min	500,000 min	500,000 min
OUTPUT CHARACTERISTICS				
Voltage @ $R_L \ge 2k\Omega$, $T_A = 0^{\circ}C$ to $+70^{\circ}C$	±10V min (±13V typ)	•	•	
Load Capacitance	1000pF	•	•	
Output Current	10mA min	•	•	
Short Circuit Current	25mA	•	•	
FREQUENCY RESPONSE				
Unity Gain, Small Signal, C _c = 390pF	300kHz	•	•	
Full Power Response, $C_c = 390 pF$	1.5kHz	•	•	
Slew Rate, Unity Gain, C _c = 390pF	$0.12V/\mu sec$	•	•	
INPUT OFFSET VOLTAGE				
Initial Offset, $R_S \leq 10k\Omega$	2.5mV max	1.5mV max	0.5mV max	0.5mV max
vs. Temp., $T_A = 0^\circ C$ to $+70^\circ C$, V_{OS} nulled	$5.0\mu V/^{\circ}C max$	$3.0\mu V/^{\circ}C max$	$1.0\mu V/^{\circ}C \max$	$0.5\mu V/^{\circ} C \max$
$T_{A} = 0^{\circ}C \text{ to } +70^{\circ}C,$				
Vos unnulled (Note 1)	$10\mu V/^{\circ}C \max$	$5.0\mu V/^{\circ}C max$	$2.0\mu V/^{\circ}C max$	$1.0\mu V/^{\circ}C \max$
vs. Supply	$25\mu V/V max$	$15\mu V/V max$	$10\mu V/V max$	$10\mu V/V$ max
(a) $T_A = 0^{\circ}C$ to $+70^{\circ}C$	$40\mu V/V$	$25\mu V/V max$	$15\mu V/V max$	$15\mu V/V max$
vs. Time	$20\mu V/mo$	$15 \mu V/mo$	$10\mu V/mo$	10µV/mo
INDUT OFFICET CURDENT				
POT OFFSET CORRENT	40nA max	15nA max	10nA max	10nA max
@ 1A - +25 C	Tomatimax	15 mr max	TOUT Max	Tonix max
INPUT BIAS CURRENT	200-1	100-1	00-1	00- A
	200nA max	100nA max	SUNA max	80nA max
(a) $I_A = 0$ C to +70 C	300nA max	150nA max	100nA max	100nA max
vs. Temp., $T_A = 0 C to + 70 C$	300pA/ C	250pA/ C	200pA/ C	200pA/ C
INPUT IMPEDANCE				
Differential	0.5MS2	1.0MS2	1.3MS2	1.3MS2
Common Mode	100M\$2 4pF	•	•	
INPUT NOISE				
Voltage, 0.1Hz to 10Hz	$1.0\mu V (p-p)$			$0.6\mu V (p-p) \max$
f = 100Hz	$10nV/\sqrt{Hz}$ (rms)			$10 \text{nV}/\sqrt{\text{Hz}(\text{rms}) \text{max}}$
f = 1 kHz	8nV/VHz (rms)			9nV/VHz (rms) max
Current, $f = 10Hz$	$1.0pA/\sqrt{Hz}$ (rms)			1.3pA/VHz (rms) max
f = 100Hz	0.6pA/VHz (rms)			0.6pA/VHz (rms) max
t = 1 kHz	0.5pA/VHz (rms)	*	•	0.3pA/VHz (rms) max
INPUT VOLTAGE RANGE				
Differential or Common Mode, max safe	±V _S	*	*	
Common Mode Rejection, $V_{in} = \pm 10V$	94dB min	100dB min	110dB min	110dB min
POWER SUPPLY				
Rated Performance	±15V.		*	
Operating	±(5 to 18)V	*	•	
Current, Quiescent	±4.0mA max	±3.0mA max	±3.0mA max	±3.0mA max
TEMPERATURE RANGE	2			
Operating, Rated Performance	0 to +70°C	•	•	
Storage	-65°C to +150°C	•	*	
PRICE				
(1-24)	\$11.20	\$19.80	\$28.00	\$30.00
(25-99)	9.55	16.80 .	21.80	23.80
	0.40	15 20	20.40	22.00

¹ This parameter is not 100% tested. Typically, 90% of the units meet this limit.

*Specifications same as for AD504J.

LOWEST COST HIGH ACCURACY OP AMPS AD30IAL, AD74IJ/K/L/S

GENERAL DESCRIPTION

The AD301AL and AD741J/K/L/S op amps provide the user with the highest possible performance achieved by the two most popular IC op amp series, combined with the lowest possible cost. Their performance approaches that of precision amplifiers, and offers the user the additional advantage of using op amps with which he is already familiar.

The AD301AL offers a 30% improvement in accuracy over the AD201A by reducing errors due to offset voltage (0.5mV max), offset voltage drift ($5.0\mu V/^{\circ} C$ max), bias current (30nA max), offset current (5nA max), voltage gain (80,000 min), PSRR (90dB min), and CMRR (90dB min).

The AD741J, AD741K, and AD741L substantially increase overall accuracy over the standard AD741C by providing maximum limits on voltage drift, and significantly reducing errors due to offset voltage, bias and offset currents, gain, PSRR and CMRR. Similarly, the AD741S provides considerably improperformance over the AD741 for wide temperature range ap plications. Results of a typical error analysis indicate a facto of 8 improvement in accuracy of the AD741L, a factor of 5 using the AD741K, and a factor of 2.5 using the AD741J. T AD741S achieves a 3.5 times improvement over the AD741.

All models are supplied in both the TO-99 metal can and molded minidip DIL packages.

AD301AL pin configurations same as standard AD101A seri (See page 169.) AD741 J/K/L/S pin configurations same as standard AD741. (See page 169.)

SPECIFICATIONS (Typical @ +25°C and ±15VDC, unless otherwise specified)

Model	AD301AL	Model	AD741J	AD741K	AD741L	AD741S
Open Loop Gain $V_0 = \pm 10V, R_L \ge 2k\Omega$ $T_{min/max}$	80,000 min 40,000 min	Open Loop Gain $R_L = 1k\Omega$, $V_O = \pm 10V$ $R_L = 2k\Omega$, $V_O = \pm 10V$	50,000 min	50,000 min	50,000 min	•
Output Characteristics Voltage, $R_L \ge 10k\Omega$, $T_{min/max}$ $R_L \ge 2k\Omega$, $T_{min/max}$ Short Circuit Current	±12V min ±10V min 25mA	Over Temp Range, T _{min/max} , same loads as above Output Characteristics Voltage @ R ₁ = 1kΩ, T _{min} /may	25,000 min ±10V min	•	•	•
Frequency Response Small Sig., A = 1, C _C = 30pF	1MHz	Voltage @ R _L = 2kΩ, T _{min/max} Short Circuit Current	25mA	±10V min *	±10V min *	
Feedforward F _P , C _C = 30pF Feedforward Slew Rate A = 1, C _C = 30pF Feedforward	10MHz 6kHz 150kHz 0.25V/µsec 9V/µsec	Frequency Response Unity Gain, Small Signal Full Power Response Slew Rate, Unity Gain	1MHz 10kHz 0.5V/µsec	÷	÷	:
Input Offset Voltage Initial, $R_S < 50 k\Omega$ vs. Temperature, $T_{min/max}$ vs. Supply @ $T_A = 0$ to $+70^{\circ}$ C	0.5mV max 5µV/°C max 90dB min 80dB min	Input Offset Voltage Initial, $R_5 \leq 10k\Omega$ $T_{min/max}$ Avg vs Temperature (untrim.)	3mV max 4mV max $20\mu V/^{\circ}C max$	2mV max 3mV max 15μV/°C max	0.5 mV max 1 mV max $5 \mu \text{V/}^{\circ} \text{C max}$	2mV max 15µV/°C max
Input Offset Current Initial @ T _{min/max} vs. Temperature, T _{min/max}	5nA max 10nA max 0.1nA/°C max	Input Offset Current Initial Tmin/max Avg vs Temperature	50nA max 100nA max 0.1 nA/ $^{\circ}$ C	$15\mu \sqrt{v}$ max 10nA max 15nA max $0.2nA/^{\circ}C$ max	$5 \mu \sqrt{v} \max$ $5 nA \max$ $10 nA \max$ $0.1 nA/^{\circ}C \max$	10nA max 25nA max 0.25nA/°C ma:
Input Bias Current Initial @ Tmin/max	30nA max 45nA max	Input Bias Current Initial	200nA max	75nA max	50nA max	75nA max
Input Voltage Noise f = 10Hz	35nV/√Hz	T _{min/max} Avg vs Temperature Input Impedance	400nA max 0.6nA/°C	120nA max 1.5nA/°C max	100nA max 1nA/°C max	250nA max 2nA/°C max
f = 1kHz	$28 \text{ mV}/\sqrt{\text{Hz}}$ $22 \text{ mV}/\sqrt{\text{Hz}}$ 1.5 MO min	Differential Input Voltage Range (Note 1)	1ΜΩ	2ΜΩ	2ΜΩ	2ΜΩ
Input Voltage Range Diff. or CM, max safe Common Mode Rejection Ratio	$\pm V_S, V_S \leq 15V$ 90dB min 80dB min	Differential, max safe Common Mode, max safe Common Mode Rejection T _{min/max}	±30V ±15V 80dB min	* * 90dB min	* * 90dB min	:
Power Supply Rated Performance Operating Quiescent Current	±15V ±18V 3mA max	Power Supply Rated Performance Operating Current, Quiescent	±15V ±(5 to 18)V 3.3mA max	* ±(5 to 22)V 2.8mA max	* ±(5 to 22)V 2.8mA max	* ±(5 to 22)V 2.8mA max
Temperature Range Operating, Rated Performance Storage	0 to +70°C -65°C to +150°C	Temperature Range Operating, Rated Performance Storage	0 to +70°C -65°C to +150°C	:	:	-55°C to +125°C
Price (1-24) (25-99) (100-999)	\$6.00 \$4.80 \$4.50	Price (1-24) (25-99) (100-999)	\$1.85 \$1.50 \$1.25	\$3.40 \$2.70 \$2.25	\$9.00 \$7.20 \$6.00	\$4.95 \$4.00 \$3.30

Note 1: For supply voltages less than $\pm 15V$, the absolute maximum input voltage is equal to the supply voltage. *Specifications same as AD741J.

CHOPPERLESS LOW DRIFT OPERATIONAL AMPLIFIER

GENERAL DESCRIPTION

The Analog Devices AD508 is the highest accuracy IC operational amplifier presently available. Its combination of low drift $(0.5\mu V/^{\circ}C max)$, low offset current (1.0nA max), and long term stability (10 μ V/month max) make it the choice for all applications requiring the utmost in precise performance from an IC op amp. Guaranteed parameters also include gain greater than 10⁶, PSRR less than 10 μ V/V, CMRR above 110dB, and offset voltage below 0.5mV – nullable to zero. In addition, the AD508's superbeta input transistor quad results in maximum offset and bias currents of 1nA and 10nA, while permitting the input stage to operate at sufficiently high current levels to provide a unity gain slew rate of 0.12V/ μ sec and small signal bandwidth of 300kHz.

The outstanding long term stability of the AD508 is attained by subjecting 100% of the devices to a 100 hour stabilization burn-in. Following this, the AD508L is closely monitored during an additional 500 hours of operation, during which



time it must meet interim and end-point limits in order to be qualified to its 10μ V/month maximum drift performance. The AD508J, K and L are supplied in the TO-99 package for operation over the 0 to $+70^{\circ}$ C temperature range.

ELECTRICAL SPECIFICATIONS (Typical @ +25°C and ±15VDC, unless otherwise specified)

Parameter	AD508J	AD508K	AD508L
Open Loop Gain			
$V_{O} = \pm 10V, R_{L} \ge 2k\Omega$	$250,000 \min (4 \times 10^6 \text{ typ})$	$10^6 \min(8 \ge 10^6 \text{ typ})$	$10^6 \min(8 \ge 10^6 \text{ typ})$
(a) $T_A = 0^{\circ}C$ to $+70^{\circ}C$	125,000 min (10 ⁶ typ)	500,000 min (10 ⁶ typ)	500,000 min (10 ⁶ typ)
Output Characteristics			
Voltage, $R_L \ge 2k\Omega$, $T_A = 0^{\circ}C$ to $+70^{\circ}C$	±10V min (±13V typ)	•	•
Output Current	10mA min	•	•
Frequency Response			
Unity Gain, Small Signal, C _C = 390pF	300kHz	*	•
Full Power Response, $C_C = 390 pF$	1.5kHz	*	•
Slew Rate, Unity Gain, C _C = 390pF	0.12V/µsec	*	*
Input Offset Voltage			
Initial Offset, $R_S \le 100\Omega$	±2.5mV max (±1.0mV typ)	±0.5mV max (±0.2mV typ)	±0.5mV max (±0.2mV typ)
vs. Temperature,	0	0	0
$T_A = 0$ C to +70 C, V_{OS} nulled	$\pm 3.0\mu V/C max (\pm 0.5\mu V/C typ)$	$\pm 0.5 \mu V/C \max (\pm 0.25 \mu V/C typ)$	$\pm 1.0\mu V/C \max (\pm 0.3\mu V/C typ)$
$T_A = 0^{\circ}C$ to +70°C, V_{OS} unnulled†	$\pm 10\mu V/^{\circ}C \max(\pm 1.5\mu V/^{\circ}C typ)$	$\pm 2.5 \mu V/^{\circ} C \max (\pm 1.0 \mu V/^{\circ} C typ)$	$\pm 2.5\mu V/^{\circ}C max (\pm 1.0\mu V/^{\circ}C typ)$
vs. Supply	$\pm 25 \mu V/V max$	$\pm 10 \mu V/V max$	$\pm 10 \mu V/V max$
(a) $T_A = 0^{\circ}C$ to $+70^{\circ}C$	$\pm 40 \mu V/V$	$\pm 15 \mu V/V max$	$\pm 15 \mu V/V max$
vs. Time	±15µV/mo	$\pm 10 \mu V/mo$	$\pm 10 \mu V/mo max$
Input Offset Current			
Initial	±5.0nA max (±2.5nA typ)	±1.0nA max (±0.5nA typ)	± 1.0 nA max (± 0.5 nA typ)
vs. Temp, $T_A = 0^\circ C$ to $+70^\circ C$	±14pA/°C	±4pA/°C	±4pA/°C
Input Bias Current			
Initial	25nA max (10nA typ)	10nA max (6nA typ)	10nA max (6nA typ)
vs. Temp, $T_A = 0^{\circ}C$ to $+70^{\circ}C$	±100pA/°C	±40pA/°C	±40pA/°C
Input Noise			
Voltage, 0.01 to 10Hz	1.0µV (p-p)	•	*
100Hz	$12 nV / \sqrt{Hz(rms)}$	•	*
1kHz	$10 nV / \sqrt{Hz(rms)}$	•	*
Current, 100Hz	$0.3 \text{pA}/\sqrt{\text{Hz}(\text{rms})}$	•	*
1kHz	$0.2 pA/\sqrt{Hz(rms)}$	*	*
Input Voltage Range			
Differential or Common Mode, Max Safe	±V _S	•	•
Common Mode Rejection, $V_{in} = \pm 10V$	94dB min (120dB typ)	110dB min (120dB typ)	110dB min (120dB typ)
Power Supply			
Current, Quiescent	±4.0mA max (±1.5mA typ)	±3.0mA max (±1.5mA typ)	±3.0mA max (±1.5mA typ)
Temperature Range			
Operating, Rated Performance	0° C to $+70^{\circ}$ C	•	
Storage	-65° C to $+150^{\circ}$ C		•
Price (1-24)	\$21.20	\$29.80	\$38.00
(25-99)	\$16.80	\$24.00	\$34.00
(100-999)	\$14.00	\$20.00	\$30.00

*Specification same as for AD508J.

†This parameter is not 100% tested; typically, 90% of the units meet this limit.

INSTRUMENTATION AMPLIFIER AD520

GENERAL DESCRIPTION

The Analog Devices' AD520 is the first instrumentation amplifier to be manufactured in integrated circuit form. It is a closed loop gain block with differential inputs and an accurately predictable input-to-output gain relationship. The AD520's performance is unlike that of conventional IC operational amplifiers because of an internal feedback design which permits gain adjustment from 1 to 1000 by varying the value of a single resistor. Further, high input impedance is achieved at both inputs and both input impedance and CMRR remain high at all gain settings.

The AD520 performs like a modular instrumentation amplifier. Because of its monolithic construction, however, its cost is significantly below that of modules, and becomes even lower with larger quantity requirements. The AD520 features low bias and offset currents, high gain linea-ity, excellent frequency response, and is short circuit protect ed and offset voltage nullable. Thus it is ideally suited for all general purpose, high accuracy amplifier requirements. Its small size, low cost, and complete-on-a-chip ease of application offer the circuit designer an attractive alternative to both modular instrumentation amplifier packages, and user-wired collections of IC op amps and high-precision external components. The AD520 finds excellent application in the amplification of low level signals from bridge circuits, thermocouples, strain gauges, and other transducers. Other applications include chart recorders, line reviewers, and in medical electronics. For increased versatility, the amplifier has a remote sense terminal for current-

SPECIFICATIONS (Typical at $V_S = \pm 15V$ and $T_A = \pm 25^{\circ}C$ unless otherwise noted)

Parameter	AD520J	AD520K	AD520S
Gain			
Range	1 to 1000	•	*
Equation	$G = (10^5 / R_{rain}) V / V$		•
Error from Equation Value	adjustable to zero	*	*
Non-Linearity (% of FS max)	±0.05% (±0.02% typ)	*	*
Output Characteristics			
Rated Output – Voltage (min)	±10V	*	*
Current (min)	±5mA	*	*
Impedance at G = 100, dc to 100Hz	2Ω	*	*
Frequency Response Small Signal Bandwidth (-3dB)			
G = 1	200kHz	*	*
G = 10	175kHz	*	•
G = 100	125kHz	*	*
G = 1000	25kHz	*	*
Full Power Response (min)	50kHz (75kHz typ)	*	*
Slew Rate (all gain settings) (min)	2.5V/µsec (4.0V/µsec typ)	*	*
Offset Voltage Initial Offset Voltage (Note 1) Input Offset at G = 1000 (RTI) (Note 2)	adjustable to zero	•	
vs Temperature, 0 to $+70^{\circ}$ C (max) vs Temperature, -55° C to $+125^{\circ}$ C (max)	$\pm 10 \mu V/^{\circ} C \ (\pm 5 \mu V/^{\circ} C \ typ)$	$\pm 5\mu V/^{\circ} C (\pm 2\mu V/^{\circ} C \text{ typ})$	$\pm 5\mu V/^{\circ} C (\pm 2\mu V/^{\circ} C typ)$
vs Supply (RTI) Input Offset at G = 1 (RTI) (Note 2)	$\pm 50 \mu V/V$	*	*
vs Temperature, 0 to $+70^{\circ}$ C (max) vs Temperature, -55° C to $+125^{\circ}$ C (max)	$\pm 1.0 \mathrm{mV/}^{\circ}\mathrm{C} (\pm 0.5 \mathrm{mV/}^{\circ}\mathrm{C} \mathrm{typ})$	$\pm 0.5 \text{mV}/^{\circ} \text{C} (\pm 0.25 \text{mV}/^{\circ} \text{C typ})$	±0.5mV/°C (±0.25mV/°C typ
vs Supply (RTI)	±400µV/V	*	*
Bias Current (either input) at +25°C (max)	±80nA (±40nA typ)	±40nA (±20nA typ)	**
vs Temperature, 0 to +70°C vs Temperature, -55°C to +125°C	±0.5nA/°C	±0.2nA/ C	$\pm 0.5 \mathrm{nA/}^{\circ}\mathrm{C}$
Offset Current			
at $+25^{\circ}C$ (max)	±40nA (±10nA typ)	±20nA (±10nA typ)	**
Input Impedance			
Differential	$2 \times 10^9 \Omega$	*	*
Common Mode	$2 \times 10^9 \Omega$	*	*
Noise			
dc to 10Hz (p-p), G = 1000 (RTI)	$5\mu V$	*	*
10Hz to 200 kHz (rms), G = 1 (RTI)	1mV	*	*
1Hz to 5kHz (rms), G = 1000 (RTI)	$2\mu V$	*	*



controlled load applications. A separate output reference terminal is also provided so that the output can be biased independently of the gain setting.

Both the AD520J and AD520K are supplied in a 14-lead hermetically-sealed dual-in-line package, and are specified for operation from 0 to $+70^{\circ}$ C. The AD520S, in the same package, is specified for -55° C to $+125^{\circ}$ C operation.

SPECIFICATIONS (continued)

Parameter	AD520J	AD520K	AD520S
Input Voltage Pange			*
Differential may safe	+Vo		
Differential max linear	- VS +10V		
Common Mode, max safe	-10 V +Vc	*	*
Common Mode, max sare	±10V	*	*
Common Mode Rejection Ratio			
dc to 100Hz, Rs imbalance = $1k\Omega$			
G = 1 (min)	65dB (80dB typ)	70dB (80dB typ)	**
G = 10 (min)	75dB (90dB typ)	86dB (100dB typ)	**
G = 100 (min)	90dB (100dB typ)	100dB (110dB typ)	**
G = 1000 (min)	95dB (106dB typ)	106dB (110dB typ)	**
G = 1000, f = 1.0 kHz	86dB	*	*
Power Supply Requirements			
Rated Supply Voltage (Note 3)	±15VDC	•	*
Voltage, Operating	±(5 to 18)VDC	•	*
Current, Quiescent (max)	±6.0mA (±4.0mA typ)	•	•
Reference Terminal Characteristics			<i>2</i>
R _{in}	$5 \times 10^7 \Omega$	*	*
Output Offset Range	±10V	•	•
Gain to Output	±1	*	•
Bias Current	500nA	•	•
Temperature Range			
Rated Performance	$0 \text{ to } +70^{\circ}\text{C}$	•	-55° C to $+125^{\circ}$ C
Operating	-25° C to $+85^{\circ}$ C.	*	-55° C to $+125^{\circ}$ C
Storage	-65° C to $+150^{\circ}$ C	*	•
Price			
1-24	\$18.00	\$24.00	\$33.00
25-99	\$14.40	\$19.20	\$26.50
100-999	\$12.00	\$16.00	\$22.00

NOTES:

1. Trim terminal must be connected.

2. Maximum drift specifications are guaranteed using a 50ppm T.C. trim potentiometer for offset nulling at each gain setting per the recommended nulling procedure.

3. Supply voltage must always be present before applying an input signal.

*Specifications same as AD520J.

**Specifications same as AD520K.

HIGH SPEED OPERATIONAL AMPLIFIERS AD505

The AD505J, AD505K and AD505S are monolithic operational amplifiers that are specifically designed for applications requiring high slew rate and fast settling time to high accuracy. The AD505 achieves a minimum slew rate of $120V/\mu$ sec, provides an adjustable unity gain bandwidth product of 4MHz to 10MHz, and settles to 0.1% in 800nsec. In addition to its superior dynamic characteristics, the AD505 maintains high gain, maximum offset voltage drift of $15\mu V/^{\circ}C$, maximum bias currents of 25nA and high output swing.

The circuit has a stable 6dB/octave rolloff for closed loop operation. It is also capable of being externally adjusted for up to 35dB of additional closed loop gain at high frequencies, without causing the small signal or large signal bandwidth to decrease, and without increasing settling times.

The AD505 is designed for high speed inverting applications by using a feed-forward technique. It can drive capacitive loads in excess of 1000pF and is short circuit protected. All the circuits are supplied in the TO-100 package. The AD505J and AD505K are specified for 0° C to $+70^{\circ}$ C temperature range operation; the AD505S for operation. from -55° C to $+100^{\circ}$ C.



ELECTRICAL CHARACTERISTICS ($V_S = \pm T_A = +25^{\circ}C$)

Parameter	AD505J	AD505K	AD505S
OPEN LOOP GAIN			
$R_{\rm L} = 2k\Omega, V_{\rm O} = \pm 10V$	100,000 min (500,000 typ)	200.000 min (500.000 typ)	**
Over Temp Range (Tmin to Tmax)	75.000 min	150,000 min	100 000 min
OUTDUT CHADACTEDICTICS		100,000 11111	100,000 mm
Velses @ P. 210			
Voltage $@$ $R_L = 2KS2$	(1001 - 1100 - 1)		
Over Temp Range (T _{min} to T _{max})	$\pm 10V \min(\pm 12V \text{ typ})$		•
Current (a) $V_0 = \pm 10V$	±10mA		•
Short Circuit Current	25mA	•	*
FREQUENCY RESPONSE			
Unity Gain, Small Signal	4 - 10MHz (adjustable)	•	•
Full Power Response	2.0MHz min (2.5MHz typ)	•	•
Slew Rate	120V/µsec min (150V/µsec typ)	•	•
Settling Time			
to 0.1%	800nsec	•	•
to 0.01%	2.0µsec	•	•
INPUT OFFSET VOLTAGE			
Initial $R_c \leq 10k\Omega$	5 0mV max (1 0mV tun)	25mV max (1 0mV mm)	**
Augus Temp $(T + to T)$	$15 \mu V \rho^{\circ} C$	2.5 mV max (1.0 mV typ)	20
Avg vs remp (1min to 1max)	$15\mu V/C$	$15\mu v/C \max(8\mu v/C typ)$	$20\mu v / C \max(10\mu v / C typ)$
vs supply (1 _{min} to 1 _{max})	$150\mu V/V \max (80\mu V/V typ)$		•
INPUT BIAS CURRENT			
Initial	75nA max (15nA typ)	25nA max (15nA typ)	**
Over Temp Range (T _{min} to T _{max})	100nA max	40nA max	80nA max
Avg vs Temp (Tmin to Tmax)	0.1 n A/°C	•	•
INPUT IMPEDANCE			
DC	2ΜΩ	• '	•
Above 10Hz	20kΩ	•	*
INPUT NOISE			
Voltage 0.01 to 10Hz(p-p)	2.5 uV		
0.01 to $1.0MHz(rms)$	1000		
Current 0.01 to 1.0 Hr/(n-n)	0.1p.4		
	0.1111		
POWER SUPPLY			
Rated Performance	±15V		•
Operating, Derated Performance	±(5 to 20)V		
Current, Quiescent	8.0mA max (6.0mA typ)	*	*
TEMPERATURE RANGE			
Rated Performance (Tmin to Tmax)	$0^{\circ}C$ to $+70^{\circ}C$	•	-55° C to $+100^{\circ}$ C (Note 1)
Operating	-25° C to $+85^{\circ}$ C	•	-55° C to $+100^{\circ}$ C (Note 1)
Storage	-65° C to $+150^{\circ}$ C	•	*
PRICE			
(1-24)	\$15.00	\$18.00	\$21.00
(25-99)	\$12.00	\$14.40	\$16.90
(100-999)	\$12.00	\$12.00	\$14.00
(100-999)	\$10.00	\$12.00	\$14.00

*Specifications same as AD505J.

**Specifications same as AD505K.

WIDEBAND, FAST SLEWING GENERAL PURPOSE OP AMPS AD507

GENERAL DESCRIPTION

The AD507J, AD507K, and AD507S are low cost high performince monolithic operational amplifiers that combine slew rates of $35V/\mu$ sec and 100MHz gain bandwidth with bias and offset currents below 10nA, and gain of 150,000 V/V. They are intended for applications where performance uperior to that of the popular AD741 or AD101A series s required, and are especially well suited for use in fast high impedance comparators, integrators, wideband amplifiers, and in sample-and-hold circuits. The AD507 is stable it closed loop gains above ten due to its internal 6dB per octave rolloff. External compensation provides stability to unity gain, and permits flexibility for special frequency applications. The circuit is short circuit protected and offset voltage nullable. Both the AD507J and AD507K

PIN CONFIGURATION **Top View** .1µF FREQUENCY 5 OFFSET OFFSET NUL \$ 2KΩ (7) V+ INVERTING INPUT OUTPUT ACL 1µF 1 20pF (CERAMIC DISK) NON-INVERTING OFFSET NULL OpF ≥ 10 INPUT **TO-99** *NOT REQUIRED FOR CL = 50pF **BEST INPUT SIGNAL GROUND AVAILABLE

are supplied in the TO-99 package for operation over the 0 to $+70^{\circ}$ C temperature range. The AD507S is specified for operation from -55°C to +125°C.

SPECIFICATIONS (Typical @ +25°C and ±15VDC unless otherwise noted)

Model	AD507J	AD507K	AD507S
Open Loop Gain			
$R_{\rm L} = 2k\Omega, C_{\rm L} = 50 pF$	80,000 min (150,000 typ)	100,000 min (150,000 typ)	100,000 min (150,000 typ)
Over Temp Range (Tmin to Tmax)	70,000 min	85,000 min	70,000 min
Output Characteristics			
Voltage @ $R_1 = 2k\Omega$, $C_1 = 50pF$			
Over Temp Range (Tmin to Tmax)	$\pm 10V \min(\pm 12V typ)$	*	
Current @ $V_{o} = \pm 10V$	± 10 mA min (± 20 mA typ)		± 15 mA min (± 22 mA typ)
Short Circuit Current	25mA	*	*
Frequency Response	201111		
Unity Gain Small Signal			
(a) A = 1 (open loop)	35MHz	*	
(a) A = 100 (closed loop)	100MHz		
Full Power Response	320kHz min (600kHz typ)	400kHz min (600 kHz typ)	400kHz min (600kHz typ)
Slew Pate	$\pm 20 \text{V}/\mu\text{sec} \min(\pm 25 \text{V}/\mu\text{sec} \tan)$	$\pm 25 V/\mu sec min (\pm 25 V/\mu sec tun)$	+20V/usec (+35V/usec typ)
Siew Rate	$=20\sqrt{\mu}\text{sec} \min(=35\sqrt{\mu}\text{sec}(yp))$	=25 v /µsec mm (=55 v /µsec typ)	=20 v / µsec (= 55 v / µsec typ
Input Offset Valuere	900118		
Input Offset Voltage	5.0-V	20 mV may $(15 mV$ my)	10-W
	5.0mv max (5.0mv typ)	5.0 m x max (1.5 m v typ)	4.0 mV max (0.5 mV typ)
Avg vs Temp, (T _{min} to T _{max})	15µV/ C	$15\mu V/C \max(8\mu V/C typ)$	$20\mu V/C \max(8\mu V/C typ)$
vs Supply, (T _{min} to T _{max})	$200\mu V/V max$	$100\mu V/V \text{ max}$	$100\mu V/V \text{ max}$
Input Bias Current			
Initial	25nA max	15nA max	15nA max
Over Temp Range (T_{min} to T_{max})	40nA max	25nA max	35nA max
Input Offset Current			
Initial	25nA max	15nA max	15nA max
Over Temp Range (T _{min} to T _{max})	40nA max	25nA max	35nA max
Avg vs Temp (T_{min} to T_{max})	0.5nA/°C	0.2nA/°C	0.2nA/°C
Input Impedance			
Differential	$40M\Omega \min (300M\Omega typ)$	*	
Common Mode	1000ΜΩ	*	
Input Voltage Noise			
f = 10Hz	$100 \text{nV} / \sqrt{\text{Hz}}$	•	
f = 100Hz	$30 \text{nV} / \sqrt{\text{Hz}}$	•	
f = 100 kHz	$12 n V / \sqrt{Hz}$	*	
Input Voltage Range			
Differential, Max Safe	±12.0V	•	•
Common Mode Voltage Range			
Tmin to Tmax	±11.0V		
Common Mode Rejection @ ±15V			
Tmin to Tman	74dB min (100dB typ)	80dB min (100dB typ)	80dB min (100dB tvp)
Power Supply			
Rated Performance	±15V	•	
Operating	+(5 to 20)V	•	
Current Quiescent	4.0mA max $(3.0$ mA typ)		
Temperature Range	4.0mm max (5.0mm typ)		the second s
Rated Performance	$0 to \pm 70^{\circ}C$		$-55^{\circ}C$ to $+125^{\circ}C$
Storage	-65°C to +150°C		*
Drice	-05 C (0 +150 C		
(1-24)	\$9.50	\$15.00	\$22.50
(1-24)	\$9.50	\$12.00	\$18.00
(100,000)	\$6.10	\$10.00	\$15.00
(100-999)	JU.73	\$10.00	\$13.00

HIGH SPEED, FAST SETTLING OPERATIONAL AMPLIFIER AD509 PIN CONFIGURA

GENERAL DESCRIPTION

The AD509J, AD509K and AD509S are fast differential input operational amplifiers whose combination of low cost and excellent dynamic characteristics make them well suited for 12bit D/A and A/D circuits, sample/hold circuits, multiplexers, and other applications requiring fast settling time to low error levels. Of particular significance are the maximum settling time specifications of 2.0μ sec to 0.01% and 500nsec to 0.1%of the AD509K and AD509S.

Other excellent specifications include unity gain small signal bandwidth of 20MHz, slew rate of $120V/\mu$ sec, and ± 10 mA minimum output current at $\pm 10V$. The AD509 is stable for



all values of closed loop gain greater than 3 without external compensation, and can be stabilized with a single external capacitor for any value of closed-loop gain. The AD509J and AD509K are specified for operation from 0 to $+70^{\circ}$ C; the AD509S from -55° C to $+125^{\circ}$ C. All models are supplied in the TO-99 metal can package.

SPECIFICATION SUMMARY (Typical $@+25^{\circ}$ C and ± 15 VDC, unless otherwise specified)

Model	AD509J	AD509K	AD509S	
Open Loop Gain				
$R_{I} = 2k\Omega$	7,500 min (15,000 typ)	10,000 min (15,000 typ)	••	
(a) $T_A = \min to \max t$	5,000 min	7,500 min	••	
Output Characteristics				
Voltage @ $R_1 = 2k\Omega$. T _A = min to max	±10V min (±12V typ)			
Current @ $V_0 = \pm 10V$	± 10 mA min (± 20 mA typ)	*		
Short Circuit Current	25mA			
Frequency Perponse				
Unity Cain Small Signal	20MHz		14	
Full Power Response $V_0 = \pm 10V$	120kHz min $(1.6$ MHz typ)	150kHz min (2MHz typ)		
Slew Rate R ₁ = $2k\Omega$ V ₀ = $\pm 10V$ C ₁ = $50nF$	$80V/usec \min(120V/usec typ)$	100V/usec min (120V/usec typ)		
Settling Time	80 v /μsee min (120 v /μsee typ)	100 v/µsee mm (120 v/µsee (yp)		
to 0.1%	200nsec	500nsec max (200nsec typ)	**	
to 0.01%	1µsec	2μ sec max (1μ sec typ)	• *	
Input Offset Voltage				
Initial	10mV max (5mV typ)	8mV max (4mV typ)	1.4	
$T_A = \min to \max$	14mV max	11mV max	. *	
Avg vs Temperature, $T_A = \min to \max$	$20\mu V/^{\circ}C$	$30\mu V/^{\circ}C \max (20\mu V/^{\circ}C typ)$	ж.у.	
vs Supply, $T_A = \min to \max$	$200\mu V/V max$	$100\mu V/V max$	3.4	
Input Bias Current				
Initial	250nA max (125nA typ)	200nA max (100nA typ)	. 5 %	
$T_A = \min to \max$	500nA max	400nA max	* *	
Input Offset Current				
Initial	50nA max (20nA typ)	25nA max (10nA typ)	* *	
$T_{A} = \min to \max$	100nA max	50nA max	••	
Input Impedance				
Differential	$40M\Omega \min (300M\Omega typ)$	$50M\Omega \min(300M\Omega typ)$	**	
Input Voltage Range	(1			
Differential max safe	±15V			
Common Mode Voltage Range	-101			
$T_{\rm A} = \min_{i=1}^{1} t_{\rm A} \max_{i=1}^{1} t_{\rm A}$	+10V		•	
Common Mode Rejection @ +5V	-101			
$T_{A} = \min to \max$	74dB min (90dB typ)	80dB min (90dB typ)	**	
Power Supply	· · · · · · · · · · · · · · · · · · ·			
Rated Performance	±15V		•	
Operating	+(5 to 20)V		•	
Current Quiescent	6mA max (4mA typ)		*	
Tomporatura Pange				
Pated Performance	$0 \pm 70^{\circ}C$		$-55^{\circ}C$ to $+125^{\circ}C$	
Storage	$-65^{\circ}C$ to $+150^{\circ}C$		*	
Deise	05 0 10 1150 0			
(1.24)	\$11 50	\$19.75	\$26.00	
(1-24)	\$11.50	\$10./J	\$20.00	
(25-99)	\$10.20	\$13.00	\$22.00	
(100-999)	38.30	\$12.50	\$19.00	

**Specifications same as AD509K.

HIGH SPEED, LOW COST, OPERATIONAL AMPLIFIER AD518

new product: AD518

NERAL DESCRIPTION

: AD518J, AD518K, and AD518S are precision high speed nolithic operational amplifiers designed for applications ere high slew rate and wide bandwidth are required but low t and ease of use are essential. The devices are internally npensated for unity gain applications with a 60° phase rgin to insure stability, a minimum slew rate of 50V/ μ sec, a typical bandwidth of 12MHz. In addition, in inverting lications, external feedforward compensation may be led to increase the slew rate to over 100V/ μ sec, and nearly ible the bandwidth. If desired, settling time to 0.1% can be uced to under 1 μ sec with a single external capacitor.

AD518's dc performance is consistent with its precision namic characteristics. The devices feature offset voltages be- 2 2mV, maximum offset drifts of 10μ V/°C, and offset curts below 50nA max.



The high slew rate, fast settling time, ease of use, and low cost of the AD518 make it ideal for use with the D/A and A/D converters, as well as active filters, sample and hold circuits, and as a general purpose amplifier. The AD518 is supplied in the TO-99 package. The AD518J and AD518K are specified for operation over the 0 to $+70^{\circ}$ C temperature range; the AD518S for operation from -55° C to $+125^{\circ}$ C.

Parameter	AD518J	AD518K	AD518S
pen Loop Gain			
$R_{\rm I} \ge 2k, V_{\rm O} = \pm 10V$	25,000 min (200,000 typ)	50,000 min (200,000 typ)	50,000 min (200,000 typ)
(a) $T_A = \min to \max$	20,000 min	25,000 min	25,000 min
utput Characteristics			
Voltage @ $R_L = 2k\Omega$, T = min to max	±12V min (±13V typ)	*	*
Current (a) $V_O = \pm 10V$	±10mA min	*	*
Short Circuit Current	25mA	*	*
requency Response			
Unity Gain, Small Signal	12MHz typ	10MHz min (12MHz typ)	10MHz min (12MHz typ)
Slew Rate, Unity Gain	$50V/\mu sec min (70V/\mu sec typ)$	*	*
Settling Time to 0.1%	· · · · / · · · · · · · · · · · · · ·		
(Single Capacitor Compensation)	800nsec	*	*
Phase Margin Uncompensated at Unity			
Gain Crossover Frequency	+60°	*	
aput Offset Voltage			
Initial $B_c \leq 10 k\Omega$	10mV max (4mV typ)	4mV max (2mV typ)	4mV max (2mV typ)
$T_{\star} = \min_{i} to \max_{i}$	15mV max	6mV max	6mV max
Avg vs Temp $T \rightarrow to T$	$10\mu V/^{\circ}C$	$10\mu V/^{\circ} C \max (5\mu V/^{\circ} C \tan)$	$10\mu V/^{\circ} C \max (5\mu V/^{\circ} C \tan \theta)$
Avg vs Supply T to T	65dB min (80dB tyn)	70dB min (80dB typ)	70dB min (80dB typ)
Price Current	oyab min (oodb typ)	/oub min (ooub typ)	/oub min (boub typ)
Initial	500nA max (120nA turn)	200nA max (120nA tun)	200n A max (120n A tun)
T = min to may	750p (max (1201A typ)	2001A max (1201A typ)	2001A max (1201A typ)
I _A - IIII to IIIAX	750HA HIAX	400IIA IIIax	400IIA IIIax
nput Offset Current	200- 1 (20- 1)		50 A
Initial	200nA max (30nA typ)	SUNA max (on A typ)	SonA max (onA typ)
$I_A = \min to \max$	300nA max	100nA max	100nA max
nput Impedance			
Differential	0.5MS2 min (3MS2 typ)	*	*
nput Voltage Range			
Differential, max safe	$\pm V_{S}, V_{S} \leq 15V$	*	*
Common Voltage Rejection Ratio	70dB min (100dB typ)	80dB min (100dB typ)	80dB min (100dB typ)
ower Supply			
Rated Performance	±15V	*	*
Operating	±(5 to 20)V	*	*
Current, Quiescent	10mA max (5mA typ)	7mA max (5mA typ)	7mA max (5mA typ)
emperature Range			
Rated Performance	$0 \text{ to } +70^{\circ}\text{C}$	*	-55° C to $+125^{\circ}$ C
Storage	-65° C to $+150^{\circ}$ C	*	*
rice			
(1-24)	\$3.00	\$7.20	\$12.00
(25-99)	\$2.40	\$6.00	\$9.60
(100-999)	\$1.95	\$4.95	\$7.95

LECTRICAL SPECIFICATIONS (Typical @ +25°C and ±15VDC, unless otherwise noted.)

LOW I_B, HIGH ACCURACY BIPOLAR OP AMPS ADI08, ADI08A



GENERAL DESCRIPTION

The AD108 and AD108A series offer a level of input isolation ranging between that of general purpose op amps, such as the AD741 or AD101A families, and the high performance FET op amps, such as the AD506 or AD516 series. The use of superbeta transistors in the input stage, combined with extremely precise processing results in guaranteed input currents nearly a thousand times lower than those of the AD741. The AD108, AD208, and AD308 feature excellent input characteristics, with typical I_b of less than 1.0nA, I_{OS} of less than 100pA, and V_{OS} of less than 1.0mV. In addition, the devices are tightly specified for temperature drift operation, with a maximum voltage drift of $15\mu V/^{\circ}C$ for the AD108 and AD208, and $30\mu V/^{\circ}C$ for the AD308. The "A" series offer several improved specifications, including maximum V_{OS} of 0.5mV, minimum gain of 80,000, maximum voltage drift of $5.0\mu V/^{\circ}$ C, and minimum CMRR of 96dB. The capability of both series to operate with supply voltages as low as $\pm 2V$, and their extremely low power consumption, make them ideal for battery-powered applications. Frequency compensation is accomplished externally, in most cases with a single capacitor.

All the amplifiers are supplied in the TO-99 metal can package; the AD108 and AD108A are specified for operation from -55° C to $+125^{\circ}$ C, the AD208 and AD208A from -25° C to $+85^{\circ}$ C, and the AD308 and AD308A from 0 to $+70^{\circ}$ C.

SPECIFICATION SUMMARY (Typical @ +25°C and ±15VDC power supply unless otherwise noted.)

Model	AD108	AD208	AD308	AD108A	AD208A	AD308A
Open Loop Gain						
DC Rated, Load, V/V Min	50,000	50,000	25,000	50,000	50,000	25,000
Rated Output, Min, $R_{I} \ge 10 k\Omega$	±13V	•	•	•	•	•
Frequency Response						
Unity Gain, Small Signal (Variable						
With External Compensation)	0.3 to 3.0MHz		•	•	•	•
Slewing Rate (Variable as Above)	0.3 to 1.3V/µsec	•	•	•	•	•
Input Offset Voltage						
Initial, +25°C, min	2.0mV	2.0mV	7.5mV	0.5mV	0.5mV	0.5mV
Avg. vs. Temp, max	$15\mu V/^{\circ}C$	$15\mu V/^{\circ}C$	$30\mu V/^{\circ}C$	$5.0\mu V/^{\circ}C$	$5.0\mu V/^{\circ}C$	5.0µV/°C
Supply, min, TA min to max	80dB	80dB	80dB	96dB	96dB	96dB
Input Bias Current						
Initial, +25°C, max	2.0nA	2.0nA	7.0nA	2.0nA	2.0nA	7.0nA
Input Difference Current						
Initial, +25°C, max	0.2nA	0.2nA	1.0nA	0.2nA	0.2nA	1.0nA
Avg. vs. Temp, max	2.5pA/°C	2.5pA/°C	10pA/°C	2.5pA/°C	2.5pA/°C	10pA/°C
Input Voltage Range						
Common Mode Voltage, min	±14V	•	•	*	•	•
Common Mode Rejection, min	85dB	85dB	80dB	96dB	96dB	96dB
Differential Input Current (Note 1)	±10mA	•	•	•	•	*
Power Supply Range (VDC)	±(2 to 20)V	±(2 to 20)V	±(2 to 15)V	±(2 to 20)V	±(2 to 20)V	±(2 to 15)V
Rated Specification (VDC)	±(5 to 20)V	±(5 to 20)V	±(5 to 15)V	±(5 to 20)V	±(5 to 20)V	±(5 to 15)V
Quiescent Current, max	0.6mA	0.6mA	0.3mA typ	0.6mA	0.6mA	0.3mA typ
Temperature Range						
Operating, Rated Specification	-55°C to +125°C	-25° C to $+85^{\circ}$ C	0 to $+70^{\circ}$ C	-55°C to +125°C	-25°C to +85°C	$0 \text{ to } +70^{\circ}\text{C}$
Storage	-65°C to +150°C	•	*	•	•	•
Price						
(1-24)	\$18.75	\$10.50	\$3.00	\$26.50	\$21.00	\$10.50
(25-99)	\$15.00	\$8.50	\$2.35	\$21.00	\$16.75	\$8.40
(100-999)	\$12.50	\$7.00	\$1.95	\$17.50	\$14.00	\$7.00

Note 1. Current must be limited to ±10mA. Inputs have shunt-diode protection *Specifications same as for AD108.

LOW INPUT CURRENT 709, 741 REPLACEMENTS AD801, AD502



GENERAL DESCRIPTION

The AD801 and AD502 are low input current replacements for the popular 709 and 741 operational amplifiers. Levels of I_b below 4nA and I_{OS} below 1nA are achieved by utilizing a Darlington input modification of the basic 709 and 741 designs, with no significant change in other operating parameters. Thus the user is afforded the opportunity of upgrading performance in his 709 and 741 sockets without resorting to a new amplifier design. The AD801 offers the 709's flexibility of external compensation; the AD502, like the 741, is internally compensated. Both devices are supplied in the TO-99 metal can package.

SPECIFICATION SUMMARY (Typical @ $T_A = +25^{\circ}C$ and $V_S = \pm 15V$ unless otherwise noted)

	AD801			AD502		
	А	В	S	J	К	L
Open Loop Gain			_			
$R_L \ge 2k\Omega, E_0 = \pm 10V, \min$	15,000	•		20,000	**	* *
Rated Output Voltage						
$R_L \ge 2k\Omega$, min	±10V	*	*	±10V	* *	* *
Frequency Response						
Unity Gain, Small Signal	500kHz (note 1)	*	*	1MHz	**	* *
Full Power Response	200kHz (note 2)	•	*	10kHz	* *	**
Slew Rate	$10V/\mu sec$ (note 2)	*	*	$0.5V/\mu sec$	**	* *
Input Offset Voltage						
(a) +25 °C max	±5mV	*	*	±6mV	±5mV	±5mV
Over Temp Range $(T_1 \text{ to } T_h)$, max	$\pm 7.4 \text{mV}$	±5.6mV	$\pm 7.0 \text{mV}$	$\pm 7.5 \text{mV}$	±6mV	±6mV
Avg. vs Temp (T_1 to +25 C to T_h), max	$\pm 40\mu V/C$	$\pm 10\mu V/C$	$\pm 20\mu V/C$	$\pm 40\mu V/C$	$\pm 20\mu V/C$	$\pm 10 \mu V/C$
vs Supply Voltage, max	$\pm 200 \mu V/V$	-		$\pm 150\mu V/V$	* *	**
Input Bias Current	1			25.4	-	
(a) +25 C, max	4nA	*	16.0.4	25nA	/nA	4nA
Input Difference Current	TTUA		TOUA	JUIA	1511A	IUNA
mput Difference Current	+2 4	+1 - 4	+2= 4	+12-4	+ 4 - 4	
Over Temp Pange (T. to T.) may	$\pm 2nA$	$\pm 1 nA$ $\pm 2 nA$	±2nA	$\pm 12nA$	$\pm 4nA$	$\pm 1 nA$
over remp Range (1] to 1h), max	±onA	±2nA	±5nA	-24nA	-8nA	±2nA
Input Impedance	25110			2510		
Differential, min	25M32			25MS2		
Common Mode	500M22			500M22		
Input Voltage Noise	100 11			100.11		
0.01 to TOHz, p-p	100μV			Τοομν	**	**
TOHZ to SKHZ, rms	δμν			6μν		* *
Input Voltage Range						-
Common Mode Voltage, Min	$\pm 8V$	*	*	±10V	* *	* *
Common Mode Rejection, Min	65dB	*	*	70dB	**	* *
Max Safe Differential Voltage	±10V	*	*	±VS	* *	* *
Power Supply						
Voltage, Rated Specification	±(15 to 16)V	*	*	±(15 to 16)V	* *	* *
Voltage, Derated Specification	±(5 to 18)V		*	±(5 to 18)V	* *	**
Current, Quiescent, max	±6mA	*	*	±2.8mA	* *	* *
Temperature Range						
Operating, Rated Specifications	$T_1 = -25^{\circ}C$,	$T_1 = -25^{\circ}C$,	$T_1 = -55^{\circ}C$,	$T_1 = 0$,	* *	**
	$T_h = +85^{\circ}C$	$T_h = +85^{\circ}C$	$T_{h} = +125^{\circ}C$	$T_h = +70^{\circ}C$	* *	* *
Operating, Derated Specifications	-55°C to +125°C	*	*	-55° C to $+125^{\circ}$ C	* *	* *
Storage	-65° C to $+150^{\circ}$ C	*	*	-65° C to $+150^{\circ}$ C	* *	* *
Mechanical						
Case Style - Pin Configuration	TO-99	*	*	TO-99	* *	* *
Price						
1-24	\$14.00	\$19.00	\$23.00	\$4.50	\$9.00	\$19.00
25-99	\$12.00	\$16.00	\$19.00	\$3.60	\$7.20	\$15.00
100-999	\$9.75	\$13.00	\$15.00	\$3.00	\$6.00	\$12.50

NOTES

1. $C_1 = 5000 \text{pF}, R_1 = 1.5 \text{k}\Omega, C_2 = 200 \text{pF} (A_{\text{CL}} = 1).$

2. $C_1 = 10 pF$, $R_1 = 0\Omega$, $C_2 = 3 pF$ ($A_{CL} = 1000$).

*Specifications same as for AD801A.

**Specifications same as for AD502J.

HIGH OUTPUT CURRENT OPERATIONAL AMPLIFIERS AD512

GENERAL DESCRIPTION

The AD512K and AD512S are monolithic operational amplifiers specifically designed for high output current capability. High efficiency output transistors, thermally balanced chip design and precise short circuit current control insure against gain degradation at high current levels and temperature extremes. The AD512K specifies a minimum gain of 20,000 swinging ± 12 volts into a 1k Ω load from 0 to +70°C; the AD512S specifies a minimum gain of 15,000 swinging ± 10 volts into a 1k Ω load from -55°C to +125°C. In addition, the devices offer excellent input characteristics and common mode and power supply rejection ratios, and are internally compensated. Both are available in the TO-99 package; the AD512K for 0 to +70°C temperature range operation, and the AD512S for operation from -55°C to +125°C.



*

4

ELECTRICAL SPI otherwise noted.)	CIFICATIONS (Typical @ +25°C and =	±15VDC, unless	
Model	AD512K	AD512S	
Open Loop Gain $V_{OS} = \pm 10V, R_L \ge$ (a) $T_A = \min to max$	1kΩ 50,000 min (200,000 typ) 25,000 min	:	
Output Characteristics Voltage @ RL ≥1kΩ Short Circuit Curren	2, $T_A = \min to \max \frac{\pm 10V \min (\pm 13V typ)}{25 \text{ mA}}$:	
Frequency Response Unity Gain, Small Si Full Power Response Slew Rate, Unity Ga	gnal 1MHz e 10kHz tin 0.5V/µsee	÷	
Input Offset Voltage Initial, $R_S \le 10 k\Omega$ (T_{min} to T_{max} Avg vs Temperature vs Supply, $T_A =$	Adjustable to Zero) $3mV max (1mV typ)$ $5mV max$ (Untrimmed) $20\mu V/^{\circ}C max$ min to max $100\mu V/V max (30\mu V/V ty)$	25μV/°C max p)	
Input Offset Current Initial T _{min} to T _{max} Input Bias Current Initial	50nA max (5nA typ) 100nA max 200nA max (40nA typ)	* 150nA max 200nA max (40nA typ)	
T _{min} to T _{max} Input Impedance	400nA max	600nA max	
Differential Input Voltage Range (N Differential, Max Sa Common Mode, Ma: Common Mode Reje	$\frac{1MS2}{fc}$ solution $\frac{\pm 30V}{t}$ solution $\frac{\pm 15V}{t}$		
$V_{IN} = \pm 12V$	80dB min (90dB typ)	*	
Power Supply Rated Performance Operating Current, Quiescent Temperature Range	±15V ±(5 to 18)V 3.3mA max (2.0mA typ)	±(5 to 22)V	
Operating, Rated Pe Storage	rformance $0 \text{ to } +70^{\circ}\text{C}$ -65 $^{\circ}\text{C} \text{ to } +150^{\circ}\text{C}$	-55"C to +125"C	
Price (1-24) (25-99) (100-999)	\$6.00 \$4.80 \$4.00	\$9.00 \$7.20 \$6.00	

Note 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage. *Same specifications as AD512K.

LOW COST, GENERAL PURPOSE OP AMPS AD74I, ADIOIA

GENERAL DESCRIPTION

The AD741 and AD101A amplifier series are Analog Devices' versions of the two most popular IC op amps. They are designed for general purpose use where medium performance is acceptable and economy is mandatory. Both offer full short circuit protection, external offset voltage nulling, high common mode range, and the absence of latch-up. The AD741 and AD741C emphasize simplicity of use, requiring no external compensation. The ADI01A, AD201A and AD301A provide somewhat higher DC accuracy and require external compensation, thus affording the user the opportunity to fit the amplifier's dynamic characteristics to its specific application. The AD741 is available in the TO-99 metal can package for operation from -55°C to +125°C; the AD741C is packaged in both the TO-99 and plastic mini-DIP DIL and operates from 0 to +70°C. The AD101A is specified in both the TO-99 and ceramic flat packages from -55°C to +125°C; the AD201A is available in the TO-99, mini-DIP and flat packages for -25°C to +85°C and 0 to +70°C operation; and the AD301A is packaged in the TO-99 and mini-DIP, and operates from $0 \text{ to } +70^{\circ} \text{C}.$



SPECIFICATIONS (Typical @ +25°C and ±15VDC power supply unless otherwise noted.)

Model	AD741	AD741C	AD101A	AD201A	AD301A
Open Loop Gain					
DC Rated Load, V/V Min	50,000	20,000	50,000	50,000	25,000
Rated Output, Min, $R_I \ge 2k\Omega$	±10V	*	*	*	*
Frequency Response					
Unity Gain, Small Signal	1.0MHz	*	1.0 to 8.0MHz	1.0 to 8.0MHz	1.0 to 8.0MHz
Slewing Rate	0.5V/µs	*	0.5 to 10V/µs	0.5 to 10V/µs	0.5 to 10V/µs
Input Offset Voltage					
Initial, +25°C (Adj. to Zero) Min	5.0mV	6.0mV	2.0mV	2.0mV	7.5mV
Avg vs Temperature, Max	-	-	$15\mu V/^{\circ}C$	$15\mu V/^{\circ}C$	30µV/°C
vs Supply Voltage	30µV/V	*	96dB	96dB	96dB
Input Bias Current					
Initial, +25°C, Max	500nA	*	75nA	75nA	250nA
Input Difference Current					
Initial, +25°C, Max	200nA	*	10nA	10nA	50nA
Avg vs Temperature, Max	_	-	$0.2nA/^{\circ}C$	$0.2 n A/^{\circ} C$	0.6nA/°C
Input Impedance					
Differential	2.0MΩ	*	4.0MΩ	4.0MΩ	2.0MΩ
Input Voltage Range					
Common Mode Voltage, Min	±12V	*	*	*	*
Common Mode Rejection, Min	70dB	*	80dB	80dB	70dB
Differential Voltage	±30V	*	*	*	*
Power Supply Range (VDC)	±(5 to 22)V	±(5 to 18)V	±(5 to 22)V	±(5 to 22)V	±(5 to 18)V
Rated Specification (VDC)	±15V		*	*	*
Quiescent Current, Max	2.8mA	*	3.0mA	3.0mA	3.0mA
Temperature Range					
Operating, Rated Specification.	-55°C to +125°C	0 to $+70^{\circ}$ C	-55° C to $+125^{\circ}$ C	-25° C to $+85^{\circ}$ C ¹	0 to $+70^{\circ}$ C
Package Outline	TO-99	TO-99 mini-DIP	TO-99 flat pack	TO-99 flat pack	TO-99 mini-DI
	10 //	10 //, 1111 211	ro ,, nut putt.	mini-DIP	10 77, 1111 01
Price ²					
(1-24)	\$3.00	\$1.50	\$4.50	\$4.10	\$1.50
(25-99)	\$2.40	\$1.20	\$3.60	\$3.30	\$1.20
(100-999)	\$2.00	\$1.00	\$3.00	\$2.75	\$1.00

¹0 to +70°C in mini-DIP package.

²TO-99 package, and mini-DIP package (where listed).

*Same specifications as AD741;

MULTIPLIER/DIVIDER COMPUTATION CIRCUITS AD530, AD531, AD532

GENERAL DESCRIPTION

Models AD530, AD531, and AD532 utilize the Gilbert linearized transconductance technique to perform the basic functions of multiplying, dividing, squaring and square rooting. In addition to being most useful operations in themselves, these functions are excellently applied in circuitry for modulation and demodulation, frequency discrimination, phase detection, automatic gain control, vector computation, function generation, and true RMS-to-DC conversion.

Each multiplier offers the user specific choices in the areas of performance, flexibility, ease of use, and cost, and should be carefully evaluated to ascertain which is best suited for the particular application. Certain performance features are common to all models, and are described here. The differences are covered in the individual product descriptions.

Since all the multipliers operate over four quadrants, there are no restrictions as to signal polarity. The guaranteed maximum error specifications include the contributions from all sources ... feedthrough, offset, scale factor, and nonlinearity ... in the four quadrants. Further, in addition to the transconductance element, the design of the three models incorporates a stable reference and output amplifier on the monolithic chip. The AD530 and AD532 are available in the hermetically-sealed TO-100 metal can and TO-116 ceramic DIL packages, the AD531 only in the DIL package, and are specified for operation over the 0 to $+70^{\circ}$ C and -55° C to $+125^{\circ}$ C temperature ranges.

AD530: V_x · V_y/10; 2%, 1%, 0.5% MAX ERRORS

The low-priced AD530 multiplies in four quadrants with a transfer function of XY/10, divides in two quadrants with a 10Z/X transfer function, and square roots in one quadrant with a transfer function of $-\sqrt{10Z}$. Due to its design completeness, which includes the output amplifier, frequency compensation, level shifting, and scaling on the chip, the AD530's complement of external components is confined to feedthrough, output zero and gain adjusting trim pots.

The AD530J, AD530K, and AD530L operate from 0 to +70°C and are specified for maximum full scale multiplying errors of $\pm 2\%, \pm 1\%$, and $\pm 0.5\%$, respectively, at ± 25 °C. The AD530S, designed for wide temperature range military and aerospace requirements, is guaranteed for a maximum multiplying error of $\pm 1\%$, at ± 25 °C, and is 100% temperature tested to insure less than $\pm 3\%$ error from -55°C to ± 125 °C. The high accuracy AD530L is also 100% tested to guarantee a maximum error of $\pm 1.5\%$ from 0 to ± 70 °C. These low maximum errors over temperature are indicative of the excellent temperature stability of the AD530; performance that is unmatched by any IC multipliers except those supplied by Analog Devices.

AD531: $V_x \cdot V_y/V_z$; 2%, 1%, 0.5% MAX ERRORS

The AD531 is the first monolithic multiplier/computation circuit to provide the true transfer function $V_x \cdot V_y/kIz$ without the need for an external level shifting op amp at the output. Significant flexibility of operation is achieved by means of the variable scale factor kIz, which can be set by an external resistor or varied dynamically by an externally derived reference

current to obtain the overall transfer function $V_x \cdot V_y/V_z$. This provision for the direct computation of three variables greatly simplifies the design of such complex circuits as the true RMS-to-DC converter, AGC, vector computation, and absolute value. Further, multipliers less flexible than the AD531 must put the multiplying element in the feedback of an op amp to obtain division, often with significant sacrifice in accuracy and bandwidth.

The unique features of the AD531 include a differential V_x input with 75dB of CMR, an internally derived stable reference for use in fixed scale applications, and a sense feedback terminal for simple load sensing or special applications. The circuit's complement of required external components is limited to feedthrough and output zero adjusting trim pots, and passive or active adjustment of the scaling current I_z .

The AD531J, AD531K, and AD531L operate from 0 to $+70^{\circ}$ C and have maximum multiplying errors of $\pm 2\%$, $\pm 1\%$, and $\pm 0.5\%$ of full scale respectively, at $+25^{\circ}$ C. The AD531L is also guaranteed to have less than $\pm 1.5\%$ error from 0 to $+70^{\circ}$ C. The AD531S is guaranteed for a maximum error of $\pm 1\%$ at $+25^{\circ}$ C, and is also 100% tested to guarantee a maximum error of $\pm 3\%$ from -55° C to $+125^{\circ}$ C.

AD532: $(V_{x_1} - V_{x_2}) (V_{y_1} - V_{y_2})/10$; 2%, 1%; INTERNALLY TRIMMED

The AD532 is the first totally self-contained monolithic multiplier/divider. Because it needs no external components for accuracy trimming or output level shifting, the AD532 provides design engineers who require analog multiplication $[(V_{x_1} - V_{x_2}) (V_{y_1} - V_{y_2})/10$ in four quadrants], division $[10Z/(X_1 - X_2)$ in two quadrants], square rooting $(\pm\sqrt{10Z}$ in one quadrant), and squaring, with the best in-board combination of low cost, small size, and simplicity of use. It can be inserted directly into the circuit board – much as an internally compensated IC op amp – thus saving the user the time and expense of providing external trimming resistors and of performing the relatively sophisticated adjustment procedure.

In addition to the benefits of internal trimming, the AD532, which can be used in the same socket as the AD530 by omitting the external trim connections, offers significant versatility in new applications by providing differential X and Y inputs (typical 75dB CMR), and an output null terminal which permits an independent setting of the output offset.

The AD532J and AD532K operate from 0 to $+70^{\circ}$ C and have maximum multiplying errors of $\pm 2\%$ and $\pm 1\%$ of full scale at $+25^{\circ}$ C. The AD532S is guaranteed for a maximum error of $\pm 1\%$ at $+25^{\circ}$ C, and is 100% temperature tested to guarantee a maximum error of $\pm 4\%$ from -55° C to $+125^{\circ}$ C.

MIL-STD-883

All wide temperature range versions of the IC multipliers are available as standard products with processing to MIL-STD-883, Method 5004, Class B. Type numbers are AD530S/883, AD531S/883, AD532S/883.

AD530 SPECIFICATIONS (Typical @ +25°C, externally trimmed and ±15VDC, unless otherwise specified.)

CIRCUIT FUNCTIONS



*With Z (feedback) terminal used as an input terminal.

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PARAMETER

AD531J (531K)(531L)(531S)

	······································
PERFORMANCE SPECIFICA	TIONS
Transfer Function	$V_{x} \cdot V_{y}/kIz$
Total Error (% FS, kIz = 10V)	
$T_A = 25^{\circ}C$	2.0%(1.0%)(0.5%)(1.0%) max
$T_A = min to max$	2.5%(1.5%)(1.5% max)(3.0% max)
Terminal Limits	
Input Voltage	$-10V \leq V_{X} \cdot V_{y} \leq +10V$
Reference Current	$0 \le kIz \le +10V, V_x/kIz \le 2.5$
Nonlinearity	
X input	0.8(0.5)(0.3)(0.5)%
Yinput	0.3(0.2)(0.2)(0.2)%
Z input $(0.1 < kIz < 10V)$	0.5(0.5)(0.5)(0.5)%
Feedthrough	
X input	150(80)(40)(80)mV max
Y input	100(60)(30)(60)mV max
Z input $(1 \leq klz \leq 10V)$	50(50)(50)(50)mV typ
INPUT SPECIFICATIONS	
X terminal	
Differential Input	
Resistance	10ΜΩ
Common Mode	
Input Resistance	80ΜΩ
Input Bias Current	8μA max
Common Mode	
Voltage Range	±10V min
CMRR	60dB
Y terminal	
Input Resistance	6ΜΩ
Input Bias Current	8μA max
Z terminal	
Reference Current	
(for kIz = 10V)	$+320\mu A \leq I_z \leq +490\mu A$
Sense Terminal	
Input Resistance	36kΩ
Input Bias Current	15μA max
Null Input Voltages	
V _{vo} , V _{os}	±15 (±10)(±10)(±10)V max
V _{xo}	$+10V < V_{xo} < +15V$
DVNAMIC SPECIFICATIONS	
Small Signal Unity Cain	1.000
Small Signal, Unity Gain	T.OMHZ
Full Power Bandwidth	750KHZ
Snew Kate Small Signal Amplitude	$+3 \sqrt{\mu}$ sec
Error	1% at 751-Uz
Small Signal 1% Vector	170 at 7 JKIIZ
Frror	5kHz
Settling Time	Jusec to 2%
Overload Recovery	$\frac{1}{2} \frac{1}{2} \frac{1}$
overload recovery	2µ3CC 10 2 /0
OUTPUT AMPLIFIER SPECIF	FICATIONS
Output Voltage Swing	
$(T_A = \min \text{ to } \max)$	±10V min @ 5mA
Output Offset Voltage	
vs. Temperature	$0.7(0.7)(1.0 \text{ max})(2.0 \text{ max})\text{mV/}^{\circ}\text{C}$
POWER SUPPLY SPECIFICAT	TIONS
Supply Voltage	
Rated	±15V
Operating	± 15 to 18)(10 to 18)(10 to 18)
operating	(10 to 22)V
Supply Current quiescent	+6mA max
Power Supply Variation	-onix max
(includes effects of recomme	ended null nots)
Multiplier Accuracy	+0.5%/%
Output Offset	±10mV/%
Scale Factor	±0.1%/%
Feedthrough	$\pm 10 \text{mV}/\%$

\$30.00(\$45.00)(\$54.00)(\$60.00)

CIRCUIT FUNCTIONS





MULTIPLIER, SQUARER (FIXED SCALE FACTOR CONNECTION)



TRUE RMS-TO-DC CONVERTER



(1-24)

PRICE

AD532 SPECIFICATIONS (Typical @ +25°C and ±15VDC, unless otherwise specified.)

PARAMETER AD532J (AD532K)(AD532S) MULTIPLY MULTIPLIER SPECIFICATIONS Transfer Function $(V_{x_1} - V_{x_2})(V_{y_1} - V_{y_2})/10V$ X10 +XIN ZIN Total Error (% FS @ +25°C) 2.0%(1.0%)(1.0%) max -XIN X20 $(T_A = \min to max)$ 2.5%(1.5%)(4.0% max) OUT AD532 -0 vs. Temperature VOUT +YIN Y10 $(T_A = \min to max)$ $0.04(0.03)(0.02 \text{ max})\%/^{\circ}C$ YIN Y20 Nonlinearity X input 0.8%(0.5%)(0.5%) $(X_1 - X_2)(Y_1 - Y_2)$ VOUT Y input 0.3%(0.2%)(0.2%) 10V Feedthrough X input 150(80)(80)mV max Y input 100(60)(60)mV max **DIVIDER SPECIFICATIONS* Transfer Function** $10Z/(X_1 - X_2)$ Total Error (% FS) 2.0%(1%)(1%) **DIFFERENCE OF SQUARES** SQUARER SPECIFICATIONS $\pm X^{2}/10$ Transfer Function Total Error (% FS) 0.8%(0.4%)(0.4%) + XIN ZIN SQUARE ROOTER SPECIFICATIONS -XIN $-\sqrt{10V_{z_{in}}}$ * Transfer Function + YIN OUT AD532 Ó VOUT Total Error (% FS) 0.8%(0.4%)(0.4%) -YIN INPUT SPECIFICATIONS $X^2 - Y^2$ CMRR X_{in} , $Y_{in} = \pm 10V$ 40(60)(60)dB min V_{OUT}= 10 Input Resistance X input 10MΩ Y input 10MΩ Z input* 36kΩ Input Bias Current X, Y inputs 3.0(4.0 max)(4.0 max)µA Z input* 10(15 max)(15 max)µA Input Voltage (for rated accuracy) DIVIDE V_x, V_y, V_z $(T_A = \min to \max)$ ±10V ZIC Null Input Voltage (required to trim) Vos ±15V max X10 +X IN ZIN DYNAMIC SPECIFICATIONS -X_{IN} X20 AD532 OUT Small Signal, Unity Gain -0 +YIN 1.0MHz VOUT Full Power Bandwidth 750kHz YIN Slew Rate 45V/µsec ÷ Small Signal Amplitude Error 1% at 75kHz Small Signal 1% Vector Error 5kHz 10Z 1 $V_{OUT} = \frac{1}{(X_1 - X_2)}$ Settling Time 1µsec to 2% ; -10V<(X₁-X₂)≰OV **Overload Recovery** 2µsec to 2% **OUTPUT AMPLIFIER SPECIFICATIONS** Output Voltage Swing $(T_A = min to max)$ ±10V min @ 5mA Output Offset Voltage** ±50(±20)(±20)mV max 0.7(0.7)(2.0 max)mV/°C vs Temperature. **PIN CONFIGURATIONS** POWER SUPPLY SPECIFICATIONS **Top View** Supply Voltage H SUFFIX Rated ±15V Operating ±15 to 18(10 to 18)(10 to 22)V Supply Current, Quiescent ±6mA max **D** SUFFIX Power Supply Variation GND +Vs O2 Multiplier Accuracy ±0.5(±0.5 max)(±0.5 max)%/% **TO-116** Output Offset ±10(±10 max)(±10 max)mV/% Scale Factor ±0.1(±0.1)(±0.1)%/% 4 Feedthrough ±10(±10 max)(±10 max)mV/% PRICE (1-24)\$26.00(\$36.00)(\$49.00) **TO-100** *With Z (feedback) terminal used as an input terminal. **Trimmable to zero.

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12

9

10

new product: AD53

CIRCUIT FUNCTIONS

SWITCHES AND RESISTOR NETWORKS FOR A/D AND D/A CONVERTERS AD550, AD551, AD552, AD555, AD850, AD852, AD853, AD855

GENERAL DESCRIPTION

The converter components discussed in this section were designed to form the heart of current and voltage switched D/A and A/D converters.

CURRENT STEERING CONVERTERS

The AD550 and AD551 are quad current switches that can be provided in matched sets to build 4, 8 and 12-bit converters. The AD552 is a quint current switch for building 5 and 10-bit converters. They consist of four (AD550, AD551) or five (AD552) logic-operated current steering switches with a reference transistor on a single monolithic chip. Further, the switch emitter areas are geometrically proportioned to achieve constant current density and thus attain virtually perfect V_{BE} matching and tracking between switches. The reference transistor is provided to compensate the external voltage reference, which powers the binary current determining resistor ladder network (e.g., AD850) for V_{BE}.

The basic operation of the current steering switch is shown in Figure 1 using the AD551. For a nominal full scale output current of 2.0mA (less one LSB), a stable reference zener and precision resistor are used to establish a reference current of 1/8mA (LSB weight) into the reference transistor Q₁. The op amp then adjusts the common base rail so that the individual bit currents will assume their correct values, as shown. These bit currents are then steered into the load or the -5V supply according to the logic level at each input. A complete 12-bit converter is shown on the page describing the AD550, AD551 and AD552.

VOLTAGE SWITCHING CONVERTERS

The AD555 is a dielectrically-isolated quad voltage switch that can be provided in matched sets to build 4, 8 and 12-bit converters. Comprising four logic-operated single pole, double throw (SPDT) switches, the AD555 can switch AC signals at its reference terminals, making it ideal for multiplying and D/S and S/D converter applications. Voltage switching involves the switching of resistor legs of an R/2R ladder network (e.g., AD855) between two continuously variable voltage references as shown in Figure 2. Depending on the logic state of the input terminals, the 2R leg of the R/2R network will be connected to the voltage appearing on either Ref A or Ref B. The R/2R network has the property that, no matter what state the digital inputs are in, the impedance seen from the R/2R output (non-inverting terminal of the output amplifier) is always R. A complete 12-bit D/A converter is shown on the page describing the AD555 switch.

LADDER NETWORKS

The AD850 and AD852, AD853 are binary weighted resistor ladder networks for use with the current steering switches AD550, AD551 and AD552. The AD855 is an R/2R ladder for use with the AD555 voltage switch. Nichrome thin-film construction combined with small physical size offer temperature tracking of 1ppm/°C (within the network) and excellent long term stability.

The AD850 includes the binary ladder network and applications resistors to build complete 12-bit converters. For BCD weighting, order the AD851.

The AD852 can be used either alone to build 8-bit converters, or combined with the AD853 (which includes the last quad and the circuit applications resistors) to build full 12-bit converters.

The AD855 R/2R ladder has been specifically designed for use with the AD555 voltage switch ($R_{sw} \approx 15\Omega$, AD555 L/U) and includes the applications resistors for building 12-bit converters.



MONOLITHIC CURRENT SWITCHES AD550, AD551, AD552

GENERAL DESCRIPTION

The AD550 and AD551 are quad current switches for building 4, 8 and 12-bit accurate A/D and D/A converters. The AD552 is a quint current switch for building 5 and 10-bit converters. They feature monolithic construction to obtain tight switch matching and tracking with temperature and high reliability for military and avionics applications.

To obtain 12-bit linearity it is important that the AD550 and AD551 switches be ordered and used as matched sets. Units shipped as matched sets will be marked with a " V_{BE} group number" (-9 to +9) following the grade selection for the TO-116 package (e.g., 551K + 3D where +3 is the grade selection and D the package suffix) and following the pin 1 designator for the flat pack (e.g., \bullet +5XXXX, where \bullet is the pin 1 designator and XXXX the date code).

The AD552 does not require V_{BE} classification.

APPLICATION



NOTE: The AD850 includes the binary resistors, interquad attenuators, gain resistors, a bipolar option and reference current resistors on a single substrate.

ELECTRICAL CHARACTERISTICS (Typical @ +25°C unless otherwise noted)

Parameter	AD550	AD551	AD552	
Logic Inputs				
"0" (Switch ON)	0.8V max, 1.6mA nom. (Avg. Sum of 4)	0.8V max, 1.6mA max (Each Input)	0.8V max, 1.6mA max (Fach Input)	
"1" (Switch OFF)	2.0V min, 100µA max	*	(bach input)	
Common Base Bias Voltage	-2.0V max (-5.0V min)	*		
Input Coding	Complementary Binary	*		
Output Current (Nominal)				
Bit 1	1.0mA	*		
Bit 2	0.5mA	*		
Bit 3	0.25mA	*		
Bit 4	0.125mA	*	•	
Bit 5	N/A	N/A	0.062mA	
Output Voltage Limit				
Unloaded	$0V$ (Amplifier Σ pt)	*	•	
Resistor Load	-2V to +10V	*	•	
Switch Speed				
Switching Time (to turn on LSB) Settling Time to ±½LSB	500nsec	60nsec	90nsec	
12 Bits	1.8µsec	200nsec		
10 Bits	0.8µsec	120nsec	120nsec	
Accuracy (% Full Scale, With 10V				
Across Resistor Network)				
Linearity J/S	1.0% max	*	±1.0%	
K/T	0.1% max	*	±0.05%	
L/U	0.01% max	*	N/A	
Temperature Coefficient	2ppm/°C	*	7ppm/°C	
Power Requirements				
+5VDC (±5%)	±12mA max	*	•	
-15VDC (±3%)	-9mA max	-10mA max	-10mA max	
Packages	TO-87 (F.P.)	*		
	TO-116A (DIL)	*	TO-116B (DIL)	
Operating Temperature Range				
J, K, L	0 to $+70^{\circ}$ C	*		
S, T, U	-55° C to $+125^{\circ}$ C	*	•	
*Same as AD550.				

ORDERING GUIDE

AD550 X Y* Z	X =	Performance/Temperature Grade J, K, L, S, T, U
--------------	-----	--

AD551 X Y* Z $Y = V_{BE}$ Characteristic (-9 to +9)

AD552 X Z Z = JEDEC Package Designation D = TO-116, F = TO-87

*Do not specify unless ordering a replacement part. Units ordered as 12 bit matched sets will automatically be shipped with the same V_{BE} characteristic.

PRICES: Consult the factory or your local representative for the latest pricing.

VOLTAGE SWITCH AD555

APPLICATION



The AD555 is a dielectrically isolated quad voltage switch which is optimized for applications where both digital and analog signals vary – such as in digital to synchro conversion or multiplying DAC applications. Temperature coefficient has been specified to insure full 12 bit linearity when used with a $50k\Omega$ R-2R ladder network, such as the AD855.

DIGITAL NUMBER, N LSB MSB 1 VREF Vout AD5555 AD555 AD5551 VREF B R/2 2 ₹R/2 AD855 R-2R NETWORK LADDER

ELECTRICAL CHARACTERISTIC	S
Parameter	AD555
Input Signals	
Digital	"0" <0.8V max @ −500µA, max
	"1" >2.0V min @ +100µA, max
Analog 1. Ref A and/or Ref B	
in any combinations	-3 Volts, min to +3 Volts, max
2. Ref A Alone	
(Ref B Grounded)	-4 Volts, min to +4 Volts, max
Analog Input Current	
(Ref A or Ref B)	-1.5mA, max
Output Voltage Range	±4 Volts
Switch Offset Voltage, E _{os}	555 J/S +10mV, max
	555 K/T +3mV, max
	555 L/U +2mV, max
Switch Offset Mismatch, ΔE_{os}	AD555 L/U ± 1 mV, max
Switch on Resistance, R _S	555 J/S 100Ω, max
	555 K/T 40Ω, max
	555 L/U 25 Ω , max
On Resistance Mismatch, ΔR_S	555 L/U 10 Ω , max
Switch Load Current	0.5mA, max
Settling Time (0.01%)	5µsec
Switch Leakage Current	1.5nA, max
Error Temp Coefficient	±5ppm/°C
Power Requirements	±15V ±20% @ +7mA
	-4V ±1% @ -3mA
Dissipation	130mW (typ), 200mW (max)
Packages	TO-87 Flat Pack
	TO-116 Dual In-Line
Operating Temperature Range	Types J, K, L 0 to $+70^{\circ}$ C
	Types S, T, U -55° C to $+125^{\circ}$ C

ORDERING GUIDE:

AD555 X Y :

X = Performance/Temperature Grade J, K, L, S, T, U Y = Package designator D = TO-116 DIL F = TO-87 F.P.

GENERAL DESCRIPTION

The nichrome thin-film resistor networks outlined here have been designed for use with the μ DAC current and voltage switches already described. The AD850 is a 12-bit binary current determining ladder network for use with the AD550, AD551 and AD552 current switches, and the AD851 is its BCD equivalent. The AD852 is an eight-bit current ladder network for 8-bit applications, which can be extended to 12 bits using the AD853. The AD855 is an R/2R twelve-bit ladder network specifically designed for use with the AD555 voltage switch. All the networks include applications resistors to build the complete D/A converter.

BINARY CURRENT LADDER

ELECTRICAL SPECIFICATIONS (Typical @ +25°C, unless otherwise noted.)

Parameter	AD850 L (U)	AD852 L (U)	AD853 L (U)
$R1 = 10k\Omega$	±5% Abs.	±0.3% Abs.	
$R2 = 20k\Omega$	0.015%	0.015%	
$R3 = 40k\Omega$	0.03%	0.03%	
$R4 = 80k\Omega$	0.05%	0.05%	
$R5 = 10k\Omega$	0.10%	0.10%	
$R6 = 20k\Omega$	0.2%	0.2%	
$R7 = 40k\Omega$	0.4%	0.4%	
$R8 = 80k\Omega$	0.8%	0.8%	
$R9 = 10k\Omega$	1%		0.3% Abs.
$R10 = 20k\Omega$	1%		Ratio to R9 1%
$R11 = 40k\Omega$	1%		Ratio to R9 1%
$R12 = 80k\Omega$	1%		Ratio to R9 1%
$R13 = 5k\Omega$	0.1%		Ratio to R160.2%
$R14 = 14.0625 k\Omega$	Ratio to R17 0.05%	Ratio to R17 0.05%	
$R15 = 14.0625k\Omega$	Ratio to R17 1%		Ratio to R18 0.3%
$R16 = 5k\Omega$	0.1%		0.5% Abs.
$R17 = 1k\Omega$	±5% Abs.	±0.5% Abs.	
$R18 = 937.5k\Omega$	Ratio to R17 1%		0.3% Abs.
$R19 = 80k\Omega$	0.1%	0.2%	
$R20 = 6.00k\Omega$	0.1%		Ratio to R21 0.2%
$R21 = 48.40k\Omega$	0.1%		0.5% Abs.
$R22 = 15k\Omega$		Ratio to R17 0.5%	
Operating Temp. Range			
L Grade	$0 \text{ to } +70^{\circ}\text{C}$		1
U Grade	-55°C to +125°C	•	
Packages (Suffix E or F)	24 Pin Epoxy	TO-87 Flat Pack	TO-87 Flat Pack
(Suffix D)	24 Pin DIL	TO-116 DIL	TO-116 DIL

1. All resistors ratio to R1 unless otherwise specified.

2. Total positive or negative contribution to error is less than 0.012%.

3. AD851 (= BCD form of AD850): R13 = R16 = $4k\Omega$; R14 = $8.1325k\Omega$;

 $R15 = 8.4375 k\Omega.$

*Specifications same as for AD850.

R-2R VOLTAGE LADDER

ELECTRICAL SPECIFICATIONS (Typical @ +25°C, unless otherwise noted.)

Parameter	AD855 L (U)			
R	$50k\Omega \pm 10\%$ Abs.			
2R	100kΩ			
R _{SW}	15Ω			
Resistor Ratio Accuracy	<0.004%			
Operating Temperature Range				
L Grade	$0 \text{ to } +70^{\circ}\text{C}$			
U Grade	-55°C to +125°C			
Packages (Suffix F)	TO-87 Flat Pack			
(Suffix D)	TO-116 Dual-In-Line			









DUAL FET'S AD3954 SERIES

GENERAL DESCRIPTION

Types AD3954 through AD3958 are a family of dual monolithic N-channel silicon junction field-effect transistors in the hermetically-sealed TO-71 package. They are designed to provide low input drift (to $5\mu V/^{\circ}C$ max) and bias current (to 50pA max) when used in the input stages of general-purpose differential amplifiers. They will generally provide superior performance when replacing equivalent members of the 2N3954-58 family.

The dual FET's are fabricated on N-type silicon wafers, and the two elements are diffusion-isolated. This isolation eliminates gate-to-gate breakdowns; bulk biasing and input gate protection are not needed for the great majority of practical designs. Monolithic fabrication of dual FET's provides inherently superior matching by *design*, and eliminates the costly handling employed in assembling 2-chip duals, as well as improving yield and reliability. The low offset drifts resulting from this matching tend to be linear with temperature and can be maintained in practical environments because of the monolithics' insensitivity to thermal gradients.

ELECTRICAL CHARACTERISTICS (@ +25°C unless otherwise noted)

Parameter	Symbol	Conditions	AD3954A	AD3954	AD3955	AD3956	AD3958	Units
Drift vs Temperature	$\left \frac{\Delta V_{GS_{1-2}}}{\Delta T}\right _{max}$	$V_{DG} = 20V, I_D = 200\mu A$ $T_A = -55^{\circ}C \text{ to } +25^{\circ}C \text{ to } +125^{\circ}C$	} 5	10	25	50	100	μV/°C
Offset Voltage, $+25^{\circ}C$	V _{GS1-2} max	$V_{DG} = 20V, I_D = 200\mu A$) 10	10	25	25	25	mV
Temp Drift Nonlinearity	TDN	$V_{DG} = 20V, I_D = 200\mu A$	€ ±1	±1	±1	±1	±5	$\mu V/^{\circ}C$
	TDN max	$T_A = -55^{\circ}C \text{ to } +25^{\circ}C \text{ to } +125^{\circ}C$	2 ∩ ±5	±5	±5	±5	-	$\mu V/^{\circ}C$
Price (1-99)			6.90	5.65	4.25	3.00	2.25	\$

ALL DEVICES						
Parameter	Symbol	Conditions	MIN	ТҮР	MAX	Units
Transconductance						
Full Conduction	Y _{fss}	$V_{DG} = 20V, V_{GS} = 0, f = 1kHz$	1000	2000	3000	μ mho
Typical Operation	Y _{fs}	ſ	-	700	—	μ mho
Mismatch	$\frac{ Y_{fs_{1-2}} }{ Y_{fs} }$	$V_{DG} = 20V, I_D = 200\mu A$	-	0.6	3	%
Drain Current						
Full Conduction	IDSS		0.5	2	5	mA
Mismatch at Full Conduction	$\frac{I_{\text{DSS}_{1-2}}}{I_{\text{DSS}}}$	$V_{\rm DG} = 20V, V_{\rm GS} = 0$	-	1	5	%
Gate Current						
Operating	-IG	$V_{DG} = 20V, I_D = 200\mu A$	-	20	50	pA
High Temperature	-I _G	$V_{DG} = 20V, I_D = 200\mu A, T_A = +125$	5°C –	-	50	nA
Reduced VDG	-I _G	$V_{DG} = 10V, I_D = 200\mu A$	-	5	_	pA
Forward Current	I_G (f) D*	Any Condition	-	-	50	mA
At Full Conduction	-I _{GSS}	$V_{DG} = 20V, V_{DS} = 0$	-	-	100	pA
Output Conductance						
Full Conduction	Yoss	$V_{DG} = 20V, V_{GS} = 0$	-	-	5	μ mho
Operating	Yos	$V = 20 V I = 200 \mu A$	-	0.1	1	μ mho
Differential	Y _{os1-2}	$v_{DG} = 20v, I_D = 200\mu A$	-	0.01	0.1	μ mho
Common Mode Rejectio	n	(
$\Delta V_{GS_{1-2}}$	CMR	ΔV_{DS} = 10 to 20V, I _D = 200 μ A	-	100	_	dB
$-20 \log \left \frac{\Delta V_{DS}}{\Delta V_{DS}} \right $	CMR	${\bigtriangleup V_{\rm DS}}$ = 5 to 10V, $I_{\rm D}$ = 200 $\mu {\rm A}$	-	75	-	dB
PIN CONFIGURATION Bottom View

TO-71

ALL DEVICES									
Parameter	Symbol	Conditions	MIN	TYP	MAX	Units			
Gate Voltage Pinchoff Voltage	V _{GS} (off) or V _p	$V_{DS} = 20V, I_D = 1nA$	1	2	4.5	v			
Operating Range	V _{GS}	$V_{DS} = 20V, I_D = 200\mu A$	0.5	-	4	v			
Breakdown Voltage	BVGSS	$V_{DS} = 0, I_D = 1nA$	40	-	_	v			
To Source or Drain	V _{GSS} D*	Any Condition	2 <u>-</u> 5	-	40	v			
Gate-to-Gate Breakdo	wnVGGO	$I_{G} = 1nA, I_{D} = 0, I_{S} = 0$	40	-		v			
Drain-Source Voltage	V _{DSO} D*	Any Condition	-	-	40	v			
Noise Figure	NF	$V_{DS} = 20V, V_{GS} = 0, R_G = 10M\Omega$ f = 100Hz, NBW = 6Hz	-	-	0.5	dB			
Voltage	en	$v_{\rm DS} = 20v, n_{\rm D} = 200\mu A, n = 10HZ$ NBW = 1Hz	-	25	70	nV/\sqrt{Hz}			
Capacitance									
Input	Ciss		-	—	6	pF			
Reverse Transfer	Crss	$v_{\rm DS} = 20V, v_{\rm GS} = 0, t = 1 \text{MHz}$	_	—	2	pF			
Drain to Drain	C _{dd}	$V_{DG} = 20V, I_D = 200\mu A$	_	0.1	-	pF			
Temperature									
Storage	T _S D*	Any Condition	-65	_	+150	°C			
Junction	T _I D*	Any Condition	—	-	+150	°C			
Lead	T _L D*	10 sec max $- 1/16''$ or more from case	-	_	+300	°C			
Can Dissipation	P _D D*	$T_A = +25^{\circ}C$, Derate $3.3 \text{mW/}^{\circ}C$	-	-	400	mW			

ELECTRICAL CHARACTERISTICS (Continued)

*D indicates an Absolute Maximum Limit above which Degradation or Destruction may occur.

DUAL LOW IG FET'S AD5905 SERIES

GENERAL DESCRIPTION

Types AD5905 through AD5909 are a family of smallgeometry dual monolithic N-channel silicon junction FET's. They are designed for use in low level differential amplifiers that measure small currents, or small voltages at high impedance, and in high-impedance analog computing circuitry (e.g., long-term integrators, slow differentiators). They will generally provide superior performance when used to replace members of the 2N5902-9 and U248-251 families.

The dual device is fabricated on N-type silicon wafers with diffusion isolation between the two FET's. For this reason, low "punch-through" gate-gate breakdowns are eliminated, and bulk biasing is not needed for most applications. The substrate is connected to the can, and can be used as an effective shield and guard in circuit designs demanding extremely-low leakage current.

With leakage currents less than 1pA at V_{DG} = 10V, and even less at lower voltages, these dual junction FET's, used with circuit design and assembly techniques appropriate to their capabilities, will excel in such applications as pH meters, photo and ion-current transducers, low-drift integrators, and sample-holds.

PIN CONFIGURATION Bottom View



TO-71

ELECTRICAL CHARACTERISTICS (@ +25°C unless otherwise noted)

Parameter	Symbol
Gate Difference Voltage	
Drift vs Temperature	$\left \frac{\Delta \mathbf{V}_{\mathrm{GS}_{1-2}}}{\Delta \mathrm{T}} \right \max$
Offset Voltage, $+25^{\circ}C$	V _{GS1-2} max
Temp Drift, Nonlinearity	TDN
Gate Leakage Current	
Operating	-I _G max
$T_A = +125^{\circ}C$	-I _G max
Full Conduction	-IGSS max
$T_A = +125^{\circ}C$	-l _{GSS} max
Price (1-99)	

Parameter	Symbol
Transconductance	
Full Conduction	Yfss
Typical Operation	Yfs
Mismatch	$\left \frac{Y_{fs_{1-2}}}{Y_{fs}}\right $
Drain Current	1 1
Full Conduction	Ince
i un conduction	
Mismatch, at	$\frac{1}{\text{DSS}_{1-2}}$
Full Conduction	I _{DSS}
Output Conductor co	
Eull Conductance	V
Pull Conduction	YOSS
Differential	V I
Differential	Y _{os1-2}
Common Mode Rejection	
$ \Delta V_{GS} $	CMP
$-20 \log \left(\frac{GS_{1-2}}{\Delta V} \right)$	CMR
	CMIK
Gate Voltage	-V _n or
Pinchoff Voltage	$-V_{CS}$ (off)
Operating Pange	-V
Breakdown Voltage	VGS
To Source or Drain	DYGSS
Cate to Cate Breakdown	VGSS D
Gale-to-Gale Bleakdown	D V GGO
Gate Current	
Gate-to-Gate Leakage	IGGO
Gate Reverse Current	$-I_G D^*$
Gate Forward Current	I_G (f) D*
Drain to Source Voltage	-V _{DSO} D*
Noise	
Figure	NF
5	
Spot Voltage	en
Capacitance	
Input	Ciss
Reverse Transfer	Crss
Drain to Drain	C _{dd}
Temperature	
Storage	T _c D*
Junction	TI D*
Lead	T _I D*
Can Dissination	Pp D*
Can Dissipation	TD D

Conditions	AD5906	AD5907	AD5908	AD5909	AD5905	Units	
$V_{} = 10V_{} = 2000$							
$v_{DG} = 10v, i_D = 50\mu A$ T _A = -55°C to +25°C to +125°C	5	10	20	40	75	μV/°C	
$V_{\rm RC} = 10V_{\rm RC} = 3000$	25	25	25	25	25	mV	
$V_{DC} = 10V, I_{D} = 30\mu A$	25	25	25	25	25	iii v	
$T_{A} = -55^{\circ}C \text{ to } +25^{\circ}C \text{ to } +125^{\circ}C$	±1	±1	±1	±1	±5	μV/°C	
(1	1	1	1	3	nA	
$V_{DG} = 10V, I_D = 30\mu A$	1	1	1	1	3	nA	
$V_{DS} = 0, V_{GS} = -20V$	2	2	2	2	5	pA	
(5 11.20	5 8 90	5 7.00	5.10	4 20	nA \$	
	11.00	0.70	ALL DEVICES	S		Ψ	
Conditions	MIN	I	TYP		MAX	Units	
	-		100				
$V_{DG} = 10V, V_{GS} = 0, f = 1kHz$	(50		300		500 200	μ mho μ mho	
$V_{DG} = 10V$, $I_D = 30\mu A$, $f = 1 \text{kHz}$	}						
	(–		1		5	%	
			100				
	60		400		1000	μA	
$V_{DG} = 10V, V_{GS} = 0$	l –		2		5	%	
$V_{DG} = 10V, V_{GS} = 0$	_		—		5	μmho	
$V_{DC} = 10V$, $I_D = 30\mu A$	1 -		-		0.5	μmho	
) –		-		0.1	μmho	
$\Delta V_{DS} = 10$ to 20V, $I_D = 30\mu A$ $\Delta V_{DS} = 5$ to 10V, $I_D = 30\mu A$	-		90 90		_	dB dB	
			,,,			u b	
$V_{DS} = 10V, I_D = 1nA$	0.6		2		4.5	v	
$V_{DG} = 10V, I_D = 30\mu A$	-		-		4	v	
$V_{DS} = 0$, $I_D = 1nA$	-40		-60		- 40	v	
$I_{C} = 1nA, I_{D} = 0, I_{S} = 0$	40		_		-	v	
$V_{GG} = 20V$	-		1		-	pA	
Any Condition Any Condition	_		_		10	mA	
	-		_		40	v	
$V_{\rm DS} = 10V, V_{\rm GS} = 0, R_{\rm G} = 10M\Omega$	_		_		1	dB	
f = 100Hz, NBW = $6Hz$			-		•	11/11	
$\left.\begin{array}{l} V_{DG} = 10V, I_D = 30\mu A\\ NBW = 1Hz, f = 10Hz \end{array}\right\}$	_		70		-	nV/V Hz	
	1 -		_		3	pF	
$V_{DS} = 10V, V_{GS} = 0, f = 1MHz$	1 -		-		1.5	pF	
$V_{DG} = 10V, I_D = 30\mu A$	-				0.1	pF	
	-65		_		+150	°C	
	-		-		+150	°C	
10 sec max $- 1/16''$ or more from case			—		+300	°C	
$T_{A} = +125^{\circ}C$	-		-		40	mW	

*D indicates an Absolute Maximum Limit above which Degradation or Destruction may occur.

DUAL ULTRA LOW IG FET'S AD830 SERIES

GENERAL DESCRIPTION

Types AD830 through AD833 are a family of small-geometry dual monolithic N-channel silicon junction FET's. They are designed for use in low-level differential amplifiers that measure extremely small currents, or small voltages at very high impedance, and in high-impedance analog-computing circuitry (e.g., long-term integrators, slow differentiators). They will generally provide superior performance when used to replace devices having similar geometry but higher leakage currents, such as members of the AD5905-5909 family.

The dual device is fabricated on N-type silicon wafers using silicon nitride passivation, with diffusion isolation between the two FET's. For this reason, low "punch-through" gategate breakdowns are eliminated, and bulk biasing is not needed for most applications. The substrate is connected to the TO-78 can, and a connection is provided to use it as an effective shield and guard in circuit designs demanding extremely-low leakage current and noise pickup.

With leakage currents less than 0.1 pA at V_{DG} = 10V, and even less at lower voltages, these dual junction FET's, used with circuit design and assembly techniques appropriate to their capabilities, will excel in such applications as pH meters, electrometers, photo and ion-current transducers, low-drift integrators, and sample-holds.

> **PIN CONFIGURATION Bottom View**



TO-78

ELECTRICAL CHARACTERISTICS

(@ +25°C unless otherwise noted)

Parameter	Symbol
Gate Difference Voltage	
Drift vs Temperature	$\left \frac{\Delta V_{GS_{1-2}}}{\Delta T} \right \max$
Offset Voltage, +25°C	V _{GS1-2} max
Temp Drift, Nonlinearity	TDN TDN max
Gate Leakage Current	
Operating	-I _G max
$T_A = +125^{\circ}C$	-I _G max
Full Conduction	-I _{GSS} max
$T_A = +125^{\circ}C$	-I _{GSS} max
Price(1-99)	

Parameter Symbol Transconductance **Full Conduction** Yfss **Typical Operation** Yfs $Y_{fs_{1-2}}$ Mismatch Yfs Drain Current **Full Conduction** IDSS IDSS₁₋₂ Mismatch, at IDSS **Full Conduction Output** Conductance **Full Conduction** Yoss Operating Yos Differential Yos₁₋₂ Common Mode Rejection $\Delta V_{GS_{1-2}}$ CMR -20 log ΔV_{DS} CMR Gate Voltage -Vp or Pinchoff Voltage -V_{GS} (off) **Operating Range** -V_{GS} BVGSS Breakdown Voltage To Source or Drain -VGSS D* Gate-to-Gate Breakdown BVGGO Gate Current Gate-to-Gate Leakage IGGO $-I_G D^*$ Gate Reverse Current I_G (f) D* Gate Forward Current Drain to Source Voltage -V_{DSO} D* Noise Figure NF Spot Voltage en Capacitance Input Ciss **Reverse** Transfer Crss Drain to Drain Cdd Temperature T_s D* Storage T_J D* Junction $T_L D^*$ Lead P_D D*

Can Dissipation

	Conditions	AD830	AD831	AD832	AD833	AD833A	Units
	$V_{DG} = 10V, I_D = 30\mu A$.0
	$T_{A} = -55^{\circ}C \text{ to } +25^{\circ}C \text{ to } +125^{\circ}C $	5	10	20	75	40	µV/°C
	$V_{DG} = 10V, I_D = 30\mu A$	25	25	25	25	25	mV
	$V_{DG} = 10V, I_D = 30\mu A$	±1	±1	±1	±5	±1	μV/°C
	$T_{A} = -55^{\circ}C \text{ to } +25^{\circ}C \text{ to } +125^{\circ}C $	±5	±5	±5	-	±5	μV/°C
	1	0.1	0.1	0.1	0.5	0.1	pА
	$V_{DG} = 10V, I_D = 30\mu A$	0.1	0.1	0.1	0.5	0.1	nA
	$V_{DS} = 0, V_{CS} = -20V$	0.2	0.2	0.2	1.0	0.2	pA
		0.5 13.40	0.5	0.5 8.60	1.0	0.5 7.00	nA \$
_		15.10	AI	L DEVICES			
	Conditions	MI	N	ТҮР	MAX	Units	
	$V_{DG} = 10V, V_{GS} = 0, f = 1kHz$	70 50		300 100	500 200	µmho µmho	
	$V_{DG} = 10V, I_D = 30\mu A, f = 1kHz$	}		1	E	9/	
		(–		1	5	70	
		60		400	1000	μA	
	$V_{DG} = 10V, V_{GS} = 0$	1 _		2	5	04	
				2	5	70	
	$V_{DG} = 10V, V_{GS} = 0$	-		_	5	μmho	
	$V_{DG} = 10V, I_D = 30\mu A$	{ -		-	0.5	μmho	
		(–		-	0.1	μmho	
	ΔV_{DS} = 10 to 20V, I _D = 30 μ A			90	_	dB	
	$\Delta V_{DS} = 5$ to 10V, $I_D = 30\mu A$	-		90	-	dB	
	$V_{DS} = 10V, I_D = 1nA$	0.6		2	4.5	v	
	$V_{DG} = 10V, I_D = 30\mu A$	_		-	4	v	
	$V_{DS} = 0$, $I_D = 1nA$	-40)	-60	-	V	
	Either V_{GS} or V_{GD}	-		_	40	V	
	$I_{G} = I_{HA}, I_{D} = 0, I_{S} = 0$	40		-		•	
	$V_{GG} = 20V$	_		1	-	pA	
	Any Condition	_		_	10	μA mA	
	They condition	-		_	40	v	
	V_{DS} = 10V, V_{GS} = 0, R_G = 10M Ω	}		_	1	dB	
	f = 100Hz, NBW = 6Hz	2		70		nV/4/Hz	
	NBW = 1Hz, f = 10Hz	} -		70		11 1 1 1 1 2	
	$V_{DS} = 10V$, $V_{CS} = 0$, $f = 1MH_7$	2 -		_	3	pF	
	$V_{DC} = 10V$, $V_{C} = 300A$	(-		_	1.5	pF	
	DG = 100, D = 50021					P-	
		-65	5	—	+150	ိင	
	10 sec max $-1/16''$ or more from case	e _		-	+150	°C	
	To see max = 1/10 or more from cas	-					

*D indicates an Absolute Maximum Limit above which Degradation or Destruction may occur.

DUAL ULTRA LOW NOISE FET'S AD840 SERIES

GENERAL DESCRIPTION

TRAK-FET's, AD840/841/842 are large geometry, dual monolithic silicon N-channel J-FET's optimized for operation in differential amplifier applications where extremely low noise levels are required. The AD840 series is ideal for sensing very small signals commonly found in optoelectronic and biomedical applications.

The dual FET's are fabricated on N-type silicon wafers and the two elements are diffusion isolated. This isolation eliminates gate-to-gate breakdowns; bulk biasing and input gate protection are not generally needed.

The AD840 series dual monolithic FET's are the only devices available where initial offset voltage and drift can be closely correlated. The secret: a breakthrough in process and a thorough understanding of critical parameters in matching and tracking.

These devices are almost as predictable as dual monolithic transistors. At the same time, no interdigitated geometry is needed to obtain this close matching and tracking, hence no gate-to-gate breakdown problems at $2 \times V_p$.

For these reasons the AD840 series is offered at extremely low $V_{GS_1} - V_{GS_2}$ offsets, 5mV maximum, and tracking, 5 and $10\mu V/^{\circ}C$.

Outside these most important parameters, very close Y_{fs} and Y_{os} matching is natural for these devices. Furthermore, these devices were specifically designed for very low voltage noise, less than $15nV/\sqrt{Hz}$ @ 10Hz.

Besides all these features, the devices do not compromise on gate leakage current as the typical number of 5pA @ 10V indicates.

The above given characteristics make these FET's superior replacements for the 2N5515, 2N5520 series which in contrast are hybrid dual-chip devices.

PIN CONFIGURATION

Bottom View



TO-71

SPECIFICATIONS

(@ +25°C unless otherwise noted)

Parameter	Symbol
Drift vs Temperature	$\frac{\Delta V_{GS_{1-2}}}{\Delta T \max}$
Offset Voltage, +25°C	V _{GS1-2} max
Temp Drift Nonlinearity	TDN TDN max

Price (1-99)

Parameter	Symbol
Transconductance	
Full Conduction	Y _{fss}
Typical Operation	Y _{fs}
Mismatch	$\left \frac{Y_{fs_{1-2}}}{Y_{fs}} \right $
Drain Current Full Conduction	I _{DSS}
Mismatch at Full Conduction	IDSS
Gate Current Operating High Temperature Reduced V _{DG} Forward Current At Full Conduction	-I _G -I _G -I _G I _G (f) D* -I _{G SS}
Output Conductance Full Conduction Operating Differential	$ \begin{vmatrix} Y_{0SS} \\ Y_{0S} \\ Y_{0S_{1-2}} \end{vmatrix} $
Common Mode Rejection -20 log $\left \frac{\Delta V_{GS_{1-2}}}{\Delta V_{DS}} \right $	CMR
Gate Voltage	
Pinchoff Voltage	V _{GS} (off) or V _p
Operating Range Breakdown Range To Source or Drain Gate-to-Gate Breakdown	V _{GS} BV _{GSS} V _{GSS} D* V _{GC}
Drain Source Voltage	V D*
Naisa	VDSO D
Noise	
Voltage	en
Voltage	en
Capacitance	
Input Reverse Transfer Drain to Drain	C _{iss} C _{rss} C _{dd}
Temperature	
Storage	T _S D*
Junction	T _J D*
Lead	T _L D*
Can Dissipation	P _D D*

new product: AD840

Conditions		AD840	AD841	AD842	Units
$V_{DG} = 20V, I_D = 200\mu A$ $T_A = -55^{\circ}C \text{ to } +25^{\circ}C \text{ to } +125^{\circ}C$	ł	5	10	40	$\mu V/^{\circ} C$
$V_{DG} = 20V, I_D = 200\mu A$		5	5	25	mV
$V_{DG} = 20V, I_D = 200\mu A$ $T_A = -55^{\circ}C \text{ to } +25^{\circ}C \text{ to } +125^{\circ}C$	}	±1 ±3	±1 ±3	±1 ±3	$\mu V/^{\circ} C$ $\mu V/^{\circ} C$
		9.40	7.80	3.50	\$

	вотн	DE	VICES			
	Conditions		MIN	ТҮР	MAX	Units
	$V_{DG} = 20V, V_{GS} = 0, f = 1kHz$		1,000		4,000	µmho
	$V_{DG} = 20V, I_D = 200\mu A$	5	500		1,000	μmho
		1		0.6	3	%
	$V_{DG} = 20V, V_{GS} = 0$	}	0.5	2	5	mA
		(1	,	70
	$V_{DG} = 20V, I_D = 200\mu A$			20	50	pA
	$V_{DG} = 20V, I_D = 200\mu A, T_A = +125^{\circ}C$				50	nA
	$V_{DG} = 10V, I_D = 200\mu A$			5		pA
	Any Condition				50	mA
	$\mathbf{v}_{\mathbf{D}\mathbf{G}} = 20\mathbf{v}, \ \mathbf{v}_{\mathbf{D}\mathbf{S}} = 0$				100	рА
	$V_{DC} = 20V, V_{CS} = 0$				10	µmho
	$V_{\rm TR} = 20 V_{\rm TR} = 200 \mu \Lambda$	1		0.1	1	µmho
	VDG - 20V, ID - 200µA	1		0.01	0.1	µmho
	$\triangle V_{DS}$ = 10 to 20V, I_D = 200 μA			100		dB
	$\triangle V_{DS}$ = 5 to 10V, I_D = 200 μA			75		dB
	$V_{DS} = 20V, I_D = 1nA$		1	2	4.5	V
	$V_{DS} = 20V I_{D} = 200 \mu A$		0.6		4	V
	$V_{DS} = 0$, $I_D = 1$ nA		40			v
	Any Condition				40	V
	$I_{\rm G} = 1 {\rm nA}, I_{\rm D} = 0, I_{\rm S} = 0$		40			V
	Any Condition				40	v
	$V_{DS} = 20V, I_D = 200\mu A, f = 10Hz$ NBW = 1Hz				15	nV/√Hz
	$V_{DS} = 20V, I_D = 200\mu A, f = 1kHz$ NBW = 1Hz				10	nV/√Hz
		(25	pF
	$V_{DS} = 20V, V_{GS} = 0, f = 1MHz$	1			5	pF
	$V_{DG} = 20V, I_D = 200\mu A$	•		0.1		pF
	Any Condition		-65		+150	°C
	Any Condition				+150	°C
	10 sec max-1/16" or more from case				+300	°C
	$T_A = +25^{\circ}C$, Derate $3.3 \text{mW/}^{\circ}C$				400	mW
_						

*D indicates an Absolute Maximum Limit above which Degradation or Destruction may occur.

DUAL NPN TRANSISTORS AD810 SERIES

GENERAL DESCRIPTION

The Analog Devices AD810, AD811, AD812, and AD813 are monolithic dual NPN transistors designed for use in ADI's modular products. Thus, they are suited for a wide range of applications requiring excellent matching of characteristics, high current gain, and high voltage breakdown.

The AD810 series is manufactured with linear I.C. processing techniques. The resulting V_{BE} characteristics – voltage differential less than 0.5mV, temperature drift below $2.5\mu V/^{\circ}$ C, breakdown voltage above 40V – make the devices ideal for critical differential input stage requirements. In addition, the excellent current gain performance – typically 500 over a 10μ A to 5mA collector range – insures high performance operation in second stage applications.

The AD810, AD811, AD812, and AD813 are specified for operation over the -55° C to $+125^{\circ}$ C temperature range and are supplied in the hermetically sealed TO-71 package.

PIN CONFIGURATION Bottom View



TO-71

MATCHING CHARACTERISTICS ($T_A = +25^{\circ}C$, unless otherwise noted)							
Parameter	Test Condition	Limit	AD810	AD811	AD812	AD813	Units
$V_{BE1} - V_{BE2}$	$I_{c} = 10\mu A$ to 5.0mA, $V_{ce} = 5.0V$	max	3.0	1.5	1.0	0.5	mV
$\frac{\Delta(V_{BE1} - V_{BE2})}{\Delta T}$	$I_c = 10\mu A, V_{ce} = 5.0V$ $T_A = -55^{\circ}C \text{ to } +125^{\circ}C$	max	15	7.5	5.0	2.5	μV/°C
$I_{B1} - I_{B2}$	$I_c = 10\mu A, V_{ce} = 5.0V$	max	20	10	2.5	5	nA
$\frac{\Delta(I_{B1} - I_{B2})}{\Delta T}$	$I_{c} = 10\mu A, V_{ce} = 5.0V T_{A} = -55^{\circ}C \text{ to } +125^{\circ}C $	max	0.6	0.3	0.3	0.3	nA/°C

ELECTRICAL CHARACTERISTICS ($T_A = +25^{\circ}C$, unless otherwise noted)

Parameter	Test Condition	Limit	AD810	AD811	AD812	AD813	Units
h _{EE}	$I_c = 10\mu A, V_{ce} = 5.0V$	(min	100	200	400	200	
I. F.		1 max	_	600	1000	600	-
h _{EE}	$I_c = 1.0 \text{mA}, V_{ce} = 5.0 \text{V}$	min	100	200	400	200	-
h _{FF}	$I_c = 5.0 \text{mA}, V_{ce} = 5.0 \text{V}$	min	85	170	350	170	-
$h_{\rm FF}$ (-55°C)	$I_c = 10\mu A, V_{ce} = 5.0V$	min	35	75	150	75	—
BVCBO	$I_{c} = 10\mu A, I_{e} = 0$	min	35	45	35	45	V
BVCEO	$I_{\rm b} = 0, I_{\rm c} = 5.0 {\rm mA}$	min	35	45	35	45	V
BVCC	$I_{cc} = 10\mu A$	min	35	40	50	50	V
BVERO	$I_e = 10\mu A, I_c = 0$	min	6.5	6.5	6.5	6.5	V
V _{CE} (sat)	$I_{c} = 1.0 \text{mA}, I_{b} = 0.1 \text{mA}$	max	0.5	0.3	0.3	0.3	V
V_{CE} (sat)	$I_{c} = 5.0 \text{mA}, I_{b} = 0.5 \text{mA}$	max	1.0	0.8	0.8	0.8	V
V_{BE} (sat)	$I_c = 5.0 \text{mA}, I_b = 0.5 \text{mA}$	max	0.9	0.9	0.9	0.9	V
V_{BE} (on)	$I_{c} = 10\mu A, V_{ce} = 5.0V$	max	0.7	0.7	0.7	0.7	V
I _{CBO}	$I_e = 0$, $V_{eb} = 80\%$ rated BV_{CBO}	max	1.0	0.2	0.2	0.2	nA
I_{CBO} (+150°C)	$I_e = 0$, $V_{cb} = 80\%$ rated BV_{CBO}	max	1.0	0.2	0.2	0.2	μA
IFRO	$I_c = 0, V_{eb} = 5.0V$	max	0.3	0.2	0.2	0.2	nA
Cab	$I_e = 0, V_{eb} = 5.0V$	typ	2.5	2.5	2.5	2.5	pF
f_{τ}	$I_c = 1.0 \text{mA}, V_{ce} = 5.0 \text{V}$	typ	125	125	125	125	MHz
Price (1-99)			2.00	2.60	3.80	4.75	\$

DUAL "SUPERBETA" NPN TRANSISTORS AD814 SERIES

GENERAL DESCRIPTION

Fypes AD814, AD815 and AD816 are super-beta, monolithic lual NPN transistors which are designed to provide very high DC current gain over wide, collector current ranges with attendant high breakdown voltages. When used in the input stages of differential amplifiers, they provide very low offset voltages with very low drift over temperature. High gain, coupled with high breakdown voltages, tight V_{BE} matching and low output capacitance are all characteristics enhancing a wide range of applications.

The AD814 series is manufactured utilizing super-beta NPN transistor technology, and advanced silicon nitride passivation techniques. The resulting V_{BE} characteristics – voltage differential less than 0.2mV, temperature drift below $1\mu V/^{\circ}C$, breakdown voltages of 20V – 30V make these duals ideal for applications requiring critical, differential input stages. Also, very high DC gain of 2000 from 1 to 500 μ A makes for most efficient second stage applications.

The AD814, AD815 and AD816 are specified for operation over the full military temperature range $(-55^{\circ}C \text{ to } +125^{\circ}C)$ and are supplied in hermetically-sealed TO-71 packages.

PIN CONFIGURATION Bottom View



SPECIFICATIONS (@	$2 + 25^{\circ}$ C unless otherwise noted)					
Parameter	Test Condition	AD814	AD815	AD816	Units	
h _{FE1} min	$l_{\rm C} = 1 \mu {\rm A}, {\rm V}_{\rm CE} = 5 {\rm V}$	1000	2000	2000		
h_{FE_2} min	$I_C = 10\mu A$, $V_{CE} = 5V$	1000	2000	2000		
h _{FE3} min	$l_{\rm C} = 500 \mu A, V_{\rm CE} = 5 V$	1000	2000	2000		
h_{FE_4} (-55°C)	$I_{\rm C} = 100 \mu A, V_{\rm CE} = 5 V$	600	800	800		
BVCBO	$I_{\rm C} = 100 \mu {\rm A}, I_{\rm E} = 0$	35	20	10	V	
BV _{EBO}	$I_{\rm E} = 10\mu A, I_{\rm C} = 0$	7	7	7	V	
V _{CEO} (sust)	$I_{\rm C} = 100 \mu {\rm A}, I_{\rm B} = 0$	35	20	10	V	
 Price (1-99)		5.00	6.50	5.75	\$	
COMMON DEVICE P	ARAMETERS					
Parameter	Test Condition	MIN	TYP	MAX	Units	
V _{BE (on)}	$I_{\rm C} = 10\mu A$, $V_{\rm CE} = 5V$			0.7	V	
V _{CE} (sat)	$I_{C} = 1 \text{ mA}, I_{B} = 0.1 \text{ mA}$			0.5	V	
$ V_{BE_1} - V_{BE_2} $	$I_{\rm C} = 10\mu A$, $V_{\rm CE} = 1V$		0.2	1.0	mV	
$\left \frac{V_{BE}}{T} \right $	$I_{C} = 10\mu A, V_{CE} = 1V$ $T_{A} = -55^{\circ}C \text{ to } +125^{\circ}C$		1.0	5.0	$\mu V/^{\circ} C$	
ICBO 1	$I_{\rm E} = 0, V_{\rm CB} = 10V$			10	pA	
I_{CBO_2} (+150°C)	$l_{\rm E} = 0, V_{\rm CB} = 10 \rm V$			10	nA	
I _{EBO}	$I_{\rm C} = 0, V_{\rm EB} = 5 {\rm V}$			5	pA	
I _{C1C2}	$V_{CC} = \pm 100 V$			10	pA	
$[I_{B_1} - I_{B_2}]$	$I_{\rm C}=10\mu{\rm A},V_{\rm CE}=1V$			0.5	nA	
f _{T1}	$I_{\rm C} = 10\mu A$, $V_{\rm CE} = 5V$	10			MHz	
f _{T2}	$I_{\rm C} = 200 \mu A, V_{\rm CE} = 5 V$	100			MHz	
Сово	$I_{\rm E} = 0, V_{\rm CB} = 1V$			0.8	pF	
C _{TE}	$I_{\rm C} = 0, V_{\rm EB} = 0.5 {\rm V}$			1.0	pF	
C _{C1} C ₂	$V_{CC} = 0$			1.2	pF	
NF	$\left. \begin{array}{l} I_{\rm C} = 10 \mu {\rm A}, V_{\rm CE} = 3V \\ f = 1 {\rm kHz}, {\rm R}_{\rm G} = 10 {\rm k\Omega} \\ \\ {\rm BW} = 200 {\rm Hz} \end{array} \right\}$			3.0	dB	

DUAL "LOG CONFORMANCE" NPN TRANSISTORS AD818

GENERAL DESCRIPTION

The AD818 is an excellent dual monolithic NPN log conformance transistor designed specifically for computational circuits using logarithmic conversions.

The outstanding characteristic of the AD818 is the low r_e tracking error (Δr_e), typically 1 Ω , over a wide collector current range up to 1mA. This results in more than 6 decades of excellent log conformance.

Excellent reliability and long term stability are achieved through a proprietary device surface stabilization process that features a Nitrox[®] nitride passivation over the silicon and a Silox[®] glass passivation over the entire structure.

B Applied Materials Technology, Inc.

The AD818 is designed for operation over full military temperature range from -55° C to $+125^{\circ}$ C and is offered in hermetically-sealed TO-52 packages (TO-71 and TO-78 are optional).



MATCHING CHA	RACTERISTICS ($T_A = +25$	C and ± 15 V	DC, unless	otherwise not	ed)	
Parameter	Test Condition	MIN	TYP	MAX	Units	
$V_{BE_1} - V_{BE_2}$	$I_{\rm C} = 10 \mu A$, $V_{\rm CE} = 5.0 V$		0.4	1.0	mV	
$\frac{\triangle (V_{BE_1} - V_{BE_2})}{\triangle T}$	$I_{C} = 10\mu A$, $V_{CE} = 5.0V$ $T_{A} = -55^{\circ}C$ to $+125^{\circ}C$	}	1.0	5.0	μV/°C	
h _{FE1} /h _{FE2}	$I_{\rm C} = 10 \mu A, V_{\rm CE} = 5.0 V$			5	%	
$I_{B_{1}} - I_{B_{2}}$	$l_{\rm C} = 10 \mu A, V_{\rm CE} = 5.0 V$			10	nA	
$\frac{\triangle(\mathbf{I_{B_1}} - \mathbf{I_{B_2}})}{\triangle T}$	$I_{C} = 10\mu A, V_{CE} = 5.0V$ $T_{A} = -55^{\circ}C \text{ to } +125^{\circ}C$	}		0.5	nA/ [°] C	

ELECTRICAL CHARACTERISTICS ($T_A = +25^{\circ}C$ and ± 15 VDC, unless otherwise noted)

		ev e una -ry	· · • 0, ume	ou other whoe	noted)	
Parameter	Test Condition	MIN	TYP	MAX	Units	
hFE	$I_{\rm C} = 10 \mu A, V_{\rm CE} = 5.0 V$	150		600		
hFE	$I_{\rm C} = 100 \mu A$, $V_{\rm CE} = 5.0 V$	150		600		
hFE	$I_{C} = 1.0 \text{mA}, V_{CE} = 5.0 \text{V}$	150				
h _{FE} (-55°C)	$I_{\rm C} = 10 \mu A$, $V_{\rm CE} = 5.0 V$	50				
∆r _e •	$l_{\rm C} = 10-100-1000\mu A,$ $V_{\rm CE} = 5.0V$	}	1.0		Ω	
BVCBO	$I_{\rm C} = 10\mu A$, $I_{\rm E} = 0$	25			v	
BVCEO	$l_{\rm B} = 0, l_{\rm C} = 10.0 \mu {\rm A}$	25			v	
BVCC	$l_{CC} = 10\mu A$	45			v	
BVEBO	$I_{\rm E} = 10\mu A$, $I_{\rm C} = 0$	6.5			V	
VCE (sat)	$l_{\rm C}$ = 1.0mA, $l_{\rm B}$ = 0.1mA			0.5	v	
V _{BE (on)}	$I_{\rm C} = 10 \mu A, V_{\rm CE} = 5.0 V$	`		0.7	V	
I _{CBO}	$I_E = 0, V_{CB} = 80\%$ rated BV_{CBO}	}		0.2	nA	
l_{CBO} (+150°C)	1 _E = 0, V _{CB} = 80% rated BV _{CBO}	}		0.2	μΑ	
IEBO	$I_{C} = 0, V_{EB} = 5.0V$,		0.2	nA	
ICC	$V_{CC} = \pm 45V$			0.5	nA	
Сов	$I_{\rm E} = 0, V_{\rm CB} = 5.0 V$			2	pF	
CEB	$I_{\rm C} = 0, V_{\rm EB} = 0.5 V$		3		pF	
CTE	$I_{\rm C} = 0, V_{\rm FB} = 0.5 V$			2	pF	
f ₇	$I_{C} = 1.0 mA$, $V_{CE} = 5.0 V$	200			MHz	
f ₇	$I_{\rm C} = 200 \mu A, V_{\rm CE} = 5.0 V$	100			MHz	
NF	$I_{C} = 100\mu A$, $V_{CE} = 5.0V$ BW = 200Hz, $R_{G} = 10k\Omega$	}		3	dB	
Price (1-99)			5.00		s	
*∆r _e is a deviation	n from the ideal r _e and detern	nines the log c	onformanc	e.		

DUAL PNP TRANSISTORS AD820 SERIES

GENERAL DESCRIPTION

Types AD820, AD821 and AD822 are small signal, dual monolithic PNP transistors which are primarily designed to provide high gain over wide, collector current ranges with high breakdown voltages, close matching and predictable temperature drift.

Through precise, linear IC production processes coupled with advanced silicon nitride passivation techniques, it is now possible to routinely fabricate these dual monolithic PNP transistors with voltage breakdowns in excess of 60V; voltage offsets of 0.5 mV; temperature drifts of $< 2.5 \mu \text{V/}^{\circ}$ C and $I_{B_1} - I_{B_2}$ drift $< 0.3 \text{nA/}^{\circ}$ C. Additionally, gain linearity is evident from $10 \mu \text{A}$ to 1.0mA of collector current.

The AD820 series is designed for operation over full military temperature range from -55°C to +125°C, and is offered in hermetically-sealed TO-71 packages (TO-78 is optional).



$ \begin{array}{c c} V_{BE_{1}} - V_{BE_{2}} & i_{C} = \\ & V_{Q} \\ \hline \\ \frac{\Delta(V_{BE_{1}} - V_{BE_{2}})}{\Delta T} & i_{C} = \\ \hline \\ \hline \\ \hline \\ \frac{1}{\Delta T} & 1_{B_{2}} & i_{C} = \\ \hline \\ \frac{\Delta(I_{B_{1}} - I_{B_{2}})}{\Delta T} & i_{C} = \\ \hline \\ \hline \\ \frac{1}{\Delta T} & T_{A} \\ \hline \\ h_{FE_{1}} / h_{FE_{2}} & i_{C} = \\ \hline \\$	$ \begin{array}{c} 0\mu A \text{ to } 5.0\text{mA} \\ F = 5.0\text{V} \\ 0\mu A, V_{CE} = 5.0\text{V} \\ 0\mu A, V_{CE} = 5.0\text{V} \\ \mu A, V_{CE} = 5.0\text{V} \\ 0\mu A, V_{CE} = 5.0\text{V} \\ = -55^{\circ}\text{C to} + 125^{\circ}\text{C} \\ 0\mu A, V_{CE} = 5.0\text{V} \\ = -55^{\circ}\text{C to} + 125^{\circ}\text{C} \\ 0\mu A, V_{CE} = 5.0\text{V} \\ \end{array} \right\} $	max max max max tsp 25°C, unle Limit min max min max min max min max min max min	5.0 20 10 ss otherwise AD820 100 - 100 30 0.5 0.7 25	1.0 5 10 0.5 5 noted) AD821 150 600 150 50 0.5 50 0.5 0.7	0.5 2.5 5.0 0.3 5 AD822 200 600 200 600 200 600 200 75 0.5 0.7	mV μV/°C nA nA/°C %6 Units
$\frac{\Delta(V_{BE_1} - V_{BE_2})}{\Delta T} I_C = \frac{1}{\Delta T} T_A$ $\frac{I_{B_1} - I_{B_2}}{\Delta T} I_C = \frac{1}{\Delta T} T_A$ $\frac{I_{B_1} - I_{B_2}}{\Delta T} I_C = \frac{1}{\Delta T} T_A$ $\frac{I_{EECTRICAL CHARACC}}{ELECTRICAL CHARACC}$ $\frac{Parameter}{I_C} I_C = \frac{1}{\Delta T} I_C = \frac{1}{\Delta T}$ $\frac{I_FE}{I_C} I_C = \frac{1}{\Delta T} I_C = \frac{1}{\Delta T}$ $\frac{I_FE}{I_C} I_C = \frac{1}{\Delta T}$	$ \begin{array}{l} 0\mu A, V_{CE} = 5 \ 0V \\ z = -55^{\circ}C \ to + 125^{\circ}C \\ 0\mu A, V_{CE} = 5.0V \\ 0\mu A, V_{CE} = 5.0V \\ z = -55^{\circ}C \ to + 125^{\circ}C \\ z = -55^{\circ}C \ to + 125^{\circ}C \\ 0\mu A, V_{CE} = 5.0V \\ \hline \end{array} \right\} $	max max typ 25°C, unle Limit min max min max min max min max min min	20 10 ss otherwise AD820 100 	5 10 0.5 5 noted) AD821 150 600 150 600 150 50 0.5 0.7	2.5 5.0 0.3 5 AD822 200 600 200 600 200 75 0.5 0.7	μV/°C nA nA/°C %6 Units - - - - - - - - - - - - -
$ \begin{array}{c} I_{B_1} - I_{B_2} & I_C = \\ \\ \hline \Delta (I_{B_1} - I_{B_2}) & I_C = \\ \hline \Delta T & T_A \\ \hline \\ \hline \\ h_{FE_1} / h_{FE_2} & I_C = \\ \end{array} \\ \hline	$\begin{array}{l} 0\mu A, V_{CF} = 5.0V \\ 0\mu A, V_{CF} = 5.0V \\ = -55^{\circ}C \ to + 125^{\circ}C \\ 0\mu A, V_{CL} = 5.0V \\ \hline \\ 0\mu A, V_{CL} = 5.0V \\ \hline \\ $	max max typ 25°C, unle Limit min max min max min max min max min max min	10 ss otherwise AD820 100 - 100 30 0.5 0.7	10 0,5 5 noted) AD821 150 600 150 600 150 50 0.5 0,7	5.0 0.3 5 AD822 200 600 200 600 200 75 0.5 0.7	nA nA/ ^o C % Units - - - - - - - V V V
$\begin{array}{c} \Delta(I_{B_1} - I_{B_2}) & I_C = \\ \hline & & I_C \\ \hline & & & I_C \\ \hline & & & & I_C \\ \hline & & & & & I_C \\ \hline & & & & & & & I_C \\ \hline & & & & & & & I_C \\ \hline & & & & & & & I_C \\ \hline & & & & & & & I_C \\ \hline & & & & & & & I_C \\ \hline & & & & & & & I_C \\ \hline & & & & & & & I_C \\ \hline & & & & & & & & & I_C \\ \hline & & & & & & & & & I_C \\ \hline & & & & & & & & & I_C \\ \hline & & & & & & & & & I_C \\ \hline & & & & & & & & & I_C \\ \hline & & & & & & & & & I_C \\ \hline & & & & & & & & & I_C \\ \hline & & & & & & & & & I_C \\ \hline & & & & & & & & & I_C \\ \hline & & & & & & & & & I_C \\ \hline & & & & & & & & & I_C \\ \hline & & & & & & & & & I_C \\ \hline & & & & & & & & & I_C \\ \hline & & & & & & & & & I_C \\ \hline & & & & & & & & I_C \\ \hline & & & & & & & & I_C \\ \hline & & & & & & & & I_C \\ \hline & & & & & & & & I_C \\ \hline & & & & & & & & I_C \\ \hline & & & & & & & I_C \\ \hline & & & & & & & I_C \\ \hline & & & & & & & I_C \\ \hline & & & & & & & I_C \\ \hline & & & & & & & I_C \\ \hline & & & & & & & I_C \\ \hline & & & & & & I_C \\ \hline & & & & & & I_C \\ \hline & & & & & & I_C \\ \hline & & & & & & I_C \\ \hline & & & & & & I_C \\ \hline & & & & & & I_C \\ \hline & & & & & & I_C \\ \hline & & & & & & I_C \\ \hline & & & & & & I_C \\ \hline & & & & & & I_C \\ \hline & $	$ \begin{array}{l} 0\mu A, V_{CE} = 5.0V \\ = -55^{\circ}C \ to + 125^{\circ}C \\ 0\mu A, V_{CL} = 5^{\circ}0V \\ \hline \end{array} \right\} \\ 0\mu A, V_{CL} = 5^{\circ}0V \\ \hline \end{array} \\ \hline \begin{array}{l} \hline \end{array} \\ \hline \begin{array}{l} \hline \end{array} \\ \hline \end{array} $ \\ \hline \end{array} \\ \\ \hline \end{array} \\ \hline \end{array} \\ \hline \end{array} \\ \hline \end{array} \\ \hline \end{array} \\ \hline \end{array} \\ \hline \end{array} \\ \hline \end{array} \\ \hline \end{array} \\ \hline \end{array} \\ \hline \end{array} \\ \hline \end{array} \\ \hline \end{array} \\ \hline \end{array} \\ \hline \\ \hline \end{array} \\ \hline \\ \hline \end{array} \\ \hline \end{array} \\ \hline \\ \hline \end{array} \\ \hline \end{array} \\ \hline \\ \hline \\ \hline \end{array} \\ \\ \hline \end{array} \\ \hline \end{array} \\ \hline \\ \hline \\ \\ \hline \\ \\ \hline \\ \\ \\ \\ \\ \\ \\	max TSP 25°C, unle Limit min max min max min max min max min max min max	10 ss otherwise AD820 100 - 100 30 0.5 0.7	0.5 5 noted) AD821 150 600 150 50 0.5 0.5 0.7	0.3 5 AD822 200 600 200 600 200 75 0.5 0.7	nA/°C %
$ \begin{array}{c c} h_{FE_1}/h_{FE_2} & I_C = \\ \hline \\ \hline \hline \\ \hline$	$\begin{array}{l} 0\mu A, V_{CL} = 5.0V\\ \hline \textbf{TERISTICS} (T_A = +2\\ \hline \textbf{Test Condition}\\ 0\mu A, V_{CE} = 5.0V\\ 00\mu A, V_{CE} = 5.0V\\ 0.0mA, V_{CE} = 5.0V\\ 0.0mA, I_B = 0.1mA\\ 0\mu A, V_{CE} = 5.0V\\ 0\mu A, I_E = 0\\ 0, I_C = 100\mu A\\ \end{array}$	DP 25°C, unle Limit min max min max min max min max min	10 ss otherwise AD820 100 - 100 30 0.5 0.7 25	5 noted) AD821 150 600 150 600 150 50 0.5 0.7	5 AD822 200 600 200 600 200 75 0.5 0.7	%
ELECTRICAL CHARAC Parameter hFE IC = NFE IC = VCE (sat) IC = VCE (sat) IC = VBE (on) IC = BVCBO IC = BVCBO IE = ICBO IE = ICBO IE = IEBO IC =	TERISTICS ($T_A = +2$ Test Condition $0\mu A, V_{CE} = 5.0V$ $00\mu A, V_{CE} = 5.0V$ $0mA, V_{CE} = 5.0V$ $0mA, V_{CE} = 5.0V$ $0mA, I_B = 0.1mA$ $0\mu A, V_{CE} = 5.0V$ $0\mu A, I_E = 0$ $0, I_C = 100\mu A$	25°C, unle Limit min max min max min max max min max	ss otherwise AD820 100 - 100 30 0.5 0.7 25	noted) AD821 150 600 150 600 150 50 0.5 0.7	AD822 200 600 200 600 200 75 0.5 0.7	Units V V V
Parameter h_{FE} $I_C = 1$ V_{CE} (sat) $I_C = 1$ V_{CE} (sat) $I_C = 1$ V_{BE} (on) $I_C = 1$ BV_{CBO} $I_C = 1$ BV_{CEO} $I_B = 1$ BV_{CBO} $I_E = 1$ I_{CBO} (+150°C) $I_E = 4$ I_{CBO} (+150°C) $I_E = 4$ I_{CBO} (+150°C) $I_E = 4$	Test Condition $0\mu A, V_{CE} = 5.0V$ $00\mu A, V_{CE} = 5.0V$.0mA, $V_{CE} = 5.0V$.0mA, $V_{CE} = 5.0V$.0mA, $I_B = 0.1mA$.0\mu A, $V_{CE} = 5.0V$.0mA, $I_B = 0.1mA$.0\mu A, $V_{CE} = 5.0V$.0mA, $I_E = 0.0V$.0mA, $I_E = 0.0V$.0mA, $I_E = 0.0V$	Limit min max min max min max max min	AD820 100 - 100 - 100 30 0.5 0.7	AD821 150 600 150 600 150 50 0.5 0.7	AD822 200 600 200 600 200 75 0.5 0.7	Units V V
$ \begin{split} h_{FE} & _{C} = \\ h_{FE} & (-55^\circ C) & _{C} = \\ V_{CE} & (sat) & _{C} = \\ V_{CE} & (sat) & _{C} = \\ V_{BE} & (on) & _{C} = \\ BV_{CBO} & _{C} = \\ BV_{CBO} & _{C} = \\ BV_{CEO} & _{B} = \\ BV_{CBO} & _{E} = \\ BV_{EBO} & _{E} = \\ _{CBO} & _{E} = \\ _{CBO} & (+150^\circ C) & _{E} = \\ B^{V} \\ _{CBO} & _{C} = \\ B^{V} \\ _{CBO} $	$ \begin{array}{l} 0\mu A, V_{CE} = 5.0V \\ 00\mu A, V_{CE} = 5.0V \\ .0mA, V_{CE} = 5.0V \\ .0mA, V_{CE} = 5.0V \\ .0mA, I_B = 0.1mA \\ 0\mu A, V_{CF} = 5.0V \\ 0\mu A, I_E = 0 \\ 0, I_C = 100\mu A \\ .0mA \end{array} $	min max min max min max max min min	100 	150 600 150 600 150 50 0.5 0.7	200 600 200 600 200 75 0.5 0.7	
hFE IC VCE (sat) VCE IC BVCBO IC BVCC ICC BVEBO IE ICBO IE ICBO IE BY ICBO IEBO IC	$\left.\begin{array}{c} 00\mu A, V_{CE} = 5.0V\\ 00\mu A, V_{CE} = 5.0V\\ 0\mu A, V_{CE} = 5.0V\\ 0\mu A, V_{CE} = 5.0V\\ 00\mu A, I_B = 0.1mA\\ 0\mu A, V_{CE} = 5.0V\\ 0\mu A, I_E = 0\\ 0, I_C = 100\mu A\\ 100\mu A\end{array}\right.$	max min max min max max max min	100 100 30 0.5 0.7	600 150 600 150 50 0.5 0.7	600 200 600 200 75 0.5 0.7	 V V
$ \begin{split} h_{FE} & I_C = i \\ h_{FE} & I_C = i \\ h_{FE} & (-55^\circ C) & I_C = i \\ V_{CE} & (sat) & I_C = i \\ V_{BE} & (on) & I_C = i \\ BV_{CBO} & I_C = i \\ BV_{CEO} & I_B = i \\ BV_{CEO} & I_B = i \\ BV_{EBO} & I_F = i \\ I_{CBO} & I_E = i \\ I_{CBO} & (+150^\circ C) & I_E = i \\ BV_{EBO} & I_C = i$	$00\mu A, V_{CE} = 5.0V$ $.0mA, V_{CE} = 5.0V$ $0\mu A, V_{CE} = 5.0V$ $.0mA, I_B = 0.1mA$ $0\mu A, V_{CE} = 5.0V$ $0\mu A, I_E = 0$ $0, I_C = 100\mu A$	min max min min max max min	100 100 30 0.5 0.7	150 600 150 50 0.5 0,7	200 600 200 75 0.5 0.7	 V V
hFE IC hFE IC hFE IC hFE IC hFE IC hFE IC VCE IC VBE IC BVCBO IC BVCEO IB BVCC ICC BVEBO IE ICBO IE ICBO IE ICBO IE ICBO IE ICBO IC	$\begin{array}{c} 0.0\mu A, \ V_{CE} = 5.0V \\ 0.0mA, \ V_{CE} = 5.0V \\ 0.0mA, \ I_B = 0.1mA \\ 0.0mA, \ I_B = 0.1mA \\ 0.0\mu A, \ V_{CE} = 5.0V \\ 0.0\mu A, \ I_E = 0 \\ 0, \ I_C = 100\mu A \\ 0.0mA \end{array}$	max min min max max min	100 30 0.5 0.7	600 150 50 0.5 0.7	600 200 75 0.5 0.7	
$ \begin{array}{cccc} h_{FE} & l_{C} = \\ h_{FE} & (-55^{\circ}C) & l_{C} = \\ V_{CE} & (sat) & l_{C} = \\ V_{BE} & (on) & l_{C} = \\ BV_{CBO} & l_{C} = \\ BV_{CC} & l_{C} = \\ BV_{CC} & l_{C} = \\ BV_{EBO} & l_{E} = \\ l_{CBO} & (+150^{\circ}C) & l_{E} = \\ BV_{EBO} & l_{C} = \\ BV_{EBO} & l_{C} = \\ \end{array} $	$0mA. V_{CE} = 5.0V$ $0\mu A. V_{CE} = 5.0V$ $0mA. I_B = 0.1mA$ $0\mu A. V_{CE} = 5.0V$ $0\mu A. I_E = 0$ $0, I_C = 100\mu A$	min min max max min	100 30 0.5 0.7	150 50 0.5 0.7	200 75 0.5 0.7	
$h_{FE} (-55^{\circ}C) \qquad l_{C} = \\ V_{CE} (_{3at}) \qquad l_{C} = \\ V_{BE} (_{0n}) \qquad l_{C} = \\ BV_{CBO} \qquad l_{C} = \\ BV_{CEO} \qquad l_{B} = (\\ BV_{CC} \qquad l_{CC} = \\ BV_{CBO} \qquad l_{E} = \\ l_{CBO} \qquad l_{E} = \\ l_{CBO} (+150^{\circ}C) \qquad l_{E} = (\\ BV_{CBO} \qquad l_{C} = \\ BV_{CBO} \qquad l_{C} = (100^{\circ}C)) \qquad l_{C} = (100^{\circ}C) \\ BV_{CBO} \qquad l_{C} = (100^{\circ}C)) \qquad l_{C} = (100^{\circ}C) \\ BV_{CBO} \qquad l_{C} = (100^{\circ}C)) \qquad l_{C} = (100^{\circ}C) \\ BV_{CBO} \qquad l_{C} = (100^{\circ}C)) \qquad l_{C} = (100^{\circ}C) \\ BV_{CBO} \qquad l_{C} = (100^{\circ}C)) \qquad l_{C} = (100^{\circ}C) \\ BV_{CBO} \qquad l_{C} = (100^{\circ}C)) \qquad l_{C} = (100^{\circ}C) \\ BV_{CBO} \qquad l_{C} = (100^{\circ}C)) \qquad l_{C} = (100^{\circ}C) \\ BV_{CBO} \qquad l_{C} = (100^{\circ}C)) \qquad l_{C} = (100^{\circ}C) \\ BV_{CBO} \qquad l_{C} = (100^{\circ}C)) \qquad l_{C} = (100^{\circ}C) \\ BV_{CBO} \qquad l_{C} = (100^{\circ}C) \\ BV_{CBO} \qquad l_{C} = (100^{\circ}C) \\ BV_{CBO} \qquad l_{C} = (100^{\circ}C)) \\ BV_{CBO} \qquad l_{C} = (100^{\circ}C) \\ BV_{C} \qquad l_{C} = (100$	$0\mu A$, $V_{CE} = 5.0V$ $.0mA$, $I_B = 0.1mA$ $0\mu A$, $V_{CE} = 5.0V$ $0\mu A$, $I_E = 0$ 0 , $I_C = 100\mu A$	min max max min	30 0.5 0.7	50 0.5 0.7	75 0.5 0.7	v v
$V_{CE} (sat) \qquad l_C =$ $V_{BE} (on) \qquad l_C =$ $BV_{CBO} \qquad l_C =$ $BV_{CEO} \qquad l_B = ($ $BV_{CC} \qquad l_{CC} =$ $BV_{EBO} \qquad l_E =$ $l_{CBO} (+150^{\circ}C) \qquad l_E = ($ $BV_{EBO} \qquad l_C =$	$0mA, I_B = 0.1mA$ $0\mu A, V_{CF} = 5.0V$ $0\mu A, I_E = 0$ $0, I_C = 100\mu A$	max max min	0.5	0.5	0.5 0.7	v v
VBE (on) IC = BVCBO IC = BVCEO IB = (BVCC ICC = BVEBO IE = ICBO (+150°C) IE = (BY BN ICBO IC =	$0\mu A$, $V_{CF} = 5.0V$ $0\mu A$, $I_E = 0$ 0 , $I_C = 100\mu A$	max min	0.7	0.7	0.7	v
$BV_{CBO} \qquad I_C =$ $BV_{CEO} \qquad I_B = ($ $BV_{CC} \qquad I_{CC} =$ $BV_{EBO} \qquad I_E =$ $I_{CBO} \qquad I_E = ($ $BV_{CBO} \qquad I_E = ($ $BV_{CO} \qquad I_E = ($ $BV_{$	$0\mu A$, $I_E = 0$), $I_C = 100\mu A$	min	25			
$BV_{CEO} I_B = (I_B + I_B) = (I_B + I_B) = (I_B + I_B) = (I_C + I_B)$	$I_{\rm C} = 100 \mu {\rm A}$	min	23	45	60	v
$BV_{CC} = 1_{CC} = 1_{CC} = 1_{CBO} = 1_{C} = $	10		25	45	60	v
	τομΑ	min	30	60	100	v
$I_{CBO} \qquad I_E = (B)$ $I_{CBO} (+150^{\circ}C) \qquad I_E = (B)$ $I_E = (B)$ $I_E = (C)$	$0\mu A$, $I_{C} = 0$	min	6.5	6.5	6.5	v
I_{CBO} (+150°C) $I_E = 0$ BV I_{EBO} $I_C = 0$	$\left. \begin{array}{l} V_{CB} = 80\% \text{ rated} \\ CBO \end{array} \right\}$	max	0.2	0.2	0.2	nA
IEBO IC =	$\left. \begin{array}{c} V_{CB} = 80\% \text{ rated} \\ V_{CBO} \end{array} \right\}$	max	0.2	0.2	0.2	μΑ
	$V_{EB} = 4.0V$	max	0.2	0.2	0.2	nA
Ic ₁ c ₂ V _{CC}	= 80% rated BV _{CBO}	max	0.5	0.5	0.5	nA
Сов 1н. =	$V_{CB} = 5.0V$	max	2,0	2.0	2.5	рF
C _{TE} I _C =	$V_{\rm FB} = 0.5 \rm V$	max	2.0	2.0	2.0	p۲
C _{CC} V _{CC}	= 0	max	2.0	2.0	2.0	pF
f ₇ I _C =	$0mA, V_{CE} = 5.0V$	min		200	200	MHz
f ₇ l _C =	$200\mu A, V_{CE} = 5.0V$	min		100	100	MHz
NF I _C = V _{CE}	100μA, = 5.0V, BW = 200Hz	typ		3.0	2.0	dB

MECHANICAL OUTLINES ANALOG PRODUCTS

MODULE TERMINAL



SOCKET TERMINAL



 I.8
 B-1 AC1037

 I.8
 Image: Constraint of the second secon

GENERAL NOTES:

- All pin diagrams are terminal views. Grids are on 0.1" spacing for reference only.
- Pin designations are for reference only; in general designations are silk screened on the sockets.
- Pins are gold plated, half-hard brass, 0.04" in diameter, 0.2" minimum length.
- Mating socket numbers are shown with each pinning diagram. Socket outlines are shown on page 171.
- Socket material is NEMA grade G-10 glass epoxy, 0.093" thick. Terminals are 0.5" maximum length.
- All dimensions shown in inches.

B PACKAGE MODEL 171





F, FA PACKAGES

*H-3

MODELS 41, 119, 120, 146, 153, 163, 183, 184, 233, 234, 260, 261, 350, 422, 426, 428, 429, 433, 434, 602, 603, 605, 755, 756



O VAC

Model 274 "HI IN #1" and "Gain" pins are detachable.

+VsC

+Vso

M PACKAGE MODELS 40, 43, 118, 165, 751



N PACKAGE **MODELS 46, 50**



Q, QB, QC PACKAGES

MODELS B100, 42, 44, 45, 47, 48, 180, 432, 752

Q-1. QB-1*, QC-1 AC 1003

+VsO

-VsO

+VsO

-VsO

EINO



*Model 42 (QB-1) common pin may be missing. No connecting required.



QC-2 AC 1032

al_+V _s O_
сомо
-Vs0
ουτο
zo

MODELS 210, 211

R PACKAGE



W, WA PACKAGES MODELS 231, 310, 311



MODEL 425 OUTLINE



NOTES:

1. Model 425 gain adjust pot in series with X input.

2. Mating socket supplied with unit (ADI part no. 60-42820).

MPD POWER SUPPLIES

MPD 15/100A USE MOUNTING CARD AC 2714A



MPD 15/300A USE MOUNTING CARD AC 4482



USE MOUNTING CARD AC 2714B 150V - (MPD 5 150 ONLY) LEAD 4 KEEP SHORT OR SHIELD 5K WW \$ \$ T .040 DIA. 1 0-= = -.20 TYP. 115V AC LINE IN ±.015 -. 4 0-1.00 \$ 0 1,09 1.09 4 40 INSERT (4 PLACES) 1.34 -- 1.34 ---.20 3.19 <u>+.015</u>

MPD 5-150A and MPD 5/750A

MOUNTING CARDS

AC 2714 A/B



AC 4482



194 MECHANICAL OUTLINES

POWER SUPPLY MANIFOLD



OPERATIONAL AMPLIFIER MANIFOLD MODEL 194





MODEL 79P CERMET BALANCE POT

Analog Devices has selected the Beckman Helitrim Model 79P as suitable for most applications and carries this balance pot in stock. We offer this service since you may find it more economical or convenient to order your balance pots directly from Analog Devices along with your amplifiers. The identical pots are also available from Beckman or their stocking distributors.



SPECIFICATIONS

Tempco, max Input voltage, max Power rating End resistance, max Resolution Ambient temperature range Adjustment turns, nominal 15 Sealing (immersion test) Temperature cycling Humidity cycling Shock Vibration Load life at 0.75 watts Rotational life ANALOG DEVICES PART NUMBER 79PR1k 79PR2k 79PR5k 79PR10k 79PR50k 79PR100k 79PR250k

±100ppm (0 to -250ppm for 250k ohms) 200VDC or RMS 0.75 watts at $+25^{\circ}$ C, derated to 0 watts at $+105^{\circ}C$ 2 ohms essentially infinite -55°C to +105°C meets MIL-R-22097C 5 cycles -55° C to $+105^{\circ}$ C 5 cycles 50G's 10 to 500kz, 10G's 1,000 hrs. at +25°C 200 cycles RESISTANCE PRICE OHMS 1k ±10% 2k ±10% 5k ±10% (1 - 9)\$3.00 10k ±10% (10 - 99)\$2.75 50k ±10% (100-249) \$2.50 100k ±10% 250k ±10%



196 MECHANICAL OUTLINES

MECHANICAL OUTLINES CONVERTER PRODUCTS

GENERAL NOTES:

- All pinning diagrams are terminal views on 0.1" grids. All modules are 0.4" in height unless otherwise noted.
- All possible pin locations are shown, even though pins are installed in only a portion of these locations for any given product.

PACKAGE STYLES

- Unless otherwise noted, all module pins are gold plated rodar (MIL-G-45 204), 0.02" in diameter, and 0.2" minimum length.
- All models constructed on printed circuit boards are supplied with mating edge connectors.
- All dimensions shown in inches.

C-3, CA-3



*Pin No. 29 for model MPX-8A. (Functional pin also used as key)



Note: Pins on SHA-2 are 0.040" dia. gold-plated brass.







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 270

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C-5



Note: Pin 1 is identified with a mark on the top surface and with a colored glass bead sealer on the bottom.



MOUNTING BOARDS

MODEL NO.	MOUNTING BOARD	BOARD DIMENSIONS	PRICE (1-9)
		A B	
ADC-I	AC1500	4½" x 6"	\$60.
ADC-QM	AC4451	$4\frac{1}{2}'' \times 3\frac{3}{4}''$	\$25.
ADC-QU	AC4451	$4\frac{1}{2}'' \times 3\frac{3}{4}''$	\$25.
ADC-8S	AC4751	4½" x 6"	\$25.
ADC-10Z	AC1504	4½" x 6"	\$25.
ADC-12QZ	AC1548	4½" x 6"	\$25.
ADC1100	AC1550	4½" x 6"	\$25.
ADC1103	AC1549	4 ¹ / ₂ " x 6"	\$25.
DAC-10Z	AC4102	see outline	\$15.
DAC-12QZ	AC4516	$4\frac{1}{2}'' \times 3\frac{3}{4}''$	\$40.
DAC-QM	AC4494	$4\frac{1}{2}$ x $3\frac{3}{4}$	\$40.
DAC-QS	AC4516	$4\frac{1}{2}'' \times 3\frac{3}{4}''$	\$40.
DAC-M	AC4102	see outline	\$15.
MDA-10Z	AC4102	see outline	\$15.
MDA-10F	AC4159	4½" x 2¼"	\$15.
MDA-11MF	AC1509	4½" x 6"	\$25.
MPX-8A	AC6160	4½" x 2½"	\$40.
SHA-1A	AC4102	see outline	\$15.
SHA-2A	AC1503	4½" x 2¼"	\$35.
SHA-3	AC4102	see outline	\$15.
SHA-4	AC4102	see outline	\$15.
SHA-5	AC4102	see outline	\$15.
SHA-6	AC1508	4½" x 6"	\$15.



NOTES:

- 1. Material: 1/16" G-10 glass epoxy per MIL-D-139, 2 oz. copper clad with solder plating.
- Edge connectors gold plated per MIL-G-45204.
- 2. Mating cinch connector supplied with mounting board.
- 3. Trim adjustment pots mounted on boards (when applicable).

MECHANICAL OUTLINES DIGITAL PANEL METERS

MODEL AD2001

OVERALL DIMENSIONS



MODELS AD2002, AD2003, AD2004, AD2010



OVERALL DIMENSIONS

MODEL	D ₁	D ₂
AD2002	1.520	2.020
AD2003	2.020	2.800
AD2004	2.520	3.300
AD2010	0.750	1.400

ALL DIMENSIONS ARE IN INCHES

MECHANICAL OUTLINES LINEAR INTEGRATED CIRCUITS

CN2



TO-78













TO-99



TO-100















0.280



24 PIN MOLDED PACKAGE



MINI-DIP



TO-116 14 PIN



MP72



TO-87



24 PIN DIL



TO-116 16 PIN



BUSINESS GUIDE

The following minimal procedures are designed to make it as convenient as possible for you to conduct business with us. Any questions regarding products, applications or service can be referred to any office listed in the Worldwide Service Directory or to our Norwood headquarters.

PLACING AN ORDER

When placing an order please provide specific information regarding model type, number, option designations, quantity, ship-to and bill-to address. Prices quoted are list and do not include applicable taxes, customs or shipping charges. Unless otherwise requested, all shipments are FOB, factory.

ORDERING INSIDE THE UNITED STATES: Orders may be placed with our local representative in your area, or directly with Norwood. Orders may be telephoned, sent via TELEX or TWX or mailed. Orders are acknowledged upon receipt; billing and delivery information is included.

ORDERING OUTSIDE THE UNITED STATES: All orders should be placed with the local representative serving your country. Where there is no local representation, orders may be forwarded directly to Norwood. TELEX facilities are available for such international requests.

RETURNS AND WARRANTY SERVICE

Product warranties are uniform worldwide. Defective units being returned for servicing should be accompanied by a statement outlining the nature of the failure and the application in which the failure occurred. Upon receipt of the defective unit, notices will be issued, when applicable, regarding warranty status, cost for repair, or nonrepairability. Applicable credits are issued immediately, and replacement units scheduled. Repairable units out of warranty will be serviced, upon customer authorization, on a quoted time/material charge basis. Where practical, we request that all defective units, serviceable or not, be returned so we may include them in our on-going product reliability program.

RETURNS INSIDE THE UNITED STATES: All defective units should be sent to our Norwood location to the attention of our "Returns Department." Consultation with the local representative, although suggested, is not required.

RETURNS OUTSIDE THE UNITED STATES: All defective units should be brought to the attention of the local representative who will instruct you as to the disposition of the unit. For improved customer service, a complete repair depot is located in our Munich office; limited repair facilities are also located in England and Japan. From those countries not served by representatives, defective units should be forwarded directly to Norwood.

EVALUATION SAMPLES, SPECIAL SERVICES, PRICE OFFERS

To assist you in final product selection, we can make available, through our local representatives, evaluation samples of our products. However, offers for such samples, price promotions, and special services promoted by Analog Devices, Inc. through U.S.-based publications, are not necessarily available abroad in the same form.



LITERATURE

To assist you in understanding our products and how to use them we maintain an active technical communications program which produces many forms of documentation in addition to this comprehensive PRODUCT GUIDE. All of the material in our "library" has been prepared by our engineering and marketing staffs. The following summarizes the more popular literature offerings currently available. Please direct requests for this material by title to our Norwood headquarters, overseas representative offices, or European literature depot.

DATA SHEETS: All standard products are supported by detailed data sheets which provide specifications and all other information necessary to apply our products. Many data sheets also contain extensive supplementary application data. Order data sheets by model type and number. (Free)

ANALOG DIALOGUE: This international technical journal is published approximately six times per year and contains articles on state-of-the-art techniques, application notes, new product descriptions and a variety of other information about Analog Devices and the current technical thought. User articles are welcome. (Free)

ANALOG-DIGITAL CONVERSION HANDBOOK: This 400 page treatment of A/D and D/A conversion was prepared by the engineering staff of Analog Devices. Heavily applications oriented, this HANDBOOK explains what A/D and D/A converters are, what role they play in the data handling environment, how they are applied, and how they are specified. It contains more than 250 reference tables and illustrations and is written primarily for the practicing design engineer. U.S. \$3.95 or foreign currency equivalent.

APPLICATION NOTES: A limited quantity is in stock on the following subjects. Many of these appeared in trade magazines and in technical papers and seminars given by Analog Devices. High Performance Monolithic Instrumentation

Amplifier (AD520)

AD530, Complete Monolithic Multiplier/Divider Applying the AD504 Precision IC Operational Amplifier AD513, AD516 IC FET Input Operational Amplifiers AD503, AD506 IC FET Input Operational Amplifiers "Computational Module Stresses Applications Versatility,"

- ELECTRONICS reprint on Model 433 multifunction module.
- "New Applications Open Up for the Versatile Isolation Amplifier," ELECTRONICS reprint.
- ADC-I Dual Slope Integrating A/D Converter
- "The Multiplying D/A Converter," ELECTRONICS PRODUCTS reprint.
- Designing with µDAC Monolithic IC D/A Converter Components
- High Speed Versatile D/A Quad Current Switch Circuit Advantages of Chopper Stabilized Operational Amplifiers
- Designing with Chopper Stabilized Operational Amplifiers Design of Temperature Compensated Log Circuits Employ-
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- Understanding Multiplier/Divider Circuits
- "Applications for Instrumentation Amplifiers," ELECTRONICS PRODUCTS reprint
- "16-Bit Data Conversion," a two part article from ELECTRONICS
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- **17. HEADQUARTERS**

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WARRANTY

STANDARD TERMS: All Analog Devices, Inc. products are warranted against defects in workmanship, materials, and construction under normal use and service for a one year period from date of shipment, except that liability for defective components shall conform and be limited to the obligations of the original manufacturer's warranties covering these components. This warranty does not extend to any of our products which have been subjected to misuse, neglect, accident or improper installation or application. Nor shall it extend to products which have been repaired or altered outside of our factory. Analog Devices will repair or replace the defective products in accordance with its own best judgment.

EXCEPTION: Each new digital panel meter manufactured and/or sold by Analog Devices is warranted to be free from defects in material and workmanship for one year. Should a failure resulting from defects in material or workmanship occur within ninety (90) days after shipment, such failure will be repaired and the unit recalibrated and tested at no charge. Non-catastrophic failures resulting from misuse, neglect, accident or improper installation or application, will be repaired for a flat charge of \$25.00 during this period.

For a period from ninety (90) days to one year after shipment, non-catastrophic failures, regardless of cause, will be repaired at a flat charge of \$25.00.

WARRANTY SERVICE: For service under this warranty, please advise promptly the factory, or representative if outside the United States, of all pertinent details. Transportation charges covering return of defective products to our factory shall be at our expense if such products are determined to be defective within the limitations of this warranty.

Analog Devices, Inc. requests immediate notification for any claims arising from damage in transit in order to determine if carrier responsibility exists.

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